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*Published in:*

Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on

*Link to article, DOI:*

[10.1109/ISCAS.1998.704572](https://doi.org/10.1109/ISCAS.1998.704572)

*Publication date:*

1998

*Document Version*

Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

*Citation (APA):*

Bruun, E. (1998). Harmonic Distortion in CMOS Current Mirrors. In Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on (Vol. 1, pp. 567-570). IEEE. DOI: 10.1109/ISCAS.1998.704572

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# HARMONIC DISTORTION IN CMOS CURRENT MIRRORS

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## ABSTRACT

One of the origins of harmonic distortion in CMOS current mirrors is the inevitable mismatch between the MOS transistors involved. In this paper we examine both single current mirrors and complementary class AB current mirrors and develop an analytical model for the mismatch induced harmonic distortion. This analytical model is verified through simulations and is used for a discussion of the impact of mismatch on harmonic distortion properties of CMOS current mirrors. It is found that distortion levels somewhat below 1% can be attained by carefully matching the mirror transistors but ultra low distortion is not achievable with CMOS current mirrors.

## 1. INTRODUCTION

Most current mode circuits rely on current mirrors to produce multiple outputs. This is true both for continuous time circuits such as current conveyors [1] and for switched current circuits [2]. The current mirrors used to produce current mode output signals are normally not included in a feedback loop and this implies that any non-linearity of the current mirrors will directly enter into the transfer function of the conveyor or current processing circuit. In other words, the linearity of the current mirror itself is a fundamental limitation in current mode signal processing. The linearity of a CMOS current mirror is limited by the matching properties of the transistors in the mirror. Some of the current mirror mismatch can be attributed to mismatch in geometric sizes and in the transconductance parameter of the transistors. Using a standard Shichman-Hodges transistor model [3], this kind of mismatch appears as a constant factor to the output signal and, hence, does not introduce any non-linearity in a single current mirror. However, in a complementary class AB current mirror, differences in the current transfer ratio between the NMOS and PMOS current mirror introduce nonlinearities. Another source of mismatch is differences in the operating conditions of the current mirror transistors, in particular differences in the drain-source voltages of the input transistor and output transistor. This mismatch can be eliminated by proper circuit techniques (cascode) ensuring identical operating conditions for the two transistors [4] and will not be further dealt with in the present paper. Another important contribution to the mismatch comes from mismatch in threshold voltages, and this contribution is obviously non-linear as it appears in the quadratic term of the drain current expression. Therefore, this mismatch will give rise to a non-linear current mirror transfer function, both for a single current mirror and for a complementary current mirror. In the present paper we analyze the influence of mismatch in the geometries, transconductance parameters and threshold voltages on the distortion in both single

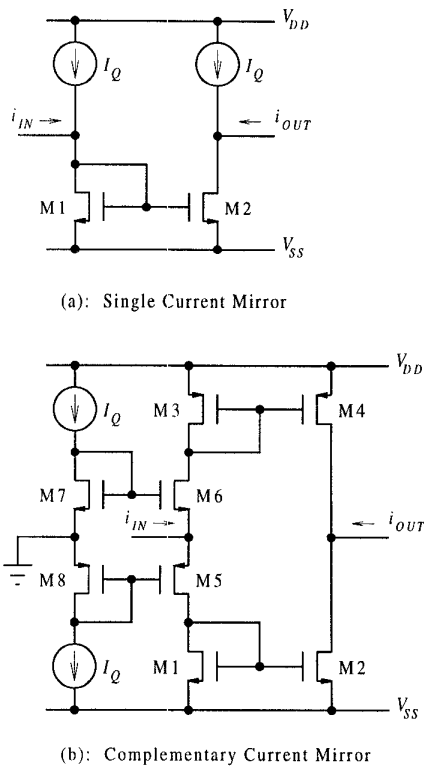


Figure 1. Simple CMOS current mirror.

current mirrors and complementary current mirrors. At high frequencies mismatch due to capacitive effects also cause distortion [5]. This problem falls outside the scope of the present paper.

## 2. CURRENT MIRROR MODEL

In order to simplify the analysis we consider just the simple current mirrors shown in fig. 1. The current mirrors are shown without the cascode transistors required to ensure equal drain voltages for the input and output transistors.

For the theoretical analysis we assume a Shichman-Hodges transistor model [3]. For a single current mirror with an input transistor

M1 and an output transistor M2 this leads to

$$\begin{aligned}
v_{GS} &= V_{T1} + \sqrt{\frac{2i_{D1}}{\beta_1(1 + \lambda_1 v_{DS1})}} \Rightarrow \\
i_{D2} &= \frac{\beta_2}{2} (v_{GS} - V_{T2})^2 (1 + \lambda_2 v_{DS2}) \\
&= \frac{\beta_2}{2} \left( V_{T1} - V_{T2} \right. \\
&\quad \left. + \sqrt{\frac{2i_{D1}}{\beta_1(1 + \lambda_1 v_{DS1})}} \right)^2 (1 + \lambda_2 v_{DS2}) \\
&= \frac{\beta_2}{2} \left( \frac{2i_{D1}}{\beta_1(1 + \lambda_1 v_{DS1})} + \Delta V_T^2 \right. \\
&\quad \left. - 2\Delta V_T \sqrt{\frac{2i_{D1}}{\beta_1(1 + \lambda_1 v_{DS1})}} \right) (1 + \lambda_2 v_{DS2}) \\
&\simeq \left( 1 + \frac{\Delta\beta}{\beta} \right) i_{D1} - \Delta V_T \sqrt{2\beta i_{D1}} \quad (1)
\end{aligned}$$

where we have used the conventional transistor parameter and voltage notation. We have introduced  $\Delta V_T = V_{T2} - V_{T1}$  and  $\Delta\beta = \beta_2 - \beta_1$  and for the last approximation we have assumed  $\Delta\beta \ll \beta = \beta_1 \simeq \beta_2$ ,  $\Delta V_T \ll \sqrt{\frac{2i_{D1}}{\beta_1}}$  and  $\lambda_1 v_{DS1} = \lambda_2 v_{DS2} \ll 1$ .

For the complementary current mirror shown in fig. 1(b) a similar equation applies to the current mirror M3-M4 and the input and output currents are given by  $i_{IN} = i_{D1} + i_{D3}$  and  $i_{OUT} = i_{D2} + i_{D4}$ . The distribution of  $i_{IN}$  between M1 and M3 depends on the transistors M5 and M6 and on the magnitude of the input current relative to the quiescent current  $I_Q$  in M1 and M3. For  $|i_{IN}| \gg I_Q$  we assume  $i_{IN} = i_{D1}$  for  $i_{IN} > 0$  and  $i_{IN} = i_{D3}$  for  $i_{IN} < 0$ . For small values of  $i_{IN}$  we assume  $i_{D1} = I_Q + i_{IN}/2$  and  $i_{D3} = -I_Q + i_{IN}/2$ . Also, we assume  $\beta = \beta_1 \simeq \beta_2 \simeq \beta_3 \simeq \beta_4$ .

### 3. DISTORTION ANALYSIS

Often when calculating harmonic distortion one would make a series expansion of the transfer function from the quiescent point, taking into account not only the first order (small signal) term but also higher order terms. This is perfectly feasible for the simple current mirror of fig. 1(a) assuming a quiescent current of  $I_Q$  and a signal current of  $i_{IN} = I_m \cos \omega t$ . However, it is not useful for the complementary current mirror with different transfer functions for positive and negative input signals. Instead, a five points analysis based on a calculation of the output signal  $i_{OUT}$  for input signals of  $I_m$ ,  $-I_m$ ,  $I_m/2$ ,  $-I_m/2$ , and 0 can be employed. This method was developed more than 60 years ago, [6, 7, 8] and has also been described in later standard textbooks, eg. [9, 10]. The method is illustrated in fig. 2. The output signals corresponding to the input signals  $I_m$ ,  $-I_m$ ,  $I_m/2$ ,  $-I_m/2$ , and 0 are denoted  $I_{max}$ ,  $I_{min}$ ,  $I_{1/2}$ ,  $I_{-1/2}$ , and  $I_0$ , respectively. It can be shown that the amplitudes  $B_1$ ,  $B_2$ ,  $B_3$ , and  $B_4$  of the first order, second order, third order and fourth order harmonics, respectively, in the output signal can be approximated by

$$B_1 = (I_{max} + I_{1/2} - I_{-1/2} - I_{min})/3 \quad (2)$$

$$B_2 = (I_{max} - 2I_0 + I_{min})/4 \quad (3)$$

$$B_3 = (I_{max} - 2I_{1/2} + 2I_{-1/2} - I_{min})/6 \quad (4)$$

$$B_4 = (I_{max} - 4I_{1/2} + 6I_0 - 4I_{-1/2} + I_{min})/12 \quad (5)$$

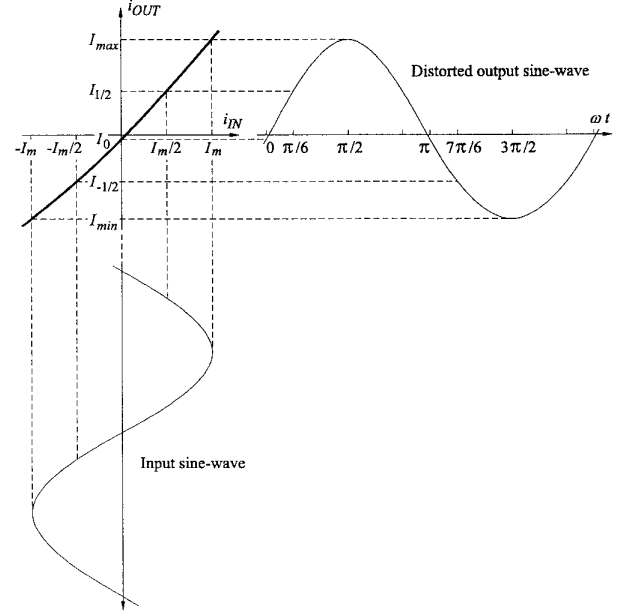


Figure 2. Current mirror input and output waveforms.

The distortion corresponding to the different harmonics is then obtained as

$$D_2 = B_2/B_1 \quad (6)$$

$$D_3 = B_3/B_1 \quad (7)$$

$$D_4 = B_4/B_1 \quad (8)$$

For the CMOS current mirrors shown in fig. 1 the second order and third order harmonic distortion has been calculated. The results of this analysis can be summarized as follows:

For the single current mirror we find:

$$\begin{aligned}
D_2 &= \frac{\sqrt{2}}{16} \Delta V_T \sqrt{\beta} \frac{I_m}{I_Q^{3/2}} \\
&= \frac{\sqrt{2}}{16} \Delta V_T \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} \frac{I_m}{I_Q^{3/2}}} \quad (9)
\end{aligned}$$

$$\begin{aligned}
D_3 &= \frac{\sqrt{2}}{64} \Delta V_T \sqrt{\beta} \frac{I_m^2}{I_Q^{5/2}} \\
&= \frac{\sqrt{2}}{64} \Delta V_T \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} \frac{I_m^2}{I_Q^{5/2}}} \quad (10)
\end{aligned}$$

For the complementary current mirror we find (for  $I_m \gg I_Q$ ):

$$\begin{aligned}
D_2 &= \frac{1}{4} \left( \frac{\Delta\beta_N}{\beta_N} - \frac{\Delta\beta_P}{\beta_P} \right) \left( 1 - 2 \frac{I_Q}{I_m} \right) \\
&\quad - \frac{\sqrt{2}}{4} \sqrt{\beta} (\Delta V_{TP} + \Delta V_{TN}) \frac{1}{\sqrt{I_m}} \left( 1 - 2 \sqrt{\frac{I_Q}{I_m}} \right)
\end{aligned}$$

$$= \frac{1}{4} \left( \frac{\Delta\beta_N}{\beta_N} - \frac{\Delta\beta_P}{\beta_P} \right) \left( 1 - 2 \frac{I_Q}{I_m} \right) - \frac{\sqrt{2}}{4} \sqrt{\mu_n C_{ox} \frac{W_1}{L_1}} (\Delta V_{TP} + \Delta V_{TN}) \frac{1}{\sqrt{I_m}} \left( 1 - 2 \sqrt{\frac{I_Q}{I_m}} \right) \quad (11)$$

$$D_3 = \frac{2 - \sqrt{2}}{6} \sqrt{\beta} (\Delta V_{TN} - \Delta V_{TP}) \frac{1}{\sqrt{I_m}} = \frac{2 - \sqrt{2}}{6} \sqrt{\mu_n C_{ox} \frac{W_1}{L_1}} (\Delta V_{TN} - \Delta V_{TP}) \frac{1}{\sqrt{I_m}} \quad (12)$$

#### 4. DISCUSSION

Examining first the single current mirror we see as expected that the distortion is caused only by threshold voltage mismatch and not by gain errors. Also, we find that the distortion is linearly related to the threshold voltage and increases with increasing signal amplitude relative to the quiescent current. Apparently, the second harmonic  $D_2$  is much larger than the third harmonic  $D_3$ . Obviously, for this type of current mirror distortion can be reduced by using a large quiescent current relative to the signal swing and by using long transistors. This will lead to a fairly large effective gate voltage, so the design consideration for minimum distortion will be to bias the current mirror to the maximum quiescent input voltage which can be used in the system. This is ultimately limited by the supply voltage. In other words, low distortion requires high supply voltage and high quiescent current, i.e. large power consumption. In order to reduce  $\Delta V_T$ , large geometry transistors can be employed.

For the complementary current mirror we see that a second harmonic is generated both by mismatches in  $\beta$  and by mismatches in  $V_T$  whereas the third harmonic is only caused by threshold voltage mismatch. We see that the distortion caused by mismatch in  $\beta$  (i.e. in transistor geometries and transconductance parameters) is only weakly signal dependent (for  $I_m \gg I_Q$ ) and can be minimized only by a careful matching of the transistors. The distortion caused by threshold voltage mismatch decreases with increasing signal amplitude and can be reduced by using long transistors, which leads to large effective gate voltages, again requiring large supply voltage. Fortunately, even a small quiescent current  $I_Q$  will reduce the second harmonic distortion significantly due to the factor  $(1 - 2\sqrt{I_Q/I_m})$  so there is no need for a large quiescent current, implying that the power consumption can be kept low with the complementary current mirror. Obviously, for small signals ( $I_m \leq I_Q$ ) the expressions given above are not correct. An analysis of this situation yields distortion dependencies similar to the single class A current mirror.

From a design point of view statistical variations in  $V_T$  and  $\beta$  must be taken into account. The distortion model given above can be used together with statistical models [11, 12, 13] relating the variation in  $V_T$  and  $\beta$  to the design parameters  $W$  and  $L$  to give estimates for the attainable distortion levels. Assuming that  $\Delta V_{TN}$ ,  $\Delta V_{TP}$ ,  $\Delta\beta_N$  and  $\Delta\beta_P$  are characterized by the standard deviations  $\sigma_{V_{TN}}$ ,  $\sigma_{V_{TP}}$ ,  $\sigma_{\beta_N}$  and  $\sigma_{\beta_P}$  we find the following contributions to the distortion in the complementary current mirror:

$$D_{2,\Delta\beta_N}^2 = 0.06 \left( 1 - 2 \frac{I_Q}{I_m} \right)^2 \frac{\sigma_{\beta_N}^2}{\beta_N^2} \quad (13)$$

$$D_{2,\Delta\beta_P}^2 = 0.06 \left( 1 - 2 \frac{I_Q}{I_m} \right)^2 \frac{\sigma_{\beta_P}^2}{\beta_P^2} \quad (14)$$

$$D_{2,\Delta V_{TN}}^2 = 0.13 \left( 1 - 2 \sqrt{\frac{I_Q}{I_m}} \right)^2 \frac{\beta}{I_m} \sigma_{V_{TN}}^2 \quad (15)$$

$$D_{2,\Delta V_{TP}}^2 = 0.13 \left( 1 - 2 \sqrt{\frac{I_Q}{I_m}} \right)^2 \frac{\beta}{I_m} \sigma_{V_{TP}}^2 \quad (16)$$

and

$$D_{3,\Delta V_{TN}}^2 = 0.01 \frac{\beta}{I_m} \sigma_{V_{TN}}^2 \quad (17)$$

$$D_{3,\Delta V_{TP}}^2 = 0.01 \frac{\beta}{I_m} \sigma_{V_{TP}}^2 \quad (18)$$

A common approximation is to consider  $\sigma_{\beta}/\beta$  and  $\sigma_{V_T}$  to be inversely proportional to the square root of the gate area with proportionality constants  $A_{\beta}$  and  $A_{V_T}$ , respectively [12]. As an example, the constants found in [12] for a  $2.5\mu\text{m}$  n-well process are as follows:

Parameter	NMOS	PMOS	Unit
$A_{V_T}$	30	35	$mV\mu\text{m}$
$A_{\beta}$	2.3	3.2	$\% \mu\text{m}$

It should be emphasized that these parameters are process-specific. The parameters given above are from a specific  $2.5\mu\text{m}$  process and can only be used for this process. For transistor areas on the order of  $(10\mu\text{m})^2$  the parameters above lead to  $\sigma_{\beta}/\beta$  of about 0.3% and  $\sigma_{V_T}$  of about  $3mV$ . With realistic values of  $\beta$ ,  $I_m$  and  $I_Q$  it is evident from (13)-(18) that the threshold mismatch is the dominant cause of distortion. It is not obvious whether the second harmonic or the third harmonic will dominate. This depends on  $I_Q/I_m$  as can be seen from (15) and (16). It can also be noted that the different contributions to the total harmonic distortion, THD, given by (13)-(18) are not uncorrelated. From (11) and (12) we note that the second harmonic depends on the sum of NMOS and PMOS threshold voltage mismatch whereas the third harmonic depends on the difference between the NMOS and PMOS threshold voltage mismatch. Thus, the threshold voltage mismatch may cancel the third order harmonic distortion while causing a significant second order distortion or vice versa. However, a worst case estimate may be obtained by adding the (squared) distortion contributions given by (13)-(18).

#### 5. A DESIGN EXAMPLE

Let us consider a complementary current mirror with a maximum input current of  $I_m = 100\mu\text{A}$ . We would like to operate the mirror from supply voltages of  $V_{DD} = -V_{SS} = 1.5V$  and at a quiescent current of  $I_Q = 5\mu\text{A}$ . For the transistors we assume  $\mu_n C_{ox} = 50\mu\text{A}/V^2$ ,  $|\mu_p| C_{ox} = 20\mu\text{A}/V^2$ , and  $V_{TN} = |V_{TP}| = 0.8V$ . The mirror transistors must be designed with a maximum gate-source voltage which will fit within the supply voltage limitations. We select  $W_1/L_1 = 16$  and  $W_3/L_3 = 40$ , giving a maximum gate-source voltage of about  $1.3V$  which still leaves room for the drain-source saturation voltages of M5 and M6 (see fig. 1(b)). Let us assume  $\sqrt{W_1 L_1} = 10\mu\text{m}$  and  $\sqrt{W_3 L_3} = 16\mu\text{m}$ . With the matching parameters from the table above we find  $\sigma_{V_{TN}} = 3.0mV$ ,  $\sigma_{V_{TP}} = 2.2mV$ ,  $\sigma_{\beta_N}/\beta_N = 0.23\%$  and  $\sigma_{\beta_P}/\beta_P = 0.20\%$ . Using even larger areas may not yield significant improvements as the mismatch tends to reach saturation values for large area devices [13]. From (11) and (12) we find estimates for the distortion as follows:  $D_{2,\Delta\beta_N} \approx 0.06\%$ ,  $D_{2,\Delta\beta_P} \approx 0.05\%$ ,  $D_{2,\Delta V_{TN}} \approx 0.17\%$ ,  $D_{2,\Delta V_{TP}} \approx 0.12\%$ ,  $D_{3,\Delta V_{TN}} \approx 0.08\%$ ,

$I_m = 100\mu A$ $(W/L)_N = 16$ $(W/L)_P = 40$		Poor matching		Fair matching		Good matching		
		Theory	Simulation	Theory	Simulation	Theory	Simulation	
Single mirror $I_Q = 150\mu A$		$\Delta V_{TN} = -10mV$ $\Delta V_{TP} = -5mV$ $\frac{\Delta\beta_N}{\beta_N} = 0.05, \frac{\Delta\beta_P}{\beta_P} = -0.03$		$\Delta V_{TN} = -5mV$ $\Delta V_{TP} = 3mV$ $\frac{\Delta\beta_N}{\beta_N} = 0.02, \frac{\Delta\beta_P}{\beta_P} = 0.01$		$\Delta V_{TN} = 3mV$ $\Delta V_{TP} = 2mV$ $\frac{\Delta\beta_N}{\beta_N} = 0.002, \frac{\Delta\beta_P}{\beta_P} = 0.002$		
		$D_2$	0.14%	0.17%	0.07%	0.09%	0.04%	0.05%
		$D_3$	0.03%	0.03%	0.01%	0.01%	0.00%	0.00%
Compl. mirror $I_Q = 5\mu A$		–		–		–		
		THD	–	0.18%	–	0.09%	–	0.05%
		$D_2$	2.60%	2.32%	0.34%	0.32%	0.27%	0.25%
		$D_3$	0.14%	0.18%	0.22%	0.25%	0.03%	0.04%
		THD	–	2.37%	–	0.43%	–	0.26%

**Table 1.** Calculated and simulated distortion levels for selected current mirror examples

and  $D_3, \Delta V_{TP} \simeq 0.06\%$ . A worst case estimate for the THD would then be a THD of about 0.25% for a mirror with all the mismatch parameter values corresponding to the standard deviations in  $V_T$  and  $\beta$ . With four independent mismatch parameters only about  $(0.68)^4 \times 100\% = 22\%$  of the functional devices of a fabrication batch can be expected to have all four mismatch parameters smaller than the standard deviations. A more useful estimate for the worst case distortion would be to consider the  $3\sigma$ -limit. As the distortion components are proportional to the mismatch parameters this would result in an estimated THD which is below 0.75% for more than 98% of the devices in a batch.

## 6. SIMULATION

In order to verify the analytical model and to investigate whether a more realistic model than the ideal Shichman-Hodges transistor model would significantly influence the considerations given above the current mirrors have been simulated using device parameters (level 3) from a commercially available  $2\mu m$  CMOS process. Simulations have been carried out for different values of mismatch, also values of mismatch significantly exceeding the values which can be expected in practice in order to verify the analytical model.

Representative results are shown in the table above, illustrating the distortion levels found in mirrors with different mismatches. It is found that although the transistor model used for the theoretical analysis is very simple the distortion analysis gives results which are in reasonable agreement with the simulated values and it reveals the relevant dependencies and design criteria. Also, by comparing the THD and the second and third harmonic we see that harmonics of higher order than 3 do not contribute much to the total harmonic distortion and that distortion levels of less than 1% THD can be obtained through a careful design.

## 7. CONCLUSION

We have presented an analytical model for the distortion in CMOS current mirrors, both single current mirrors and complementary current mirrors. The model has been verified through simulations and relevant design considerations for low distortion current mirrors have been discussed. The model can be combined with statistical models for variations in device parameters and can be used to estimate expected distortion levels versus layout parameters. It is found that distortion levels below 1% are attainable. However, it is also clear that ultra-low distortion requirements cannot be fulfilled by a current mirror. This implies for instance that a current mirror should not be inserted in a feedforward signal path in a system with requirements for very low distortion or in the I/O path to

a high precision data converter.

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