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**Heschel, Matthias; Bouwstra, Siebe**

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# Conformal Coating By Photoresist Of Sharp Corners Of Anisotropically Etched Through-Holes In Silicon

Matthias Heschel and Siebe Bouwstra
Mikroelektronik Centret, DTU bldg. 345-East, DK–2800 Lyngby, Denmark

## Summary

This Extended Abstract describes a photoresist treatment yielding conformal coating of three-dimensional silicon structures. This even includes the sharp corners of through-holes obtained by anisotropic etching in 100-silicon. Resist reflow from these corners is avoided by replacing the commonly done baking procedure with a proper vacuum treatment. The investigated photoresist is Shipley's Eagle 2100 ED, a negative-working electrodepositable photoresist. Electrical frontside to backside interconnections have been made using this photoresist as etch mask.

**Keywords:** electrodepositable photoresist, feedthroughs, 3 D lithography.

## Introduction

Beside the ongoing trend to make better and smaller devices - both in Microelectronics and Micromechanics - great efforts are made to integrate individual high performance chips to obtain more complex systems. Hereby, space constraints call for stacking rather than standard planar arrangements. Moreover, stacked Multichip Modules (MCM), see for example [1, 2], benefit from shortened electrical interconnections in terms of faster operation speed and reduced parasitic parameters. The electrical interconnections between stacked chips are best realized by vertical feedthroughs through these chips. In cases where multiple interconnections per through-hole are required the patterning of the metallization layer is the major challenge. Standard photoresist techniques fail because of their unability to cover structured silicon wafers. A very promising solution is the application of electrodepositable (ED) photoresists as proposed in [3] and [4]. Photolithography in deep cavities using electrodepositable photoresists has already been presented in [5]. All three use ED photoresists manufactured by *Shipley Europe Ltd.* In [3] the photoresist is the positive-working *PEPR 2400*, used as mold for electroplating of gold, resulting in one feedthrough per through-hole. In [4] the negative-working *Eagle 2100 ED* was used as an etch mask. Here multiple feedthroughs per hole were realized. Both references fault an insufficient photoresist coverage at the acute corners of the anisotropically etched through-holes. In [4] the photoresist thickness at these corners is only half of that on flat surfaces. Consequently, a sufficient corner coverage requires the photoresist on flat surfaces to be much thicker than actually needed. Thus, the resolution may be lowered. The coverage problems are caused by reflow of photoresist during baking procedures. Baking (here prebaking) of photoresist serves several purposes. First of all, it removes excess water and other solvents which would affect both exposure and development. Furthermore, it increases the etch resistance and improves the adhesion between photoresist and the layer to be patterned [6].

Slight reflow of the photoresist might be acceptable as long as the metallization system is simple and can be patterned by etching. However, stacking would require much more complicated metallization schemes, suitable for example as under bump metallization or top surface metallization for solder bumps. Such metallization systems usually consist of several layers, serving for adhesion, diffusion barrier, wettable surface, and corrosion protection. The choice of proper metals is solder dependent. Patterning of such metallization schemes by etching can be very difficult because of the different etchants needed for the different metal layers. Furthermore, etching of a complicated metallization system might not be the same as etching of the individual layers. Therefore, the patterning of the metallization should preferably be done either by lift-off or electro(less) plating (one has to check whether the resist is stable in the plating bath). However, both techniques require a conformal photoresist thickness all over the sample, including sharp corners. This can nearly be achieved by applying a new photoresist treatment as we will show in the following sections.

## Experimental

The processing of the samples is quite similar to that presented in [4] and will be described here only briefly.

### Through-Holes

The through-holes were made by anisotropic etching in (100)-silicon using a 2 $\mu m$ thick thermal silicon dioxide as etch mask and 28 wt% potassium hydroxide as etchant. The silicon wafers are double-side polished and 350 $\mu m$ in thickness. The openings of the holes are $1.1 \times 1.1\ mm^2$ and $2 \times 3\ mm^2$, respectively. After the through-holes were realized a thermal oxide with a thickness of 2 $\mu m$ was grown to serve as insulating layer between the later interconnections and the bulk silicon. The metallization was evaporated and consists of titanium as adhesion layer and gold as intercon-

nect material. The thicknesses were 300 Å and 4000 Å, respectively.

### Interconnection lines

The patterning of the evaporated metallization system is the key process. To obtain a conformal photoresist coating of our structured silicon wafer we used the negative-working ED photoresist *Eagle 2100 ED*. This photoresist has been developed for the use in printed circuit board (PCB) industry, where it is used as etch mask for copper metallizations. It is deposited from an aqueous emulsion with around 10 % solids. An excellent description can be found in [7] where also the following details were taken from. The solids are made up of micelles which are acrylic co-polymers carrying ionizable amino groups. In an acidic environment these amino groups become positively charged and cause negatively charged counter-ions to position around the micelles to stabilize them. Applying a voltage between two electrodes causes the micelles to migrate towards the cathode and the counter-ions to migrate towards the anode. Simultaneously, electrolysis of water takes place in the vicinity of the electrodes, increasing the pH-value in these regions. Reaching the cathode, the positive charge on the micelles is neutralized by hydroxide ions. The micelles become unstable and deposit onto the cathode, forming an insulating film. As the film thickness increases the electric field driving the migration of the micelles diminishes. Thus, reaching a certain thickness the voltage entirely drops across the insulating film and the deposition terminates. The final resist thickness depends on coating voltage, bath temperature and, if not self-terminated, coating time. As coating takes place, solids are taken from the bath which increases the conductivity of the bath by building up acid. However, to ensure good reproducibility of film thickness and quality, both conductivity and content of solids have to be kept at given levels. Therefore, *Shipley Europe Ltd.* recommends a closed loop system with ultrafiltration and permeate rinse bath.

Our ED photoresist setup is much simpler and does not contain any of the options mentioned above. We simply measure each of these parameters and add deionized water or resist emulsion if needed. This way, we maintain the conductivity between 250 and 350 $\mu S/cm$ and the content of solids between 8 and 12 %.

Since the cathode is the electrode to be coated, the metallized silicon wafer is negatively biased. Two stainless steel anodes are placed 9 cm from either side of the wafer. The wafer is cleaned in 95 wt% sulphuric acid prior to deposition to achieve a chemically clean gold surface. The photoresist depositions were performed at a bath temperature of 34°C and a voltage of 150 V. The deposition time was limited to 40 s, resulting in a photoresist thickness of around 12 $\mu m$. Longer deposition increases the number of pinholes and the roughness of the film. After deposition the wafer was rinsed in deionized water to remove excess resist particles.

To remove excess water and trace solvents two procedures were applied, baking and vacuum treatment. Baking was performed at 50, 65 and 80°C for 25, 10 and 3 min, respectively. Vacuum treatment was done at high vacuum ($10^{-4}$ Pa) and at low vacuum (3 Pa). Treatment durations varied between 1 hour and 18 hours.

The photoresist was patterned by exposure to ultraviolet light through masks with feedthrough structures both on frontside and backside. The handling of a wafer with trough-holes and photoresist on both sides is not standard and requires special tools for alignment and exposure.

The unexposed (non-polymerised) resist was removed using *Eagle 2005 Developer* from *Shipley Europe Ltd.*, diluted with deionized water.

Next, the exposed gold was etched in a potassium iodine solution using the photoresist pattern as etch mask.

The photoresist was stripped in *Eagle 2010 Remover* from *Shipley Europe Ltd.* and the titanium was finally etched in 5% hydrofluoric acid.

## Results

Figure 1 shows examples of electrical interconnections through silicon wafers fabricated according to the process described above. We applied both baking and vacuum treatment.

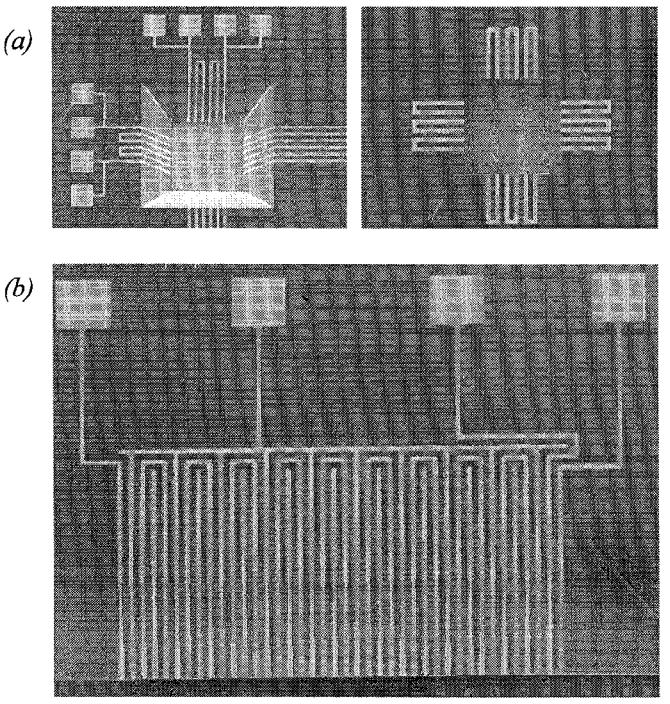


*Figure 1: Vertical multiple electrical interconnections through silicon wafers. (a): Frontside (left) and backside (right) of a 1.1 × 1.1 $mm^2$ through-hole with 30 $\mu m$ lines and 30 $\mu m$ spacings. (b) from [4]: Frontside of a 2 × 3 $mm^2$ trough-hole with 20 $\mu m$ lines and 20 $\mu m$ spacings.*

Linewidth and spacing are equal and vary between 10 and 50 $\mu m$. Compared to the feedthroughs in [4] the yield was significantly improved. Feedthroughs with 40 and 50 $\mu m$ linewidth and spacing were made with 100% yield. This was achieved by improved processing and better handling tools. However, misalignment reduces still the yield for 30 $\mu m$ linewidth and spacing to 80%. Here better alignment marks in our masks are needed. The yield for 20 $\mu m$ structures is still reduced by short circuits caused by light reflection from the opposite sidewall. This problem is hoped to be solved by using linearly polarized light. This should minimize the reflectivity of two opposite sidewalls. For experimental purpose, the hole size can be increased so that the reflected light goes through the bottom opening of the hole, see Figure 1b. The top opening of the through-hole has to be at least 3.5 times the wafer thickness. A more sophisticated way to get rid of the reflection problems is to use a so-called antireflective coating (ARC) underneath the resist. However, a proper ARC is hard to find. It has to meet special requirements, for example for wavelength, angle of incidence, conductivity and deposition technique. The probably easiest way to avoid reflections is to have spacings of at least 30 $\mu m$. According to *Shipley Europe Ltd.*, the minimum linewidth obtainable is 10 $\mu m$. However, one has to consider that the resolution decreases with increasing proximity (here equal to the wafer thickness) during exposure.

The results shown in Figure 1 were obtained both by baking the photoresist at 50°C for 25 min as well as by vacuum treatment. This means that both techniques can be used if the patterning technique is etching. Our main interest, however, was to achieve a conformal photoresist coverage at the sharp corners. Figure 2 shows how the corner coverage changes with baking temperature and time and vacuum treatment duration. Figure 3 shows Scanning Electron Microscope (SEM) images of the samples as deposited (a) and prebaked (b-d). The photoresist as deposited shows an excellent corner coverage. The resist thickness is around 12 $\mu m$, also at the obtuse corner and around 10 $\mu m$ at the acute corner. Baking the resist at 50°C results in a slight reflow at the obtuse corner and a strong reflow at the acute corner. After 25 min baking time the resist thicknesses are 8 and 4 $\mu m$, respectively, at these corners (Figure 3b). Increasing the temperature to 65°C or even 80°C results in a strong reflow both at the obtuse and the acute corner. The curves for resist thickness drop almost instantly.

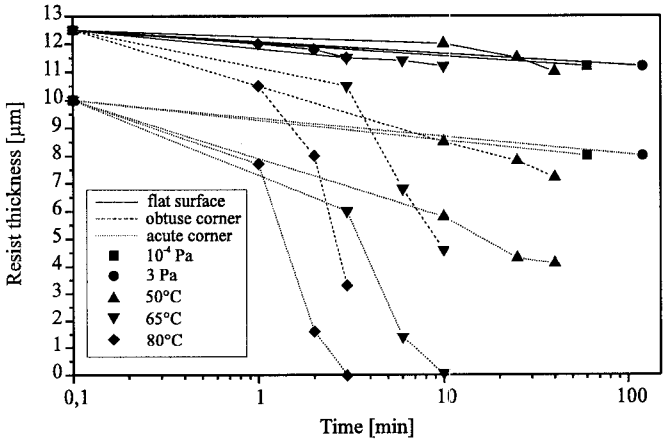


*Figure 2: Photoresist thickness vs. prebake temperature and time and vacuum treatment duration at flat surfaces, obtuse and acute corners. After the solvent has been driven out the photoresist thickness is around 11.5 $\mu m$ at the flat surface.*

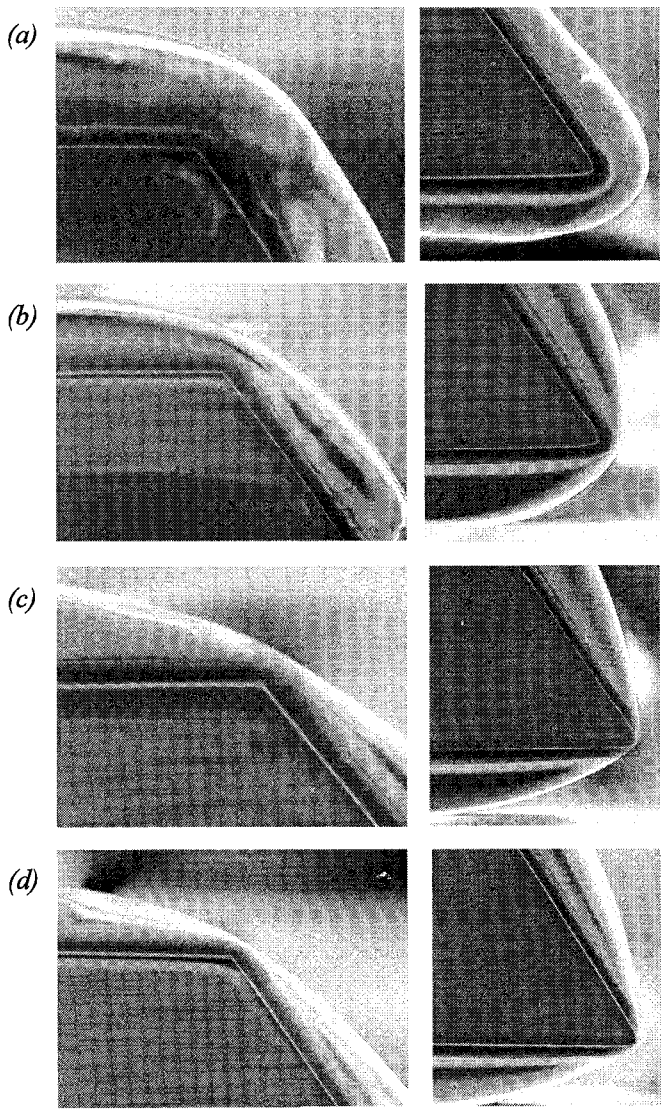


*Figure 3: SEM images of obtuse (left) and acute (right) corner coverage by ED photoresist Eagle 2100 ED. The resist thickness at flat surfaces is around 12 $\mu m$. (a): as deposited, (b): 25 min at 50°C prebake, (c): 10 min at 65°C prebake, and (d): 3 min at 80°C prebake.*

Figure 2 also shows the resist thicknesses for vacuum

treated samples. It turns out that neither vacuum pressure nor time is important. Both low and high vacuum show very good results. Resist coverage at both corners is shown in Figure 4. Absolutely no reflow took place at the obtuse corner. The reflow at the acute corner is very little. Although time is not very important one has to ensure that all excess water and trace solvents are removed. At the other hand, one should not have the sample too long in vacuum, the resist will simply overdry. This overdrying occurs mainly at large flat surfaces which then become very resistant to the developer. The adhesion between photoresist and gold layer for a vacuum treated sample is not as good as for a prebaked sample. Figure 4b shows that the resist lifts-off at the edges, leading to underetching of the metallization. However, in the case of lift-off this could even be an advantage and could counteract the disadvantage of the positive resist sidewalls. Lift-off has not been done yet but will be the next step in our work.

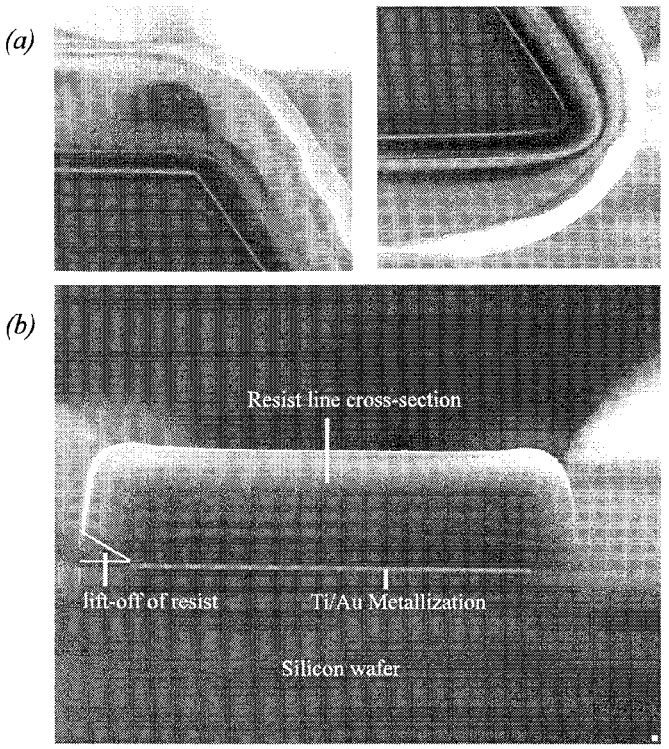


*Figure 4: SEM images of (a) obtuse (left) and acute (right) corners with vacuum treated photoresist (1h at $10^{-4}$ Pa). (b): Cross-sectional view of a 40 $\mu m$ photoresist line.*

## Conclusions

We have shown that the prebake of ED photoresist *Eagle 2100 ED* can be replaced by a simple vacuum treatment. 1-2 hours in a vacuum of between 3 and $10^{-4}$ Pa are sufficient to remove all excess water and trace solvents. The resulting resist film is non-sticking. The photoresist coating is very uniform including the sharp corners of anisotropically edged through-holes. Vertical multiple electrical feedthroughs were realized by etching which showed 100% yield for 40 and 50 $\mu m$ linewidth and spacing. Next, lift-off as metallization patterning technique will be applied

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