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# Aggressive Media Exposed Differential Pressure Sensor with a Deposited Membrane

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## ABSTRACT

A new piezoresistive differential pressure sensor design for harsh wet environments is presented. The sensor design is based on a deposited membrane, which is deposited on top of polysilicon interconnects and piezoresistors. Flat membrane surfaces are thereby achieved. This enables thin film protective coating using sputtered films, which usually have poor step coverage. The concept is demonstrated using both epitaxial silicon and sputtered amorphous silicon as membrane materials and tantalum oxide as coating material. Using polysilicon piezoresistors, a sensitivity of 11.3 mV/V bar was obtained. Exposure of the sensors with sputtered amorphous silicon membranes to aggressive media with pH 11 and 70°C for 20 hours did not change their performance.

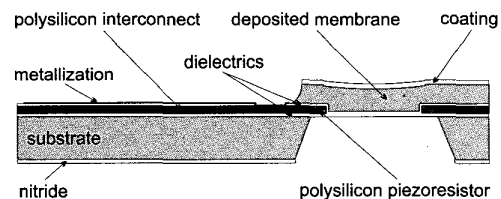
## INTRODUCTION

Measurement in aggressive wet media usually involves complicated encapsulation schemes. The cost of the encapsulation is typically much higher than the cost of the actual silicon chip. Exposure of the silicon chip directly to the aggressive media reduces the cost greatly, since packaging is reduced [1].

Sputtered amorphous tantalum oxide (a-TaO) has shown promise as coating material due to excellent chemical and mechanical properties [2]. The step coverage of the sputtered film is poor. It is difficult to coat patterns with steep sidewalls and sharp concave corners, such as polysilicon piezoresistors and interconnects [2]. The design presented here enables coatings on both sides of the membrane. The membrane is deposited on top of the interconnects and piezoresistors, thereby in principal smoothening the topography, see *Figure 1*. Other advantages may include: simple etch stop, dielectrically insulated piezoresistors, easily upgradable to SOI technology, adjustable residual stress in the membrane, well defined membrane thickness and generic technology platform suitable for different membrane materials as well as for other types of devices.

Epitaxial silicon (i.e. polysilicon grown in an epitaxial reactor [3]) and sputtered amorphous silicon were chosen as membrane materials. Epitaxial silicon is suitable for MEMS applications, i.e. pressure sensors as shown elsewhere [3,4].

To our knowledge only passive sputtered amorphous silicon beams have been reported so far [5].



*Figure 1: Schematic cross section (side view) of the piezoresistive differential pressure sensor with a deposited membrane. Dimensions are not to scale.*

## FABRICATION

An LPCVD nitride with a thickness of 1100 Å was deposited on an <100> Si double sided polished wafer. A TEOS oxide was then deposited and removed in BHF from the front-side. The TEOS oxide acts as protection for the subsequent front-side removal of the nitride in phosphoric acid. 1000 Å wet thermal oxide was then grown.

5500 Å LPCVD polysilicon was deposited and removed from the backside. The polysilicon was boron implanted at a low dose yielding the desired doping level of the piezoresistors (*Figure 2A*). The resistors and interconnects were then defined by Reactive Ion Etch (RIE) and, using aluminum as mask material, the interconnects were boron implanted at a high dose.

1000 Å thermal wet oxide was grown in order to dielectrically insulate the piezoresistors and interconnects (*Figure 2B*). 9.3 μm sputtered amorphous silicon and 0.5 μm sputtered a-TaO were then deposited (*Figure 2C*). In between, the wafers were annealed at 500°C for 10 min. The heat treatment reduces the residual stress,  $\sigma_R$ , of the sputtered amorphous silicon from approximately -121 MPa to only -8 MPa, without influencing the film quality adversely.

Thick sputtered amorphous silicon is very sensitive for annealing in nitrogen at elevated temperatures. Figures 3 and 4 show the result of annealing at 500°C and 600°C for 30 min. (including long ramping). A dramatic increase in pin-hole density was observed at annealing temperatures

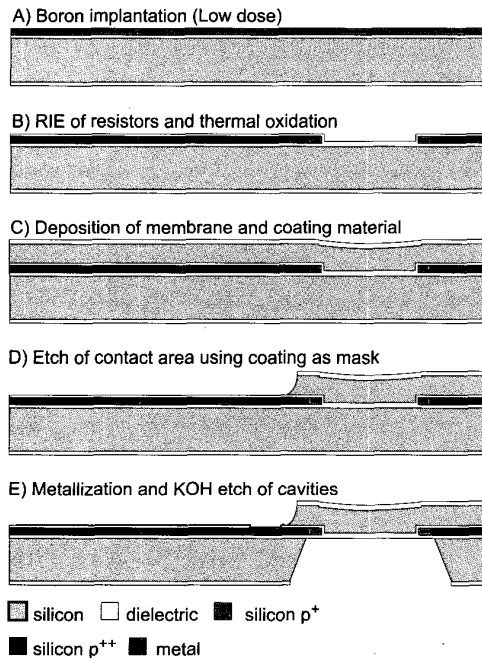


Figure 2: Process sequence.

between 500°C and 600°C. Microscopic cracks, instead of pin-holes, were observed after annealing at temperatures of 600°C and higher. The peculiar behavior with regard to pin-holes is unclear. Crystallization of amorphous silicon can however take place at annealing temperatures of 600°C [6] and the microscopic cracks are most-likely caused by very high tensile stress in the film.

Using the a-TaO coating as mask, the sputtered silicon was etched away from the contact areas in a 28 wt% KOH solution at 80°C (Figure 2D). Small windows were etched in the oxide covering the interconnects using a 10 μm thick resist. 500 Å Ti and 5000 Å Al were then deposited and patterned in phosphoric acid. The wafers were annealed again, this time at 400°C for 30 min. The annealing ensures good electrical contact between the metallization and the polysilicon interconnects and reduces  $\sigma_R$  of the a-TaO from approximately -250 MPa to roughly 0 MPa [2]. The residual stress of the sputtered silicon is only marginally influenced by this heat treatment.

Finally, the membranes were defined by etching cavities from the backside in KOH (28 wt% solution at 80°C) using the oxide as etch-stop and nitride as mask (Figure 2E). The membrane seen from the backside is shown on Figure 5. The polysilicon piezoresistors and interconnects are clearly visible through the oxide.

The process sequence for pressure sensors with epipoly silicon membranes is very similar. The difference is the removal of epipoly silicon from the backside of the substrate and that annealing of the membranes is unnecessary. The residual stress,  $\sigma_R$ , is only -20 MPa at a deposition temperature of 900°C (Figure 6). The corresponding deposition

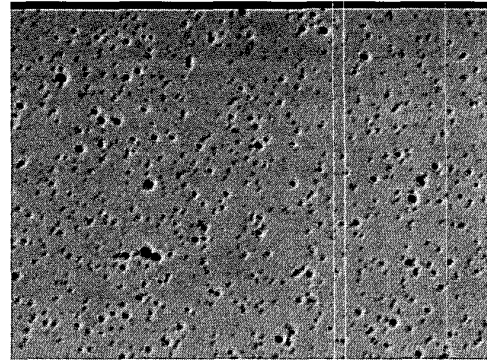


Figure 3: Optical microscope image of 8 μm sputtered silicon after annealing at 500 °C for 30 min. (including long ramping). Large number of pin-holes.

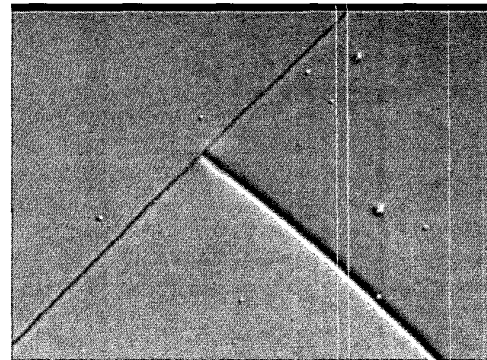


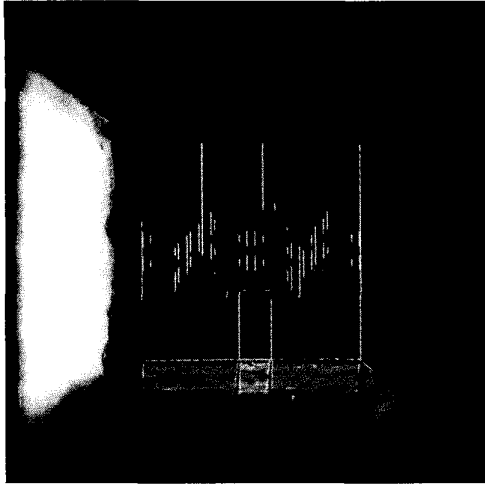
Figure 4: Optical microscope image of 8 μm sputtered amorphous silicon after annealing at 600 °C for 30 min. (including long ramping). Few pin-holes but microscopic cracks.

rate is  $\approx 200$  Å/min, which is considerably lower than what is typically reported for epipoly silicon growth [7]. The low pressure and flow used in the UHV-CVD process impede the growth (the reactions takes place in the mass transport limited regime).

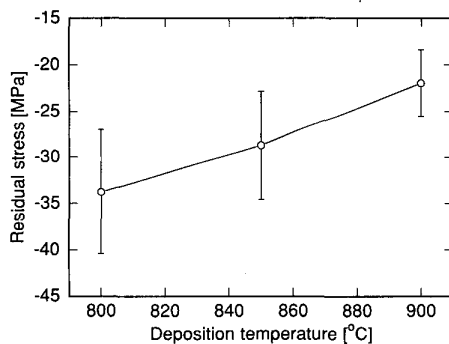
Due to high surface roughness of the epipoly silicon ( $R_p \approx 2700$  Å) and relatively poor step-coverage of a-TaO, the a-TaO coating could not withstand the front-side KOH etch of the contact areas. Polishing of the epipoly silicon is required for the protective coating and useful for UV exposure reasons [3]. Only sensors with single side a-TaO coating were realized so far.

## SENSOR CHARACTERIZATION

Sensors were mounted in titanium housings between o-rings. Sputtered silicon membrane sensors were exposed to aggressive media with pH 11 at 70°C for 20 hours. The output signals as a function of pressure at room temperature is shown in Figure 7. The output signal did not change significantly after exposure. Sensor characteristics are listed in Table 1.



**Figure 5:** Optical microscope image of the membrane seen from the backside. The polysilicon piezoresistors and interconnects at the bottom of the membrane are clearly visible.



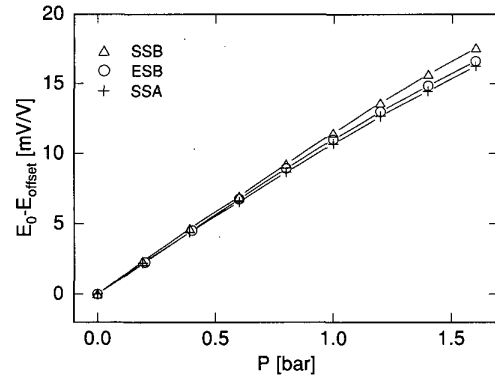
**Figure 6:** Residual stress,  $\sigma_R$ , of epipoly silicon as a function of deposition temperature.

The nonlinearities of the sensors are high. This is primarily due to the low membrane thickness in relation to the pressure range, i.e. nonlinear deflection. A thickness increase of 50 % should lead to  $\sim 0.1$  % nonlinearity.

## CONCLUSIONS

A new piezoresistive differential pressure sensor design based on a deposited membrane was demonstrated. Epipoly silicon and sputtered silicon were used as membrane materials and a-TaO was used as coating material.

Thick sputtered amorphous silicon is highly sensitive towards anneal temperature and time. The residual stress of the as-deposited silicon was reduced considerably by a short heat treatment. This did not influence the film quality adversely. Heat treatment of epipoly silicon was unnecessary due to low residual stress. Polishing is however necessary.



**Figure 7:** Output signal,  $E_0 - E_{\text{offset}}$ , versus pressure,  $P$ , at room temperature. ESB and SSB are the epipoly silicon membrane sensor and sputtered silicon membrane sensor not exposed to aggressive media respectively, and SSA is SSB after exposure. The sensors were driven in constant current mode ( $I_i = 0.53 \text{ mA}$ , which corresponds to a voltage of  $\sim 5 \text{ V}$ ).

**Table 1:** Sensor characteristics at room temperature. The coating ( $0.5 \mu\text{m}$ ) is not included in the mentioned thickness and  $\langle R \rangle$  is the bridge resistance including the series resistance ( $\sim 2.6 \text{ k}\Omega$ ). Measurements were also performed at temperatures up to  $90^\circ \text{C}$  in the case of ESB.

	ESB	SSB	SSA
Thickness [ $\mu\text{m}$ ]	7.5	9.3	9.3
$\sigma_R$ [MPa]	-20	-8	-8
S [mV/V bar]	10.4	11.3	10.2
Nonlinearity [% FS]	3.8	2.6	3.3
$\langle R \rangle$ [k $\Omega$ ]	9.5	9.2	9.4
TCS [% FS/ $^\circ\text{C}$ ]	-0.090		
TCO [% FS/ $^\circ\text{C}$ ]	0.40		
TCR [ppm/ $^\circ\text{C}$ ]	53		

The device performance was unchanged after exposure to aggressive media with pH 11 and  $70^\circ \text{C}$  for 20 hours.

## ACKNOWLEDGEMENTS

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