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Two-Stage Power Factor Corrected Power Supplies: The Low Component-Stress Approach

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***Abstract*- The discussion concerning the use of single-stage contra two-stage PFC solutions has been going on for the last decade and it continues. The purpose of this paper is to direct the focus back on how the power is processed and not so much as to the number of stages or the amount of power processed. The performance of the basic DC/DC topologies is reviewed with focus on the component stress. The knowledge obtained in this process is used to review some examples of the alternative PFC solutions and compare these solutions with the basic two-stage PFC solution.**

I. INTRODUCTION

Numerous single-stage and reduced power processing topologies have been presented in the literature predicting higher efficiency and/or lower cost. But very seldom these predictions are verified.

The purpose of this paper is to direct the focus back on how the power is processed and not so much as to the number of stages or the portion of energy processed. The method used to compare the different approaches take its basis in the concept of Component Load Factors (CLF) introduced in [1]. Component stress can be translated into cost, size and efficiency so investigating the basic topologies and reviewing how the component stress evolves under different circumstances an overview of reasonable solutions are obtained together with an overview of what not to do. The knowledge obtained from the use of CLF can then be used to recognize where unnecessary component-stress is produced. Examples are given in section IV. In the first example part of a detailed analysis is shown. In the second example the limitations of the configuration is identified.

II. COMPONENT LOAD FACTORS (CLF)

The motivation for using a tool like CLF to compare different converter topologies is that it gives a quantitative measure of the performance of the converter. This is very useful when choosing between topologies.

Definition of CLF:

$$CLF = \frac{V^* \cdot I^*}{P} \tag{1}$$

The V^* and I^* in (1) are the voltages and currents that the specific component is sensitive to. E.g. MOSFETs are sensitive to maximum drain-source voltage and peak-currents with respect to switching losses and rms-currents with respect to conduction losses. More information and background for CLF can be found in [1].

To keep the CLF calculations simple, the following assumptions are made:

a. $P_{IN} = P_{OUT}$
b. Inductor ripple current is small – meaning that square current waveforms are being switched.

In the first part of this section the case where the input is a DC-source will be reviewed. In the second part the CLF for the converters connected to an AC-source will be discussed.

A. DC Input

The Component Load Factors for the three basic topologies Buck, Boost and Buck-Boost will be presented. Since CLF represents accumulated stress for each component type, the calculated CLF of the basic Buck-Boost converter shown in figure 1c will actual represent the CLF for all Buck-Boost derived converters like the SEPIC, Cuk etc.

If MOSFETs are used as switches (Q) in Fig. 1, the currents of interest are the peak-, and rms-currents. For the diodes the currents of interests are the peak-, and average-currents and to some extend rms-currents. The inductors (L) in Fig. 1 are all high-frequency inductors, so the use of rms-currents and the average voltage is of interest. The capacitors are sensitive to the DC-voltages and the RMS-currents.

In table 1 the relevant CLF is listed for the three topologies shown in Fig. 1. The calculated CLF is presented as a function of the input/output voltage ratio.

Device	V*	I*	Buck	Boost	Buck-Boost	Isolated Buck	Isolated Boost
Q (MOSFET)	$V_{DS,\,Peak}$	I_{Peak}	$\frac{V_{IN}}{V_{OUT}}$	$\frac{V_{OUT}}{V_{IN}}$	$2+\frac{V_{IN}}{V_{OUT}}+\frac{V_{OUT}}{V_{IN}}$	$4\cdot\frac{V_{IN}}{V_{OUT}}$	$4\cdot\frac{V_{OUT}}{V_{IN}}$
	$V_{DS,\,Peak}$	I_{RMS}	$\sqrt{\frac{V_{IN}}{V_{OUT}}}$	$\frac{V_{OUT}}{V_{IN}}\cdot\sqrt{1-\frac{V_{IN}}{V_{OUT}}}$	$\sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right)^2+3\cdot\frac{V_{OUT}}{V_{IN}}+\frac{V_{IN}}{V_{OUT}}+3}$	$\sqrt{8\cdot\frac{V_{IN}}{V_{OUT}}}$	$\frac{V_{OUT}}{V_{IN}}\cdot\sqrt{4-\frac{4\cdot V_{IN}}{V_{OUT}}}$
D (diode)	$V_{AC,\,Peak}$	I_{Peak}	$\frac{V_{IN}}{V_{OUT}}$	$\frac{V_{OUT}}{V_{IN}}$	$2+\frac{V_{IN}}{V_{OUT}}+\frac{V_{OUT}}{V_{IN}}$	$4\cdot\frac{V_{IN}}{V_{OUT}}$	$4\cdot\frac{V_{OUT}}{V_{IN}}$
	$V_{AC,\,Peak}$	$I_{Average}$	$\frac{V_{IN}}{V_{OUT}}-1$	1	$1+\frac{V_{IN}}{V_{OUT}}$	$\frac{V_{IN}}{V_{OUT}}+1$	2
L (Inductor)	$V_{Average}$	$I_{DC(RMS)}$	$2\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$	$2\cdot\left(1-\frac{V_{IN}}{V_{OUT}}\right)$	2	* $2\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$	* $2\cdot\left(1-\frac{V_{IN}}{V_{OUT}}\right)$
C_1 (Input Capacitor)	V_{DC}	I_{RMS}	$\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$	0	$\sqrt{\frac{V_{IN}}{V_{OUT}}}$	* $\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$	0
C_2 (Output Capacitor)	V_{DC}	I_{RMS}	0	$\sqrt{\frac{V_{OUT}}{V_{IN}}-1}$	$\sqrt{\frac{V_{OUT}}{V_{IN}}}$	0	* $\sqrt{\frac{V_{OUT}}{V_{IN}}-1}$

Table 1. CLF for the basic topologies: Buck, Boost, Buck-Boost, isolated Buck and isolated Boost.
* Does not apply to single-ended isolated Buck- and Boost converters

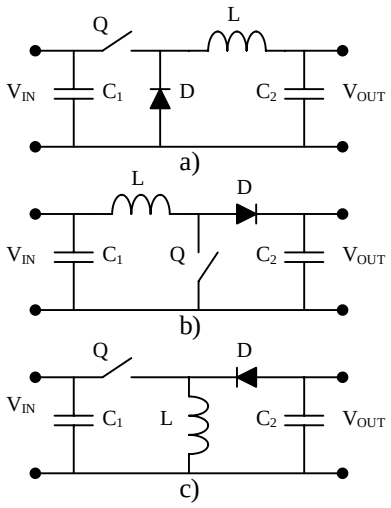

Figure 1. a) Buck DC-DC converter. b) Boost DC-DC converter. c) Buck-Boost DC-DC converter.

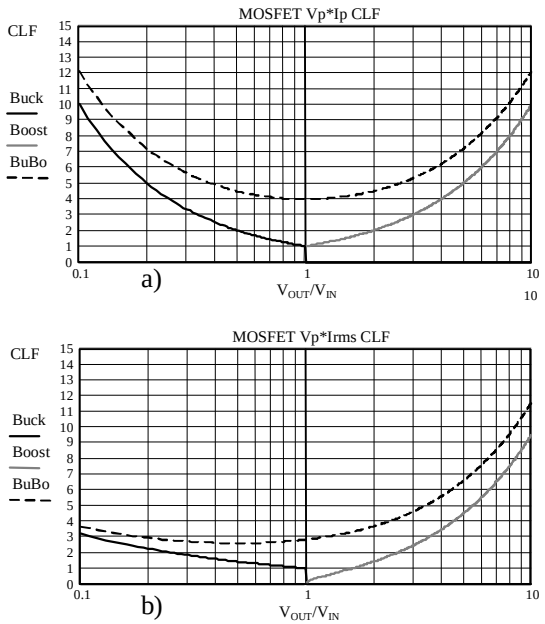

Figure 2. Switch CLF. a) CLF calculated with peak voltage and -current. b) CLF calculated with peak voltage and rms current.

The capacitor stress calculated in table 1 is carried out by assuming that the current flowing into and out of the converters of Fig. 1 are DC-currents.

By investigating the results of table 1, one will find that the performance of the Buck and Boost converter is very similar and that they exhibit lower component stress than the Buck-Boost derived converters, which should not come as a surprise.

In the case where peak voltages and peak currents are used to calculate the CLF, shown in Fig. 2a, the Buck and boost performance is similar.

The lowest CLF is obtained at the input/output ratio of 1 where the CLF=1 for the Buck and the Boost topology and CLF=4 for the Buck-Boost topology. As expected, the switch stress in the Buck-Boost topology is significantly higher. When the switch CLF using rms currents are used, the Buck and the Boost converter no longer perform the same. Fig. 2b, shows how the Boost topology is exposed to more stress compared to the Buck topology when the output/input ratio

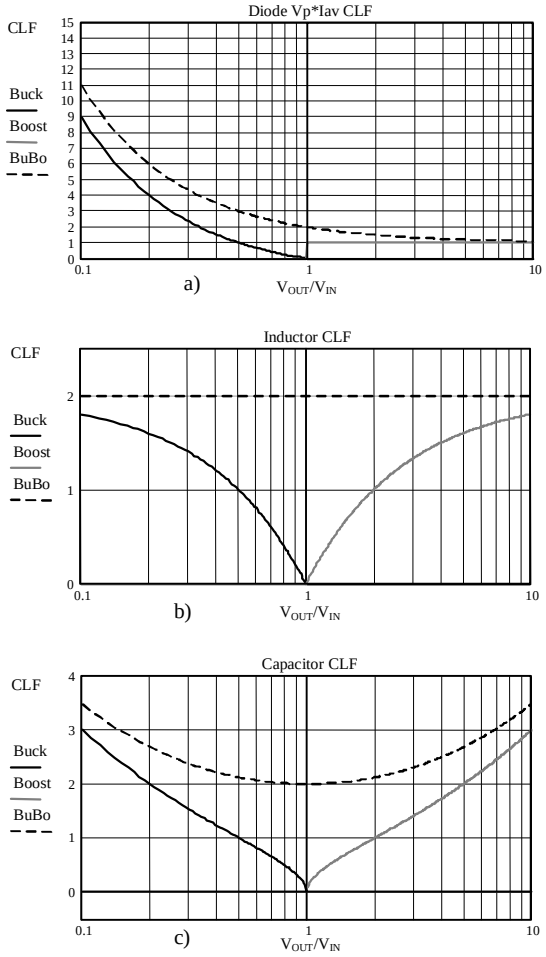

Figure 3 CLF. a) Diode CLF calculated with peak voltage and average current. b) Inductor CLF calculated with mean voltage and RMS current. c) Capacitor CLF calculated with DC voltage and RMS current.

increases/decreases. The stress characteristic for the Buck-Boost topology seems to follow the Buck and the Boost stress pattern in the respective output/input ranges, although higher. The diode, inductor and capacitor stress is shown in Fig. 3. In all cases the Buck-Boost topology impose the most stress on the components.

It is worth noticing the large difference in inductor and capacitor stress between the Buck-Boost derived topologies and the Buck- and Boost derived topologies when moderate step-up/step-down ratios are considered. As the step-up/step-down ratio increases the difference in component stress evens out.

If isolated converters derived from these three basic topologies are investigated one will find that the stress characteristics will change. Using isolated Buck- or Boost derived topologies will result in a substantial increase in semiconductor stress where as the stress on the rest of the components remain the same except when single-ended converters are used. The reason for this is that the effective

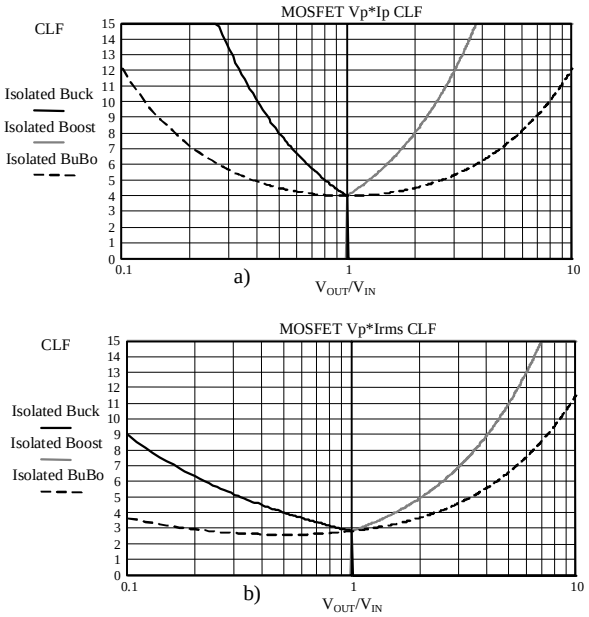

Figure 4. Switch CLF for the isolated versions of the converters of figure 1. a) CLF calculated with peak voltage and current. b) CLF calculated with peak voltage and RMS current.

duty-cycle of these converters cannot exceed 50 percent. The minimum component stress for the inductors and capacitors is therefore equal to the component stress found at a step-up/step-down ratio of 2 for the non-isolated Buck- and Boost converters. For the Buck-Boost topology the isolation will not affect the component stress.

The minimum stress for the isolated Buck and Boost derived topologies is obtained at an input/output ratio of 1 (CLF=4, Fig. 4a). The switch stress for the isolated Buck- and Boost derived topologies shown in figure 4a, is a factor of 4 larger than for the non-isolated converters.

The observations made when considering the component load factors for the basic topologies leads to the following key points:

No voltage variations at the input:

- The non-isolated Buck and Boost topologies are superior to the Buck-Boost topologies with regard to component stress.
- Isolating the Buck- and Boost derived topologies give rise to a substantial increase in semiconductor stress whereas the isolation does not affect the Buck-Boost derived topologies.
- If voltage step-up/step-down of more than a factor 4 is needed, an isolated topology should be considered.

Voltage variations at the input:

- Two-stage solutions should be considered since:
  1) Isolated Buck- and Boost derived topologies are severely penalized with regard to semiconductor stress.
  2) Buck-Boost derived topologies have high overall component stress.

B. Rectified AC Input

By investigating Boost and Buck-Boost derived topologies almost all practical PFC front-end circuits are covered. The Buck derived topologies are very seldom used especially when the universal line application is considered since the output voltage has to be lower the line peak voltage.

Developing an AC/DC-version of the Component Load Factor is not as straight forward as for the DC/DC version. The good thing about CLF for the DC/DC converters is the simplicity of the calculations. This also insures that the correlation between the calculated stress factors and the actual component stress is not lost in process. For the AC/DC converters the voltages and/or currents change in the components during the line period. Therefore some kind of averaging is needed and in doing so, some of the characteristics of the circuit may disappear in this process. In the AC/DC case the inductors carry both a low and a high frequency component which makes it unsuitable to be characterized with a simple number as done for the DC/DC case. Semiconductor stress can be characterized using the same methods as in the previous section. The switch stress of the 3 obvious PFC candidates is shown in Fig. 5.

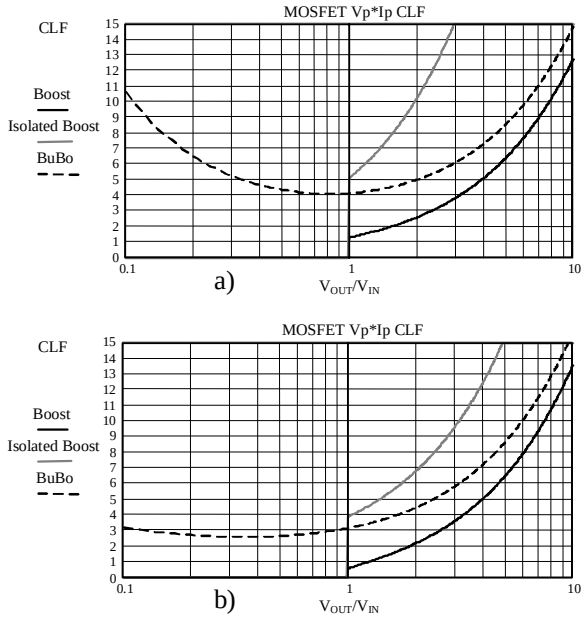

Figure 5. Switch CLF for the PFC Boost, Isolated Boost and Isolated/Non-Isolated Buck-Boost converters. a) CLF calculated with peak voltage and current. b) CLF calculated with peak voltage and rms current.

The step-up/step-down ratio for the AC/DC converters is defined as the ratio of the output- to line peak-voltage.

From Fig. 5 it is clear to see that the isolated Boost PFC is a pour choice with regard to switch stress. The non-isolated Boost PFC exhibits the lowest switch stress but it is difficult see how it will perform compared to the Buck-Boost PFC, especially in case of the universal line range. This property will be investigated in section IV.

III. PFC SOLUTIONS

There are numerous ways to classify the different proposed PFC solutions. A suggestion of how this can be done is shown in Table 2[2]. There are two main groups: "1. Sinusoidal Current" and "2. Non-sinusoidal current".

1. Sinusoidal Current	**2. Non-Sinusoidal Current**
1.1 Voltage follower	2.1 Passive filters
1.2 Passive filters	2.2 Reducing switches
1.3 Processing less energy	2.3 Removing control loops
1.4 Better processing	2.4 Combining topologies
1.5 Active filtering	2.5 Modifying DC/DC

Table 2. Characterizing PFC solutions [2]

More information about the groupings of table 2 can be found in [2].

Almost all of the alternative PFC solutions presented in the different subgroups of table 2 uses one or both of the following properties:

1. Isolated converters operated directly from the ac-source (1.4, 1.5).
2. Energy storage capacitor where the storage voltage is dependent on the AC-source voltage (2.2, 2.3, 2.4, 2.5).

A. Property 1

For the solutions where the main idea is to process the energy less than 2 times the isolated converter has to be connected to both the input and the output since any galvanic isolation requires at least 1 full power-processing step. So in order to keep the processing below 2 full power-processing steps the isolated converter must be connected AC-source.

As shown both for the DC/DC and AC/DC case the isolated converters have high semiconductor stress. In case of voltage variation at the input the semiconductor stress for the Boost converter increase dramatically. The Buck-Boost derived converters are not so sensitive to the voltage variation but these converters suffer from overall high component stress.

B. Property 2

In order to comply with the given regulations pulsating power has to be drawn from the AC-line. Therefore, internal

decoupling of this pulsating power is also a requirement to maintain fast output regulation.

The PFC approaches that use non-regulated internal energy storage are also known as Single-Stage converters. Normally these converters have a single control loop that regulates the output voltage but sometimes frequency control is added to the duty-cycle control to either limit the maximum internal storage voltage or to force the input current to comply with regulations. In all cases, the storage voltage is not constant but will vary with the input voltage.

IV. High Component Stress PFC Configurations

In this section examples of converters that suffer high component stress caused by the properties outlined in the previous section will be presented. The originally idea for the example converters of this section was to increase the efficiency by either reduce the number of stages or reduce the processing of power.

A. Processing less power:

The converter presented in [3] is the type of converter that without increasing the circuit-complexity compared to a two-stage approach only process the power 1.5 times. The idea is that by reducing the total power processed higher efficiency can be achieved.

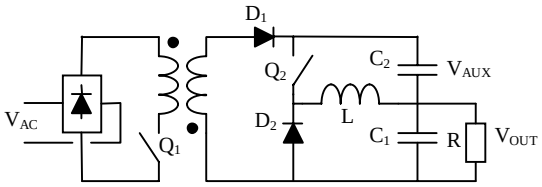

Figure 6. Converter of [3] with 1.5 times power-processing.

The voltage V_{AUX} in Fig. 6 is equal to V_{OUT}, which enables half of the power to be transferred directly to the output reducing the overall power-processing to 1.5 times compared to 2 times for the standard two-stage approach.

The auxiliary converter can be identified as Q_2, D_2, L and C_2 and make up a Buck-Boost converter. The power processed by the auxiliary converter is pulsating from zero to full output power with an average equal to half the output power.

Instead of the scheme shown in Fig. 6, the components used for the buck-boost converter could be used to utilize a Buck or a Boost converter as a post regulator in a two-stage configuration. In order to keep the comparison fair, the boost configuration is omitted because of its lacking ability to limit the output current. The voltage, V_{AUX}, on the capacitor C_2 is assumed to be equal to two times the output voltage so that the conditions for the isolated PFC stage is unchanged. A simple comparison between the schemes of Fig. 6 and Fig. 7 can then be carried out. The component stress for the two different approaches is presented in table 3.

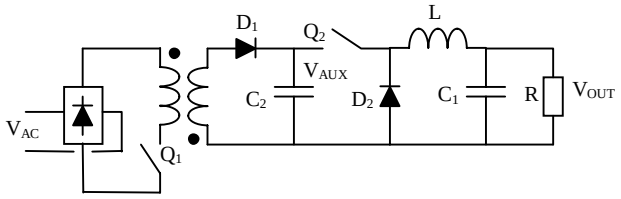

Figure 7. Two-stage PFC

		I. Buck-Boost	II. Buck	I./II. Ratio
Q_2	V_{Peak}	$2 \cdot V_O$	$2 \cdot V_O$	1
	I_{RMS}	P_O / V_O	$P_O / (\sqrt{2} \cdot V_O)$	$\sqrt{2}$
	$I_{P,mean}$	$(4 \cdot P_O) / (\pi \cdot V_O)$	P_O / V_O	$4/\pi$
D_2	V_{Peak}	$2 \cdot V_O$	$2 \cdot V_O$	1
	I_{AV}	$P_O / (2 \cdot V_O)$	$P_O / (2 \cdot V_O)$	1
	$I_{P,mean}$	$(4 \cdot P_O) / (\pi \cdot V_O)$	P_O / V_O	$4/\pi$
L	V_{Mean}	V_O	V_O	1
	I_{RMS}	$\sqrt{2} \cdot P_O / V_O$	P_O / V_O	$\sqrt{2}$

Table 3. Comparison between a "50%" power processing Buck-Boost converter and a "100%" power processing Buck converter.

The result of the comparison between the two approaches clearly shows that even though the Buck-Boost auxiliary/post regulator only process 50% of the power, the component stress and thereby the loses are greater than the approach with the Buck regulator despite the fact that this stage process 100% of the power.

Besides the fact that the approach with the Buck converter is offering less component stress also energy storage and dynamic behavior of the converter is improved.

In the scheme of Fig. 6, the auxiliary-converter has to be a Buck-Boost type or an isolated Buck or Boost converter – all which would have higher component stress compared to the solution with the simple Buck converter as a pre regulator.

The isolated PFC converter is necessary for the PFC approach that process less power. From Fig. 5 in section II, it is clear to see that the isolated Boost PFC are subjected to severe semiconductor stress, especially if the universal voltage range is applied. For the isolated Buck-Boost derived PFC circuits it is not clear to see if the component stress could be reduced by separating the PFC-function from the isolated converter.

In order to investigate the switch stress of the isolated PFC buck-boost converter of Fig. 8a, the conduction and switching losses of this configuration will be compared with the two-stage system shown in Fig. 8b. This system consists of a PFC boost converter and an isolated Buck derived converter. Here the switch stress comparison is carried out assuming that the total chip die area is the same for the two configurations of figure 8. Further more, it is assumed that the switching devices have the same voltage rating. The last assumption is not completely fair to the two-stage system since lower voltage rated devices can be used compared to the isolated PFC Buck-Boost converter.

For the universal line range ($90V_{AC}$-$270V_{AC}$) the output voltage of the boost converter has to be:

$$V_{OUT,BOOST} = Voltage\_range \cdot \hat{V}_{Line,Min} \quad (2)$$

As shown in section II, the minimum component stress for the Buck-Boost derived converters is in the area of 50% duty-cycle (V_{IN} = V_{OUT}). The output voltage should therefore be calculated as:

$$V_{OUT,BUCK-BOOST} = \sqrt{Voltage\_range} \cdot \hat{V}_{Line,Min} \quad (3)$$

The On-resistance of a MOSFET is proportional to $1/A_{Die}$ [4]. The conduction losses are therefore proportional to:

$$P_{Conduction-loss} \propto \frac{I_{RMS}^2}{A_{Die}} \quad (4)$$

The largest conduction losses occur at low line for both systems. An expression for the conduction losses as a function of the input power and the peak line-voltage can be calculated for the two systems in figure 8. Using the relation between V_{OUT} and $V_{Line,Min}$, expressions for the conduction losses can be calculated. For the Buck-Boost PFC the losses are proportional to:

$$P_{Loss\_BUCK-BOOST} \propto \left(\frac{P}{\hat{V}_{Line,Min}}\right)^2 \cdot \frac{2.98}{A_{Die}} \quad (5)$$

For the two-stage system the losses are proportional to:

$$P_{Loss\_BOOST+BUCK} \propto \left(\frac{P}{\hat{V}_{Line,Min}}\right)^2 \cdot \left(\frac{1.43}{(1-x)\cdot A_{Die}} + \frac{0.22}{x \cdot A_{Die}}\right) \quad (6)$$

$x \in [0,1]$

As it is seen from (6), the total chip die area is shared between the two stages of figure 8b. Minimum conduction losses are achieved for x = 0.28 meaning that 72% of the total die area should be used for the PFC Boost converter and the rest for the isolated Buck converter. The ratio of (5) to (6) is the relation between the conduction losses of the two systems.

$$K_{Conduction-Loss\_ratio} = \frac{P_{Loss\_BUCK-BOST}}{P_{Loss\_BOOST+BUCK}} = 1.07 \quad (7)$$

From (7) one can see that even though the power is processed by two stages the system does not generate more conduction loss per chip die are.

The switching losses are assumed to be proportional to the product of the voltages and currents being switched and the switching transition-time is proportional to the chip die area. The switching losses can then be approximated with:

$$P_{Swithing-Loss} \propto V \cdot I \cdot A_{Die} \quad (8)$$

The switching loss ratio is given by:

$$K_{Switching-Loss\_ratio} = \frac{P_{Loss\_BUCK-BOST}}{P_{Loss\_BOOST+BUCK}} = 1.21 \quad (9)$$

Again, the two-stage solution does not increase the switching losses.

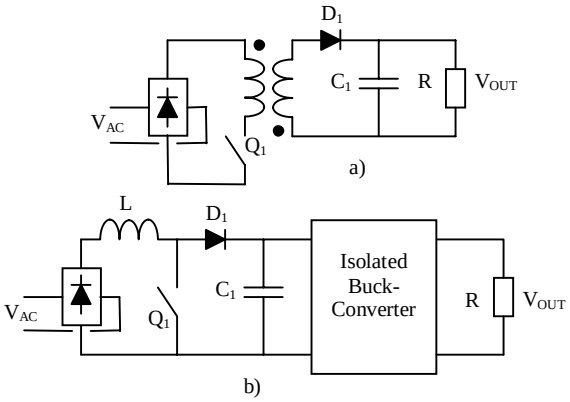

Figure 8. a) Isolated Buck-Boost PFC. b) Two-stage PFC system comprised of a Boost PFC and an isolated Buck DC/DC converter.

B. Single-Stage PFC converters:

The most severe problem with the single-stage converters is the voltage variation of the internal bus. Besides the problems with hold-up capacity the major contributor to power loss in the single-stage converters is the increased semiconductor stress.

The biggest problems arise when the application is targeted for the universal input voltage. In order to reduce the voltage variation, a voltage-doubler version of the Single-Stage topology presented in [5] was proposed in [6] (Fig. 9a). The converter was designed for a 5V, 90A output.

When analyzing the current-shaper block in Fig. 9a one will find that this configuration is very efficient and the stress imposed on the switches in the 2-Switch Forward is moderate. If allowing the use of a range-switch, other Boost derived topologies would perform just as good as the scheme shown in Fig. 9a. An example of such a converter could be the half-bridge Boost PFC converter with range-switch presented in [7].

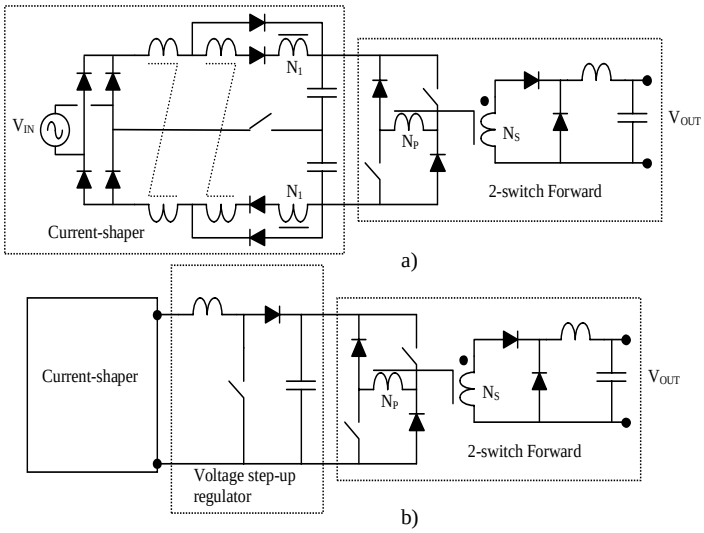

Figure 9. a) Single-stage PFC converter proposed in [6]. b) A reduced component stress version.

	Components	2-Switch Forward: V_{IN}: 235V-375V	2-Switch Forward: V_{IN}: 375V	DC-DC Boost: V_{IN}: 235V-375V
1	Switches	3 A_{RMS}, 375V	1.88 A_{RMS}, 375V	1.3 A_{RMS}, 375V
2	Diodes	69 $A_{Average}$, 21V	50 $A_{Average}$, 15V	1.3 $A_{Average}$, 375V
3	Transformer	No difference	No difference	-
4	Inductors	3.45 V·s/f_{Switch}, 100A_{DC}	2.5 V·s/f_{Switch}, 100A_{DC}	88 V·s/f_{Switch}, 2.12 A_{DC}
5	Capacitors	* See below in text	* See below in text	* See below in text

Table 4. Comparison of the two output sections of Fig. 9.

The voltage at the input-terminals of the 2-switch Forward in Fig. 9a varies from 235V to 375V at full power for the universal-line range 90V_{AC}-265V_{AC}. From the observations made in section II, it is clear that the voltage variation at the input of the 2-switch Forward will increase the component stress. As an example of the effects of the input voltage variations, it will be shown that adding an extra stage to cope with this, will actual reduce the overall stress and thereby improve efficiency.

The configuration of Fig. 9b uses an extra switch to perform the step-up action. Again, to keep the comparison fair the same total chip die-area (A_{Die}) is available for the two configurations. In order for the 2-stage output section to have less conduction loss than in the case with the single-stage output section the following equation has to be true:

$$\frac{4 \cdot I^2_{RMS,Forward,Single-Stage}}{A_{Die}} \geq \frac{4 \cdot I^2_{RMS,Forward,Two-Stage}}{x \cdot A_{Die}} + \frac{I^2_{RMS,Step-up}}{(1-x) \cdot A_{Die}}$$
$$x \in [0,1]$$

Solving the above equation and minimizing the conduction losses in the two-stage configuration will result in a value of x = 0.67. Using the data of table 4 one finds that the Single-stage configuration increases the switch conduction losses with 40% even though the voltage variation is moderate compared to other Single-Stage converters.

The switching losses can found to be about the same in the two cases (7% increase in switching losses when using the single-stage configuration).

The output diodes in the single-stage configuration are also subjected to an increase of 40% in both blocking voltage and current rating which in this case where the output current is high will have an impact on the efficiency. The diode added in the step-up converter is subjected to an average current of 1.33A, which will not affect the efficiency noticeable.

The worst-case transformer stress is at the duty-cycle D = 0.5 and in both cases the transformer stress is the same. The output inductor stress in the two-stage case is less than for the single-stage case but an extra inductor is needed in the step-up converter. The overall inductor stress is higher in the two-stage configuration because a single-ended Buck derived topology is used. The magnetic stress would be the same if half-bridge or full-bridge isolated converters were used.

In case of the capacitor the two-stage solution offer a clear advantage with respect to hold-up capacity. The energy is stored at a high voltage and since the step-up converter is inserted between the current-shaper and the 2-Switch Forward all the energy stored at the output of the current-shaper can be utilized.

V. Conclusion

The two-stage approach secures a minimum total stress on the circuit components. Further research in PFC systems should be directed towards optimizing the PFC stage and/or the DC/DC stage. It is misunderstood that reducing the number of stages and/or processing less power automatically achieves higher efficiency. Proper design and proper power processing achieve high efficiency.

In general low component stress can be translated into high efficiency, small physical size and low cost. In the low power range some of the alternative solutions can have an advantage in cost compared to the two-stage solution but the efficiency will be sacrificed.

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