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# All-optical bit-pattern recognition in data segments using logic AND and XOR in a single all-active MZI wavelength converter

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*Abstract: A novel and cost-effective scheme for comparing a segment of an incoming data stream to an expected sequence, using a single, all- active MZI is proposed. The comparator comprises the logic AND and XOR functions, and is demonstrated at 10 Gb/s.*

## Introduction

Before fully transparent optical networks become reality, a number of solutions for all-optical signal processing tasks must be developed. Apart from wavelength conversion and regeneration, which are among the most mature signal processing applications [1], functionalities such as data encryption/decryption [2], label-swapping [3], and pattern recognition [4] have been demonstrated and may too become feasible in the optical domain. The latter example, pattern recognition, is a very versatile functionality that applies wherever an unknown bit-sequence is compared to a known and expected sequence. Examples of such applications include address recognition in all-optical packet routers, and implementation of all-optical error detection. The latter is the first step towards an optical implementation of forward error correction (FEC), which is believed to become standard in 40 Gb/s systems [5].

Bit comparators can be implemented using either the Boolean AND or XOR gate, both of which have been demonstrated optically at bit rates ≥ 20 Gb/s using SOA-based, integrated Mach Zehnder (MZI) and Michelson (MI) interferometers [6-7], as well as the UNI, which is a fiber/SOA hybrid interferometer [8-9]. There are advantages and disadvantages related to using either the AND or XOR gate as a comparator, which will be detailed in the following section. However, in this paper we present a novel bit-comparison scheme based on a combination of AND and XOR that eliminates the disadvantages of the individual gates. The comparator is operated at 10 Gb/s, and is realized using a single all-active, polarization independent MZI designed for 10 Gb/s operation [10].

## Principle

Bitwise comparison between an input pattern and a comparator sequence is shown in Fig. 1 using (a) an AND gate, (b) an XOR gate, and (c) a combination of the two gates. The input pattern is expected to contain the sequence "1011" at a specific time, indicated by the hatched area, but for some reason the second "1" bit is incorrect, and the timeslot contains a "0" instead (indicated by the dashed pulse). In all three implementations in Fig. 1, the comparators produce a pulse at the output for each erroneous bit detected. The output is detected by a photo detector (P.D.), and thus a surge in the photo current will correspond to an error. A high-bandwidth P.D. will be able to identify individual errors, whereas a cost-effective low-bandwidth solution will simply reveal the presence of errors, which may be sufficient for a number of applications.

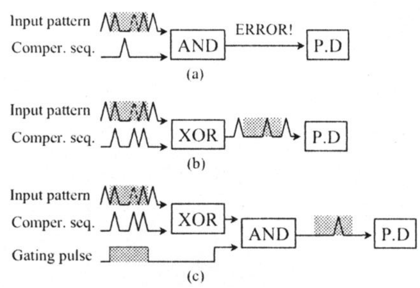


Fig. 1. Bit-comparators based on (a) AND, (b) XOR, and (c) AND + XOR. P.D = photo detector.

When using an AND gate as a comparator, the comparator sequence must be the inverted of the expected sequence. In the present example this is a single pulse synchronized to the expected "0" in the input sequence. Fig. 1 (a) reveals the disadvantage of the AND-comparator: it is insensitive to bit-errors synchronized to "0"s in the comparator sequence, which means that the probability of detecting a single bit-error will be given by the ratio of "0"s to "1"s of the input sequence to be identified (in this case 25%). Using an XOR gate instead, as shown in Fig. 1 (b), with a comparator sequence equal to the expected sequence in the input pattern, all bit-differences are identified and result in a pulse at the output. However, since the XOR comparator sequence consists of "0"s outside the time span containing the expected sequence, all bits in the input pattern outside this time window will be transmitted to the output. Consequently, a simple detection of P.D. power surge will not reveal the presence of errors. An additional gate is needed at the output to suppress the bits outside the window of interest, before the result can be detected. This gating procedure is obviously not needed with the AND-comparator, since the output is inherently "0" outside the time window of interest. This property of the AND gate can be exploited as shown in Fig. 1 (c), where the output of the XOR comparator is gated by a pulse equal in duration - and synchronized to – the time window of interest. Rather than using a separate AND gate, the gating function has been implemented using the same MZI that performs the XOR operation, thus reducing complexity and increasing cost-effectiveness. The principle of operation is explained with reference to Fig. 2, which illustrates the experimental setup schematically: the MZI is balanced to obtain destructive interference at the output of a signal injected into the common arm (labeled G) in the case where both input signals D1 and D2 are off. A logic "1" bit in either input changes the phase in the corresponding arm by π, and thereby changes the output state of the MZI to constructive interference. A "1" bit in both inputs leaves the state of the interferometer unchanged, and the XOR truth-table is realized.

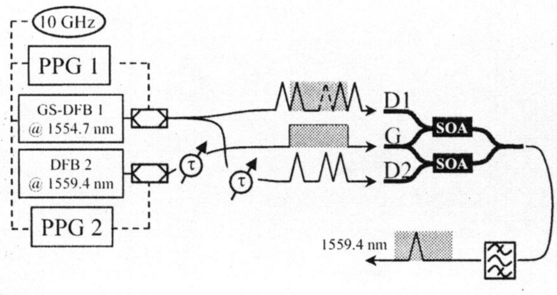


Fig. 2. Experimental setup of new comparator scheme

The signal G launched into the common arm samples the state of the MZI, and consequently it is seen that the logic function obtained at the output of the filter is G AND (D1 XOR D2). In other words the function depicted in Fig. 1 (c) can be realized with a single MZI by injecting the synchronized gating pulse into the common arm.

## Experiments and results

As indicated in Fig. 2, the AND-XOR data segment comparator is demonstrated using two 10 Gb/s pattern generators (PPGs) to drive two modulators independently. PPG1 modulates a PRB sequence ($2^7$-1) onto a 10 GHz train of ~25 ps wide pulses emitted from a gain-switched DFB laser (DFB1) at a wavelength of 1554.7 nm. This signal is split in two, and forms the two input data signals D1 and D2. A variable delay in the arm carrying D2 ensures synchronization between the bits in the two signals. PPG2 modulates a periodic signal consisting of 63 NRZ "1"s followed by 64 "0"s onto a CW beam from a DFB laser (DFB2) at a wavelength of 1559.4 nm. This is the gating signal G, which passes through a synchronizing delay line before being injected into the common arm of the MZI. The result is shown in Fig. 3 in the form of data pulse patterns. The 3 rows from the top contain data signal 1 (D1), data signal 2 (D2), and the gating signal (G). The bottom row shows the gated XOR-compared output G AND (D1 XOR D2). The output pulses are observed to be somewhat broader than the input pulses. This is due to the finite gain/phase response of the device, which may be compensated for by letting G consist of RZ pulses of width smaller than, or comparable to, the input data signals (see e.g. [2]).

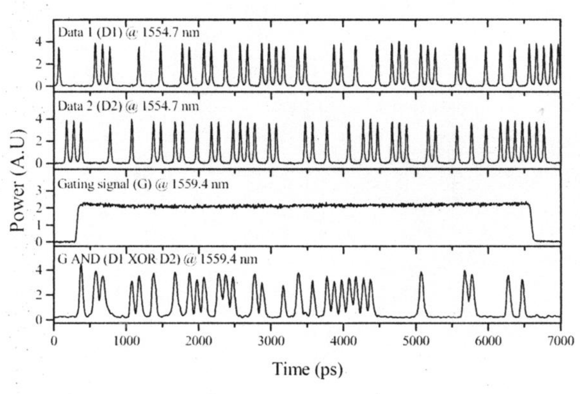


Fig. 3. The two input data patterns (D1, D2), the gating pulse (G), and the output of the comparator.

The output extinction ratio (ER) is 10 dB and the optical signal-to-noise ratio (OSNR) is ~30 dB/ 0.1 nm, which are indicators of a good signal quality. We were not able to measure bit error rates (BERs) due to a technical problem with PPG2. However, by replacing the gating pulse with a CW beam, still at 1559.4 nm, BERs were measured on the resulting D1 XOR D2 output, and as observed in Fig. 4 the operation is penalty-free. To the authors' knowledge this is the first BER measurement on an MZI-XOR gate, using PRBS data for both input signals. The BER performance of the gated XOR signal is expected to be slightly degraded compared to Fig. 4, although the only difference is the modulation of the gating signal, G. The reason for this is that the peak power in the gating pulse cannot be as high as the (optimum) power of a corresponding CW beam. This is because the large contrast in the "0" to "1" transition gives rise to a gain-saturation induced temporal overshoot of the output, which ultimately leads to a reduction of the extinction ratio.

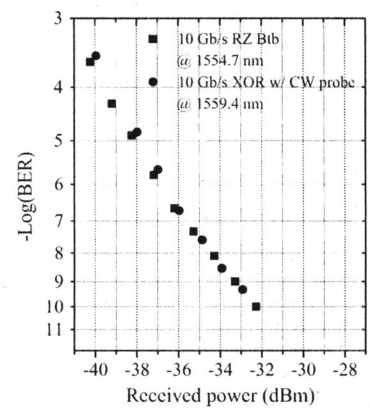


Fig. 4. BER performance of MZI-XOR comparator

## Conclusions

A new pattern recognition scheme capable of comparing a *segment* of a data stream to an expected sequence has been proposed. The principle makes use of the logic AND and XOR functions, and has been demonstrated in a single all-active, polarization independent MZI at 10 Gb/s with good results.

## References


/1/ O. Leclerc, Technical Digest OFC 2002, Anaheim, USA, March 2002, paper TuN1.

/2/ M. L. Nielsen et al., Technical Digest OAA 2002, Vancouver, Canada, July 2002, paper OTuD.

/3/ T. Fjelde et al., IEEE Phot. Techn. Lett., vol. 13, no. 7 (2001), pp. 750-52.

/4/ K.L. Hall et al., IEE Electr. Lett., vol. 32, no. 13 (1996), pp. 1215-16.

/5/ J.-P. Elbers, Technical Digest OFC 2002, Anaheim, USA, March 2002, paper ThD3.

/6/ B.-K. Kang et al., Proceedings of LEOS 2000, Puerto Rico, USA, November 2000, paper MM3.

/7/ T. Fjelde et al., IEE Electr. Lett., vol. 32, no. 22 (2000), pp. 1863-64.

/8/ K.L. Hall et al., Opt.Lett. vol. 23, no. 16 (1998), pp. 1271-3.

/9/ C. Bintjas et al., IEEE Phot. Techn. Lett. Vol. 12, no. 7 (2000), pp. 834-36.

/10/ C. Janz et al., Technical Digest OFC 1999, San Diego, USA, March 1999.