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SOI SILICON ON GLASS FOR OPTICAL MEMS

Kristian. P. Larsen*, Jan. T. Ravnkilde**, Ole Hansen*

*MIC, Technical University of Denmark, 2800 Lyngby, Denmark, **Dicon A/S, Denmark

E-mail: kpl@mic.dtu.dk

ABSTRACT

A newly developed fabrication method for fabrication of single crystalline Si (SCS) components on glass, utilizing Deep Reactive Ion Etching (DRIE) of a Silicon On Insulator (SOI) wafer is presented. The devices are packaged at wafer level in a glass-silicon-glass (GSG) stack by anodic bonding and a final sealing at the interconnects can be performed using a suitable polymer. Packaged MEMS on glass are advantageous within Optical MEMS and for sensitive capacitive devices. We report on experiences with bonding SOI to Pyrex. Uniform DRIE shallow and deep etching was achieved by a combination of an optimized device layout and an optimized process recipe. The behavior of the buried oxide membrane when used as an etch stop for the through-hole etch is described. No harmful buckling or fracture of the membrane is observed for an oxide thickness below $1\mu\text{m}$, but larger and more fragile released structures will need a thinner oxide in order to prevent damage.

INTRODUCTION

This work describes a new fabrication method for silicon devices on glass, which enables sealing and stacking possibilities in a glass-silicon-glass configuration. Since the devices are built using DRIE of the silicon device layer of an SOI wafer, the method is superior to conventional Poly-Si surface micromachining with respect to layer thicknesses and internal stress control. Integration of single crystalline silicon structures on a glass substrate provides several attractive properties for MEMS and optical MEMS: 1) Capacitive devices will benefit from low RF losses at high frequencies and low parasitic capacitances [1]. 2) Optical applications such as spatial light modulators (SLM), displays, pixel arrays, scanning [2], and optical sensing in micro fluidic systems.

The presented method allows packaging on wafer-level which is attractive, as packaging often represents a great part of the production costs. Another recent work on SOI-glass wafer-level packaging is done in [3] for fabrication of micro resonators. With our method the GSG wafer-level package is obtained by anodic bonding

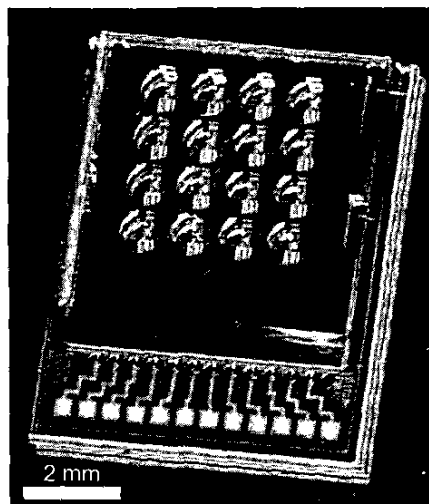


Figure 1: A complete packaged glass-silicon(SOI)-glass chip with bonding pads at the bottom.

of two glass wafers, which makes it more suitable for Optical MEMS. The package is prepared for further integration with micro optical components optimized for various optical applications.

The fabrication process is relatively fast and simple. The most critical part is control of the DRIE steps regarding the sidewall slopes and uniformity of the etch across the wafer and for the different geometries within the chip. To handle this, different device designs and etch parameters has been tested.

FABRICATION

Fabrication is performed using double sided polished SOI wafers with a $460\mu\text{m}$ handle wafer, $1\mu\text{m}$ oxide and $50\mu\text{m}$ device layer thickness. The first mask step defining the Anchor pattern is defined using a $1.5\mu\text{m}$ photoresist (PR) mould, which is transferred into $3.9\mu\text{m}$ deep trenches in the SOI device layer by RIE, see Fig. 2.A1. A standard parallel plate RIE system from STS is used for this step and the process consists of: an 11min anisotropic Si etch (8sccm SF_6 , 32sccm O_2 , at 80mTorr

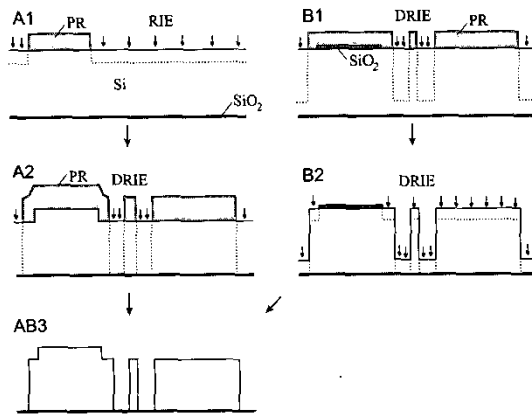


Figure 2: Two alternative device layer processes, A1-A2 is recommended and used.

and 30W), followed by resist stripping in an oxygen plasma. The next mask step is performed with 6.2µm PR as shown on Fig. 2.A2. An initial short buffered hydrofluoric acid (BHF) dip is necessary for good adhesion of the resist. Since this step defines the mechanically active structures, great care must be taken with the photolithography. DRIE is now applied using a STS advanced Silicon Etcher (ASE) with a standard shallow etch (passivation gas C₄F₈, etch gas SF₆) with increased gas flows, optimized for high uniformity of the etch. The etch stops at the buried oxide layer, but notching of the sidewalls is seen with continued etch. Insufficient etch results in footing of the structures and is even less wanted, thus a precise control of the etch depth is needed. One should be aware of the specified variation of the SOI device layer thickness. This thickness can be estimated by measuring the step height at the wafer edge with a profilometer. We have achieved acceptable etch depth control by observation of certain indicator structures and subsequent additional etching. After successful etching the resist is removed in an oxygen plasma, Fig. 2.AB3.

Fig. 2.B1-3 describes an alternative process that can be used when larger release heights are needed. Here, both lithographic steps are performed on a flat surface. First, the Anchor pattern is transferred to a thin oxide layer. Then, the mechanically active structures are etched as described above. However, the etch is not stopped on the buried oxide, but it is timed so that the intended release height is remaining. After stripping of the PR in an oxygen plasma the remaining silicon is etched using the oxide mask.

Before anodic bonding the wafers are carefully cleaned in Piranha (80% H₂SO₄ + 20% H₂O₂). Glass substrates (Pyrex 7740, 500µm thick) are processed in

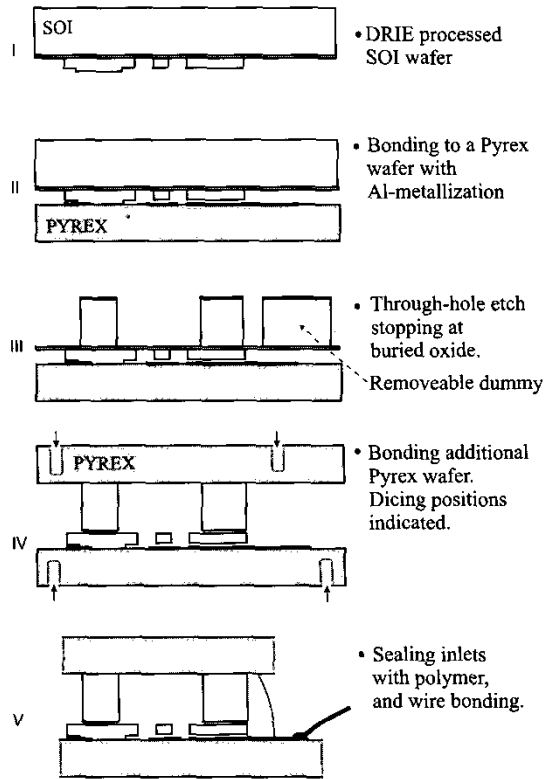


Figure 3: Process sequence continued.

parallel using the following sequence. After careful cleaning of the glass substrate 500nm of aluminum is deposited by e-beam evaporation. The metal is then patterned with 1.5µm PR and etched in H₃PO₄ based Al-etch. Finally, the resist is stripped in an oxygen plasma. The substrates were aligned with a precision of 2µm and anodically bonded at 300°C. During bonding the voltage is ramped up to V_{max}=600V, while the current should not exceed I_{max}=2mA. When the current has dropped below 0.5mA, an additional 10 minutes latency is used before shutting off the voltage. The bonded wafers, sketched in Fig. 3 II, are rinsed in DI-water and BHF. The backside of the SOI wafer is patterned with the through-hole etch mask in 13µm PR with alignment to the silicon device layer. In order for the glass side to electrostatically clamp in the ASE, the glass surface is covered by 100nm aluminum by e-beam evaporation. Through-holes in the silicon handle wafer are etched using DRIE with a standard deep-etch stopping on the buried oxide membrane, see Fig. 3 III. The PR is removed in an oxygen plasma and the oxide membrane is removed in a RIE glass etch (20sccm CF₄, 20sccm CHF₃ at 100mT and 60W). An additional glass

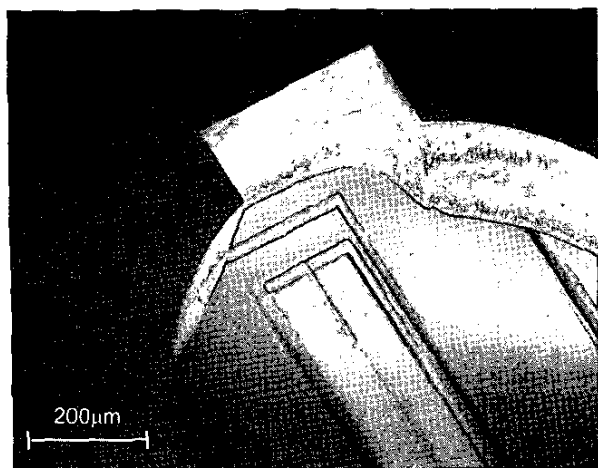


Figure 4: SEM image showing 460 μm high spacer structures and the 45 μm high mechanical device on a glass wafer with a metallization pattern.

wafer is anodically bonded on top of the wafer stack. The bonding is performed at 300°C, $V_{max}=1000\text{V}$, and $I_{max}=2\text{mA}$. Finally, the aluminum layer on the backside of the stack is removed by etching. The dicing into chips is discussed in the next chapter.

Fig. 5 show an example of a fabricated device. At Fig. 4 and 6 the devices can be seen together with the walls from the wafer through-hole. A finished chip is shown on Fig. 1. The devices have beams as narrow as 2 μm with a height of 46 μm , elevated 4 μm above the glass substrate. Electrode gaps were controlled down to 0.5 μm .

RESULTS AND DISCUSSION

DRIE Uniformity Optimization.

The most challenging process step in this method involves control of the DRIE. Both micro and macro loading effects and diffusion limited etching are present and result in uneven etch rates. In Fig. 5 notching is seen on certain trenches and not on others. This is caused by different etch rates due to the micro loading effect. The macro load of the wafer goes to zero as the etch reaches the oxide everywhere, so a uniform etch is much appreciated. By placing dummy structures it is partly possible to control the loading effect to avoid notching at critical places. A recipe with a high gas flow rate and a low etch power was found to give the most uniform etch, reducing the effects of micro and macro loading. This etch also showed acceptable sidewall slopes. For very small openings below 5 $\mu\text{m}\times 5\mu\text{m}$, the etch rate becomes diffusion limited and the etch rate is smaller. This effect can be utilized to reduce the proof mass of movable

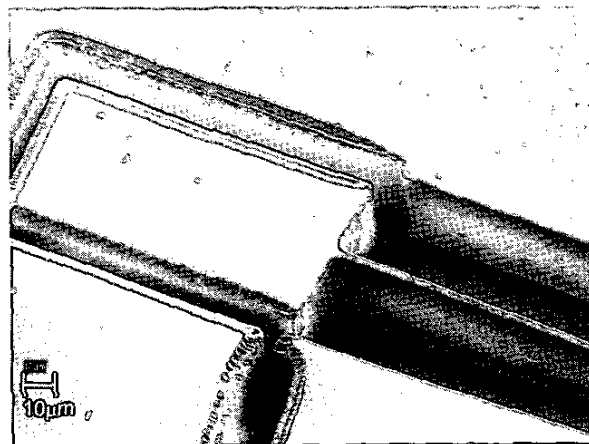


Figure 5: A beam test device. Note notching is prominent near the narrow trenches but absent at the large open areas of the narrow suspension beam.

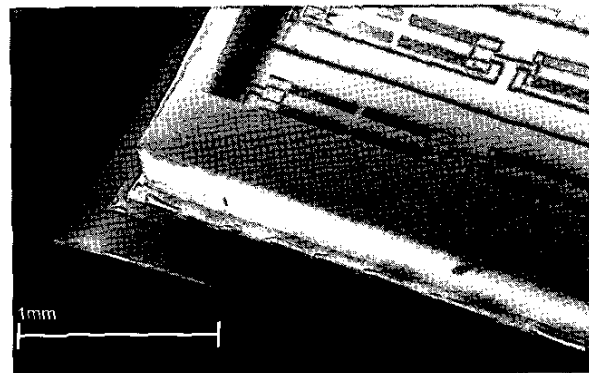


Figure 6: Beam test devices and the walls surrounding a chip with no glass lid.

parts by non-penetrating holes.

For the through-hole etching the uniformity is also important, especially at macro loading level, where it results in a higher etch rate at the edges of the wafer compared to the center. This is greatly reduced by lowering the overall load of the wafer. Dummy structures suspended only by the oxide membrane can be employed, and removed after the final etching of the oxide membrane, see Fig. 3 III. A uniform through-hole etch is needed to enable the thinnest possible buried oxide thickness The importance of which is explained in the next section.

Buried oxide as etch stop for through-hole etch.

As the through-hole etch reaches the buried oxide, the membrane buckles due to compressive stresses. Tests

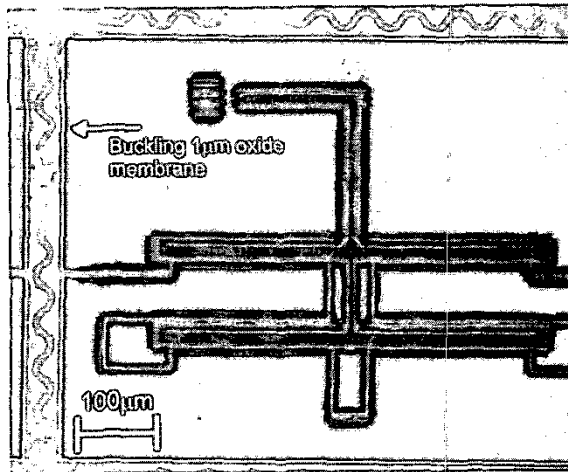


Figure 7: Optical image of the 1 μm buckling membrane after the through-hole etch (visible at the trenches) No damage is seen on the fragile movable parts of the beam bending device.

with a 2 μm membrane showed buckling and major rupture of the components. For a 1 μm membrane rupture is observed occasionally. Generally, the membrane should be as thin as allowed by the over etch from uniformity of the DRIE. The selectivity to oxide is specified to 1:250. A higher wafer temperature during etching due to low heat conductance through the glass wafer may reduce the selectivity. A membrane thickness of 0.5 μm is proposed to be optimal for the process, and should withstand more than 100 μm of over etch.

Bonding of SOI and Pyrex.

The exact mechanism behind anodic bonding of SOI and Pyrex has been debated. Nevertheless we have had no problems, and have bonded with standard conditions, but with increased duration of the bonding to a total of 20-30 minutes, since the bonding current is lower. The bonding time is expected to depend on the quality of the buried oxide of the SOI wafer. Though we have not measured the bonding strength, we have had no difficulties in bonding SOI wafers with buried oxide thicknesses of 0.1-2 μm . Structures with anchor sizes down to 20 $\mu\text{m} \times 20 \mu\text{m}$ have been fabricated.

Dicing and Sealing Procedures.

Figure 3 IV shows a proposed dicing procedure for the chips. It is important not to dice the whole way through the glass as the feed inlets still are open and sensitive

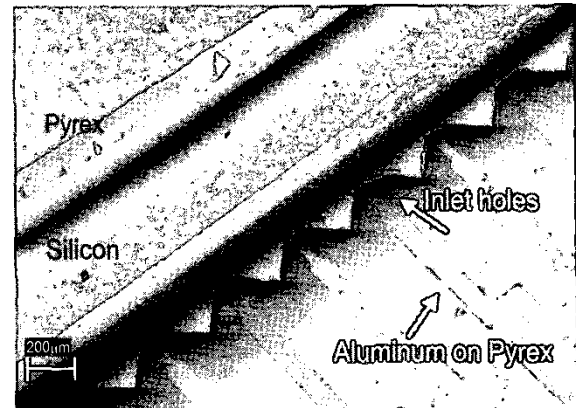


Figure 8: Aluminum feed-throughs into the chip with a glass lid. Sealing can be obtained by application of a suitable polymer as shown in Fig. 3 V.

water and dust. After breaking into chips, the final sealing can be performed by placing a suitable polymer over the inlet holes which are 4 μm high and 100 μm wide per metal wire. The inlets are shown on Fig. 8.

CONCLUSION AND FURTHER WORK

A fabrication method for wafer-level packaged MEMS devices in a GSG stack has been developed. The method utilizes DRIE of a SOI wafer, and anodic bonding to glass forming high aspect ratio single crystalline components on glass. The buried oxide membrane is used as etch stop and requires precise control of the DRIE in order to avoid notching from overetch. Reducing the overetch will also allow for a thinner oxide membrane of the SOI wafer, which will reduce harmful buckling effects.

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