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A 10-BIT 100 MSAMPLES/S BICMOS D/A CONVERTER

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ABSTRACT

A 10-bit 100MSamples/s current-steering D/A converter (DAC) has been designed and processed in a 0.8μm BiCMOS process. The DAC is intended for applications using direct digital synthesis, and focus has been set on reducing dynamic nonlinearities to achieve a high spurious free dynamic range (SFDR[1]) at high generated frequencies. The main part of the DAC consists of a matrix of current cells. Each current cell contains an emitter-coupled logic (ECL) flip-flop, clocked by a global ECL clock to ensure accurate clocking. A bipolar differential pair, steered by the differential output of the ECL flip-flop, is used in each current cell to steer the current. The DAC operates at 5V, and has a power consumption of 650mW. The area of the chip-core is 2.2mm × 2.2mm. The measured integral nonlinearity (INL) and differential nonlinearity (DNL) were both approximately 2 LSB. At a generated frequency of $f_g \approx 0.3 f_s$ (f_s = 100 *MSamples/s*), the measured SFDR was approximately 43dB.

I. INTRODUCTION

High-speed and high resolution DACs are used in various applications such as direct digital synthesis (DDS), arbitrary waveform generation (AFG), new TV/Video systems and communications local oscillators. For these applications the dynamic performance of the DAC is very critical. For the DAC described in this paper, focus has been set on achieving a high spurious free dynamic range (SFDR) at high generated frequencies, f_g, compared to the conversion rate, f_s (100*MSamples/s*), i.e., $f_g \approx 0.3 \cdot f_s$. Any static or dynamic nonlinearity will generate spurious frequencies at the DAC output. For current steering DACs static nonlinearities can be reduced significantly by careful layout and by using different kinds of switching schemes for the current cells [5], [6]. The main dynamic nonlinearities are nonequal and code dependent rise and fall times, delay between rise and fall transients, and nonlinear clock and data feedthrough. For a typical current steering DAC one of the main challenges is to generate steering signals for the current cells with very little skew [1], [3], [5]. A solution is to use clocked current cells. One then has to generate a global clock for the current cells that has an acceptable low clock skew over the current cell matrix. Clock-skew can more easily be controlled than the delays of different steering signals, therefore the use of clocked current cells is an advantage.

The DAC presented in this paper is constructed using this scheme. Each current cell contains an ECL flip-flop. The skew between the steering signals for the different current cells are then controlled by a global clock signal.

The DAC architecture is described in section II, and the current cells are described in section III. Section IV gives some considerations about the chip layout, and in section V the measurement results are presented.

II. DAC ARCHITECTURE

The DAC is based on the well-known current steering principle [1]-[7]. The DAC architecture is shown in Fig. 1.

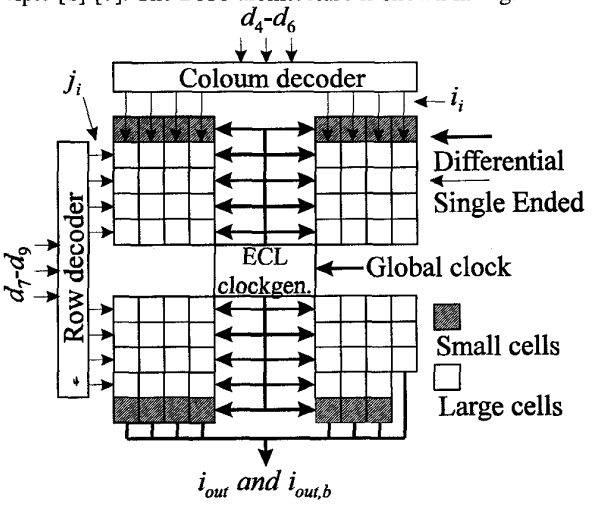

Fig. 1. DAC Architecture

The main part of the DAC consists of a matrix of current cells. The current cells are arranged in a matrix. This matrix consists of 63 large current cells that determine the 6 most significant bits (6 MSB), and 15 smaller cells that determine the 4 least significant bits (4 LSB). One large current cell sinks a current 16 times the current in a small current cell. The DAC operates as follows: The digital input word, d_9(MSB)-d_0(LSB), is stored in an input register. The 6 MSB

[1] SFDR is measured from the generated frequency to the highest harmonic or non-harmonic spur within the frequency band 0-f_s/2.

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are decoded into row, j_0 to j_7, and column, i_0 to i_8, signals. All signals (the 4 LSB, i_p and j_q) are then latched before fed to the current cells. In Fig. 1 the registers and latches are contained in the column and row decoders. The decoding ensures that a minimum number of the large current cells are turned on or off; this reduces dynamic nonlinearities. The hierarchical switching scheme [6] is used for the large current cells to reduce nonlinearities. This switching scheme reduces both symmetrical and graded errors. For the small current cells, a simple "chessboard scheme" is used controlled by the digital signals d_3-d_0.

In each current cell (see Fig. 2) the CMOS steering signals, i_p, i_{p+1} and j_q, are decoded by CMOS logic. The decoded signal is then converted into ECL levels and latched by an ECL flip-flop clocked by the global differential ECL clock. Thus, one reduces the problem with skew between the steering signals over the matrix. The differential current outputs of all current cells are connected to the DAC output pins i_{out} and $i_{out,b}$ as shown in Fig. 1. These are, externally, each connected to a 50Ω resistor that again is connected to the positive power supply ($5V$). The maximum output current from the DAC is designed to be $20mA$. The ECL clock generator is placed in the middle of the current cell matrix to minimise clock skew. This also causes the clock skew to be a symmetrical error. Therefore it will be reduced by the hierarchical switching scheme.

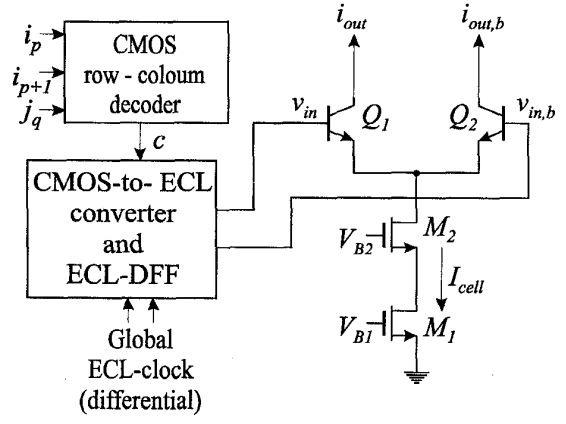

Fig. 2. The large current cell

III. CURRENT CELLS

In a previous design of a $100MSamples/s$ 10-bit DAC [1] the INL and DNL were found to be less than 1 LSB. The static nonlinearities for this DAC were acceptable whereas the dynamic performance at high generated frequencies compared to the sampling rate was very poor. Focus in the design of the DAC presented in this paper was therefore set on reducing dynamic nonlinearities to reduce the effects of these at high generated frequencies. This was done be designing very fast current cells.

A simplified schematic of the large current cells is shown in Fig. 2 [2]. A differential pair with bipolar transistors, Q_1 and Q_2, is used to steer the current. The cascode current sink consists of two NMOS transistors M_1 and M_2. The current cell includes a CMOS input section which decodes the row and column signals. The decoded signal is converted into a differential ECL signal that is latched before fed to the differential pair, Q_1 and Q_2.

The use of a bipolar differential pair offers several advantages compared to the MOS counterpart. As the DAC should operate at a very high conversion rate, it is obvious to use fast bipolar transistors to toggle the current I_{cell} between the two outputs. Furthermore, the required voltage swing at the input, v_{in}-$v_{in,b}$, is much lower compared to the input swing of a MOS differential pair in a practical design. The differential input voltage which guaranties that the total erroneous output current from all N_{cells} current cells is less than 1/2 LSB of the total current, is given by (1). In (1) the collector currents I_{C1} and I_{C2} are given by the well-known exponential equation for the bipolar transistor. V_T is the thermal voltage which equals $26mV$ at room temperature.

$$\frac{I_{C1}}{I_{C2}} > 2^{N+1} N_{cells} \Rightarrow \Delta v_{in} = v_{in} - v_{in,b} > V_T \ln(2^{N+1} N_{cells}) \quad (1)$$

Using the number of bits N = 10, N_{cells} = 64 (63 large, plus 15 small which equal approximately 1 large) we find that $\Delta v_{be} > 12V_T = 312mV$. This small ECL voltage swing and the fast ECL flip-flop output signals potentially give low dynamic nonlinearities at the DAC output.

The setup time of the output, c, from the CMOS input section in the current cell varies strongly depending on the input signals i_p, i_{p+1} and j_q. If these CMOS signals, c, were used to steer the current cells directly the output signal from the DAC would contain higher levels of nonlinearities. The output from the CMOS part is therefore latched in the ECL section. The skew between the steering signals, v_{in} - $v_{in,b}$, is therefore only dependent on the clock skew in the global ECL clock. The worst case clock skew over the matrix is designed to be less than $8ps$.

The small current cells have the same architecture as the large ones but i_p is connected to V_{dd}, i_{p+1} is connected to ground and the cells are only steered by j_q.

For the bipolar transistor the relation between the terminal currents is $I_e = I_b + I_c$ or $I_e = (1+\beta)\cdot I_b$. The current amplification factor, β, is process dependent and as bipolar transistors are used in the differential pair it is important to evaluate the influence of this in the collector current. We find:

$$I_c = \alpha \cdot I_e , \quad \alpha = \frac{\beta}{1+\beta} \quad (2)$$

The sensitivity of α with respect to β:

$$S_\beta^\alpha = \frac{\partial \alpha}{\partial \beta} \cdot \frac{\beta}{\alpha} = \frac{1}{(1+\beta)^2} \cdot \frac{\beta}{\alpha} \quad (3)$$

The relative variation in α is approximately given by

$$\frac{\Delta\alpha}{\alpha} \approx S_{\beta}^{\alpha}\frac{\Delta\beta}{\beta} \qquad (4)$$

Assuming $\beta = 120$ and $\Delta\beta/\beta$ better than 2% for transistors on the same chip, one obtain a $\Delta\alpha/\alpha$ of approximately 0.02%. This will be of minor importance compared to other mismatch sources, such as ground potential variations and mismatch between NMOS current sinks (i.e., geometrical mismatch, threshold mismatch etc.).

IV. Layout Considerations

The DAC is processed in a 0.8μm double-metal double-poly BiCMOS process. To minimise switching noise from the CMOS- and ECL-logic to couple to the output of the DAC, the power supplies for the CMOS- and ECL-logic and the current sinks are routed separately. The current I_{cell} from each large current cell introduces a voltage drop in the analogue ground. The analogue ground wires are therefore made wide. Also, several pads on each side of the current cell matrix are used to connect the analogue ground. Furthermore, all different parts of the circuitry are surrounded by guardrings and all major parts by double guardrings to minimise noise injected to the output through the substrate. A separate power pad has been used for the n-well parts of the guard rings. All bias lines, both to the ECL-logic and the current sinks in the current cells, have both local and global decoupling capacitors. Horizontal and vertical shielding between the analogue routing and digital data lines (both CMOS and ECL) have been used to minimise coupling between these. Careful layout and design were necessary to obtain sufficient time margin for the data setup with respect to the ECL clock. The chip was mounted in a 44 pin CLCC package.

Clock skew, ground potential variation, etc., that generate dynamic nonlinearities at the DAC output have been taken into account and were designed to introduce errors at the output, each less than ½ LSB. The switching scheme will tend to cancel must of them. The total error at the output is therefore not the sum of all errors. The size of the chip-core is $2.2mm \times 2.2mm$.

V. Experimental Results

The performance of a DAC is normally evaluated by considering the static and dynamic nonlinearities. The static nonlinearities INL and DNL are presented in Fig. 3 and Fig. 4. All measurements were performed with single ended output as no differences were seen between single ended and differential output.

The INL and DNL show that the current cells are not matched within an accuracy of 10 bit.

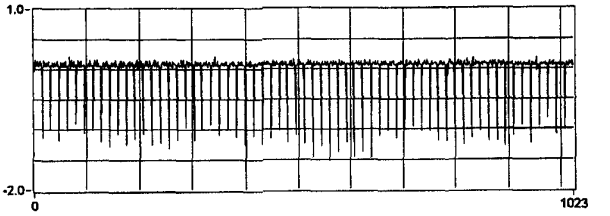

Fig. 3. Measured differential nonlinearity (DNL) versus input code.

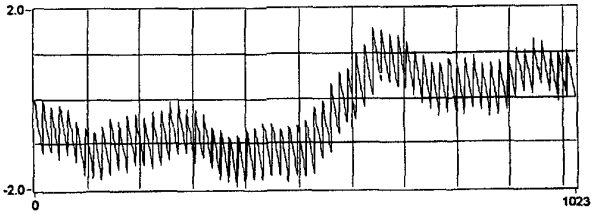

Fig. 4. Measured integral nonlinearity (INL) versus input code.

The dynamic performance of the DAC can still be evaluated separately. This is done by letting the DAC generate two different frequencies, one low and one high. When generating a low frequency the static nonlinearities will dominate and cause the spurious frequencies at the output. At high frequencies the dynamic nonlinearities will dominate and the effect of these can be viewed as the difference between the two spectra.

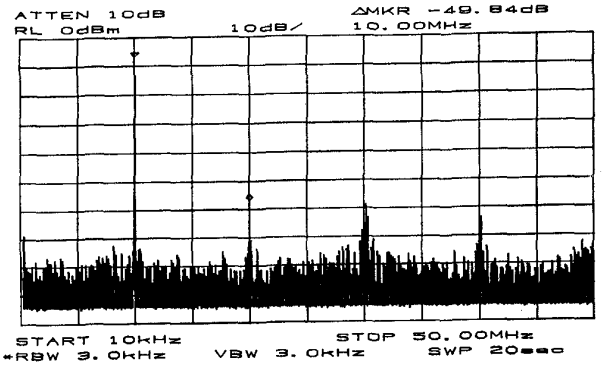

Fig. 5. The measured spectra for $f_s = 100MSamples/s$; $f_g = (820/8192)\cdot f_s \approx 0.1\cdot f_s$.

The dynamic performance is evaluated by forcing a digital sine-wave to the input of the DAC. The digital sines are saved in a cyclic 8*k*-memory, i.e., 8192 samples with no delay in the cyclic readout. To ensure phase continuity the data are obtained by generating f_g as $(n/8192)\cdot f_s$, n integer. A Colby Instruments Inc. SG8000A was used as the reference clock and an HP8563A spectrum analyser was used to

measure the spectra which are presented in Fig 5 and Fig. 6 for $f_g \approx 0.1 \cdot f_s$ and $f_g \approx 0.3 \cdot f_s$. The result in Fig. 5 shows that the SFDR is approximately 50dB at $f_g \approx 0.1 \cdot f_s$. The SFDR in Fig. 6 is further reduced by 7dB to approximately 43dB.

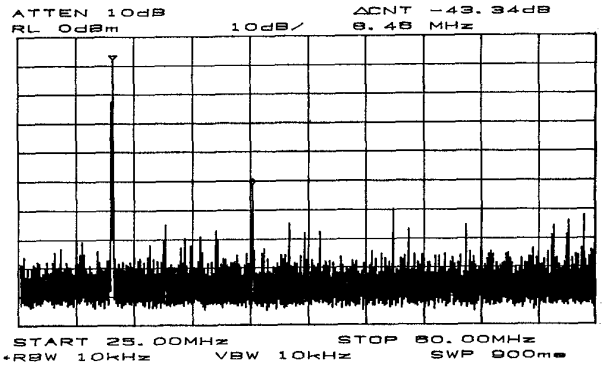

Fig. 6. The measured spectra for $f_s = 100MSamples/s$; $f_g = (2501/8192) \cdot f_s \approx 0.3 \cdot f_s$.

For three different ratios between the generated frequency and sampling frequency the SFDR was measured for $10MHz < f_s < 150MHz$. The results are shown in Fig. 7.

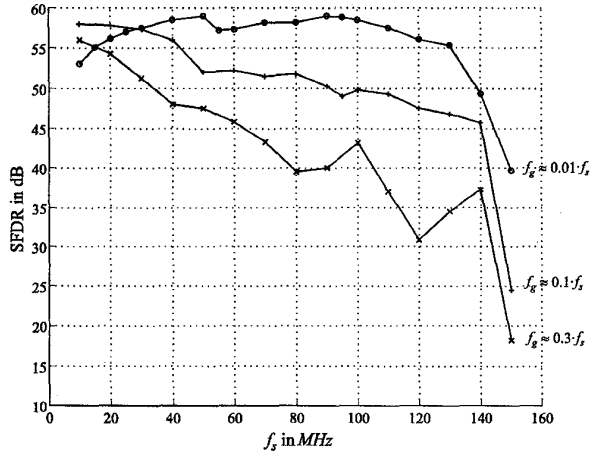

Fig. 7. The measured SFDR for $f_g = (79/8192) \cdot f_s \approx 0.01 \cdot f_s$, $f_g \approx 0.1 \cdot f_s$ and $f_g \approx 0.3 \cdot f_s$ as a function of f_s.

From Fig. 7 it can be seen that the DAC operated up to a sampling rate of $140MSamples/s$ after which the DAC did not generate a sine wave at the output. This was due to internal timing problems. The SFDR at $f_s = 140MSamples/s$ is approximately $6dB$ lower than that of the test with $f_s = 100MSamples/s$. This corresponds well with the fact that the energy of one LSB is approximately halved and the dynamic nonlinearities are the same which result in a reduction in the SFDR of 6dB. The power consumption was $650mW$. Because the INL and DNL are larger than 1 LSB one does not obtain a SFDR of 60dB at low generated frequencies compared to the sampling frequency. For a constant ratio between f_g and f_s the SFDR increases when f_s is decreased. This is again due to the fact that the dynamic nonlinearities become relatively less significant as the energy of one LSB is increased.

VI. Conclusion

A 10-bit $100MSamples/s$ current steering DAC has been designed and fabricated in a $0.8\mu m$ BiCMOS process. The core of the DAC consists of a matrix of current cells. Each current cell includes CMOS decoding logic, a CMOS-to-ECL converter, an ECL flip-flop and a bipolar differential pair to steer the current. The ECL flip-flop is clocked by a global ECL differential clock, and the differential output of the flip-flop directly steers the bipolar differential pair. The measured static nonlinearities INL and DNL were both approximately 2 LSB. The measured SFDR was $43dB$ at a generated frequency of approximately $0.3 \cdot f_s$ ($f_s = 100MSamples/s$) and $50dB$ at approximately $1/10 \cdot f_s$.

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