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Design and Characterization of Vertical Mesh Capacitors in Standard CMOS

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Abstract

This paper shows how good RF capacitors can be made in a standard digital CMOS process. The capacitors which are also well suited for binary weighted switched capacitor banks show very good RF performance: Q-values of 57 at 4.0 GHz, a density of 0.27 fF/μm^2, 2.2 μm wide shielded unit capacitors, 6% bottom plate capacitance, better than 3-5% process variation and negligible series inductance. Further a simple yet accurate method is presented that allows hand calculation of the capacitance value.

Introduction

Only a decade ago it was considered impossible to make good radio frequency integrated circuits in digital CMOS processes due to the lack of good passive components and slow transistors. Since then the massive investments in digital CMOS have resulted in exceedingly fast devices and many metal layers as standard. These many metal layers have made on-chip inductors feasible by reducing ohmic loss. Further on-chip inductors have one very nice property. Because the inductance value is dependent on large physical dimensions in processes where dimensions are controlled to less than 0.1 micron the inductance value is highly repeatable. Typical lot-to-lot variations are better than 1%. Meanwhile RF IC designers have grown accustomed to using huge safety margins in for instance VCO tuning range to make up for at least ±10% capacitance variation in the thin film capacitors (poly-poly or metal-metal) they use in the specialized RF IC processes. These safety margins lower the achievable RF performance and therefore high-Q capacitors with better tolerances are very desirable. Another consequence of the rapid CMOS process development is that now CMOS switches have very good RF performance. This has created an alternative to the use of varactors as frequency selective devices. By switching between a number of binary weighted capacitors it is now possible to achieve the same tuning range and as-good-as or better Q-value with a linear capacitance.

Capacitor Construction

Today oxide layers and metal layers in digital CMOS processes are typically kept larger than 0.5 micron to minimize RC delays. At the same time minimum metal spacing is dropping to significantly below 0.5 micron to improve the density. This means that now lateral capacitance contributions are significantly larger than the vertical contributions between different metal layers.

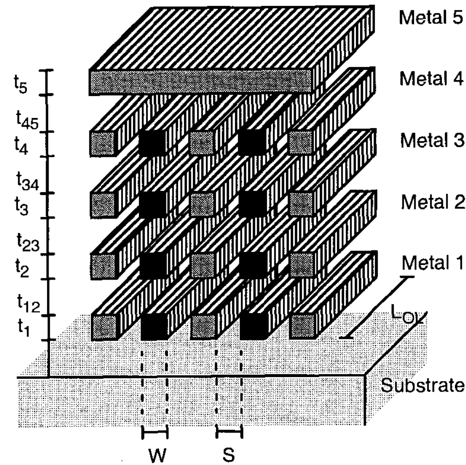

Figure 1. Four Stacked Lateral Flux Capacitors. Fingers with dark cross-sections are connected to one port. The remaining fingers are connected to the other port.

Therefore using interleaved metal fingers results in higher capacitance per area (see figure 1). Higher capacitance per area can be achieved by shifting the fingers in each layer [1] but the improvement is minor compared to the solution that is shown in figure 1. Further this solution can be improved by connecting all fingers with vias and thereby creating extra lateral capacitance contribution (figure 2). By doing so we have formed vertical metal meshes that are completely shielded from each other. This and the fact that each vertical capacitor unit is only roughly two microns wide makes them ideal as unit capacitors used in binary weighted switched capacitor banks that need to be well matched even at RF frequencies. In figure 2 we can also see that there is some parasitic bottom plate capacitance. For this structure the bottom plate capacitance is very small i.e. in the order of 5% of the mesh capacitance but if the bottom plate capacitance is a problem e.g. due to substrate losses or capacitive division metal1 can be used as a ground plane or as a bottom shield just like metal5 is used as a top shield in figure 2. This reduces loss in the first case and removes C_{par} in the second case at the expense of lower capacitance per area.

Capacitance Calculation

For a vertical mesh capacitor using four layers of lateral capacitance contributions like the one in figure 2 it is clear that the capacitance of each vertical mesh (C_{mesh}) is a

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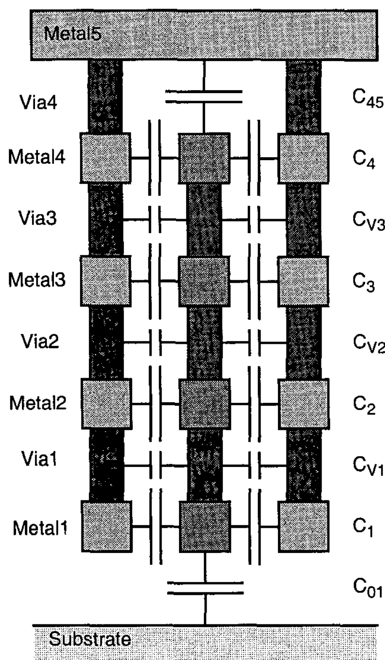

Figure 2. Cross-Section of a Vertical Mesh Capacitor. Stacked fingers are connected by vias and thereby forming vertical meshes. The result is very narrow high-Q encapsulated capacitors that are ideal for binary weighted switched capacitor banks at RF frequencies.

combination of seven lateral capacitance contributions and one vertical (1) while the parasitic capacitance to ground is equal to C_{01} (2).

$$C_{mesh} = 2(C_1 + C_{V1} + C_2 + C_{V2} + C_3 + C_{V3} + C_4) + C_{45} \quad (1)$$

$$C_{par} = C_{01} \quad (2)$$

In order to be able to estimate what C_{mesh} and C_{par} amount to it is necessary to characterize each of these nine contributions separately. Fortunately there are only three types of capacitance contributions that are different in nature so it is sufficient to derive three capacitance formulas.

Before doing so a number of definitions are made to ease the presentation (see next column). Each of these definitions refers to a parameter that is shown on figure 1, figure 2 or figure 3. Note that the virtual parallel plate capacitance areas are parallel plate capacitance areas that are increased enough to take the fringing capacitance contributions into account as well. I.e. if the fringing capacitance constitutes 25% of the parallel plate capacitance then the virtual parallel plate capacitance area is simply made 25% larger than the actual parallel plate capacitance area. This way the individual capacitance contributions including the fringing effects can be calculated by simply using the parallel plate capacitance formula (3) with A_{plate} being the virtual parallel plate capacitance area.

A_i	virtual parallel plate capacitance area between two fingers in metal layer i
A_{vi}	virtual parallel plate capacitance area between opposite vias on two fingers in metal layer i
A_{ij}	virtual parallel plate capacitance area between conducting metal layer i and metal layer j (i = 0 represents substrate or poly)
C_i	lateral flux capacitance contribution from metal layer i on one side of one vertical mesh
C_{ij}	capacitance between metal layer i and metal layer j from one vertical mesh
C_{main}	main capacitance
C_{mesh}	capacitance of one vertical mesh
C_{par}	parasitic bottom plate capacitance of one mesh
C_{vi}	capacitance between opposite vias on two fingers in metal layer i capacitance between via i and metal layer j from one vertical mesh
ε_0	permittivity of vacuum (= 8.854e-12AsV^{-1}m^{-1})
ε_{rij}	relative permittivity of the dielectric between metal layer i and metal layer j
k	number of topmost metal layer in the capacitor
L_{ol}	length where two vertical meshes overlap
L_{eff}	effective mesh length taking end contributions into account as well ($L_{eff} = L_{ol} + W + \pi S/2$)
n	number of individual meshes connected to one port of the capacitor.
S	vertical mesh spacing
S_{vi}	spacing between vias in layer i
t_i	thickness of metal layer i
t_{ij}	thickness of dielectric between metal i and metal j
W	width of the metal fingers
W_{vi}	width of vias in layer i
W_{eni}	metal enclosure of via i

$$C_{ParallelPlate} = \varepsilon_{relative} \cdot \varepsilon_0 \cdot \frac{A_{Plate}}{distance} \quad (3)$$

Naturally estimating these virtual parallel plate capacitance areas is not trivial and usually it is necessary to carry out time consuming 3D electromagnetic simulations but in this case it is possible to make some simplifying assumptions that allow a very rapid estimation of the virtual parallel plate capacitance area.

Figure 3 shows a side view of a vertical mesh. An estimate of the virtual parallel plate capacitance area of C_3 (i.e. A_3) is indicated by the upper rectangle. The width of the rectangle is L_{eff} i.e. the length of the vertical mesh. The height is more involved because this is the parameter that takes the fringing effects into account. The rectangle height is some fraction of t_{23} representing the lower fringing contribution plus the thickness of metal3 (t_3) plus some fraction of t_{34} representing the upper fringing contribution.

Now guessing the fraction of t_{23} (and t_{34}) is the challenging part. The lower bound must be zero because this corresponds to no fringing capacitance. The upper bound must be 1/2 because this corresponds to a solid plate i.e. if the holes were filled with metal.

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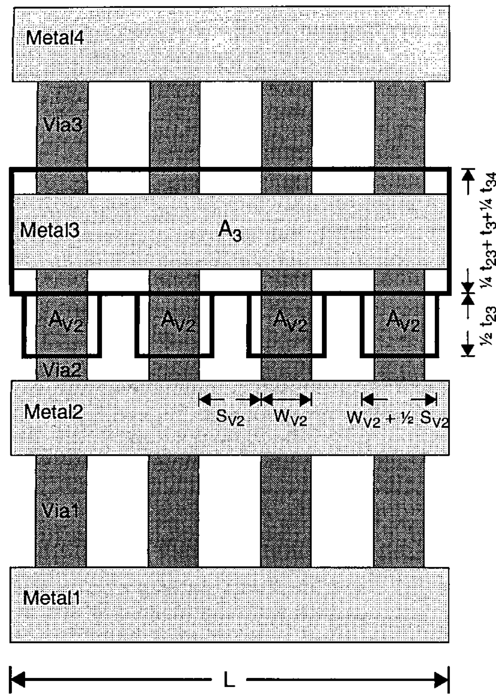

Figure 3. Side view of a vertical mesh. Estimation of individual lateral flux capacitance contributions. Parallel plate capacitance areas are increased to take the fringing field capacitance contributions into account (A_3 and A_{V2}).

The lower limit is reached when S/t_{23} approaches zero because the fringing contribution becomes negligible compared to t_{23} and the upper bound is reached when S/t_{23} approaches infinity. For reasonable choices of mesh spacing S/t_{23} (and S/t_{34}) are in the order of one and therefore a justified guess is that the fraction is halfway between the two bounds i.e. 1/4 of t_{23} and likewise 1/4 of t_{34}. This is the simplifying assumption that allows hand calculation of the vertical mesh capacitance. Therefore the lateral capacitance contribution of metal layer i including the fringing capacitance contributions can be expressed as (4).

$$C_i = \varepsilon_{ri}\varepsilon_0\frac{A_i}{S} = \varepsilon_{ri}\varepsilon_0\frac{L_{eff}\left(\frac{t_{(i-1)i}}{4} + t_i + \frac{t_{i(i+1)}}{4}\right)}{S} \quad (4)$$

The lateral capacitance contributions from the vias as for instance C_{V2} also need to be characterized. In the same manner as before these capacitance contributions are calculated using virtual parallel plate capacitance areas. Figure 3 shows the virtual parallel plate capacitance area of C_{V2} i.e. A_{V2} as a number of small rectangles. Each rectangle corresponds to the contribution from one via.

The height of the rectangle is limited to $t_{23} - 2 \times (t_{23}/4) = ½\, t_{23}$ because the same area can not be counted twice. The width of each rectangle is estimated in the same way as before i.e. halfway between the upper and the lower bound. The lower bound is W_{V2} and the upper bound is $W_{V2} + 2 \times (S_{V2}/2)$ and thus the width is estimated to be $W_{V2} + S_{V2}/2$. In order to find the total amount of capacitance from one layer of vias this rectangle area should be multiplied by the number of vias. The number of vias is approximately $L_{eff}/(W_{V2} + S_{V2})$ and therefore the capacitance contribution from one side of a mesh from vias in layer i (C_{Vi}) can be expressed as (5).

$$C_{vi} = \varepsilon_{rvi}\varepsilon_0\frac{A_{vi}}{S + 2W_{eni}} = \varepsilon_{rvi}\varepsilon_0\frac{L_{eff}\frac{W_{vi} + S_{vi}/2}{W_{vi} + S_{vi}}\frac{t_{i(i+1)}}{2}}{S + 2W_{eni}} \quad (5)$$

The remaining capacitance contributions are the vertical capacitance contributions i.e. the top and the bottom capacitances. These contributions are also estimated using a virtual parallel plate capacitance area. Both virtual capacitance areas are estimated by the mesh overlap length plus half t_{ij} (fringing) multiplied by the mesh width W plus half the mesh spacing (fringing). This leads to the expression for the top and bottom capacitances (6).

$$C_{ij} = \varepsilon_{rij}\varepsilon_0\frac{(L_{ol} + t_{ij}/2)\cdot(W + S/2)}{t_{ij}} \quad (6)$$

Now we have expressions for all the individual capacitance contributions of one vertical mesh capacitor. Thus all we need to do to get the total capacitance C_{main} is to add the contributions and multiply by the number of vertical meshes (n) i.e. (7). Note that the bottom plate capacitance C_{01} is not included because it is considered a parasitic capacitance. If the other terminal is connected to ground this capacitance should be added to C_{main}.

$$C_{main} = n\cdot\left(\sum_{i=1}^{k} 2C_i + \sum_{i=1}^{k-1} 2C_{vi} + C_{k(k+1)}\right) \quad (7)$$

Process Variation

Perhaps the most important feature of the vertical mesh capacitor is that it uses a combination of many capacitance contributions that are formed in different processing steps. This means that the process variations of these capacitances are *not correlated* and therefore the combined mesh capacitor experiences significant averaging. For instance if a vertical mesh capacitor is made out of four equal sized contributions with ±10% variation each then the combined capacitor has $\pm 10\%/\sqrt{4} = \pm 5\%$ variation and if the capacitor is made of nine equal sized contributions then the variation is $\pm 10\%/\sqrt{9} = \pm 3.3\%$. The individual capacitances depend on three main parameters; layer thickness, spacing and relative dielectric constant. If the capacitor is designed with sufficiently large mesh spacing then the capacitance variation is dominated by the layer thickness variation which is typically in the order of ±10%. Therefore well designed vertical mesh capacitors have as little as ±3-5% process variation.

Measurement Results

A vertical mesh capacitor was designed for an LC resonator with switched capacitor tuning (figure 6) in a standard 0.25 micron CMOS process with 6 metal layers. Also a separate test structure with 42 capacitor meshes was fabricated to be

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able to characterize the capacitor through probe measurements. Metal 2, 3 and 4 were used for the meshes, metal 5 was used as top shield and metal 1 was used as a (relatively) low loss ground plane. The mesh spacing was chosen to be 0.5 micron and the meshes were made 51 micron long to give the desired unit capacitance value. The measured capacitance (figure 4) show excellent agreement with the calculated values. The model overestimates the capacitance by only 2.4% which must be considered excellent and the average capacitances of the three measured capacitors varied by as little as ±0.2%. Naturally this is a very small data set but still the result is satisfying because it hints that the process variation is better than 3-5% as expected.

Although not optimized for maximum Q the measurements also show very good Q-values (figure 5). Measuring high-Q devices is not trivial because the S-parameters are located at the edge of the Smith chart. Therefore for this device the Q-values are not very accurate below 3-4 GHz and the loss is most likely dominated by the test fixture and especially by the probe contact resistance so the actual device Q-value is probably better than what the measurements indicate.

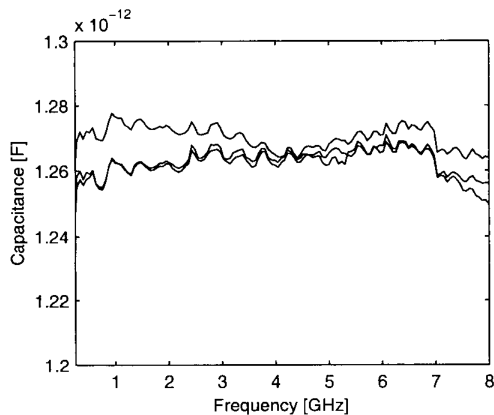

Figure 4. Capacitance of 42 meshes (M2, M3 and M4) each 51 micron long. Measurements from three dice.

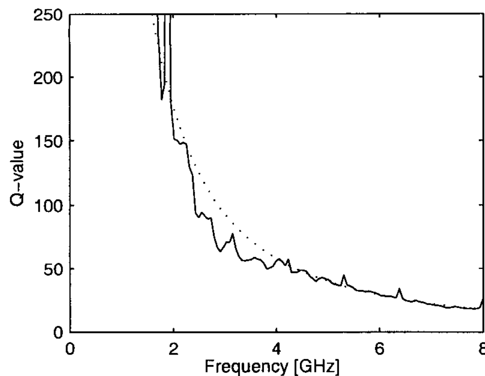

Figure 5. Quality factor of the fabricated capacitor. Measured Q = -Im(Z) / Re(Z) (solid), measured with second order polynomial fit of Re(Z) from 4 to 8 GHz (dotted).

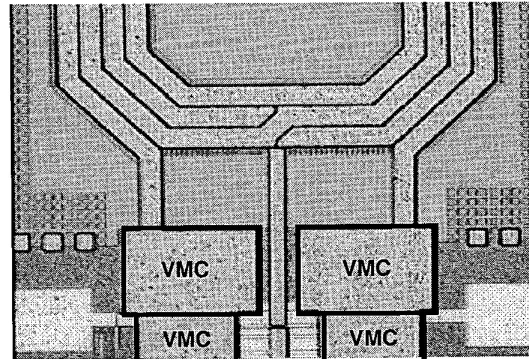

Figure 6. Chip photo of Vertical Mesh Capacitors used in an LC resonator with programmable centre frequency.

Table 1: Summary of Capacitor Characteristics

Parameter	Calculated	Measured
Capacitance	1.30 pF	1.27 pF
Bottom plate capacitance	74fF ~ 6%	---
Capacitance per Area (M2-M4)	0.27 fF/μm^2	0.26 fF/μm^2
Capacitance per Mesh (51 μm)	30.6 fF	29.9 fF
Q-value at 4.0 GHz	> 100	> 57
Chip-to-Chip Capacitance Variation (average 250MHz - 8.0GHz)	<± 3-5%	± 0.2%

Conclusion

This paper explains how good RF capacitors can be made in standard CMOS processes. By stacking a number of interleaved metal fingers and connecting them with vias it is possible to form vertical metal meshes that provide good capacitance density and high Q-value. Each unit capacitor is completely shielded yet it is only two microns wide which makes it ideal for binary weighted switched capacitor banks. The capacitors show low process variation due to averaging of capacitance tolerances adhering from process steps that are not correlated. Also the measured capacitance is almost constant up to 8GHz so the series inductance is negligible over that frequency span. Finally the paper presents a simple yet accurate method for calculating the capacitance of these structures. By using this method it was possible to predict the measured capacitance with an error of only 2.4%.

Acknowledgements

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