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A CALIBRATION METHOD FOR PLLS BASED ON TRANSIENT RESPONSE*

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ABSTRACT

A novel method to calibrate the frequency response of a Phase-Locked Loop is presented. The method requires just an additional digital counter and an auxiliary Phase-Frequency Detector (PFD) to measure the natural frequency of the PLL. The measured value can be used to tune the PLL response to the desired value. The method is demonstrated mathematically on a typical PLL topology and it is extended to $\Sigma\Delta$ fractional-N PLLs. A set of simulations performed with two different simulators is used to verify the applicability of the method.

1. INTRODUCTION

Phase-Locked Loop (PLL) frequency synthesizers are building blocks of all communication systems. An accurate PLL response is required in many situations, especially when $\Sigma\Delta$ PLLs for direct modulation [1] are used. In these types of PLLs, the data fed into the $\Sigma\Delta$ modulator is often undergoing a pre-filtering process in order to cancel the low-pass PLL transfer function and thereby to extend the modulation bandwidth [2]. The pre-distortion filter presents a transfer function equal to the inverse of the PLL transfer function and it is usually implemented digitally. Consequently, a tight matching between the pre-distortion filter and the analogue PLL transfer function is necessary to avoid distortion of the transmitted data.

Especially for on-chip Voltage Controlled Oscillators (VCO), the gain K_{VCO} is typically the parameter with the poorest accuracy among the PLL analog components. However to establish an accurate PLL transfer function only the product $K_{VCO} \times I_{CP}/C$ needs to be accurate [3]. The PLL can then be calibrated by adjusting the Charge-Pump current; the problem is how to measure the accuracy of the PLL transfer function.

A continuous calibration technique is presented in [4]. The transmitted data is digitally compared with the input data and the Charge-Pump current is then adjusted to compensate the detected error. This method offers the possibility of continuous calibration at the expense of increased circuit complexity; since the error detection is based on the cross-correlation between input and transmitted data, this approach will not work on unmodulated synthesizers. An alternative approach is found in [5], where a method based on the detection of pulse skipping is described. The presence of one or several pulse skips can be used as an indication of the bandwidth. This method requires an input frequency step large enough to push the PLL into its non-linear operating region and only offers a rough estimation of the actual PLL bandwidth.

* This work was carried out as a part of an internship at the QCT department of Qualcomm CDMA Technologies.

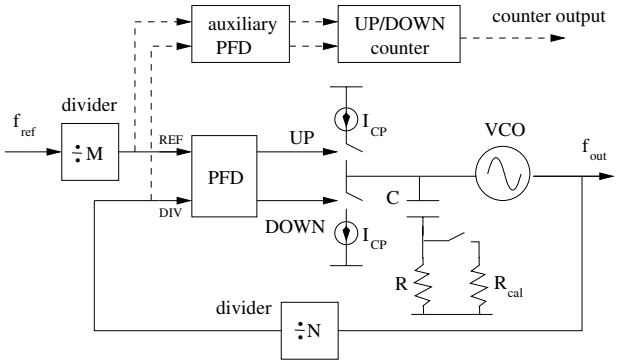

Fig. 1. Classical PLL structure.

In this paper we present a simple and novel approach that makes it possible to determine the characteristics of the PLL transfer function by simply adding a digital counter and an auxiliary Phase Frequency Detector (PFD).

The paper is organized as follows: in section 2 we present the basic idea behind the method and in section 3 we discuss its mathematical formulation. The extension of the method to $\Sigma\Delta$ PLLs is presented in section 4. Finally, in section 5, the results from different simulations are compared with the theory developed.

2. MEASURING SCHEME

A calibration cycle is required by this method. Consider the typical PLL topology in fig. 1: to start the calibration, the switch to R_{cal} is closed and the calibration resistor R_{cal} is connected to the resistor R. By reducing the total filter resistance, the loop transfer function presents under-damped characteristics. Note that, if the loop transfer function is already designed with under-damped characteristics, then the calibration switch is not necessary. By changing the ratio M of the f_{ref} divider or of the ratio N of the f_{out} divider, a frequency step can be applied to the PLL. The natural frequency of the induced transient response can be indirectly measured by counting the UP/DOWN pulses produced by the PFD. If the counter counts 1 up for each UP pulse and counts 1 down for each DOWN pulse, then the maximum counter value is a measure of the natural frequency of the PLL transfer function. This can be seen in fig. 2, where the expected behavior of the phase error together with the counter value trajectory are presented. The Charge-Pump current can be adjusted so that the PLL natural frequency is the desired one.

For the calibration method to work properly, the leakage current in the Charge-Pump should be kept small and the trickle cur-

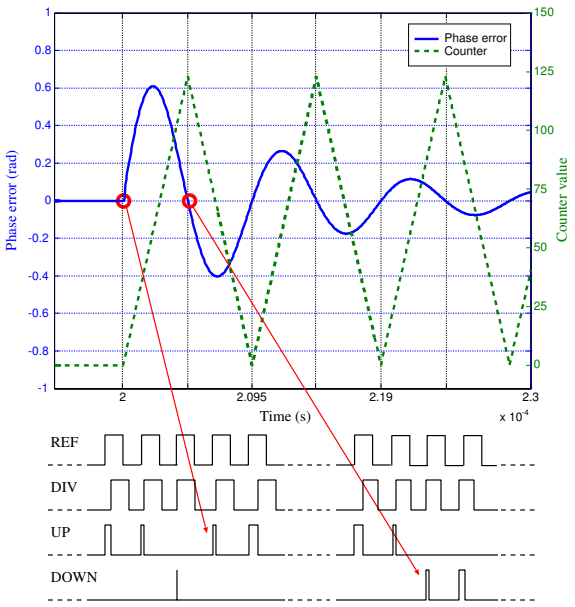

Fig. 2. Phase error with corresponding UP/DOWN pulses.

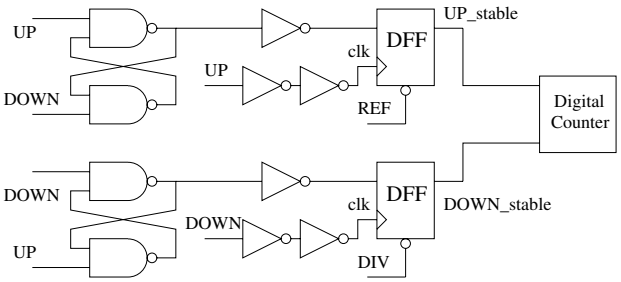

Fig. 3. Auxiliary circuit and digital counter.

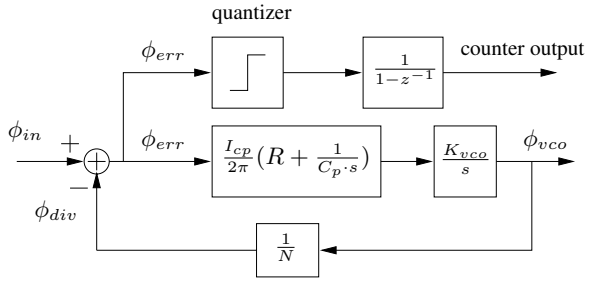

Fig. 4. Classical PLL linear model.

rent (if any) should be turned off. Any leakage or trickle currents will induce a static phase error at the PFD input. This, in turn, means an increased number of pulses in one direction (e.g. UP pulses). Consequently, the counter value is no longer an accurate representation of the natural frequency.

The auxiliary PFD in fig. 1 is required to generate stable UP/DOWN pulses for the digital counter. A possible circuit implementation that works together with a typical PFD is shown in fig. 3. The two set-reset flip-flops (SR-FF) are used to establish which one between the UP/DOWN pulses occurs first. This is necessary because the UP and DOWN pulses are simultaneously high for a length equal to the delay in the PFD reset path [5]. If the UP pulse rises before the DOWN pulse, then a logical 'ONE' appears at the input of the top edge-triggered resettable D flip-flop (fig. 3) and a logical 'ZERO' appears at the input of the bottom D flip-flop. The UP pulse delayed through a couple of inverters clocks the flip-flop and the negative transition of the REF clock resets the flip-flop. Hence the flip-flop produces an *UP_stable* pulse whose length is approximately equal to the REF semiperiod.

The opposite happens if the DOWN pulse occurs before the UP pulse. If the PFD produces aligned UP and DOWN pulses (this is the case if the input phase error is smaller than the dead-zone of the PFD) then the *UP_stable* and the *DOWN_stable* signals are high at the same time.

3. MATHEMATICAL DERIVATION

The mathematical formulation will be based on the PLL topology of fig. 1; however, the applicability of the method extends to other topologies, as it will be demonstrated in the next section. We start by deriving the PLL loop transfer function with the aid of the linear model of fig. 4:

$$H_{loop}(s) = \frac{I_{cp}(R \cdot C_p s + 1)K_{VCO}}{2\pi C_p s^2 N} \qquad (1)$$

The transfer function from phase input to phase error is given by:

$$\frac{\Phi_{err}(s)}{\Phi_{in}(s)} = \frac{1}{1 + H_{loop}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (2)$$

where $\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi C_p N_d}}$ and $\zeta = \frac{R}{2}\sqrt{\frac{I_{CP}C_p K_{VCO}}{2\pi N}}$ and ω_n and ζ represent, respectively, the natural frequency and the damping factor of the PLL. A unit input frequency step corresponds to an input phase ramp, with Laplace transform given by $\Phi_{in}(s) = \frac{1}{s^2}$. The Laplace transform of the phase error is then given by:

$$\Phi_{err}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{1}{s^2} \qquad (3)$$

The behavior in the time domain of equation 3 is the impulse response of a second order system:

$$\phi_{err}(t) = \frac{1}{\omega_n\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_0 t) \qquad (4)$$

where $\omega_0 = \omega_n\sqrt{(1-\zeta^2)}$. As long as the phase error function $\phi_{err}(t)$ is positive, the PFD generates UP pulses. If the error becomes negative, DOWN pulses are generated. Assuming a positive frequency step, an initial sequence of UP pulses is produced by the PFD and the counter value increases monotonically. When the phase error crosses the zero-error phase, occurring at $t_{cross} = \frac{\pi}{\omega_0}$ according to equation 4, DOWN pulses start to appear decreasing the counter value. Hence at the crossing time the counter reaches its maximum value, V_{max}; the crossing point can also be expressed as $t_{cross} = V_{max} \cdot T_{ref}$, where T_{ref} is the period of the REF clock (fig. 1). For stability reason [3], the PLL dynamics is always much slower than the REF signal: the error introduced by quantizing t_{cross} is then insignificant. ω_0 can then be approximated as:

$$\omega_0 = \frac{\pi}{V_{max} \cdot T_{ref}} \qquad (5)$$

4. EXTENSION TO ΣΔ PLL TOPOLOGIES

The applicability of the measuring technique will be now demonstrated for ΣΔ fractional-N PLLs. These PLLs use high-order multi-bit ΣΔ modulators to dither the divider modulus; direct modulation is achieved by feeding the data into the modulator. Thus, to measure ω_o, the frequency step is, in this case, applied to the ΣΔ modulator input.

The linear model of a ΣΔ fractional-N PLL is shown in fig. 5. A complete derivation of the linear model can be found in [6]. The Loop Filter is typically a high-order structure to attenuate the high-frequency quantization noise. In the example analyzed in this section, the Loop Filter transfer function presents 4 poles (including the Charge-Pump integration) and 1 zero. The mathematics involved in this case is lengthier, but the final transfer function can be reduced to an equivalent 2^{nd} order equation.

We start by finding the transfer function from the ΣΔ modulator input to phase error $\Phi_{err}(s)$. With the aid of fig. 5, considering that the effect of the ΣΔ modulator Signal Transfer Function (STF) is just adding a delay to the input data, the transfer function is given by:

$$\frac{\Phi_{err}(s)}{\Sigma\Delta_{in}(s)} = \frac{2\pi}{N+\mu_b} \cdot \frac{e^{-sT_{ref}}}{1-e^{-sT_{ref}}} \frac{1}{1+H_{loop}(s)} \qquad (6)$$

where $N+\mu_b$ is the instantaneous divider ratio.

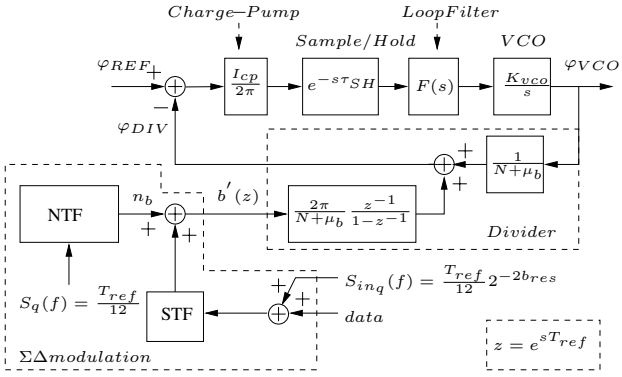

Fig. 5. ΣΔ fractional-N PLL linear model.

Indicating with ω_3, ω_4, ω_5 and z_1 the high order poles and, respectively, the zero of the Loop Filter, and by setting:

$$T_{eq}^2 = \frac{1}{\omega_4^2} + \frac{1}{\omega_4 \cdot \omega_3} + \frac{1}{\omega_4 \cdot \omega_5} + \frac{1}{\omega_3^2} + \frac{1}{\omega_3 \cdot \omega_5} + \frac{1}{\omega_5^2} - \frac{1}{\omega_4 \cdot z_1} - \frac{1}{\omega_3 \cdot z_1} - \frac{1}{\omega_5 \cdot z_1}$$

it is possible to define an equivalent natural frequency ω_{n1} and an equivalent damping factor ζ_1:

$$\omega_{n1} := \sqrt{\frac{\omega_n^2}{\left[1+(\omega_n T_{eq})^2\right]}} \qquad (7)$$

$$\zeta_1 = \frac{1}{2}\omega_{n1}\left(\frac{1}{z_1} - \frac{1}{\omega_3} - \frac{1}{\omega_4} - \frac{1}{\omega_5}\right) \qquad (8)$$

After proper manipulations, eq. 6 can be reduced to the following approximated expression:

$$\frac{\Phi_{err}(s)}{\Sigma\Delta_{in}(s)} = G \cdot \frac{s}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} \qquad (9)$$

with the gain factor given by $G = \left(\frac{\omega_{n1}}{\omega_n}\right)^2 \frac{2\pi}{N+\mu_b}\frac{1}{T_{ref}}$. The final expression for the phase error, obtained by applying a step function to the ΣΔ modulator, is given by:

$$\Phi_{err}(s) = \frac{G}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} \qquad (10)$$

and it corresponds directly to equation 3. The smaller is the loop damping factor ζ, the more accurate is the approximation in equation 10. Thus, the natural frequency can be calculated as described in section 3.

However the use of ΣΔ fractional-N PLLs introduces a new requirement for the correct applicability of the method. The input step to the modulator needs to be large enough to overcome the random effects of the modulator itself. If the input step is too small, then the UP sequence is no longer monotonic and the extracted value of ω_0 is no longer accurate. On the other hand, the equations derived so far are based on the assumption that the PLL is working in its linear region. If a large input step is applied, the PLL may be pushed out of its linear region. In this case, the previous equations are no longer valid, but, as mentioned in [7], the calibration method will still work, since the final counter value can be extracted from simulations. Alternatively, the counter can be reset whenever a pulse skip is detected: in this way the final value in the counter represents the number of UP (or DOWN) pulses occurred during the linear part of the step response. In other words, the counter starts to operate properly when the PLL leaves the frequency acquisition mode and enters the phase acquisition mode.

5. SIMULATION RESULTS

The main parameters of the simulated PLL are resumed in table 1. The ΣΔ modulator is a MASH 4^{th} order and the parameters of the Loop Filter are presented in table 2. Based on the simulation results, the ΣΔ fractional-N PLL topology can be simulated with a liner simulator such as Simulink; however the system behavior has been also investigated through a Verilog implementation. The use of Verilog provides the possibility to simulate a model more close to a real PLL implementation, capable of capturing the nonlinear behavior of the system [6].

As already discussed in the introduction, the VCO gain K_{VCO} is the parameter with the poorest accuracy; the ΣΔ PLL was simulated with the nominal K_{VCO} value and with a gain variation of $\pm$ 30% with respect to the nominal value. In fig. 6 the counter behavior for the 3 different K_{VCO} values is presented. It is apparent that the three curves reach different peaks according to the value of K_{VCO}; as the time proceeds the effects of the ΣΔ modulator start to appear.

By substituting the values of the parameters in the equations presented in section 3, the theoretical maximum counter values for the three different VCO gains, are, respectively, 150, 123, and 106. The values extracted from the Verilog simulation of fig. 6 are 148, 122, and 105; these values closely match the predicted ones. The counter behavior for different input frequency steps is presented in fig. 7. As the step is increased, overcoming the ΣΔ modulator noise, the measured values match very well the predicted ones. In the same figure the results for both simulators, Verilog and Simulink, are presented. Notice that the Simulink curves are

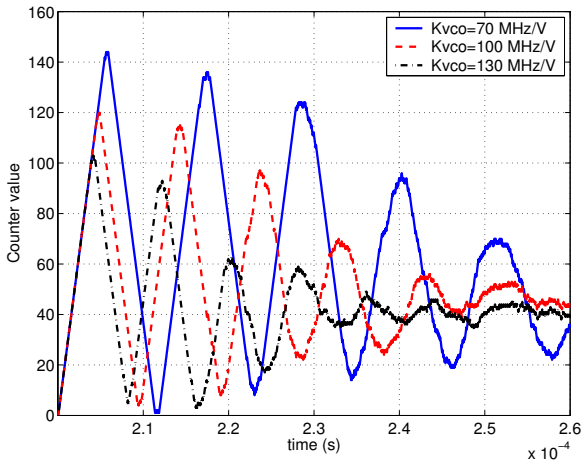

Fig. 6. Counter behavior vs. time

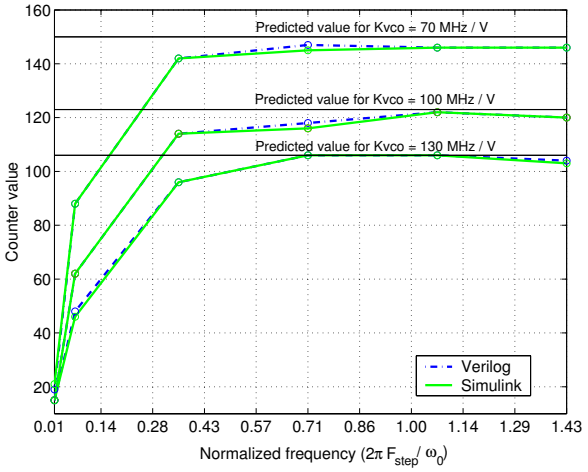

Fig. 7. Counter maximum vs. frequency steps.

very close to the curves obtained with Verilog, which confirms that the linear simulator describes accurately the transient behavior of the $\Sigma\Delta$ PLL even for fairly large input frequency steps.

As previously discussed, the presence of a leakage current will result in an average phase error different from zero. If the leakage current is too large, even in lock condition of the PLL, the PFD will only produce UP pulses (for a negative leakage current) or DOWN pulses (for a positive leakage current). The simulations show that the calibration method is very robust to leakage currents: a $\pm 1\%$ leakage current will produce less than $\pm 6\%$ deviation from the nominal ω_o. By observing the difference between the maximum number of UP (DOWN) pulses and the maximum number of following DOWN (UP) pulses, it is actually possible to obtain the polarity and a magnitude estimation of the static phase offset. In fact, with zero static phase offset the length of the two sequence would be the same; if a positive phase offset is present, the phase error curve for a positive frequency step is shifted up with respect to the zero offset curve: in this case the monotonic sequence of UP pulses will be longer than the following sequence of DOWN pulses.

f_{out}	N	μ_b	I_{CP}	K_{VCO}
$3.62\ MHz$	139	0.375	$10\ \mu A$	$100 MHz/V$

Table 1. Design parameters.

C_{CP}	z_1	ω_3	ω_4	ω_5
$18.158\ pF$	$167 kHz$	$500 KHz$	$1 MHz$	$5 MHz$

Table 2. Loop parameters.

6. CONCLUSIONS

A new method to calibrate the PLL transfer-function has been presented. The implementation does not require any additional analogue component. The only extra circuitry necessary is an auxiliary PFD and a digital counter. This new approach does not offer continuous calibration and it requires a calibration cycle, but it is very simple and virtually no extra silicon area and no extra power consumption is required. Moreover, this technique works for both linear and non-linear PLL frequency step responses; also, it can be used to estimate the static phase offset. The mathematical formulation of the method has been verified with simulations based on a $\Sigma\Delta$ fractional-N PLL topology, run both on Verilog and Simulink. Results from both simulations closely match the theoretical values.

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