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Design of a 10-bit 100 MSamples/s BiCMOS D/A Converter

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ABSTRACT

A 10-bit 100MSamples/s current-steering D/A converter (DAC) has been designed and processed in a 0.8μm BiCMOS process. The DAC is intended for applications using direct digital synthesis, and focus has been set on achieving a high spurious free dynamic range (SFDR[1]). The main part of the DAC is a matrix of current cells. To reduce skew between the steering signals to the current cells, an emitter-coupled logic (ECL) flip-flop, clocked by a global ECL clock, is included in each current cell. A bipolar differential pair, steered by the differential output of the ECL flip-flop, is used in each current cell to steer the current. At a generated frequency of $f_g \approx 0.3 \cdot f_s$ (f_s = 100 *MSamples/s*), the simulated SFDR is larger than 60dB. The DAC operates at 5V, and has a power consumption of approximately 650*mW*. The area of the chip-core is 2.2mm×2.2mm. Furthermore a measure to estimate the SFDR for the DAC based on short term simulations is presented. This measure seems to correspond very well with SFDR for long term simulations.

I. INTRODUCTION

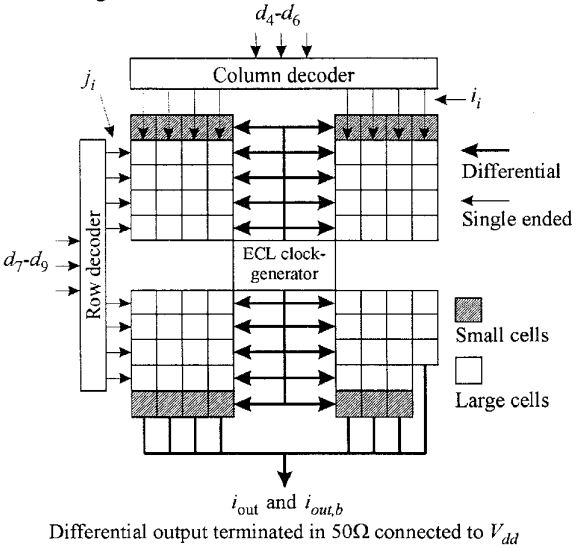
High-speed and high resolution DACs are used in various applications such as direct digital synthesis (DDS), arbitrary waveform generation (AFG), new TV/Video systems and communications local oscillators. For these applications the dynamic performance of the DAC is very critical. For the DAC described in this paper, focus has been set on achieving a high spurious free dynamic range (SFDR) at high generated frequencies, f_g, compared to the conversion rate, f_s (100*MSamples/s*), i.e., $f_g \approx 0.3 \cdot f_s$. Any static or dynamic nonlinearity will generate spurious frequencies at the DAC output. Static nonlinearities can be reduced significantly by careful layout and by using different kinds of switching schemes for the current cells [5], [6]. The main dynamic nonlinearities are nonequal and code dependent rise and fall times, delay between rise and fall transients, and nonlinear clock and data feedthrough. For a typical current steering DAC one of the main challenges is to generate steering signals for the current cells with very little skew between these [1], [3], [5]. A solution is to use clocked current cells. One then has to generate a global clock for the current cells that has an acceptable low clock skew over the current cell matrix. This is an advantage because clock-skew can more easily be controlled than the delays of different steering signals.

The DAC presented in this paper is constructed using this scheme. Each current cell contains an ECL flip-flop. The skew between the steering signals for the different current cells are then controlled by a global clock signal.

The DAC architecture is described in section II, and the current cells are described in section III. Section IV.A shows the simulation results of the DAC with special emphasis on SFDR. A measure, especially useful during circuit simulations of the dynamic performance of high-speed DACs, is proposed in section IV.B.

II. DAC ARCHITECTURE

The DAC presented in this paper is based on the well-known current steering principle [1]-[7]. The DAC architecture is shown in Fig. 1.



Differential output terminated in 50Ω connected to V_{dd}

Fig. 1. DAC Architecture

[1] SFDR is measured from the generated frequency to the highest harmonic or non-harmonic spur within the frequency band 0-f_s/2.

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The current cells are arranged in a matrix. This matrix consists of 63 large current cells that determine the 6 most significant bits (6 MSB), and 15 smaller cells that determine the 4 least significant bits (4 LSB). One large current cell sinks a current 16 times the current in a small current cell. The DAC operates as follows: The digital input word, d_9(MSB)-d_0(LSB), is stored in an input register, and decoded into row and column signals (for the 6 MSB), and then latched before being fed to the current cells. In Fig. 1 the registers and latches are contained in the column and row decoders. The decoding ensures that a minimum of current cells are turned on or off; this reduces dynamic nonlinearities. The hierarchical switching scheme [6] is used for the large current cells to reduce nonlinearities. This switching scheme reduces both symmetrical and graded errors. For the small current cells, a simple "chessboard scheme" is used controlled by the digital signals d_3-d_0.

In each current cell (see Fig. 2) the CMOS steering signals, i, i+1 and j, are decoded by CMOS logic. The decoded signal is then converted into ECL levels, v_{in} and $v_{in,b}$, and latched by an ECL flip-flop clocked by the global differential ECL clock. Thus, one reduces the problem with skew between the steering signals over the matrix. The differential current outputs of all current cells are connected to the DAC output pins i_{out} and $i_{out,b}$ as shown in Fig.1. These are, externally, each connected to a 50Ω resistor that again is connected to the positive power supply ($5V$). The maximum output current from the DAC is $20mA$. The ECL clock generator is placed in the middle of the current cell matrix to minimise clock skew. This also causes the clock skew to be a symmetrical error. Therefore it will, to some extent, be reduced by the hierarchical switching scheme.

The DAC consumes approximately 650mW. The temperature operating range for the DAC is from -40°C to 80°C.

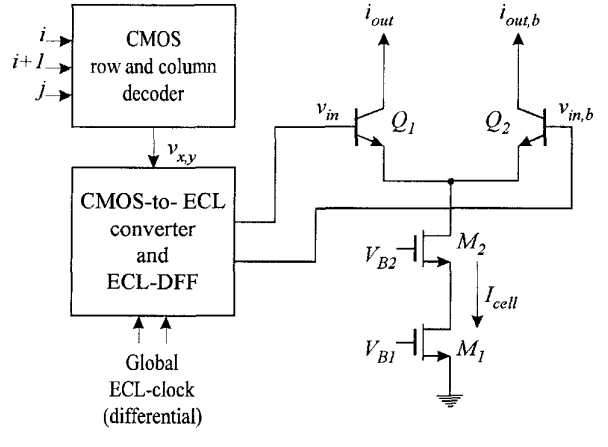

Fig. 2. The large current cell

III. Current Cells

A schematic of the large current cells is shown in Fig. 2 [2]. A differential pair with bipolar transistors, Q_1 and Q_2, is used to steer the current. The cascode current sink consists of two NMOS transistors M_1 and M_2. The current cell includes a CMOS input section which decodes the row and column signals. The decoded signal is converted into a differential ECL signal that is latched before fed to the differential pair, Q_1 and Q_2.

The use of a bipolar differential pair offers several advantages compared to the MOS counterpart. As the DAC should operate at a very high conversion rate, it is obvious to use fast bipolar transistors to toggle the current I_{cell} between the two outputs. Furthermore, the required voltage swing at the input, v_{in}-$v_{in,b}$, is much lower compared to the input swing of a MOS differential pair in a practical design. The differential input voltage that guaranties that the total erroneous output current from all N_{cells} current cells is less than 1/2 LSB of the total current, is given by (1). In (1) the collector currents I_{C1} and I_{C2} are given by the well-known exponential equation for the bipolar transistor. V_T is the thermal voltage which equals $26mV$ at room temperature.

$$\frac{I_{C1}}{I_{C2}} > 2^{N+1} N_{cells} \Rightarrow \Delta v_{in} = v_{in} - v_{in,b} > V_T \ln(2^{N+1} N_{cells}) \qquad (1)$$

Using the number of bits N=10, N_{cells}=64 (63 large, plus 15 small which equals approximately 1 large) we find that $\Delta v_{be} > 12V_T = 312mV$. This small ECL voltage swing and the fast ECL flip-flop output signals potentially give low spurious frequencies at the DAC output.

The delay of the output from the CMOS input section, $v_{x,y}$, in the current cell varies strongly depending on the input signals i, $i+1$ and j. The delay, rise and fall times for $v_{x,y}$ vary strongly dependent on the inputs i, i+1, j. If these CMOS signals, $v_{x,y}$, were used to steer the current cells directly the output signal contain higher level of spurious frequencies. The output from the CMOS part is therefore latched in the ECL section. The skew between the steering signals is therefore only dependent on the clock skew in the global ECL clock. The worst case clock skew over the matrix is designed to be less than 8ps.

The small current cells have the same architecture as the large ones but i is connected to V_{dd}, $i+1$ is connected to ground and the cells are only steered by j.

Because of α-mismatch, the bipolar differential pairs introduce current mismatch between the current cells. Assuming a $\Delta\beta/\beta$ better than 2% for transistors on the same chip, one obtain an $\Delta\alpha/\alpha$ of approximately 0.02%. This will be of minor importance compared to the other mismatch sources, such as ground potential variations and mismatch between NMOS current sinks.

IV. DAC Top-Level Simulations

A. Simulation of SFDR

The DAC has been simulated with Accusim from Mentor Graphics. To simulate the SFDR, an ideal sine wave was forced to an ideal A/D converter, to produce a pure 10-bit digital "sine" that was used as input to the DAC. Fig. 3 shows a segment of the resulting DAC output. Here, the generated frequency was approximately $30MHz$, and the conversion rate was $100MSamples/s$. During this simulation, a lumped resistance model of the ground network, and a lumped resistance and capacitance model of the ECL clock tree, were used. About 75 periods of the generated frequency were simulated. Fig. 4 shows the FFT of the differential DAC output signal shown in Fig. 3. (window function: Kaiser-Bessel). The simulation shows that SFDR > 60dB.

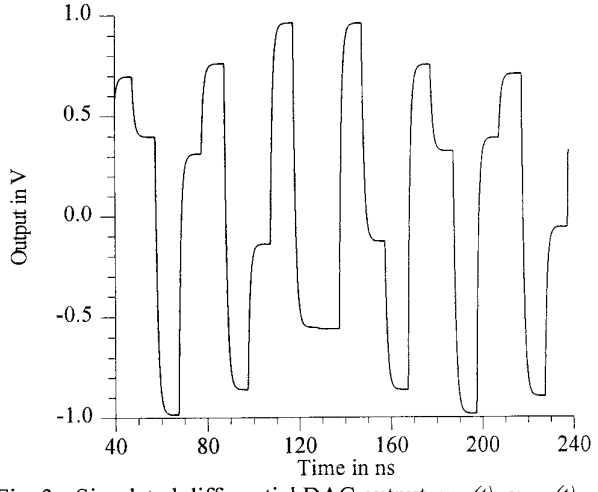

Fig. 3. Simulated differential DAC output, $v_{out}(t)$- $v_{out,b}(t)$, $f_g \approx 0.3 \cdot f_s$, f_s=100$MSamples/s$

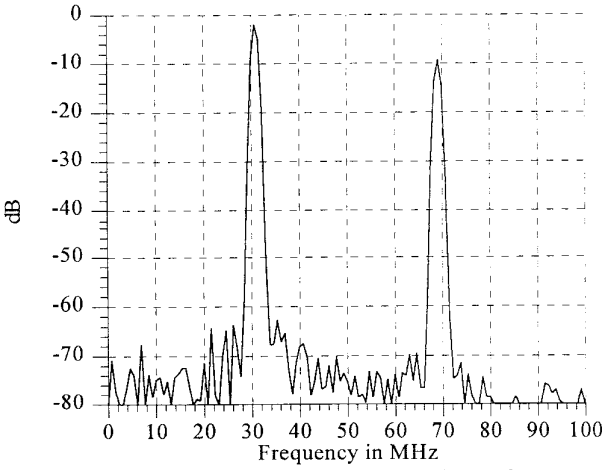

Fig. 4. FFT of the simulated DAC output, $f_g \approx 0.3 \cdot f_s$, f_s=100$MSamples/s$

B. A Measure of DAC Dynamic Performance

Top level simulations of the DAC to evaluate the SFDR are very time consuming as one has to simulate several periods of the generated frequency. E.g., the simulation of the final DAC that produced the result in Fig. 4 lasted for approximately 2 weeks on an HP 735 workstation.

A measure, mean error energy per conversion period E_{mean}, that estimates the SFDR of the final DAC, is therefore proposed. The measure is intended to be used for DACs with a switching scheme like the one used in this paper, i.e., a switching scheme that guaranties that a minimum of current cells are turned on or off each clock period. This measure is based on the dynamic behaviour of the entire DAC during a full scale output transient (input codes: 00..00 → 11..11). The simulation time is therefore reduced significantly.

For a DAC with differential output, $v_{out}(t)$ and $v_{out,b}(t)$, one first finds the error voltage for a full swing transient:

$$v_{error}(t) = v_{out}(t) + v_{out,b}(t) - v_{DC} \qquad (2)$$

v_{DC} is the mean value of $v_{out}(t) + v_{out,b}(t)$. $v_{error}(t)$ will include the effects of different rise and fall times, different delays for rise and fall transients, etc. Ideally $v_{error}(t)$ should equal zero. The error energy per conversion period, T_C, is then calculated:

$$E_{error} = \int_0^{T_C} |v_{error}(t)| dt \qquad [V \cdot s] \qquad (3)$$

To estimate E_{mean} for a given generated frequency, one has to multiply E_{error} with the average step size at the DAC output. For a DAC generating a sine wave, the relative average step size at the output, S_{mean}, compared to the full ouput swing of the DAC, is given by:

$$S_{mean} \approx 2\frac{f_g}{f_s} \qquad (4)$$

In (4) it is assumed that the digital "sine" utilises the full output swing of the DAC. One can now calculate E_{mean} at the DAC output:

$$E_{mean} \approx S_{mean} \cdot E_{error} \qquad [V \cdot s] \qquad (5)$$

This energy is compared to the energy of one LSB at the output of the DAC which is given by

$$E_{LSB} = V_{full-swing} T_C 2^{-N} \qquad [V \cdot s] \qquad (6)$$

Here $V_{full-swing}$ is the maximum differential voltage swing at the output of the DAC. As a conservative design target E_{mean} should be less than $E_{LSB}/2$ if the SFDR should be higher than $N \cdot 6dB$.

E_{error} was simulated to $17.8pVs$ (T_C = $10ns$). This means that $E_{mean} \approx 10.7pVs$ for a generated frequency of $0.3 \cdot f_s$. Comparing E_{mean} to $E_{LSB}/2$, which equals $10pVs$, one finds that this corresponds to SFDR ≈ $60dB$ that also was the result in section IV.A. The actual E_{mean} for the simulation shown in

Fig. 3 and Fig. 4 was 11.2pVs which corresponds very well with the estimated value of E_{mean}.

This measure offers the opportunity to compare the performance of different current cells in a DAC without performing long term top level simulations. The dynamic performance of a DAC is often given in terms of the glitch energy. Contrary to E_{mean}, the glitch energy is not based on a full scale transition. The full scale transition includes all nonideal dynamic effects. Therefore E_{mean} provides a better estimate of the dynamic performance than the conventional glitch energy which only contains the nonideal effects of one or more specific transients. Also some DAC architectures, such as the one presented here, inherently do not have the typical large glitch energy at the transition 011...11 to 100..00. Therefore E_{mean} is a more appropriate measure.

E_{mean} was also used to evaluate the dynamic behaviour of a single current cell. However, E_{mean} multiplied with the number of current cells gives a too optimistic estimate of the dynamic behaviour of the entire DAC. The measure still applies very well when comparing the dynamic behaviour of different current cells.

V. Layout Considerations

The DAC is processed in a 0.8μm double-metal double-poly BiCMOS process provided by Austria Mikro Systeme International GmbH (AMS). To minimise switching noise from the CMOS- and ECL-logic to couple to the output of the DAC, the power supplies for the CMOS- and ECL-logic and the current sinks are routed separately. The current I_{cell} from each large current cell introduce a voltage drop in the analogue ground. The analogue ground wires are therefore made wide. Also, several pads on each side of the current cell matrix are used to connect the analogue ground. Furthermore, all different parts of the circuitry are surrounded by guardrings and all major parts by double guardrings to minimise noise injected to the output through the substrate. A separate power pad has been used for the n-well parts of the guard rings. All bias lines, both to the ECL-logic and the current sinks in the current cells, have both local and global decoupling capacitors to minimise spikes on these. Horizontal and vertical shielding between the analogue routing and digital data lines (both CMOS and ECL) have been used to minimise coupling between these. Careful layout and design were necessary to obtain sufficient time margin for the data setup with respect to the ECL clock.

Clock skew, ground potential variation, etc., that generate spurious frequencies at the DAC output have been taken into account and were designed to introduce errors at the output, each less than ½ LSB. The switching scheme will tend to cancel must of them. The total error at the output is therefore not the sum of all errors. The size of the chip-core is 2.2mm × 2.2mm.

VI. Experimental Results

At the present time no measurement results are available as the chip is currently being processed.

VII. Conclusion

A 10-bit 100MSamples/s current steering DAC has been designed and fabricated in a 0.8μm BiCMOS process. The core of the DAC consists of a matrix of current cells. Each current cell includes CMOS decoding logic, a CMOS-to-ECL converter, an ECL flip-flop and a bipolar differential pair to steer the current. The ECL flip-flop is clocked by a global ECL differential clock. The differential output of the flip-flop directly steers the bipolar differential pair. The DAC shows a considerable potential for achieving a high SFDR. A measure to predict the SFDR from short term simulations is presented, and it seems to correspond very well with the actual simulated SFDR.

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