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INTEGRATING DATA CONVERTERS FOR PICOAMPERE CURRENTS FROM ELECTROCHEMICAL TRANSDUCERS

Madalina Breten   *Torsten Lehmann*   *Erik Bruun*

Department of Information Technology, Bldg. 344
Technical University of Denmark
DK–2800 Lyngby, Denmark

ABSTRACT

This paper describes a current mode A/D converter designed for a maximum input current range of 5nA and a resolution of the order of 1pA. The converter is designed for a potentiostat for amperometric chemical sensors and provides a constant polarization voltage for the measuring electrode. A prototype chip using the dual slope conversion method has been fabricated in a 0.7μm CMOS process. Experimental results from this converter are reported. Design problems and limitations of the converter are discussed and a new conversion technique providing a larger dynamic range and easy calibration is proposed.

1. INTRODUCTION

Electrochemical transducers are widely used in equipment such as blood analyzers. For example, an amperometric chemical sensor can be used to measure the concentration of oxygen in blood. Such a sensor provides a current proportional to the concentration if the sensor is biased with a constant voltage V_{pol} of about 0.6V. However, the maximum current of the sensor is very small, in the order of a nA, so for high resolution data converters (more than about 10 bits) the least significant bit corresponds to a current in the order of pA's or even less. Such converters can be designed using standard commercially available parts but it is desirable to implement the converter as a part of an integrated transducer front-end in order to reduce size, weight, power consumption and (possibly) production cost of the sensor system [1]. This implies that the converter should be designed in a standard CMOS process and that it should be designed to be insensitive to process variations and device tolerances such as offset voltages and non-linearities of components.

2. CIRCUIT DESCRIPTION

A block diagram of the prototype version of the potentiostatic A/D converter is shown in fig. 1. It is implemented as a dual slope converter. Since the signal to be converted is essentially a (very small) dc current, an integrating converter type is advantageous because it filters out high frequency noise components. Noise is critical in an application with such small currents. However, the conversion time can be selected to be fairly long, about 200ms, implying that stochastic noise above approximately 10Hz is attenuated by the converter integration.

The left part of the diagram shows the potentiostatic control made by the transconductance amplifier OTA_P and the pass transistor M_{n1}. The potentiostatic control system applies a polarization voltage V_{pol} between the working electrode WE and the reference electrode RE. For the test chip an external polarization voltage is used. The transconductance amplifier OTA_P and the transistor M_{n1} are connected as a voltage follower, so the input voltage to OTA_P will also appear at the working electrode. This electrode is coated with a chemically sensitive membrane (CSM) and behaves as a constant current source when V_{pol} is larger than about 0.4V. An optimum value of 0.6V results in a linear relationship between the current I_{mes} and the solution concentration. Since the input current to OTA_P is negligible, the current I_{mes} flows entirely through M_{n1}.

The current I_{mes} is charging the integration capacitor of the dual slope converter during a fixed integration time t_{up}. After this period the reference current I_{ref} is connected to the input of the dual slope converter and the capacitor is discharged. The switching between I_{mes} and I_{ref} is done by a bridge of four switches S_1, S_2, S_3 and S_4. The measurement current I_{mes} is switched between S_3 and S_4, keeping a constant current flow through M_{n1} and a constant voltage at the drain of M_{n1}. The reference current I_{ref} is switched between S_1 and S_2. The bridge is constructed using minimum size N-MOS transistors. The reference current is buffered by a regulated cascode OTA_N and M_{p1}.

The core of the converter is the integrator and the comparator, followed by the digital block. The integrator is implemented by the transconductance amplifier OTA, the capacitor C and a reset switch S_{reset}. The offset and the 1/f noise associated with the MOS input transistors of the integrator are compensated using an auxiliary input of reduced sensitivity in parallel with the main input of the integrator [2].

An important advantage of the dual slope ADC is its tolerance to variations and nonlinearities of most of the circuit parameters. In dual slope technique, the current to be measured I_{mes} causes the integrator to ramp-up for a fixed time $t_{up} = 2^N T_{clk}$, where T_{clk} is the period of the clock signal and N is the resolution in bits. Then a known current of opposite polarity I_{ref} is applied until the output crosses the threshold of the comparator (Fig. 2). To achieve maximum resolution, I_{ref} is selected close to the full-scale value of the current to be measured: $I_{ref} \cong I_{FS}$. The comparator and the integrator have the same reference voltage. Assuming the ideal case, when there is no voltage error across the capacitor at the beginning and the end of the conversion, that is $V_i = V_f = 0V$, the ramp-down time t_{down} is proportional to I_{mes}:

$$t_{down} = I_{mes} \frac{t_{up}}{I_{ref}} \qquad (1)$$

The ramp-down time is measured using a digital timing circuit. The conversion time is given by: $t_{conv} \leq 2^{N+1} T_{clk}$. A clock signal
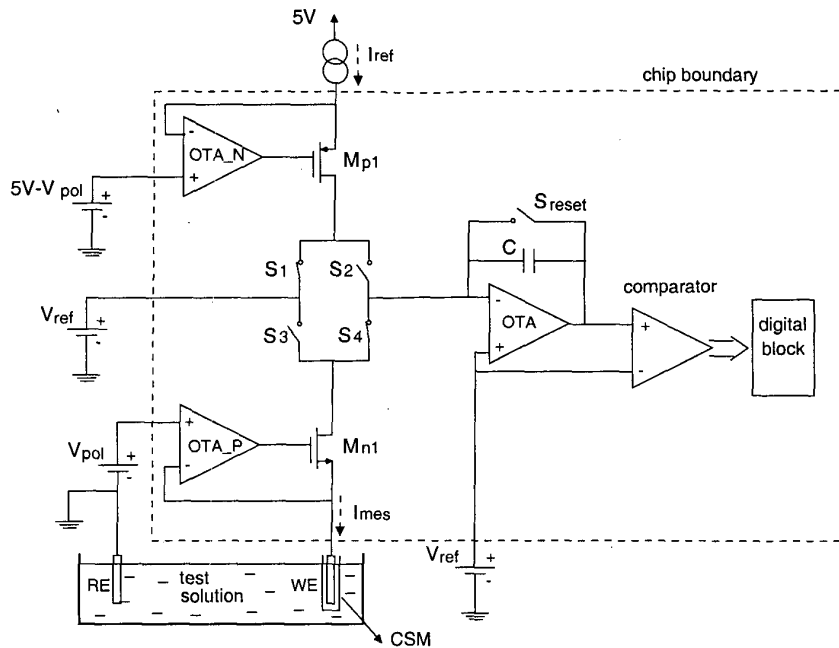
Figure 1. Block diagram of the prototype circuit.

of $T_{clk} = 1\mu s$ allows 16 bits resolution within a conversion time of $t_{conv} < 200$ms, and still leave some time for calibration. The capacitor C must have a rather big value in order to keep the integrator output voltage within the permissible output voltage range V_{range} of the OTA. C is limited by:

$$C \geq \frac{I_{FS} \cdot t_{up}}{V_{range}} \qquad (2)$$

With $V_{range} = 3$V, $I_{FS} = 5$nA and $t_{up} = 65$ms a minimum capacitor value is about 100pF.

3. PROBLEM AREAS

Some of the important problems related to the design of the dual slope converter are:

1. Input offset voltages of comparator and integrator;
2. Speed of comparator;
3. Charge injection from switches;
4. Noise considerations.

The input offset voltages of the comparator and the integrator (or rather the difference in their offset voltages) cause the capacitor voltage V_f at the end of the conversion to be different from the capacitor voltage V_i at the start of ramp-up period: $V_{off} = V_f - V_i$. For an ideal reset switch V_i is equal to 0V. If the offset voltages cause the comparator output state to be low (counter disabled) after the reset, the conversion has to proceed for a time $t_{off} = CV_{off}/I_{mes}$ before the comparator changes state and the counter starts counting the time t_{up}. With offsets in the mV-range and $C \simeq 100$pF this delay is unacceptably long for small values (order of pA) of I_{mes}, so the comparator and OTA must be offset

compensated or designed to have an offset that ensures $V_f < V_i$. If $V_f < V_i$ the deintegration time t_{down} will be too long, the error being CV_{off}/I_{ref}. However, this is a constant error which can be eliminated by calibration.

The comparator delay has a similar effect as the offset voltage in the sense that a delayed response from the comparator causes the counter to add a number of counts equal to t_{delay}/T_{clk}. The delay t_{delay} depends on the comparator design and the slope of the discharge, essentially being inversely proportional to the square root of the slope [3]. Simulations show delay times in the order of less than 1μs with a slope of 5nA/100pF=50μV/μs, implying an error of less than 1 LSB's with a 1MHz clock. Furthermore, this is a con-
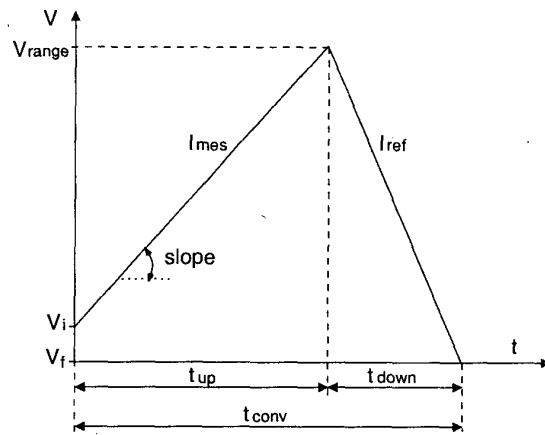

Figure 2. The voltage across the integration capacitor.

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stant error. At the onset of the conversion a comparator delay is worse because it is a signal dependent. As an example, the delay is larger than $100\mu s$ for a current of 10pA, so it is important to ensure that $V_f < V_i$ in order to start with the comparator in the logic high output state.

Charge injection from the switching between I_{ref} and I_{mes} and from the reset switch injects an error charge into the integration capacitor. For a small size transistor, the charge injected into the source or drain terminal in our case is approximately 2.3fC, which can be compared to the charge corresponding to 1 LSB, i.e. $50\mu V \cdot 100pF=5fC$. Apparently, the injected charge is of the same order of magnitude as one LSB, so a means of cancellation of the injected charge is desirable. This is accomplished by using the bridge NMOS switch between I_{mes} and I_{ref} and by using a switch with a dummy transistor for the reset.

Noise is a fundamental performance limitation of the converter. It comes from different sources: an equivalent noise from the reference current and the polarization voltage, an equivalent input noise from the integrator OTA and the comparator, and switching noise induced from the digital components in the system. The noise from the cascode transistor M_{p1} and M_{n1} and the switches is not important because of the impedance levels at these transistor terminals. For the test chip the reference current is supplied from an external current source. For a fully integrated version, the reference current can be supplied by a PMOS transistor which is advantageous compared to an NMOS transistor with respect to $1/f$−noise. Likewise, for the test chip, the polarization voltage is applied externally. Noise and offset voltage at the input of OTA_P will appear as a small voltage across the high impedance node of the measuring electrode, resulting in a change in the current I_{mes} which is the noise and offset voltage divided by the output impedance of the measuring electrode.

The noise at the comparator input and the integrator input are uncorrelated and add to form an equivalent uncertainty (noise) of the comparator threshold. Both high frequency and low frequency equivalent input noise is important. The lower frequency limit can be controlled by the reset cycle (offset compensation cycle) and the high frequency limit can be assumed to be related to the comparator delay, being of the order of t_{delay}^{-1}. With these assumptions we find a total equivalent rms noise from the comparator and the OTA of about $200\mu V$. This corresponds to an uncertainty of 4 LSB's and assuming a Gaussian amplitude distribution of the noise voltage amplitude the maximum uncertainty caused by the comparator and OTA input noise is about 12 LSB's.

4. EXPERIMENTAL RESULTS

The test chip has been designed for a $0.7\mu m$ CMOS process from MIETEC. A full custom layout has been used. The circuit is designed for a supply voltage of 5V. Separate power and ground are used to the analog part of the chip to isolate the more sensitive analog circuitry from the digital switching noise. The comparator is a track-and-latch type [4]. The most critical performance limiting factor has been found to be the equivalent noise at the comparator input. This is around $500\mu V$ which is somewhat higher than expected from the simulations. The reason for this has not yet been fully resolved but some noise is believed to be caused by the external test setup and some noise is believed to be introduced from the digital part of the chip.

The converter has been tested with specially designed current sources I_{ref} and I_{mes}. These sources have a low output noise and
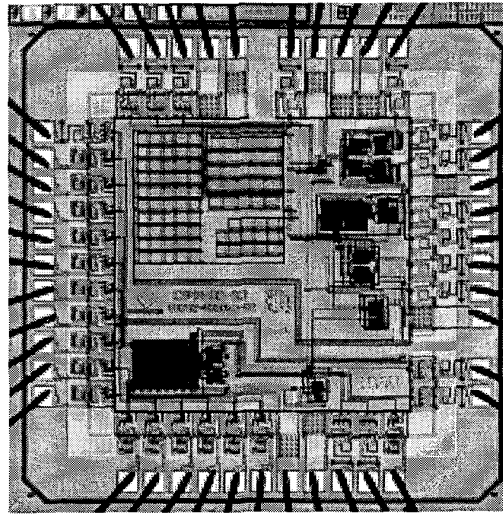

Figure 3. Photomicrograph of the prototype chip.

can be adjusted in the pA range. Due to the low signal level and the high output impedance of the current sources the whole system was shielded by a metal box. Experimentally, when the dynamic range of the integrator is about 1V, the A/D converter was found to have a resolution of 11 bits for a full-scale current of 5nA. Better performance is expected from a fully integrated circuit.

5. FOLDED DUAL SLOPE CONVERTER

Clearly, a design target of 16 bits resolution has not been met with the experimental design. The most severe problem appears to be the equivalent noise at the input of the comparator. In order to reduce this problem it would be highly desirable to have a substantially larger slope of the voltage ramp. If we were able to increase the slope with a factor n, the voltage change during comparisons on the deintegrating ramp would also increase with a factor n, thus increasing the comparator resolution with that factor. However, for the same full scale current I_{ref} this would require a larger dynamic output range of the integrator and this is not possible with a low supply voltage. Instead, a new multi-slope technique [5] is proposed in which the up/down integrations are folded into the available integrator output range. Given an allowed conversion time, with this technique the integration capacitor is reduced by a factor of n, and n up/down integration cycles are performed for each conversion without resetting the integrator between these cycles. Fig. 4 shows the integrator output. Clearly, the integration slope is increased by a factor of n compared to a standard dual slope conversion within an integrator output range of V_{range}. The output of the converter is measured with N-bits resolution in a similar way as a dual slope converter, i.e. by subtracting the known total ramp-up time t_{up} (i.e., the sum of the n ramp-up times t_{up}/n) from the total conversion time t_{conv}.

It is important to realize that the exact time occurrences for the changes between integrating and deintegrating periods does not affect the comparator resolution. What is important is that the total integration and deintegration times are equal to that of the equivalent dual-slope converter, and that the integrator output voltage does not exceed V_{range}. To see this, consider a situation where
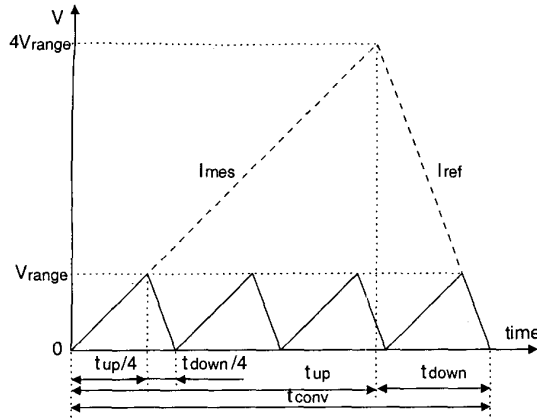
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Figure 4. The integrator output of the folded dual slope ADC ($n = 4$).

the end of the ramp-down period occurs at an integrator voltage of $V_f + \Delta V_f$; i.e., the period has been $\Delta V_f C / I_{ref}$ too short (the ΔV_f could be caused by noise at the comparator input). At the end of the next ramp-up period, the integrator output voltage would be ΔV_f higher than in the ideal case, and the next ramp-down time would then be $\Delta V_f C / I_{ref}$ longer, canceling the error from the previous ramp-down. Thus, only the comparator noise from the very last comparison will affect the total count t_{down}; we have increased the converter resolution by $\log_2(n)$ bits.

A possible problem with the folded dual-slope technique is the charge injection generated by the switches S_1–S_4, when n is high. Assume that the charge injected on C during a conversion cycle is $Q_{sw} + q_{sw}$, where Q_{sw} is a constant value and q_{sw} is a stochastic variable that is evaluated at each cycle. When scaling C by $1/n$, the relative integrator output error after n cycles will be $V_{swerr}/nV_{range} = (nQ_{sw} + \sqrt{n}\,\sigma_{q_{sw}})/(CV_{range})$, where $\sigma_{q_{sw}}^2$ is the q_{sw} variance, compared with $V_{swerr}/V_{range} = (Q_{sw} + \sigma_{q_{sw}})/(CV_{range})$ for the normal dual-slope converter. As the first term is a constant error, it can be eliminated by compensation; the second term, however, shows that there is a limit on high we can choose n. Because we are dealing with such small currents, even if $\sigma_{q_{sw}}$ is in the order of $0.1fQ$, this limit cannot be neglected. Another problem with the accumulated charge injection is when measuring very small currents: if $n^2 Q_{sw}/C$ happen to be negative and larger than the accumulated integrator output caused by the input current, the output of the converter will be a zero. For this reason, it is necessary to deliberately introduce a small positive input offset current (which, of course will be eliminated during the compensation phase).

Apart from the above mentioned accumulated charge injections, the problem areas, and the effects of these, for the folded dual-slope converter are the same as for the conventional dual-slope converter with an integrator range nV_{range}. The converter can easily be calibrated because each switch is operated a fixed number of times during each conversion. The errors from the comparator delay, charge injection, and capacitor nonlinearities can be made signal independent if the same transition of the comparator controls the end of a cycle and the beginning of the next one. An $N = 16$bit folded dual slope converter with $n = 2^6$, and $C = 10$pF offers a good solution.

6. CONCLUSION

A prototype chip of an analog to digital converter for electrochemical amperometric sensors was designed and tested. Test chips demonstrated that a resolution of about 11 bits is readily achievable with a dual slope converter with a full range of 5nA.

In order to achieve higher resolution a new conversion method, folded dual slope, was proposed. The folded dual slope converter requires only very simple extra digital circuitry. Experimental results combined with simulations indicate that the folded dual slope converter can achieve 16 bits resolution in a conversion time less than 200ms. A future version of the test chip will include simple modifications of the digital block to implement the proposed converter.

ACKNOWLEDGMENT

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