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Rasmussen, Tonny Wederberg

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Active gate driver for dv/dt control and active voltage clamping in an IGBT stack

Tonny Wederberg Rasmussen
TECHNICAL UNIVERSITY OF DENMARK
Oersted-DTU, Automation, Elektrovej, building 325
DK-2800 Kgs. Lyngby, Denmark
Tel: +45 45 25 35 26
Fax: +45 45 66 81 11
E-mail: twr@oersted.dtu.dk
URL: www.oersted.dtu.dk

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Keywords

«Converter circuit», «Converter control», «IGBT», «Regulation», «Voltage Source Converter»

Abstract

For high voltages converters stacks of IGBTs can be used if the static and dynamic voltage sharing among the IGBTs can be applied. dV_{CE}/dt should also be controlled in order not to damage insulation material. This paper describes theory and measurements of an active gate driver for stacking IGBTs. For the measurements two series connected standard IGBTs made for hard switching applications are used. Problems are shown and proposals for improvements are given.

Introduction

When using IGBTs in converters the blocking capability is limited to about 6kV. For high power converters in the utility systems such as ASVC (Advanced Static Var Compensators), UPFC (Unified Power Flow Control) and HVDC (High Voltage Direct Current transmission) a higher blocking voltage is necessary. The high voltage blocking capability is needed in order to avoid transformers and to transmit high power without a very high current. Instead of a single IGBT a stack (series connection) can be used [1]. To do this a good control of the static voltage across the Collector-Emitter terminals of the IGBT (Insulated Gate Bipolar Transistor) U_{CE} and the dynamic voltage du_{CE}/dt must be carried out. For this control passive balancing [2] or an active system [3] can be used. For this use an analogue active gate driver has been constructed with an internal reference generation of the voltage U_{CE} across the single IGBT. The functionality of the gate driver is described together with the use of active voltage clamp. Also delay problems are described and solutions are shown. Finally, the gate driver is tested in the laboratory in a stack of two IGBTs and the results for turn-on and turn-off of the IGBTs are shown together with the active clamping. The goal of this work is to control a stack of standard IGBTs.

The requirement for an IGBT stack

The laboratory setup with the IGBT stack, the load R-L and freewheeling diode D_F is shown in Fig. 1. The gate driver is described in Fig. 2.

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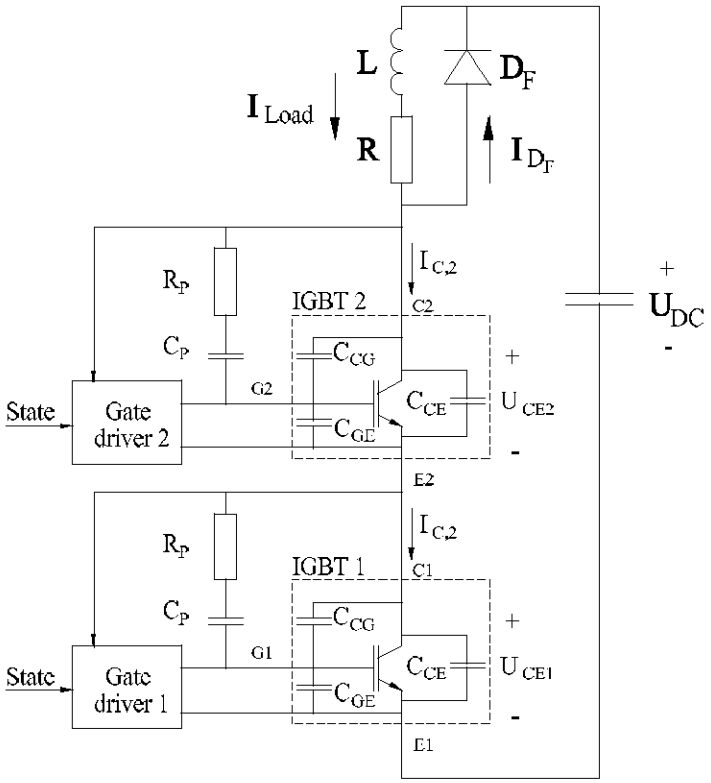

Fig. 1: The laboratory setup U_{DC} = 400V I_{LOAD} = 30A

When switching between on and off the single IGBTs is in the active area of operation characterized by a voltage U_{GE} controlled current generator I_C (2). It is also surrounded by three capacitors internal in the semiconductor C_{CE}, C_{GE} and C_{CG} where C_{CG} changes its value depending on the voltage U_{CG}. At the test bench a capacitor C_P = 10nF in series with a damping resistor R_P = 18Ω is placed in parallel with the Collector-Gate terminals in order to avoid oscillations when $U_{GE} = U_{CG}$. R_P is a damping resistor. This capacitor C_P contributes to the switching loss and should be reduced in future work.

In the stationary turn on (The IGBT conduct current) there is no problem with voltage sharing while the gate voltage U_{GE} is given as high voltage as possible and only the saturation voltage $U_{CE,sat}$ is seen across the IGBTs.
In the stationary turn off (The IGBT does not conduct load current) the possibility of different cut-off currents I_{CES} in the two IGBTs have to be taken into account while these currents can charge or recharge the capacitors C_{CE} and C_{CG} and hereby the IGBTs do not share the voltage equally after some time. In this situation the gate driver works as an active voltage clamp circuit. When U_{CE} reaches the maximum value the gate driver keeps the U_{CE} at that level.

The dynamic turn on process is a commutation of the load current from the free whiling diode to the IGBT and then a discharging of the capacitors (1) C_{CE} and C_{CG} done by the internal current generator.

$$I_{C,CE} = C\frac{du_{CE}}{dt} \tag{1}$$

First, the IGBT takes over the load current from the free wheeling diode I_{DF} and the current $I_{C,CE}$ that is needed to have the right du_{CE}/dt across the IGBT.

The dynamic turn off is a charging of the capacitors C_{CE} and C_{CG} with the right current (1). The IGBT turns off some of the load current and the rest of the current charges the capacitors. This means that there is lower limit of the load current and the du_{CE}/dt according to (1).

The functionality of the gate driver

The block diagram of the gate driver is seen in Fig. 2.

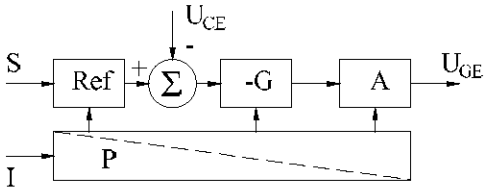

Fig. 2: The block diagram of the gate driver

P is a galvanic insulated (Current transformer) power supply for the gate driver supplied by an AC current I [4]. S is a state signal for on off the IGBT supplied by a fiber-optic cable. Ref is the voltage reference generator described below. G is a proportional gain and A is an analog power amplifier for setting the voltage across C_{GE} and hereby controls the current in the IGBT by (2) and then the voltage slope by (1).

$$I_C = (U_{GE} - U_{TH}) \cdot G_{FS} \tag{2}$$

The basic reference voltage is seen in Fig. 3.

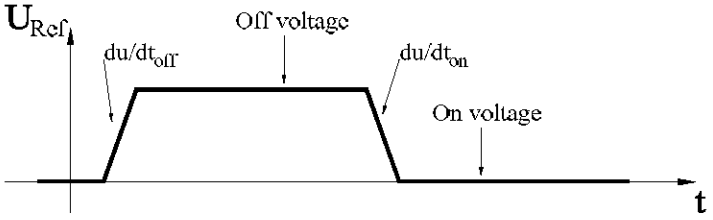

Fig. 3: Reference voltage

The du/dt_{off} is a trade-off between small losses and load current together with the bandwidth of the control system. The reference off voltage should be a little higher than the expected maximum voltage U_{CE} of the IGBT in order to ensure a negative gate voltage U_{GE} at the IGBT. The reference off voltage must not be too high because it has to act as an active clamp voltage for a long turn off period if the leakages currents in the IGBTs are different. Also at the turn on period a high Gate Emitter U_{GE} should be used in order to have a low saturation voltage U_{CE} across the IGBT. This can be done if the reference is made negative in this period. These changes together with the state signal S is shown in Fig. 4 with the thin line as the reference and the tick line as the U_{ce}.

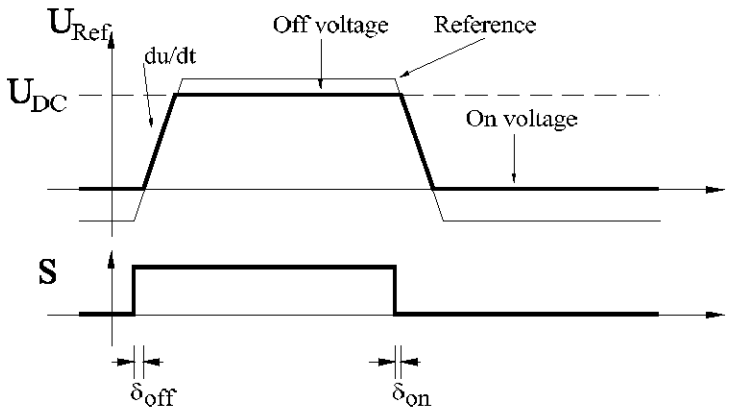

Fig. 4: State signal S together with the delays and reference signal.

Some delays are seen in the system. When the state signal changes to the off it take some time δ_{off} for the reference to reach a negative value close to 0 where (after passing G and A Fig. 2) the gate voltage is in the active area for the IGBT. Also at the turn on there is a small time delay δ_{on} before the IGBT reaches the active area. This delay includes commutation of the load current from the diode D_F to the IGBT.

Delay problem at turn on and turn off

A solution to the delay problem is shown in Fig. 5.

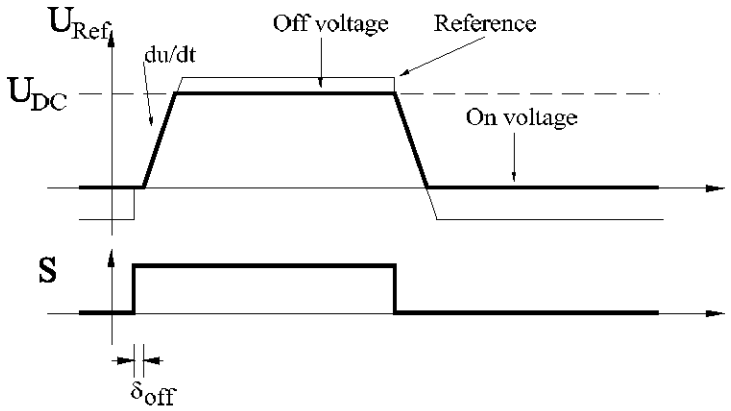

Fig. 5: Reference signal with reduction of delay

At turn off the reference signal is given a step to a negative value close to zero. Then only a small delay is needed to change the gate voltage. Also a step in the turn on could be given but is not used here while the delay is small. A step at turn on can disturb the control system if the active clamp facility is in use.

Laboratory measurements of non-symmetrical conditions

To show the function of the active clamp in the case of non-symmetry in the IGBTs' leakage currents a resistor is placed parallel with C_{CE} across IGBT2 in Fig. 1 in order to discharge the capacitors. The resistor is used while the two leakage currents match each other very well.

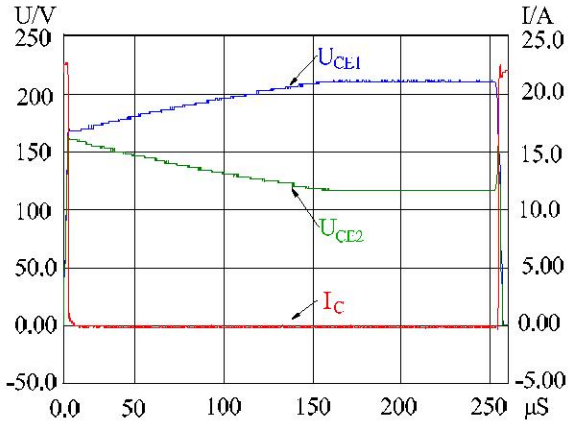

Fig. 6: Active clamping with non-symmetrical conditions

When the IGBTs are switched off U_{CE} increases I_C decreases to 0A and the two IGBTs share the voltage between them t = 5µs. The difference in leakage current caused by the resistor makes the voltage across IGBT2 decrease (Green curve U_{CE1}) but due to the constant DC voltage across the stack of IGBTs the voltage across IGBT1 increases. When U_{CE1} increases to above the reference off voltage the $IGBT_1$ turns on with a small collector current I_C to keep the U_{ce} constant. This is seen in Fig. 6 to 150µS.

Measurements of turn off at non-symmetrical conditions

Fig. 7 shows the reaction of the control system when U_{CE} passes the reference off voltage green curve U_R.

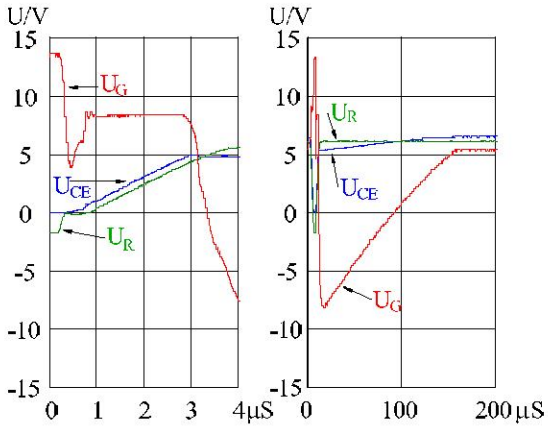

Fig. 7: Control signals at turn off. U_G=Gate voltage, U_R=Reference voltage, U_{GE}=Collector Emitter voltage

On the left of Fig. 7 the gate voltage reduces when the step in reference is made to 0.5µS and after this the gate voltage drive the IGBT in the active mode to control the du_{CE}/dt. When the maximum DC voltage applies across the IGBTs the reference passes the U_{CE} and the IGBT is turned completely off by the negative gate signal voltage.
In the non-symmetrical case Fig. 7 right the Collector Emitter voltage U_{CE} passes the reference to 100µS and the gate turns on the IGBT so I_C matches the leakage current in the other IGBT and hereby the active clamp is in function.

Measurements of turn on at non-symmetrical conditions

When the reference decreases U_{CE1} follows the reference but IGBT2 is off while the voltage is below the reference and U_{CE2} increases until they share the voltage at the reference level and can then turn on I_C. Subsequently, the two voltages decrease until they reach the saturated on voltage.

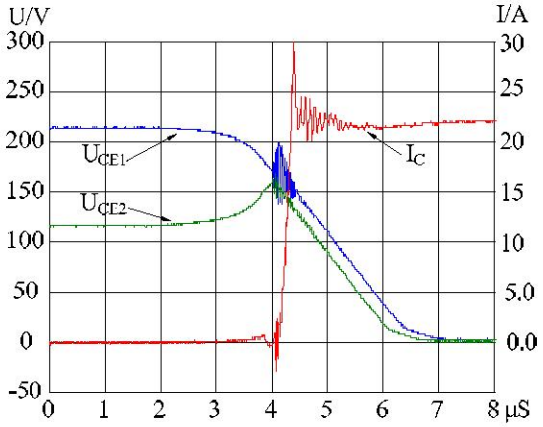

Fig. 8: Turn on after non-symmetrical voltage sharing

There is some high frequency voltage oscillation showing that it is a low inductive construction. The peak in the current comes from the reverse current in the diode.

Dynamic switching at symmetrical condition

Switch on of the IGBTs is seen in Fig. 9 under symmetrical condition where the leakage currents are equal in the two IGBTs.

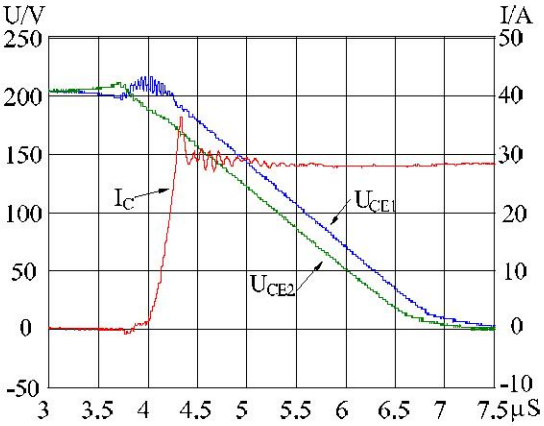

Fig. 9: Turn on of the IGBTs

To 3.5µS the reference not shown in the figure starts decreasing. As long as the collector current I_C is less than the load current the total voltage $U_{CE1}+U_{CE2}$ across the IGBTs has to be constant while the free-wheeling diode D_F conducts load current see Fig. 1. In the interval 4.0µS to 4.3µS the voltage is less than 2 times 200V because of the parasitic inductance from the DC power supply and between the IGBTs (bonding wires) and the free whiling diode gives a voltage drop because of high dI_C/dt in the current.

The difference in gain and delay in the two control systems gives the difference between U_{CE1} and U_{CE2} at 4.0μS. For a better track of the slope a D control is needed together with an improvement in the references.

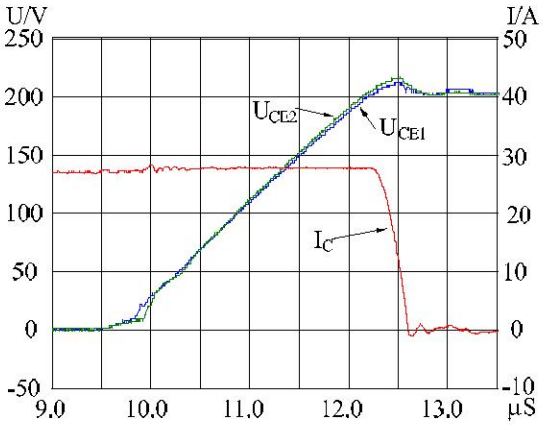

Fig. 10: Turn off of the IGBTs

At turn off the two voltages match each other well. The voltage that overshoots around 12.5μS comes from the dynamic voltage drop across the freewhiling diode when it starts to conduct current.

Discussion

To have equal conditions for the two IGBTs it is very important that the two reference signals are very similar even when they are generated separately for each IGBT.
At turn on the gain in the two control units should match each other in order to have a smaller difference between the U_{CE} at the two IGBTs. This has been tried out but gives difficulties in the turn off process.

The switch loss for this case $U_{CE,MAX}$ = 800,V I_C = 50A, f_s = 15kHz, $t_{on} + t_{off}$ = 5μs is with the used IGBT SKM 100 GB 123D from SEMIKRON is

$$P_{sw} = f_{sw} \cdot \left(t_{on} + t_{off}\right) \cdot \frac{U_{CE} \cdot I_C}{2} = 1.5kW \qquad (3)$$

This shows that the frequency f_{sw} and switching time $t_{on}+t_{off}$ should be reduced. If a better turn-on voltage sharing is made the switching time could be reduced. A high slope of U_{CE} needs a high bandwidth of the gate driver.

The results from an ongoing detailed study of the IGBT and improvement of the reference together with a detailed circuit schematic are the subject for a future paper.

Conclusion

A gate driver for active voltage control including an active voltage clamp for stacking standard IGBTs is described. Laboratory test of an experimental setup has shown good results and pointed out where to improve the gate driver system. It has been shown that standard IGBT can be used even though they are made for hard switching application. The results of the switching are shown and discussed.

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