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A 0.8V, 7μA, Rail-to-Rail Input/Output, Constant G_m Operational Amplifier in Standard Digital 0.18μm CMOS

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Abstract

A two-stage amplifier, operational at 0.8V and drawing 7μA, has been integrated in a standard digital 0.18μm CMOS process. Rail-to-rail operations at the input are enabled by complementary transistor pairs with g_m control. The efficient rail-to-rail output stage is biased in class AB. The measured DC gain of the amplifier is 75dB, and the unity-gain frequency is 870kHz with a 12pF, 100kΩ load. Both input and output stage transistors are biased in weak inversion.

1. Introduction

Constant IC feature size scaling and use of battery powered devices drive nowadays ICs towards reduced supply voltages. Unlike digital circuits, analog circuits do not always benefit from the low supply conditions. The dynamic range is reduced when decreasing signals in a circuit. To increase it, a low-voltage operational amplifier, the main building block in analog and mixed mode circuits, has to deal with signals that extend from rail to rail. An additional challenge in the low-voltage design is the requirement for new circuit solutions because of the fact that the threshold voltage is not scaled proportionally with the supply voltage.

Compact low-voltage power-efficient amplifiers are described in [1-4]. These amplifiers have very good rail-to-rail complementary input stages and current efficient rail-to-rail class-AB output stages. The minimum supply voltage they are able to operate with is equal to two gate-source plus two saturation voltages (2.5 V in [2]).

To ensure operation close to 1V with transistors having relatively high threshold voltages several design techniques such as input level shift [5], bulk driving [6-7], current driven bulk [8], floating-gate MOSFET [9] and DTMOS [10] have been developed. Even though it is possible to overcome the threshold voltage problems, these methods have some disadvantages. Level shifting using resistors increases noise and area, bulk-driven transistors (as well as floating-gate) result in smaller transconductance and therefore less GBW and more noise, are prone to latch-up, and the polarity of the transistor is technology dependent. DTMOS and floating-gate MOSFET require expensive non-standard processing steps.

The amplifier presented here is designed using the approach from [1-2] and a very efficient sub-1V operation is achieved with nMOS (pMOS) transistors having a threshold voltage of 0.45V (-0.5V) by biasing them in subthreshold. In the next chapter the amplifier topology will be presented. Subsequently measurement results will be compared to simulations and finally conclusions will be drawn.

2. Amplifier Description

The amplifier implemented is shown in Figure 1. Its input, output stage and frequency compensation method are described in the following subsections.

2.1. Rail-to-rail Input Stage

A well known method for obtaining a rail-to-rail operation at the input is placing two differential pairs (nMOS and pMOS) in parallel. For low values of common-mode voltage the pMOS transistor pair (M3-M4) will be on, while for high common-mode voltages the nMOS pair (M1-M2) is on. The minimum necessary supply voltage for this configuration is:

$$V_{sup,min} = V_{GSn} + V_{GSp} + V_{DSatn} + V_{DSatp} \quad (1)$$

where V_{GSn} and V_{GSp} are the gate-source voltages of the nMOS and pMOS input transistor pairs, and V_{DSatn} and V_{DSatp} are the saturation voltages of the current sources M9 and M10. For 0.8V operation, the input transistors are biased in weak inversion (2×0.3V + 2×0.1V = 0.8V).

A problem when using a complementary input stage is that the transconductance varies over the input common-mode voltage range, impeding an optimal frequency compensation. In fact, in the middle part of the common-mode voltage range, both input pairs are active at the same time, and the sum of their drain currents is two times the current in the outer part of the common-mode voltage range, when only one of the input pairs is on. Therefore some extra circuitry is needed to keep the total g_m constant. In this amplifier, g_m control is provided by current switches M5-M8. Several g_m control methods have been developed for different regions of operation of input transistors [1, 4]. A good feature of the input stage with the current switches g_m control applied here is that it delivers a constant output current to the summing circuit, consisting of a

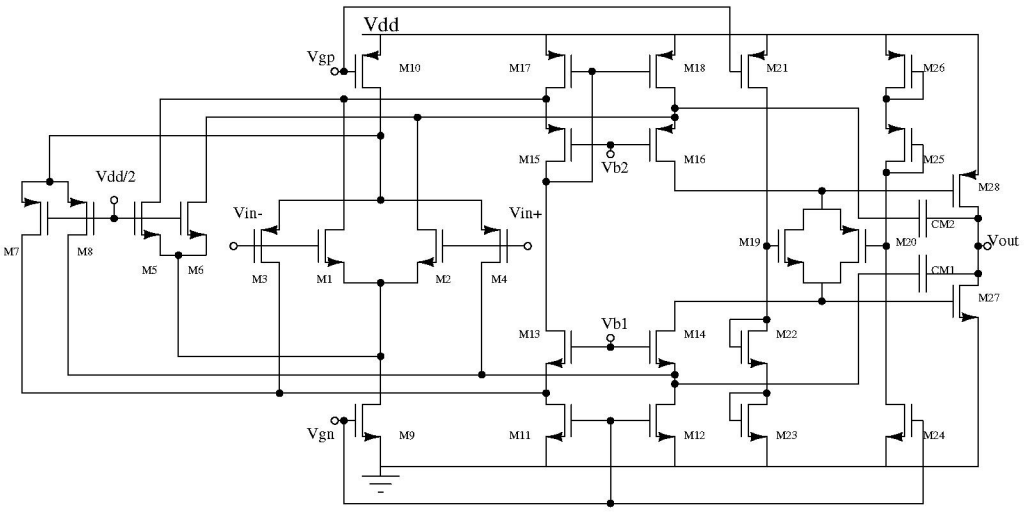

Figure 1: Amplifier Schematics.

high-swing current mirror (M15-M18) and common-gate stages (M13-M14). The summing circuit needs one gate-source voltage (in strong inversion) plus two drain-source voltages for proper operations.

2.2. Class AB Output Stage

To ensure output rail-to-rail operations, the output transistors M27-M28 are connected in a common-source configuration. For the efficient use of the power supply they have to be biased in class AB. Compact class-AB output stages are presented in e.g. [1-3].

In our amplifier, class-AB operations are allowed by the control transistors M19-M20. These transistors are driven by the signal currents from the summing circuit transistors M14 and M16, and their gates are kept at a constant voltage by two pairs of diode-connected transistors (M22-M23 and M25-M26). The diode-connected transistors, the class-AB control transistors, and the output transistor form two translinear loops (M27, M19, M22, M23 and M28, M20, M25, M26), which determine the bias current in the output transistors. Assuming that M22 and M19 have the same gate-source voltages and the same dimensions, M23 and M27 will have the same gate-source voltage as well, and the output quiescent current will be determined by the ratio of the aspect ratios of M27 and M23.

From Fig. 1 it can be concluded that the branch with stacked diodes needs two gate-source voltages plus one saturation voltage for proper operations. In this 0.8V implementation all transistors in the output stage except the current sources are biased in weak inversion. A weak point of this implementation is that the output current varies as a function of the supply voltage.

2.3. Complete Realization

The dimensions of the components shown in Fig. 1 are given in Table 1.

The amplifier is frequency compensated by the cascoded Miller frequency compensation method [2], which, compared to the classical Miller compensation, shifts the non-dominant pole to higher frequencies. This is due to the fact that the cascode transistors are included in the Miller loop, since the compensating capacitors are placed between the drains of the output transistors and the sources of the cascode transistors. The frequency of the non-dominant pole when using the classical Miller compensation depends on the load capacitor, the transconductance of the output transistor, and its gate-source capacitance approximately as $g_m/(C_L + C_{gs})$, and it can be adjusted by changing the current in the output transistor. But since the main goal in this design was a very low current consumption, having at the same time transistors forming translinear loops with two diodes stacked on only 0.7V, it was not possible to obtain optimal frequency compensation with the classical Miller technique, and the cascoded Miller is used instead.

MOST	W(μm)/L(μm)	I_D(I_{REF}=1.09μA)
M1, M2, M5, M6	50/0.36	$I_{REF}/4$
M3, M4, M7, M8	165/0.36	$I_{REF}/4$
M13, M14	10/0.36	$I_{REF}/2$
M15, M16	33/0.36	$I_{REF}/2$
M9, M11, M12	10/6	I_{REF}
M10, M17, M18	33/6	I_{REF}
M24	2.5/6	$I_{REF}/4$
M21	8.25/6	$I_{REF}/4$
M19, M22	30/0.18	$I_{REF}/4$
M20, M25	99/0.18	$I_{REF}/4$
M23	5/0.18	$I_{REF}/4$
M26	16.5/0.18	$I_{REF}/4$
M27	60/0.18	$3I_{REF}$
M28	198/0.18	$3I_{REF}$
CM1, CM2	1.075pF	

Table 1: Transistor dimensions, drain currents (with a common-mode voltage of $V_{DD}/2$), and capacitor values.

In this implementation, the class-AB control transistors are biased by the summing circuit, which is feasible since the output current of the first stage for the used g_m control method is not dependent of the common-mode voltage. To obtain an output circuit independent of the g_m control method, with minimized noise and minimized depen-

dence of the quiescent output current on the supply voltage, the compact operational amplifiers described in [1-2] have two high-swing current mirrors biased by a floating current source. For proper operation the two current mirrors need two gate-source voltages in strong inversion, and this implementation is not feasible for 0.8V operations in the technology used here.

3. Amplifier Performance

The amplifier has been fabricated in a standard digital 0.18μm n-well CMOS process (threshold voltages of 0.45V and -0.5V for nMOs and pMOS, respectively). The chip photograph is shown in Fig. 2.

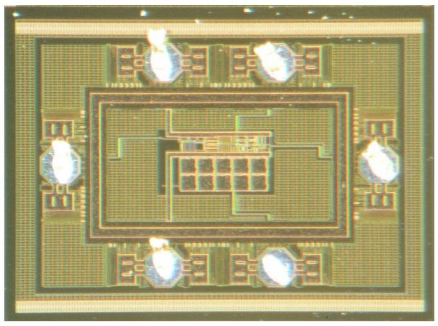

Figure 2: Chip photo.

Using a 1pF Miller capacitor, the simulated unity-gain frequency (GBW) is 1.1MHz for a 5pF load, with a phase margin of 71°. The simulated DC gain is 84dB, while the measured value is 74dB. The capacitive load in the measurement setup is estimated at 12pF in parallel to 100kΩ. The measured unity-gain frequency is 870kHz. When reducing the supply voltage to 0.7V, the amplifier will still be operational, with a GBW reduced to 760kHz. Simulated and measured frequency characteristics are compared in Fig. 3 (V_{DD}=0.8 V, input common-mode voltage V_{COM}=0.4 V).

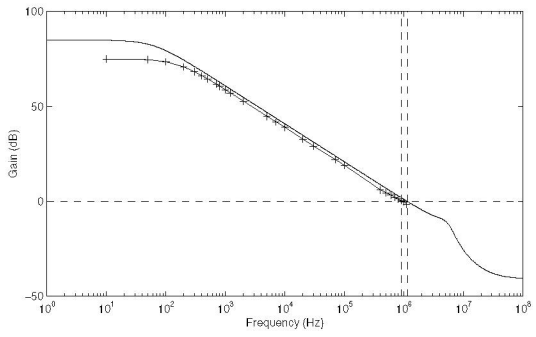

Figure 3: Comparison of the simulated and measured (+) frequency response of the amplifier.

The measured current consumption for this amplifier is 7μA with 0.8V supply voltage, and it is simulated that the supply current will increase to 10.5 μA for V_{DD} of 1.5 V. This increase is due to the increase of the quiescent current in the output transistors for higher supply voltage.

The simulated GBW variation as a function of the common-mode voltage is compared to the measured variation in Fig. 4. The measured variation is 8%, which is very close to the variations for transistors in weak inversion found in the literature [1, 5].

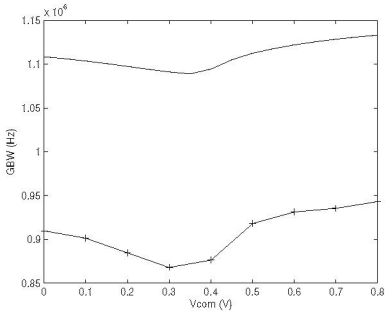

Figure 4: Simulated versus measured (+) variation of the GBW as a function of the input common-mode voltage.

Measurement results when the amplifier is connected in a unity-gain buffer configuration are shown in Fig. 5. Large (300mV) and small (50mV) 250kHz input step signals are shown, along with the respective measured and simulated outputs. The measured slew rate is 0.6V/μs,

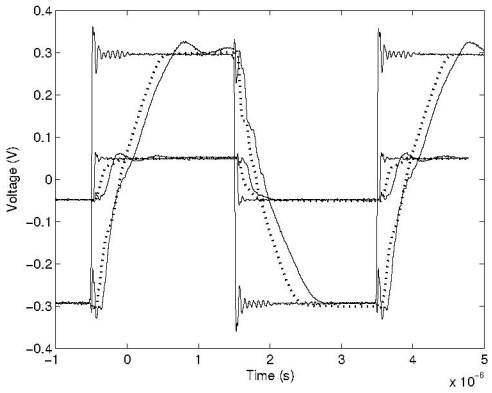

Figure 5: Measured input and output and simulated output (·) signal for unity-gain buffer configuration.

matching well the simulated 0.66V/μs. Due to the high load capacitance, the phase margin of the amplifier is reduced, compared to the simulated value, and therefore an overshoot can be noticed in the measured response. It has been simulated that the frequency response of the buffer starts deteriorating for common-mode voltages 50mV from the supply rails. When the amplifier is loaded resistively in the unity-gain buffer configuration, it has been measured that the output signal will be clipped ±20mV from the supply with a 1kΩ load, while simulations show clipping at V_{DD}-16mV and V_{SS}+10 mV. The simulated value of the maximum current that can be delivered is 2mA for an output voltage 100mV from the supply rails.

Method	Ref.	Tech.	VDD (V)	Gain (dB)	GBW, PM	Load	Isup (μA)	$\frac{GBW}{P}$ ($\frac{MHz}{mW}$)
Compl. pair	[2]	1 μ	2.5-6	85	2.6 MHz, 66 $^\circ$	10 pF, 10 kΩ	180	5.77
Compl. pair	[2]	1 μ	2.5-6	87	6.4 MHz, 53 $^\circ$	10 pF, 10 kΩ	180	14
Compl. pair	[3]	1.6 μ	1.8-7	86	4 MHz, 67 $^\circ$	5 pF, 10 kΩ	230	9.66
Compl. pair	[4]	0.7 μ	1.3-1.8	84	1.3 MHz, 64 $^\circ$	15 pF	350	2.85
Compl. pair level shift	[5]	0.8 μ	1	75	1.8 MHz, 57 $^\circ$	15 pF,1 MΩ	136	13.25
Bulk-driven	[6]	2 μ	1	48	1.3 MHz, 57 $^\circ$	22 pF	300	4.3
Bulk-driven	[7]	0.35 μ	1	70	190 kHz, 60 $^\circ$	7 pF	5	38
Current-driven bulk	[8]	0.5 μ	0.7-1	62	2 MHz, 57 $^\circ$	20 pF	40	71
Floating-gate	[9]	0.35 μ	1.2	65	230 kHz, 62 $^\circ$	9 pF	4.3	44
DTMOS (Simul. only)	[10]	0.18 μ	1	64	35.7 MHz, 64 $^\circ$	5 pF, 10 kΩ	522	68
Compl. pair	This work	0.18 μ	0.8	74	870 kHz, 66 $^\circ$	12 pF, 100 kΩ	7	155

Table 2: Properties of low-voltage amplifiers from literature.

The corner frequency of the flicker noise lies at 2.5kHz, and the thermal noise level is 120$\frac{nV}{\sqrt{Hz}}$. The amplifier occupies an area of 0.033 mm^2.

4. Conclusion

The designed amplifier shows very good performances concerning low-voltage, low-power, rail-to-rail operations, and it is capable of driving resistive loads efficiently as well. Its design is based on a robust approach, and low-power operations are achieved by the use of very low bias currents in a modern technology.

The main properties of rail-to-rail, low-voltage amplifiers found in the literature are summarized in Table 2, and the properties of the amplifier designed in this work are listed in Table 3. If the ratio of GBW to power consumption (for the same load) is taken as a figure of merit, as proposed in [2], the amplifier described here shows superior performance compared to the amplifiers in Table 2.

Parameter	Value	Unit
Die area	245×135 (0.033)	μm^2 (mm^2)
Supply voltage	0.8 to 2	V
Supply current	7	μA
Max. out curr. (Sup $\pm$100 mV) *	2	mA
g_m variation	8	%
CMIR*	0.05 to V_{DD}-0.05	V
Out. swing (with 1 kΩ load)	0.02 to V_{DD}-0.02	V
Offset voltage	3.6	mV
Input noise floor	120	$\frac{nV}{\sqrt{Hz}}$
Corner frequency	2.5	kHz
CMRR*	75	dB
Open-loop gain	74	dB
Unity-gain frequency	870	kHz
Unity-gain phase-margin	66	$^\circ$
Slew-rate	0.6	V/μs
PSRR*	56	dB
$\frac{GBW}{P}$	155	$\frac{MHz}{mW}$
V_{DD}=0.8 V, C_L=12 pF, 100 kΩ, T=27 $^\circ$C		
*simulated value, C_L=5 pF		

Table 3: Amplifier properties.

5. Acknowledgments

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