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Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion

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Abstract:

Frequency modulation in ring VCOs is investigated. Primarily, the linearity of conversion from input voltage to output frequency is considered. Bulk-voltage control of the threshold voltage of the VCO transistors is found to be a very promising approach for applications in frequency ΔΣ converters. Different approaches apply in presence of high supply voltages, when transistors work in strong inversion, compared to low supply voltages, when transistors are in weak inversion. In strong inversion, second-order effects controlled by the supply voltage linearize the VCO modulation, while in weak inversion an improved linearity can be obtained using soft rails, at the expense of a reduced sensitivity.

1. Introduction

A frequency ΔΣ converter (FDSM) is a ΔΣ converter without feedback [1]. The feedback in a ΔΣ converter can be eliminated by building a system consisting of an integrator and a differentiator. The signal is integrated, after which it is sampled and differentiated. Assuming that the output of the sampling consists of the input signal and some added quantization noise, it can be seen that the signal is passing unchanged through the converter, while the quantization noise is differentiated or high-pass filtered. The output phase of a VCO is the input voltage integrated, and thus a complete FDSM is obtained by sampling the phase and differentiating the result, as illustrated in Fig. 1.

If the VCO is nonlinear, it will introduce a harmonic distortion to the signal, and the signal to noise and distortion ratio will possibly be limited by the nonlinearity. We believe that an attractive VCO architecture for use in a FDSM is a voltage-controlled inverter-ring oscillator (RVCO), due to the two following reasons: the possibility of a rather high linearity when frequency tuning is performed from the bulk terminal of the MOS transistors

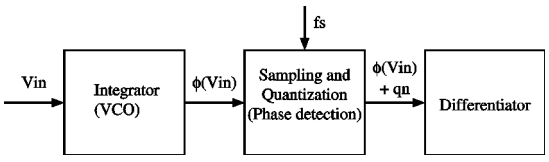

Figure 1. Block diagram of FDSM. The integrator is implemented as a VCO

(as shown later), and the low supply voltage and power consumption capabilities of this VCO type [2].

According to the literature on RVCOs, the primary consideration is often wide tuning range and low phase noise [3] [4], and current starvation is commonly used to control the oscillation frequency. These topics are of secondary importance to the FDSM, and they will not be treated in this paper. Controlling the frequency with the bulk voltage has some similarities to the current-starvation principle, but it has linearity advantages at the expense of a smaller tuning range, compared to current starvation. This is discussed in section 2.

The linearity of the bulk-controlled RVCO is discussed when transistors are operating in strong inversion and weak inversion, respectively. In both cases, the validity of the approaches is supported by spectreRF simulations.

2. Voltage to frequency relations in the RVCO

The RVCO consists of an odd number (N) of inverters connected in a ring. In each of the inverters the signal will be delayed by the time t_d, thus the output frequency of the oscillator is given from:

$$f = \frac{1}{2 N t_d} \tag{1}$$

Each node in the inverter chain is loaded by a capacitance C_L consisting of the total gate capacitance from two transistors, the total drain capacitance from two transistors, routing capacitance, and a possible additional capacitance or varactor. The delay in the inverter exists due to the time it takes the transistors in the inverter to charge C_L. If N is large enough, all nodes will be completely charged and discharged during one period, and each inverter delivers the charge $C_L V_{dd}$. The transistor charging the capacitance will initially charge it with a maximum current I_D. The current decreases during the transition, and if ηI_D is the mean current (disregarding leak currents), the frequency of the RVCO is given by

$$f = \eta \frac{I_D}{2 N C_L V_{dd}} \tag{2}$$

N and η are fixed parameters for a given RVCO, but from (2) it is clear that f can be controlled through C_L, V_{dd} and I_D.

C_L can be controlled by a varactor, such as a biased pn junction. This is simple and effective, but also highly nonlinear [5]. A linear conversion can be obtained by switching on and off fixed capacitors, according to the magnitude of the input voltage. However, this requires large capacitor arrays at each node, and, more importantly, an A/D converter to control the switches, making it unsuitable in an A/D converter design.

Controlling V_{dd} will also influence I_D, as it is seen in the following sections. This principle has been shown to produce a reasonably good linearity. However, it requires high input voltages and the input signal is loaded with pulses and a generally low impedance. This solution is not suitable in a low supply voltage and low power circuit.

I_D can be controlled through different current starving techniques. This approach results in a wide tuning range, but is also very nonlinear. Controlling I_D with the threshold voltage of the transistors through the bulk voltage yields a better linearity. Furthermore, this solution implies a high and stable input impedance, and if V_{dd} is lower than one diode voltage, it is possible to have rail to rail inputs, or even input voltages exceeding the supply voltage.

3. Bulk-controlled RVCO in strong inversion

The behavior of the RVCO depends on the operation region of the transistors. It can be assumed that all nodes are completely charged or discharged during an oscillation period. This means that the drain-source voltage across the transistor that is about to be turned on is V_{dd}, while the gate-source voltage will be lower than the drain-source voltage. Assuming that the supply voltage is high, the transistor will saturate when the gate-source voltage passes the threshold voltage (V_{th}). To a crude approximation the saturation drain current is given by

$$I = \frac{W}{2L}\mu_{eff}C_{ox}(V_{gs} - V_{th})^2 \qquad (3)$$

where W and L are transistor dimensions, μ_{eff} is the effective carrier mobility, and C_{ox} is the oxide capacitance. The maximum current used in (2) is obtained from (3) when the gate-source voltage equals V_{dd}. It is seen that V_{th} is in the equation for the drain current thus a model of the bulk dependency of V_{th} is needed. When the bulk source voltage V_{BS} is increased, the depletion area and thus the space charge is reduced. Due to charge neutrality through the MOS structure, the threshold voltage will be reduced according to:

$$V_{th} = V_{t0} + \gamma(\sqrt{2\Phi_f - V_{BS}} - \sqrt{2\Phi_f}) - K_B V_{BS} \qquad (4)$$

where V_{t0} is V_{th} when $V_{BS} = 0$, γ is a process constant and Φ_f is the surface potential of the MOS transistor. The last term is a secondary short-channel effect. It is seen from the equations that if V_{BS} is increased, V_{th} is reduced. This results in an increased current in the transistor and thus an increased oscillation frequency. Now (3) is rewritten as:

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}(V_{dd}^2 + V_{th}^2 - 2V_{dd}V_{th}) . \qquad (5)$$

To operate in strong inversion, $V_{dd} > V_{th}$ is required, and the term with linear dependency to V_{th} will dominate. If the constant part of (4) is replaced with $K_\Phi = V_{t0} - \gamma\sqrt{(2\Phi_f)}$ and the bulk-voltage dependent part is replaced with $y = \gamma\sqrt{(2\Phi_f - V_{BS})}$, a first-order approximation of the current can be written as

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}(V_{dd}^2 + K_\Phi^2 - 2V_{dd}K_\Phi + \gamma^2 y^2 - 2\gamma(V_{dd} - K_\Phi)y). \qquad (6)$$

When V_{dd} is high, the linear dependency on y is dominating, and the current will grow with a power to V_{BS} larger than one. When V_{dd} is reduced, the linear second-order effect in (4) becomes more important, making the dependency more linear.

In a real RVCO the load capacitance as well as μ_{eff} [7] will also be dependent on the bulk voltage. Reducing V_{dd}, and thus the primary effects, increases the influence of the secondary effects. These, in turn, reduce the oscillation frequency when V_{BS} is increased, and will increase the linearity in a limited V_{BS} range for low supply voltages in the strong inversion region. This is illustrated by the spectreRF simulation of a 5-stage RVCO implemented in a 0.13 µm CMOS process. In Fig. 2 the increased influence of second-order effects at low supply voltages is illustrated by the sensitivity K_s of the output frequency f versus the tuning voltage V_{BS} (i.e., $K_s = \delta f/\delta V_{BS}$), for supply voltages of 1.2 V and 600 mV. Both plots are normalized the value of the sensitivity for V_{BS} =0.6 V. It should be added that only the bulk voltage of the n-mos transistors is controlled. Both n-mos and p-mos bulk could be controlled, but it would require two different voltage levels dependent on each other, which is difficult to accomplish.

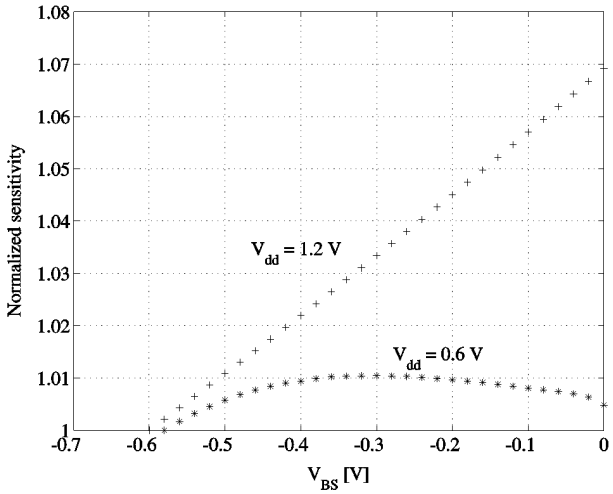

Figure 2. Sensitivity of 5 stage RVCO normalized to their minimum value with supply voltages of 1.2 V and 0.6 V

The plot of the oscillation frequency versus the tuning voltage V_{BS}, for V_{dd} = 600 mV, is shown in Fig. 3, with the corresponding sensitivity (without normalization) in Fig. 4.

A measure of the nonlinearity of the transfer function of the VCO is given by

$$NL = \frac{\Delta K_s}{2K_{s-mean}} 100\% \qquad (7)$$

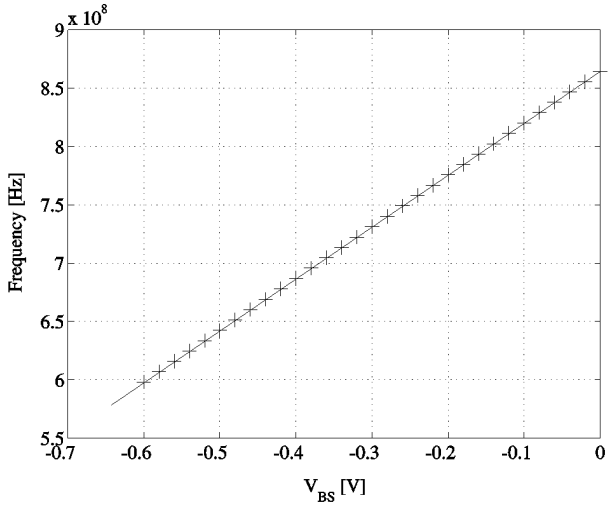

Figure 3. RVCO transfer function for a 5 stage RVCO simulated in Cadence

(see Fig. 4). The nonlinearity is 0.5 % over an input range of 0.6 V with a supply of 600 mV. However, if the supply voltage is higher, the nonlinearity increases, and e.g. at V_{dd} = 0.9 V the nonlinearity is 6.0 % and the sensitivity curve is monotonically increasing.

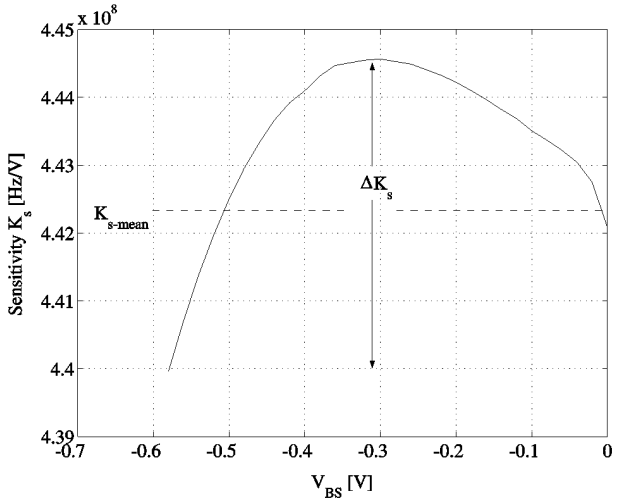

Figure 4. Sensitivity of the RVCO illustrates a nonlinearity of 0.5 %

4. Bulk-controlled RVCO in weak inversion

In many applications low supply voltages are desired. In these applications the RVCO is advantageous, and it has been reported to function down to 80 mV [2]. When V_{dd} decreases below V_{th} the channel in the transistors can no longer exist, and they are working in the weak inversion region. This means that the current expression is not given by (3), but depends exponentially on V_{gs} as in a bipolar transistor. V_{th} influences the drain current according to [6]

$$I = I_0 e^{(V_{gs}-V_{th})/nV_T}\left(1 - e^{-\delta V_{DS}/V_T}\right) \qquad (8)$$

where I_0 is a proportionality constant, V_T is the thermal voltage, δ and n are fitting parameters, and V_{DS} is the drain-source voltage. The maximum current is found, as a function of V_{th}, when $V_{gs} = V_{dd}$. The last term in (8) can be a part of I_0.

The threshold voltage V_{th} is, according to the approximation given by (4), independent of the operation region of the transistor. This means that the maximum current, and thus the frequency in weak inversion, is proportional to

$$I_D \propto e - \gamma\sqrt{2\Phi_f - V_{BS}}\,/\,nV_T \qquad (9)$$

This implies that I_D is a function of V_{BS} to a power higher than one, and the sensitivity of the RVCO will be increasing with V_{BS}. To obtain linearity, this effect should be compensated. When V_{gs} is replaced with V_{dd}, it is seen from (8) that a reduction of V_{dd} will decrease I_D, and this effect can be used as a feedback mechanism on I_D. The feedback can be obtained with so-called soft rails by providing the supply voltage in the inverters through a biased transistor, as shown in Fig. 5.

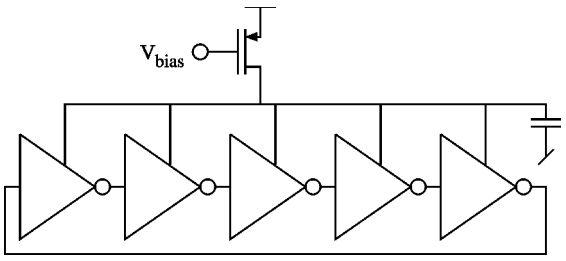

Figure 5. RVCO with soft rails

When V_{BS} is increased, V_{th} is reduced, and the average current in the bias transistor ηI_D is increased. This will cause an increased drain-source voltage across the bias transistor, and the negative feedback is obtained. The bias transistor will also be operating in weak inversion with a constant V_{gs} and V_{th}. According to (8) the drain source voltage of the bias transistor is given from the average current $I_{D\text{-}B}$ as

$$V_{DS-B} = -\frac{V_T}{\delta}\ln\left(1 - \frac{I_{D-B}}{I_{0-B}}\right) \qquad (10)$$

where $I_{0\text{-}B} = I_0 \exp((V_{bias}\text{-}V_{th})/nV_T)$. The length of the bias transistor changes the curvature of the (I,V) characteristic. To maximize the linear tuning range, it should be short. However, if it becomes too short it will not be able to provide sufficient feedback. Cadence simulations of two (I,V) characteristics for bias transistors with different lengths can be seen in Fig. 6.

The width of the bias transistor and the gate bias voltage V_{bias} adjust the work point to a portion of the (I,V) characteristic where the curvature provides the desired feedback. The principle is illustrated with a Cadence simulation of the frequency and sensitivity in Fig. 7 and Fig. 8. The same process as in the strong inversion simulation is used, and the supply voltage is 200 mV. It is seen that the nonlinearity is improved from 27 % to 2.4 % when soft rails are used, at the expense of a lower sensitivity. It should be mentioned that simulations in weak inversion are often not very reliable, and good performances for the circuit just described are likely to be obtained only after some prototyping.

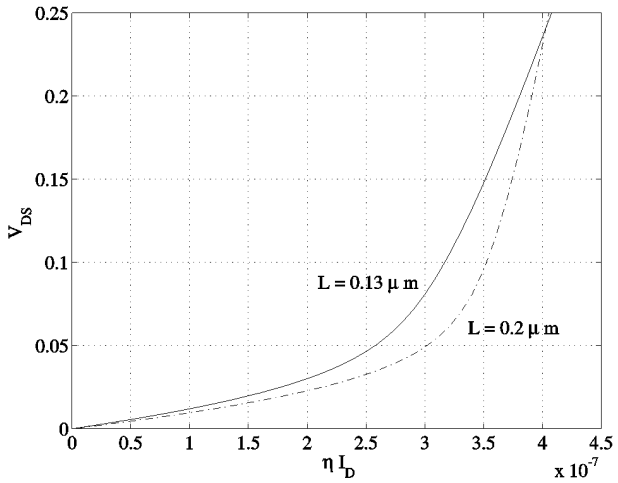

Figure 6. Cadence simulation of (I,V) characteristic of two bias transistors with lengths of 0.13 µm and 0.2 µm

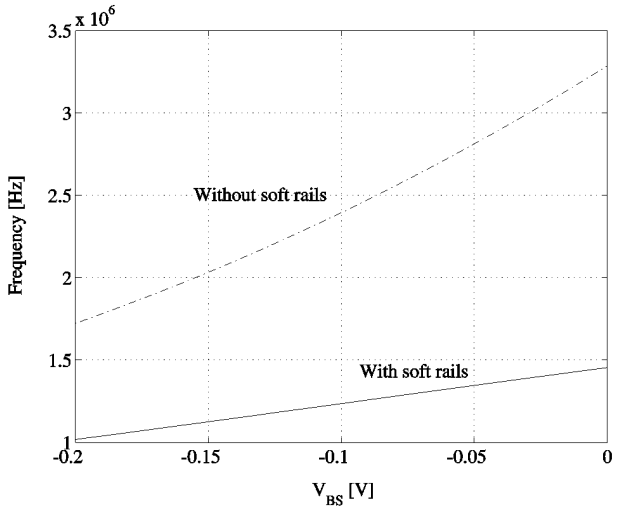

Figure 7. RVCO output frequency in weak inversion supplied with 0.2 V with and without soft rails

5. Conclusion

Modulation linearity was discussed for inverter-ring voltage-controlled oscillators (RVCOs). This type of VCO was found to be a good realization for the integrator in an FDSM, where linearity in the conversion between input voltage and output frequency is important.

The RVCO was studied in two situations: when the supply voltage is high enough to bring the transistors in strong inversion, and when the supply voltage is low, forcing the transistors in weak inversion.

In strong inversion the influence from second-order effects was seen to be controlled by the supply voltage, where a lowering of the supply voltage increased the influence of these effects. Through simulations it was shown that, when the optimal supply voltage (0.6 V in this simulation) was found, the nonlinearity could be reduced to 0.5 % for a full scale input signal.

In weak inversion it was seen that the modulation is generally nonlinear. The linearity was shown to be greatly improved by using soft rails for the supply voltage to the RVCO inverters. Through simulations on a RVCO supplied with 0.2 V this principle was shown to improve the nonlinearity from 27 % to 2.4 % for a full scale input.

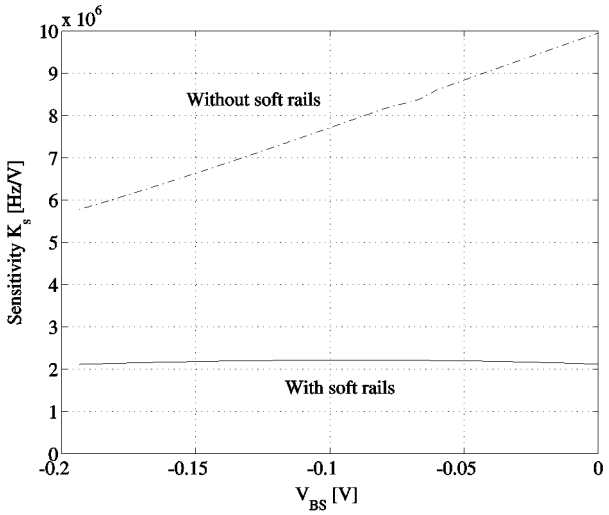

Figure 8. Sensitivity of the RVCO in weak inversion supplied with 0.2 V with and without soft rails

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