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1/f Noise Characterization in CMOS Transistors in 0.13μm Technology

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Abstract

Low-frequency noise has been studied on a set of n- and p-channel CMOS transistors fabricated in a 0.13μm technology. Noise measurements have been performed on transistors with different gate lengths operating under wide bias conditions, ranging from weak to strong inversion. Noise origin has been identified for both type of devices, and the oxide trap density N_t, the Hooge parameter α_H and the Coulomb scattering parameter α_s have been extracted. The experimental results are compared with simulations using the BSIM3v3 MOS model.

1. Introduction

There is an increasing need for accurate low-noise circuits, as the technology-driven decrease in power supply voltage makes it increasingly difficult maintaining a high signal-to-noise ratio in modern analog designs. It is well known that a reduction in device size leads to an increased 1/f noise. In addition, as low-frequency noise is strongly technology dependent, novel processing steps introduced with technology downscaling lead to performance deviations which are difficult to predict [1]. To achieve an accurate prediction of the impact of 1/f noise on circuit performance, accurate noise modelling is required. Despite more than thirty years of research, a controversy still exists about the physical origin of 1/f noise in MOS transistors. Some authors attribute its origin to fluctuations in the total number of charge carriers [2], some to fluctuations in the mobility of carriers [3], and some to both [4]-[5]. The widely used BSIM3v3 MOS noise model implemented in commercially available circuit simulators is based on the latter approach [6].

In order to investigate the validity of noise models available to a circuit designer, in this work, a low frequency noise analysis is performed on n-channel and p-channel transistors biased both in weak and strong inversion, and both in linear and saturation regime. The noise measurement data are analyzed to identify the noise origin. The physical parameters N_t (oxide trap density), α_H (Hooge parameter), and α_s (Coulomb scattering parameter) have been extracted, and finally measurement data have been compared to simulations using BSIM3v3 noise model with noise parameters provided by the foundry.

2. Noise Models

Two main theories are used to describe the origin of 1/f noise in MOS transistors.

McWhorter carrier number fluctuations (ΔN) theory explains the noise origin by the fluctuations of the channel free carriers due to the random trapping and detrapping of charges in the oxide traps near the Si-SiO_2 interface. Theoretical formulation for the drain current power spectral density S_{I_D}, based on the ΔN theory proposed by Reimbold [7] and Van der Ziel [8] for transistors working in weak inversion, is given by

$$S_{I_D} = \frac{q^4 N_t}{kTWL\gamma C_{ox}^2 \eta^2} \frac{I_D^2}{f} \tag{1}$$

where N_t is the trap density, γ (10^8/cm) is the tunnelling constant for the traps, and η is the weak inversion slope factor, given by (C_{ox}+C_D+C_{it})/C_{ox}, with C_{ox}, C_D and C_{it} being the oxide, depletion and interface trap capacitances per unit area, respectively (W, L, q, kT have their usual meaning). Experimental results in general show that the formalism (1) explains very well 1/f noise in weak inversion. In fact, the value of N_t can be extracted from noise measurements against drain current, if other parameters from (1) are known. Furthermore, this parameter is related to the BSIM noise parameter NOIA as N_t=NOIA/q. For transistors working in strong inversion in the ohmic range, the ΔN-based model of S_{I_D} can be expressed by [9]

$$S_{I_D} = \frac{q^2 kTN_t \mu_{eff}^2}{\gamma} \frac{W}{L^3} \frac{V_{DS}^2}{f} \tag{2}$$

with V_{DS} being drain-source voltage and μ_{eff} effective mobility.

The second 1/f noise theory, Hooge mobility fluctuation ($\Delta\mu$) theory [3], explains the origin of 1/f noise by the fluctuations of bulk mobility with the empirical relation for homogeneous semiconductors, given by

$$S_{I_D} = \frac{\alpha_H}{N} \frac{I_D^2}{f} \tag{3}$$

where α_H is Hooge parameter, constant for a given technology and N the total number of carriers under the gate. After estimation of N, it can be shown [9] that for a MOS transistor working in the linear region the following applies

$$S_{I_D} = \alpha_H q \mu_{eff}^2 \frac{W}{L^3} (V_{GS} - V_{th}) \frac{V_{DS}^2}{f} \tag{4}$$

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The measured 1/f noise in n-MOS transistors in strong inversion in the ohmic region usually shows constant S_{I_D}/μ_{eff}^2 versus gate bias voltage, in agreement with (2), which can not be predicted by the $\Delta\mu$ model, because of the bias-independent α_H; thus, the 1/f noise origin for n-devices is attributed to the number fluctuation theory. On the other hand, the observed dependence on the gate bias for the same region for p-channel transistors is following the $\Delta\mu$ theory, in line with equation (4), and can not be explained by ΔN. However, quadratic variation of S_{I_D} versus drain current, following the ΔN model described by (1), is observed for both n- and p-transistors in weak inversion, and can not be explained by the Hooge model. This controversy, known from the experiments published in the literature, has been observed in our experiments as well, which will be presented in the next section.

Recent modelling efforts combine the two previously described approaches in the correlated number and mobility fluctuations ΔN-$\Delta\mu$ model [4]-[5], in an attempt to come to a universal model valid for both n- and p-channel transistors in all operation regions. This model takes into account that the oxide/interface traps, apart from modulating the number of carriers, indirectly interact with the carrier mobility through Coulomb scattering. By this approach, the normalized drain current noise spectral density takes the form presented by Ghibaudo [5]

$$\frac{S_{I_D}}{I_d^2} = [1 + \alpha_s \mu_{eff} C_{ox} \frac{I_D}{g_m}]^2 (\frac{g_m}{I_D})^2 S_{Vfb} \qquad (5)$$

where α_s is scattering parameter and S_{Vfb} is the flatband voltage spectral density given by

$$S_{Vfb} = \frac{q^2 kT N_t}{\gamma W L C_{ox}^2} \frac{1}{f} \qquad (6)$$

Since for weak inversion

$$\frac{g_m}{I_D} \approx \frac{q}{kT} \frac{1}{\eta} \qquad (7)$$

and by neglecting the scattering term in (5), it can be noticed that

$$\frac{S_{I_D}}{I_D^2} = (\frac{g_m}{I_D})^2 S_{Vfb} \qquad (8)$$

equals equation (1). Similarly, by plugging in the formulas for μ_{eff} and $\frac{I_D}{g_m}$ in the linear region in (5), it can be shown that the input referred noise voltage density takes the form

$$S_{V_g} = [1 + \alpha_s \mu_0 C_{ox} (V_{GS} - V_{th})]^2 S_{Vfb} \qquad (9)$$

where μ_0 is the low-field mobility and V_{GS} the gate-source voltage.

The ΔN-$\Delta\mu$ model described shows a satisfactory fitting to the experimental data for both p- and n-channel devices. However, critical discussions on its exactness exist [10]. A form of the unified model noise expression (5)-(9) is implemented in the BSIM3v3 circuit simulator model [6].

3. Experimental Study

3.1. Measurement Set-Up

The devices studied are fabricated in a 0.13μm CMOS technology with oxide thickness 2.4nm, n+/p+ poly gate, shallow trench isolation and Co-silicided drain, source and gate. All the transistors tested have width W=10μm and different lengths. Transistors of the same type have common gate, source and bulk connections, and separate drains. Prior to noise measurements, DC characteristics $I_D(V_{GS})$ and $g_m(V_{GS})$ have been measured. From the DC characteristics for V_{DS}=50mV using the function $\frac{I_D}{\sqrt{g_m}}$ as described in [11], the conduction parameters μ_0, V_{th}, ΔL and S (S=$(\frac{dlogI_D}{dV_{GS}})^{-1} = 2.3\frac{kT\eta}{q}$), given in Table 1, have been extracted for both p- and n-transistors. The drain current noise of the tested devices has been amplified by a low-noise amplifier AD707JN connected in a transconductance configuration, and measured for different transistor bias voltages. The amplifier has been biased using batteries, while the variable voltage values supplied to the DUT have been generated from a PC using the NI6289 high precision data acquisition card. The same card has been used for measurements with the noise spectra obtained with help of NI software. Lorentzian-like spectra usually observed on the top of 1/f noise for small area or minimum size devices have not been taken into account. The same noise behavior has been observed on three measured samples.

L (μm)	0.13	0.26	0.5	1	2
$V_{thn}(V)$	0.41	0.395	0.372	0.360	0.336
$V_{thp}(V)$	0.365	0.364	0.353	0.349	
S_n (mV/dec)	86.23	84.97	84.19	95.7	97.05
S_p(mV/dec)	96.32	87.62	91.66	92.6	
ΔL_n (μm)			0.01		
ΔL_p (μm)			0.015		
μ_{0n} (cm^2/Vs)			221		
μ_{0p} (cm^2/Vs)			60		

Table 1: Extracted Transistor Conduction Parameters (W=10μm) for n- and p-MOS.

3.2. Results Discussion

The plots of the normalized drain current power spectral density S_{I_D}/I_D^2, and the corresponding $(g_m/I_D)^2$ ratio versus drain current are shown in Fig. 1 and Fig. 2 for n- and p-transistors respectively, working in the ohmic region. Analysis of these plots is considered a generic procedure to distinguish between the 1/f noise mechanisms. As explained by equations (5)-(8), if there is a good correlation of the normalized drain current noise with the corresponding transconductance to drain current ratio squared, the ΔN model dominates, which is clearly the case for our n-transistors. On the other hand, for p-transistors in Fig. 2, a departure from the $(g_m/I_D)^2$ characteristics in strong inversion can be explained by the influence of additional correlated mobility fluctuation. From the S_{I_D}/I_D^2 weak inversion plateau, using the equation (1) and the slope factor value from Table 1, the N_t values are calculated. For both types of devices, the value of N_t is about $3.5 \cdot 10^{17} - 4.5 \cdot 10^{17} (eV^{-1}cm^{-3})$. The value of N_t for n-transistors in strong inversion matches the one for weak inversion.

The input-referred noise power spectral density is plotted in Fig. 3 as a function of the effective gate-source volt-

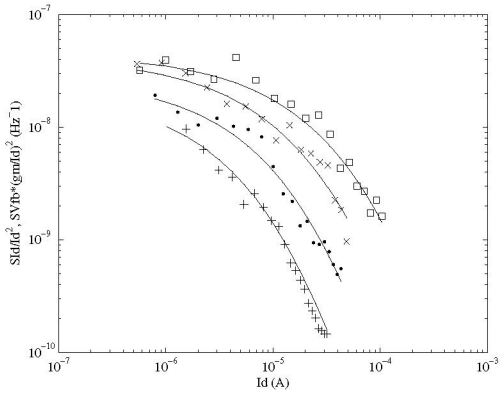

Figure 1: Normalized drain current noise S_{I_d}/I_D^2 and $(g_m/I_D)^2$ ratio of(-) versus drain current for V_{DS}=50mV for NMOS with various transistor lengths. L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

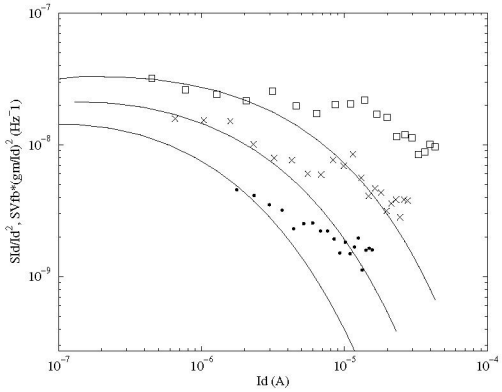

Figure 2: Normalized drain current S_{I_d}/I_D^2 noise and $(g_m/I_D)^2$ ratio (-) versus drain current for V_{DS}=50mV for various PMOS transistor lengths. L=0.26(□), 0.5 (×) and 1 (•) μm.

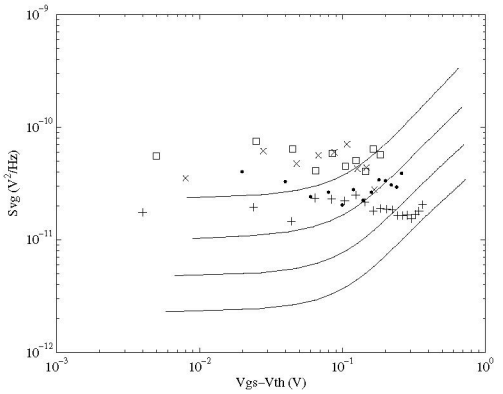

Figure 3: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various NMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

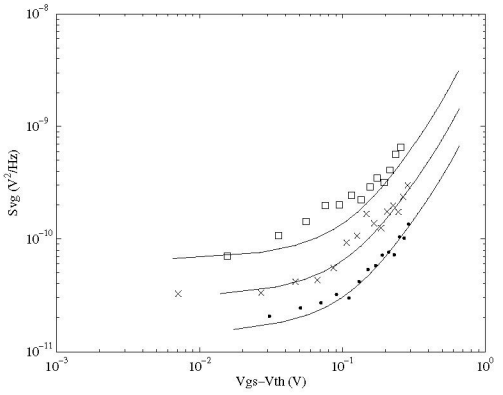

Figure 4: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various PMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×) and 1 (•) (+) μm.

age for n-transistors, and in Fig. 4 for p-transistors (V_{DS} is 50mV). From these figures, the noise origin observed in Fig. 1 and 2 can be confirmed by the fact that the input noise does not depend on V_{GS} for n-channel transistors, while it is proportional to V_{GS}-V_{th} for p-channel transistors as predicted by (2) and (4), respectively. In our experiments, the same origin has been confirmed by the plot of S_{I_D} versus V_{GS}, not shown here. The occasionally observed S_{I_D} dependence on V_{GS} for high overdrive voltages [12], due to the drain and source series resistances can not be observed for the relatively low bias voltages in Fig. 3. The solid lines in Fig. 3 and 4 are the results obtained by BSIM3v3 simulations. It can be seen that the simulator model predicts very well the noise of p-transistors, while discrepancies exist for the n-channel in linear region. The model predicts dependence on the gate bias similar to p-channel bias dependance. This might be due to the fact that for correct modelling when the ΔN model dominates, similarly to α_H, the NOIB parameter should be proportional to $(V_{GS} - V_{th})^{-1}$. Besides that, it can be seen in Fig. 3 that the model provides different value of the flatband voltage, compared to the measured one. The mean value of α_H for p-transistors with different dimensions is about $4.5 \cdot 10^{-4}$. This value is obtained from the measurement data by using a formula similar to (4) with S_{I_D} expressed as a function of I_D, V_{GS} [9] that does not require the measurement of mobility attenuation factor θ. The values of α_s for p-channel transistors, extracted using (9), have values $7.5 \cdot 10^4 - 9.5 \cdot 10^4$ (Vs/C). The values extracted are similar to the the values reported for the same technology node [13].

S_{I_D} versus drain current for V_{DS}=0.45V for various dimensions of p- and n-transistors is shown in Fig. 5 and 6, along with the simulated data. As expected, the drain current spectral density shows a quadratic dependence on the drain current in weak inversion for V_{DS}=450mV as well as for V_{DS}=50mV. As for the transistors working in linear region, measurements for p-channel transistors match very well simulations, while for n-transistors discrepancies are observed. The slope of the curve of S_{I_D} versus

drain current is the same for measured and simulated data in Fig. 5 while the measured values are somehow greater than simulated.

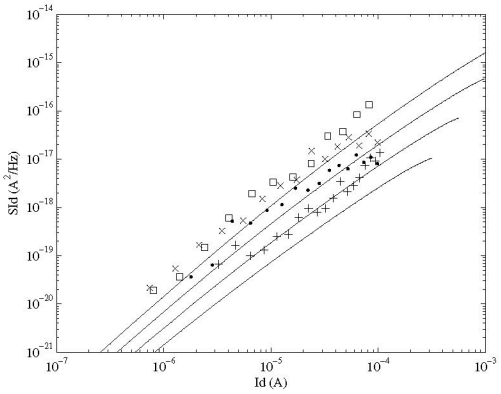

Figure 5: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various NMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

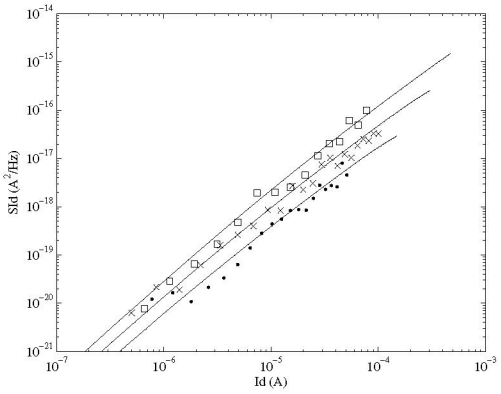

Figure 6: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various PMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×) and 1 (•) μm.

4. Conclusion

In this work, low frequency noise has been investigated on MOS transistors from 0.13μm technology. It has been observed that the noise in n-transistors originates from the number fluctuation theory, while the noise in p-MOS is due to the number fluctuations with correlated mobility fluctuations. Values of the physical parameters extracted match well the values for similar technologies. The simulation result show very good match with the measured data for p-transistors, while some discrepancies for n-transistors are observed.

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