

Millimeter-Wave Integrated Circuit Design for Wireless and Radar Applications

Johansen, Tom Keinicke; Krozer, Viktor; Vidkjær, Jens; Hadziabdic, Dzenan; Djurhuus, Torsten

Published in:
24th Norchip Conference, 2006.

Link to article, DOI:
[10.1109/NORCHP.2006.329222](https://doi.org/10.1109/NORCHP.2006.329222)

Publication date:
2006

Document Version
Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

Citation (APA):
Johansen, T. K., Krozer, V., Vidkjær, J., Hadziabdic, D., & Djurhuus, T. (2006). Millimeter-Wave Integrated Circuit Design for Wireless and Radar Applications. In 24th Norchip Conference, 2006. IEEE. DOI: 10.1109/NORCHP.2006.329222

DTU Library

Technical Information Center of Denmark

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

Millimeter-Wave Integrated Circuit Design for Wireless and Radar Applications

Tom K. Johansen, Viktor Krozer, Jens Vidkjær, Dzenan Hadziabdic and Torsten Djurhuus

Abstract—This paper describes a quadrature voltage-controlled oscillator (QVCO), frequency doubler, and subharmonic mixer (SHM) for a millimeter-wave (mm-wave) front-end implemented in a high-speed InP DHBT technology. The QVCO exhibits large tuning range from 38 to 47.8 GHz with an output power around -15 dBm. The frequency doubler is based on a novel feedback network and demonstrates an output power of -11.5 dBm at an input frequency of 31.4 GHz. The SHM shows a maximum conversion gain at 45 GHz of 10.3 dB with an LO power of only 0 dBm. The mixer is broad-band with more than 7 dB conversion gain from 40-50 GHz. To the authors knowledge the QVCO, frequency doubler, and SHM presents the first mm-wave implementations of these circuits in InP DHBT technology.

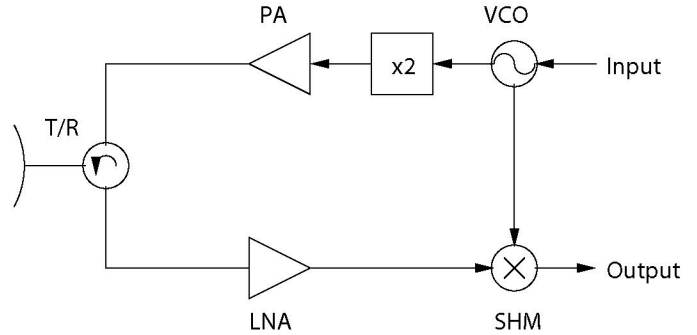


Fig. 1. Simplified block diagram of a millimeter-wave front-end.

I. INTRODUCTION

Millimeter-wave operation in the frequency range around 59 – 86 GHz is particularly interesting for WLAN, automotive, and wireless gigabit networks [1]. The frequencies around 60 GHz exhibit very strong attenuation due to atmospheric losses, whereas the losses at 80-86 GHz are very moderate and communication systems with several kilometers range and gigabit transmission capacity are feasible. An additional advantage is the large (5 GHz) instantaneous allocated frequency band, which allows for very wideband channels. It has also an advantage in microwave imaging in terms of improved resolution and better visibility than the 94 GHz band. A simplified block diagram for a millimeter-wave front-end is illustrated in figure 1. Subharmonic operation is chosen due to the difficulties in providing LO power with high spectral purity at these frequencies.

Traditionally, III-V semiconductor technologies, such as, GaAs pHEMTs have dominated the millimeter-wave market. Recently, a lot of effort have been put on the use of SiGe HBT BiCMOS technology for millimeter-wave applications [2]. SiGe HBT BiCMOS technology is attractive because of its unique potential for large-scale integration and low cost. The main obstacle preventing the widespread use of high-speed SiGe HBTs for millimeter-wave application lies in its very low breakdown voltage (typ. $BV_{ceo} < 1.7V$) giving very low transmit power. Furthermore, there exist difficulties with integration on conductive Silicon substrate at very high frequencies. Emerging technologies like GaAs mHEMT, GaN HEMTs, and InP HBTs can rival the performance of SiGe HBTs but are not yet as cost-effective solutions. These technologies, however, are likely to overcome the bottlenecks

associated with SiGe HBT BiCMOS technology for high-performance millimeter-wave applications.

This paper describes key circuits for a millimeter-wave front-end implemented in a InP DHBT high-speed technology. The front-end circuits are implemented individually as a first step towards a highly integrated solution. While the research goal is to design circuits for a 80-86 GHz wireless gigabit network, frequency down-scaled circuits will be presented due to the lack of available measurement equipment at these frequencies. The applied design techniques remains however, valid in the full mm-wave frequency band (30-100 GHz).

II. TECHNOLOGY

The circuits were fabricated in a high-speed InP/InGaAs DHBT circuit technology developed at the Alcatel-Thales III-V laboratory [3]. By reducing the base thickness the transistors in this technology exhibits $180/210$ GHz f_t/f_{max} and breakdown voltage $BV_{ceo} > 7V$. The technology also offers three Au/Ti metallizations layers, Ti resistors, and SiN metal-insulator-metal (MIM) capacitors.

For accurate circuit simulation several InP DHBT specific modeling issues must be taken into account. First, the forward transit time τ_f and base-collector capacitance C_{bc} experience modulation with bias even in the low current regime. Secondly, the base-collector heterojunction behavior may influence the characteristics in the saturation region. In [4] the authors showed that the Agilent HBT large-signal model accurately predicts the performance of InP DHBT's at mm-wave frequencies.

In mm-wave circuit design transmission lines are used for various purposes such as to form capacitive and inductive stubs needed for matching and bias injection. Due to the lack of backside metallization and via holes in the technology two different approaches can be followed for transmission

The authors are with Oersted•DTU, Section for Electromagnetic Systems, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark. (phone: +45-45253770; e-mail:tkj@oersted.dtu.dk)

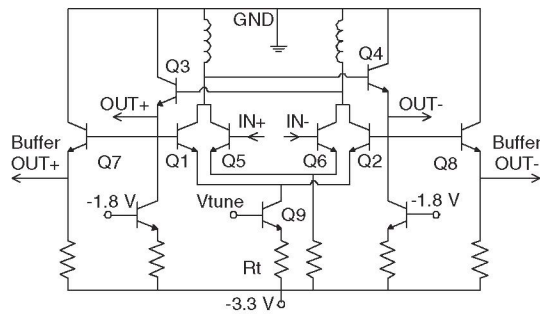


Fig. 2. Schematic of single VCO including coupling- and buffer transistors.

line implementation. The first approach is to use coplanar waveguide (CPW) structures as this facilitates easy shunt and series connection of active and passive components [5]. The second option uses thin-film microstrip lines implemented in the polyimide dielectric between the metallizations layers. The simulation approach followed in the initial design relies on built-in transmission line models from the Agilent ADS¹ simulator adjusted to match the characteristics of 3D Ansoft HFSS² simulations. Critical discontinuities are modeled separately and included in the final design simulation.

III. MMIC FOR MM-WAVE OPERATION

A. Quadrature VCO

By coupling two single differential VCO's in a ring structure 90° phase shift between the differential outputs can be obtained. Figure 2 shows the schematic of a single differential VCO, including the coupling devices and the output buffers. The devices $Q1$ and $Q2$ cross-connected by use of emitter-follower devices $Q3$ and $Q4$, provide the negative resistance needed for oscillation. The frequency tuning is accomplished by varying the tuning voltage V_{tune} which also alters the current through $Q1$ and $Q2$. This changing current affects the coupling strength between the two VCO's leading to resonator de-tuning. A tuning range of more than 20% is possible due to the resonator de-tuning mechanism alone [6]. The simulated phase noise ranges from -84 to -86 dBc/Hz at 1 MHz offset.

A microphotograph of the fabricated QVCO is shown in figure 3. The die size is 1450x1250 μm^2 with pads. To minimize phase errors a highly symmetrical layout have been aimed at. The power and frequency versus tuning range have been obtained with an Agilent E4448A spectrum analyzer. Figure 4 shows the output power for the two VCO's as well as the frequency characteristic versus tuning voltage. The tuning range from 38 to 47.8 GHz corresponds to 22 % bandwidth around 43 GHz. The output power for each VCO is around -15 ± 1 dBm over the tuning range. The observed difference between the two output power curves is believed to be due to asymmetry associated with the measurement setup. The current consumption ranges from 37 to 52 mA. To the authors knowledge the results presents the highest achieved oscillation frequency and largest tuning range for a mm-wave QVCO in any technology.

¹ADS 2004A, Agilent Technol Inc., Palo Alto, CA

²HFSS v.9, Ansoft Corp., San Jose, CA

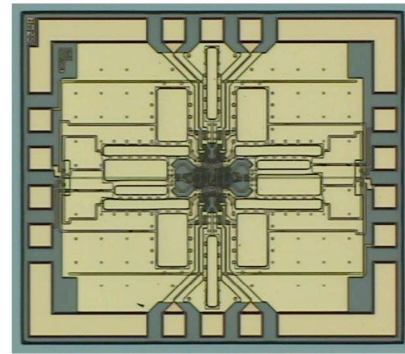


Fig. 3. Microphotograph of the QVCO. (1450x1250 μm^2 with pads).

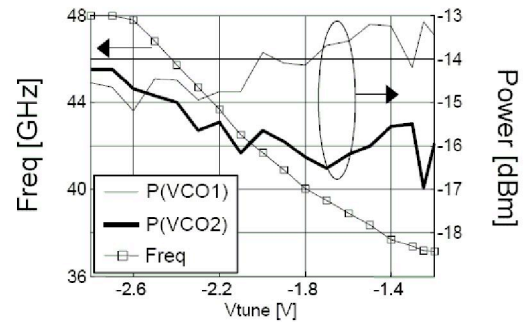


Fig. 4. Single-ended output-power for the individual oscillators in the QVCO and the frequency versus the tuning voltage V_{tune} .

B. Feedback Frequency Doubler

The frequency doubler design is based on a novel second harmonic feedback network. A nonlinear analysis using harmonic-balance technique is performed to estimate the optimum excitation for HBT frequency doubler performance [7]. It turns out to be a signal containing a second harmonic component which must be generated by feeding part of the second harmonic output signal back to the input. This excitation can be derived analytically if a pure sinusoidal excitation is assumed at the internal base-emitter junction. The frequency doubler including the novel second harmonic feedback network is shown in Fig. 5. The parallel tuned circuit assures maximum isolation between input and output of $Q1$ for the fundamental frequency signal and presents a pure reactance at the second harmonic. This reactance forms a voltage divider together with the input matching network at the second harmonic.

The microphotograph of the fabricated frequency doubler is shown in figure 6. The die size including pads is 1450x1250 μm^2 . The transmission lines have been implemented as coplanar wave guides (CPW's). Preliminary on-wafer measurements have been performed on the fabricated circuit. The frequency doubler where originally designed to operate around an input frequency of 41.75 GHz. However, due to changes in the layer stack and unaccounted parasitics in the second harmonic feedback network a shift towards lower frequencies were observed. Despite these facts the benefits of the second harmonic feedback network is evident in the output power versus control

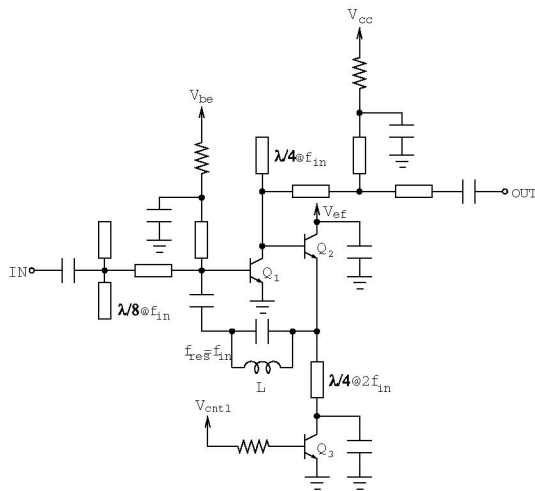


Fig. 5. Schematic of frequency doubler including second harmonic feedback network.

voltage shown in Fig. 7. In this figure a rise in output power of 2.5 dB at an input frequency of 31.4 GHz is observed when the second harmonic feedback network is active. For a properly operating HBT frequency doubler the expected increase in output power is more than 6 dB.

C. Sub-Harmonic Mixer

The sub-harmonic mixer necessary to down-convert the double frequency signal using fundamental frequency oscillator has been designed in the same process. The topology consists of an LO frequency doubler, RF pre-amplifier, and single-ended mixer integrated into a single subharmonic mixer as shown in figure 8. The single-ended mixer consists of the device Q_3 , the $\lambda/4@2f_{LO}$ short-circuited line, and the IF matching circuit. The IF matching circuit assures that unwanted mixing products at the output are shorted to ground. The frequency doubler should convert the externally applied LO excitation at f_{LO} into a $2f_{LO}$ frequency signal with sufficient amplitude to drive the single-ended mixer. The frequency doubler design is based on reactive termination at the second harmonic at the input side of device Q_2 and short circuit termination at the fundamental at the output side. The

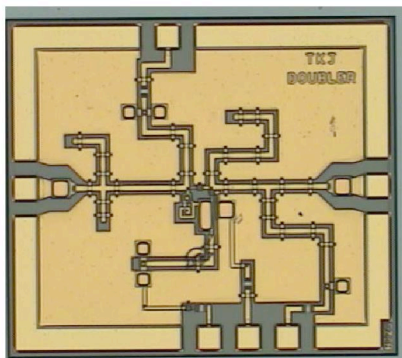


Fig. 6. Microphotograph of the feedback frequency doubler. ($1450 \times 1250 \mu m^2$ with pads).

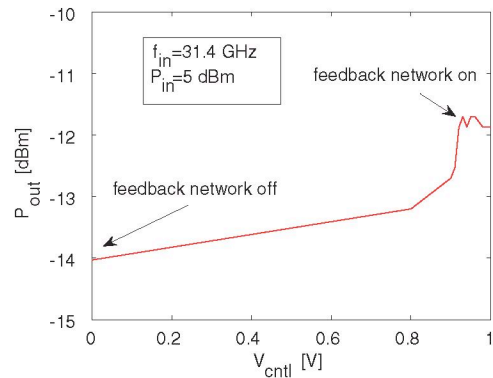


Fig. 7. Second harmonic output power versus control voltage (V_{ctrl}).

second harmonic reactive termination implemented with the $\alpha\lambda@f_{LO}$ shorted line in figure 8 increases the conversion gain of the frequency doubler for a certain range of α values [8]. The RF pre-amplifier is included to separate the output of the frequency doubler from the RF input and reduce the noise contribution from the single-ended mixer.

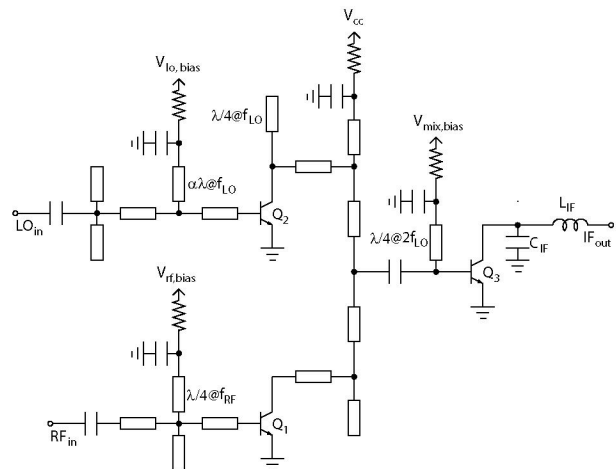


Fig. 8. Schematic of the subharmonic mixer circuit.

The microphotograph of the fabricated SHM is shown in figure 9. The die size including pads is $1450 \times 1250 \mu m^2$. Similar to the frequency doubler the transmission lines have again been implemented as CPW structures. Figure 10 shows the measured conversion gain versus the RF frequency, with a constant IF frequency of 2.5 GHz. A maximum conversion gain of 10.3 dB is achieved at an RF frequency of 45 GHz with an LO power of only 0.3 dBm. In the range between 40 – 50 GHz the conversion gain is larger than 7 dB with a small variation of around ± 1.5 dB over the overall frequency range. The SHM can be operated over even wider bands, but then with a compromise in conversion gain, as indicated in figure 10. The parasitic mixer output signal at $f_{IF} = f_{LO} - f_{RF}$ is also included in the figure and is at least 24 dB below the desired signal at the IF output. In general the measured performance of the SHM is very well predicted by simulations validating our large-signal modeling and EM simulation approaches. The

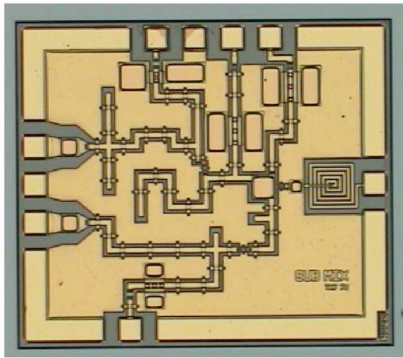


Fig. 9. Microphotograph of the subharmonic mixer ($1450 \times 1250 \mu\text{m}^2$ with pads).

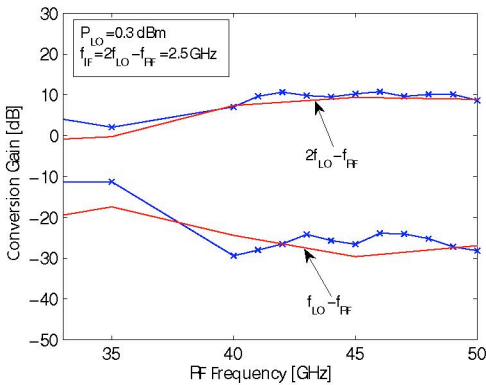


Fig. 10. Measured (symbols) and simulated (solid line) Q-band conversion gain for the sub-harmonic $2f_{LO} - f_{RF}$ and fundamental $f_{LO} - f_{RF}$ mixing product. The IF for the sub-harmonic mixer is $f_{IF} = 2.5$ GHz.

performance of the SHM is believed to be better with regards to conversion gain and LO power level than other mm-wave SHM published earlier.

IV. CONCLUSION

This paper have demonstrated key circuits for a millimeter-wave front-end implemented in a high-speed InP DHBT technology. A QVCO with a record high frequency of oscillation of 47.8 GHz and 22 % tuning range have been successfully fabricated. A frequency doubler demonstrated an 2.5 dB increase in the output power at an input frequency of 31.4 GHz due to a novel second harmonic feedback network. Finally, a SHM with more than 7 dB conversion gain over a large band from 40–50 GHz and very low LO power requirements have been demonstrated.

ACKNOWLEDGMENT

The authors wish to acknowledge Agnieszka Konczykowska, Muriel Riet, and Filipe Jorge at the Alcatel-Thales III-V laboratory, Marcoussis, France, for chip fabrication, discussions, and measurement assistance.

REFERENCES

[1] L. E. Larson. SiGe HBT BiCMOS Technology as an Enabler for Next Generation Communications Systems. In *2004 European Gallium Arsenide and other Compound Semiconductors Application Symposium*, pages 251–254, 2004.

[2] A. Joseph et al. SiGe HBT BiCMOS technology for millimeter-wave applications. *Phys. stat. sol.*, 3(No. 3):448–451, 2006.

[3] S. Blayac et al. MSI InP/InGaAs DHBT technology: beyond 40 Gbit/s circuits. In *14th Indium Phosphide and Related Materials Conference*, pages 51–54, 2002.

[4] T. K. Johansen et al. Large-signal modeling of high-speed InP DHBTs using electromagnetic simulation based de-embedding. In *2006 IEEE MTT-s Digest*, pages 655–658, june 2006.

[5] R. N. Simons. *Coplanar Waveguide Circuits, Components, and Systems*. John Wiley & Sons, Inc., 2001.

[6] D. Hadziabdic et al. A 47.8 GHz InP HBT quadrature VCO with 22 % tuning range. *Electronic Letters*. submitted for publication.

[7] T. K. Johansen et al. A novel HBT frequency doubler design for millimeter-wave applications. In *Proc. INMMIC 2006*, pages 106–109, Jan. 2006.

[8] T. K. Johansen et al. A High Conversion-Gain Q-band InP DHBT Sub-Harmonic Mixer. *IEEE Trans. Microwave Theory and Tech.* submitted for publication.