2.5 Gb/s laser-driver GaAS IC

Riishøj, Jesper

Published in:
Journal of Lightwave Technology

Link to article, DOI:
10.1109/50.238073

Publication date:
1993

Document Version
Publisher's PDF, also known as Version of record

2.5 Gb/s Laser-Driver GaAs IC

Jesper Riishøj

Abstract— **A laser-diode driver GaAs IC incorporating an optional NRZ/RZ conversion facility, having ECL and SCFL compatible inputs and providing a 0–60 mA adjustable output current into a 50 Ω/5V termination at bit rates up to 2 Gb/s NRZ and maintaining a clear eye opening of 50 mA at 2.5 Gb/s NRZ bit rate has been designed using a commercial 1 μm gate length (F_T = 12 GHz) GaAs MESFET foundry service. The high maximum output current is obtained despite a low drain-to-gate breakdown voltage by implementing the output driver as a cascode differential amplifier. The logic circuitry incorporating two data input buffers, a clock input buffer, a retiming MS-DFF, a NRZ/RZ-converter and a 2-bit selector is implemented using a novel SCFL family, DCAL type SCFL, which is based on gate-width scaling rather than on absolute values. As a result, the on-chip logic voltage swing is less sensitive to process variations than conventional SCFL. A 60% improvement in noise margin over that of conventional SCFL is also obtained. Finally, in order to verify laser driving performance a back-to-back optical-fiber transmission experiment using a Siemens DFB laser was performed giving good optical eye diagrams at 2.5 Gb/s. Further, the electro/optical interplay between laser-diode driver and laser-diode has been demonstrated using SPICE simulations employing a large-signal model of an Ortel SL-620 laser-diode module.**

I. Introduction

PRESENTLY, optical-fiber communication systems operating at gigabit per second data-rates are becoming of increasing interest for large-capacity communication systems and high-speed local area networks. In such systems a laser-diode driver is one of the key components in the transmitter, where it performs the interface between high-speed electronics and the laser-diode. Today, several laser-drivers operating above 10 Gb/s have been published [1], [2]. Common for these ultra fast devices are the modest circuit complexity. In this work we have focused on designing a more general purpose laser-driver resulting in much greater circuit complexity though at a much lower speed. At the input the laser-diode driver interfaces to gigabit electronics for which ECL levels (−0.8 V/−1.8 V) and SCFL levels (0 V, −1 V) are the most widely accepted I/O levels [3]. At the output the laser-diode driver interfaces to a laser-diode, and by making the modulation current adjustable in the 0–60 mA range most commercially available laser-diodes capable of operating at gigabit per second bit rates can be modulated to utilise the maximum available optical ON/OFF ratio. The wavelength of the laser-diode light output is well known to be temperature sensitive. Thus the pattern dependent heating caused by a NRZ data stream can cause wavelength chirp. This kind of chirp can be reduced by using a RZ data format instead of NRZ data format [4] though at the expense of a wider bandwidth requirement for the same data rate. Thus an optional NRZ/RZ conversion facility is incorporated on the laser-diode driver GaAs IC. The retiming process between data and clock, which is necessitated by the NRZ/RZ conversion option, will limit the maximum frequency of operation unnecessarily in situations, where we do not want RZ modulation, or where time jitter of the incoming signal is of little concern. Therefore a second data path bypassing the D-flip-flop is generated through a second data input buffer, data buffer 2, and a 2-bit selector. Summing up the above discussion, we end up with the chip block diagram shown in Fig. 1.

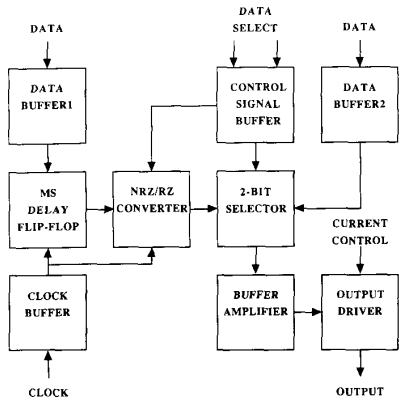


Fig. 1. Block diagram of laser-diode driver GaAs IC.

II. DCAL Type SCFL

Most published laser-diode drivers, though not all, are very simple, incorporating an output driver and buffering circuitry for interfacing to surrounding electronics. The present laser-diode driver, however, incorporates some simple digital functions, and thus a suitable logic family has to be chosen. Since the modulation current is to be adjustable, the output driver will be implemented as a differential amplifier. Therefore, source-coupled FET logic (SCFL) is an obvious choice.

During the last decade or so, many different logic families have been presented due to their superior performance in a certain sense. Of these different families, SCFL is well accepted to be one of the best choices when aiming for high-speed operation though at the expense of high power dissipation. SCFL has been seen in many variants depending on the

Manuscript received December 6, 1991; revised December 25, 1992. This work was supported by the Danish Council for Technology and the Danish Technical Research Council.

The authors are with the Center for Broadband Telecommunications, Electromagnetics Institute, Technical University of Denmark, DK 2800 Lyngby.

IEEE Log Number 9209875.

TABLE I
COMPARISON OF SIMULATED VARIATIONS IN INTERNAL LOGIC VOLTAGE SWINGS IN PERCENTAGE OF THE NOMINAL SWING AT 20°C OVER PROCESS VARIATIONS AND TEMPERATURE (27 – 80°C) BETWEEN DCAL TYPE SCFL AND RL TYPE SCFL

	ΔV_{HIGH}/%	ΔV_{LOW}/%
DCAL SCFL	+11	-14
RL SCFL	+72	-41

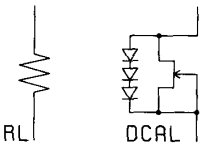


Fig. 2. Simple resistive load (RL) and diode clamped active load (DCAL).

specific application [5]–[7], but to the best of the author's knowledge, all suggested SCFL topologies employ simple resistive loads (RL type SCFL) in the differential amplifier. That approach, however, suffers from large variations in the logic voltage swing over process variations. To address this problem one could think of using active loads. It does not make sense to simply adopt simple active loads as seen in, e.g., buffered FET logic (BFL) since the differential amplifier switching FET's would then be forced way into triode operation giving poor high frequency operation. True differential operation could also be lost if the switch transistor gate-to-source diodes were driven into forward conduction. Instead we propose the use of diode-clamped active loads (DCAL's) see Fig. 2, thus suggesting DCAL type SCFL. SPICE simulation of circuit performance variation as function of process spread is enabled by the GaAs manufacturer for PCM qualified wafers through a number of worst-case model parameter sets. Thus using SPICE simulations we have found DCAL type SCFL to generate a logic voltage swing being less sensitive to process variations than experienced using resistive loads in conjunction with uncompensated current sources, see Table I. DCAL type SCFL also exhibits a substantial improvement in noise margin over that of its RL type SCFL counterpart as shown in Fig. 3(a)–(d). Thus a 60% improvement of the maximum square noise margin [8] has been obtained. The noise margin improvement can be explained by using the load lines corresponding to a RL type and a DCAL type SCFL inverter, see Fig. 4. It is clear from Fig. 4, that DCAL type SCFL is much more robust than RL type SCFL, since the load impedance in the logic voltage extremes is determined by the clamping diodes and the active load linear drain-to-source resistance at logic low and high, respectively, while the load impedance for RL type SCFL is of course equal to the value of the resistive load.

The widths of the load transistor and the three clamping diodes in the employed DCAL's have through SPICE simulations been determined to 60 and 40%, respectively, of the width of the current source to give maximum noise margin while still maintaining a comfortable margin to the maximum allowable diode current density. Finally, two additional level shifting diodes are put in between the positive voltage supply V_{DD} and the DCAL's in order to keep the input source

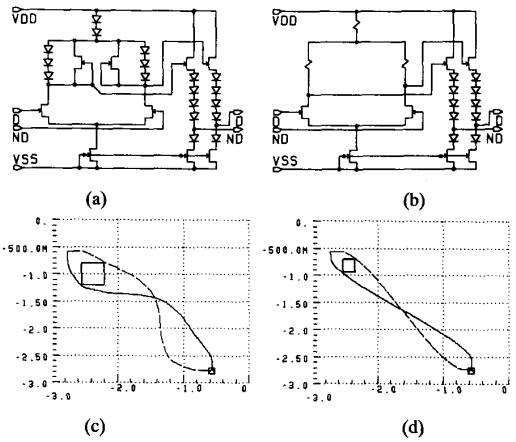


Fig. 3. Schematic circuit diagram of (a) DCAL type SCFL inverter and (b) of RL type SCFL inverter. Determination of maximum square noise margin for (c) DCAL type SCFL, and (d) for RL type SCFL.

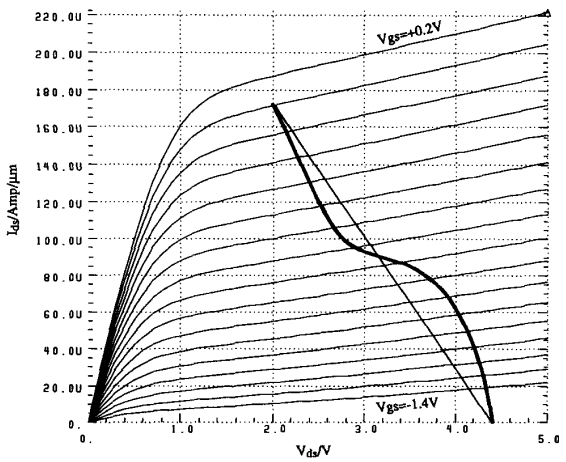


Fig. 4. Load line (bold) for DCAL type and (narrow) for RL type SCFL inverter.

follower FET's in saturation, even during logic high, thus maintaining good source follower drive capacity for the whole logic swing. The rest of the basic SCFL circuit design is similar to that of conventional SCFL.

DCAL-type SCFL uses more components than its RL type SCFL counterpart and may also be more prone to back-gating depending of course on the resistor type used in the RL type SCFL. Therefore DCAL type SCFL may not be as well suited for very high levels of integration as RL type SCFL. By applying compensated current sources based on a thorough knowledge to process parameter values and spreads process-insensitive RL type SCFL operation can also be obtained. The control voltage needed for process compensation would then have to be routed to all gates adding to the total circuit complexity and area consumption. In conclusion, DCAL-type SCFL is proposed as a complement to existing SCFL families being a simple and efficient mean to improve noise margin and to stabilise performance over process variations without adding considerably to the total circuit complexity.

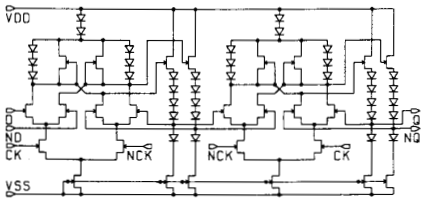


Fig. 5. Schematic circuit diagram of DCAL type SCFL MS D-Flip-Flop.

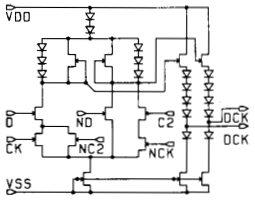


Fig. 6. Schematic circuit diagram of DCAL type SCFL NRZ/RZ converter.

III. Circuit Design

A. Input Buffers

All incoming signals except for the output current control are buffered by simple DCAL type SCFL inverters accepting and modified to be fully switched by ECL and SCFL logic levels. Thus off-chip logic levels are amplified and buffered by the input buffers to fit on-chip logic levels.

B. Flip-Flop Circuit

In order to get reliable NRZ/RZ conversion data is re-timed to the clock by using the dual clocked Master-Slave D-Flip-Flop shown in Fig. 5. The clock and its complementary signal are applied to terminals CK and NCK, respectively, via the clock input buffer. The data signal and its complementary signal are applied to terminals D and ND, respectively, via data buffer 1. The Flip-Flop output and its complementary signal are present at terminals Q and NQ, respectively.

C. NRZ/RZ Converter

A circuit diagram of the NRZ/RZ converter is shown in Fig. 6. The clock and its complementary signal are applied to terminals CK and NCK, respectively, via the clock input buffer, and the output data signal from the D-Flip-Flop are applied at terminals D and ND, respectively. The control signal determining whether NRZ/RZ conversion will take place and its complementary signal are applied to terminals C2 and NC2, respectively, via the control signal input buffer. C2 being low will disable the NRZ/RZ conversion process and simply make the converter act as an inverter passing the retimed NRZ signal from the D-Flip-Flop, while C2 high will enable the NRZ/RZ conversion process.

D. 2-Bit Selector

The process of passing a NRZ signal through the D-Flip-Flop is limited by the maximum operating frequency of the D-Flop-Flop, that is the clock frequency. Thus in order to support simple NRZ modulation where the improved pulse fidelity gained through retiming is not necessary a second data path is set up via data buffer 2. One of the two data paths can then be selected using the 2-bit selector shown in Fig. 7. The output signal and its complementary signal from the NRZ/RZ converter are applied to terminals D1 and ND1, respectively, and the data signal and its complementary signal are applied to D2 and ND2, respectively, via data buffer 2. The control signal selecting between D1or D2 and its complementary signal are applied to terminals C1 and NC1, respectively, via the control signal input buffer. C1 being high or low selects D1 or D2 to be passed to the 2-bit selector output, respectively.

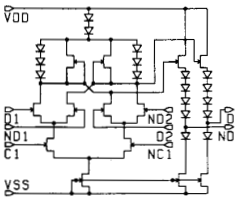


Fig. 7. Schematic circuit diagram of DCAL type SCFL 2-b selector.

IV. Output Driver

The requirement of an adjustable modulation current makes a differential amplifier type output driver an obvious choice, and as a result this type of driver is widely used [9], [10]. The input impedance of most commercially available laser-diode modules intended for gigabit per second modulation is tuned towards $50\,\Omega$, which in conjunction with the often high modulation current will result in a large voltage swing at the drain contact of the switching FET's. Therefore the drain-to-gate breakdown voltage BV_{dg} is an important parameter for design of differential amplifier type laser-diode drivers. In a digital process the drain-to-gate breakdown voltage will be low typically in the order of 4–6 V, since BV_{dg} is of secondary concern when operating at voltage supply levels of, e.g., 2 V. In an analog process BV_{dg} will typically be high, while the integration level is low. Thus the drain-to-gate breakdown voltage must be given special consideration when implementing logic functions and a differential amplifier type output driver on the same chip.

For the simple differential amplifier type output driver, shown in Fig. 8, the maximum allowable drain-to-gate voltage limitation can be expressed as

$$V_{dg1,\,\mathrm{high}} = \Delta V_{d1} + \Delta V_{g1} + V_{dg1,\,\mathrm{low}} < BV_{dg1} \qquad (1)$$

where ΔV_{d1} and ΔV_{g1} are the logic voltage swings at the switching FET Q1 drain and gate terminals, respectively, and $V_{dg1,\,\mathrm{low}}$ is the minimum drain-to-gate voltage occurring for the whole modulation current flowing in Q1. In order to prevent the switching FET's from entering poor F_τ biasing a minimum value $V_{dg1,\,\mathrm{min}}$ of $V_{dg1,\,\mathrm{low}}$ is defined as $V_{dg1,\,\mathrm{min}} = V_{dg1,\,\mathrm{sat}}$ representing the somewhat soft transition between triode and saturated operation. Equation (1) expresses the noise margin to the breakdown voltage. By rearranging (1) and employing the simple relationship $\Delta V_d = R_L I_{\mathrm{mod}}$, where R_L

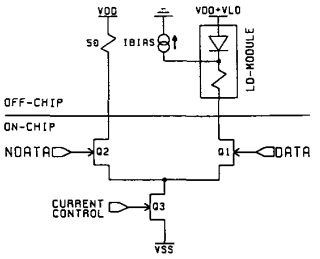


Fig. 8. Simple differential amplifier type output driver.

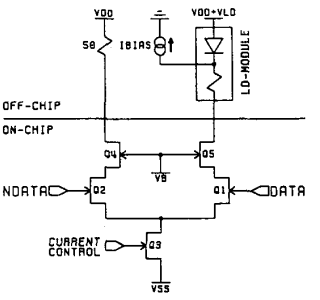


Fig. 9. Cascode differential amplifier type output driver.

is the load impedance and I_{mod} the modulation current peak-peak amplitude, the maximum allowable current amplitude for a given drain-to-gate breakdown voltage for the simple differential amplifier type output driver becomes:

$$I_{\mathrm{mod}} < \frac{BV_{dg1} - V_{dg1,\,\mathrm{sat}} - \Delta V_{g1}}{R_L}. \tag{2}$$

As a numerical illustration of the maximum obtainable modulation current amplitude using (2) let us assume identical switch and current source transistor gate widths and $R_L = 50\,\Omega$. For the present process the values of threshold voltage $V_T = -1.7$ V, $V_{dg,\,\mathrm{sat}}(V_{gs} = 0\ \mathrm{V}) = 1.3$ V and $BV_{dg} = 6$ V are representative thus limiting the maximum modulation current amplitude to $I_{\mathrm{mod}} < 60$ mA.

In order to increase the maximum allowable modulation current for a given drain-to-gate breakdown voltage while still maintaining the advantages of differential operation we propose the use of a cascode differential amplifier type output driver as shown in Fig. 9. For that configuration the maximum allowable drain-to-gate voltage limitation can be expressed as

$$\begin{aligned} V_{dg1,\,\mathrm{high}} &= 2\Delta V_{g1} + V_{dg1,\,\mathrm{low}} < BV_{dg1} \\ V_{dg5,\,\mathrm{high}} &= V_{DD} - V_B < BV_{dg5} \end{aligned} \tag{3}$$

where V_{DD} is the load impedance termination voltage, and V_B is a bias voltage. From (3) we see, that $V_{dg1,\,\mathrm{high}}$ now is independent of I_{mod}, and an increase in margin to BV_{dg1} of $R_L I_{\mathrm{mod}} - \Delta V_g$ is obtained. By applying:

$$V_{dg5,\,\mathrm{low}} = V_{DD} - R_L I_{\mathrm{mod}} - V_B > V_{dg5,\,\mathrm{sat}} \tag{4}$$

and inserting (4) into (3) the maximum allowable modulation current amplitude for a given drain-to-gate breakdown voltage for the cascode differential amplifier type output driver, shown in Fig. 9, becomes:

$$I_{\mathrm{mod}} < \frac{BV_{dg5} - V_{dg5,\,\mathrm{sat}}}{R_L}. \tag{5}$$

A comparison of (2) and (5) shows an increase in the maximum allowable modulation current amplitude of $\Delta V_g/R_L$ when employing the cascode instead of the simple differential amplifier type output driver. Thus continuing the above shown numerical example this corresponds to $\Delta V_g/R_L = 34$ mA. Smaller modulation currents will of course translate into equivalent margin to BV_{dg5}.

V. Semiconductor Laser-Diode Large-Signal Model

Circuit simulations is a well known tool used to predict performance of a given electrical circuit. However, in the case of designing a laser driver IC we also need to model the optical output from the modulated laser diode in order to evaluate the performance of the laser-driver IC. Therefore we will next develop a large-signal model for an intrinsic semiconductor laser diode, that can "easily" be implemented in a conventional circuit analysis program such as SPICE. In that manner package and chip parasitic components can easily be incorporated. It should be mentioned, that in the absence of suitable in-house measured data we have used elsewhere published data for an Ortel SL-620 laser diode [11] as being representative of laser-diodes capable of operating at gigabit per second bit rates. A suitable model for the intrinsic laser diode has been developed by Tucker [12], [13]. Tucker's large-signal model, is based on the single-mode rate equations including the effect of gain compression through ϵ:

$$\frac{dN}{dt} = \frac{I_a}{qv} - \frac{N}{\tau_n} - g_o(N - N_{om})(1 - \epsilon S)S \tag{6}$$

$$\frac{dS}{dt} = \Gamma g_o(N - N_{om})(1 - \epsilon S)S - \frac{S}{\tau_p} + \Gamma\beta\frac{N}{\tau_n} \tag{7}$$

where N is the carrier density, N_{om} is the carrier density for transparency, I_a is the current injected into the active region, v is the volume of the active region, q is the electronic charge, S is the photon density averaged over the modal volume v/Γ in a mode of the active region, Γ is the confinement factor, g_o is the optical gain coefficient, τ_n is the spontaneous recombination lifetime of the carriers, τ_p is the photon lifetime, and β is the fraction of spontaneous emission entering the lasing mode. The parameter ϵ defines the gain compression characteristics of the active region. The spontaneous recombination current is now defined as $I_{sp} = qvN/\tau_n$, and after some rearranging the rate equations can be expressed in the following convenient form corresponding to the equivalent circuit diagram shown in Fig. 10:

$$I_a = I_{sp} + \tau_n\frac{dI_{sp}}{dt} + G(I_{sp} - I_{om})(1 - \epsilon' S')S' \tag{8}$$

$$C_{ph}\frac{dS'}{dt} + \frac{S'}{R_{ph}} = \beta I_{sp} + G(I_{sp} - I_{om})(1 - \epsilon' S')S' \tag{9}$$

where $C_{ph} = qvS_n, R_{ph} = \tau_p/(S_n qv), G = \Gamma g_o S_n \tau_n, I_{om} = qvN_{om}/\tau_n$, and $\epsilon' = \epsilon\Gamma S_n$. $S' = S/(\Gamma S_n)$ is a normalization constant introduced to avoid divergences during numerical evaluation, and the term $G(I_{sp} - I_{om})(1 - \epsilon' S')S'$ is equivalent to the current generator I_{stim} in Fig. 10. One of the characteristic properties of a semiconductor laser-diode that can directly be derived from the rate equations is the threshold current I_{th} defining the lower current limit for light emission. Thus a good approximation of I_{th} can be found from (9) by assuming static conditions and neglecting ϵ. We get:

$$S' = \frac{\beta I_{sp}}{G(I_{sp} - I_{om}) - 1/R_{ph}}. \tag{10}$$

When the laser bias current is increased above threshold, the electron concentration in the active region will saturate corresponding to a $I_{sp,\,\text{sat}}$, while the photon concentration will continue to increase. Thus by assuming $I_{\text{th}} \approx I_{sp,\,\text{sat}}$ and $G(I_{sp} - I_{om}) - 1/R_{ph} = 0$ we get:

$$I_{th} \approx I_{om} + 1/R_{ph}G \tag{11}$$

The relationship between the junction voltage V_j and the spontaneous recombination current I_{sp} is modeled using an ideal diode:

$$I_{sp} = I_s[\exp(qV_j/\eta kT) - 1] \tag{12}$$

where $\eta = 2$ and $I_s = qv \cdot 4.55 \cdot 10^{24}$A. In Table II is shown device parameters for an Ortel SL-620 laser diode [11]. Choosing $S_n = 10^{20}$, we get:

$$\begin{aligned} C_{ph} &= 1.44\,\text{fF} \\ R_{ph} &= 1.39\,\text{k}\Omega \\ G &= 0.24 \\ I_{om} &= 17.81\,\text{mA} \\ \epsilon' &= 2.46 \cdot 10^{-3}\,\text{m}^3 \\ I_s &= 65.52\,\text{pA} \\ I_{\text{th}} &= 20.8\,\text{mA}. \end{aligned}$$

Please note the resemblance between the experimentally determined threshold current in Table II and the one calculated from (11). Finally, to complete the laser-diode large-signal model package and chip parasitic components have been identified and modeled [11] as shown in Fig. 11, and thus the electro/optical function of the laser-diode module can now be predicted using a conventional circuit analysis program.

VI. Simulated Interaction Between Laser-Diode Driver and Laser-Diode

In this section, we will use SPICE simulations to investigate the laser-diode driver drive capacity when driving a 50 Ω laser-diode module (Ortel SL-620). In order to obtain maximum optical on/off ratio for the lowest possible modulation current amplitude, weak relaxation oscillation and wide bandwidth the laser-diode current is usually switched between a value just below threshold I_{th} (no light) and a value close to the maximum allowable diode current $I_{\text{diode, max}}$ (maximum light output) often given in terms of I_{th}.

TABLE II
Device Parameters of Intrinsic Ortel SL-620 Laser Diode

Parameters	Description	Values	Unit
I_{th}	Threshold current	21	mA
F_τ	Small-signal relaxation frequency	2.0 (at $1.25I_{th}$) 4.0 (at $1.75I_{th}$) 5.5 (at $2.25I_{th}$)	GHz
λ	lasing wave length	835	nm
qv	q×(volume of active region)	$1.44 \cdot 10^{-35}$	m^3C
τ_p	life time of photon	2	ps
τ_n	life time of electron	3.72	ns
N_{om}	electron density for transparency	$4.6 \cdot 10^{24}$	m^{-3}
g_o	optical gain proportional constant	$1.0 \cdot 10^{-12}$	$s^{-1} \cdot m^3$
Γ	optical confinement factor	0.646	-
β	spontaneous emission to lasing mode coupling probability	0.001	-
ε	gain compression parameter	$3.8 \cdot 10^{-23}$	m^3

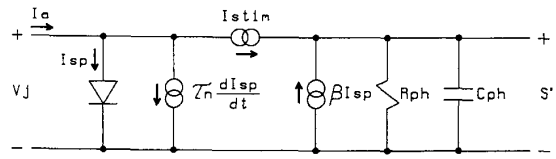


Fig. 10. Large-signal circuit model of intrinsic semiconductor laser-diode.

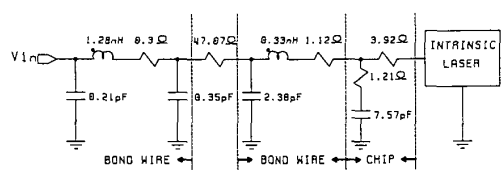


Fig. 11. Package and chip parasitics of Ortel SL-620 laser-diode module.

Differential amplifier type laser-diode drivers are ideal for ON/OFF switching a current but are not suited for generating the desired subthreshold standby current flowing in the off-state laser diode. Consequently additional dc biasing circuitry like a current source and a bias-T is needed. Instead, we suggest to use the drive setup shown in Fig. 12, where the standby current flowing into the OFF-state laser diode is easily generated. Furthermore, the laser diode is actively turned-OFF in this configuration aiding in levelling out differences between rise and fall times of the light output, since turnoff (fall time), or equivalent removal of carriers from the active region, being governed by the carrier life time is a slow process compared to turn-ON (rise time), which is governed by the relaxation oscillation being a very fast process. Finally, in many applications the laser-diode module can not be placed in direct vicinity of the driver. Due to the difficulties of obtaining a good broadband match to a laser-diode the high output impedance of the open-drain outputs may consequently cause ringing. Using the above suggested setup approximate matching can be obtained in both ends of the transmission line connecting laser-diode and driver thus greatly reducing multiple reflections.

As a circuit simulation example of the laser-driver GaAs IC capacity to drive the above described Ortel laser-diode module let us use a modulation current amplitude of $I_{\text{mod}} = 30$ mA

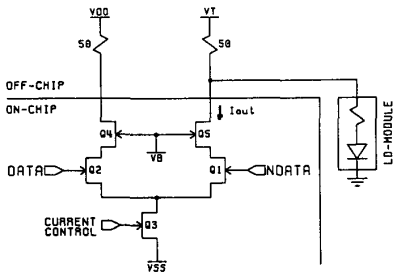
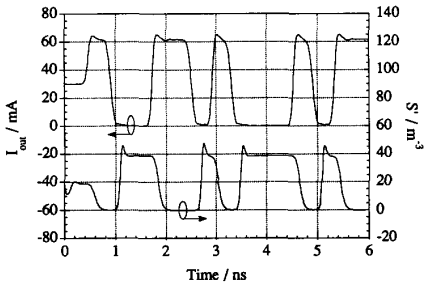


Fig. 12. Circuit diagram used for the combined simulation of laser driver IC and laser-diode.



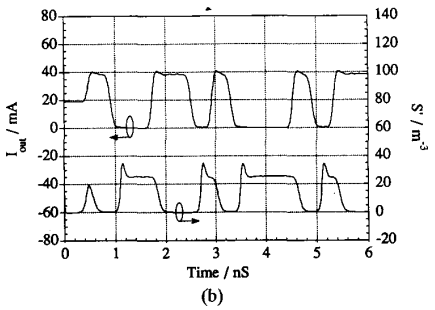


Fig. 13. Simulated laser-driver output current I_{out} and corresponding laser-diode normalized photon concentration S' obtained when applying the differential 2.5 Gb/s NRZ ECL bit sequence 01100101110100 to data input buffer 2 for (a) $V_T = 6.05$ V and (b) $V_T = 5$ V.

in conjunction with a bias current of $I_{\text{bias}} = 20$ mA $< I_{th}$ giving $I_{\text{bias}} + I_{\text{mod}} = 50$ mA $\approx I_{\text{diode, max}} = 2.5 I_{th} = 52$ mA. By then applying the driver configuration shown in Fig. 12 the laser-diode driver output current I_{out} and the corresponding normalized photon concentration $S' = S/\Gamma S_n$ of the laser-diode shown in Fig. 13(a) are obtained through SPICE simulations for the differential 2.5 Gb/s NRZ formatted ECL bit-stream 01100101110100 applied to data buffer 2.

We note that an additional power-supply ($V_T = 6.05$ V) is necessary for obtaining maximum optical ON/ OFF-ratio for the applied laser-diode and impedance level. However, in practice it is often desirable to minimize the number of power-supplies, and in that case one could use the existing positive power supply $V_{\text{DD}} = +5$ V. Performing the same simulation experiment as described above but for $V_T = 5$ V while still maintaining $I_{\text{bias}} = 20$ mA we get the laser-diode

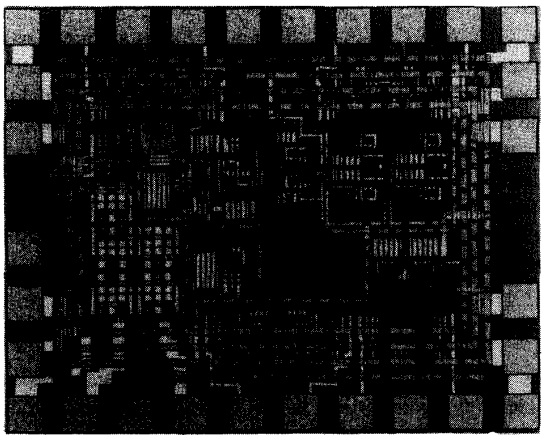


Fig. 14. Photograph of laser-diode driver GaAs MIC.

driver output current I_{out} and corresponding normalized laser-diode photon concentration $S' = S/\Gamma S_n$ responses shown in Fig. 13(b). Comparing Fig. 13(a) and (b) we notice, that approximately one third of the photon concentration is lost when decreasing V_T from $V_T = 6.05$ V to $V_T = 5$ V corresponding to a similar decrease in transmission distance. We also notice a stronger relaxation oscillation resulting in higher sensitivity to dispersion and more complicated filtering in the receiver. On the positive side, the transition times are shorter owing to the reduced modulation current amplitude.

VII. Fabrication

The laser driver IC was fabricated as being part of a multiproject chip (MPC) run using the Tri-Quint Semiconductor foundry service. In total, it incorporates 130 1 μm gate length GaAs MESFET's ranging in size from 5 to 400 μm, 180 n^+-diodes and 16 implanted resistors. A photograph of the fabricated laser-diode driver GaAs MIC (monolithic integrated circuit) is shown in Fig. 14.

VIII. Measured Performance

A. Electrical Measurements

The laser-diode driver GaAs IC's were bonded to thick-film alumina substrates. A photograph of the applied test hybrid integrated circuit (HIC) is shown in Fig. 15. Power supplies are decoupled using chip capacitors, and incoming signal lines are terminated through 50 Ω thick-film resistors. Rise and fall times and output pulse waveforms were measured using a 5 Gb/s Anritsu pulse-pattern generator and an HP 4-channel sampling oscilloscope floating at $V_{\text{DD}} = +5$ V thus generating the desired $50\,\Omega/+5$ V terminations. Therefore, outside only DC-blocks were inserted in the signal paths between sampling head and test HIC, and a both inside and outside DC-block was inserted in the trigger signal path to separate the pulse-pattern generator and oscilloscope chassis from each other.

Current eye diagrams for a modulation current amplitude of 60 mA for bit rates of 1.0 and 2.5 Gb/s using NRZ data format

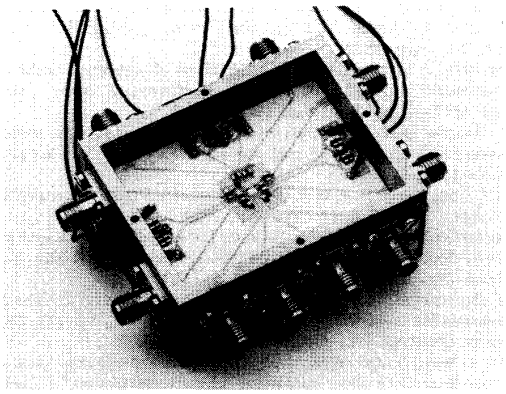


Fig. 15. Test HIC.

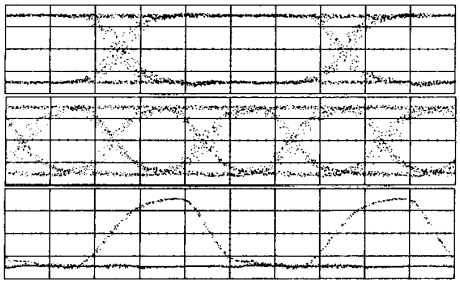


Fig. 16. Measured output current eye-diagrams in a $50\,\Omega/+5$ V load for (a) 1.0 Gb/s NRZ data (b) 2.5 Gb/s NRZ data and (c) 1.0 Gb/s RZ data. Horizontal: 60 mA/div and Vertical: 200 ps/div.

and 1 Gb/s using RZ data format is shown in Fig. 16(a)–(c), respectively. The NRZ signals are obtained using data buffer 2, while the RZ signal is (of course) obtained using data buffer 1. Thus the ability of the implemented MS-DFF to reduce time jitter is evident. From Fig. 16 we also notice the upper bit rate limit to be close to 2.5 Gb/s for a modulation current amplitude of 60 mA. It should be emphasized that the obtained NRZ eye diagrams are BER tested using a 5 Gb/s Anritsu error detector ensuring error-free eye diagrams. The total power dissipation is $P_{\rm dis} = 2$ W for a modulation current amplitude of $I_{\rm mod} = 60$ mA and nominal power supplies of $V_{\rm DD} = -V_{SS} = 5$ V.

Rise and fall-times for different modulation current amplitudes have been measured as shown in Fig. 17(a) and (b), where the corresponding expected performance from circuit simulations is also included. Thus the deviation between measured and simulated values in percentage of the predicted values is less than 5% for the rise time for modulation current amplitudes ranging from 10–60 mA for the fall times less than 15% over the modulation current amplitude range of 20–60 mA increasing to 30% for the modulation current amplitude decreasing to 10 mA.

B. Optical-Fiber Transmission Experiment

A back-to-back optical-fiber transmission experiment has also been conducted. Fig. 18 shows the experimental setup. The laser driver IC directly modulated a Siemens 1.55-μm

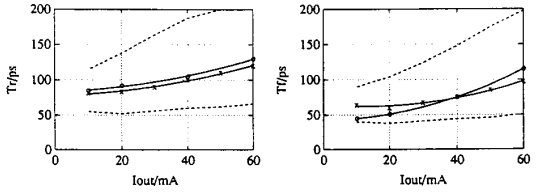


Fig. 17. Measured ($\circ$) and simulated ($\times$) transition times in a $50\,\Omega/+5$ V load as function of output current amplitude (a) rise time and (b) fall time. Dashed lines indicate simulated worst-case performance limits caused by process spread.

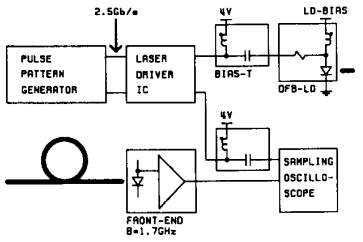


Fig. 18. Block diagram of the experimental setup used for the optical-fiber transmission experiment.

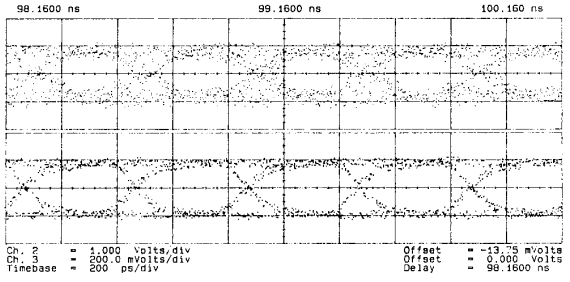


Fig. 19. Eye diagrams of the received optical signal (upper trace) and of the corresponding laser driver complementary output (lower trace). Horizontal: 200 ps/div and Vertical: 200 mV/div (upper trace) and 20 mA/div (lower trace).

wavelength DFB laser diode. The modulation current amplitude was 40 mA switching the total current just below threshold during logic low for the employed bias current. The 2.5 Gb/s PRBS input data stream was generated by an Anritsu pulse pattern generator, and the transmitted optical signal was received using a BT&D commercial front end with a bandwidth of $B = 1.7$ GHz. Finally, the output signal from the front end and the laser driver complementary output was monitored simultaneously by an HP sampling oscilloscope, see Fig. 19, and as can be seen from Fig. 19, an optical eye diagram with good eye opening was obtained.

IX. Conclusion

A laser-diode driver GaAs IC incorporating a NRZ/RZ conversion option has been designed. A novel open-drain cascode differential amplifier type output driver has been implemented allowing higher-drive currents for the same drain-to-gate break down voltage than conventional differential output drivers, and a novel logic family DCAL type SCFL improving performance

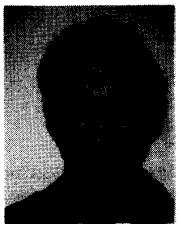
over process and significantly improving noise margin over that obtained using conventional RL type SCFL is developed for implementing the on-chip logic functions. Finally, a laser-diode large-signal model is applied to evaluate the performance of the laser-driver IC using circuit simulations. Current eye diagrams with 60 mA eye opening were measured up to NRZ bit rates of 2 Gb/s, 50 mA eye opening was demonstrated at a NRZ bit rate of 2.5 Gb/s, and a retimed low-time jitter 1 Gb/s RZ current eye diagram with 60 mA eye opening was demonstrated in a 50 Ω measuring system. The laser driving performance of the IC has been demonstrated experimentally by obtaining good optical eye diagrams when driving a Siemens DFB laser in a back-to-back optical-fiber transmission experiment at 2.5 Gb/s.

ACKNOWLEDGMENT

The author wishes to thank his colleagues in the gigabit electronics group at CBT for encouragement and discussions, and Dr. R. J. Pedersen is acknowledged for his assistance during the optical measurements.

REFERENCES

[1] M. Berroth *et al.*, "10–20 Gbit/s GaAs/AlGaAs HEMT ICs for high speed data links," in *Tech. Dig. GaAs IC Symp.* (Miami Beach, FL), Oct. 1992, pp. 291–294.
[2] K. Runge *et al.*, "AlGaAs/GaAs HBT IC's for high-speed lightwave transmission systems," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, pp. 1332–1339, Oct. 1992.
[3] T. Takada and H. Ohtsuka, "A new interfacing method "SCFL-interfacing" for ultra-high speed logic ICs," *Tech. Dig. GaAs IC Symp.* (New Orleans), Oct. 7–10 1990, pp. 211–214.
[4] K. Utsumi *et al.*, "Gigabit optical transmitter GaAs MESFET IC," *Electron. Lett.*, vol. 23, no. 8, pp. 374–375, Apr. 1987.
[5] S. Katsu *et al.*, "A GaAs monolithic frequency divider using source coupled FET logic," *IEEE Electron Dev. Lett.*, vol. EDL-3, no. 8, pp. 197–199, Aug. 1982.
[6] M. Idda, T. Takada, and T. Sudo, "Analysis of high-speed GaAs source-coupled FET logic circuits," *IEEE Trans. Microwave Theory Techniques*, vol. MTT-32, pp. 5–10, Jan. 1984.
[7] T. Takada, *et al.*, "A 2 Gb/s throughput GaAs digital time switch LSI using LSCFL," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1579–1584, Dec. 1985.
[8] S. I. Long and S. E. Butner, *Gallium Arsenide Digital Integrated Circuit Design.* New York: McGraw-Hill, 1990.
[9] Yasuyuki Suzuki *et al.*, "A 10Gbit/s laser driver IC with i-AlGaAs/n-GaAs doped-channel hetero-MISFETs (DMTs)," in *Tech. Dig. GaAs IC Symp.* (San Diego, CA), Oct. 1989, pp. 129–132.
[10] N. Kotera *et al.*, "Laser driver and receiver amplifiers for 2.4Gb/s optical transmission using WSi-gate GaAs MESFET's," in *Tech. Dig. GaAs IC Symp.* (Portland, OR), Oct. 1987, pp. 103–105.
[11] W. I. Way, "Large signal nonlinear distortion prediction for a single-mode laser diode under microwave intensity modulation," *J. Lightwave Technol.*, vol. LT-5, no. 3, pp. 305–315, Mar. 1987.
[12] R. S. Tucker, "Large-signal circuit model for simulation of injection-laser modulation dynamics," *IEE Proc.*, vol. 128, Pt. I, no. 5, Oct. 1981, pp. 180–184.
[13] R. S. Tucker and I. P. Kaminow, "High-frequency characteristics of directly modulated InGaAsP ridge waveguide and burried heterostructure lasers," *J. Lightwave Technol.*, vol. LT-2, no. 4, pp. 385–393, Aug. 1984.



Jesper Riishøj was born in Virum, Denmark, on October 14, 1961. He received the M.Sc. degree in electrical engineering from the Technical University of Denmark (TUD) in 1986. After graduation, he joined the Electromagnetics Institute (EMI) at TUD, where he copioneered the work on gigabit electronics. In 1988 he began working at EMI, where he naturally joined the Centre for Broadband Telecommunications In 1991 he received the Ph.D. degree in electrical engineering. Recently, he has been engaged in the design of monolithic integrated circuits for high-speed optical-fiber communication systems.