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De-embedding and Modelling of pnp SiGe HBTs

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***Abstract*— In this work we present a direct parameter extraction procedure for SiGe pnp heterojunction bipolar transistor (HBT) large-signal and small-signal models. Test structure parasitics are removed from the measured small-signal parameters using an open-short de-embedding technique, improved to account for the distributed nature of the interconnect lines. Good agreement is achieved between the small-signal model of the HBT and the measurements. Parameters for the large-signal VBIC model are extracted based on multi-bias small-signal model extraction, leading to consistency between measured and modeled f_T.**

I. Introduction

A complementary BiCMOS (CBiCMOS) technology is a promising approach to achieve low voltage supply, low power consumption and high speed simultaneously in millimetre-wave applications. The main challenge to develop such a process is to integrate high performance pnp transistors in a BiCMOS technology. IHP's 0.25 µm SiGe:C CBiCMOS process offers a successful combination of npn HBTs with f_T/f_{max} of 170/170GHz and pnp HBTs with f_T/f_{max} of 90/120GHz (drawn emitter area: 0.22×0.84 µm²) [1].

Successful circuit design using this technology requires accurate circuit models for both transistor types. Modelling of npn SiGe HBT devices has been a wide area of research [3]-[5]. In this paper, we focus on the modelling of the pnp HBTs.

An accurate de-embedding of the test structure parasitics is firstly implemented to improve HBT model accuracy. Hereafter, the de-embedded measurement results are applied for a direct parameter extraction of the small-signal equivalent circuit parameters. The model is verified by comparison of the simulated and measured results up to 49 GHz. The small-signal model is utilized for parameter extraction for the large-signal VBIC95 model. The VBIC95 model [6] includes several advantages compared to the SPICE Gummel-Poon model: improved Early-effect modelling, quasi saturation, substrate and oxide parasitics, avalanche-multiplication and self-heating behaviour – all of which are important for accurate modelling of modern SiGe HBTs.

Finally, the VBIC model is experimentally verified against the measurements.

II. De-Embedding of the Test Structure

A three-step de-embedding method reported in [2] is employed to remove the contribution of the test structure parasitics. This method is further developed here to account for the distribution of the interconnect lines of the test structure. The equivalent circuit for the test structure including the transistor is shown in Fig. 1. Elements Y_{inn}xx and Y_{pad}xx, model the distributed coupling of the interconnect lines and the pads to the ground. Coupling between the pads through the substrate is negligible due to the presence of the ground shield. Y_{bc} is therefore assumed to be the only transmission element in the open structure. Two loading admittances of the two respective pads together with the corresponding interconnect lines are represented as the elements of the admittance matrix Y_{line}, as

$$Y_{line} = \begin{bmatrix} Y_{open11} + Y_{open21} & 0 \\ 0 & Y_{open22} + Y_{open12} \end{bmatrix} \quad (1)$$

where Y_{open}xx are measured admittance matrix elements of the open standard. An empirical factor n is introduced to divide the Y_{line}, into Y_{pad} and Y_{inn} admittance matrices as

$$Y_{pad} = Y_{line} \cdot n\,; \qquad Y_{inn} = Y_{line} \cdot (1-n)\,, \quad (2)$$

where contribution of series impedances Z_{pb} and Z_{pc} to Y_{line} at low frequencies is assumed to be negligible. Series impedance elements, Z_{pb}, Z_{pc} and Z_{pe}, are extracted as

$$Z_p = \left(Y_{short} - Y_{pad}\right)^{-1} \quad (3)$$

$$Z_{pe} = Z_{p12} \quad (4)$$

$$Z_{pb} = \left(Z_{p11} - Z_{p21}\right) \cdot n_{shift} \quad (5)$$

$$Z_{pc} = \left(Z_{p22} - Z_{p12}\right) / n_{shift} \quad (6)$$

where Y_{short} is the admittance matrix of the short standard measurement, and n_{shift} is introduced to correct a de-embedding error, as will be explained later.

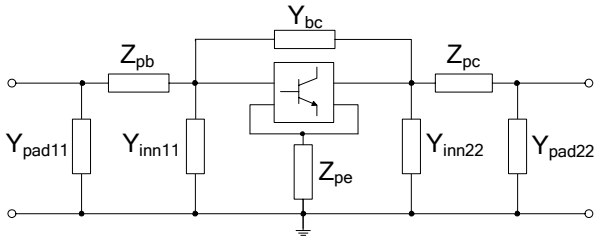

Fig. 1 Equivalent circuit model for the HBT test structure

The factor n in (2) is found from the frequency dependence of the inductive part of Z_{pb} and Z_{pc}, which both can be modelled as a series-connected inductor and resistor. As shown in Fig. 2, L_{pc} is nearly frequency independent when n=0.65, meaning that only ~65% of Y_{line} admittance is due to the physical pad. Reduced frequency dependence is correspondingly observed in the extracted small-signal equivalent circuit element values of the HBT discussed.

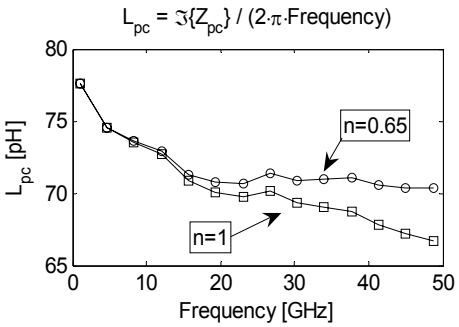

Fig. 2 Extracted inductances of the interconnect line on the collector side

III. Extraction of the Small-Signal Equivalent Circuit Parameters

The small-signal equivalent circuit for the pnp SiGe HBT is shown in Fig. 3 [3]. The bias dependent intrinsic part describes the active device, while the extrinsic part represents the device parasitics.

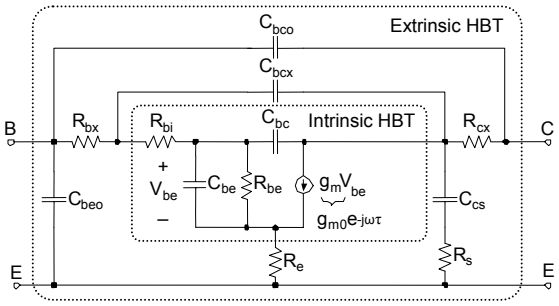

Fig. 3 Small-signal equivalent circuit of a SiGe HBT biased in forward active mode operation

A. Oxide Capacitances

The total base-emitter and base-collector capacitances, C_{in} and C_{fb}, have been extracted from the Y-parameters of an HBT biased in the cut-off mode operation [3]. They are modelled in VBIC as sums of the fixed oxide capacitances and bias dependent junction capacitances,

$$C_{in} = C_{beo} + \overbrace{\frac{C_{je}}{\left(1-\frac{V_{be}}{P_e}\right)^{M_e}}}^{C_{be}}; \quad C_{fb} = C_{bco} + \overbrace{\frac{C_{jc}+C_{jep}}{\left(1-\frac{V_{bc}}{P_c}\right)^{M_c}}}^{C_{bc}+C_{bcx}} \tag{7}$$

respectively, where C_{je} and C_{jc} are zero-bias depletion capacitances, P_e and P_c are built-in potentials and M_e and M_c are grading terms of the two respective junctions. C_{bcx} is the extrinsic base-collector zero-bias depletion capacitance. The parameters are extracted by fitting the two curves, (C_{fb}-C_{bco}) vs. (1-V_{bc}/P_c) and (C_{in}-C_{beo}) vs. (1-V_{be}/P_e) respectively, to straight lines in double logarithmic plots [4].

B. Fixed Access Resistances and Inductances

HBTs in saturation can be represented by a simple T-network of resistors corresponding to access resistances R_{bx}, R_{cx}, and R_e in Fig. 3. These resistors are found from the de-embedded Z-parameters at these bias conditions after removal of the fixed oxide capacitances as

$$R_{bx} = \Re\{Z_{11} - Z_{12}\} \tag{8}$$

$$R_e = \Re\{Z_{12}\} \tag{9}$$

$$R_{cx} = \Re\{Z_{22} - Z_{12}\}. \tag{10}$$

The values of these resistors in deep saturation (I_B=3mA) are not varying with frequency, as depicted from Fig. 4(a), over a large frequency range. The fixed resistances are found from extrapolation of the values in (8) at large base currents as shown in Fig. 4(b).

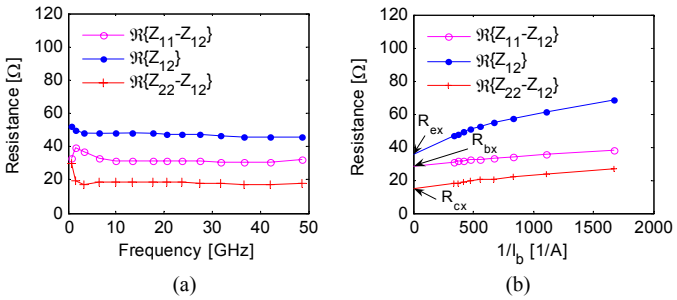

Fig. 4 (a) Extracted values of equations (8)-(10) at I_B=3mA and I_E=I_C=1.5mA. (b) Determination of R_{bx}, R_{cx}, and R_e from extrapolation of the Z-parameters.

Total access inductances of base and collector can be extracted as in (8)-(10) by using the imaginary part of the impedances. Negative collector inductance and relatively large base inductance are derived using this procedure. This indicates that the probes in the measurement setup could have been slightly shifted towards the collector side compared to the probe location in the short standard measurements. Adding 4 pH to the collector inductance and subtracting the same from the base inductance would balance both inductances. This error is compensated by the factor n_{shif}=1.06 in (5) and (6), since the compensating inductance corresponds to ~6% of the inductance of the access lines. After the compensation, the two access inductances have become negligibly small, 1.5 pH, and have therefore been omitted from the equivalent circuit.

C. Substrate Parasitics

After the oxide capacitances and the fixed resistances in base and collector have been removed, the elements of the parasitic substrate transistor can be extracted through the Y-parameters of HBTs in cut-off mode operation [3]. Neglecting the R_e in Fig. 3, the substrate resistance R_s and the collector-substrate capacitance C_{cs} have been extracted as

$$R_s = \Re\left(\frac{1}{Y_{22}+Y_{12}}\right); \qquad \omega C_{cs} = -\left\{\Im\left(\frac{1}{Y_{22}+Y_{12}}\right)\right\}^{-1}. \quad (11)$$

The extracted C_{cs} is fitted to the usual depletion capacitance expression, excluding the oxide capacitance term and using the corresponding VBIC parameters, M_s, P_s and C_{jcp}.

D. Hybrid-π Equivalent Circuit Modelling

The intrinsic HBT shown in Fig. 3 exhibits the well-known hybrid-π topology. The elements are extracted analytically from Y-parameters after removing the extrinsic part of the HBT except C_{bcx} using the method reported in [5]. Some extracted elements vs. frequency are shown in Fig. 5.

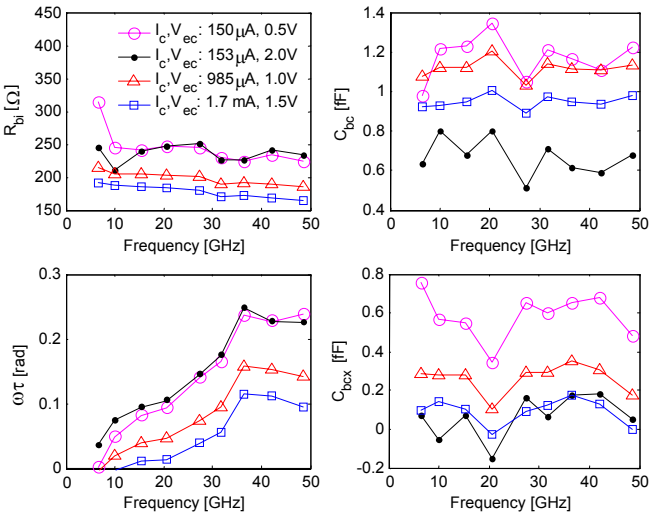

Fig. 5 Frequency dependence of the extracted elements for the hybrid-π circuit at four bias points

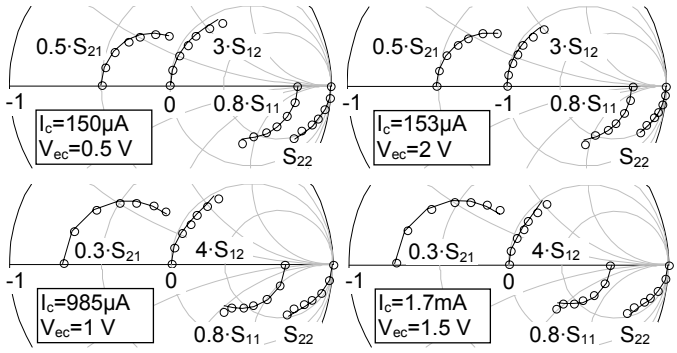

Fig. 6 Measured (o) and modelled (-) s-parameters in frequency range 0-49 GHz for the two parallel-connected HBTs biased in forward active region.

TABLE 1

EXTRACTED SMALL-SIGNAL MODEL ELEMENT VALUES

Fixed elements					
C_{bco} [fF]	C_{beo} [fF]	R_{bx} [Ω]	R_{cx} [Ω]	R_e [Ω]	R_s [Ω]
2.4	1.75	29	14.6	36	500

I_c[mA] / V_{ec}[V]	Bias dependent elements							
	C_{cs} [fF]	R_{bi} [Ω]	g_{m0} [ms]	C_{bc} [fF]	τ [ps]	C_{be} [fF]	C_{bcx} [fF]	R_{be} [kΩ]
0.15/0.5	2.1	230	5.2	0.97	0.53	10	0.70	21
0.153/2	1.8	231	5.5	0.41	0.58	9.6	0.25	8.8
0.985 /1	1.9	190	28	0.88	0.07	39	0.31	0.72
1.7/1.5	1.8	170	48	0.71	0	70	0.1	0.25

Comparison between the measured and the small-signal modelled S-parameters is shown in Fig. 6. Excellent agreement under various bias conditions is achieved in a wide frequency range. Simulated curves in Fig. 6 are based on extracted element values listed in Table 1.

IV. PARAMETER EXTRACTION FOR VBIC MODEL

Some of the extracted small-signal element values, like oxide capacitances, access resistances and parasitic substrate resistance have been directly used as parameters of the large-signal VBIC model. Collector-base depletion capacitance term in (7) at zero-bias is partitioned into C_{jc} and C_{jep} using the extracted C_{bc}/C_{bcx} ratio of ~7 at the peak cut-off frequency. Partitioning of the total base current of the reverse Gummel-plot into intrinsic base-collector current I_{bc}, and parasitic base-emitter current I_{bep} is based upon the same ratio.

The extracted values for the intrinsic base resistance plotted versus collector current are shown in Fig. 7. The base resistance in the VBIC model is modulated by the normalized base charge q_b. The value extrapolated at the zero-current is used as R_{bi} in the VBIC model since q_b approaches unity there.

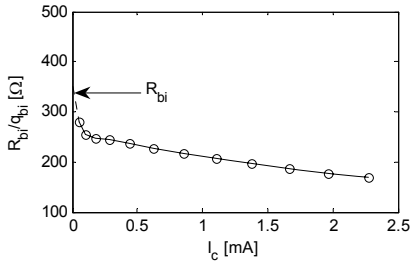

Fig. 7 Extracted intrinsic base resistance versus collector current at V_{ec}=1.5 V.

From the average slope of the $\omega\tau$ plot in the Fig. 5 it appears that the extracted excess phase delay τ falls with increasing collector current. The reason is that the base-collector reverse voltage and hence the collector depletion width, which contribute to the total transit time, decrease. Since the excess phase delay in the VBIC model is

independent on the bias, an average value of 0.4 *ps* is used for the excess phase delay parameter T_d. Such a low value for the excess phase delay has only little impact on the small-signal behaviour well below the cut-off frequency f_T.

Quasi-saturation-parameters, R_{ci}, *Gamma*, V_0 and H_{rcf}, are found by fitting the collector current I_c versus emitter-collector voltage V_{ec} curves, as shown in Fig. 8. The resulting value of R_{ci} was 95 Ω.

Subsequently, the forward transit time parameter T_F, which describes the hole transport through the base region and the collector depletion region, is estimated by extrapolation of the plot of the measured forward transit time vs. inverse collector current as illustrated in Fig. 9. The $(R_{cx}+R_{ci})\cdot C_{bc}$ term accounts for a contribution from the parasitic collector resistance.

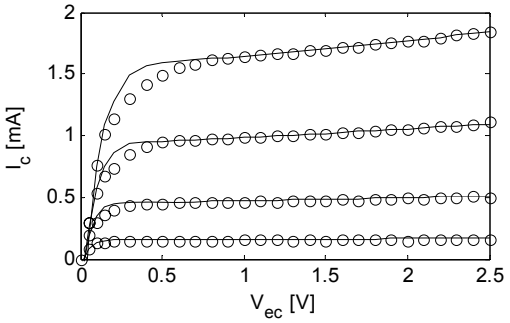

Fig. 8 Measured (o) and modelled (-) output characteristics at the base-emitter voltage swept from -0.85 to -1V in 50 *mV* steps

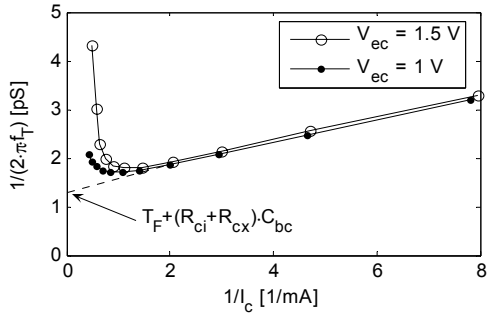

Fig. 9 Measured transit time vs. inverse collector current at two emitter-collector voltages V_{ec}.

Finally, the parameters X_{tf}, V_{tf}, I_{tf} and Q_{tf}, which determine the transit time bias dependence, are determined from the f_T - I_C curves shown in Fig. 10. Behaviour of the collector-base heterojunction was not captured by the VBIC with a high accuracy. Using an R_{ci}=200Ω in the parameter extraction would have yielded a remarkably better fit of the output characteristics in the quasi-saturation region as well as of the f_T - I_C curve at V_{ec}=0.5*V*. This resistance is however much larger than expected from the layer properties of the structure.

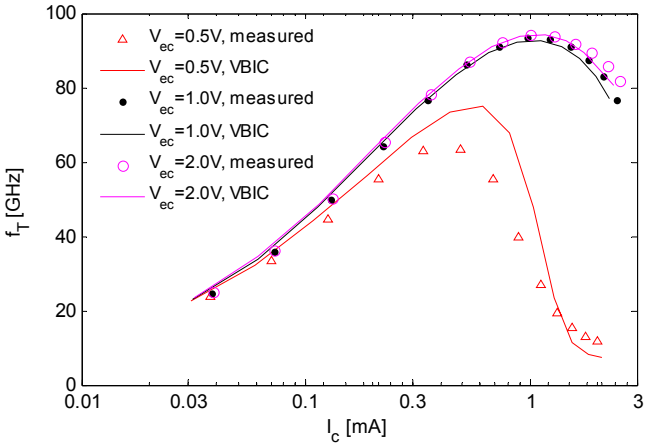

Fig. 10 Measured and modelled bias dependency of the cut-off frequency

V. Conclusions

This work focuses on modelling of high performance SiGe pnp HBT devices. Parasitics of the test structure are de-embedded taking into account distributed impedance of the interconnect lines. A de-embedding error resulting from the probe positioning inaccuracies is corrected. The elements of the small-signal equivalent circuit of the HBT are analytically extracted leading to an excellent agreement between the model and the measurements. The small-signal model has also shown to be beneficial for extraction of the VBIC model parameters. It was not possible to accurately model the transistor action in quasi-saturation, while simultaneously keeping the physical meaning of the VBIC parameters.

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