Technical University of Denmark

DTU

45% power saving in a 0.25m BiCMOS 10Gb/s 50-terminated packaged active-load laser driver

Ayranci, E.; Christensen, K.; Andreani, Pietro

Link back to DTU Orbit

DTU Library
Technical Information Center of Denmark

30.8 45% Power Saving in a 0.25µm BiCMOS 10Gb/s 50Ω-Terminated Packaged Active-Load Laser Driver

Emre Ayranci[1,2], Kenn Christensen[3], Pietro Andreani[1]

[1]Technical University of Denmark, Kgs. Lyngby, Denmark
[2]Intel Copenhagen, Skovlunde, Denmark
[3]IPtronics A/S, Roskilde, Denmark

The race for higher speed and lower power consumption in cheaper communication ICs does not appear to ever abate. This is particularly true for the circuits at the interface of optical communication systems, where it is desirable to exploit the full data rate allowed by optical fibers as much as possible while still ensuring manageable power dissipation. Access to more advanced silicon processes provides a brute-force approach to stay competitive in this market, but innovative design techniques and circuit solutions are equally or even more important. The measurement results show that using the proposed architecture shown in Fig. 30.8.2, the power consumption of the standard laser driver of Fig. 30.8.1 (see e.g. [1]) is reduced almost by half.

Although the laser diode is usually driven single-ended, the laser driver itself is implemented as a differential stage, in order to keep the current drawn from the power supply as constant as possible. This measure minimizes the amount of signal noise injected into the power supply, which would be intolerable in a single-ended laser driver, due to the large currents needed to modulate the laser. In order to keep the design as symmetrical as possible, the unused output of the laser driver is loaded in the same way as the laser-driving output, typically with a 50Ω transmission line. The output resistors R_{out} of the driver must then have a value of 50Ω as well, to properly terminate the transmission lines. This choice, however, implies that half of the signal current does not reach the laser, but is wasted on R_{out}. This translates directly in a doubling of the required bias current, and therefore of the power consumption, for a desired modulation current. This is indeed an expensive price to be paid for achieving impedance matching, and it is therefore desirable to investigate alternative design approaches to save power.

It is possible to allow high output impedances in the driver, and still enforce 50Ω-load impedance matching, by resorting to feedback. Each single-ended load impedance can be used to provide the correct termination for the other (single-ended) load impedance. Therefore, the impedance at one output is mirrored to the other output, and vice versa. The only drawback of this solution is that it only applies to AC-coupled lasers. The simplified schematic of the active-load laser driver is shown in Fig. 30.8.2, where PMOS transistors replace the output resistances. Feedback is introduced by the 2 resistances R_f and the opamp A driving the PMOS gates. If the gain of the feedback loop is large, then it is safe to assume that V_{CM} is equal to the bias voltage V_{BIAS}, i.e., V_{CM} is fixed. To show that each load resistor basically sees an impedance equal to the other load resistor, the circuit in Fig. 30.8.3 is used. In this circuit, the right-side load is substituted by a small-signal current source I_i, generating the small-signal voltage V_i. Since V_{CM} is fixed, then the same node has a zero small-signal voltage, which immediately results in $V_o = -V_i$. Using Kirchoff's current law (KCL) at the output node, I_{M2} can be written as $I_{M2} = V_i/R_f - V_o/R_{load} = V_i/R_f + V_i/R_{load}$. Since $I_{M1} = I_{M2}$, KCL at the input node finally yields $I_i = 2V_i/R_f + V_i/R_{load}$. Therefore, the input impedance R_i becomes

$$R_i \equiv \frac{V_i}{I_i} = R_{load} \parallel \frac{R_f}{2}$$

which can be simplified to $R_i \approx R_{load}$ if $R_f \gg R_{load}$. Thus, as previously stated, the load resistance at the left-hand (unused) output can

be used to terminate the load resistance at the right-hand (laser-driving) output. Of course, the reverse is also true. Similar driver designs have appeared in the literature, without, however, an awareness of their output-matching capabilities.

The 28×66µm² active-load laser driver is implemented in a 0.25µm BiCMOS process with an f_T of 70GHz for the NPN bipolar transistor. The opamp is a simple differential-input single-output stage, because it is able to provide enough low-frequency loop gain and at the same time maximize the loop bandwidth. The value of the feedback resistors R_f is set to 1kΩ and it has little impact on matching. The GBW of the loop gain is ~10GHz.

The laser driver draws 5mA from a 1.8V supply. The targeted laser is a low-current VCSEL (see e.g. [2]), although nothing in the proposed technique prevents the use of higher currents, if needed for driving more power-hungry lasers. Since the auxiliary opamp only draws an additional 0.5mA, the overall current draw is reduced by 4.5mA (i.e., 45%), when compared to the standard laser-driver design of Fig. 30.8.1 that needs 10mA for the same output signal current.

The active-load laser driver, which is part of a larger design, is mounted on a 49-pin 6×6mm² plastic-BGA (PBGA) package and tested. Figure 30.8.4 shows the return loss for the 2 outputs, when they are driven separately and single-ended. These return losses, although rather high in the vicinity of 5GHz, are sufficient for the application.

The eye diagram of the laser driver is shown in Fig. 30.8.5 for the nominal data rate of 10Gb/s. The measurements are performed on a stand-alone block, which implies that both driver inputs and driver outputs are loaded by the package. Since in a real-life application the driver would be driven on-chip, an even cleaner eye diagram is actually expected. Finally, only a very slight difference is detected comparing the eye diagram with that for the standard laser driver of Fig. 30.8.1. A die micrograph of the active-load laser driver is shown in Fig. 30.8.6.

References:
[1] Datasheet of Intel LXT17001 10Gb/s Laser Driver IC, Dec., 2005.
[2] Datasheet of 10Gb/s 850nm VCSELs HFE6x9x-56x, Advanced Optical Components, Apr., 2005.
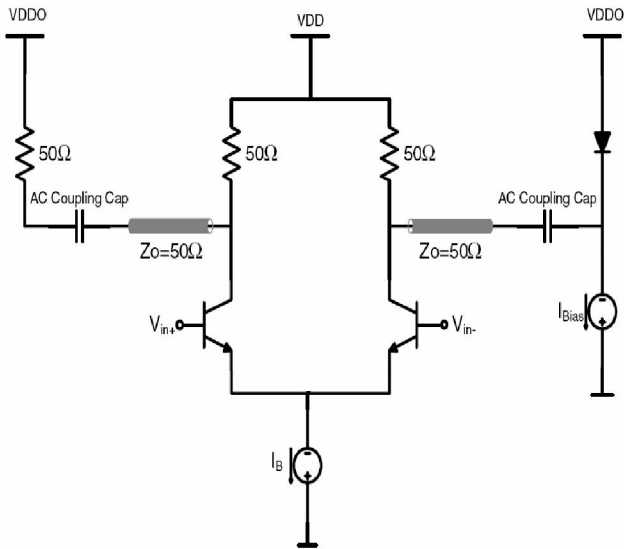
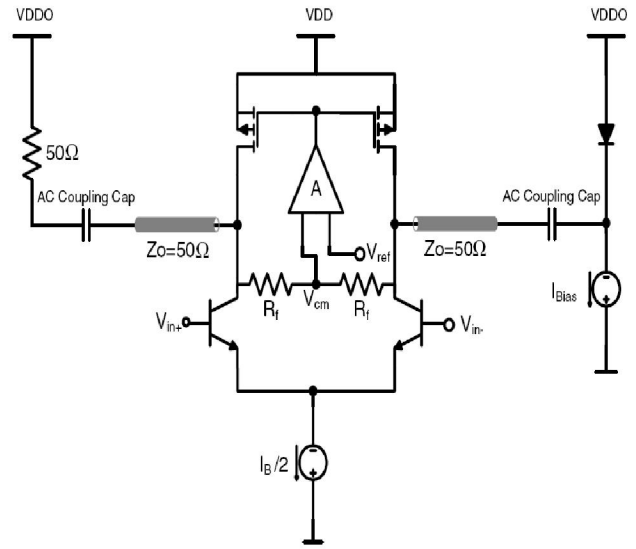Figure 30.8.1: Traditional implementation of the laser driver.

Figure 30.8.2: Proposed implementation of the laser driver, based on active loads.
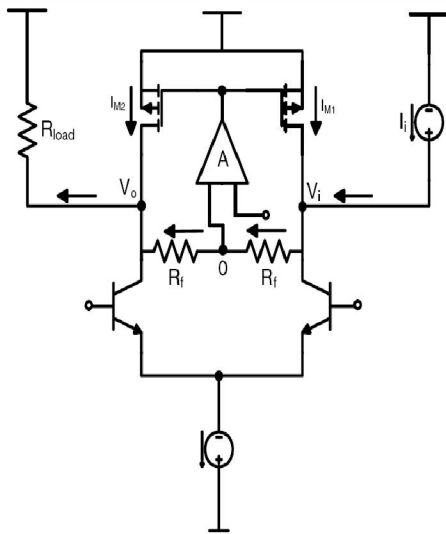

Figure 30.8.3: Small-signal analysis of the single-ended output impedance in the active-load laser driver.
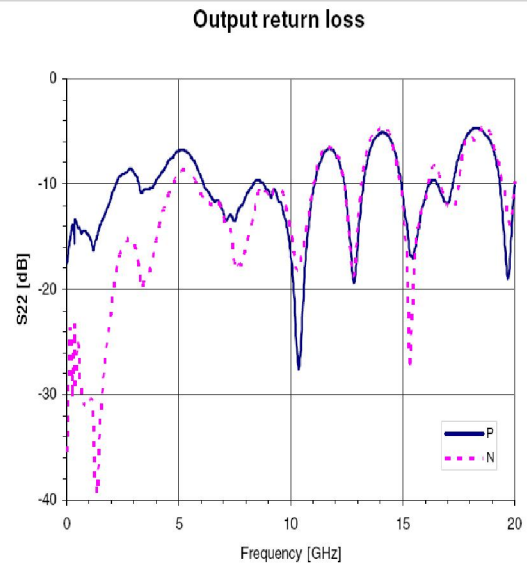

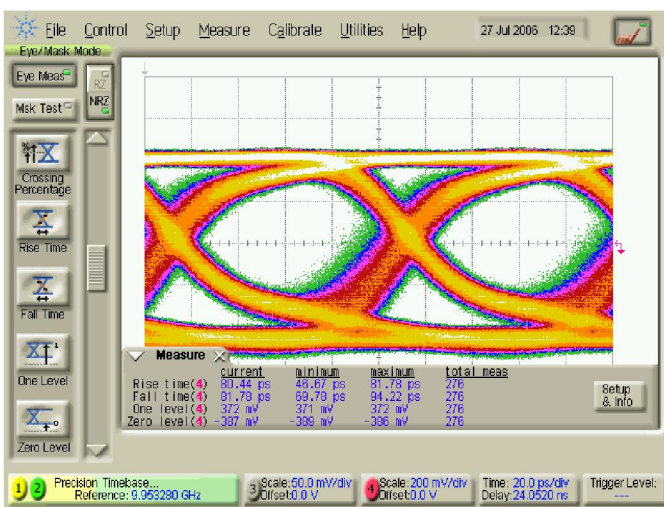Figure 30.8.4: Return loss for both outputs of the active-load laser driver.

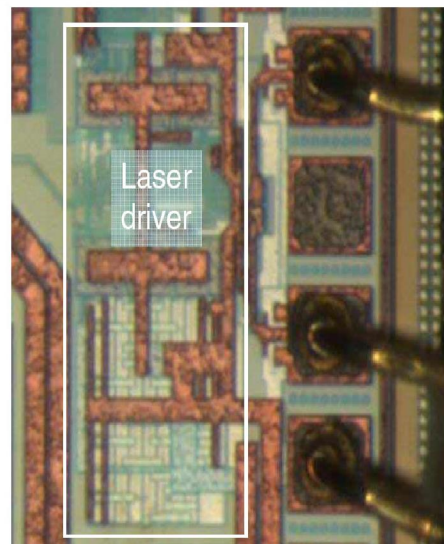Figure 30.8.5: Eye diagram for the active-load laser driver at 10Gb/s data rate.

Figure 30.8.6: Die micrograph of the active-load laser driver (active area: 28×66μm²).

30