Enhancement of VCO Linearity and Phase Noise by Implementing Frequency Locked Loop

Ayranci, E; Christensen, K; Andreani, Pietro

Published in:
EUROCON, 2007. The International Conference on "Computer as a Tool"

Link to article, DOI:
10.1109/EURCON.2007.4400681

Publication date:
2007

Document Version
Publisher's PDF, also known as Version of record

Enhancement of VCO Linearity and Phase Noise by Implementing Frequency Locked Loop

Emre Ayranci*, Kenn Christensen†, Pietro Andreani*
*Center for Physical Electronics, Oersted.DTU, Kgs. Lyngby, Denmark, e-mail: *emrea@ieee.org*
†IPtronics A/S, Roskilde, Denmark, e-mail: *kenn.christensen@iptronics.com*

***Abstract*— This paper investigates the on-chip implementation of a frequency locked loop (FLL) over a VCO that decreases the phase noise and linearizes the transfer function. Implementation of the FLL inside a PLL is also investigated and a possible application is highlighted. Design of a special kind of low noise frequency detector without a reference frequency (frequency-to-voltage converter), which is the most critical component of the FLL, is also presented in a 0.25 μm BiCMOS process. Linearization and approximately 15 dBc/Hz phase noise suppression is demonstrated over a moderate phase noise LC VCO with a center frequency of 10 GHz.**

***Keywords*— Frequency-locked loop (FLL), voltage-controlled oscillator (VCO) linearity, phase noise, frequency-to-voltage converter, phase-locked loop (PLL).**

I. Introduction

VCOs are one of the most critical blocks in PLLs, so there is a huge research going on to improve the performance of the VCOs. This paper focuses on a FLL, which shows several advantages over a standalone VCO. The FLL that includes a VCO, a frequency-to-voltage (f2V) converter, a voltage-to-current converter and a loop filter, is defined as the proposed "VCO block" in this paper.

The advantages of implementing a FLL over a VCO in a PLL can be summarized in the following two points. Firstly, the FLL makes the VCO block tuning curve linear. This brings the advantage of having the same VCO gain for different frequencies inside the VCO tuning range. When the VCO gain changes due to non-linearity, the loop gain of the PLL changes for different frequencies inside the frequency range. This results in a compromise on the jitter transfer and generation of the module. The loop filter can be changed for different regions of the frequency range to decrease this effect, but this is not an efficient solution and not possible in module level. Using a linear VCO block gives the advantage of having the same PLL transfer function for all frequencies inside the frequency range with the same loop filter. Secondly, a PLL with a low loop-bandwidth can not suppress the phase noise of the VCO at frequencies higher than PLL bandwidth. An FLL with a high loop-bandwidth yields the improvement of decreasing the phase noise of the VCO inside the FLL bandwidth.

The advantage of implementing an FLL over a VCO can be observed in both LC VCOs and inverter-based VCOs. Implementation of an FLL can linearize an LC VCO and also decrease its phase noise, depending on the frequency-to-voltage (f2V) converter noise. On the other hand, the phase noise of inverter-based VCOs can be decreased extensively, in addition to obtaining more linearity. The phase noise performance of the FLL depends mainly on the f2V converter noise and the phase noise of rather noisy VCOs can also be decreased to amounts similar to those belonging to lower phase noise VCOs.

The advantage of the method can be highlighted with the following example. In applications using PLLs, there are parts where the output jitter is more critical, such as outputs, and parts where it is more relaxed, such as inputs. In these kind of applications, an inverter-based VCO is used when output jitter is not that critical, but low phase noise LC VCOs are used in PLLs, where output jitter is important. Thus, it is often the case that both kinds of VCOs are used within the same application. If a FLL is implemented over the same inverter-based VCO that is used in the input, the phase noise of this VCO can be suppressed to a similar level with a LC VCO and it can be used in the output as well. In this way, the control voltage of the inverter-based VCO in the input can be copied to the VCO in the output and substantially decrease the locking time. In addition, this frequency-locked VCO will be linear as well, and having the same gain over the frequency range will be yet another advantage of the method.

Up to our knowledge, there has not been any work published implementing an on-chip FLL inside a PLL, in order to decrease the phase noise and achieve a linear VCO transfer function. However, there is a work on linearization with discrete components [1]. Use of switched banks in digitally-controlled oscillators gives a relative linearity to the oscillator transfer function, which is an active research area both industrially [2] and academically [3], [4]. The FLL is a good alternative to this method especially in terms of locking time, power consumption and complexity. In addition both methods can be used together as well.

In this paper, the linearization concept will be discussed and demonstrated in section II. It will be followed in section III by a proof of phase noise suppression and a transistor-level design of a f2V converter, which is the most critical component in the loop. In section IV, FLL implementation inside a PLL will be explained, and the feasibility of implementing another loop inside a PLL will be demonstrated.

1-4244-0813-X/07/$20.00 2007 IEEE.

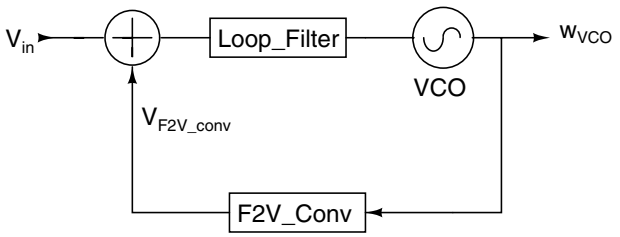

Fig. 1. The proposed "VCO Block" containing FLL

II. Linearization

A. Linearization Concept

The principle of linearizatin can be described as follows. The tuning curve of the proposed VCO block, which now consists of the FLL, is independent of the VCO tuning curve, and determined only by the response of the f2V converter. Once the FLL settles, the output frequency is set by the input voltage, which acts as an offset voltage on the response of the f2V converter. The f2V converter output voltage has to compensate the offset created by the input control voltage and the overall transfer function of the system follows the linear transfer function of this component. Hence, the structure can be used as a new VCO, where V_{in} is the control voltage and w_{vco} is the output frequency. The proposed VCO block is shown in Fig. 1.

In order to see how the concept works, let us first look at the equations of the loop. The output voltage of the f2V converter can be defined as (1), where g(x) is the transfer function of the f2V converter.

$$V_{F2Vconv} = g(w_{VCO}) \tag{1}$$

After being subtracted from the overall control voltage of the proposed VCO block (V_{in}) and integrated by the filter, the input voltage of the VCO ($V_{LF_{out}}$), which is the output voltage of the loop filter, is calculated by (2). Here, the contribution of the f2V converter is subtracted, so in the actual implementation this will be designed with a negative slope transfer function. T is the integrator constant of the loop filter.

$$V_{LF_{out}} = \frac{1}{T} \cdot \int (V_{in} - V_{F2Vconv}) \cdot dt \tag{2}$$

By using the information from (2), the output frequency of the FLL is written as

$$w_{VCO} = K_{VCO} \cdot \frac{1}{T} \cdot \int (V_{in} - V_{F2Vconv}) \cdot dt \tag{3}$$

When the loop settles, i.e. in the steady state, the VCO frequency will not change any more; so when $t \rightarrow \infty$, we obtain

$$\frac{\partial w_{VCO}}{\partial t} = \frac{K_{VCO}}{T} \cdot (V_{in} - V_{F2Vconv}) = 0 \tag{4}$$

Using (1) and (4), and noticing that K_{VCO} cannot be zero, we get

$$w_{VCO} = g^{-1}(V_{in}) \tag{5}$$

As clear from (5), the output frequency of the VCO is now dependent on the inverse function of the f2V converter, and independent of the VCO sensitivity variations. The f2V converter is the new master of the loop, and the center frequency is also set by the f2V converter.

In order to see the transfer function of f2V converter and how it matches up with these equations to give a linear voltage frequency characteristics for the VCO block, one can refer to section III-A, and particularly look at (11). As the transfer function of the f2V converter is (ideally) linear, it can be defined as a constant, $K_{F2Vconv}$, so (5) can be written as

$$w_{VCO} = \frac{1}{K_{F2Vconv}} \cdot (V_{in}) \tag{6}$$

From (6), it can be seen that the proposed VCO block will have a linear transfer function with a constant gain determined by f2V converter.

B. Simulation Results

In order to prove the concept, an example with verilog-A models is used in this section. For the simulations, both VCO and f2V converter are set to work at frequencies between 9 GHz and 11 GHz. For the f2V converter, voltages 0.5V and -0.5V corresponds to 9 GHz and 11 GHz, respectively, in order to have a reasonable sensitivity value, which is targeted in the application, so the input control voltage should be swept between -0.5V and 0.5V in order to move along the full f2V converter response.

The working principle of the system can be described as follows. When the FLL is settled, for example at the center frequency, the control voltage and the output of the f2V converter will add up to zero, and the oscillator output frequency will not change anymore. When a positive offset voltage is applied as the input control voltage, the voltage of the output of the adder will increase and, after integration, this will result in an increase in the output frequency of the oscillator. This increase will be detected by the f2V converter and will be converted as a negative voltage, because of the negative slope sensitivity. This way, the loop will stabilize again, when the input voltage of the integrator adds up to zero. So the new output frequency will correspond to another voltage-frequency point in the response of the f2V converter, which becomes the master of the loop. The steps explained can be followed in Fig. 2.

In Fig. 2, the first graph is the external control voltage, the second graph is the corresponding frequency detector output voltage, the third graph shows the output voltage of the adder, the fourth graph is the output of the integrator, and last graph is the output frequency of the proposed VCO block.

The comparison between the standalone VCO having a square root transfer function and the same VCO inside the FLL, which constitutes the frequency locked VCO (FLVCO), is done by applying the same input voltages to both and looking at the output frequencies. Input voltages between 0V and 3V are applied to both systems, and a divider and offset circuitry are placed in front of the VCO

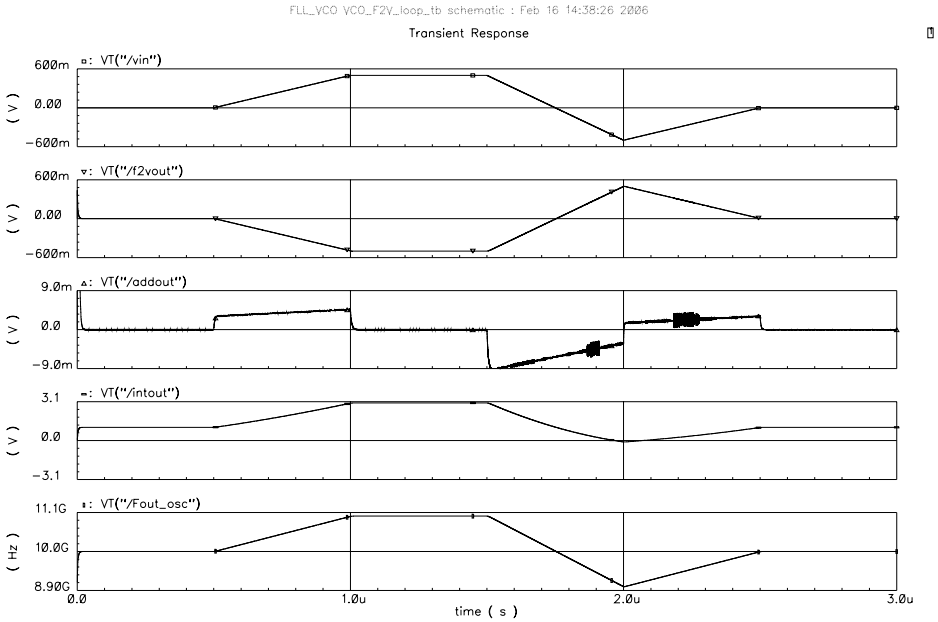

Fig. 2. The linear transient response of the VCO block to all kind of input control voltage transitions.

block to get the required voltage range at the input. The voltage-to-frequency responses and the derivatives of the responses are seen in Fig. 3. It is seen on the left that a square root function can indeed be converted to a linear transfer function, and on the right the slope of the VCO block transfer function is constant over the input voltage range, as desired.

III. Phase Noise Suppression

It is much faster to run phase noise simulations on phase-domain models, because high frequency variations associated with the voltage-domain models are not present in the phase domain. These models are suitable for phase noise simulations, so all components in the design are modeled in the phase domain, in order to show the phase noise suppression of the FLL. Noise contributions of the individual components are added to the models and the overall phase noise of the system is simulated.

In order to show the phase noise suppression in an ideal case, only the phase noise from the VCO is included in the models first. As seen in Fig. 4, with an ideal f2V converter, considerable phase noise suppression can be achieved.

After observing the phase noise suppression of the FLL

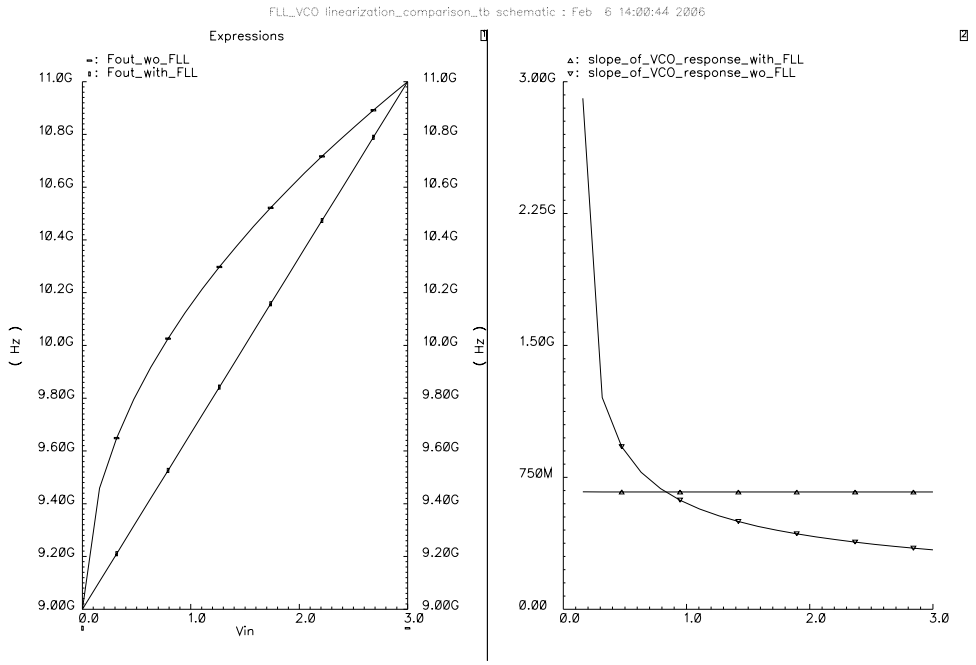

Fig. 3. a) Transfer functions of both VCO and FLVCO; b) Sensitivities (i.e., tuning ”constants”).

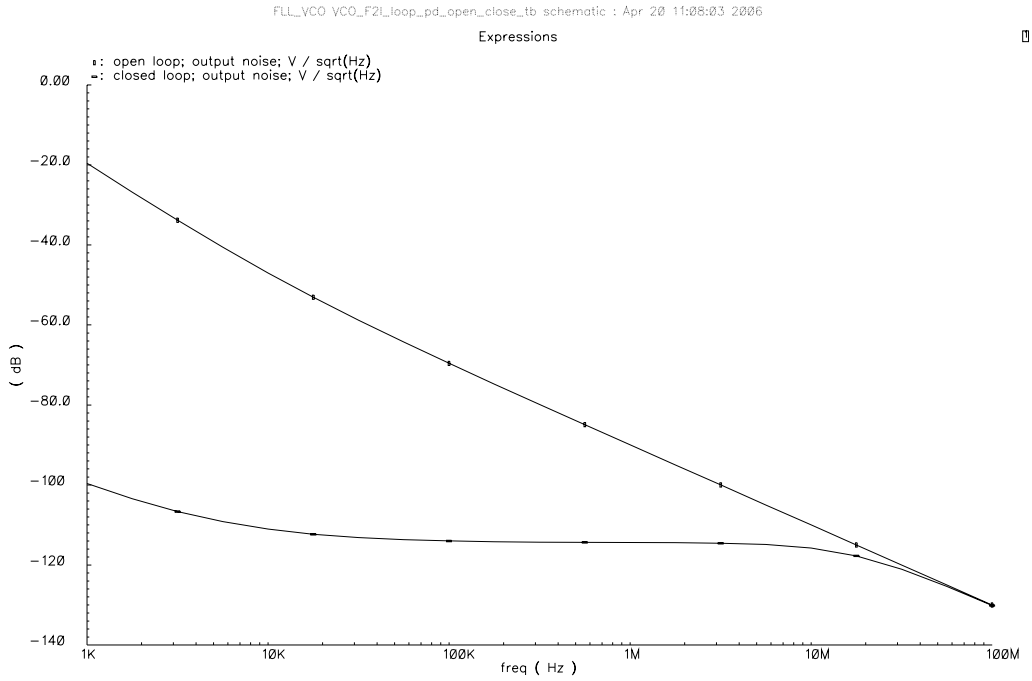

Fig. 4. Phase noise of FLVCO using noiseless phase domain models (lower curve) versus stand-alone VCO

in an ideal case, it is required to take into account the noise contribution from the f2V converter to see how it affects the suppression. F2V converter becomes the new master of the loop, also in terms of noise contribution, which will be evident from the equations in section III-B. In the next section design of the f2V converter will be described and the noise contribution will be shown.

A. Transistor Level Design of f2V Converter

After investigating several f2V converter topologies, the dual-slope detector is found to be the most suitable, in terms of low noise, acceptable detector gain within an acceptable frequency range, and high speed.

Slope detectors are the simplest type of frequency detectors. In spite of their simplicity, slope detectors are rarely used because of their poor linearity. It is necessary to look at the expression for the voltage across the LC tank in the slope detector, in order to understand why this is the case. Resonant frequency of the LC tank is defined as: $w_0 = \frac{1}{\sqrt{LC}}$, so the voltage of the LC tank is

$$V_{LC} = I_{LC} \cdot (\frac{w_{in}^2 - w_0^2}{w_{in}}) \cdot L \tag{7}$$

Since the frequency deviation of the FM signal is directly proportional to the amplitude of the modulating signal, the output of the slope detector will be distorted, because the output voltage is not directly proportional to the frequency deviation in (7).

Because of the poor linearity of single-slope detectors, a dual-slope detector is preferred, as shown in Fig. 5. Two LC tanks are designed, and resonance frequencies are set to approximately 9 GHz and 12 GHz, in order to cover the center frequency and required frequency range by giving a detector gain of acceptable value. The outputs of the two detectors have opposite signs because of the way they are connected to the amplitude detectors, and are subtracted from each other. This results in a linear region in between two frequencies, as seen in Fig. 6.

In order to understand how this circuit works, one can write the output voltage of the f2V converter as in (8), assuming that the contributions from parasitic resistances cancel out in the subtraction:

$$V(out) \approx \frac{w_{0f2}^2 - w_{0f1}^2}{w_{in}} \cdot L \cdot I_{LC} \tag{8}$$

If we express w_{in} in terms of the center frequency of the f2V converter w_0, plus a frequency change Δw, and use the approximation $\frac{1}{1+x} \approx 1 - x$ for small values of x, we obtain

$$V(out) \approx \frac{w_{0f2}^2 - w_{0f1}^2}{w_0} \cdot L \cdot I_{LC} \cdot (1 - \frac{\Delta w}{w_0}) \tag{9}$$

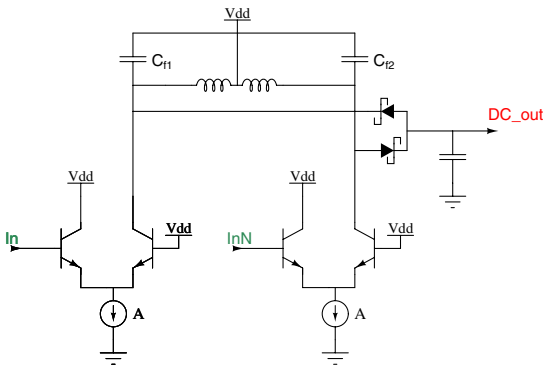

Fig. 5. Schematic of the dual-slope f2V converter.

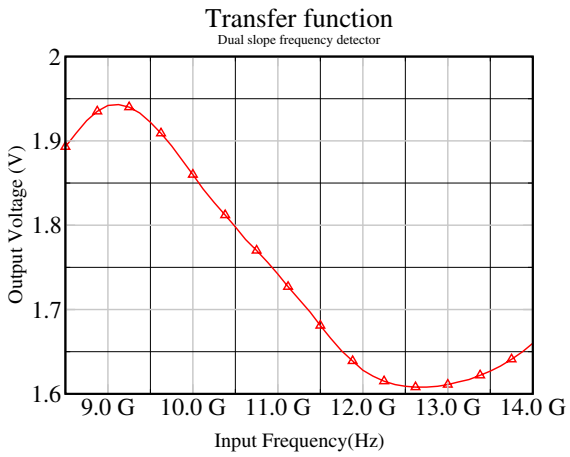

Fig. 6. Transfer function of dual-slope f2V converter.

If the dual-slope f2V converter gain is defined as

$$K_{det} = \frac{w_{0_{f2}}^2 - w_{0_{f1}}^2}{w_0} \cdot L \cdot I_{LC} \tag{10}$$

then $V(out)$ can be written as

$$V(out) = K_{det} \cdot (1 - \frac{\Delta w}{w_0}) \tag{11}$$

It is seen from (11) that dual-slope f2V converters possess a linear, negative-slope transfer function proportional to the input frequency change for frequencies near the center frequency. The layout of the dual-slope f2V converter is shown in Fig. 7. The output noise current floor of the designed detector is found as $0.27e^{-21}$ A^2/Hz for a 184 mV/GHz detector gain.

B. Phase Noise of the FLL

The noise contributions of each block must be added to the models as shown in Fig. in order to determine the overall phase noise of the FLL. 8. The forward gain of the loop is $K_{fwd} = K_{vco} \cdot H(s)/s$, where $H(s)$ is the loop filter response. The function of frequency-to-voltage converter is mathematically to differentiate the output phase of the VCO, finding the frequency and giving out the proportional voltage according to its gain factor. That's

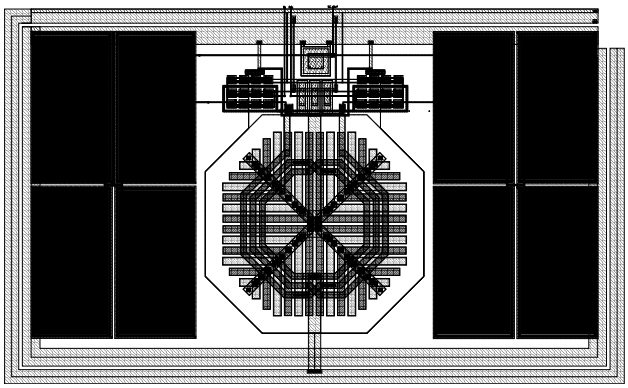

Fig. 7. Layout of the dual-slope f2V converter.

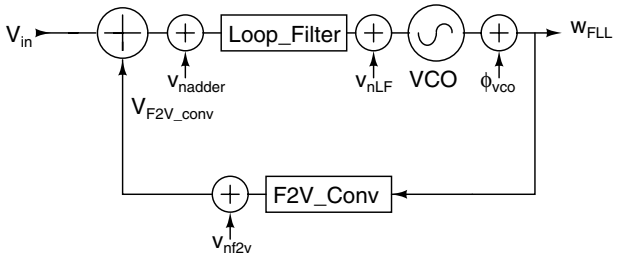

Fig. 8. Noise sources in a FLL

why, it can be described mathematically as $K_{f2v} \cdot s$, which is the inverse of the VCO transfer function. So, the loop gain is defined as $K_{loop} = K_{vco} \cdot K_{f2v} \cdot H(s)$. By using these definitions, the various noise transfer functions can be written as

$$G_{vco} = \frac{1}{1 + K_{loop}} \tag{12}$$

$$G_{f2V} = -\frac{K_{fwd}}{1 + K_{loop}} \tag{13}$$

$$G_{adder} = \frac{K_{fwd}}{1 + K_{loop}} \tag{14}$$

$$G_{LF} = \frac{K_{vco}}{1 + K_{loop}} \tag{15}$$

From these noise transfer functions, it can be seen that in the bandwidth of the FLL, the noise from the VCO is suppressed substantially by the loop, but there are additional noise contributions from the other elements of the loop, which are suppressed less. The VCO and the f2V converter are the most noisy components with most active elements, and the f2V converter noise is suppressed less than the VCO phase noise.

In addition, it can be seen that the noise contribution from the adder is added to the frequency detector noise and has a strong effect on the loop noise. As will be discussed in section IV, an explicit adder can be eliminated by current addition method.

C. Simulations Including f2V Converter Noise

After adding the noise contribution of the dual-slope f2V converter and the phase noise of a moderately noisy LC VCO, it can be seen from Fig. 9 that the phase noise of the proposed VCO block is approximately 15 dBc/Hz lower than the phase noise of standalone VCO inside the FLL bandwidth. During these simulations and investigations, it is observed that the phase noise of the overall VCO block depends heavily on the f2V converter noise performance, and that a noisy VCO can be much improved by using a low noise f2V converter, so while designing a FLL, in order to decrease the overall phase noise, more power should be used in the f2V converter instead of the VCO. Ultimately, it is the f2V converter to set the noise floor of the VCO block.

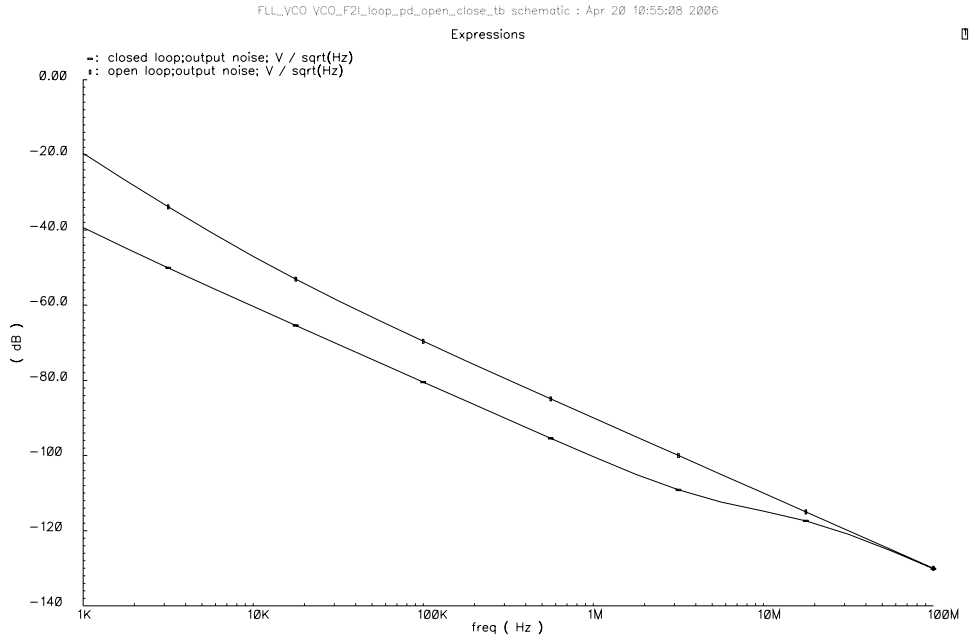

Fig. 9. Phase noise suppression using the dual slope f2V converter

IV. Implementation of a FLL inside a PLL

While implementing the FLL inside a PLL, the main concern is the stability of the loops. The bandwidths of the loops should be well separated from each other, in order not to interfere with each other. In this implementation, bandwidths are set 2 decades away from each other.

Two loops can be integrated either by a voltage adder that sums the output voltage of the phase frequency detector (PFD) filter and the f2V converter, as demonstrated in the FLL schematics in the previous sections, or by current addition method using a transconductance amplifier (TCA) to convert the output voltage of the PFD filter to a current. In the second method, after current addition in the connection point of the two loops, the final current is sent to the FLL filter, which can be implemented as in the Fig. 10. The choice between the two configurations depends on the noise contribution values of voltage adder and TCA used after the PFD filter. However; using TCA in the PLL loop gives us one more gain component in setting the PLL bandwidth.

A. Loop Transfer Functions

The zero of the f2V converter cancels the pole of the VCO inside the FLL, so the need for the zero realized by the the loop resistor is not existent in the FLL. There is a filter after the PFD in the final implementation, so the FLL resistor in Fig. 10 can be omitted in calculations. By using the definition $K_{f2I} = K_{f2v} \cdot K_{TCA}$, the FLL open-loop transfer function is

$$H_{FLL(OL)}(s) = \frac{K_{VCO} \cdot K_{f2I}}{C_{FLL} \cdot s} \tag{16}$$

As can be seen from (16), K_{f2I} and C_{FLL} can be used to set the bandwidth of the FLL, since K_{VCO} is the same for both loops. Using (16), the closed-loop transfer function is

$$H_{FLL(CL)}(s) = \frac{K_{VCO}}{s + \frac{K_{VCO} \cdot K_{f2I}}{C_{FLL}}} \tag{17}$$

The pole resulting from the VCO block is not at zero frequency, but at a frequency set by K_{VCO}, K_{f2I} and C_{FLL}. For the PLL, the only change is in the VCO transfer function, so the loop stability and bandwidth are not substantially affected by the proposed VCO block. The loop is even more stable.

B. Simulation Results

Fig. 11 shows the different noise contributions in the PLL. As seen in the graph, the region where the FLL is effective is for offset frequencies higher than the PLL bandwidth and lower than the FLL bandwidth. The standalone VCO phase noise is plotted with a dotted line, in order to show the noise suppression performed by the FLL.

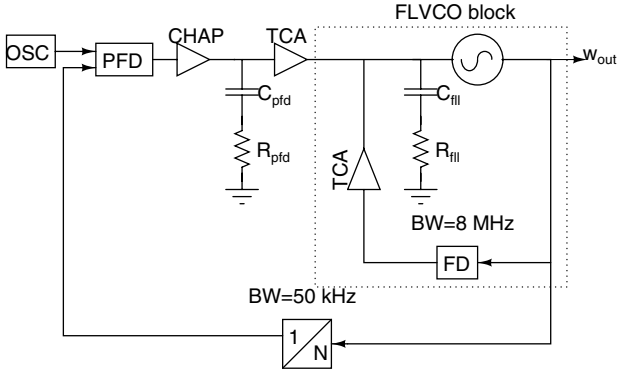

Fig. 10. Schematic of PLL including the FLL using TCAs

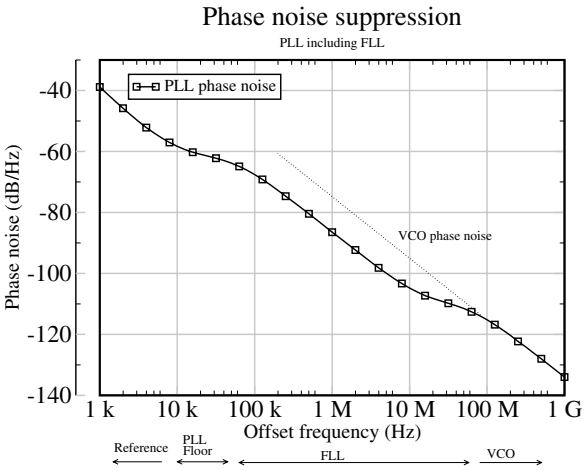

Fig. 11. Contribution of different parts to the overall PLL phase noise.

V. Conclusion

An on-chip frequency-locked loop (FLL) implementation over a VCO in a PLL has been investigated. Advantages in terms of linearity and phase noise suppression are demonstrated with both theoretical calculations and numerical simulations using Verilog-A models, including realistic noise models from transistor level designs.

The final design has not been implemented on chip yet, but it was proved by simulations that using the proposed approach, linearization can easily be achieved, and phase noise suppression may be achieved depending on the phase noise of the f2V converter. The technique is particularly promising when inverter-ring VCOs are used. The component-level implementation of a low-noise frequency-to-voltage converter that does not require a reference frequency has also been presented.

Acknowledgment

The authors would like to thank analog/high-speed group at Intel Copenhagen for their valuable discussions and support.

References

[1] J. Gustrau, F. Fiechtner, and M. Hoffmann, "VCO Linearisation by Frequency Feedback," in *IEEE Radio Frequency Integrated Circuits Symposium*, June 1998, pp. 135–138.

[2] R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold, "A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones," in *Proc. IEEE International Solid-State Circuits Conference*, no. 11, Nov 2005, pp. 2203–2211.

[3] B. Giebel, J. Lutz, and P. L. OLeary, "Digitally Controlled 0scillator," in *Proc. IEEE International Solid-State Circuits Conference*, no. 6, Jun 1989, pp. 2203–2211.

[4] N. M. Pletcher and J. M. Rabaey, "A 100 μW 1.9GHz Oscillator with Fully Digital Frequency Tuning," in *Proceedings of ESSCIRC*, Sep 2005, pp. 387–390.