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Two-Phase Interleaved Buck Converter with a new Digital Self-Oscillating Modulator

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Abstract— This paper presents a new Digital Self-Oscillating Modulator (DiSOM) for DC/DC converters. The DiSOM modulator allows the digital control algorithm to sample the output voltage at a sampling frequency higher than the converter switching frequency. This enables higher control loop bandwidth than for traditional digital PWM modulators given a certain switching frequency. A synchronised version of the DiSOM modulator is derived for interleaved converters. A prototype interleaved Buck converter for Point of Load applications has been designed and built to test the performance of DiSOM modulator. The DiSOM modulator and a digital control algorithm have been implemented in an FPGA. Experimental results show that the converter has a very fast transient response when a loadstep is applied to the output. For a loadstep of 50% of nominal output current the output voltage overshoot is less than 2.5% of the nominal output voltage and the settling time is just 8 switching periods.

I. INTRODUCTION

To design a digitally controlled DC-DC converter with fast transient response is a big challenge even though great advances have been made in the last decade. One of the main limitations in a digital controller for a DC/DC converter is the PWM modulator. Many papers have been published about digital modulators that solve either the limit cycling problems due to clock frequency quantization or the problem of how to obtain high control loop bandwidth in a digitally controlled DC/DC converter [1-3]. It can generally be said for the previously published work that the switching frequency is increased in order to increase the control loop bandwidth. This is due to the fact that the digital PWM modulators only allow the sampling frequency of the digital controller to be equal to but not higher than the switching frequency. This limitation has come into play as advanced implementations of the control law, e.g. a digital PID compensator, has reduced the computation time. Previously the main limitation was due to computational delays because microcontrollers or slow DSPs were used [4]. This paper introduces a new Digital Self-Oscillating Modulator (DiSOM) [5] that has the advantage that the digital controller can sample the output voltage at a higher sampling rate than the converter switching frequency thereby allowing the control loop bandwidth to be increased without increasing the switching frequency. A synchronised DiSOM modulator is introduced allowing the

DiSOM to be used in interleaved DC/DC converters. A prototype two-phase interleaved Buck converter has been built and tested with the synchronised DiSOM modulator.

II. DiSOM -DIGITAL SELF-OSCILLATING MODULATOR

The Digital Self-Oscillating Modulator is a new invention that covers a whole family of digital modulators, which are all self-oscillating by nature. The simplest form of the DiSOM modulator is shown in Fig. 1. It consists of a comparator with hysteresis (the red box in Fig. 1), a main forward block (MFW, the blue box in Fig. 1) configured as an integrator and a main feedback block (MFB, the green box in Fig. 1) that performs a simple multiplication. The reference signal Ref sets the duty cycle and is subtracted from the output signal of the MFB. According to the invention the MFB and MFW can both be frequency dependent and can be implemented as any kind of digital filter. By choosing other characteristics for the MFB and MFW the characteristics and performance of the DiSOM modulator can be changed. The modulator could for instance be designed to suppress quantization errors in the low-frequency band, as known from noise-shapers in class-D audio amplifiers and D/A converters. The comparator with hysteresis generates the switching output by comparing the output of the integrator to either of the hysteresis limits depending on the state of the switching output.

The output of the integrator will be a triangular waveform under steady state conditions. It can be shown that the switching frequency of the DiSOM modulator shown in Fig. 1 is given by equation (1), where n is the number of bits that is used to represent the reference input, $Window$ is the hysteresis window and T_{clock} is the period time of the clock that runs the DiSOM modulator.

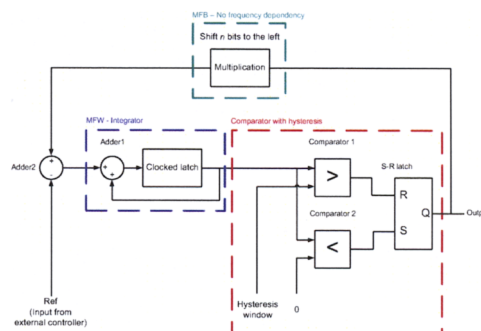


Fig. 1: A block diagram of the DiSOM modulator

$$f_{sw}(D) = \frac{2^n}{Window \cdot T_{clock}} \cdot (D - D^2) \quad (1)$$

Fig. 2 shows a typical plot of the switching frequency versus duty cycle, where the duty cycle (D) is normalised from 0 to 1. The big advantage of the DiSOM modulator over traditional PWM modulators is that the duty cycle command, i.e. the Ref input set by the digital compensator, doesn't directly affect the PWM output as it would in traditional digital PWM modulators based on a counter and comparator. Thereby unwanted transitions on the PWM output can be avoided when the duty cycle command is updated. If the duty cycle command for the DiSOM modulator, i.e. the Ref input, is changed during a switching cycle it will change the slope of the triangular waveform on the output of the integrator, but it will not instantaneously affect the PWM output. It is therefore possible for the digital compensator, which controls the output voltage, to sample the output voltage at a higher frequency than the switching frequency and update the duty cycle command at the same rate as the sampling frequency. By increasing the sampling frequency it will be possible to obtain a higher control loop bandwidth for the digitally controlled DC/DC converter, without increasing the switching frequency of the system.

III. SYNCHRONISATION OF THE DiSOM

The DiSOM modulator described in the previous section is very well suited for a typical DC/DC converter such as a Buck converter, but it isn't directly applicable to interleaved converters. The problem is that the switching frequency changes with the duty cycle, which means that the period time of the PWM signal isn't constant. The challenge then is how to ensure that the phases in an interleaved converter have the correct phase shift relative to each other, e.g. 180 degrees phase shift in a two-phase interleaved Buck converter. The solution used in the prototype converter presented in this paper is to replace the comparator with hysteresis with a clocked comparator as shown in Fig. 3. The comparator has a synchronising input, and the PWM output will transition from low to high on the positive edge of the synchronising signal. When the integrator output is equal to the hysteresis window the PWM input will transition from high to low. The principle of operation is illustrated in Fig. 4 for duty cycle values of 0.125, 0.25 and 0.375, where the "carrier" is the output of the integrator.

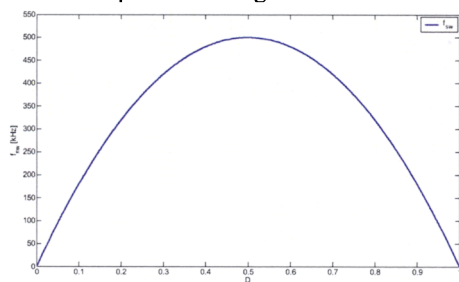


Fig. 2: Switching frequency v.duty cycle for the DiSOM

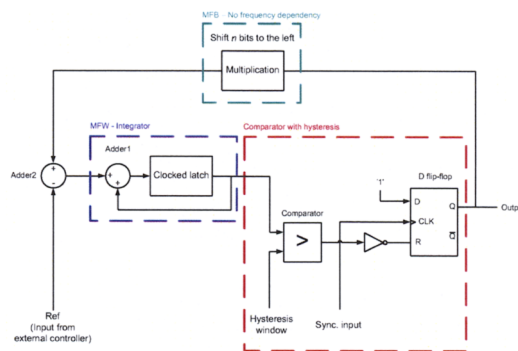


Fig. 3: DiSOM modulator with synchronisation input

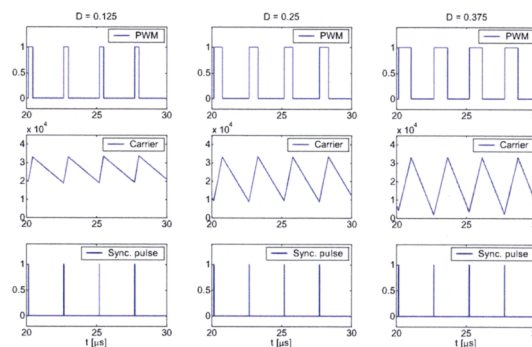


Fig. 4: Carrier and PWM signals for the synchronised DiSOM modulator

It should be noted that by adding synchronisation to the DiSOM modulator we introduce a limitation to the PWM output. The duty cycle is now limited to the range from 0 to 0.5, which is similar to the duty cycle limitation known from analogue peak current mode control. The problem can be solved by digitally adding a negative slope to the integrator output if the converter design requires duty cycles larger than 0.5. With the new synchronised DiSOM modulator it is possible to generate phase shifted PWM signals by phase shifting the synchronisation signal for each modulator. A block diagram showing how two synchronised DiSOM modulator can be used to create interleaved control signals for two Buck stages is shown in Fig. 5. The timing is controlled by a counter and the synchronisation pulses are generated by comparing the counter value to preset phase delays. The digital PID compensator sets the same duty cycle for both synchronised DiSOMs. In most digital control schemes for interleaved Buck converters the output voltage is sampled at the same rate as the per phase switching frequency effectively limiting the control loop bandwidth to the same bandwidth as would be achievable in a single phase Buck converter switching at the same frequency. Ref [1] proposes a digital control scheme where the sampling frequency is equal to N times the per phase switching frequency, where N is the number of phases of the interleaved converter. The control loop bandwidth can in that case be significantly increased, but the simulations and measurements shown in [1] shows a lot of noise on the output voltage during transient conditions. The noise is to a large extent attributable to the very high

sampling frequency of the output voltage control loop and the fact that the duty cycle of the separate phases in the interleaved converter differs during the transient condition.

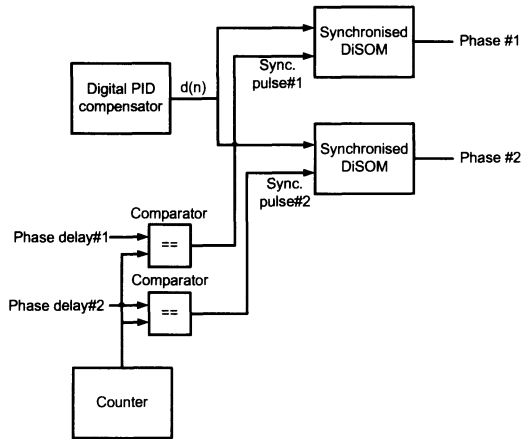


Fig. 5 Interleaving of multiple synchronised DiSOM modulators

IV. IMPLEMENTATION OF DIGITAL PID COMPENSATOR WITH SHORT COMPUTATION TIME

When designing a digital controller for a high bandwidth DC/DC converter it is important to keep the time delays to a minimum, since any delay causes negative phase shift in the control loop. The negative phase shift will have to be compensated for in the control loop design and will very often limit the performance. There are three main contributors to the delay in the digital controller. The first contributor is the PWM modulator, which for a typical uniformly sampled digital PWM modulator has the transfer function

$$G_{PWM}(s) = \frac{e^{-sDT_s}}{C_{PK}} \quad (2)$$

where D is the duty cycle of the PWM signal, T_s is the period time of the PWM signal and C_{PK} is the amplitude of the digital carrier generated by a counter [6].

The other two contributors to the time delay in the digital controller is the ADC sampling time and the time it takes to compute the digital control law, e.g. a digital PID compensator. The design of a digital PID compensator in VHDL for implementation in an FPGA can help reduce the delay time compared to implementations in a Digital Signal Processor/Controller (DSP/DSC) such as the TMS320F2801 [7].

Fig. 6 and 7 shows a block diagram and a timing diagram respectively for the digital PID compensator used in the prototype presented in this paper. The PID compensator of Fig. 6 implements the transfer function $G_c(z)$ (see equation (3)), which has two zeros and an integrator in the frequency domain.

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \quad (3)$$

The digital implementation of the PID compensator calculates the difference equation (4).

$$d(n) = d(n-1) + b_0 \cdot e(n) + b_1 \cdot e(n-1) + b_2 \cdot e(n-2) \quad (4)$$

where $d(n)$ is the duty cycle command for the two synchronised DiSOM modulators, $d(n-1)$ is the duty cycle command of the previous sample and $e(n)$, $e(n-1)$ and $e(n-2)$ is the present and two past samples of the error signal, i.e. the difference between the digital reference and the sampled output voltage.

To explain the operation of the digital PID compensator each block in the block diagram will be explained in the following description.

- **Decoder** – The decoder takes the input from a 10 bit ADC and reduces the resolution to 6 bits centered around the digital reference, which defines the output voltage. The ADC input is 10 bits because the FPGA development board used in the experimental work had a 10 bit pipelined ADC installed. The decoder updates the error signal $e(n)$ when the Read_ADC signal transitions from low to high.
- **The sequencer** is a simple state machines that generates the control signals for the remaining blocks of the PID compensator. The sequencer has a state variable that is generated by a counter, which counts from 0 to 62 and then resets to 0. The counter is clocked by a 50MHz clock and the operation of the PID compensator is synchronised to the counter. The resulting sampling frequency is equal to 794 kHz.
- **The 20-bit adder and the 20-bit register** works as an accumulator. The accumulator can take the previous result on the output of the accumulator and add it to the result on the output of the 6x14 bit multiplier or the sequencer can preload the duty cycle $d(n-1)$ that is read from the limiter.
- **The 6x14 bit multiplier** is used to multiply an error signal with its corresponding coefficient, e.g. $e(n)$ and b_0 . The coefficients b_0 , b_1 and b_2 are represented as 14 bit numbers. The 5 least significant bits represents fractions of 1 and the most significant bit is a sign bit. All calculations are performed using 2's complement binary numbers. The remaining 8 bits allows the coefficients to take on values in the range from -256 to $+256$. In a typical DSP both inputs on the multiplier would have the same word length but that increases the complexity of the multiplier. The idea of limiting the word length of one input to match the error signal is presented in [8] with the purpose of reducing the

complexity and cost of the digital compensator logic.

- The two multiplexers (labelled 3-1 MUX) are used to select, which error signal and coefficient is fed to the inputs of the multiplier. Both multiplexers are controlled by the 2-bit Mux_sel signal.
- The two 6-bit registers stores the error signals $e(n-1)$ and $e(n-2)$. The registers reads and stores the input signal on the rising edge of the control signal, i.e. Update_e1 and Update_e2.
- The limiter reads the output of the accumulator and limits it to duty cycle values between 0 and 0.5 on the rising edge of Update_D.

The digital PID compensator has a delay of two clock cycles from the ADC input is read by the decoder until the duty cycle command is updated by the limiter. The ADC is a 10-bit pipelined ADC with a sampling delay of 6 clock cycles. Both the ADC and the digital PID compensator is clocked by a 50 MHz clock and the total delay is 8 clock cycles, which makes the delay 160 ns.

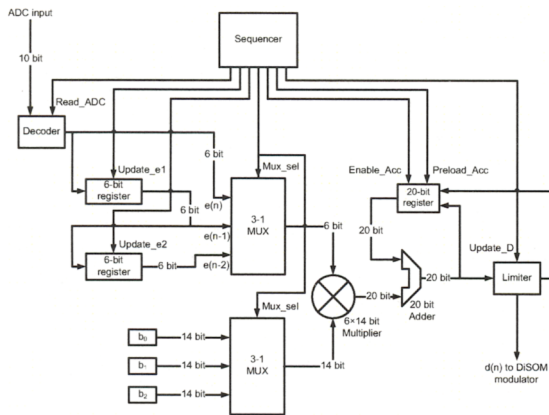


Fig. 6 Block diagram of the digital PID compensator implemented in an FPGA

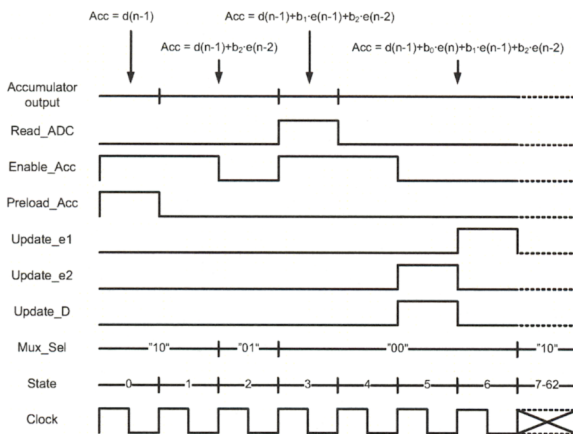


Fig. 7 Timing diagram for the digital PID compensator

The disadvantage of the digital PID compensator described above is that it can not be changed easily. If for example the

designer wants to add an extra zero or a pole to the transfer function the VHDL code will have to be modified and the design has to be simulated and tested once again. Compared to a more traditional DSP design [9], where it is a matter of rewriting a piece of assembly or C code, it is a much more challenging task to change the VHDL design.

V. EXPERIMENTAL RESULTS

A two-phase interleaved buck converter has been designed and built to verify the performance of the synchronised DiSOM modulator. The specifications of the hardware prototype are given in Table 1. The output capacitor is in fact eight 100 μ F ceramic capacitors (X5R) for low ESR. A picture of the prototype is shown in Fig. 8.

The DiSOM modulators and the digital compensator are implemented in an LCXMO1200 FPGA from Lattice Semiconductor. The ADC used in the design is the ADC10065 from National Semiconductors.

TABLE 1
PROTOTYPE SPECIFICATIONS

Parameter	Value
Input voltage	9 – 15V
Output voltage	2.0V
Output current	0 – 20A
Inductor size	1.5 μ H
Output capacitance	800 μ F
Switching frequency per phase	400 kHz
Sampling frequency	800 kHz

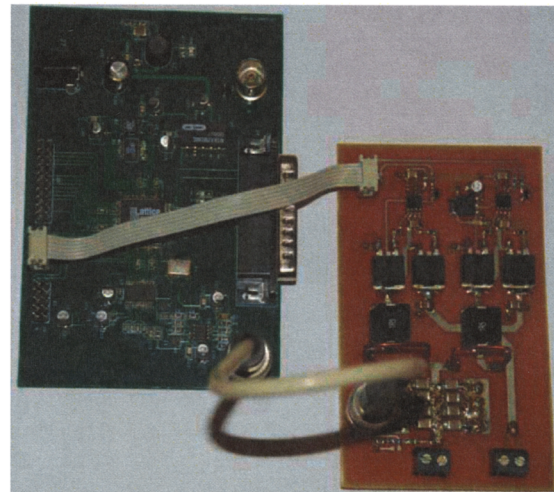


Fig. 8: Prototype POL converter board (Right) and FPGA development board (left)

A MATLAB/SIMULINK model of two-phase interleaved Buck converter and the digital controller was used to simulate the design. The Buck converter model takes into account parameters such as capacitor ESR, inductor series resistance and the MOSFET driver propagation delay.

Fig. 9 shows a comparison of the simulated and measured open loop gain of the interleaved Buck converter. The

simulated loop gain is found by injecting a sinewave into the control loop at the converter output in the same way as the loop gain is measured by a Gain/Phase analyser. The loop gain measurement shows that the open loop bandwidth of the interleaved Buck converter is 41 kHz and the phase margin is 56 degrees.

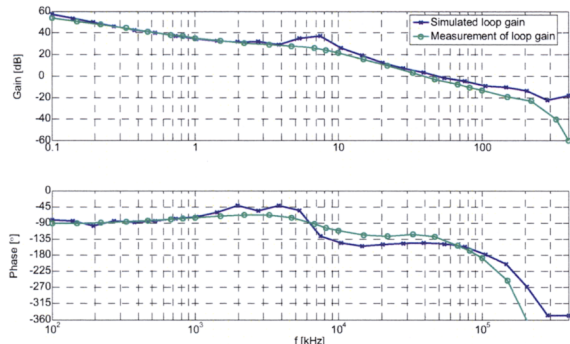


Fig. 9 Open loop gain simulation and measurement

Simulations of the output voltage response to a load step from 10 to 20A for two different current slew rates (see Fig. 10) shows that the output voltage deviation from the steady state voltage of 2.0V is 50mV for a current slew rate of 1000A/μs. If the load step has a first order lowpass response with an average slew rate of 1A/μs the output voltage deviation is approximately 40mV. The settling time is approximately 15μs for the slow load step and 20μs for the fast load step.

Fig. 11 shows the measured output voltage response to a loadstep from 10 to 20A. The output voltage deviation is less than 50mV and the settling time is less than 20μs. The electronic load used in the measurement limits the current slew to approximately 1A/μs and the measurement is comparable to the blue trace in Fig. 10. The measured output voltage deviation is slightly larger than the simulation result and the settling time is also slightly longer. The difference between simulation and measurement can be due to component tolerances and poor PCB design.

Fig. 12 shows a steady state measurement of the output voltage at nominal output current. The output voltage has some fluctuations, which isn't the ripple voltage generated by the ripple current in the inductor. Part of the explanation is the relatively low ratio between the per phase switching frequency and the clock frequency of the synchronised DiSOMs. The ratio between switching and clock frequency is 1/126, which corresponds to a PWM duty cycle resolution of 7 bits. The resolution of the duty cycle command of the digital PID compensator is 10 bits. The reason that the fluctuations on the output voltage have an amplitude of less than 10 mV peak to peak is the nature of the synchronised DiSOM modulator. The DiSOM is a closed loop system that feeds back the PWM signal and compares it with the duty cycle command and the integrator will suppress the low frequency errors. The DiSOM is in that sense similar to sigma-delta modulators that shapes the quantisation noise in

such a way that noise power is low at low frequencies and increases at high frequencies.

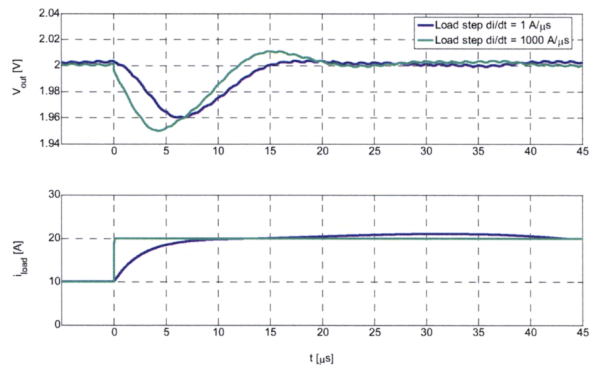


Fig. 10 Simulated load step response for $V_{in} = 12V$

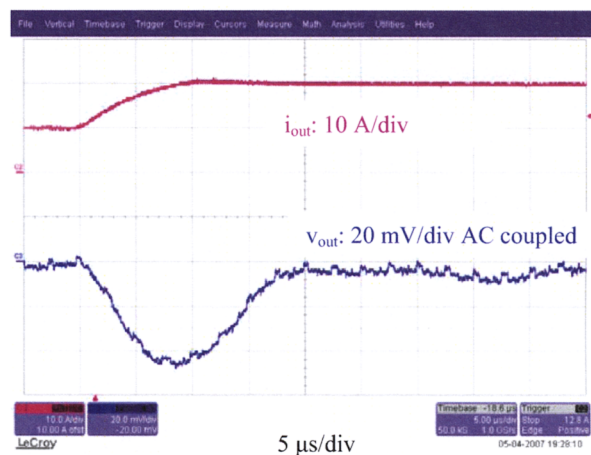


Fig. 11: Positive loadstep 10A to 20A $V_{in} = 12V$

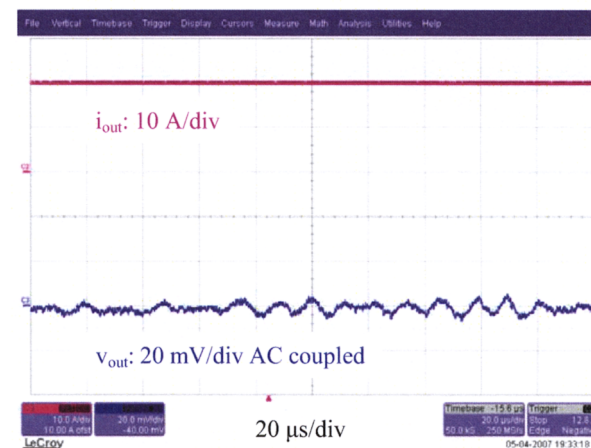


Fig. 12 Steady state measurement of the output voltage for $I_{out} = 20 A$

VI. CONCLUSION

This paper describes a two-phase interleaved buck converter with very fast transient response. A new digital modulator, called the DiSOM modulator is described and a synchronised DiSOM modulator is derived. A prototype

2.0V 20A two-phase interleaved Buck converter has been built to test the proposed modulator. The output voltage response, to a loadstep of 50% of the nominal output current, is less than 2.5% of the nominal output voltage. The settling time after a loadstep is less than 20 μ s, which corresponds to just 8 switching cycles.

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