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Packaging Aspects of Photodetector Modules for 100 Gbit/s Ethernet Applications

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***Abstract* — Packaging is a major problem at millimetre-wave frequencies approaching 100 GHz. In this paper we present that insertion losses in a multi-chip module (MCM) can be less IL < 0.6 dB at 100 GHz. The paper also analyzes in detail resonance modes in the packages. The characteristic of conductor-backed coplanar waveguides (CBCPWs) with vias is accurately analyzed using 3D electromagnetic (EM) simulation over a wide frequency range. Patch antenna mode resonances are identified as a major origin of resonances in simulated and measured transmission characteristics of the CBCPW with vias. Based on EM simulations, we propose several optimized arrangements for vias and bonding wires placement, to efficiently suppress the resonances and achieve excellent transmission performance of the PD module packaging. Based on our simulated results we postulate that it is possible to obtain resonance-free electrical transmission in the PD package with IL < 0.6 dB over a frequency from DC to 110 GHz.**

I. INTRODUCTION

High-speed multi-gigabit networks are essential for future large volume data transmission. 100 Gbit/s single channel Ethernet systems is considered to be the next generation of Ethernet application after the 10 Gbit/s Ethernet standard [1]. The optoelectronic transceiver working at the rate of 100Gbit/s is crucial for realizing 100 Gbit/s Ethernet systems. The EU FP6 project, GIBON, aims at developing the components for the 100 Gbit/s transmitter and receiver Ethernet system, partial results of which are shown here. The packaging of these high-speed components is very challenging when aiming at the rate of 100 Gbit/s, especially due to the multi-chip module (MCM) structure involving several chip-to-chip and/or chip-to-substrate transitions. In this paper we concentrate on the packaging aspects of the high-speed receiver front-end comprised of a high-speed PD with monolithically integrated fibre-connection and a MCM electrical connection.

There exist several methods to realize high-speed interconnects inside an MCM package. The most frequent solutions are wire-bonding and flip-chip interconnects. Generally, wire-bonding is regarded to be technologically easier to process, however, is not considered to be efficient at millimetre-wave frequencies. On the other hand, flip-chip interconnect technology has proven to exhibit low insertion losses, but at the expense of more complex technology. In this paper we show that wire bonding can be efficiently used up to 110 GHz with very low losses, comparable or even lower than the flip-chip insertion losses.

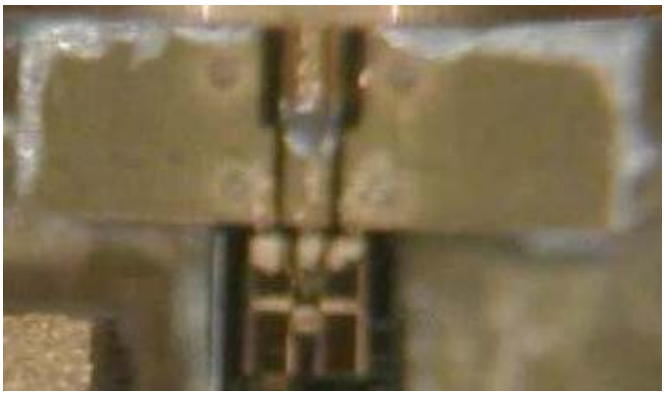


Fig. 1 Micrograph of the packaging of the photodetector module as well as the photodetector chip.

Photodetectors (PD) modules are typically packaged using conductor-backed coplanar waveguides (CBCPWs) to connect the PD chip to a coaxial connector. An illustration of the whole packaging structure is shown in Fig. 1.The pin of the 1 mm coax connector [2] is directly soldered onto the centre conductor of the CBCPW with vias to suppress losses. The upper ground planes are soldered to the outer conductor of the connector. This contact is important to obtain good transmission characteristic in the low frequency range and also shorts the gap between the CBCPW and the connector to reduce unexpected coupling effects. Bonding wires are utilized to connect the PD chip and the CBCPW.

The packaging structure including the bonding wires, the CBCPW with vias and the transition between the coaxial connector and the CBCPW, is currently limiting the frequency performance of packaged PD modules. Down-scaling of the geometrical dimension of the CBCPW for improved millimetre-wave performance is limited by the coaxial connector dimensions and by fabrication restrictions.

Developing vias in the CBCPWs is considered to be an alternative way to effectively improve the bandwidth of the packaging structure. A branch of bonding wires is another main transition in the packaging structure influencing the bandwidth. Therefore, the CBCPW with vias and bonding wires should be optimized for the wideband requirement.

II. EM Analysis of CBCPWs with Vias

The backside metallization of CBCPWs increases the ability of heat sinking, shielding and mechanical strength of coplanar circuits [3]. However, the backside metallization can couple to the upper ground planes of the CBCPW through undesired parallel plate mode, which propagates along the waveguide [4] or generates patch antenna mode resonances [5]. These higher order propagating modes and resonances seriously degrade the transmission performance for wideband applications.

A popular way to suppress the coupling effect is to utilize metallic vias to short-circuit the upper ground planes with the backside metallization. However, higher order resonances can not be suppressed efficiently if vias are placed randomly [6], which requires systematic design of the via arrangement.

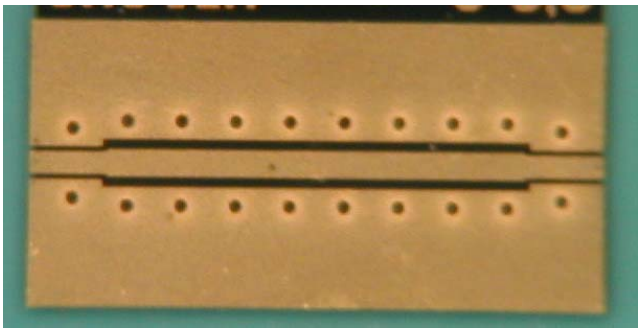


Fig. 2 The CBCPW with vias under investigation

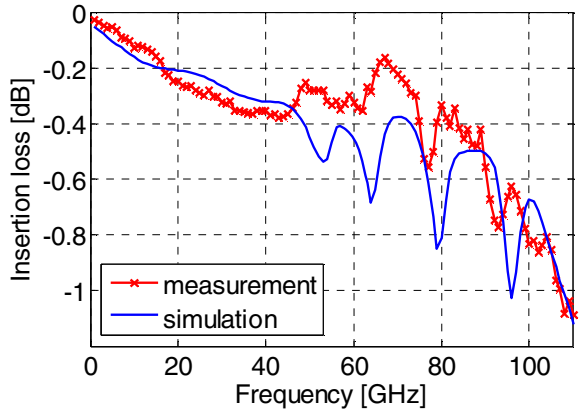
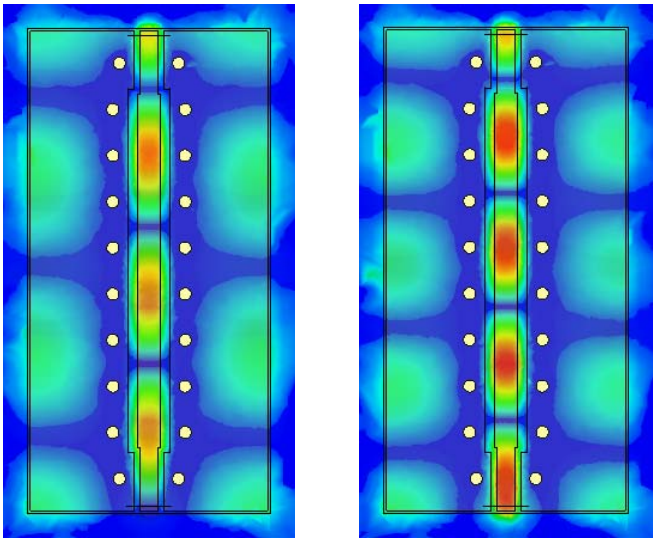


Fig. 3 Measured and simulated insertion losses of the CBCPW with vias

A CBCPW with vias, part of which will be used later in the packaging of the PD module, is shown in Fig. 2. The material of the substrate is quartz, and the conductor is gold. It is seen that the vias are placed close to the gap in the CBCPW structure and the distance between vias from center to center is kept minimum. Such an arrangement is designed to confine the transmitted electromagnetic (EM) energy to within the CBCPW structure and achieve optimal transmission characteristic [6]. However, this approach changes the characteristic impedance of the CBCPW, which has to be readjusted to achieve 50 Ω transmission line properties.

A 3D EM simulation tool, Ansoft HFSS, is utilized to perform the optimization of the via placement in the CBCPW structure. The accuracy of the EM simulation results is evaluated by comparing measured and simulated insertion loss of the CBCPW with vias is shown in Fig. 3. It is crucial to employ lumped ports in HFSS simulations in order to accurately excite the CBCPW resembling the measurement setup with GSG probes. The simulation results have been calibrated using the method described in [7].

Although the simulated insertion loss does not exactly overlap the measured one, the main features of the measured insertion loss are still accurately captured by the simulations. Some notch frequencies are observed in the both measured and simulated characteristics. Fig. 4 shows the electric fields (E-fields) in the substrate at two notch frequencies in the simulated insertion loss, which are at 79 GHz and 96 GHz, respectively. The E-field patterns exhibit typical patch antenna mode resonances.



(a) (b)

Fig. 4 The electric-field pattern in the substrate of the CBCPW with vias: (a) at 79 GHz; (b) at 96 GHz;

The resonance frequencies can be predicted analytically by

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon_r}}\left[\left(\frac{m}{w}\right)^2 + \left(\frac{n}{l}\right)^2\right]^{0.5} \quad (1)$$

where ε_r is the relative permittivity of the substrate, c is the velocity of the light in vacuum, w and l are the width and length of effective patch antennas, and m and n are the order numbers of resonances. For the cases shown in Fig. 4, m is 0.5 and n is 3 for 79 GHz and 4 for 96 GHz, respectively. The measured, simulated and analytical resonance frequencies are listed in the Table I, using w = 700 μm representing the

distance from the center of the vias to the edge of the upper ground planes, and l = 3950 µm. The resonance frequencies derived from the three different methods agree well with each other. It is evident that the vias can not eliminate the resonances completely, although they are placed very close to the slot of the CPW structure.

TABLE I
RESONANCE FREQUENCIES COMPARISON

Freq.	Measurement	HFSS	Analytical
$f_{0.5,3}$ (GHz)	77	79	80.4
$f_{0.5,4}$ (GHz)	93	96	95.6

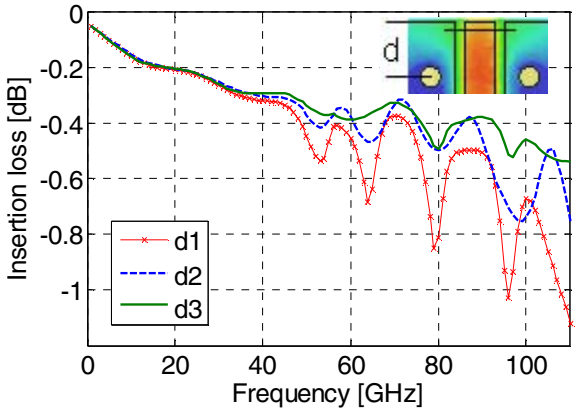


Fig. 5 Simulated insertion losses of the CBCPW with vias for decreasing distance (d1 > d2 > d3) between the end vias and the end of CBCPW is parametrically analysed.

Fig. 4 reveals that the CBCPW mode energy leaks at the end of the CBCPW with vias to the patch antenna resonances. The impact of the distance *d*, which is indicated in the inset of Fig.5, between the end-via to the edge of the CBCPW, has been carried out, as depicted in Fig.5. It demonstrates that the closer the end-vias are placed to the edge of the CBCPW structure, the lower insertion loss and less significant resonances are visible. It is concluded that the energy leakage can be inhibited by placing vias close to the edge of the CBCPW structure. Moreover, the energy leakage can also take place between vias if the distance between these is sufficiently large and should therefore be also chosen appropriately for the highest frequencies of operation.

III. EM ANALYSIS OF THE FULL PACKAGED MODULES

Our previous work, [8], investigated potential resonances due to the CBCPW alone without taking into account of the PD chip itself. Fig. 6 shows the HFSS simulation model for the new PD module packaging including the PD chip, bonding wires, the CBCPW with vias and the 1 mm coaxial connector. It resembles the real packaging structure as shown in Fig. 1. The photodiode in the PD chip is modelled by a lumped port as illustrated in the inset of Fig. 6. The bonding wire interconnect is modelled using rectangular Au structures of appropriate dimensions. Vias arrangement in the CBCPW can be recognized in Fig. 6. The 1mm coaxial connector is modelled by ideal coaxial cable line. Therefore, the loss due to the connector itself is ignored in the packaging model.

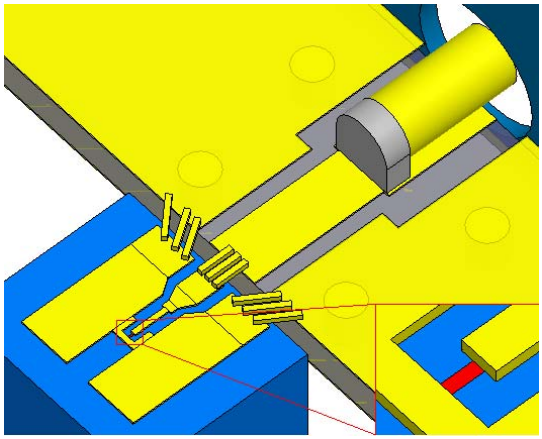


Fig. 6 HFSS model to investigate the insertion loss of the photodetector module packaging. The inset shows how a lumped port sits between anode and cathode acting as a photodiode.

Several cases have been analyzed using EM simulations and the results are presented in Fig.7. As outlined above, vias can not completely eliminate the resonances in the CBCPW transmission characteristics due to the energy leakage at the end of the CBCPW. The simulated insertion loss for the packaging structure illustrated in Fig.6 is shown in Fig.7 as the case1. Although no obvious resonances exist in the insertion loss characteristic a strong E-field at the edge of CBCPW is visible at 77 GHz, as shown in Fig. 8 (a). The pattern can be recognized as the patch antenna mode with both order numbers being 0.5. In spite of the leakage the insertion loss is less than IL<1dB up to 110 GHz.

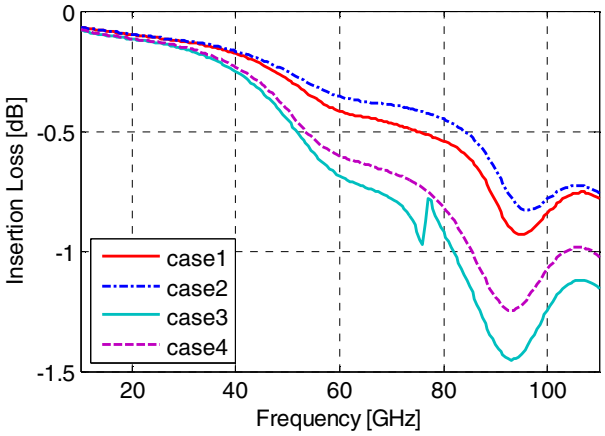
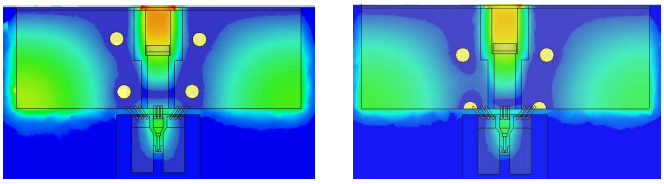


Fig. 7 The simulated insertion losses for the different packaging structures; case1: originally from Fig.6; case2: the end-vias are moved to the end of the CBCPW; case3: only one bonding wire connects each output pad of the chip to the CBCPW; case4: only one bonding wire connects each output pad of the chip to the CBCPW while the end-vias are at the end of CBCPW.

In order to prevent the energy leakage from the CBCPW mode to the substrate resonances, the end-vias are moved to the edge of CBCPW while keeping the distance between vias at the minimum value limited by fabrication technology. The insertion loss of the packaging structure with such optimization is shown in Fig. 7 as case2 and improves the insertion loss of the package by around 0.1 dB from 40 GHz

to 110 GHz. However, the resonance is not eliminated completely by the optimization as shown in Fig. 8 (b). The EM energy still leaks between vias as well as the gap between the PD chip and the CBCPW. Further EM simulations demonstrate that EM energy leakage between vias can be completely eliminated by placing more vias in the substrate.



(a) (b)

Fig. 8 (a) E-field of the original packaging structure at 77 GHz; (b) E-field of the packaging structure with the optimized vias arrangement at 77 GHz.

In the above simulations we have employed three bonding wires on each output pad of the PD chip for the chip-to-chip transition. The number of bonding wires is critical to the insertion loss of the package. Instead of three bonding wires on each pad, an interconnect with one bonding wire has also been studied in Fig. 7 as case3. Compared to the cases with three bonding wires, the insertion loss in this case is at least 0.5 dB higher independent of the optimization of the vias in the substrate, as indicated by the case 4 in Fig. 7.

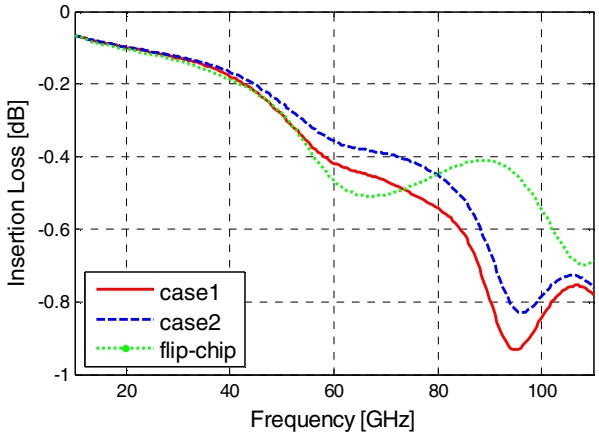


Fig. 9 Simulated insertion loss of the package with flip-chip transition instead of bonding wires. It is compared directly with the insertion losses in both case1 and case2 described in Fig.7.

The packaging structure with flip-chip transition from the PD chip to the CBCPW is investigated. An EM simulation model of the structure is built in HFSS and the simulated insertion loss is illustrated in Fig. 9. In general, the insertion loss of the package with flip-chip transition is comparable to the ones with bonding wires. The optimized package with bonding wires even exhibits lower insertion loss below 80 GHz.

IV. Conclusion

The paper presents very low-loss interconnect techniques for transition from chip to coaxial connectors up to 110 GHz in a MCM package. A notch free insertion loss characteristic of the package structure is achieved with a maximum insertion loss IL < 0.8 dB up to 110 GHz. The notch free insertion loss characteristic is achieved by optimizing the bonding wires and CBCPW structures. The paper reveals that the patch antenna mode resonance is the dominant loss mechanism for the CBCPW at higher frequencies. The resonance can be suppressed by reducing the gap between the end-vias and the end of CBCPW structure. With additional vias and bond wire structure optimization it is believed that an insertion loss IL < 0.6 dB is achievable for such a package structure.

Acknowledgment

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