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Keywords

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Abstract

In this paper, a novel push-pull-forward half-bridge (PPFHB) bi-directional DC-DC converter with coupled inductors is proposed. All switches can operate under zero-voltage-switching (ZVS). The operation principle with phase-shift modulation scheme, characteristics of coupled inductors, the steady state relationship and small-signal model are analyzed. The voltage controller based on the small-signal model in z-domain is designed. A 500W prototype controlled by TMS320F2808 DSP is implemented and tested. Experimental results show the validity of the analysis and design.

Introduction

The bi-directional dc-dc converter is generally needed as the interface circuit between the energy storage system and load or dc-bus, to control the power flow in the systems, such as uninterruptible power supply (UPS) system and hybrid electrical vehicle (HEV) system. Without isolation, buck-boost converter has been implemented in the applications without high voltage ratio requirement. For high voltage ratio application, transformer coupled and isolated bi-directional DC converters have been proposed such as dual active bridge (DAB) converter [1], [2], dual active half bridge converter [3-5], full bridge current fed converter [6], [7] and their derivatives [8-11]. To improve the system efficiency as well as increase the range of operation for the wide-range input voltage, some modulation schemes such as triangular modulation, trapezoidal modulation and PWM plus phase-shift modulation are investigated in [12], [13], and [14], with adding the duty ratio as a modulated parameter.

In this paper, a novel PPFHB bi-directional dc-dc converter with coupled inductors, shown in Fig. 1, with phase-shift modulation is investigated. Operation principle, parameters design, and closed-loop digital control based on DSP are analyzed. Finally, experimental results verify the effectiveness of the analysis and design.

Proposed PPFHB Bi-directional Converter

Operation Principles

The proposed topology employs the push-pull-forward structure to reduce the number of the power switches; utilises the half-bridge voltage doubler circuit in the secondary side of the high frequency transformer to get high voltage transition ratio. The auxiliary inductors, L_1 and L_2, and the leakage inductor of the transformer, L_{lk}, are utilized as the interface and energy transfer elements between the two high frequency voltage-source inverters in the two sides of the transformer, respectively.

The converter is controlled by the phase-shift technique to realize stable output voltage and bidirectional power flow between the low voltage (LV) side and high voltage (HV) side. Because the

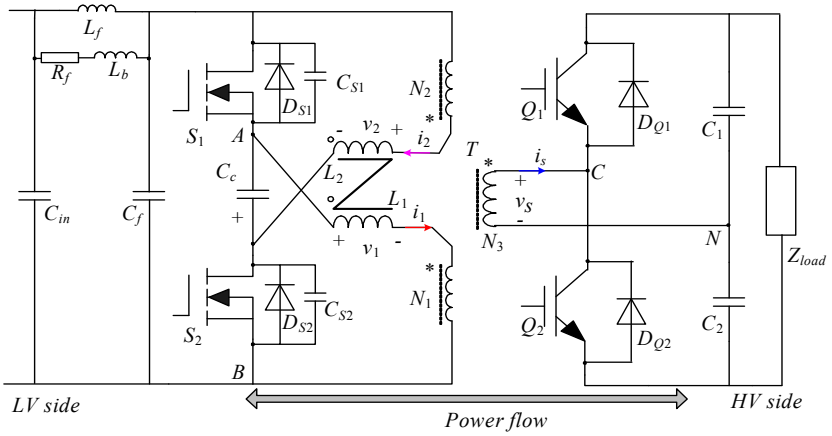


Fig. 1: The PPFHB converter with coupled inductors.

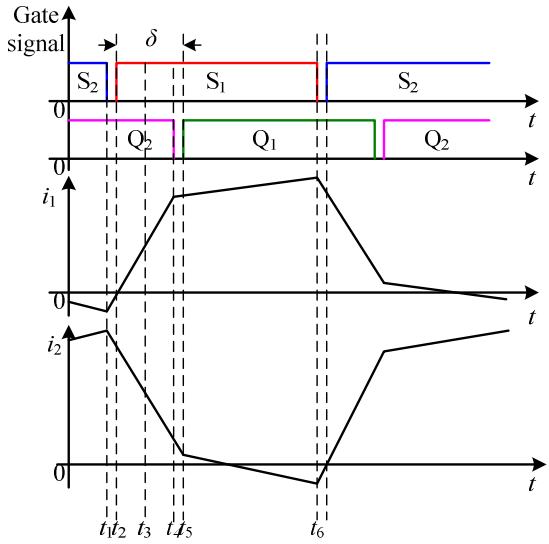


Fig. 2: Driving signals and theoretical waveforms

Table I: Gated and conducted sequence

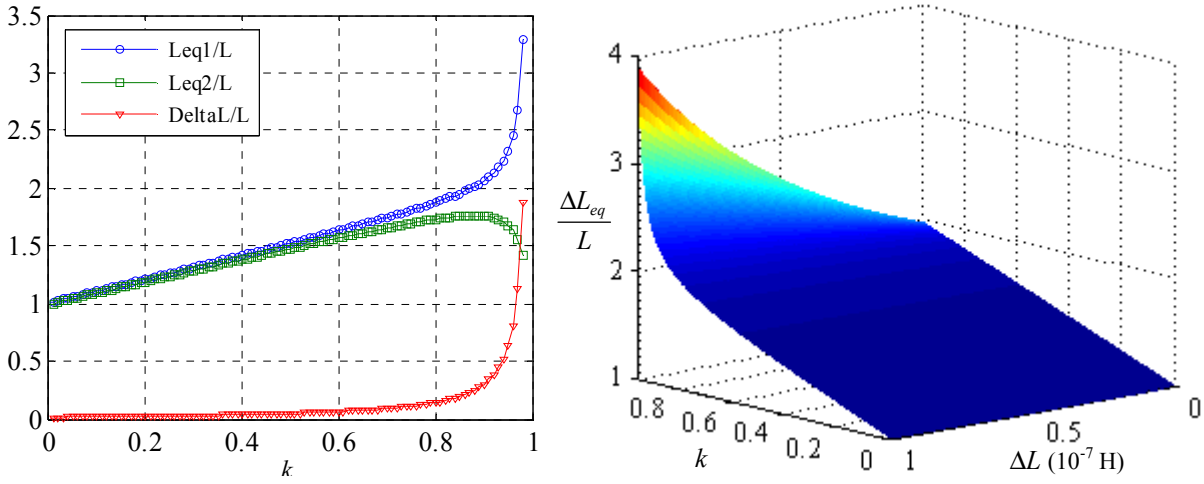
Intervals	LV side		HV side	
	Gated	Conduction	Gated	Conduction
$t_0<t<t_1$	S_2	S_2	Q_2	D_{Q2}
$t_1<t<t_2$	0	D_{S1}	Q_2	D_{Q2}
$t_2<t<t_3$	S_1	D_{S1}	Q_2	D_{Q2}
$t_3<t<t_4$	S_1	S_1	Q_2	Q_2
$t_4<t<t_5$	S_1	S_1	0	D_{Q1}
$t_5<t<t_6$	S_1	S_1	Q_1	D_{Q1}

voltages cross the switches are always leading to the currents in the corresponding switches, all the switches are turned on under ZVS.

Fig. 2 demonstrates the complete cycles of ideal circuit operation, where gate signals are square waveform with dead time. The angle between S_1 and Q_1 is the phase shift angle to be used to control the output voltage and power flow direction. The gated and conducting devices in every mode are listed in Table I.

($t_0<t<t_1$): i_1 has the current path: $V_{Cc+} \rightarrow S_2 \rightarrow N_1 \rightarrow L_1 \rightarrow V_{Cc-}$ and i_2: $V_{in+} \rightarrow N_2 \rightarrow L_2 \rightarrow S_2 \rightarrow V_{in-}$. The power is transferred in the forward direction;
($t_1<t<t_2$): In the dead time between S_1 and S_2, the energy stored in the L_1 and L_2 charges C_{S1} and discharges C_{S2} at the same time.
($t_2<t<t_3$): The voltage cross drain-source of S_1 is zero with the conducing D_{S1}.
($t_3<t<t_4$): i_1 is bigger than that of i_2 and the current is diverted from D_{S1} to S_1. In the secondary side, the current is diverted from D_{Q2} to Q_2 as well.
($t_4<t<t_5$): In the dead time between Q_1 and Q_2, the current paths are not changed.
($t_5<t<t_6$): At t_5, Q_1 is turned on under ZVS.

The detailed description of the operation principles in every interval can be found in the paper [15] that we have published before.



(a) When L=5 uH, ΔL=0.04uH (b) When L=5 uH, ΔL changes from 0 to 0.1uH

Fig. 3: The relationship curves: L_{eq1}, L_{eq2}, ΔL and k.

Coupled Inductors

Based on the operation principles of the converter, at any time, we always can get the relationship between the voltage cross the inductor L_1, v_1, and the voltage cross the inductor L_2, v_2, as: $v_1 = -v_2$. So we could couple the L_1 and L_2 together. The inverse coupling is used in this paper, shown in Fig. 1.

Its transformer model can be expressed by the following equation according to the well-known basic circuit theory:

$$\begin{cases} v_1 = L_1 \cdot \dfrac{di_1}{dt} - M \cdot \dfrac{di_2}{dt} \\ v_2 = L_2 \cdot \dfrac{di_2}{dt} - M \cdot \dfrac{di_1}{dt} \\ v_1 = -v_2 \\ M = k \cdot \sqrt{L_1 \cdot L_2} \end{cases} \Rightarrow \begin{cases} v_1 = (L+M) \cdot \dfrac{di_1}{dt} \\ v_2 = (L+M) \cdot \dfrac{di_2}{dt} \\ L_{eq} = L + M > L \end{cases} \tag{1}$$

where L_1=L_2=L is the self inductance of each winding; L_{eq} is the equivalent inductance; M is the mutual inductance and k is the coupling coefficient with $0 \le k \le 1$.

From equation (1), the coupled equivalent inductance is increased comparing with the non-coupled inductors. The AC flux is cancelled in the center leg of the inverse-coupling structure and the core loss can be reduced [16].

If the two inductors coupled together are unbalanced, we have:

$$\begin{cases} L_1 = L + \Delta L \\ L_2 = L - \Delta L \\ M' = k \cdot \sqrt{L_1 \cdot L_2} = k \cdot \sqrt{L^2 - \Delta L^2} < M \end{cases} \tag{2}$$

From equation (1) and (2), we can get:

$$\begin{aligned} v_1 &= \left(L + \Delta L + M' \cdot \frac{L - M' + \Delta L}{L - M' - \Delta L} \right) \cdot \frac{di_1}{dt} \\ v_2 &= \left(L - \Delta L + M' \cdot \frac{L - M' - \Delta L}{L - M' + \Delta L} \right) \cdot \frac{di_2}{dt} \end{aligned} \tag{3}$$

The equivalent inductances of the two inductors and the difference between them are expressed as:

$$
\begin{aligned}
L_{eq1} &= L + \Delta L + M' \cdot \frac{L - M' + \Delta L}{L - M' - \Delta L} \\
L_{eq2} &= L - \Delta L + M' \cdot \frac{L - M' - \Delta L}{L - M' + \Delta L} \\
\Delta L_{eq} &= L_{eq1} - L_{eq2} = 2 \cdot \Delta L + \frac{4 \cdot M' \cdot (L - M') \cdot \Delta L}{(L - M')^2 - \Delta L^2}
\end{aligned} \tag{4}
$$

Based on equation (4), we can plot the curves to show the relationships according to the coupling coefficient and equivalent inductance with the parameters: L=5 uH and ΔL=0.04 uH, shown in Fig. 3(a). In Fig. 3(b), we can see that when ΔL changes in the range: $0 \sim 0.1\,u$H, the unbalanced equivalent inductance is very sensitive to the variation of ΔL in the range with bigger k factor. It is clear that good coupling that means k is near to 1 between the two inductors is not appropriate in this power conversion application as the unbalance of the equivalent inductance will be too large to be acceptable. Self inductance and coupling efficient have to be properly selected to limit the unbalance and meet the inductor current ripple requirement.

Design considerations

Output Power

The delivered active power by this converter can be calculated, based on the waveforms shown in Fig. 2, by:

$$
P_O = \frac{V_{in}^2}{\omega(L + M + L_{lk})} \frac{\delta(\pi - |\delta|)}{\pi} \qquad \left(-\frac{\pi}{2} \le \delta \le \frac{\pi}{2}\right) \tag{5}
$$

where ω is the switching frequency and L_{lk} is leakage inductance of the transformer.

According to (8), when the input voltage and switching frequency are fixed, the output power is regulated by the phase shift angle and inductance $L_s = L + M + L_{lk}$. It will be found later that different phase shift angle will cause different current stresses on the devices. Therefore, the L_s can be designed according to the expected phased shift angle at the required power rating to reduce current stresses. At the same time, there is a limitation shown below to guarantee the output power is controlled in the whole range of $-0.5\pi \le \delta \le 0.5\pi$:

$$
V_{in} \ge 2\sqrt{\frac{P_O \omega L_s}{\pi}}
$$

We can find that the phase shift angle is the single control variable in the system, but when in deep regulation stage, that means the phase shift angle is near to $\pm 0.5\pi$, a large amount of reactive power will be in the high frequency transformer.

Power Device

Based on the waveform shown in Fig. 2, the peak current occurs at the point t_4 or t_6 according to the different input and output voltages. So the device rating of LV side can be calculated as:

$$
\begin{aligned}
I_{peak} &= i_1(t_4) - i_2(t_4) = \frac{4nV_{in}\delta + \pi(V_O - 2nV_{in})}{4\omega n L_s}, or \\
I_{peak} &= i_1(t_6) - i_2(t_6) = \frac{2V_O\delta + \pi(2nV_{in} - V_O)}{4\omega n L_s}, and \\
V_{peak} &= 2V_{in}
\end{aligned} \tag{6}
$$

Equation (6) shows the current stress of the main switches in the primary side against the output power because of the δ relative to the power as shown in (5); and at the same output power condition, the bigger difference between V_O and $2nV_{in}$, causes the higher current stress.

The disadvantage of the PPF circuit is that the voltage stress on the MOSFET is doubled comparing with that in full bridge circuit, so the high voltage MOSFET with higher on state resistance, R_{DS}(on),

has to be used and it leads to higher conduction loss. But because of the soft-switching operation of the converter, the switching speed can be lower. We can choose some higher current rating MOSFET with lower R_{DS}(on) as the switches to reduce the conduction loss.

ZVS conditions

In Fig. 1, the snubber capacitor is connected in parallel with each switch both to reduce switching loss and to damp out over-voltage. As described above, the conversions for primary side switches and secondary side switches occur during interval t_1~t_2 and t_4~t_5, respectively. As analyzed in [15], when I_{P1} plus I_{P2} is positive, where the I_{P1} and I_{P2} are the peak current values of i_1 and i_2, respectively, every switch can turn on under ZVS, depending on the output power P_o, the phase shift angle, the input and output voltages, and the dead time. The soft switching conditions will be shown as:

$$\begin{cases} I_{P1}(t_1)+I_{P2}(t_1)>0 \\ I_{P1}(t_4)+I_{P2}(t_4)>0 \\ I_{\min(I_{P1},I_{P2})}=\sqrt{\dfrac{2V_{in}V_O C_s}{nL_s}} \end{cases} \tag{7}$$

where C_s is the capacitance of the C_{S1}+C_{S2}, and $I_{\min(IP1,\ IP2)}$ is the minimum magnitude of the sum of i_1 and i_2 to guarantee the complete resonant between the L_s and C_s to realize ZVS.

System model and control

Based on (5), the voltage conversion ratio can be as:

$$M(\delta)=\frac{V_O}{V_{in}}=\sqrt{\frac{Z_L}{\omega(L+M+L_{lk})}\cdot\frac{\delta(\pi-\delta)}{\pi}} \tag{8}$$

where Z_L is the impedance of the load.

It is clear that output voltage is load-dependent and the system is nonlinear. To design the controller, small-signal analysis by linearization around the operating point is required.

In the given laboratory setup, the PPFHB converter is controlled by the digital signal processor (DSP TMS320F2808). Fig. 4 shows the small signal block diagram of the system in z-domain. The system sampling time, T, equals to 25 us, so we can get $z=e^{sT}$, and cut-off frequency of PI controller is $\omega_c=1/T_i$ in Fig. 4. ADC sampling delay, which is in the sub-micro second range, is ignored here. The delay caused by computation time and PWM modulator sampling delay in DSP affects the system frequency response and should be considered in the design. The transfer function of total delay effect is expressed:

$$G_{delay}(z)=G_{delayCom}\cdot G_{delayPWM}=z^{-1} \tag{9}$$

The symmetric optimum design method [17] is used to design the voltage controller. The simulation based on MatLab confirms the control method. The proportional gain K_p and integral gain K_I were set as:

$$K_P=0.2^o/\mathrm{V}\ \text{and}\ K_I=6.5^o/\mathrm{V}$$

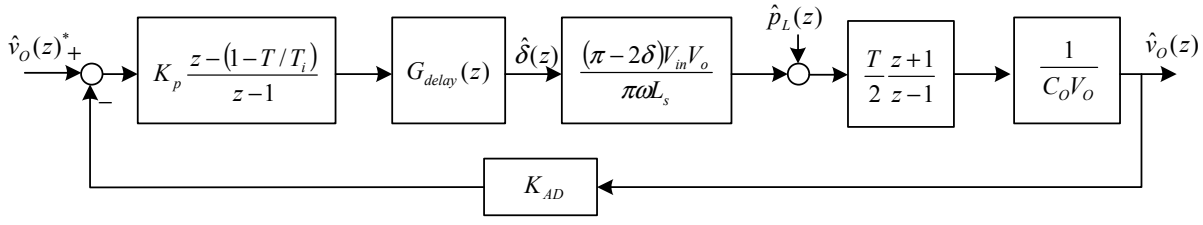
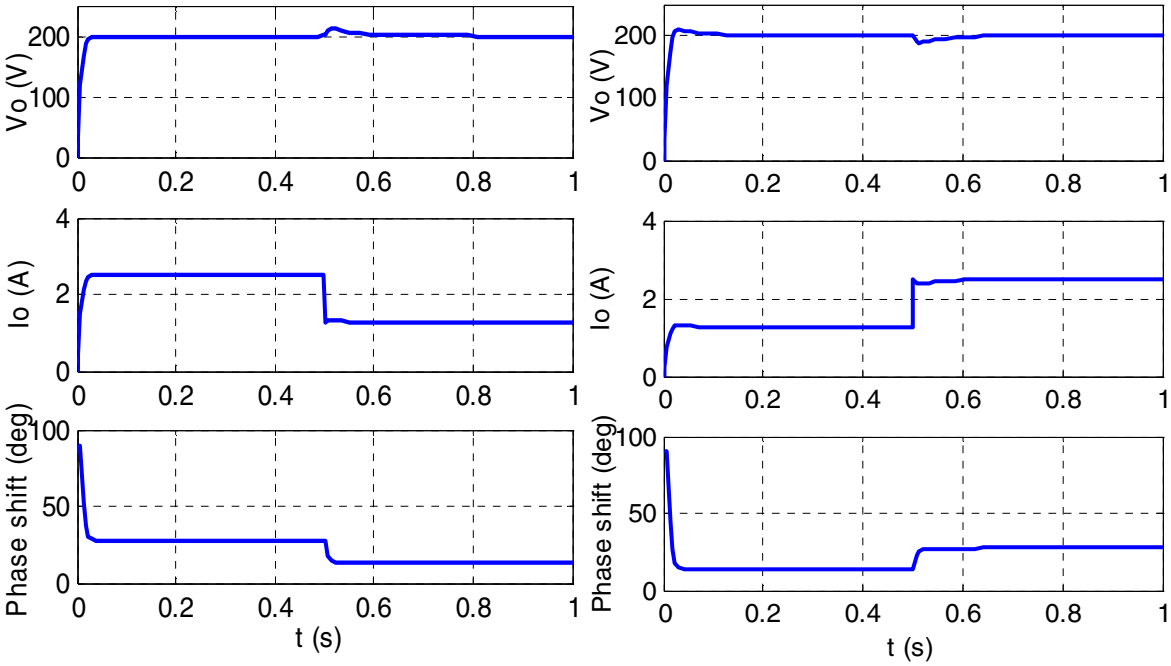


Fig. 4: Small signal z-region block diagram of the output voltage control



(a) Load changes at 0.5s from 500 W to 250 W (b) Load changes at 0.5s from 250 W to 500 W

Fig. 5: Simulation waveforms of step response and load disturbance response.

From Fig. 5, the overshoot occurs in step response with light load. The controller effectively adjusted the phase shift angle so that the dc/dc converter regulated the output voltage V_o back to 200 V in about 200 ms.

Experimental Results

In order to verify the feasibility and performance of the proposed converter, a laboratory prototype controlled by TMS320F2808 DSP, was implemented and evaluated. The specification and main parameters used in the converter are listed in Table II. The experimental results consist of relevant voltage and current waveforms, and efficiency curves.

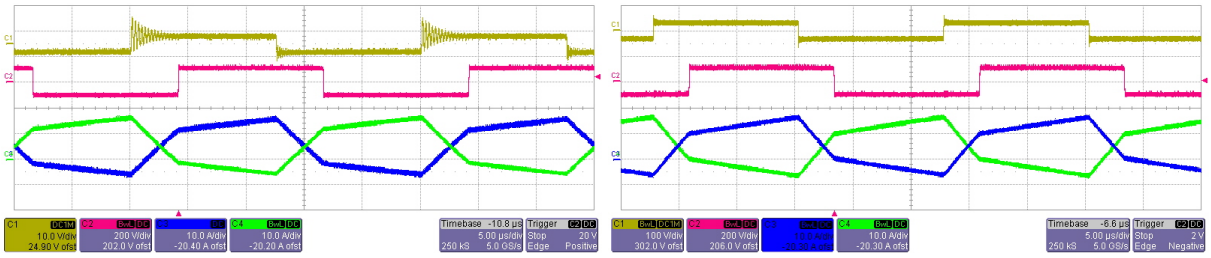
Table II: Specification, parameters and components table

Input voltage	30-50 V	Transformer	5:5:15, N87	Switches S_1 and S_2	SUP90N15
Output voltage	200 V	Inductors	L_1=L_2=6 uH	Switches Q_1 and Q_2	IRF450LC
Output Power	500 W	Coupling factor	0.35	Switching frequency	40 kH

Fig. 6 shows the voltage cross the primary side (from point A to point B, denoted in Fig. 1) and secondary side (voltage on the winding N_3) to show the phase shift modulation scheme with phase shift angle δ=40°. The waveforms of the converter with two individual inductors and that with coupled inductors are shown in Fig. 6 (a) and Fig. 6 (b), respectively. We can find that the ringing voltage on the primary side is reduced in the condition that the coupled inductors are used. The current waveforms in primary side, depicted in Fig. 2, are also confirmed by the experimental results.

The soft switching operation is validated in Fig. 7. When S_2 is gated off, the sum of i_1 and i_2 charges and discharges body capacitors C_{S1} and C_{S2}, respectively. Although S_1 is given an on signal after the dead time when S_2 is gated off, D_{S1} is conducting the current at that moment until i_1 increases to i_2. When i_1 is bigger than i_2, the current is diverted from D_{S1} to S_1 and S_1 is turned on at zero voltage. The soft-switching process can be derived similarly for other switches.

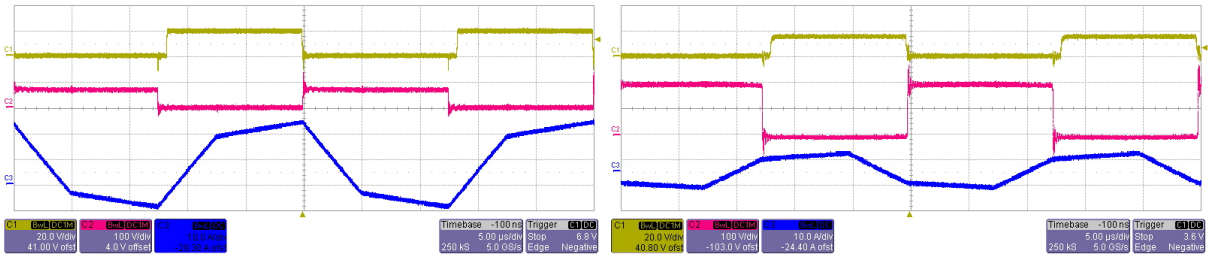
Fig. 8 shows the output voltage waveforms with step load change, and the load current stepped from 1 A to 1.5 A.



(a) The waveforms of the converter with two individual inductors

(b) The waveforms of the converter with coupled inductors

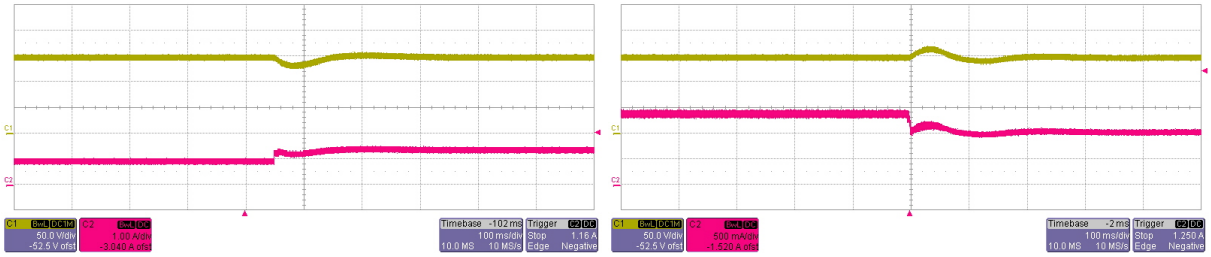
Fig. 6: the waveforms of steady state operation. Ch1: transformer primary voltage (20 V/div); Ch2: transformer secondary voltage (100 V/div); Ch3: i_1 (10 A/div); Ch4: i_2 (10 A/div). (Time: 5 *u*s/div)



(a) Ch1: gate-source voltage of S_1 (20 V/div); Ch2: drain-source voltage of S_1 (100 V/div); Ch3: i_1 (10 A/div).

(b) Ch1: gate-source voltage of Q_1 (20 V/div); Ch2: drain-source voltage of Q_1 (100 V/div); Ch3: i_s (10 A/div).

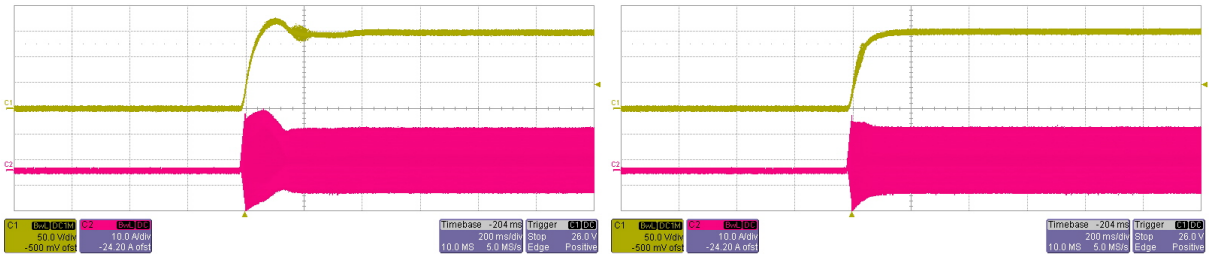
Fig. 7: The ZVS operation of the switches S_1 and Q_1. (Time: 5 *u*s/div)



(a) The load step from 1 A to 1.5 A. Ch1: Output voltage (50 V/div); Ch2: load current (1 A/div).

(b) The load step from 1.5 A to 1 A. Ch1: Output voltage (50 V/div); Ch2: load current (0.5 A/div).

Fig. 8: The load disturbance response. (Time: 100 *m*s/div)



(a) Open loop condition. Ch1: output voltage (50 V/div); Ch2: i_1 (10 A/div).

(b) Close loop condition. Ch1: output voltage (50 V/div); Ch2: i_1 (10 A/div).

Fig. 9: The output voltage and current i_1 responses with input voltage step from 0 to 30 V. (Time: 200 *m*s/div)

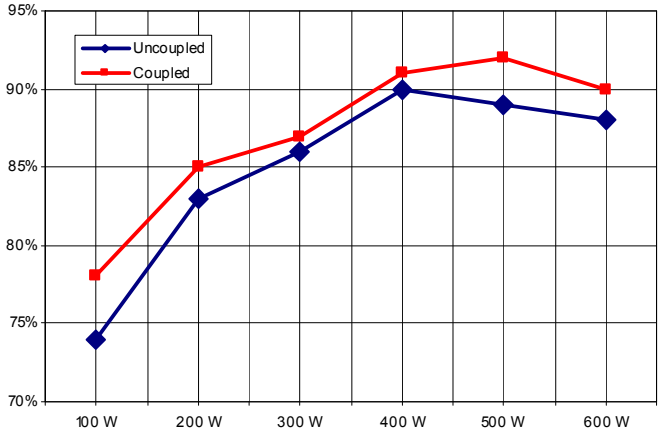


Fig. 10: Efficiency chart (V_{in}=30 V).

Fig. 9 (a) and Fig. 9 (b) show the output voltage and i_1 in step response with opened loop and closed loop, respectively. We can see that the close loop system can limit the overshoot of output voltage.

Fig. 10 plots the efficiency curves. The yellow one is the efficiency curve in the condition with the coupled inductors and green curve shows the efficiency of converter with two individual inductors (the input voltage equals to 30 V). So the usage of coupling inductors in this converter can improve the system efficiency because of the reduced core loss of inductor and the clearer waveforms. In this kind of low input voltage converter, the conduction loss is the major power loss and the switching loss is minimized due to soft switching.

Conclusion

A ZVS bidirectional dc-dc converter with coupled inductors is proposed and analysis in this paper. Using the coupled inductors in this converter can reduce the core loss and optimize the waveforms to improve the efficiency. But to limit the unbalance of the equivalent inductance, the coupling factor can not be set near to 1. Based on the waveform analysis, the parameters are designed and the ZVS range is discussed. According to the small signal model of the system in z-domain, the parameters of the voltage controller is decided by simulation. Finally, the prototype was setup and the experimental results show validity of the theoretical analysis and the performance of converter with coupled inductors is improved comparing with that with two individual inductors. So the converter proposed in this paper is a promising candidate as the bidirectional interface converter in EV systems or UPS systems for battery or super-capacitors application.

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