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Traffic analysis and signal processing in optical packet switched networks

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List of acronyms

1R	Reamplification
2R	Reamplification + Reshaping
3R	Reamplification + Reshaping + Retiming
ACTS	Advanced Communications Technologies and Services
BER	Bit Error Rate
BRF	BiRefringent Fibre
CoS	Class of Service
CW	Continuous Wave
DAVID	Data And Voice Integration over DWDM
DISC	Delayed-Interference Signal Converter
DCF	Dispersion Compensating Fibre
DFB	Distributed Feed-Back (laser)
DFG	Difference-Frequency Generation
DOMO	Dual-Order MOde
DWDM	Dense WDM
EA	Electro Absorption (modulator)
EDFA	Erbium-Doped Fibre Amplifier
EMPLS	Electrical MPLS
FDL	Fibre Delay-Line
FEC	Forward Equivalence Class
FEC	Forward Error Correction
FIFO	First-In-First-Out
FPGA	Field Programmable Gate Array
FWHM	Full Width Half Maximum
FWM	Four-Wave Mixing
GC-SOA	Gain-Clamped SOA
HOL	Head-Of-Line (blocking)
IDS	Input Data Signal
IETF	Internet Engineering Task Force
IP	In-Phase (operation)
IP	Internet Protocol
IPDR	Input Power Dynamic Range
ISSR	Input Signal Rejection Ratio
IST	Information Society Technologies

IWC	Interferometric Wavelength Converter
KEOPS	KEys to Optical Packet Switching
LAN	Local Area Network
LDP	Label Distribution Protocol
LSP	Label-Switched Path
LSR	Label-Switched Router
MAC	Media Access Control
MAN	Metropolitan Area Network
MEMS	Micro Electro-Mechanical Systems
MI	Michelson Interferometer
MMI	Multi-Mode Interference (coupler)
MPLS	Multi-Protocol Label Switching
MPλS	Multi-Protocol Lambda Switching
MZI	Mach-Zehnder Interferometer
NOLM	Nonlinear Optical Loop Mirror
NRZ	Non-Return-to-Zero
OC	Optical Channel
O/E/O	Optical-to-Electrical-to-Optical (conversion)
OMPLS	Optical MPLS
OOP	Out-Of-Phase
OPADM	Optical Packet Add-Drop Multiplexer
OPR	Optical Packet Router
OPRN	Optical Packet Ring Node
OSNR	Optical Signal-to-Noise Ratio
OSPF	Open Shortest Path First
OTDM	Optical Time-Division Multiplexing
OXC	Optical Cross-Connect
PLR	Packet Loss Ratio
PRBS	PseudoRandom Bit Sequence
QoS	Quality of Service
RAM	Random Access Memory
RZ	Return-to-Zero
SDH	Synchronous Digital Hierarchy
SDM	Space-Division Multiplexing
SLALOM	Semiconductor Laser Amplifier Loop Optical Mirror
SNR	Signal-to-Noise Ratio

SM	Single-Mode
SMF	Single-Mode Fibre
SOA	Semiconductor Optical Amplifier
TDM	Time-Division Multiplexing
TOAD	Terahertz Optical Asymmetric Demultiplexer
TOWC	Tuneable Optical Wavelength Converter
UNI	Ultrafast Nonlinear Interferometer
WAN	Wide Area Network
WDM	Wavelength Division Multiplexing
XGM	Cross-Gain Modulation
XOR	eXclusive-OR
XPM	Cross-Phase Modulation

Abstract

This thesis focuses on functionalities that are important for the realisation of future all-optical packet switched networks, and which may be implemented using the interferometric wavelength converter. The European IST research project DAVID, with the aim of demonstrating the feasibility of a Tbit/s optical packet switched network exploiting the best of optics and electronics, is used as a thread throughout the thesis.

An overview of the DAVID network architecture is given, focussing on the MAN and WAN architecture as well as the MPLS-based network hierarchy. Subsequently, the traffic performance of the DAVID core optical packet router, which exploits wavelength conversion and fibre delay-line buffers for contention resolution, is analysed using a numerical model developed for that purpose. The robustness of the shared recirculating loop buffer with respect to bursty traffic is demonstrated and compared with a standard fibre delay-line based output buffer. Moreover, the effectiveness of the recirculating loop is demonstrated through a 55% reduction in the switching fabric size enabled by a small reduction in the offered load per input channel from 0.8 to 0.6.

Different techniques for interferometric wavelength conversion are discussed and the performance of the IWC is analysed experimentally based on the all-active Mach-Zehnder and Michelson interferometer. Wavelength independence over the entire C-band is verified and wavelength conversion at up to 40 Gbit/s using the differential control scheme is demonstrated with a 0.6 dB penalty. Moreover, using a novel device denoted the DOMO MZI, co-propagational conversion to the same wavelength, an important functionality for practical networks, is demonstrated at 10 Gbit/s with a 2.4 dB penalty. Finally, a novel conversion scheme involving the injection of an additional clock signal into the IWC is presented. Results show very good transmission capabilities combined with a high-speed response.

It is argued that signal regeneration is an inherent attribute of the IWC employed as a wavelength converter due to the sinusoidal transfer function. This is verified experimentally at 40 Gbit/s on an input signal degraded by noise. Moreover, conversion to a 40 GHz clock signal, which enables re-timing, is demonstrated with a power penalty of 0.5 dB. The excellent regenerative capabilities of the novel conversion scheme are verified at 10 Gbit/s with a 4 dB improvement in receiver sensitivity. Finally, regeneration without wavelength conversion is demonstrated at 40 Gbit/s in an MZI with a 2.5 dB improvement. Additionally, the IWC's capabilities for simultaneous time-division de(multiplexing) and wavelength conversion are demonstrated experimentally for 40 to 10 Gbit/s demultiplexing and 2x10 to 20 Gbit/s multiplexing.

Lastly, the IWC's capabilities as an optical logic gate for enabling more complex signal processing are demonstrated and four applications hereof are discussed. Logic OR and AND are verified in full at 10 Gbit/s using PRBS sequences coupled into an MI. Moreover, logic XOR is demonstrated in an MZI at 10 and 20 Gbit/s with good results. Using an MI, the excellent performance of a novel scheme for MPLS label swapping exploiting logic XOR is demonstrated at 10 Gbit/s with a negligible 0.4 dB penalty. Finally, three novel schemes are described, involving all-optical pattern recognition by bit-wise sampling at multiple wavelengths, optical identification of bit differences in data segments through a combination of logic XOR and AND, and all-optical bit sequence replacement through logic OR and AND. The schemes enable important signal processing functionalities in packet switched networks to be implemented all-optically in a simple and cost-effective manner, and can be implemented using a single IWC.

Resumé (in Danish)

Denne afhandling fokuserer på funktionaliteter, der er vigtige for realisering af fremtidens fuldt-optiske pakkekoblede netværk, og som kan implementeres ved hjælp af interferometriske bølgelængdekonvertere. Det europæiske IST forskningsprojekt DAVID, som har til formål at demonstrere gennemførligheden af et Tbit/s optisk pakkekoblet netværk, der udnytter det bedste af optikken og elektronikken, er benyttet som rød tråd gennem afhandlingen.

En oversigt over DAVID netværksarkitekturen, der fokuserer på MAN og WAN arkitekturen såvel som det MPLS-baseret netværkshierarki, er givet. Herefter er trafik-ydeevnen for den optiske pakkeruter i DAVID kernenetværket, som udnytter bølgelængdekonvertering og fiber forsinkelseslinier til konfliktløsning, analyseret ved hjælp af en numerisk model udviklet til formålet. Hårdførheden af den delte recirkulerende loop buffer med hensyn til bursty trafik er demonstreret og sammen-lignet med en standard fiberforsinkelseslinie-baseret udgangsbuffer. Ydermere er effektiviteten af den recirkulerende loop demonstreret ved en 55% reduktion i switch-størrelsen, muliggjort ved en lille reduktion i trafikbelastningen per indgangskanal fra 0.8 til 0.6.

Forskellige teknikker til interferometrisk bølgelængdekonvertering er diskuteret og ydeevnen af IWC'en er analyseret eksperimentelt baseret på det fuldt-aktive Mach-Zehnder og Michelson interferometer. Bølgelængdeuafhængigheden over hele C-båndet er verificeret, og bølgelængdekonvertering ved op til 40 Gbit/s ved benyttelse af den differentielle kontrolmetode er demonstreret med en 0.6 dB følsomheds-forringelse. Ydermere, ved benyttelse af en ny komponent med betegnelsen DOMO MZI, er konvertering til samme bølgelængde med bølgeudbredelse i samme retning demonstreret ved 10 Gbit/s med en 2.4 dB følsomhedsforringelse. Denne funktionalitet er vigtig for implementering af praktiske optiske netværk. Slutteligt er en ny konverteringsmetode, der involverer kobling af et ekstra kloksignal ind i IWC'en, præsenteret. Resultater viser gode transmissionsegenskaber samt et hurtigt respons.

Det er argumenteret at signal regenerering er et medfødt attribut for IWC'en anvendt som en bølgelængdekonverter på grund af den sinusformede overførings-karakteristik. Dette er verificeret eksperimentelt ved 40 Gbit/s på et indgangssignal der er degraderet af støj, og konvertering til et 40 GHz kloksignal, som muliggør klok-genoprettelse, er demonstreret med en følsomhedsforringelse på 0.5 dB. De gode regenereringsegenskaber af den nye konverteringsmetode er verificeret ved 10 Gbit/s med en 4 dB følsomhedsforbedring. Slutteligt er regenerering uden bølgelængdekonvertering demonstreret ved 40 Gbit/s i en MZI med en 2.5 dB forbedring. Ydermere er IWC'ens anvendelse til samtidig tids-de(multipleksning) og bølgelængdekonvertering demonstreret experimentelt for 40 til 10 Gbit/s

demultipleksning og 2x10 to 20 Gbit/s multipleksning.

Slutteligt er IWC'ens evner som optisk logisk kontakt til at muliggøre mere kompleks signalprocessering blevet demonstreret, og fire applikationer af dette er diskuteret. Logisk OR og AND er fuldt verificeret ved 10 Gbit/s ved hjælp af PRBS sekvenser koblet ind i en MI. Ydermere er logisk XOR demonstreret i en MZI ved 10 og 20 Gbit/s med gode resultater. Ved anvendelse af en MI er den gode præstation af en ny metode til MPLS label swapping, der udnytter logisk XOR, blevet demonstreret ved 10 Gbit/s med en negligibel 0.4 dB følsomhedsforringelse. Tre nye metoder er blevet beskrevet til fuldt-optisk mønstergenkendelse ved bitvis sampling ved multiple bølgelængder, optisk identifikation af bitforskelle i datasegmenter gennem en kombination af logisk XOR og AND, og fuldt-optisk bitsekvenserstatning gennem logisk OR og AND. Metoderne muliggør fuldt-optisk implementation af vigtige signalprocesseringsfunktionaliteter i pakkekoblede netværk på en simpel måde, og kan implementers i en enkelt IWC.

Table of contents

Chapter 1

Introduction

More sweeping job cuts for struggling Lucent:

*As part of its second phase of restructuring, Lucent Technologies
is to slash 15,000-20,000 additional jobs.[1]*

At the time of writing, headlines like the one cited above are an everyday occurrence. What went wrong to prompt such a reversal of fortune for the communications industry since the boom in the late 1990's?

Obviously, tele- and datacommunications are closely related to the Internet, why the exponential growth of the Internet in the late 1990's spurred an explosion in requirements for bandwidth, and therefore in high-speed networking equipment and solutions. When the dot-com bubble burst in the spring of 2000 because the revenue potential could not keep up with the immense market expectations, the telecom and optical communications industry was also affected significantly. According to the magazine *Fibre Systems Europe* [1], most industry analysts agree that the service providers are to blame for the slowdown in the industry. Previously, service providers were spending large sums on new fibre infrastructure and network upgrades in order to keep pace with the growth in the Internet. Thus, optical vendors were forced to build up inventory in order to avoid losing sales. With the burst of the dot-com bubble, network expansion is not a priority, why service providers have turned to rationalisation of their business model, while waiting for the advent of next-generation networks. This reduction in capital expenditure on network infrastructure has affected the whole optical supply chain, which is left with a stockpile of depreciating hardware. As a consequence of this, many companies are announcing massive job cuts in order to minimise costs in the short term.

Fortunately, the future is not unconditionally dark for the optical communications industry. According to [1], the current downturn should instead be seen as a change of direction. Both analysts and component vendors agree that future investments should be placed in companies that will pave the way for next-generation optical networks. Here, innovation as well as product maturity is required to lower the cost and increase the flexibility of the networks.

So, what exactly does the term "next-generation optical network" cover? The development of the EDFA (erbium doped fibre amplifier) in the 1980's and its commercialisation by 1990 enabled the exploitation of optical amplification for

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[1] Fibre Systems online news week 30, 2001 (http://news.fibers.org).

increasing the repeater spacing and wavelength-division multiplexing (WDM) enabled an increase in capacity. Since then, optics has had a major role in communications networks [2]. Until now, the optical domain has been used solely for transport, while switching and more complex signal processing have been performed in the electronic domain. However, as the bit rate is increased, power-consumption and size issues make optical solutions increasingly attractive [3]. With the recent commercialisation of the micro-electro-mechanical systems (MEMS) technology for space switching [4] (e.g., employing tiny mirrors to reflect incoming light to the switch node to the appropriate outlet), all-optical networks, that route data entirely in the optical domain, are forthcoming [5].

It is envisaged that the first all-optical networks will be based on wavelength routing optical cross-connects (OXCs) employing MEMS-based switches with ms-level reconfiguration time. Most likely, Multiprotocol Lambda Switching (MPλS) will be used to set up circuits associated with optical wavelength channels [6,7].

Although a feasible solution for optical space switching is the first step towards all-optical networks, widespread application of all-optical networks requires that the practical network size is not limited through the choice of optics rather than electronics. This means that the optical network should be flexible as well as scaleable in size. Among the key components to enable this are optical wavelength converters and 3R regenerators. Wavelength conversion enables flexibility through wavelength re-use because wavelength allocation can be done on a local instead of global scale, thus allowing more efficient bandwidth usage [8,9]. Among the prime candidates for all-optical wavelength conversion is the interferometric wavelength converter (IWC), which exploits the principle of cross-phase modulation (XPM) [10-12,Pub2,Pub4,Pub12]. In order to enable large-scale optical networks and long-haul transmission, it is critical to ensure that the signal quality is maintained from source to destination. For this, optical 3R regeneration is necessary, which, apart from re-amplification, comprises correction for noise and nonlinear distortion (re-shaping) as well as ensuring that each pulse maintains its correct time position in the sequence (re-timing) [13-16,Pub1,Pub5,Pub17].

As optics matures, optical packet switching will most likely replace circuit switching due to the high degree of bandwidth utilisation and flexibility that it allows [17]. Also for packet switching, wavelength conversion is an important functionality, as it can be used to improve the traffic performance and reduce the required buffer capacity [18,19]. A likely scenario on the medium term is however still that processing of data packet overhead will be performed in the electrical domain, while the payload is switched transparently without O/E/O-conversion [20]. On the longer term, it may however be envisaged that increasingly complex signal processing functionalities can with advantage be implemented in the optical domain. For this purpose, all-optical logic gates will be key components. Using IWCs, Boolean functions such as logic

NOT, AND, OR and XOR have been demonstrated within recent years [21,22,Pub10,Pub11]. Moreover, practical applications of optical logic gates for such different purposes as generation of PRBS[2] sequences [23], MPLS[3] label swapping [Pub20] and parity checking [24] have been demonstrated.

This thesis contains modelling as well as experimental work that is important for the implementation of optical networks in general and packet switched networks in particular. The work is partially linked to the ongoing European IST[4] project DAVID (Data And Voice Integration over DWDM), for which the aim is to exploit an optimal combination of electronics and optics to demonstrate the feasibility of a high-capacity optical packet switched network. The DAVID project will also function as the main thread between the different topics that are discussed in this thesis. Firstly, a general overview of the DAVID network concept will be given. Based on this discussion, the traffic performance of the DAVID core optical packet router (OPR) is analysed through simulations. Wavelength converters are key components in enabling the excellent traffic performance of the DAVID OPR. Following this line, a detailed experimental investigation of interferometric wavelength converters will be given, as well as comparison of the most attractive wavelength conversion schemes. As mentioned previously, 3R regeneration is an important factor for optical networks. In this thesis, experimental results demonstrating the IWC's capability for regeneration will also be given. Finally, taking the concept of optical networks a step further, more exotic applications of the IWC for time-division multiplexing and demultiplexing as well as optical logic will be experimentally verified. Finally, some novel schemes relying on optical logic for more complex data processing that are of interest in packet switched networks will be described. More specifically, the contents of this thesis is as follows:

In Chapter 2 the implementation of optical packet switched networks will be described using the DAVID project as a case study. Here, the MAN (Metropolitan Area Network) and WAN (Wide Area Network) architecture will be described. Finally, a description will be given of the DAVID network hierarchy, which exploits MPLS to create a unified switching/routing approach that links all network levels together.

In Chapter 3 the focus will be on the traffic performance of the DAVID core OPR, which exploits a recirculating loop for buffering. Firstly, a general comparison of the optical component count and traffic performance will be made with a generic packet switch using optical output buffering. Subsequently, the model used for the simulations will be discussed, whereupon a closer examination of the packet loss rate of the DAVID OPR will be given, using the parameters for switch size, etc. set within

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[2] PRBS: PseudoRandom Bit Sequence
[3] MPLS: MultiProtocol Label Switching
[4] IST: Information Society Technologies

the DAVID project. Here, the effect of the size of the loop buffer and the packet arrival distribution will be discussed.

Chapter 4 gives the system requirements to optical wavelength converters and discusses some different technologies for wavelength conversion. Here, the focus is mainly on a comparison of the principle of operation, as well as advantages and disadvantages of techniques for interferometric SOA-based wavelength conversion. After some basic experimental results at 10 Gbit/s achieved with the integrated all-active Michelson interferometer (MI), conversion at up to 40 Gbit/s is presented using the all-active Mach-Zehnder interferometer (MZI). Subsequently, the Dual-Order Mode (DOMO) wavelength converter, which allows co-propagative conversion to the same wavelength through mode separation, is described, and results are given for conversion up to 20 Gbit/s. Finally, a novel conversion scheme, which enables a high-speed response combined with good transmission properties, is described, and a experimental comparison is made with standard wavelength conversion. The results shown in Fig. 4.8 and 4.15 were obtained with Mads Lønstrup Nielsen (COM), Allan Kloch (formerly COM) and Henrik Wessing (COM). The work in Sections 4.3.2 and 4.4 was carried out together with David Wolfson, Allan Kloch and Peter Bukhave Hansen, all formerly with COM, while the remainder of the experimental results were obtained with Allan Kloch and David Wolfson.

In Chapter 5, the principle of signal re-shaping and re-timing in an IWC is described. Following this, experimental results for simultaneous wavelength conversion and 2R regeneration at 40 Gbit/s are demonstrated. Subsequently, the principle of re-timing through conversion to a clock signal is given, and results are shown at 40 Gbit/s. Following this, the regenerative capabilities of the novel conversion scheme are demonstrated at 10 Gbit/s and the operating principle and 40 Gbit/s experimental results are shown for the pass-through scheme, which enables signal re-shaping in an IWC without wavelength conversion. Finally, the focus turns to application of the MZI for optical time-division demultiplexing and multiplexing. Firstly, results will be shown for simultaneous 40 to 10 Gbit/s demultiplexing and wavelength conversion, whereupon 2x10 to 20 Gbit/s multiplexing will be demonstrated. The work in Sections 5.1.2 and 5.1.3, with the exception of Section 5.1.2.3, was made together with David Wolfson, Allan Kloch and Peter Bukhave Hansen, while the remainder was done in collaboration with David Wolfson and Allan Kloch.

The topic of Chapter 6 is all-optical logic and its applications. The principle of operation and implementation-specifics, that should be paid attention to, are discussed. Moreover, experimental results are given for logic OR and AND at 10 Gbit/s using an MI and logic XOR at up to 20 Gbit/s using an MZI. Subsequently, a novel scheme for MPLS label-swapping exploiting logic XOR is

described and the scheme is verified at 10 Gbit/s. Finally, three novel schemes for complex signal processing are presented, which exploit the IWC for multiple simultaneous logic operations. The first is applicable for all-optical pattern recognition, the second for identification of bit differences in data segments, and the third scheme enables all-optical bit sequence replacement. The experimental work in this chapter has been done in collaboration with Allan Kloch and David Wolfson.

Chapter 7 concludes the thesis.

Chapter 2

Implementation of optical packet-switched networks: a case study

With the broad use of WDM as the transport technology in commercial networks, an important step has been taken in meeting the increasing demands for bandwidth within the last years. To cope with this evolution, the capacity and functionality of electronic IP (Internet Protocol) routers are also increasing dramatically, although technological breakthroughs are still required [3]. Due to issues of cost, power-consumption and physical size, other alternatives to electronic IP routers are being widely investigated; first optical layer cross-connects, e.g., based on the MEMS technology [4], that will increase capacity in current SDH[5] networks, are being developed [5]. An IETF[6] proposal is under study, involving exploitation of this OXC technology to enable the transport of IP traffic directly over a WDM infrastructure with the aid of MPλS[7] to set up circuits, or label-switched paths (LSPs), associated with optical wavelength channels [6,7].

In the meantime, several research projects worldwide, and especially in Europe, have investigated techniques for optical packet switching, which has the advantage of increased network flexibility and a larger degree of granularity (i.e., packets instead of wavelengths) than the circuit-switched technology that MPλS offers. This granularity increase enables an efficient reduction in the required network capacity, and thus a potential reduction in the connect cost for users, thanks to a better sharing of the physical resources. This is, however, at the expense of added complexity, both with respect to optical technology as well as electronic control.

In the European ACTS[8] project KEOPS (Keys to Optical Packet Switching), the feasibility of optical packet switching in the core network was studied intensely, with the focus on optical implementations of the required processing functionalities, e.g., for temporal synchronisation of packets, regeneration, switching, etc. [25,26]. However, very little attention was paid to the interoperability between optics and electronics and implementation of the required control electronics. As an extension of the KEOPS project, the IST project DAVID was started in the Summer 2000.

In this chapter, the implementation of an optical packet switched network will be discussed using the DAVID project as a case study. In Section 2.1, the objectives of the DAVID project will be discussed, whereupon a general overview of the DAVID

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[5] SDH: Synchronous Digital Hierarchy
[6] IETF: Internet Engineering Task Force
[7] The concept of MPλS will be discussed in more detail in Section 2.2.3.
[8] ACTS: Advanced Communications Technologies and Services

network architecture will be given in Section 2.2. Finally, a summary will be given in Section 2.3. It should be noted that, as the DAVID project is still running, some of the elements discussed in this chapter may be subject to change as the research project evolves.

2.1 Objectives of the IST project DAVID

As mentioned in the introduction to this chapter, the goal of the KEOPS project was mainly to demonstrate that the processing functionalities required in a packet switched network could, to a large extent, be implemented in the optical domain. Very little consideration was paid to integration in a practical network and interoperability between optics and electronics.

The objective of the DAVID project [27] is to exploit the experience gained, e.g., through the KEOPS project to develop a packet-over-WDM network concept that is feasible on a medium term. Both the network traffic properties and management will be taken into account, and the focus will both be on the metro and backbone level. Solutions exploiting both optics and electronics are investigated to find the optimum combination that will realise a multi-Tbit/s capacity; optics are introduced in order to offer a high capacity, while electronics are introduced in order to ease complex signal processing and enable buffering on longer time scales. Furthermore, in order to cope with the convergence in the transport of voice, data and multimedia applications that is seen in commercial networks today, several classes of service will be developed and service differentiation will be investigated. By the end of the project in 2003, a test-bed will be assembled to demonstrate the DAVID solution for metro-core network implementation and integration, as well as interfacing to the client layer.

2.2 Overview of the DAVID network architecture

In Fig. 2.1 is shown a schematic of the DAVID network architecture, consisting of a metropolitan part (MAN) and a backbone part (WAN) [28,29]. The complete DAVID network forms an optical transport network that is able to carry (among other things) IP traffic. Both the MAN and the WAN operate in a packet switched mode in order to exploit the network capacity as much as possible. As indicated, the MAN consists of optical packet rings interconnecting optical packet ring nodes (OPRN), with several such rings interconnected through a Hub. The Hub will also provide access to the WAN through a gateway interface. The WAN consists of optical packet routers forming a mesh network. Some of the OPRs function as edge routers that are directly coupled to the MAN and handle add- and drop-traffic from and to the metro network, respectively, while others function as core routers that only handle transit traffic within the core network. Connection points for client traffic are provided in the MAN through connection of IP routers to the MAN ring nodes.
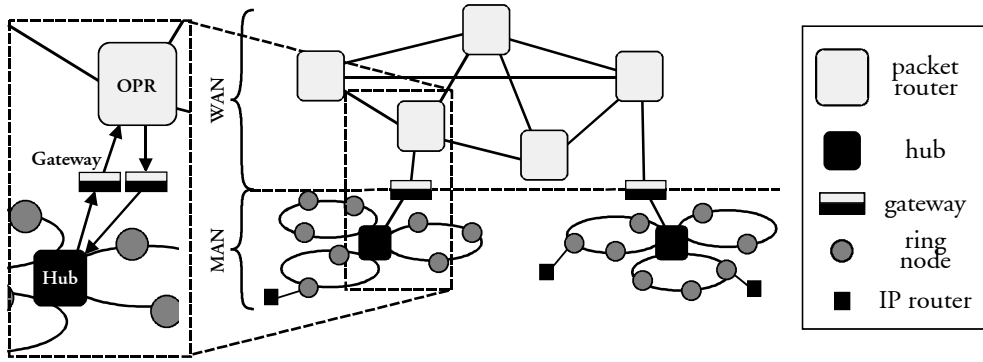
Fig. 2.1: General overview of the DAVID network. To the left a portion of the schematic is shown in an expanded version, and to the right is shown a key to the elements in the figure.

2.2.1   The metro network (MAN)

As mentioned, the DAVID metro network consists of several unidirectional optical physical rings that are interconnected in a star-topology by a Hub. On each fibre, a fixed number of wavelengths are available through the use of WDM. Logical rings (from now on simply denoted rings) can either be physically separated on different fibres, or be obtained by partitioning the optical bandwidth into subsets of wavelengths. Nodes belonging to the same logical ring access the same set of shared resources. All the nodes on a ring can transmit and receive on any wavelength used in that ring. Ring resources are shared by the nodes of the MAN using a statistical time/wavelength/space-division scheme. This is done in the following manner:

- Each wavelength is time-slotted (TDM) with a slot duration of ∼0.5-1 μs[9]
- Several slots are simultaneously transmitted through WDM
- Rings can be disjoint in space, i.e., on different physical fibres (SDM)

Time slots are aligned on all wavelengths of the same ring so that a multi-slot, consisting of all wavelengths on a logical ring, is available to each node in each time slot. The Hub handles slot alignment among different metro rings.

One of the wavelengths in each multi-slot is dedicated to control and management. This slot, which references data slots in the same multi-slot[10], can be read and written by each node independently of transmission/reception of data in the other slots of the multi-slot. Ring-to-ring transmission is controlled by a MAC (Media Access Control) protocol and performed via the Hub on a time-slot basis through

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[9] The value in the demonstrator is set to 0.5 μs, while the exact value for the concept is to be determined.

[10] Thus, the addition of a delay is required in each node to process and modify information in the control slot.

dynamic (input ring, output ring) permutation allocation. At any time, all wavelengths in the multi-slot are devoted to transmission to a specific destination ring, identified by a label in the control slot. A ring node may use any wavelength to reach a specific node in the destination ring.

In the MAN, collisions (multiple transmission in the same time slot) and receiver contentions (the number of packets destined for the same node simultaneously exceeds receiver capacity) are avoided at each source node through employment of a MAC protocol [28]. This is done by monitoring the state of the incoming multi-slot and giving priority to in-transit traffic, i.e., traffic not bound for that specific node. Collisions are avoided by prohibiting transmission of packets in a busy time slot, while contentions are avoided by prohibiting packet transmission to a given destination node if its capacity limit (i.e., number of receivers) is already met. It should be noted that contentions may also occur at the Hub. These are avoided by defining the Hub as a space-switch and running a proper slot scheduling algorithm.

Each ring node is basically composed of two parts: an optical and an electronic part. The optical part, denoted the Optical Packet Add/Drop Multiplexer (OPADM), consists of a transit-, add- and drop part, as shown in Fig. 2.2. The traffic flows from left to right. At the input, a fraction of the WDM signal is tapped off for the drop part. The wavelengths are demultiplexed, whereupon an array of SOA-gates selects the packets to be dropped. These are detected by using a receiver-block, and the rest of the signal is transmitted on to the transit part. Here, an array of SOA-gates placed between a demultiplexer and a multiplexer functions as a fast wavelength selector, which erases packets that are terminated in the node, and allows the rest to pass. The advantage of this configuration is that it allows broadcasting, if desired. At the OPADM output, packets are added to the ring through an array of (tuneable) transmitters followed by a multiplexer. Note that the SOAs placed at the transmitter output are not mandatory; they may or may not be inserted depending on the on/off ratio[11] of the lasers in the transmitter-block in order to prevent excessive cross-talk that degrades the signal quality.
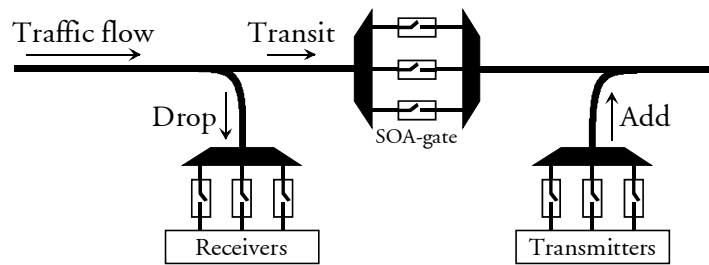
Fig. 2.2: Schematic of the optical part of the MAN ring node (OPADM).

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[11] On-off ratio: ratio between output power when the laser is turned on and when it is turned off.

The electronic part of the ring node is used to interface to the client layer. It consists of an aggregation (reassembly) stage to create higher bit rate fixed-size data units from variable size packets (and vice-versa), a load-balancing stage to distribute the packets evenly on the available logical rings, and a queuing stage in which packets are grouped and stored per destination ring. The electronic interface also controls the MAC protocol and takes care of packet insertion onto the ring in a free slot.

The role of the Hub is to switch packets between metro rings and between the MAN and the WAN. A schematic of the Hub, which is all-optical, is shown in Fig. 2.3. F in- and output ports, each carrying G wavelengths, are dedicated to traffic coming from and going to the metro rings. Furthermore, a number of ports are dedicated to traffic coming from or going to the WAN. In order to prepare the traffic exchange between the MAN and the WAN, electronic format adaptation is performed (in the Gateway, c.f., Fig. 2.1). This will be discussed in more detail in Section 2.2.3. At the metro input interfaces, wander compensation (i.e., coarse, slow packet synchronisation) is performed in the WDM domain in order to align packets from the rings to the local frame clock of the Hub and to enable switching in a synchronous manner within the Hub. This synchronisation is required to compensate for slow delay variations due to, e.g., temperature fluctuations in the network. The exact configuration of the MAN wander compensator is, unlike the one in the WAN that will be discussed in Section 2.2.2, not decided yet. However, because the constraints are more relaxed in the MAN than the WAN, the wander compensator will be simpler, as will be discussed in Section 2.2.2. At the output of the wander compensators, wavelength conversion and 3R regeneration[12] are performed simultaneously through the use of SOA-based interferometers, which will be described in more detail in Chapters 4 and 5. Wavelength conversion is necessary to relax the constraints on the ring nodes and ease the slot scheduling in the MAN. 3R regeneration is employed in order to ensure a good signal quality. At the output of the space-switching fabric, which will be described in Section 2.2.2, wavelength conversion and 3R regeneration are performed
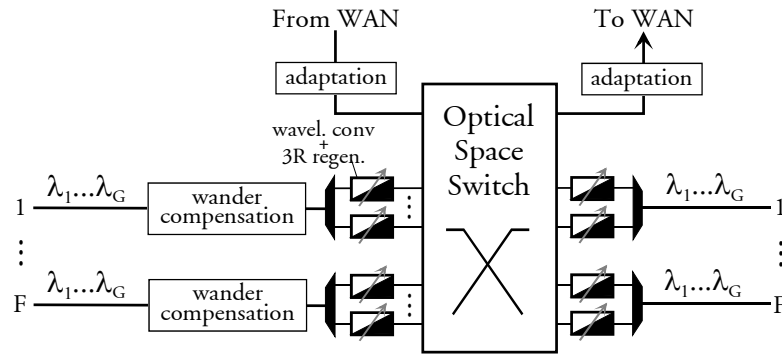
Fig. 2.3: Schematic of the Hub.

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[12] 3R regeneration: Re-amplification + Re-shaping + Re-timing.

again to prepare for subsequent transmission. It can be noted that an advantage of having wavelength conversion both at the input and output of the switching fabric is that it allows complete decoupling between the wavelengths used internally in the Hub and the wavelengths used externally in the network. This may relax the requirements to the optical component count in the switching fabric, depending on the chosen configuration as discussed in Section 2.2.2.

2.2.2 The core network (WAN)

As mentioned previously, the WAN consists of optical packet routers forming a mesh network. The structure of the core OPR [30], which is shown in Fig. 2.4, is much like the Hub as seen in Fig. 2.3. For the OPR, M in- and output ports, each carrying N wavelengths, are dedicated to transit traffic within the WAN. Furthermore, if the OPR is an edge router, a number of ports are dedicated to add- and drop traffic coming from or going to the MAN Hub, respectively. Finally, a number of ports are dedicated to packet contention resolution through the use of an optical fibre-delay line (FDL) recirculating loop buffer. The mode of operation and traffic performance of the optical buffer will be discussed in more detail in Chapter 3. In addition to the WDM wander compensation blocks, the OPR also contains single-channel jitter extraction blocks, which enable synchronisation to the local clock of the OPR by compensating for packet-by-packet jitter introduced when cascading many core nodes. This jitter occurs because exact matching of the lengths of different optical paths within a core node is impossible. As packets in the MAN only traverse one node, namely the Hub, the jitter extraction blocks are not necessary in the metro network. The OPR packet synchronisation unit is described in detail in [31]: the WDM wander compensator consists of two identical blocks that are switched between, so that each block services alternate packets. Each block
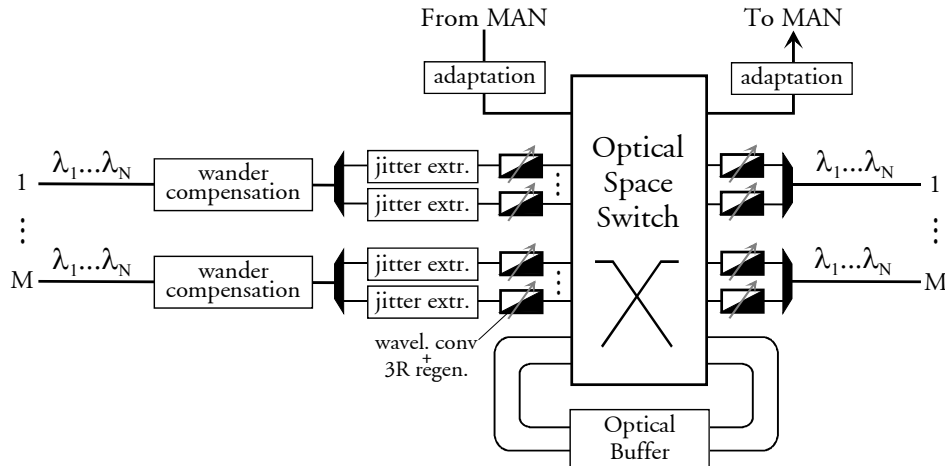
Fig. 2.4: Schematic of the WAN optical packet router [30].

consists of a cascade of 11 slow switches with FDLs of different lengths, exponentially distributed, placed in between. The jitter extractor, which has a resolution of 5 ns, consists of an array of four SOAs and FDLs of different lengths placed in between a 1:4 splitter and a 4:1 combiner, thus enabling fast packet-by-packet alignment. It should be mentioned that precise dispersion management is done on the transmission links, meaning that dispersion compensation is not performed as part of the synchronisation unit.

In Fig. 2.5a is shown a schematic of the optical switching fabric employed in the Hub and OPR. Note that, for completeness, the input and output wavelength converters are also shown in the figure. At the input to the switching fabric, packets arrive at mn (=MN) different input streams. Subsequent wavelength conversion and multiplexing band the mn input streams into m internal WDM groups, each carrying n wavelength channels. The m WDM groups are split out to mn SOA-based space- and wavelength selection blocks that enable fully non-blocking switching. These blocks can, e.g., be implemented as shown in Fig. 2.5b using two sets of SOA arrays separated by mxn star couplers. The first set of SOAs selects a group of wavelengths coming from one of the switching fabric inputs, while the second set of SOAs in conjunction with the following multiplexers select a specific wavelength. Thus, at the output of each space- and wavelength selection block, a single packet within each time slot has been selected. This configuration has been chosen, among other things, because it allows both point-to-point connection as well as multicasting. Moreover, as very fast wavelength selection (ns-level) is not currently possible using tuneable filters, why the scheme using SOAs in conjunction with multiplexers must be employed. Following the space- and wavelength selection blocks, wavelength converters convert the wavelength to prepare for the following transmission, while 3R regeneration is performed to compensate for signal distortion caused in the optical switching fabric (in analogy to the Hub). Note that (m,n), used internally in the switching fabric, can be different from (M,N), which refers to the external fibres/wavelengths to the OPR. The (m,n) wavelength banding is performed to reduce the optical component count in the space- and wavelength selection blocks to a minimum, which for symmetry reasons is obtained for m=n (see Fig. 2.5b). In the DAVID project, the goal with respect to throughput in the WAN is 2.56 Tbit/s for each OPR. The bit rate is set to 10 Gbit/s, thus giving a maximum-size switching fabric of 256x256. The throughput of 2.56 Tbit/s is enabled through the use of 32 wavelengths per fibre, meaning (M,N)=(8,32). However, internally in the switching fabric (m,n)=(16,16) is used to reduce the optical component count, as discussed. The electronic control and header processing performed in the core OPRs is closely related to the switching/routing approach that is adopted in the DAVID project. This topic is discussed in Section 2.2.3.
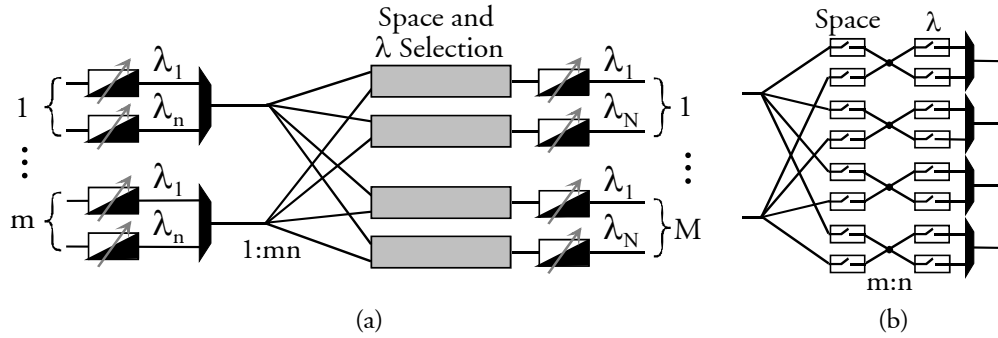
Fig. 2.5: (a) Optical switching fabric in the Hub and OPR. (b) One possible implementation of space and wavelength selection blocks (shown with interconnection shuffle at input) [30].

2.2.3   The DAVID network hierarchy

The DAVID network concept covers a whole range of networking levels from the metro network to the optical backbone network. Within DAVID, Multiprotocol Label Switching is used to create a unified switching/routing approach covering all network levels including the MAN. This affects the functionalities included, e.g., in the interface (Gateway) between the MAN and the WAN and electronic control of the WAN OPR. In this section the concept of MPLS will be discussed briefly, and the hierarchical MPLS approach used in the DAVID project will be described. Furthermore, the affect this has on the functionalities implemented in the MAN-WAN gateway and the header processing performed in the OPRs is also discussed.

Historically, MPLS was the result of a convergence of a number of "IP switching" schemes or techniques that used ATM (Asynchronous Transfer Mode) hardware to speed up the forwarding of IP packets (see [32,33] for an overview). In order to standardise the different IP switching schemes, the MPLS working group was founded in the Internet Engineering Task Force (IETF) in 1997 [34]. This working group has since then been working on a common technology for IP switching that is independent of the underlying transport layer.

In a traditional IP network, an IP packet is stored and forwarded in each router it passes based on a longest-prefix match processing of the global destination address. However, due to the unsystematic relation between the IP address and destination, this table look-up is rather cumbersome. In IP/MPLS networks [35], the IP table look-up is replaced by simple and fast label switching: the IP control plane, with its flexibility and scalability is preserved, but extended with the MPLS functionality. In contrast to regular IP, MPLS is a connection-oriented protocol that works by setting up unidirectional label-switched paths. As will be explained below, this has important consequences with respect to, e.g., traffic engineering.

Control and forwarding:

Network-layer routing can be divided into two basic components, namely control and forwarding [32,33]. The relationship between the routing and forwarding components in MPLS is illustrated in Fig. 2.6. The control component employs standard routing protocols (e.g., OSPF (Open Shortest Path First) [36]) to exchange information with other routers, and based on routing algorithms, it uses LDP (Label Distribution Protocol) to build up and maintain a forwarding table based on the routing information. The forwarding component has the task of processing incoming packets, examining the headers and making forwarding decisions based on the forwarding table.
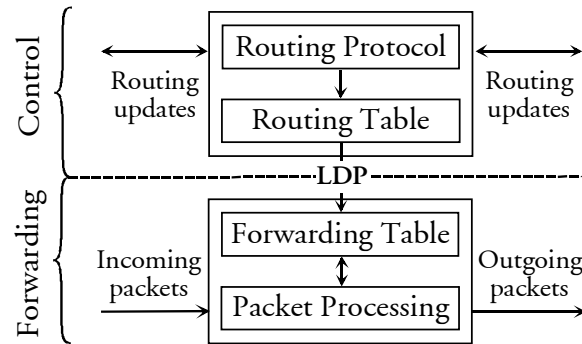
Fig. 2.6: Relationship between routing and forwarding components in MPLS.

Forwarding based on FEC and label swapping:

An IP header contains considerably more information than is needed to choose the next hop towards a packet's destination. Choosing the next hop can be thought of as a composition of two sub-functions [37]. The first is to partition the entire set of all possible packets so that a router can forward a finite number of subsets, or Forward Equivalence Classes (FECs). From a forwarding point-of-view, packets belonging to the same subset are indistinguishable: they are treated by the router in the same way. The second sub-function performed by the forwarding component is to map each FEC to a next hop.

In MPLS the assignment of a particular packet to a specific FEC is done only once, as the packet enters the MPLS network at the co-called ingress label-switched router (LSR). The FEC, to which a packet is assigned, is encoded as a short, fixed length value, called a label. When a packet is forwarded to its next hop, the label is sent along with it. At subsequent hops, there is no further analysis of the packet's network layer header: only the attached label needs to be examined. This label-processing that is performed in each LSR is denoted label swapping, as illustrated in Fig. 2.7: a packet carrying the label L_{in} arrives at an LSR. This label is recognised and subsequently used as an index in the forwarding table (i.e., look-up table) that

specifies the next hop and the new label to use. When forwarding the packet to the next hop (located at output port #2 in the figure), the old label is replaced with the new label, L_{out}, which is processed at the next LSR upon arrival. This replacement of an old label with a new label is called label swapping. It can be mentioned that both label recognition and label swapping can be performed all-optically; Sections 6.2.1 and 6.2.2 describe some novel schemes to perform these functionalities in a simple manner by using a single SOA-based interferometer as a logic gate. Finally, at the node where the packet leaves the MPLS network (the so-called egress node), the label will be stripped off, reducing the packet to the format it entered the MPLS domain in (e.g., an IP packet): this is called label popping.
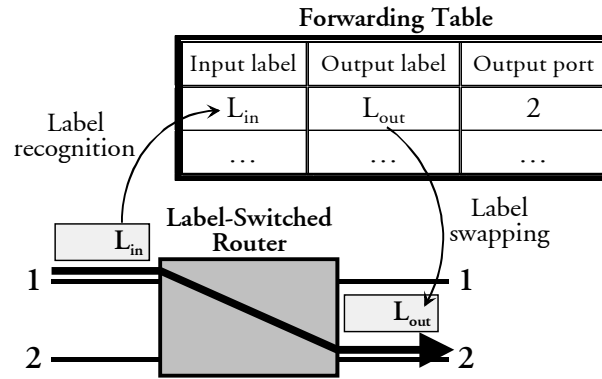
Fig. 2.7: The principle of label swapping in an MPLS network. In the LSR, the input label, L_{in}, in a packet is recognised and subsequently processed in a forwarding table. It is replaced by a new label, L_{out}, and the packet is forwarded to port #2.

Within the DAVID project, it has been decided that in order to ensure that the WAN is both flexible and future-proof, it should be structured in a manner that can handle various bit-rates, different levels of aggregation and functionality. From the MAN access to the core of the WAN the throughput of nodes increases and the granularity decreases. Close to the MAN, to cope with a lower level of aggregation and limited throughput compared to the core WAN, one solution is to consider electronic routers that can provide the required flexibility and the capacity. Then, going more deeply in the core of the backbone, optical switching nodes can provide a higher capacity as well as flexibility by employing a medium level of aggregation combined with the granularity of the optical packet. Finally, in the high levels of the WAN, one can imagine that the level of aggregation is sufficient to allocate dynamic wavelength paths. This view of the network enables definition of a hierarchical DAVID network architecture, as shown in Fig. 2.8. Within each level of the hierarchy, MPLS is used. As indicated, within level 1 electrical MPLS (EMPLS) is employed, level 2 uses optical MPLS (OMPLS) and level 3 uses MPλS. In this connection, it should be noted that the terms mentioned here are not standardised; they originate within the DAVID project.

An MPLS-like networking concept is used within each level of the DAVID WAN hierarchy because of the scalability of MPLS, its support of Quality of Service (QoS) at the network level, and because MPLS provides the tools for traffic engineering in the network: with MPLS one can set up explicit routes through the network to optimise the usage of available network resources, or to create distinct paths for different QoS classes. Moreover, MPLS supports the formation of hierarchies, which is beneficial for the DAVID concept. Each hierarchical level in Fig. 2.8 can be described as follows [38]:

Level 0: The MAN- as discussed in Section 2.2.1, the WDM dimension is used to establish a virtual topology, which is modified within the duration of a packet. At any time, the virtual topology within the MAN is controlled by the MAC protocol.

Level 1: The EMPLS level is composed of packet routers that perform electrical switching of packets (i.e., O/E/O conversion is performed), including label swapping. In DAVID, the EMPLS level is used at the periphery of the hierarchical WAN where the capacity of electronic routers is sufficient. Moreover, it acts as an adaptation level, which performs traffic aggregation [38] and advanced label processing between the MAN and the OMPLS level. Thus, the functionalities implemented by the EMPLS level are concentrated in the MAN-WAN Gateway, as shown in Fig. 2.1. These functions are not yet feasible within the optical domain, mainly because the required sophisticated buffering schemes can only be implemented in electronics. This is discussed in more detail in Chapter 3.

Level 2: At the OMPLS level, the packet payload is switched transparently within the optical packet routers as a means to enable higher throughput nodes (higher bit rates and more wavelengths). Packet forwarding is based on a look-up table, and the wavelength dimension is used to resolve contention, as far as possible. This is done by employing different wavelengths for packets bound simultaneously for the same output fibre. The OMPLS level uses optical packet forwarding to achieve a very high throughput. However, the functionality of optical packet switches is rather limited, why, in order to reach a high throughput, the granularity of the optical packets must be larger than the granularity used at the EMPLS level. The required packet duration is, among other things, dictated by the header processing time and the reconfiguration time needed by the optical switches. This has been studied extensively in connection with, e.g., the KEOPS project [39].

Level 3: If a larger extent of aggregation is beneficial than the OMPLS level can provide, an addition lambda-switched level may be the best solution. The MPλS level switches at the wavelength level with the wavelength assignment being performed by the MPLS control plane functions. Another use of the MPλS level could be in connection with service differentiation, where a specific lambda-switched path is set up for a service class requiring a superior QoS. It should be noted that the OPR architecture shown in Fig. 2.4 and Fig. 2.5 can support MPλS by allowing the set-up of dedicated circuits, meaning that the specific path through the optical switch is not reconfigured on a packet-by-packet basis. On this level, the MPLS label is equivalent to a specific wavelength, meaning that label swapping is equivalent to wavelength conversion. This means that all-optical wavelength conversion, which is the topic of Chapter 4, is a critical factor for the implementation of optical MPλS.

Practical implementation of the MPLS hierarchy is enabled by allowing packets to carry a number of labels, organised as a last-in first-out stack, denoted a label stack [37]. Each level in the hierarchy is associated with one label in the stack, and the packet is processed based on the top-level label at that moment. At the ingress to each level, a new label is pushed onto the stack, and at the egress, the label used within that specific hierarchical domain is popped off again.
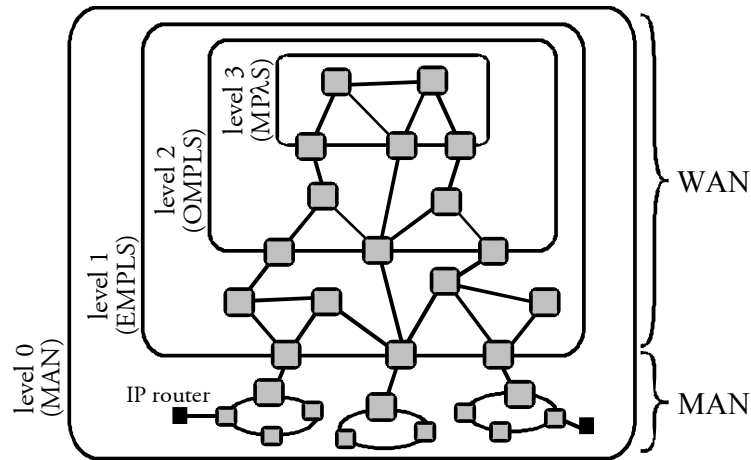
Fig. 2.8: The DAVID network hierarchy [38].

2.3 Summary

In this chapter, the implementation of an optical packet-switched network has been discussed, using the European research project DAVID as a case study. It has been argued that optical packet switching is advantageous for implementing packet-over-WDM due to the flexibility, scalability and high level of granularity is offers.

The DAVID network, which includes both a metro and core part, has been discussed. The metro network consists of rings exploiting WDM that interconnect optical packet ring nodes. A central Hub exploiting a MAC protocol takes care of the access control. A MAN-WAN Gateway performs the interfacing, which includes traffic shaping and aggregation, between the two network layers. Finally, in the core network a mesh topology interconnects optical packet routers that exploit WDM in conjunction with wavelength conversion as well as an optical fibre delay-line buffer for contention resolution.

The overall DAVID network concept is hierarchical, and employs MPLS in order to exploit the advantages of, e.g., traffic engineering and aggregation. A description of the different levels in the DAVID hierarchy has been given and the different levels involving electrical MPLS, optical MPLS as well as MPλS have been related to the DAVID network architecture.

Chapter 3

The traffic performance of an optical packet router

When dimensioning a packet switched network, there are two major aspects that need to be taken into account in order to ensure that information can be transferred from source to destination with an acceptable result and cost. Firstly, the physical performance of the network must be good, meaning that the data can be transmitted with a level of distortion (i.e., signal quality) that is acceptable for the operator/user. This may typically involve a required bit error rate (BER) at the receiver in the order of 10^{-12}-10^{-15}. This good signal quality is ensured through careful planning and design of the physical structure of the network, and will in today's commercial networks mean dispersion mapping, calculation of the end-to-end power budget, repeater spacing, etc. Secondly, the end-to-end traffic performance, which covers aspects relating to quality of service, must be acceptable. This means limiting the packet loss ratio (PLR)[13] to the order of 10^{-6}-10^{-10}, strongly depending on application. Furthermore, the end-to-end delay should be bounded. This factor is especially critical in the case of real-time traffic (e.g., telephony), where a delay of more than 25 ms [40] may degrade the quality. The network should be dimensioned to ensure an acceptable traffic performance for a well-defined offered traffic load. Again, the exact value required will vary, but a good design choice may be in the ~0.8 range. This high value is chosen in order to ensure that the bandwidth utilisation is kept high and the PLR reasonably low. Often the requirement of a high traffic load in conjunction with reasonable PLR will be difficult to meet in practice, especially under bursty traffic conditions, why careful dimensioning of the network switch nodes and traffic shaping will be necessary.

In this chapter the traffic performance of optical packet routers in core networks will be discussed, with the focus on minimising the PLR while keeping the component count and physical implementation feasible. In Section 3.1, the restraints placed on the packet router implementation due to limitations in optics will be discussed. Subsequently, two generic implementations of OPRs, relying on output and shared buffering, will be given and the traffic performance will be compared. Finally, in Section 3.3.3, a more in-depth analysis will be given of the traffic performance of the DAVID OPR, which was described in Chapter 2. The analysis will be based on a packet scheduling algorithm developed as a contribution to the DAVID project.

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[13] The packet loss ratio is defined as the ratio between data packets lost due to congestion/overload and the total number of packets transmitted.

3.1   The pros and cons of the optical packet router

Within the last years, much research has been devoted to the investigation of packet routers/switches implemented in the optical domain [17,25,26,41]. One of the major advantages of all-optical packet routers, as opposed to electronic routers involving O/E/O-conversion, is that scaling of the switch capacity can be achieved cost-effectively. Electronic IP/MPLS routers are now reaching capacities in the sub-Tbit/s throughput range with 10 Gbit/s line cards. However, reaching multi-Tbit/s throughput requires extensive parallelism and complex interconnection, which, although feasible, is not likely to be cost-effective [17]. Furthermore, power consumption and size are likely to be critical factors for the implementation of high-capacity electrical packet routers [3].

Thus, the advantage of all-optical high-capacity packet routers seems obvious; because the payload is switched transparently using, e.g., optical gates, complexity and power consumption is less dependent on bit rate. However, conversion to the electrical domain enables the exploitation of some very attractive features, which, as yet, are not practically feasible in the optical domain. One functionality that is quite complex, and therefore currently only feasible in the electrical domain is header processing, which, e.g., involves address recognition and -modification in data packets. Although much research is devoted to the optical implementation of these functionalities, as will be discussed in Chapter 6, the technology has not yet reached maturity, why pure optical packet switching is still years away. For medium-term network scenarios an opto-electronic approach where optical packet routers use electronic control and header processing is more realistic. This is also the scheme used in the DAVID research project, as discussed in Chapter 2. Packet switching requires a packet buffer memory in order to resolve contention between packets arriving simultaneously at the switch node input destined for the same output. This contention resolution is performed by delaying one packet with respect to the other, combined with wavelength conversion for handling wavelength blocking (wavelength conversion will be discussed in Chapter 4). An optical buffer would be desirable in order to preserve a high capacity all-optical data path. However, optical memory is at this time at a rather primitive stage, why it is necessary to resort to fibre delay-lines for packet storage. In general, the packet loss ratio is reduced when the delay-line length is increased. However, even small optical delay-line buffers with delays up to, e.g., ~20 time slots require long fibre spans in the range of ~4 km[14]. This is problematic due to issues such as cost, physical size and temperature

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[14] A packet time duration of 1 μs is assumed, corresponding to a length of 200 m. Packet durations in the range ~0.5-1.5 μs are deemed to be optimal for applications in WANs. For example in the European ACTS project KEOPS, a packet duration of ~1.65 μs was chosen [25], while a packet duration of 1 μs is tentatively chosen in the DAVID project.

stabilisation. In contrast, an electronic RAM for storage of hundreds of thousands of packets is easily implemented and the storage time can be chosen freely. Thus, the implementation of optical packet routers requires careful dimensioning of the optical buffer in order to ensure that the required traffic performance is achieved without compromising the practical implementation. This is the topic of the remainder of this chapter.

3.2 Comparison of optical packet router architectures

There exist three basic types of buffering schemes in electronic packet switch architectures that can also be implemented in the optical domain, namely input- and output queuing and shared loop-back buffering. With input queuing, a separate buffer is placed on each input of the switch and in the simplest case of first-in-first-out (FIFO) queuing, packets arriving at the inputs are forwarded to the correct output in turn. With output queuing, a buffer is placed at each output of the switch, and arriving packets are forwarded to the correct output before being buffered. In the electrical domain, there exists a trade-off between input and output queuing. For traditional input queuing, the throughput is limited[15] because a packet can be held up by another packet ahead of it in line that is destined for a different output. This phenomenon, known as head-of-line (HOL) blocking, is, however, not a problem nowadays due to the introduction of Virtual Output Queuing (VOQ), where each input buffer is divided into separate logical queues for each output [42], thus avoiding HOL. Unfortunately, VOQ requires a rather complex scheduling algorithm, why alternatives to strict VOQ are attractive. These issues do not exist for output queuing with which there, however, exists a problem of internal speed-up because several packets destined for the same output may arrive simultaneously. Thus, the processing speed in the electrical output buffer must be K times the external line rate if there are K input ports to the switch. This means that, in practice, a combination of VOQ and output queuing is used for electronic buffers [43], thus exploiting the advantages of each scheme.

An optical buffer is constructed using fibre delay-lines, why the problem associated with speed-up for output queuing is nonexistent. For this reason output queuing is advantageous to input queuing in all respects in the optical domain.

The third buffering scheme is shared buffering, in which the memory is pooled and shared completely between all outputs. This sharing allows a reduction in the total amount of buffering, however at the expense of a larger switching fabric, as will be seen in Section 3.2.2. Another potential problem with completely shared buffering is

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[15] Assuming FIFO queuing and independent, identically distributed arrival processes with destinations uniformly distributed over all outputs, the throughput is limited to $(2-\sqrt{2})\approx58.6\%$ [44].

that one heavily loaded output might monopolise use of the shared buffer, thus adversely affecting the performance of the other outputs [45]. This can, however, be prevented with an appropriately designed buffer scheduling algorithm.

3.2.1   Description of architectures

Based on the discussion given above, output and shared buffering are the two alternatives to be considered for optical packet switching. In Fig. 3.1 below are shown two generic optical packet router architectures relying on output buffering (Fig. 3.1a) and shared buffering (Fig. 3.1b), respectively. Both exploit WDM in conjunction with wavelength conversion for contention resolution. Note that the specific OPR architectures shown in Fig. 3.1 have been chosen as similar as possible in order for a fair comparison of the performance and space-switch size to be made in this section.

The architecture in Fig. 3.1a, denoted OPR a, has been proposed in the KEOPS project [18], wherein the traffic performance of optical packet switches using output buffering was investigated. The architecture, which has M in- and output ports, each carrying N wavelengths, can be divided into three main blocks: 1) The input section, where packets arriving at each inlet on the N fixed wavelengths λ_1-λ_N are separated through demultiplexing, and tuneable optical wavelength converters change the wavelength of each incoming packet to address free space in the N different queues made available by the FDLs at each output. 2) The space switch, which is used to access the correct output as well as FDL, and therefore the proper delay. 3) Packet buffers that are realised by FDLs. As seen from the figure, the space switch has the size $MNxM(B/N+1)$, where B is the number of packet positions in each output buffer and B/N is the number of fibre delay-lines. In the simplest case, the buffer is denoted degenerate[16] and consists of FDLs with length increments corresponding to one packet duration, i.e., the FDL has a length of one time slot, the second a length of two time slots, etc., and the last delay-line has a length of $B/N=D$ time slots. Logically, each output buffer functions as a set of N FIFO queues, as illustrated schematically in Fig. 3.2a. Here, an example is given where the number of wavelengths, N, is two and the number of FDLs, D, is three. As indicated, this means that, by exploiting WDM, the buffer can store six packets simultaneously in two logical FIFO queues. Note that this means that temporal synchronisation of packets at the same wavelength in different FDLs is not allowed, as this will result in contention at the output.

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[16] A non-degenerate FDL buffer will have delay-line length increments that are not equal to one timeslot. Often an exponential increment is used. As shown in [46] this may result in a good traffic performance with the use of fewer FDLs, however at the expense of an increased length, more complex packet scheduling and a larger probability of the packet sequence integrity being violated.

In Fig. 3.1b is shown an OPR architecture (denoted OPR *b*), which relies on a recirculating loop to implement the optical buffer. An architecture, which logically functions as the one shown here, has been proposed as part of the DAVID project (see Fig. 2.4). As in Fig. 3.1a, the architecture has M in- and output ports for transit or add/drop traffic, each carrying N wavelength channels. Furthermore, L in- and outlets to the switching fabric are allocated to a recirculating loop buffer, which is shared by all outlets. After demultiplexing, tuneable wavelength converters are used to address a free output wavelength channel at the desired outlet. Alternatively, in case of contention the wavelength converters may be used to address free wavelengths in the recirculating loop, depending on the loop structure. This will be discussed in more detail later. The space switch, having the size *(MN+L)x(M+L)*, is used to access the correct output port and wavelength channel or, in case of contention, the correct recirculating loop inlet. Note that wavelength converters are not placed at the loop outlets. This choice is made in order to allow a better comparison of the two architectures, as neither architecture allows full flexibility with respect to output wavelength as they are shown in Fig. 3.1; the output wavelength is partially determined by the queuing situation at hand. Regarding the
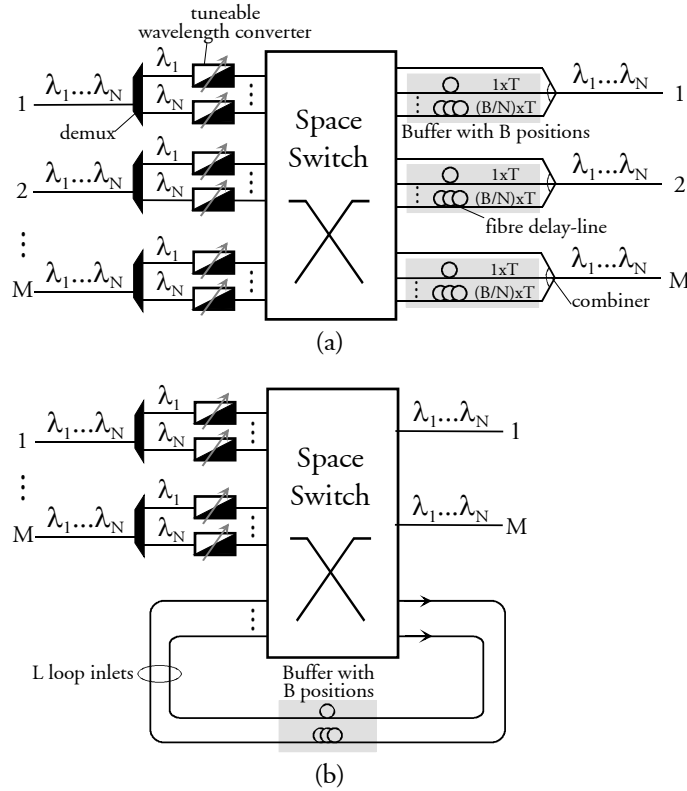
Fig. 3.1: Generic optical packet router architectures exploiting WDM for contention resolution. (a) Output buffering using fibre delay-lines. (b) Shared buffering using a recirculating loop.

structure of the recirculating loop, many different scenarios are possible. The simplest one is the fixed size loop, where all L inlets lead to the same delay D, thus enabling buffering of up to $B=LD$ packets simultaneously. This structure can be implemented, e.g., by employing just one fibre in the loop with L wavelengths and adding a demultiplexer and a multiplexer at the in- and output of the loop, respectively. Alternatively, L different fibres can be used with the same length, thus avoiding the use of costly (de)multiplexers but at the expense of a more bulky design. In both cases, the traffic performance of the loop buffer will be the same.

In Fig. 3.2b is shown the logical structure of the fixed size recirculating loop buffer in the case of $L=3$ fibres with length $D=3$ time slots, each carrying one wavelength per time slot, but exploiting two different wavelengths internally. As indicated, unlike the output queuing in Fig. 3.2a, the shared buffer does not forbid temporal overlap of packets at the same wavelength in different FDLs if they are destined for different output ports. The packet scheduling algorithm, which will be described in more detail in Section 3.2.2, ensures that packets exiting the loop simultaneously destined for the same output port will be wavelength converted to different wavelengths before buffering.
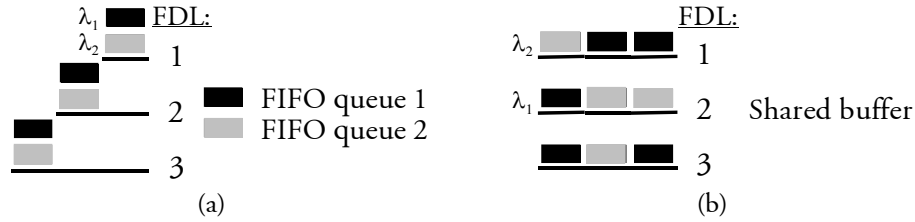
Fig. 3.2: Examples of the logical structure of the output buffer (a) and recirculating shared buffer (b) in Fig. 3.1a and b, respectively.

3.2.2   Component count and basic traffic performance

The same logical OPR architecture can be implemented physically in numerous ways. For example, the switching fabric within the logical architecture shown in Fig. 3.1b, which is used in the DAVID project, can be implemented in its simplest form by splitting out to an array of $(MN+L)x(M+L)$ SOA gates [18] and subsequent combining, or it can be implemented as shown in Fig. 2.5. This configuration is chosen to ensure a good physical performance, as discussed in Section 2.2.2. The same is the case for the architecture in Fig. 3.1a.

In this section a comparison of the component count of the two architectures in Fig. 3.1 will be given, assuming the most simple physical implementation of the architectures, which, as discussed above, may involve the employment of an SOA gate array with a size corresponding to the size of the space-switching fabric. This choice is made in order to ensure a fair comparison of the two architectures, as mentioned previously. Assuming that the space-switching fabric is implemented as discussed

above, a comparison of the component count and total buffer capacity for the switch is given in Table 3.1 below. As indicated, the required number of tuneable optical wavelength converters is identical for the two packet router architectures, and corresponds to the total number of input ports to the switching fabric that are dedicated to traffic arrivals. With respect to the space-switch size and total buffer capacity, the values for the two architectures differ.

	OPR a (Fig. 3.1a)	OPR b (Fig. 3.1b)
Buffer type	Output queuing	Shared recirculating loop
TOWC	MN	MN
Space-switch size (gates)	$MN \cdot M(D+1)$	$(MN+L)(M+L)$
Total buffer capacity	DNM	DL

Table 3.1: Comparison of OPR architectures in Fig. 3.1 with respect to component count and total buffer capacity. TOWC: tuneable optical wavelength converter. D is the maximum fibre delay-line length in the buffer and L is the number of loop inlets.

In order to compare the component count of the two architectures it is necessary to take the traffic performance into account, as the two factors are very closely coupled, as illustrated in Fig. 3.3. In Fig. 3.3a is shown the packet loss ratio as a function of the total buffer capacity for OPR a and b. Here, the performance for two different traffic arrival distributions, namely uniform traffic and bursty traffic with a mean burst length, β_{on}, of 4, is investigated. It should be noted, that the precise definition of the traffic arrival distributions will be given in Section 3.3.1. Here, they are only employed to give a basis for comparison of the two packet router architectures.

In Fig. 3.3b, the space-switch size is plotted as a function of the total buffer capacity. In both figures, the number of in- and outlets for transit traffic, M, is set to 6, and the number of wavelength channels, N, is equal to 32. These values are chosen to conform to the DAVID project, as discussed in Section 2.2.2. For OPR b, a fixed-size recirculating loop is chosen, and the fibre loop length, D, is set to 7 as this value of D ensures that the traffic performance for uniform and bursty traffic with $\beta_{on}=4$ is almost identical, while keeping an acceptable FDL length, as will be discussed in more detail in Section 3.3.3. It should be noted that the general traffic model for OPR b will be described in Section 3.3.1, while a more detailed description of the traffic model for OPR a is given in [18,47].

Fig. 3.3a shows that by using a recirculating loop, a significantly smaller buffer capacity is required to achieve a specific PLR for bursty traffic than if output queuing is used, while the result is almost identical for uniform traffic. For example, for a PLR $\leq 10^{-7}$ with bursty traffic, a buffer capacity of 217 packets is sufficient if OPR b is chosen, while OPR a requires a total capacity of 960 packets. It should be noted that these values for the capacity are employed because PLR$=10^{-7}$ corresponds to a non-integer

number of FDLs. Thus the required number of FDLs is rounded up to the nearest integer, corresponding to *DMN*=5x6x32 for OPR *a* and *DL*=7x31 for OPR *b* (see Table 3.1). Finally, it should be mentioned that the results in Fig. 3.3a for OPR *a* with uniform traffic are obtained analytically using the model described in [18].

Another important factor for the practical feasibility of an OPR architecture is the robustness of the configuration towards varying traffic arrival distributions. A large degree of robustness is important, as it is virtually impossible to predict the exact traffic characteristics in a practical network. Furthermore, the core nodes must be able to cope with some degree of change in the traffic pattern without compromising the traffic performance. Focusing on Fig. 3.3, it can be seen that for the recirculating loop buffer, bursty traffic only causes very minor increase in PLR compared to uniform traffic. This is in contrast to the output buffer, where bursty traffic with β_{on}=4 requires more than six times the buffer capacity to handle than uniform traffic. This robustness of the recirculating loop towards bursty traffic can be explained as follows: because the buffer is a shared medium, bursts are absorbed alternately from the OPR inputs. The output buffers cannot exploit this, as they are independent, why at some instances some output buffers may be heavily overloaded, while others are empty. As an added note it can be mentioned that results in Section 3.3.3 verify the tendencies shown in Fig. 3.3a for OPR *b*, while the difficulty of OPR *a* in handling bursty traffic is verified in [19,47,48], where it is shown that the PLR increases with orders of magnitude as the traffic burstiness is increased. This indicates that if output buffering is used, a larger degree of traffic shaping is necessary as compensation, e.g., at the interface between the client layer and the MAN (see Fig. 2.1).

However, as shown in Fig. 3.3b, there is a significant advantage associated with the output buffer. It is seen that a significantly larger space-switch is required to implement a buffer with a given total capacity if the recirculating loop is used than if output queuing is used. This is an important factor for determining the total cost of an optical packet router, why limiting the space-switch size is of great importance. The results shown in Fig. 3.3b should, however, be compared with Fig. 3.3a in order for a fair comparison of the two OPR configurations to the made. Using the same example as previously (i.e., bursty traffic), insertion of the values for total buffer capacity in Table 3.1 gives a required space-switch size of 6912 to achieve a PLR of equal to or less than 10^{-7} with OPR *a*, while OPR *b* requires a space-switch size of 8251. This indicates that there exists a trade-off between the space-switch size and robustness towards bursty traffic for the two buffering schemes, which must be taken into account when choosing the OPR configuration in a practical network.
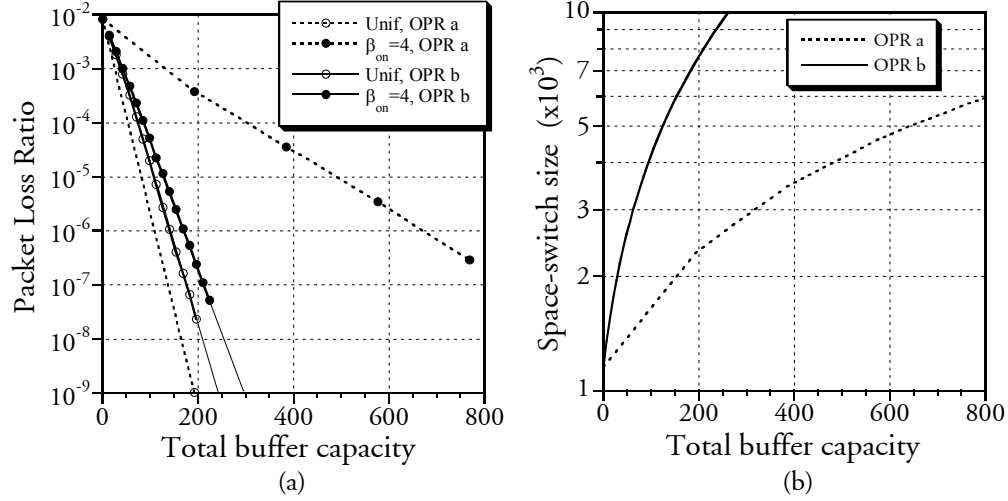
Fig. 3.3: (a) Packet loss ratio versus total buffer capacity for OPR configurations *a* and *b*. Results are shown for uniform traffic and bursty traffic with mean burst length, β_{on}=4. (b) Space-switch size versus total buffer capacity for OPR *a* and *b*.

Finally, a point should be made about the preservation of packet sequence integrity, which is not taken into account in the simulations. For both OPR configurations, although especially for the recirculating loop, this may result in packet sequence violation. Preservation of the sequentiality, which relates specifically to upholding the order in which packets from the same client (i.e., source) flow are transmitted, is an important aspect for the end-to-end performance of the network. If the sequence is not kept, an electrical buffer will have to be placed at the WAN-MAN gateway to allow resequencing. This increases the complexity and cost, which is undesirable. Fortunately, there are some aspects in relation to traffic aggregation and shaping in the DAVID network that argue that packet sequence violation may only occur very seldom. As discussed in Sections 2.2.1 and 2.2.3, traffic aggregation occurs both at the interface between the legacy network (LAN) and the MAN, and at the gateway between the MAN and WAN. A traffic aggregation unit aggregates many incoming packet flows into fewer (higher bit rate) outgoing flows with the aid of bundling queues [38]. Each queue may, e.g., determine a specific destination and/or class of service (CoS). Outgoing packets from the queues are transmitted in an order that is determined by the packet scheduling algorithm, which may perform traffic shaping to smooth out the aggregated flow. Depending on the ratio between the bit rate of the incoming packet flow and the bit rate of the aggregated flow, the number of queues in the aggregation unit, and the use of traffic shaping, the interarrival time between two optical packets carrying data from the same client flow may be relatively large because all packets from a specific client are aggregated in one bundling queue during the transmission from other bundling queues. Thus, the problem of sequentiality preservation in the OPR may, to a large extent, be nonexistent in practice.

It should be mentioned that within the DAVID project, the main motivation for choosing a shared buffer OPR architecture instead of the output buffer architecture that was used in the KEOPS project is not related to the pros and cons of the two buffering schemes that have been discussed until now. The OPR architecture in the DAVID project, as shown in Figs. 2.4 and 2.5, is chosen because it allows a high throughput, in contrast to the KEOPS architecture [25]: in the KEOPS architecture, the switch uses output buffering at a logical level, but physically, the buffer is shared. This is enabled through the use of WDM with *NM* internal wavelengths on each fibre-delay line in conjunction with broadcasting of every packet to every FDL as well as output. Thus, internally, the capacity of the KEOPS switch is very high, but externally, it is not. Furthermore, during the KEOPS project it was identified that the total throughput of the KEOPS switch is limited to 160 Gbit/s, which is much less than what is the target of the DAVID project (1.92 Tbit/s, see Section 3.3.3).

3.3 The DAVID optical packet router

In this section, the traffic performance of a WAN optical packet router will be given, using the DAVID OPR as a case study. In Section 3.3.1, the simulator used to model the traffic arrivals and packet buffering in the recirculating loop will be discussed. After this, a description of the proposed packet scheduling algorithm will be given in Section 3.3.2, and results of the traffic simulations will be shown in Section 3.3.3.

3.3.1 General traffic model overview

The simulation model can basically be split into two parts, namely the traffic arrivals and the packet scheduling. The latter, which takes care of packet forwarding to the correct outlet, buffering and packet dropping in case of overload, will be discussed in more detail in the next section. Here, the focus will be on the general model implementation and traffic arrivals.

The nomenclature used in this section will be the same as in Section 3.2, Fig. 3.1b: *M* is the number of input and output fibres for traffic arrivals, *N* is the number of wavelength channels per in- and output fibre, *L* is the number of in- and outlets for the recirculating loop buffer, and *D* is the maximum delay, i.e., largest fibre length, in the loop. The following assumptions are made concerning the traffic arrivals:

- **Packet format:**

  A *slotted, fixed duration packet format* is assumed, in agreement with the DAVID project concept. It has been shown in [47,49] that slotted (synchronous) operation of the OPR by far gives the best traffic performance. Furthermore, in [50] is has been shown that fixed duration packets also ensure a better performance than variable length packets. In both cases, the reason for this is that the buffer capacity cannot be exploited optimally for storing unslotted and/or variable length packets [47,49,50].

- **Traffic differentiation:**

  In a practical network, traffic arriving at the M inlets may be transit traffic, thus originating from the WAN. Alternatively, the traffic may be add-traffic originating from the MAN. It is obvious that the characteristics of the traffic arrivals will depend on the origin, however, for simplicity this is not taken into account; transit and add-traffic are treated the same. Furthermore, service differentiation, in which some types of traffic are given a higher priority than others [51], is not investigated, either. This is, however, an important factor, which will be taken into account in the DAVID project. Thus, it is assumed that *each of the MN traffic sources is identically, independently distributed (i.i.d.).* Furthermore, it is assumed that there is an *equal probability, 1/M, of arriving traffic being destined for each of the M output ports.*

- **Packet arrival distributions:**

  Two different types of traffic, namely uniform (random) traffic and bursty traffic are investigated. In any case, a traffic load of ρ is assumed for each of the MN sources.

  <u>Uniform traffic:</u>

  Independent uniform traffic refers to a traffic pattern where packets arrive according to a Bernoulli process and packets arriving at the inputs are independent of each other with uniformly distributed destinations, as mentioned above. The Bernoulli process is a good approximation for slotted traditional teletraffic[17] (with Poisson arrivals as the unslotted equivalent), where it is exploited that multiplexing a large number independent traffic streams results in a Poisson (i.e., smooth) process [52]. Thus, uniform traffic represents the best-case situation with respect to the traffic conditions, thereby setting a lower bound on the PLR.

  Here, uniform traffic is modelled by allowing the NM independent sources to generate packets with geometrically distributed interarrival times. The interarrival times are found using the Monte Carlo method [53] in conjunction with the geometric distribution function:

  $$F(x) = P(X \leq x) = 1 - (1 - \rho)^x$$

  (3.1)

  <u>Bursty traffic:</u>

  Bursty traffic is, unlike uniform traffic, characterised by longer active periods in which the source transmits to one specific destination, followed by an idle period in which the source is inactive. A bursty traffic model is used to simulate more realistic data-centric traffic, which places severer demands on the OPR architecture in order to ensure an acceptable traffic performance.

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[17] I.e., Plain Old Telephone Service (POTS).

Here, it is assumed that both the active and idle periods of the bursty traffic sources are geometrically distributed. During the active period it is assumed that packets arrive in consecutive time slots. Furthermore, it is assumed that there is at least one packet in each active burst, but the duration of the idle period can be zero. The burst lengths are assumed to be statistically independent. The active and idle periods are characterised by the parameters r_{on} and r_{off}, respectively, where the mean (active) burst length is $\beta_{on}=1/r_{on}$ and the mean idle duration is $\beta_{off}=1/r_{off}-1$. The relation between the offered load, ρ, and the mean active and idle period lengths is given by: $\rho=\beta_{on}/(\beta_{on}+\beta_{off})$. Note that the difference between the definition of β_{on} and β_{off} is introduced in order to allow the duration of the idle period to be zero [54]. This choice is made because it is deemed to be the most realistic; nothing in the DAVID concept or telecommunications networks in general prevents packet bursts from being generated immediately after each other.

In the simulations, the mean burst length, β_{on}, and the traffic load are set. Thereby, r_{on} and r_{off} are determined. Using the Monte Carlo method, the length of the active period, x_{on}, is found in the simulations by inserting r_{on} in the expression for the geometric distribution (3.1) in the place of ρ:

$$F(x_{on}) = 1 - (1 - r_{on})^{x_{on}}, \qquad x_{on} \in N \tag{3.2}$$

It should be noted that because a slotted format is used, the value for x_{on} found using the Monte Carlo method is rounded up to the nearest whole number.

The random variable X_{off} is derived from a geometric distribution X'_{off} with mean value $1/r_{off}$ as $X_{off}=X'_{off}-1$. This expands the set of possible values of x_{off} to include 0 (in addition to 1,2…), as required. Thus the distribution function for the idle period length is:

$$F(x_{off}) = 1 - (1 - r_{off})^{x_{off}+1}, \qquad x_{off} \in N_0 \tag{3.3}$$

Note that $1/r_{off}=1+\beta_{off}$, hence the mean value of X_{off} equals $E\{X'_{off}\}-1=1/r_{off}-1=\beta_{off}$.

3.3.2   Description of packet scheduling algorithm

The traffic performance of the DAVID WAN OPR is evaluated using two different recirculating loop configurations: a fixed-size loop buffer, which was described in Section 3.2.1, and a degenerate loop buffer. The degenerate loop buffer is analogous to the degenerate output buffer described in Section 3.2.1, except that temporal overlap of packets at the same wavelength in different fibre delay-lines is allowed if they are destined for different output ports.

The following procedure is followed in each time step (corresponding to a time slot duration): the number of packets at the input ports and loop outputs destined for each

outlet is determined. If this number exceeds N, packets will need to be buffered and/or lost. The number of packets for each destination to be buffered in the loop is determined by using the algorithm discussed in the following. If more than L packets require buffering, the remaining are lost.

Packet scheduling is performed using a representation of the recirculating loop as shown in Fig. 3.4a for the fixed loop configuration and in Fig. 3.4b for the degenerate loop. In the schematic, packets are inserted in the dark grey squares and each time step they move one square to the left until they reach the column denoted OUT, whereafter they are routed to the destination outlet or back to the loop input, depending on the situation at hand. This means that packets in the same column leave the loop at the same time. It should be noted that for the degenerate loop in Fig. 3.4b, the physical extent of the FDLs is limited to the grey squares; placement of packets in the white squares is prohibited.
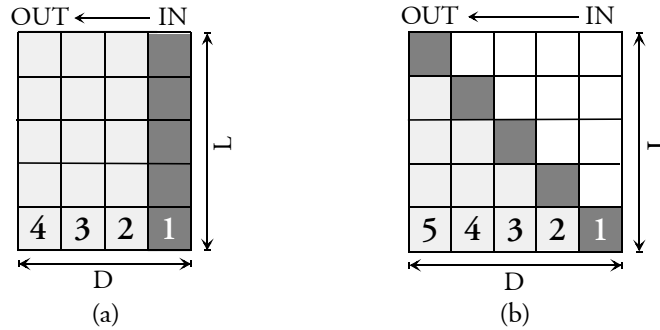
Fig. 3.4: Representations of recirculating loop used for packet scheduling in DAVID WAN OPR. Packets are inserted in dark grey squares and shifted one square to the left in each time step (slot). (a) Fixed-size loop for L=5 and D=4. (b) Degenerate loop for L=5 and D=5. Placement of packets in the white squares is prohibited.

In the simulations, the recirculating loop is considered a completely shared medium; packets from all sources to all destinations have equal access. The traffic performance of the recirculating loop is optimised by employing the following procedure:

- **Minimisation of delay:**

  The number of round-trips that a packet must take in the loop is kept as low as possible. This is done to minimise delay as well as to retain the packet sequence integrity. No more than R round-trips are ever necessary if the following criterion is obeyed: $RN \leq L$ (assuming all packets have the same priority)[18]. Thus, with

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[18] This can be understood by considering the following example: assume N=2 and L=4. Thus, a maximum of 2 packets can exit one single outlet at any time. If more than 2 packets are destined for a specific outlet some must be looped. Assume 7 packets arrive at one time destined of a specific outlet. 2 packets are routed straight to the outlet, 4 are looped and 1 is dropped. After traversing the loop, 2 of the 4 packets are routed to the outlet and the remaining two are looped again. These will be routed to the outlet after exiting the loop.

N=32, as assumed for the DAVID OPR, no more than one loop round-trip will ever be necessary if L is kept equal to or below 32. For L>32, packets already in the loop have first priority to exit the OPR over packets just arriving at the OPR input ports.

For the fixed-size loop, optimisation of round-trip delay is not an option. For the degenerate loop, the delay-line resulting in the shortest delay possible will be chosen. It should be mentioned, however, that delay minimisation has second priority to minimisation of packet loss, which is achieved through, e.g., load balancing.

- **Load balancing:**

  Load balancing is important to achieve a low packet loss. This is done during buffering by choosing the loop input that results in the minimum number of packets destined for the same OPR output port exiting the loop simultaneously. This is straightforward for the fixed-size loop, as all packets entering the loop at the same time also exit the loop at the same time. However, for the degenerate loop this involves keeping track of the number of packets for a specific destination in each column in Fig. 3.4b. The FDL that ensures placement in the column with the smallest number packets for that specific destination is chosen. If different FDLs give the same result the one that corresponds to the smallest delay is chosen.

  In the case of overload, i.e., where packets must be dropped, a form of traffic shaping is achieved by dropping packets bound for the most heavily loaded destinations.

  The above-mentioned procedures allow a minimisation of the packet loss because they ensure that the number of packets to be routed to each destination at any time is balanced as much as possible.

- **Maximisation of loop utilisation:**

  A final method that is used to achieve a low packet loss, is the maximisation of the loop utilisation. This is done by dropping packets at the OPR inlets instead of packets in the loop in case of overload, thus ensuring that the loop capacity is not wasted.

It should be mentioned that decisions concerning routing of packets to the output ports and placement of packets in the loop buffer are taken in turn by port number in a Round Robin-fashion, based on the procedures given above. For example, if packets need to be looped, a single packet destined for output port #1 is serviced first, then for port #2, etc. When all ports have been serviced once, output port #1 is serviced again, and so on, until all loop positions have been filled.

Obviously, practical control of the OPR using the packet scheduling algorithm discussed above requires considerations to be made concerning, e.g., the choice of

wavelength to convert an input packet to. This can be done by keeping track of the wavelengths employed for all packets in the loop. The wavelengths of arriving packets forwarded directly to an output port are selected by examining the wavelengths of packets at the loop exit bound for the same outlet, and choosing a free wavelength. The same is the case for wavelength allocation at the loop input. It should be noted, as discussed in Chapter 2, that if wavelength converters are placed both at the OPR input and output, it is only necessary to keep track of the wavelengths used internally in the loop; wavelength correlation between the loop and input ports is not necessary.

3.3.3   Traffic performance

Using the simulation model described in the previous sections, calculations of the packet loss ratio for different packet arrival distributions and loop configurations have been made.

The model has been verified in the following way:

The arrival processes: the results obtained using the arrival process-related part of the developed model in conjunction with a queuing model of OPR *a* have been compared with an analytical model described in [18] for uniform traffic and results from [19] for bursty traffic. The good agreement verifies the accuracy of the modelling of arrival processes.

The recirculating loop: in [55], the traffic performance of a switch node with a recirculating loop has been evaluated for uniform traffic with N=1 (i.e., without employment of WDM for contention resolution) and varying L. Results of the developed model show good agreement with results in [55], thus verifying the model of the loop and packet scheduling algorithm.

The traffic performance of the DAVID WAN OPR has been assessed using parameters defined within the DAVID project. A maximum-size switching fabric of 256x256 is assumed, giving a total capacity of 2.56 Tbit/s for a single channel bit rate of 10 Gbit/s. Six ports, each carrying 32 wavelengths, are dedicated to transit/add-drop traffic (giving a total throughput of 1.92 Tbit/s). This leaves a maximum of 64 in- and outputs for the recirculating loop. The loop configuration can be varied freely. However, it is necessary that the maximum FDL length in the loop is kept below 50 time slots, and a maximum length kept in the range 10-20 time slots is desirable. This is due to stability and size-issues, as discussed previously. Finally, a packet loss ratio of 10^{-6} or less is required. Thus, the parameters used are as follows: M=6, N=32, $L \leq 64$, D_{max}=50, D_{opt}=10-20, PLR=10^{-7}.

Fig. 3.5 shows the packet loss ratio as a function of the number of in- and outputs (L) to a fixed-size recirculating loop. In Fig. 3.5a are shown results for a FDL length, D, of 1 time slot with the traffic arrival distribution as a parameter. As indicated, the traffic performance under bursty traffic conditions is much poorer than for uniform

traffic. As an example, only ~25 inputs need to be allocated to the loop in order to ensure a PLR~10^{-7} for uniform traffic, while L~64 are needed for bursty traffic with a mean burst length of 2. Bursty traffic with a mean burst length of 4 cannot be accommodated within the DAVID requirements using this loop configuration. This difference in performance is well known, and can be explained as follows: for bursty traffic, an active period will have a length in mean that is greater than one. In the event that a relatively large number of sources are active simultaneously, packets will be dropped due to buffer overload. For bursty traffic, this period of overload will occur over multiple time slots, in contrast to the situation for uniform traffic, thus increasing the PLR. The subsequent idle period will not be registered by the loop buffer due to its limited size (D=1), and therefore limited memory.

Thus, it may seem intuitively obvious that an increase in FDL length, D, must improve the performance of the recirculating loop for bursty traffic, as the correlation is reduced. This is verified in Fig. 3.5b, which shows results for uniform traffic with D=1, bursty traffic with β_{on}=2 and D=7, and bursty traffic with β_{on}=4 and D varied between 1 and 7. As indicated by the results for β_{on}=4 (triangles), an increase in D reduces the PLR significantly. It is also seen that the improvement in PLR saturates as the loop FDL length is increased; changing D from 3 to 5 time slots reduces the loop size by 18 inputs from L~54 to L~36, while a further increase of D to 7 only reduces L further by 5 to L~31 (@ PLR=10^{-7}). The results shown for uniform traffic represents a lower bound which the PLR for bursty traffic converges towards as the loop FDL length is increased. Hence, the level of correlation is reduced.
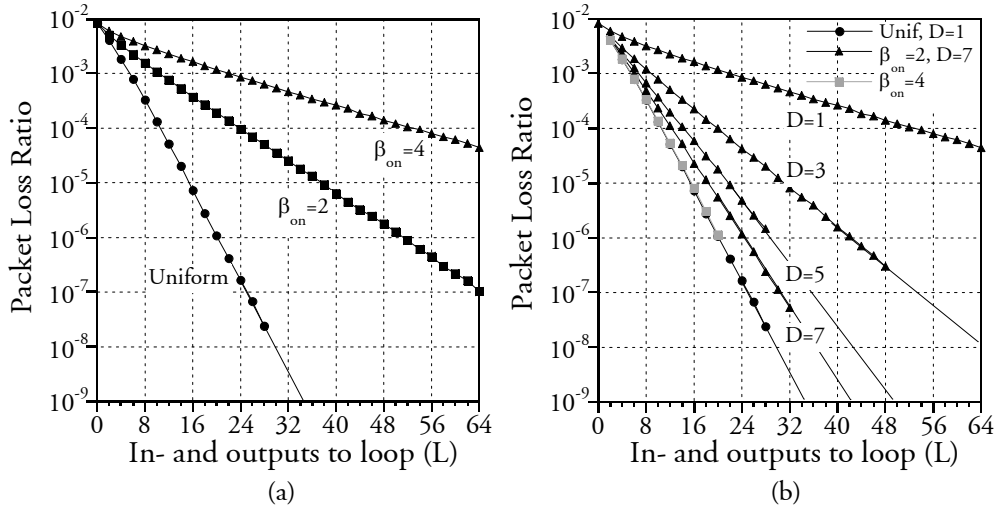
Fig. 3.5: Packet loss ratio versus number of inputs (L) to a fixed-size recirculating loop. (a) Results for D=1 under uniform and bursty traffic conditions with mean burst lengths, β_{on}, of 2 and 4. (b) Results for uniform and bursty traffic with β_{on}=4 for D varied.

It can be seen by comparing with the results for β_{on}=2 (grey markers) and D=7 that a good performance can be obtained for a relatively lower value of D if the traffic is less bursty; with β_{on}=2 and D=7 the performance is almost identical to the case for uniform traffic. It should also be noted that increasing D for uniform traffic does not reduce the PLR, as no correlation exists between the arriving packets.

The improved performance of the recirculating loop under bursty traffic conditions when the FDL length is increased can be explained as follows: when a relatively large number of sources are active simultaneously, the loop buffer must be exploited. When the packets originating from the start of the active period reach the loop exit, they are not correlated to the packets arriving at the switch inputs, whereby the packet loss is reduced. The actual choice of FDL length, D, is of course dependent on the desired traffic performance. However, the FDL length, D, should be at least equal to the mean burst length. It can be mentioned that (β_{on}, D) =(2,3), (β_{on}, D) =(6,11), and (β_{on}, D) =(8,15) gives almost the same PLR as (β_{on}, D) =(4,7).

The above-mentioned results seem to indicate that as the mean burst length is increased, the efficiency of the traffic smoothing achieved with the fixed loop is reduced. Thus, relatively larger FDL lengths are required for a good traffic performance as the traffic becomes more bursty. It should, however, be mentioned, that a design parameter within the DAVID project states that traffic aggregation at the MAN-WAN gateway, and especially traffic shaping at the client layer interface (see Fig. 2.1), should be so effective that traffic within the WAN is limited in burstiness to 2<β_{on}<4. It is, however, not as yet determined whether an acceptable degree of traffic smoothing can be achieved if the traffic in the MAN exhibits self-similarity[19]. Furthermore, the literature is also unresolved in this respect. In [56] it is demonstrated that shaping only has a limited effect on the queuing performance of self-similar traffic, while in [57] it is shown that traffic shaping may improve the overall traffic performance without removing the long-range dependency. However, the effect of large-scale traffic aggregation has not been investigated.

In Fig. 3.6 the traffic performance with an offered load, ρ=0.8, 0.6 and 0.4 for the fixed loop configuration is compared with the performance for the degenerate loop (see Fig. 3.4b for reference). Fig. 3.1a shows results for the fixed-size loop with D=1 for uniform traffic and D=7 for bursty traffic. As indicated, the requirements to the number of in- and outputs allocated to the loop are greatly relaxed if the traffic load per input channel is reduced from 0.8 to 0.6. For a PLR of 10^{-7}, L can be reduced by 16 from 25 to 9 by a limited reduction in the load from 0.8 to 0.6. By inserting these

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[19] Self-similarity: the autocorrelation function of a self-similar process follows a power-law, as opposed to an exponential decay (as exhibited by traditional, e.g., Poisson, traffic). This means that with self-similar traffic, there is no natural length of a burst, and active and idle periods can, with a non-negligible probability, be very long. This places severe demands on the buffer capacity.

numbers into the expression in Table 3.1 for the space-switch size for OPR b, it can be seen that this corresponds to a 55% reduction in the space-switch size (from 6727 to 3015). This indicates that significant savings are possible in OPR component count if the WAN is dimensioned for lower traffic loads than 0.8. In fact, one solution that is investigated within the DAVID project is the employment of an OPR structure that exists of parallel planes, each taking care of a fraction of the traffic load [58]. According to the above-mentioned results, this load division should be effectively able to reduce the total optical component count. Whether or not this is the most cost-effective overall network solution is, however, dependent on many factors, e.g., the added complexity involved with controlling multiple parallel planes. Thus, a more in-depth analysis is required to determine the optimal solution.

In Fig. 3.6b are shown results for the degenerate loop. By comparing these results with the results for the fixed-size loop, it can be seen that the performance for a load of 0.8 is better with the degenerate loop than the fixed loop; for uniform traffic, only 19 inputs need to be allocated to the degenerate loop, while 25 inputs are necessary for the fixed loop. This is due to the fact that the placement of packets in the degenerate buffer offers more flexibility with respect to delay choice; there exists only one alternative in the fixed loop. This gives some degrees of freedom that can be used to reduce the PLR. It can be seen, however, that this changes as the load is reduced to 0.6. For bursty traffic with $\beta_{on}=4$ the performance is slightly better for the fixed buffer than for the degenerate buffer, while the performance is almost identical for the other two traffic distributions. Furthermore, the difference in the performance of the fixed buffer for the three traffic distributions
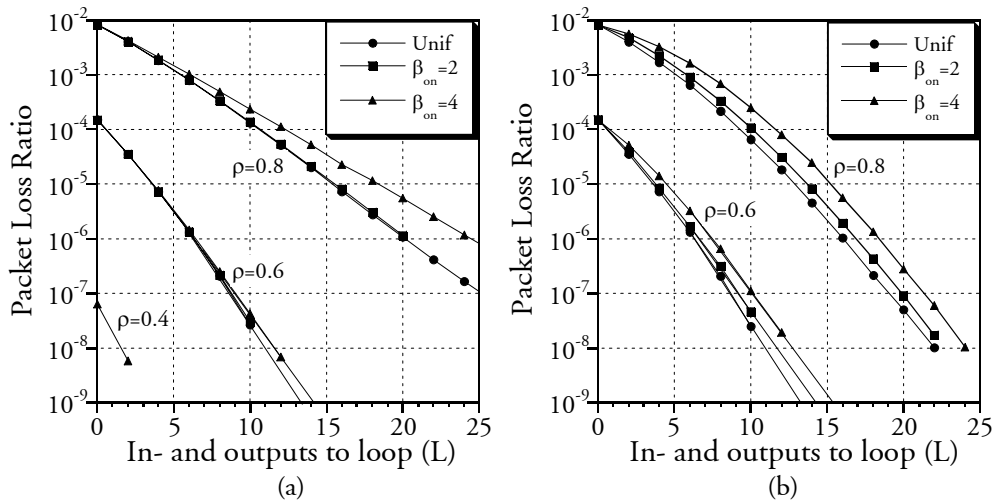
Fig. 3.6: Packet loss ratio as a function of the number of inputs to loop (L) for offered load, ρ=0.8, 0.6 and 0.4. Results are shown for uniform traffic and bursty traffic with β_{on}=2 and 4. (a) Fixed size loop with D=1 for uniform traffic and D=7 for bursty traffic. (b) Degenerate loop.

is very small, indicating the robustness of the fixed loop configuration at smaller traffic loads. As discussed previously, this is a very important factor for the practical implementation of a network, as it is virtually impossible to predict the exact traffic characteristics in practice.

As a final point, it should be mentioned that, of course, the decision concerning choice of recirculating loop configuration should not be limited to the traffic performance; also the packet scheduling complexity should be taken into account. Going back to Fig. 3.4, it can be seen that the packet scheduling algorithm required to make employment of the degenerate loop effective is much more complex than for the fixed loop. This is because packets in the fixed loop experience the same delay, meaning that a decision only has to be made concerning which packets to buffer, and not where to place them. Thus, only the destination of packets arriving to the loop will have to be registered. If, however, the degenerate loop is employed, a decision also has to be made concerning where to place the packets in the loop (i.e., which delay to choose). Thus, the destination of every packet in the loop must be tracked, making the loop control much more complex.

3.4 Summary

In this chapter, the focus has been on the traffic performance of WAN optical packet routers. A comparison of the performance when using output- and shared buffering has been made for two generic OPR architectures, and the corresponding required space-switch size has been taken into account. Furthermore, a simulation model, that has been developed to investigate the performance of the OPR architecture employed in the European research project DAVID, has been described, and results gained from the model have been discussed.

It has been demonstrated that using by a recirculating loop buffer a much smaller total buffer capacity is required to achieve a given packet loss rate than if a fibre delay-line based output buffer is used. Moreover, bursty traffic only causes a minor increase in the PLR compared to uniform traffic, in contrast to the output buffer, where bursty traffic with β_{on}=4 requires more than six times the buffer capacity to handle a given PLR than uniform traffic. This robustness is inherent of the recirculating loop buffer; because the buffer is a shared medium, bursts are absorbed alternately from the OPR inputs. However, a drawback to the recirculating loop buffer is that it requires a larger switching fabric to be implemented, thus compromising the optical component count and therefore cost-effectiveness. Thus, there exists a trade-off between the two buffer configurations that must be taken into account when choosing the OPR architecture for a practical network.

The remainder of the chapter has focused on the traffic performance of the DAVID OPR using the parameters specified within the DAVID concept: a maximum-size switching fabric of 256x256 with 6 ports carrying 32 wavelengths dedicated to transit

traffic and up to the remaining 64 switch inlets dedicated to the recirculating loop buffer. The performance has been evaluated under uniform and bursty traffic conditions for a fixed-size- and degenerate loop buffer. The simulation results indicate that a PLR of 10^{-7} can be achieved for uniform traffic with ~19 switch inlets (L) allocated to the loop if a degenerate buffer is used, while 25 are necessary for the fixed loop (at a traffic load of 0.8). These values are well within the requirements in the DAVID project. Furthermore, when the offered load is reduced to 0.6, the difference between the performances of the two loop configurations becomes negligible and a considerable reduction in the required loop size (L), corresponding to a 55% reduction in switching fabric, is possible. This indicates the efficiency of the recirculating loop and is worth considering when network dimensioning is performed.

For the fixed-size loop, keeping L fixed but increasing the FDL length can reduce the PLR for bursty traffic. Thus, a performance that converges towards the situation for uniform traffic can be achieved in a very simple manner; e.g., for a mean burst length of 4, a FDL length of 7 enables a PLR of 10^{-7} with just 30 inlets allocated to the loop. This indicates the robustness of the recirculating loop with respect to the traffic pattern.

Chapter 4

Interferometric wavelength conversion

As discussed in the introduction to Chapter 2, today's telecommunications networks deploy an "opaque" architecture where the switching fabric in the network nodes is electronic, i.e., O/E/O conversion is performed at each node [13]. However, as the capacity requirements grow and optical solutions mature, all-optical cross-connects are becoming commercially available. One very important limitation connected to the initial product announcements of OXCs[20] is the lack of wavelength conversion. Extensive research has been made in determining the importance of wavelength conversion in wavelength-routed networks (e.g., employing MPλS as discussed in Chapter 2). Most researchers agree that wavelength conversion is necessary to ensure a high bandwidth utilisation. In [9] simulations on a test network with OC-48 (2.5 Gbit/s) services have demonstrated that a significant penalty (2-3 times as much distance-weighted point-to-point capacity) is required if wavelength conversion in not available. This is because wavelength conversion enables flexibility, meaning that wavelength allocation can be done on a local instead of global scale, thus enabling more efficient bandwidth usage [8]. Furthermore, in optical packet switched networks, wavelength conversion is critical to resolve contention in switch nodes, thus dramatically reducing the buffer capacity needed for a specific packet loss rate, as discussed in Chapter 3. Finally, as will be demonstrated in Chapter 5, all-optical IWCs, which are prime candidates for future optical networks, can be employed for 3R regeneration in conjunction with wavelength conversion. This attribute is necessary for ensuring an acceptable signal quality at the destination [13,17]. For all these reasons, all-optical wavelength converters are key components in future optical networks.

In this chapter, the focus will be on interferometric wavelength conversion. In Section 4.1, the system requirements to wavelength converters in general will be discussed, while different techniques for wavelength conversion will be described in Section 4.2 with the focus mainly on IWCs. Subsequently, results for standard wavelength conversion performed with the SOA-based Mach-Zehnder interferometer (MZI) and Michelson interferometer (MI) will be given, and the differential control scheme, which increases the speed capabilities, will be discussed. In Section 4.5 will be given results obtained with a type of IWC, which allows co-directional conversion to the same wavelength without use of a filter. Finally, a novel scheme for wavelength conversion will be described in Section 4.6.

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[20] In this report, it is assumed that an OXC has an all-optical switching fabric. This is in contrast to the definition that some vendors employ, where the switching fabric may be electronic.

4.1 System requirements to wavelength converters

In practice, the requirements to wavelength converters will of course depend on the network structure. However, there are some criteria that are often noted in connection with wavelength conversion. The list below gives some of the most relevant wavelength converter specifications:

- Negligible insertion penalty[21]
- Bit rate transparency
- Wavelength independent operation and large optical bandwidth
- Good conversion efficiency[22]
- Polarisation independence
- High input power dynamic range (IPDR)[23]
- Low frequency chirp
- Format transparency
- Good cascadability performance
- Low electrical power consumption
- Low optical input power levels
- Mechanical stability
- Low temperature dependency
- Simple and cost-effective implementation
- Good reproducibility

Most of the points in the list are more or less self-explanatory. In the next section the advantages and disadvantages of some of the most attractive wavelength conversion techniques will be discussed, with reference to the above list.

4.2 Different techniques for wavelength conversion

The straightforward way to perform wavelength conversion, and the method that is employed in commercial networks today[24], is opto-electronic conversion, where the optical signal is detected using a photodetector, whereupon the resulting electrical

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[21] Insertion penalty/power penalty: defined as the reduction in receiver sensitivity induced by insertion of a device under test (DUT) compared to the back-to-back case. The receiver sensitivity is in this thesis measured at a BER of 10^{-9}.

[22] Conversion efficiency: ratio of average output power to input power

[23] IPDR: defined as the input power range in which the power penalty is below a specific value. For a receiver without(with) preamplifier a 1 dB(2 dB) penalty is normally used.

[24] It should be noted that opto-electronic conversion in commercial networks in normally done in conjunction with electrical regeneration in order to ensure an acceptable performance.

signal is used for external or direct modulation of a laser at a different wavelength. Using this technique, conversion at 2.5 Gbit/s with a high extinction ratio[25] of 43 dB has been demonstrated [59]. Furthermore, using a complex photodiode design, 10 Gbit/s conversion has been performed with an insertion penalty of ~1.5 dB [60]. However, as demonstrated in [61], opto-electronic wavelength conversion is far inferior to all-optical wavelength conversion with respect to cascadability; eight times as many all-optical wavelength converters can be cascaded at 2.5 Gbit/s as opto-electronic converters due to a smaller pattern-dependent jitter accumulation as a consequence of an inherently flatter transfer function. Furthermore, due to price and power-consumption issues all-optical wavelength conversion is preferable at higher bit rates.

Among the techniques for all-optical wavelength conversion, both four-wave mixing (FWM) and difference-frequency generation (DFG) yield format transparent conversion. Furthermore, these techniques have the potential of operation at very high bit rates as they exploit ultrafast nonlinear effects in fibres or SOAs. As the phase conjugate is generated through FWM and DFG, both techniques can be used for mid-span spectral inversion, which is attractive for dispersion compensation [62]. Unfortunately, there are some disadvantages associated with FWM and DFG. With respect to the FWM process, then polarisation sensitivity is inherent, why very complex arrangements are needed to circumvent the problem [63]. Furthermore, the conversion efficiency is relatively poor for both FWM and DFG; typical obtainable efficiencies are in the order of –10 dB for FWM [64] and –17 dB for DFG [65]. As the signal-to-noise ratio (SNR) is inversely proportional to the conversion efficiency, a limited cascadability must be expected; the record number of cascaded FWM-based converters is two (@10 Gbit/s), where the SNR was reduced from 40 to 20 dB through the process [66]. This clearly limits the practical use of these schemes in an optical network, where it is expected that multiple wavelength converters must be traversed from source to destination (cf., e.g., Chapter 2).

A very simple scheme for all-optical wavelength conversion involves the exploitation of gain saturation effects in active devices, e.g., SOAs. The principle of the technique, which is called cross-gain modulation (XGM), is sketched in Fig. 4.1. As shown in Fig. 4.1a, bias current is applied to an SOA, thereby inverting the carrier population. An input data signal at the wavelength λ_{in} is coupled into the SOA along with CW-light at the wavelength λ_{conv} (here, in co-propagation). As the data signal propagates through the SOA, it will modulate the carrier density, and therefore the gain. As shown in Fig. 4.1b, the high optical power in the marks of the data signal causes a larger depletion of carriers, and therefore gain saturation, than a space. The CW-light at λ_{conv} experiences this change in the gain so that CW-light traversing the SOA with a mark will experience a lower gain than light traversing with a space. Thus, a copy of

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[25] Extinction ratio: the ratio between the power in a mark and a space

the original data signal with inverted polarity is obtained at λ_{conv} at the SOA output. Note that a filter is placed at the SOA output to select the signal at λ_{conv}. This can be omitted if the two signals counter-propagate through the SOA. However, as will be discussed in Section 4.5, there are some drawbacks to using this scheme.
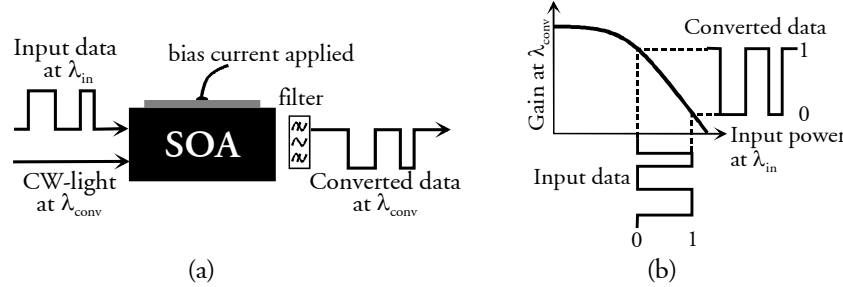
Fig. 4.1: (a) Wavelength conversion by cross-gain modulation in an SOA. **(b)** Schematic of the XGM conversion mechanism, where gain saturation in, e.g. an SOA, is exploited to generate a converted signal with inverted polarity. A dB-scale is shown.

Some significant advantages are associated with XGM-based wavelength conversion, the most significant one being the simplicity of the scheme. This will become more apparent in the following, where conversion based on cross-phase modulation (XPM) will be described. Furthermore, very impressive high-speed results have been obtained for conversion using XGM; with the aid of subsequent high-pass filtering using a detuned grating, 100 Gbit/s wavelength conversion has been demonstrated [67]. Furthermore, XGM conversion is polarisation-independent if the SOA gain is polarisation independent. This can be achieved by using bulk devices with a square cross-section or by introducing strain in bulk or quantum-well devices. Unfortunately, there are also disadvantages to XGM-based wavelength conversion. The most critical one in a network perspective is the chirped output signal caused by XGM; the carrier dynamics lead to a frequency shift at the leading and trailing edges of the converted pulses. Due to the polarity inversion, this results in a severe penalty when the converted signal is transmitted over standard dispersive fibre, thus limiting the transmission distance significantly [68]. Another drawback is that the differential gain[26] is smaller for longer wavelengths [69]. Thus, the output extinction ratio for up-conversion (i.e., conversion to longer wavelengths) is smaller than for down-conversion, which compromises the performance. Finally, it should be mentioned that polarity inversion, which is inherent of XGM conversion, may be undesirable in future optical networks, especially if the RZ-format is used. This is because polarity inversion is associated with pulse inversion, which may complicate subsequent optical signal processing, like, e.g., optical logic, that requires the input RZ signals to have identical pulse shapes. This will be discussed in more detail in Section 6.1.3.

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[26] Differential gain: gain change caused by a change in carrier density ($\partial g / \partial N$).

One of the most promising techniques for all-optical wavelength conversion, which does not have the disadvantages mentioned above, is based on cross-phase modulation (XPM). The nonlinear element used to generate the phase change can be both fibre- as well as SOA-based. Very good high-speed results (up to 80 Gbit/s conversion) have been obtained with fibre-based schemes, e.g., the nonlinear loop-mirror (NOLM) [70], however, for practical purposes SOA-based XPM conversion is preferable due to power-efficiency, stability issues and compactness. Thus, the remainder of this section will be dedicated to SOA-based interferometric wavelength converters.

In Fig. 4.2a (upper) is shown schematically the structure of the SOA-based Mach-Zehnder interferometer and the principle of standard wavelength conversion using this device. The Mach-Zehnder interferometer consists of a standard interferometric structure with SOAs placed in the two interferometer arms. Wavelength conversion is achieved in the following way: a data signal at λ_{in} is coupled into port #1 of the MZI. As the signal propagates through the upper SOA, it modulates the carrier density, causing a change in the refractive index, and thereby a phase modulation. CW-light at the wavelength λ_{conv} is coupled into port #3 and is subsequently split equally to the two interferometer arms. In the lower arm the CW-light will experience a constant phase change, ϕ_2, determined by the biasing of the lower SOA. However, in the upper arm the CW-light will experience a phase change ϕ_1 depending on the bit pattern of the input data signal. Thus, the CW-light will combine constructively or destructively at the interferometer output depending on the modulation of the input data signal. In this way, the bit pattern is transferred to the CW-light, which is selected at the output using a filter. In Fig. 4.2a (lower) is shown the Michelson interferometer, which is simply a folded version of the MZI; the left input facet is reflective (~33%), and made by cleaving the SOA material along its crystal plane. The data signal is coupled directly into the upper interferometer arm of the MI counter-directionally to the CW-light. When the CW-light reaches the left input facet, it is reflected, and thus propagates twice through the interferometer arms before being recombined at port #3.

Although the MZI and MI basically function the same way, there are some differences in characteristics due to their different structures. Firstly, as the CW-light enters and leaves the same port of the MI, a circulator must be used to separate the two components. Furthermore, since the input data signal also leaves port #3, a filter is always required, and conversion to the same wavelength is not possible. The importance of the latter will be discussed in more detail in Section 4.5. Secondly, the data signal is injected directly into the interferometer arm of the MI. This, combined with the fact that the CW-light propagates twice through the SOAs, means that, in principle, the MI exhibits the largest modulation bandwidth and therefore best high-speed performance, enabled by a large photon intensity and a long interaction length [69,71]. However, transient effects associated with the counter-propagation in the MI will limit the actual modulation bandwidth while compromising the high-speed

performance due to timing jitter as the time slot duration approaches the physical length of the Michelson interferometer [72]. Thus, although the first 40 Gbit/s conversion experiments were demonstrated with an MI [10], the MZI is expected to be superior when conversion at higher bit rates is demonstrated in the future.

A schematic of the transfer function of the IWC in dB-scale is shown in Fig. 4.2b, where the output power at λ_{conv} is illustrated as a function of the power of the input data signal at λ_{in}. The transfer function is linked to the following expression for the converted output power, $P_{cw,out}$, as a function of the CW input power, $P_{cw,in}$:

$$P_{cw,out} = \tfrac{1}{8} P_{cw,in} (G_1 + G_2 + 2\sqrt{G_1 G_2} \cos(\Delta\phi)) \qquad (4.1)$$

where (G_1,ϕ_1) and (G_2,ϕ_2) refer to the gains and phase changes in the upper and lower interferometer arms, respectively, and $\Delta\phi = |\phi_1 - \phi_2|$. As indicated, the transfer function is periodic, depending on cosine to the phase difference, $\cos(\Delta\phi)$, between the two arms; a phase shift of π will change the output power from maximum to minimum and vice versa. This also means, as shown in Fig. 4.2b, that the converted output signal can either be inverted or non-inverted compared to the input data signal, simply by operating on the negative or positive slope, respectively. Operation on the negative slope is often denoted out-of-phase operation, while operation on the positive slope is called in-phase operation.
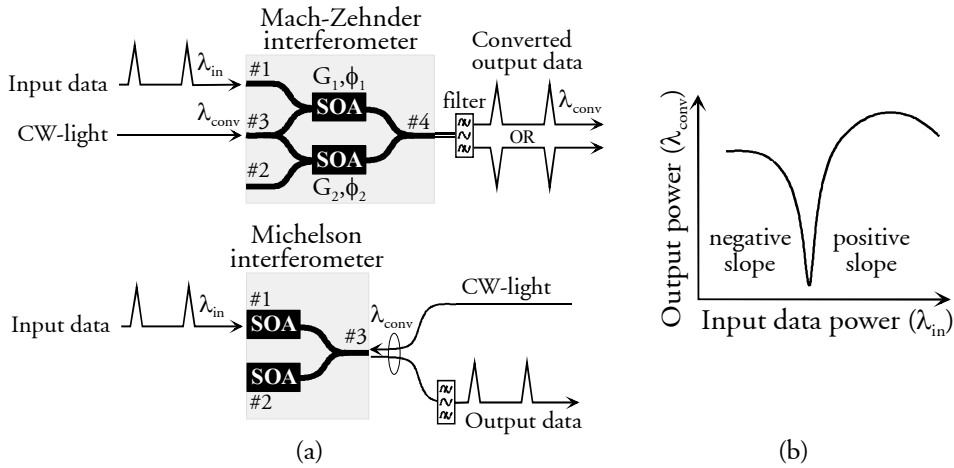
Fig. 4.2 (a) Schematic of the SOA-based Mach-Zehnder interferometer (upper) and Michelson interferometer (lower). (b) The corresponding transfer function of the two IWCs, illustrating the converted output power versus the data signal input power in dB-scale. (G_1,ϕ_1) and (G_2,ϕ_2) refer to the gains and phase changes in the upper and lower interferometer arms, respectively.

At this time, the record wavelength conversion rate of 168 Gbit/s has been achieved by Ueno et al. through employment of a delayed-interference signal converter (DISC) [11]. In Fig. 4.3 is shown the principle of wavelength conversion with a DISC: the

SOA at the input of the DISC enables cross-phase modulation of the CW-light by the data signal. Subsequently, the CW-light is injected into a passive Mach-Zehnder interferometer with arms that differ in length; the longer arm of the interferometer provides a delay of $\Delta\tau$ between the two parts of the CW-signal. At the output of the interferometer, constructive or destructive interference will occur depending on the phase difference between the two arms. The shorter arm contains a phase shifter, which allows the phase to be adjusted so that in-phase or out-of-phase operation can be obtained (see Fig. 4.2). As an optional addition, the output combiner in the interferometer can be made as a tuneable coupler, which enables fine-tuning of the operation point to improve the extinction ratio. This scheme is employed in [12], where wavelength conversion at up to 100 Gbit/s is demonstrated with good performance in an integrated DISC. A switching (conversion) window is generated by the delay- and phase shifter-combination, which enables wavelength conversion. Note that a useable switching window will only be generated if the input data signal has an RZ-format. Thus, only conversion of RZ-signals is possible with the DISC.
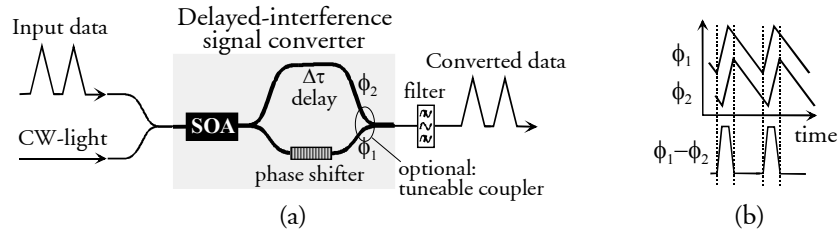
Fig. 4.3: (a) Schematic of wavelength conversion in a delayed-interference signal converter (DISC). (b) Illustration detailing principle.

Another type of IWC, which is widely used for research purposes, is the terahertz optical asymmetric demultiplexer (TOAD)[27]. The principle of the TOAD, which was first proposed by Sokoloff et al. as a time-division demultiplexer [73], is shown schematically in Fig. 4.4. As indicated, the device consists of an SOA placed asymmetrically within a fibre loop-mirror, which is usually biased in the reflecting mode[28]. When CW-light or a data pulse is injected into the TOAD at port #3, it is split into clockwise and counter clockwise travelling components by a 3-dB coupler. A switching pulse injected into port #1 (i.e., the data signal must be RZ-format) is timed such that it arrives after the clockwise travelling data pulse has passed through the SOA but before the counter clockwise travelling data pulse arrives. The switching pulse causes a phase shift of ~π, which is experienced by the counter clockwise data pulse. Thus, a switching window is created in analogy to the one shown Fig. 4.3b for the DISC. It should be mentioned that the reason both a clock signal and CW-light is

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[27] The TOAD is also often denoted the SOA-assisted Sagnac loop or SLALOM.
[28] Reflecting mode: when the data signal is a space, the signal injected into port #3 will also be coupled out of port #3.

shown at the input to port #3 is that, although conversion to CW-light is possible with the TOAD, it is rarely demonstrated. This may be due to the fact that the co- and counter-propagative mode in conjunction with the single-SOA configuration limits the performance achievable without the aid of clock pulses, which effectively shape the output pulses, as will be discussed in Section 5.1.1 and 5.1.2.2. This is due to the fact that the counter-propagating pulses experience a different gain and phase response than the co-propagating pulses [74], why the extinction ratio is compromised. This can be partially compensated for either through application of a tuneable coupler (as in the DISC) or by inserting a birefringent polarisation controller in the loop, that allows the optical path length to be adjusted individually for the co- and counter-propagating pulses (as in the UNI, cf., Fig. 4.5) [74].
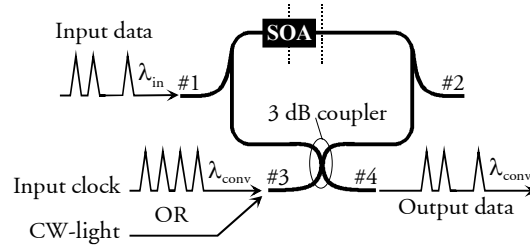

Fig. 4.4: Schematic of the terahertz optical asymmetric demultiplexer (TOAD).

Another type of IWC, which is widely used for high-speed signal processing, is the ultrafast non-linear interferometer (UNI), which was first proposed by Patel et al. in 1996 [75]. The principle of the UNI is shown schematically in Fig. 4.5: clock pulses are coupled into port #2 of the UNI. Here, the pulses are injected into a birefringent fibre at a 45° angle and are thereby split into two orthogonally polarised pulses with a spacing determined by the differential group delay of the fibre. These two clock components traverse the SOA, are temporally recombined in a second birefringent fibre, and interfere in a polarizer. The UNI can be biased on or off by adjustment of the polarisation controller in front of the output polarizer. The data pulses (i.e., RZ-format must be used), which function as control pulses, are coupled into port #1 and subsequently injected into the SOA, where they temporally overlap (i.e., are synchronised to) one of the two clock components. The control pulses induce ultrafast (intraband) as well as long-lived (interband) changes in the refractive index and the gain of the SOA. In the UNI, long-lived refractive index changes are sensed equally by both clock components, so the switching operation is relatively insensitive to these changes. However, ultrafast refractive index nonlinearities induced in one of the two clock components by the overlapping data pulse change the polarisation of the recombined signal components and switch the transmission at the output polarizer. Finally, an optical filter at the UNI output selects the switched-out clock pulses, now containing the original input data. It should be noted that the principle of ultrafast refractive index changes for wavelength conversion can equally well be employed in,

e.g., a MZI or MI. It should also be noted that the UNI requires conversion to clock pulses meaning that in a practical system, clock recovery must be performed, thus increasing the complexity of the wavelength conversion scheme (see Section 5.1.1). In [76] BER measurements have been performed for 80 Gbit/s wavelength conversion using the scheme shown in Fig. 4.5, and in [21] wavelength conversion at 100 Gbit/s has been demonstrated, although without BER measurements.
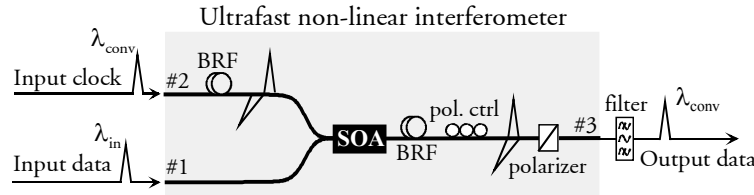

Fig. 4.5: Schematic of wavelength conversion using the ultrafast nonlinear interfero-meter (UNI). BRF: birefringent fibre.

This section has given an overview of the different techniques for interferometric wavelength conversion using SOA-based devices. Some of these techniques have also been used to demonstrate all-optical Boolean logic, as will be discussed in more detail in Chapter 6.

With respect to experimental results, in the remainder of the thesis the focus will be on the Mach-Zehnder and Michelson interferometers, as shown in Fig. 4.2a. These devices can be realised as an active-passive structure, where only the interferometer arms are active, and using an all-active structure, where the entire interferometer, including input arms and couplers as well as the output coupler, are active. The active-passive devices have the advantage that they are easier to control and have lower power consumption, as current is only applied to the two interferometer arms. However, the all-active devices are easier and potentially cheaper to fabricate, as fewer epitaxial- and processing steps are required [77]. Furthermore, the absence of active-passive transitions avoids parasitic reflections that are especially critical for high bias currents [77]. An additional benefit of the all-active structure is that the active input sections can be used as pre-amplifiers [78], thus reducing the required input power levels. Alternatively, through active control of the bias currents, fast power equalisation is possible, as described in Section 4.4.3 and [79,Pub4]. Moreover, the output section can be used as a power booster, why conversion efficiencies as high as 10 dB can be obtained with all-active devices, while –10 dB is typical for active-passive structures. However, due to the active input and output sections, there are also some drawbacks to the all-active structure. The input sections cause potential extinction ratio degradation and generate amplified spontaneous emission (ASE), thus degrading the OSNR. Hence, the input and output arms should be dimensioned as short as possible. In [80], Alcatel Opto+ has made a performance comparison at 20 Gbit/s of an all-active and active-passive MZI. Here, the superior OSNR of the active-passive device (~6 dB

larger) has been verified. However, with respect to the conversion capabilities, the two device structures function equally well. Finally, it has been noted that the reproducibility of the active-passive devices is better, thus easing the insertion in practical systems.

All the results that are shown in the remainder of the thesis will be based on all-active bulk tensile-strained devices fabricated by Alcatel Opto+.

4.3 Standard wavelength conversion by cross-phase modulation

For application in practical networks, all-optical wavelength conversion should be relatively simple, exhibit a good performance and be flexible with respect to, e.g., modulation format. Apart from standard conversion using an MI or MZI as described in Fig. 4.2a, all the other interferometric wavelength conversion techniques discussed in Section 4.2 require an RZ-format, thus restricting the format specifications in the network (commercial networks today employ the NRZ-format). For this reason, and because of the simplicity of the scheme compared to, e.g., the differential control scheme, which will be discussed in Section 4.4, standard wavelength conversion is considered an attractive technique.

4.3.1 Wavelength dependency of the MI at 10 Gbit/s

As noted in Section 4.1, a very important requirement of wavelength converters is wavelength independence. Because SOA-based interferometric wavelength conversion is governed by a carrier density-dependent refractive index change, which is nearly wavelength independent (especially at high carrier densities) [81], interferometric wavelength conversion is wavelength independent over a wide range (usually within ±15-20 nm of the IWC gain peak) in sharp contrast to XGM-based conversion (c.f., Section 4.2).

This wavelength independence is verified experimentally at 10 Gbit/s in Fig. 4.6 for an MI with 1200 µm long interferometer arms. Fig. 4.6a shows the pre-amplified power penalty when the input data signal wavelength is varied over 30 nm and the CW wavelength is kept fixed at 1540 nm, while Fig. 4.6b shows the case where the (data) signal wavelength is kept fixed at 1540 nm and the CW wavelength is varied. As seen, an excellent performance is obtained in both cases, with a penalty below 1 dB. The higher penalty at longer wavelengths can be ascribed to the position of the gain peak, which is at ~1525 nm. Thus, it can be expected that the total optical bandwidth of the MI by far exceeds 30 nm; measurements below 1530 nm were not performed due to limitations of tuneable optical filters and EDFAs in the experimental set-up. The negative penalty at short wavelengths is caused by signal reshaping in the MI compared to the back-to-back case. This illustrates the powerful regenerative capabilities of the IWC, which is a consequence of the sinusoidal transfer function shown in Fig. 4.2b. All-optical regeneration using IWCs is the topic of Section 5.1.
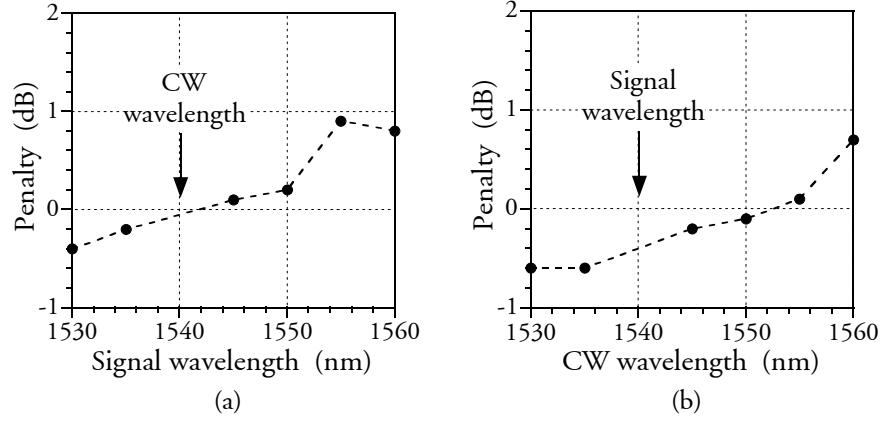
Fig. 4.6: Preamplified penalty for 10 Gbit/s standard wavelength conversion using a MI. (a) With the signal wavelength varied and CW wavelength at 1540 nm. (b) With the CW wavelength varied and signal wavelength at 1540 nm.

The good performance of the MI at 10 Gbit/s is also verified in Fig. 4.7, which shows the eye-diagram for conversion from 1545 to 1550 nm (a) and the spectrum in 0.1 nm bandwidth at the MI output (b) The eye-diagram is clear and open with a good extinction ratio of ~11.4 dB, verifying the good performance. The optical spectrum shows that the optical output power and OSNR are high, ~2 dBm and ~40 dB, respectively; both factors are important for the cascadability of the MI.
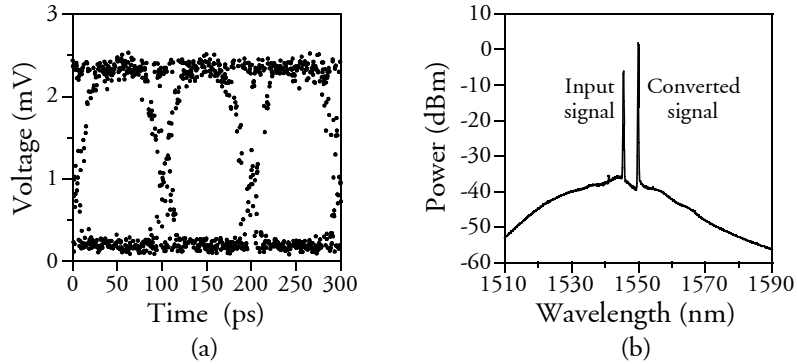
Fig. 4.7: Results of 1545 to 1550 nm conversion using MI (a) Converted eye-diagram (b) Optical output spectrum in 0.1 nm.

4.3.2 20 Gbit/s wavelength conversion using an MZI

As yet, the highest bit rate at which standard conversion has been performed with good results in an MZI is 20 Gbit/s. However, using the Michelson interferometer, 40 Gbit/s standard conversion was shown in 1997 [10], while 20 Gbit/s standard conversion in a Mach-Zehnder interferometer was not demonstrated until 1999 [Pub2]. This clearly reflects the discussion in Section 4.2, where it was argued that MIs have a better performance than MZIs at moderate bit rates.

Eye-diagrams are shown in Fig. 4.8 for standard conversion at 20 Gbit/s using an MZI with 2000 µm long interferometer arms. Here, a comparison is made between operation on the negative- and positive flank of the transfer function in Fig. 4.2b, resulting in an inverted- or non-inverted polarity at the output, respectively. As indicated, the eye-diagrams obtained are in both cases clear and open with a high extinction ratio greater than 10 dB. Furthermore, the RZ-format is preserved very well through the conversion process, indicating the high-speed response of the MZI. However, the quality of the in-phase eye-diagram in Fig. 4.8b is a little better than for the out-of-phase eye-diagram in Fig. 4.8a; the base level is less noisy, the pulses are narrower and the slope of the flanks is more equal, indicating a higher speed response. These results, which were typical for this specific device, contradict the basic theory, which states that out-of-phase conversion has the highest modulation bandwidth since cross-gain modulation aids the conversion process. This is in contrast to in-phase conversion, where cross-gain- and cross-phase modulation counteract each other.

              (a)   (b)
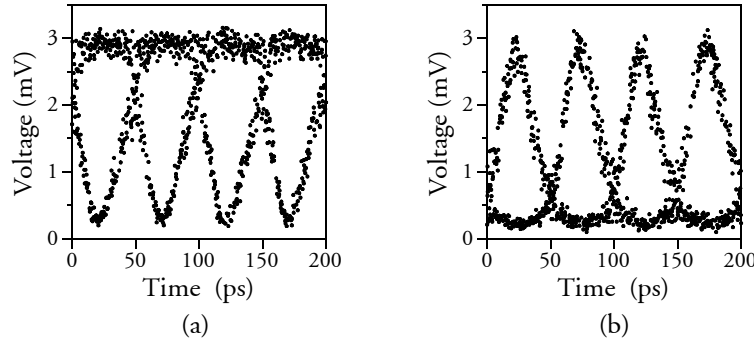
Fig. 4.8: Eye-diagrams for 20 Gbit/s standard wavelength conversion using MZI with 2000 µm long interferometer arms [Pub29]. (a) Out-of-phase operation, resulting in inverted polarity, (b) In-phase operation, resulting in same polarity as input signal.

Using a different Mach-Zehnder interferometer with 1200 µm long interferometer arms [77], BER measurements have been performed at 20 Gbit/s [Pub2]; in Fig. 4.9 is shown the experimental set-up used. In the transmitter, short pulses having a FWHM[29] width of ~7 ps are generated at 1554 nm by a gain-switched DFB[30] laser, followed by pulse compression in a dispersion compensating fibre (DCF). The short pulses are subsequently modulated at 10 Gbit/s in a LiNbO$_3$ Mach-Zehnder modulator and passively multiplexed to 20 Gbit/s using fibre delay-lines. The data signal and CW signal at 1549 nm are then coupled into the converter co-directionally, and the filter at the output selects the converted signal. The 20 Gbit/s converted signal is optically demultiplexed to 10 Gbit/s by an electro-absorption (EA) modulator before detection and error counting in a preamplified receiver.

[29] FWHM: Full Width Half Maximum
[30] DFB: Distributed Feed-Back
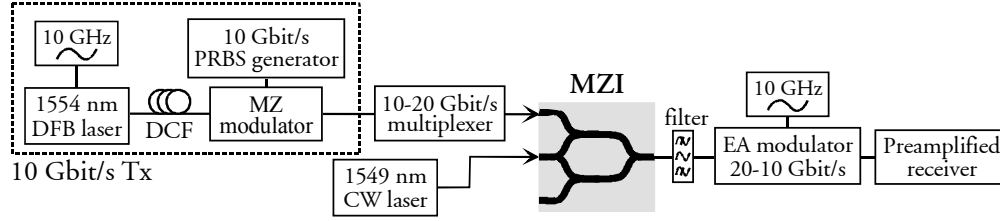
Fig. 4.9: Experimental set-up for 20 Gbit/s standard wavelength conversion in an all-active MZI with 1200 μm long interferometer arms. Additional information about the MZI is given in [77].

In Fig. 4.10a and b the measured input eye-diagram at 1554 nm and converted eye-diagram at 1549 nm are shown, respectively. As seen in the figure, a clear and open inverted eye diagram is obtained for the converted signal. Note also that the RZ input signal format is preserved through the wavelength conversion, although not to as great an extent as for the 2000 μm long MZI[31] (see Fig. 4.78). The difference in conversion speed can partly be attributed to the difference in length; as discussed in Section 4.2, a long interaction length enables a higher modulation bandwidth. It should be noted that interferometer arms much longer than 2000 μm are not advantageous due to an increased noise figure. To support this, it can be mentioned that an output OSNR in the order of ~34 dB (in 0.1 nm) was measured in conjunction with the results shown in Fig. 4.8 for the 2000 μm long MZI. In contrast, the 1200 μm long MZI exhibits an OSNR of ~40 dB (in 0.1 nm). Fig. 4.10c shows the measured bit error rate versus received power for the back-to-back case as well as the converted signal for the 1200 μm long MZI. As seen, some degree of pulse broadening and extinction ratio degradation results in a small conversion penalty (@BER=10^{-9}) of 0.9 dB.
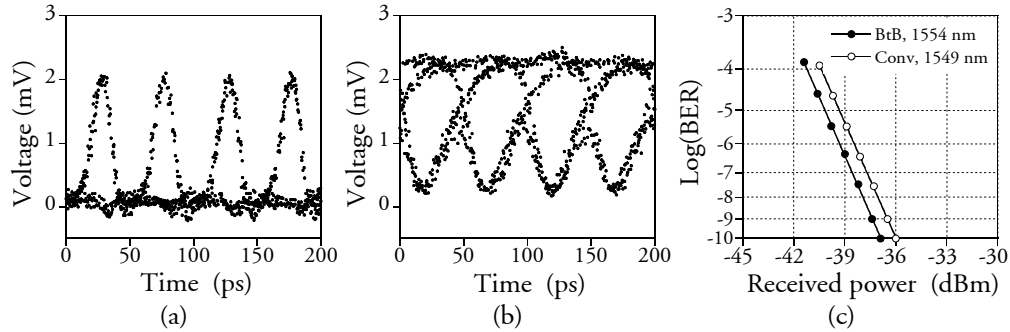
Fig. 4.10: Eye-diagrams at 20 Gbit/s for the back-to-back signal at 1554 nm (a) and the converted signal at 1549 nm (b). (c) The corresponding BER curves after demultiplexing to 10 Gbit/s. BtB: back-to-back.

[31] The length of an MZI or MI will from now on refer to the length of the interferometer arms.

4.4 High-speed interferometric wavelength conversion using the differential control scheme

As mentioned in Section 4.3.2, 20 Gbit/s is the highest bit rate at which standard wavelength conversion has been demonstrated in an MZI, although wavelength conversion at higher bit rates should be possible. As yet, wavelength conversion at higher bit rates requires a more complex scheme, which compensates for the slow carrier recovery of the SOA, thus increasing the conversion speed in spite of a limited SOA modulation bandwidth. In this section, the differential control scheme, as it is called, will be described and experimental results obtained using the scheme will be given.

4.4.1 The principle of the differential control scheme

The differential control scheme was first introduced by Nakamura et al. [82]. The principle, which is only applicable for the RZ modulation format, is illustrated in Fig. 4.11a: in contrast to the standard scheme shown in Fig. 4.2a, the data signal is split up and introduced into both of the interferometer arms. The signal in the lower arm is attenuated and delayed by $\Delta\tau$ with respect to the signal in the upper arm. In the common arm, CW-light is introduced as in the standard scheme.

The reason why the differential scheme is faster than the standard scheme can be understood from Fig. 4.11b, which shows the phase modulation occurring in the upper and lower interferometer arms, and the corresponding phase difference. As indicated, the attenuation of the lower input signal will result in a smaller phase modulation in the lower SOA than in the upper SOA. If the delay, $\Delta\tau$, is chosen appropriately, the resulting phase modulation will be of a short time span despite the relatively slow carrier recovery of the generated phase changes in the individual SOAs. Thus, a conversion (switching) window having a short, well-defined time span is created. It should be noted that the scheme works equally well with the MI as the MZI. Finally, it is important to mention that in spite of the efficiency of the differential control scheme, the conversion speed cannot be made infinitely high simply by reducing the size of the switching window; patterning effects in the SOAs will ultimately be the limiting factor.
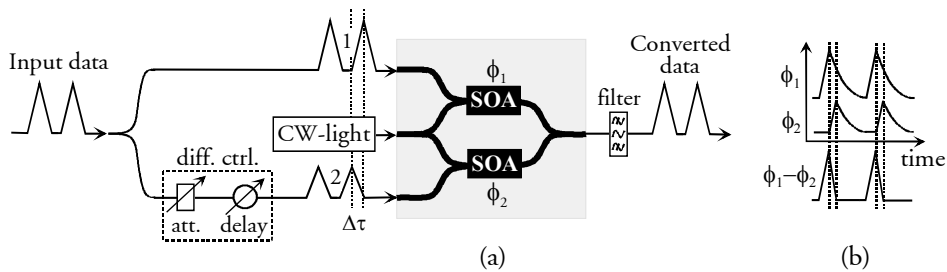
Fig. 4.11: (a) Schematic of the differential control scheme for high-speed wavelength conversion of RZ-signals, here using an MZI. (b) Illustration detailing the effect of the differential scheme, which enables the generation of a narrow switching window.

The principle of the differential scheme is very much like the wavelength conversion schemes using a DISC, TOAD and UNI (see Section 4.2). In all cases, delay of two phase components results in the generation of a narrow switching window, which compensates for the slow carrier recovery of the SOA. However, there is one important difference between the differential scheme in Fig. 4.11 and the others: for the differential control scheme, the phase modulation depth of the two phase components is not identical, as they are each generated in two different SOAs (see Fig. 4.11b), while it is identical for the other conversion techniques because a single SOA generates the phase modulation (see Fig. 4.3b). This means that unlike the MZI and MI, the DISC, TOAD and UNI are inherently balanced in their mode of operation. According to [83][32], the lack of this extra parameter of freedom in the latter cases means that the achieved output extinction ratio depends on the linearity of the carrier recovery. Moreover, in [84] it has been demonstrated that, compared to the TOAD, the MZI exhibits the best performance in terms of the minimum switching window width and extinction ratio. This is also the reason why wavelength conversion using a TOAD, as discussed in Section 4.2, is normally done using a clock signal instead of CW-signal, in order to exploit selective switching of clock pulses that relaxes the operation requirements [83].

The influence of the differential control scheme in Fig. 4.11a is demonstrated experimentally in Fig. 4.12, which shows 10 Gbit/s wavelength converted eye-diagrams. The figure compares an eye-diagram obtained using standard conversion (Fig. 4.12a) with eye-diagrams obtained using partial differential control (Fig. 4.12b) and fully optimised differential control (Fig. 4.12c). Partial differential control is achieved by using a non-optimised value of $\Delta\tau$. It is clearly seen that the tail of the converted signal caused by the relatively slow carrier recovery is suppressed as $\Delta\tau$ is optimised. However, it is also seen that the extinction ratio is degraded as the
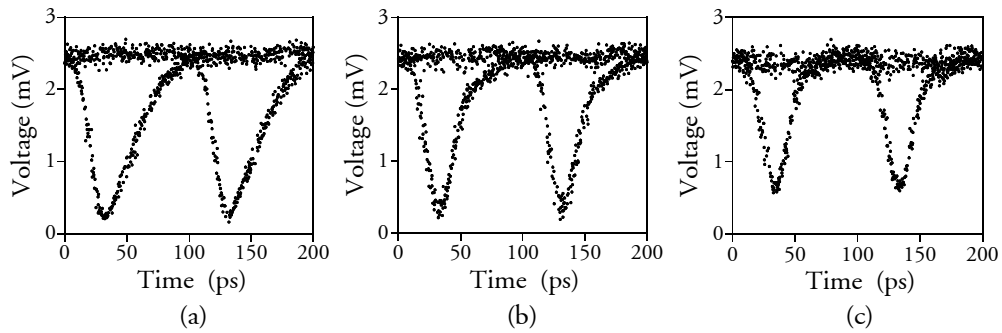
Fig. 4.12: Eye-diagrams of a 10 Gbit/s wavelength converted signal without differential control (a), with partial differential control (b) and with fully optimised differential control (c). An MZI was used.

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[32] With reference to the TOAD, specifically.

differential scheme takes effect because the delay between the signal pulses becomes so small that the phase difference does not reach π before the second pulse closes the switching window. Thus, the switching window size is ultimately limited by the input signal pulse width.

4.4.2 40 Gbit/s differential wavelength conversion in an MZI

The differential control scheme is assessed at 40 Gbit/s using the experimental set-up shown in Fig. 4.13 [Pub4, Pub7]. A 10 Gbit/s RZ data signal is generated using a transmitter like the one in Fig. 4.9, whereupon passive multiplexing to 40 Gbit/s is performed. In accordance with Fig. 4.11a, the resulting signal is split equally and one part is delayed and attenuated with respect to the other before being coupled into the upper and lower interferometer arm of the MZI. The CW signal at 1549 nm is coupled co-directionally into the MZI, and the converted signal is selected at the output using a filter. An EA-modulator performs electro-optic demultiplexing from 40 to 10 Gbit/s before error counting in a preamplified receiver. It should be noted that the same 1200 μm long MZI is used for these experiments as the one that was used for 20 Gbit/s standard conversion in Section 4.3.2.
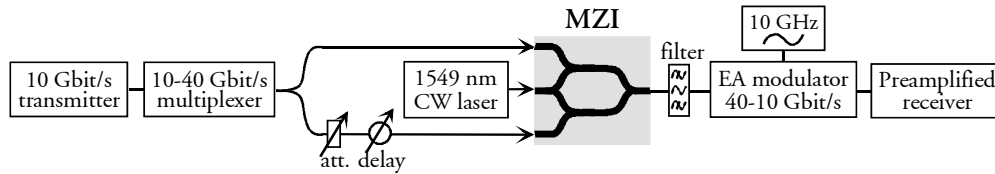
Fig. 4.13: Experimental assessment of the differential control scheme for wavelength conversion at 40 Gbit/s. The 10 Gbit/s transmitter is identical to the one in Fig. 4.9.

Eye-diagrams of the input signal and the converted signal at 40 Gbit/s as well as BER curves obtained after demultiplexing to 10 Gbit/s are shown in Fig. 4.14a, b, and c, respectively. As indicated, the converted eye-diagram is clear and open with a good extinction ratio of ~10 dB. However, comparing the back-to-back and converted eye-diagrams, it can be seen that a format conversion from RZ to NRZ has occurred due to the relatively wide switching window (see Fig. 4.12c) that was used, in conjunction with an insufficiently high modulation bandwidth. Despite the format translation, the BER curves in Fig. 4.14c show a preamplified penalty of 0.7 dB. This low penalty may partly be attributed to the shaping performed by the EA-modulator used for demultiplexing to 10 Gbit/s.
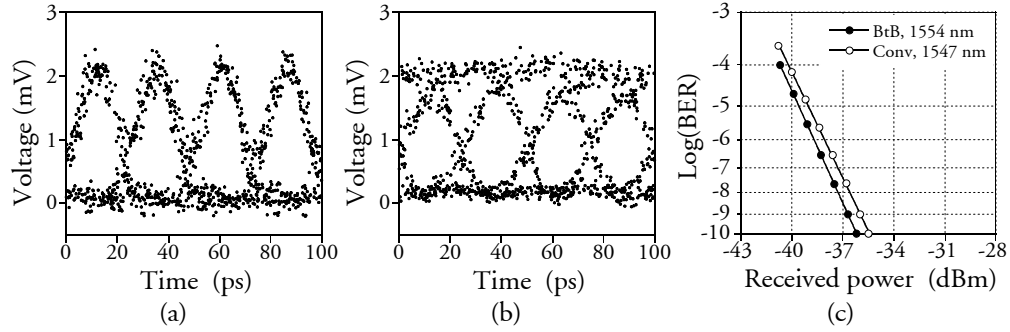
Fig. 4.14: 40 Gbit/s differential conversion using 1200 μm long MZI: measured eye-diagrams at 40 Gbit/s of the back-to-back signal at 1554 nm (a) and the converted signal at 1547 nm (b). (c) The corresponding BER curves after demultiplexing from 40 to 10 Gbit/s.

It was demonstrated in Section 4.3.2, that the length of the interferometer arms is an important factor for the modulation bandwidth of IWCs. This is also evident in Fig. 4.15, which shows eye-diagrams for 40 Gbit/s standard (a) and differential conversion (b) in the 2000 μm long MZI also used to achieve the results in Fig. 4.8. Focusing on Fig. 4.15a, it can be seen that although the eye-diagram for standard conversion is quite noisy, the response of the MZI is very fast; a full conversion to NRZ format has not occurred. It should be noted that to the author's knowledge this is the first demonstration of an open eye-diagram at 40 Gbit/s using standard conversion in an MZI. By employing the differential control scheme with $\Delta\tau \sim 5$ ps, a very good performance is obtained; the RZ-format is preserved through the conversion process and a high extinction ratio of $\sim$10.8 dB is obtained.
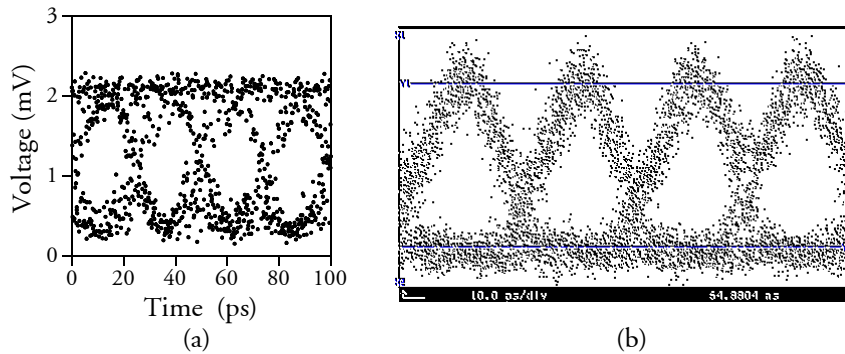
Fig. 4.15: 40 Gbit/s wavelength conversion using 2000 μm long MZI. (a) Standard conversion. (b) Conversion using the differential control scheme.

Comparing Fig. 4.15b with Fig. 4.14b, the difference in performance of the two MZIs is evident. This is partly due to the difference in length, however, another factor in relation to the chip design may also be responsible for the good performance of the 2000 μm long MZI: when the differential control scheme is used

with an all-active device, the beat signal generated by the two data signal components as they combine at the interferometer output may cross-gain modulate the converted signal, thereby adding random power fluctuations that will degrade the signal quality. As a means to circumvent this problem, the 2000 μm long MZI, which is part of a new generation of devices, has been fabricated with a passive output section. Thus, the good 40 Gbit/s performance of this device may partly be attributed to the new design. It should be stressed that the effect described here is not relevant for the standard conversion scheme.

4.4.3   Scheme for increased input-power dynamic range

As demonstrated so far, the IWC exhibits some very attractive features such as wavelength independent operation, high-speed response, as well as enabling a high output OSNR and extinction ratio. However, one factor, which must be taken into account in a network perspective, is the IWC's sensitivity towards fluctuations in the optical input power levels: a minor change in the input power will shift the operation point, which, due to the sinusoidal transfer function, will cause a relatively large change in the characteristics of the converted signal, and thereby an increased power penalty. This translates into a very limited input power dynamic range of 2-4 dB if active control is not applied [Pub4,85,86]. This limited IPDR is problematic in a network perspective, e.g., because signals entering packet switch nodes from different sources will inherently have different power levels and ageing of, e.g., EDFAs will cause power alterations with time.

In this section, a method for increasing the IPDR of IWCs through power equalisation is discussed. It relies very simply on individual adjustment of the bias currents to the active input sections according to the optical input power. The scheme yields a compact and cost-effective solution, as it employs SOAs already monolithically integrated in the all-active IWC structure. Furthermore, as the carrier effects in SOAs are inherently fast (~sub ns range), the control scheme is only limited in speed by the control electronics.

Fig. 4.16 shows the experimental set-up used for static assessment of the control scheme described above when differential conversion is used. The IPDR of the MZI is evaluated by adjusting the input power to the device with an attenuator. Note that the attenuator is placed before splitting as part of the differential control scheme, meaning that a change in input power will affect both interferometer arms equally. This input power change is compensated for through individual adjustment of the bias currents to the upper and lower input sections of the MZI, as illustrated. For each input power level, the minimum penalty obtainable through optimisation of the bias currents is registered.
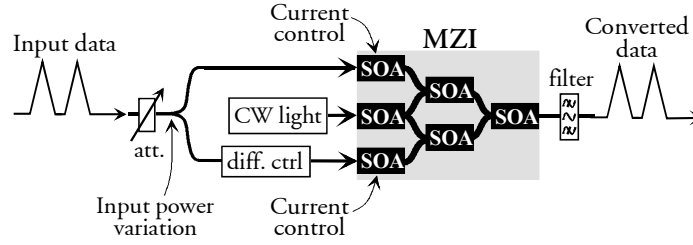
Fig. 4.16: Schematic of set-up used to increase the input power dynamic range of an all-active MZI operated in the differential mode. As indicated, the operation point is adjusted by controlling the bias current to the input sections. The differential control block consists of an optical attenuator and delay, as shown in Fig. 4.11a.

The IPDR is measured at 40 Gbit/s with and without current control to the two input sections using the set-up in Fig. 4.13. The experimental results, which are based on [Pub4], are given in Fig. 4.17, which shows the measured excess penalty as a function of the input power variation relative to the optimal operation point. The increase in input power dynamic range caused by the current control is evident: the IPDR without control is ~4.5 dB, measured for a preamplified penalty of 2 dB, while with control the IPDR is increased to~6 dB. At high input powers the IPDR is increased through a reduction of the bias currents from 105 mA to 85 mA. However, contrary to what is expected, no improvement is observed for lower input power levels.
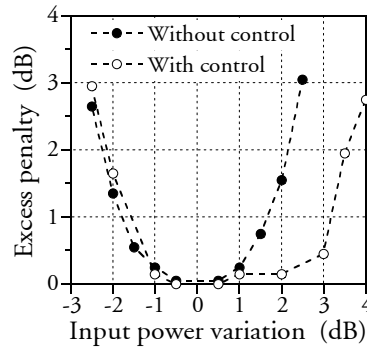
Fig. 4.17: The input power dynamic range with and without control for 40 Gbit/s differential wavelength conversion using an MZI. The excess penalty, which is measured at BER=10^{-9} is without the 0.55 dB insertion penalty.

Whether or not an IPDR of ~6 dB is sufficient in practice will depend on the application and placement of the converter in the network. Another solution for power equalisation is to place an amplifier in front of the IWC. In [86] an increase in IPDR from 2 dB to >20 dB is demonstrated through the use of a two-section SOA, while in [79] more than 40 dB of IPDR is achieved with an EDFA, however, at the expense of a response time in the ms-order. This indicates that external power equalisation is preferable if compensation for larger power fluctuations is needed, however, with the drawback of added complexity and cost.
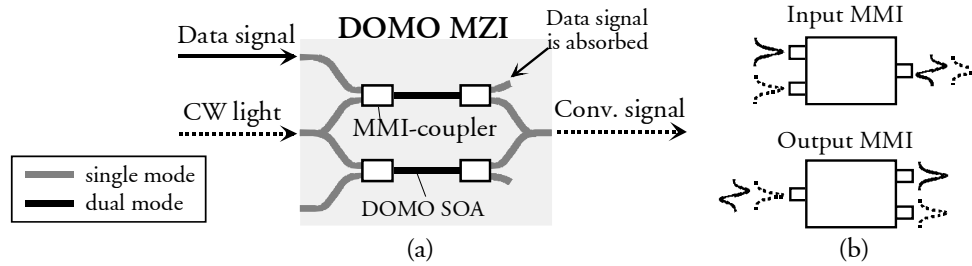
4.5 The dual-order mode Mach-Zehnder wavelength converter

As discussed in Chapter 2 and 3, one of the main applications of the wavelength converter is in switch nodes. Here, the large degree of wavelength flexibility that a large optical bandwidth gives, is important. As demonstrated in Section 4.3.1, the IWC exhibits excellent conversion capabilities over the entire EDFA range. However, in order to ensure the full wavelength flexibility that is needed in switch nodes, conversion to the same wavelength is desirable; simply bypassing the wavelength converter with the aid of a switch is not an attractive solution, as it adds complexity as well as causing a potential difference in signal quality dependent on whether conversion is done to the same wavelength or not. Thus, the converter itself will most likely do conversion to the same wavelength. As discussed in Section 4.2, this is possible with the MZI by injecting the data signal and CW-light counter-directionally into the device. However, as demonstrated in [72] counter-directional coupling causes pattern-dependent timing jitter, which limits the cascadability. Moreover, the conversion speed is limited by a modulation bandwidth, which is inherently lower than for co-directional coupling [87]. Another alternative to counter-directional coupling is a dual-stage converter, where conversion to the same wavelength can be achieved co-directionally through conversion to an internal wavelength in the first stage, and conversion back to the input wavelength in the second stage. This scheme has been demonstrated with good results at 20 Gbit/s using two MIs [88]. In spite of the good results obtainable with the dual-stage converter, the scheme may be undesirable in a system perspective due to the added complexity and cost. For these reasons, an alternative solution to conversion to the same wavelength is attractive.

Within recent years, single-stage co-directional wavelength conversion has been made possible with the development of the all-active dual-order mode (DOMO) MZI [89]. As shown in Fig. 4.18, this has been made possible by exploiting mode separation between the input data signal and CW-light achieved through placement of multi-mode interference (MMI) couplers [90] at the input and output of the interferometer arms. The DOMO MZI functions as follows: the data signal and CW-light are coupled into the device using the standard scheme (as in Fig. 4.2a). As the data signal traverses the upper input MMI, it is converted from the fundamental- to the first-order mode, while the CW-light remains in the fundamental mode. The interferometer arms are designed to sustain both lateral modes through an increase in the active layer width, thereby allowing propagation of both signals. At the output MMI, the data signal will, due to its mode symmetry, be directed to the upper output that leads to an unpumped waveguide, whereby it will be absorbed. The CW-light is guided through the lower output of the MMI to the output of the converter. Thus, co-directional wavelength conversion is allowed in one stage and the data signal is suppressed in the device itself, thereby allowing filterless operation as well as

conversion to the same wavelength. It should be noted that the former is very attractive if a tuneable output wavelength is required, as fast tuneable filters for packet switching purposes are as yet not commercially available, as discussed in Section 2.2.2.

It should be stressed that the principle of the input and output MMIs described above, as well as the illustration shown in Fig. 4.18b, are simplified strongly. Using [90] as a basis, it can be noted that the input and output MMIs are not identical: the input MMI is significantly more complex than the output MMI because conversion from fundamental to first order mode is not straightforward. Still, the overall scheme described above remains applicable.

Fig. 4.18: (a) Schematic of the dual-order mode Mach-Zehnder interferometer that allows co-directional conversion to the same wavelength through mode separation of the data signal and CW-light. MMI couplers are incorporated at the input and output of the interferometer arms, which sustain two lateral modes. (b) Principle of mode-conversion in the input and output MMIs, respectively, using the upper arm as an example.

In the following, results for conversion at 10 and 20 Gbit/s with a DOMO MZI having 1800 μm long interferometer arms will be assessed. The results are based on [Pub8,Pub14]. At 10 Gbit/s a tuneable NRZ transmitter and CW laser have been used in order to evaluate the wavelength dependency of the device.

An example of the performance of the DOMO MZI at 10 Gbit/s is given in Fig. 4.19, which shows the 10 Gbit/s back-to-back eye-diagram at 1550 nm (a), an eye-diagram for conversion from 1540 to 1550 nm (b), and the corresponding optical spectrum in 0.1 nm at the output of the converter. As indicated, the converted eye-diagram is clear and open, and clearly not limited by speed, although a small extinction ratio degradation has occurred. Focusing on Fig. 4.19c, it is seen that the DOMO MZI has successfully suppressed the input signal; the ratio between the power of the original input signal and the converted signal at the converter output, denoted the input signal suppression ratio (ISSR), is ~27 dB. It should be noted, that the ISSR is not dependent on the mode separation in the MMIs alone- it will also depend on the input power levels. In this case –7.7 dBm was used for the input data signal, while 4 dBm was used for the CW-light, clearly affecting the ISSR. Thus, the ISSR should not be evaluated as an absolute measure of the effectiveness of the DOMO scheme, but rather as an indication of the performance degradation

(penalty) that can be expected due to crosstalk in a practical system, since no filter is applied at the output of the DOMO MZI.
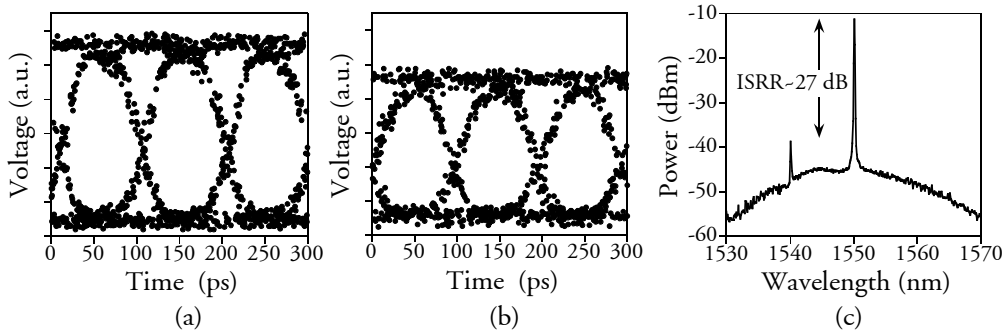
Fig. 4.19: Measured eye-diagram of the back-to-back signal at 1550 nm (a), after conversion from 1540 nm to 1550 nm (b), and the corresponding optical spectrum in 0.1 nm at the converter output, demonstrating an ISRR of ~27 dB (c).

An overview of the performance of the DOMO MZI at 10 Gbit/s is given in Fig. 4.20. The penalty and ISSR are shown when the signal wavelength is varied and the CW wavelength kept at 1550 nm (a), the CW wavelength is varied and the signal wavelength is fixed at 1550 nm (b), and the signal- and CW wavelengths are identical. Focusing first on Fig. 4.20a and b, it is seen that the insertion penalty for the DOMO converter is between ~1.2 and 2.4 dB when the signal and CW wavelengths are not identical. Moreover, the ISSR varies from ~15 to 29 dB. Here, conversion from 1550 to 1530 nm is not taken into account, in which case the penalty is ~4.5 dB. Furthermore, the ISSR is ~7 dB, partly due to a low converted output power as the wavelength is far from the gain peak. It would seem obvious to explain the high penalty with the low ISSR, which may attribute to power-addition crosstalk in the electrical receiver. However, a 1.4 nm optical filter is included in the preamplifier block in order to filter out ASE, why the original data signal, as a side effect, is suppressed entirely before the electrical receiver. Thus, the cause of the excess penalty for this specific wavelength combination must be found elsewhere

In general, long interferometer arms compromise the optical bandwidth, in analogy to what happens when filters are concatenated. However, it is seen that in spite of the fact that the DOMO MZI has 1800 μm long interferometer arms, the device has a large optical bandwidth. This may be due to a low effective confinement factor caused by the weak mode overlap between the data signal and the CW-light that is inherent of the DOMO scheme.

Finally, comparing Fig. 4.20c with a and b, it can be seen that conversion to the same wavelength results in a penalty that is approximately 2 dB larger than for conversion to a different wavelength. This can be explained as follows in a system perspective: when the signal- and CW wavelengths are not identical, a high ISSR is not as critical, as it simply determines the degree of power-addition crosstalk. It can be shown that ~7 dB

of crosstalk suppression (ISSR) is sufficient to ensure a 1 dB penalty for power-addition crosstalk [47,48]. However, when the signal- and CW wavelengths are identical, a large ISSR is critical for the performance as interferometric crosstalk is generated; ~20 dB of crosstalk suppression is necessary to limit the penalty to 1 dB [91], clearly explaining the relatively large penalty observed in Fig. 4.20c. As described in [92], the performance for conversion to the same wavelength is not only limited by the beating of the two signals at the converter output; also lateral mode beating in the interferometer arm(s) will lead to pattern-dependent cross-talk, which degrades the performance. Thus, the 3-4 dB penalty measured for conversion to the same wavelength may be attributed to a combination of these effects..
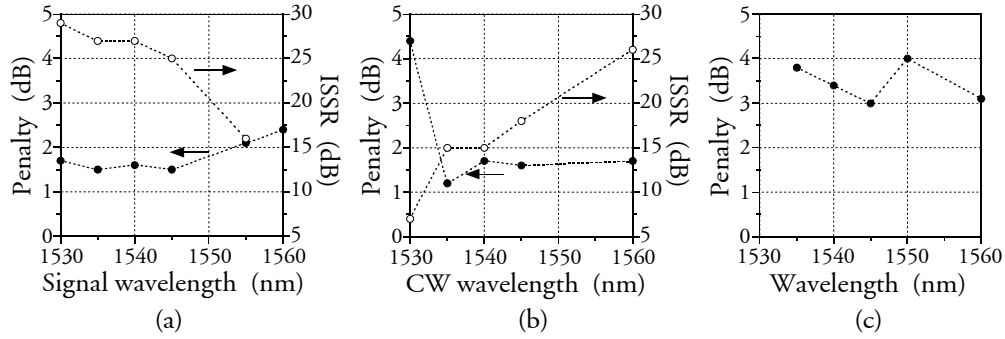
Fig. 4.20: Measured penalty and ISSR for 10 Gbit/s conversion using DOMO MZI. (a) Signal wavelength is varied and CW wavelength is 1550 nm. (b) CW wavelength is varied and signal wavelength is 1550 nm. (c) Signal- and CW wavelength are identical.

The difference in performance when conversion is done to the same and a different wavelength is also evident in Fig. 4.21. In Fig. 4.21a, an eye-diagram is shown for conversion from 1550.1 nm to 1550 nm, i.e., the signal- and CW wavelengths differ by ~0.1 nm (~12.5 GHz). Here, a good performance is obtained, in contrast to the eye-diagram in Fig. 4.21b, which shows the situation when the data signal wavelength subsequently has been adjusted to closely match the CW wavelength. In the latter case, the performance is severely degraded because the gain variation caused by lateral mode beating perturbs the mode symmetries, thereby distorting the converted signal. This effect becomes less prominent as the difference between the wavelengths of the data signal and CW-light is increased due to the limited carrier response in the SOA(s). Finally, in Fig. 4.21c, the operation point has been adjusted to compensate for this effect, whereby an improved signal quality is obtained. However, it can be seen by comparing Fig. 4.21a and c that optimising the operation point only improves the eye-diagram quality somewhat. It should be noted that the degradation seen in Fig. 4.21b does not occur because the original data signal, in this case, lies inside the electrical receiver bandwidth, while it does not in Fig. 4.21b; in both cases, a photodetector with a ~30 GHz bandwidth was used to achieve the eye-diagrams.
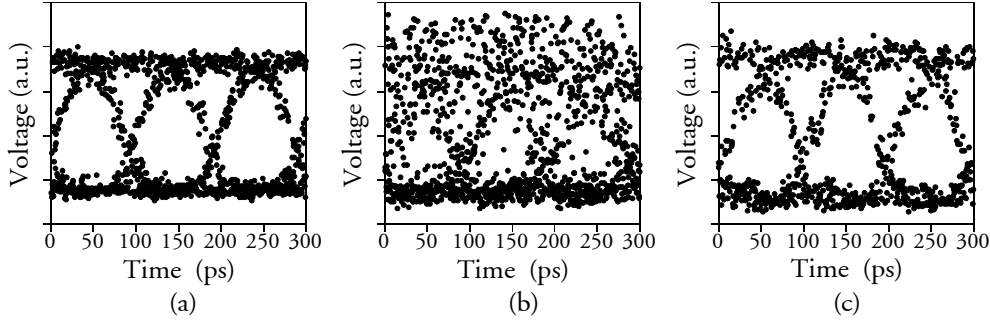
Fig. 4.21: Eye-diagrams of the 10 Gbit/s converted signal when the signal- and CW wavelengths differ by 0.1 nm (a), the wavelengths are adjusted to be identical, (c) the wavelengths are identical and the operation point is optimised.

The performance of the DOMO MZI has also been evaluated at 20 Gbit/s with the results shown in Fig. 4.22 for out-of-phase conversion (a), in-phase conversion (b) and the optical output spectrum in 0.1 nm (c). As seen, noisy but nevertheless open eye-diagrams are achieved. Furthermore, the optical spectrum demonstrates that conversion has been done with an output OSNR of ~30 dB and an ISSR of ~27 dB. Comparing the results in Fig. 4.22 with the results in Section 4.3.2 for the 2000 µm long standard MZI, it would seem that the conversion speed of the DOMO MZI at 20 Gbit/s should be higher, as the interferometer arms of the two MZIs are comparable in length. However, as shown in [92], since the DOMO interferometer arms have a larger optical area[33] than a standard SM MZI as they need to support two modes, the DOMO MZI inherently has a reduced conversion speed.
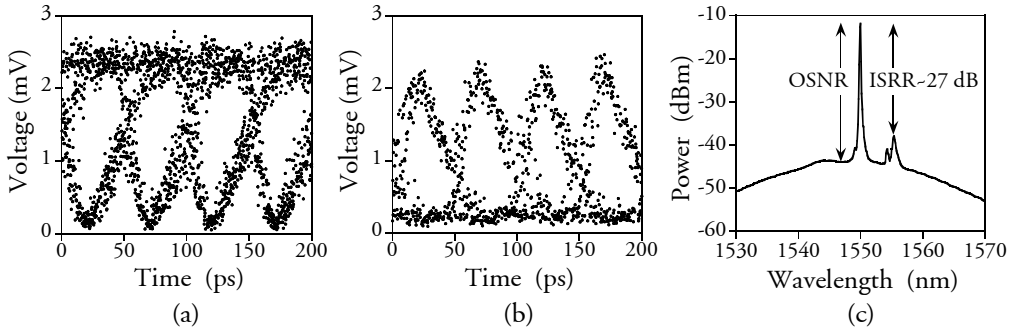
Fig. 4.22: 20 Gbit/s conversion from 1555 to 1550 nm. Eye-diagram for out-of-phase operation (a) and in-phase operation (b). (c) The optical output spectrum in 0.1 nm.

Taking the above discussion into account, it can be concluded that the pros and cons of the DOMO converter should evaluated before a decision is made as to whether or not this device should be employed in a system; flexibility with respect to wavelength choice and filterless operation are gained, however, at the expense of reduced conversion speed.

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[33] Optical area is defined as the ratio of cross-section area to optical confinement factor.

4.6 Novel scheme for interferometric wavelength conversion

Compared to, e.g., XGM, wavelength conversion using XPM is superior with respect to transmission capabilities because the chirp properties of the IWC are better. This is due to the fact that a smaller carrier density modulation is necessary to achieve the phase modulation (i.e., π phase shift) required for XPM conversion than what is the case for gain modulation when XGM conversion is employed. Still, there exists a trade-off between the modulation bandwidth and transmission properties of the IWC: as mentioned in Section 4.3.2 the conversion speed for standard out-of-phase conversion is normally higher than for in-phase conversion, while the transmission properties are inferior for out-of-phase operation due to the positive chirp parameter[34], which in analogy to the situation for XGM conversion (see Section 4.2) is detrimental for transmission on standard SM fibre due to pulse broadening.

In this section a novel conversion scheme that shows good transmission properties and high-speed performance simultaneously will be demonstrated. The scheme, which has been patented by Alcatel Opto+ in collaboration with COM [Pat1], also shows good regenerative capabilities, as demonstrated in Section 5.1.2.3 and [Pub17]. The results shown in this section are based on [Pub12,Pub21].

4.6.1 Principle of operation

The principle of operation using the standard scheme and novel scheme are compared in Fig. 4.23a and b, respectively. As seen, the novel scheme differs from the standard scheme in that a clock signal (at λ_{clk}) at the same rate as the input data signal (at λ_{in}) is coupled into the lower interferometer arm. The clock signal and data signal are synchronised in time to each other. The MZI is biased symmetrically so that pulses present in both interferometer arms (i.e., data signal is a mark) will cancel each other out at the MZI output, in analogy to the scheme used to create a well-defined conversion (switching) window in the differential control scheme (see Section 4.4.1). Thus, only when the input data signal is a mark will amplitude modulation occur at the converter output. As shown in Fig. 4.23b, this amplitude modulation can be either with non-inverted or inverted (i.e., "upside-down") pulses, depending on whether conversion has been performed on the positive or negative slope, respectively, of the MZI transfer function. As seen, operation on the positive slope (i.e., with non-inverted pulses) will result in a logical inversion[35] of the input data signal, why this mode of operation from now on will be denoted inverting. In analogy, operation on the negative slope (i.e., with inverted pulses) will be denoted

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[34] Chirp parameter, α: relates how the phase changes with the intensity [93]. Operation on the negative(positive) flank of the IWC transfer function in Fig. 4.2b gives a positive(negative) chirp parameter, meaning that the leading edges of the converted pulses are blue(red) shifted and the trailing edges are red(blue) shifted.

[35] Logical inversion: a logical 1-bit is changed to a 0 and vice versa.

non-inverting. Note that the scheme only works with the RZ format, in analogy to the differential control scheme.
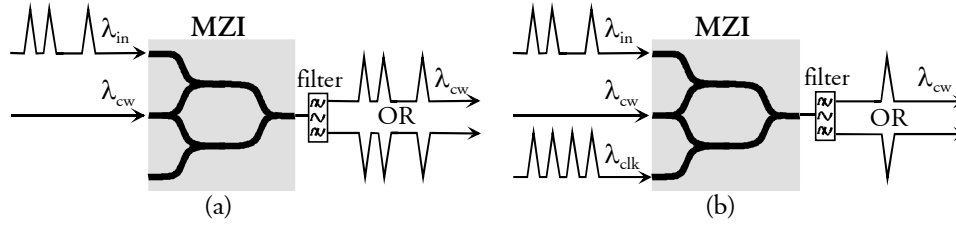
Fig. 4.23: Comparison of the principle of operation for conversion with the standard conversion scheme (a) and the novel scheme (b). At the converter output two different converted signals are shown; the upper is for operation on the positive flank of the IWC transfer function and the lower is for operation on the negative flank (see Fig. 4.2a). The novel scheme is also applicable with the MI.

It should be mentioned that, because a synchronised clock signal at the input signal rate is required for the novel scheme, practical implementation requires clock and phase recovery of the input data signal. Techniques for clock and phase recovery, both electrical and optical, will be discussed in more detail in Section 5.1.1, as they are also relevant for the implementation of 3R regenerators, which are discussed in Section 5.1.2.2.

4.6.2 Speed performance and transmission properties

The performance of the novel conversion scheme is assessed through comparison with results obtained for standard conversion using the set-up shown in Fig. 4.24. Clock pulses having a pulse width of ~26 ps are generated at 1546 nm and 1553 nm through modulation of gain-switched DFB lasers at 10 GHz. The clock pulses at 1546 nm are modulated at 10 Gbit/s using an MZ modulator, whereupon the hereby-generated 10 Gbit/s RZ data signal is coupled into the upper interferometer arm of an all-active MZI. Using an optical tuneable delay, the 1553 nm clock pulses are synchronised to the data pulses before injection into the lower interferometer arm of the MZI. CW light at 1556 nm is coupled into the common arm of the MZI, and at the output, the converted signal is selected using a filter whereupon a preamplified 10 Gbit/s receiver performs error counting. Standard SM fibre having a length of ~25 km is inserted at will before the receiver in order to assess the transmission capabilities of the scheme. Furthermore, a comparison is made with standard conversion using the same experimental set-up, except for the omission of the 1553 nm DFB laser and the optical tuneable delay.
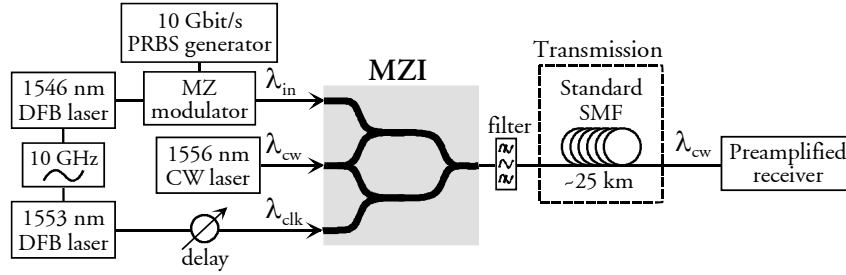
Fig. 4.24: Experimental set-up for assessment of the novel conversion scheme at 10 Gbit/s. The ~25 km of standard SM fibre is used for transmission experiments. The all-active MZI has interferometer arms with a length of 1200 μm.

An example of the performance of the novel scheme is given in Fig. 4.25, showing pulse traces (a) as well as BER curves (b) for the back-to-back signal and the converted signal for inverting operation. Comparing the two pulse traces, it can be seen that logical inversion indeed has been performed through the conversion scheme; a mark in the input signal has been replaced with a space and vice versa. The converted signal exhibits a slight pulse broadening, indicating the speed limitations of the MZI in response to the narrow pulses at the input. Nevertheless, the novel scheme performs well; a negligible penalty is incurred through the conversion process.
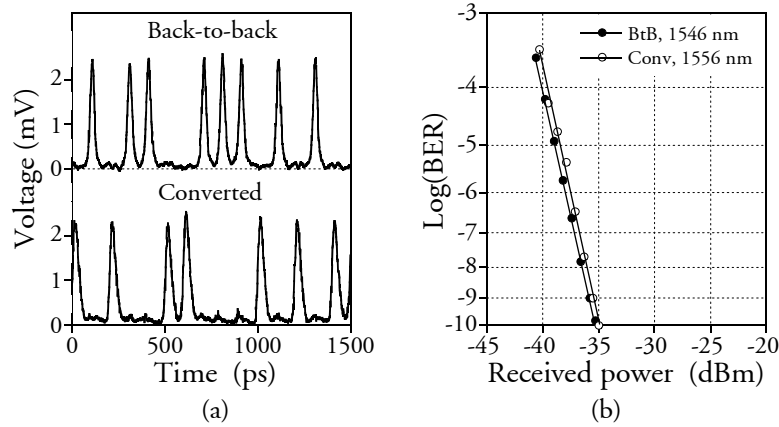
Fig. 4.25: Results of the novel conversion scheme for inverting operation: measured pulse traces (a) and BER curves (b) for the back-to-back signal and the converted signal.

In Fig. 4.26 are shown eye-diagrams at 10 Gbit/s for standard conversion with non-inverting- (a) and inverting operation (b) as well as for the novel conversion scheme with non-inverting- (c) and inverting operation (d). The good performance of the novel scheme is apparent: comparing Fig. 4.26a and d (non-inverted pulses), it can be seen that a narrower pulse width is achieved with the novel scheme, indicating a higher conversion speed. Comparing Fig. 4.26b and c, it can be seen that the eye-diagrams in this case are quite comparable, indicating similar performance when operating on the negative flank of the transfer function.
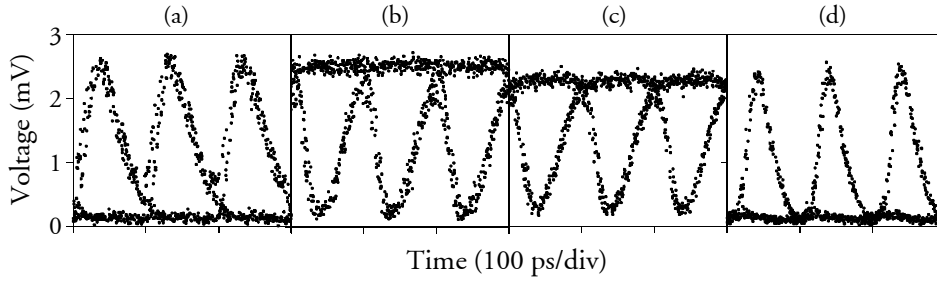
Fig. 4.26: Comparison of eye-diagrams for standard conversion and the novel conversion scheme at 10 Gbit/s- Standard scheme with non-inverting- (a) and inverting operation (b), novel scheme with non-inverting- (c) and inverting operation (d).

Results of BER measurements corresponding to the eye-diagrams in Fig. 4.26a, b and d are shown in Fig. 4.27a, along with the back-to-back BER curve. As seen, nearly penalty-free operation is achieved for standard inverting operation and the novel scheme (inverting operation). The highest penalty is observed for standard non-inverting operation, primarily due to the lower modulation bandwidth (cf., Fig. 4.26a). BER measurements obtained after subsequent transmission over ~25 km standard fibre are shown in Fig. 4.27b. For standard inverting operation, the detrimental effect of the positive chirp is apparent; a preamplified penalty of ~17 dB has been incurred by the transmission. In contrast, the penalty is very limited (~2 dB) for both standard non-inverting operation and the novel scheme with inverting operation, due to the negative sign of the chirp.
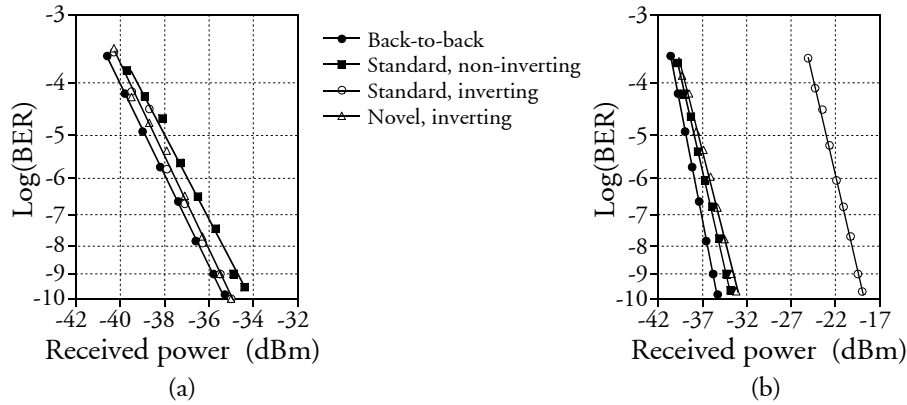
Fig. 4.27: BER measurements at 10 Gbit/s of the back-to-back signal and the converted signals using the standard and novel scheme before (a) and after (b) transmission over 25 km standard SM fibre.

The performance in these two cases is comparable because the sign of the chirp is solely dependent on whether pulse inversion occurs through the conversion process or not; if pulse inversion occurs (cf., Fig. 4.26b and c), the leading edge of the converted pulse will be blue shifted and the trailing edge will be red shifted, thus resulting in pulse broadening on standard SMF. If pulse inversion does not occur

(cf., Fig. 4.26a and d), the leading edge of the converted pulse will be red shifted and the trailing edge will be blue shifted, thus resulting in initial pulse compression on standard SMF, which may be beneficial for the transmission capabilities. Thus, although it is not shown here, results for the novel scheme with non-inverting operation are comparable to standard inverting operation. This is also verified in Fig. 4.28, which shows eye-diagrams after transmission over 25 km standard SM fibre corresponding to the eye-diagrams in Fig. 4.26. Clearly, the conversion methods that do not involve pulse inversion (Fig. 4.28a and d) have superior transmission capabilities, while the eye-diagrams in Fig. 4.28b and c are very distorted, which reflects the significant penalty shown in Fig. 4.27b.
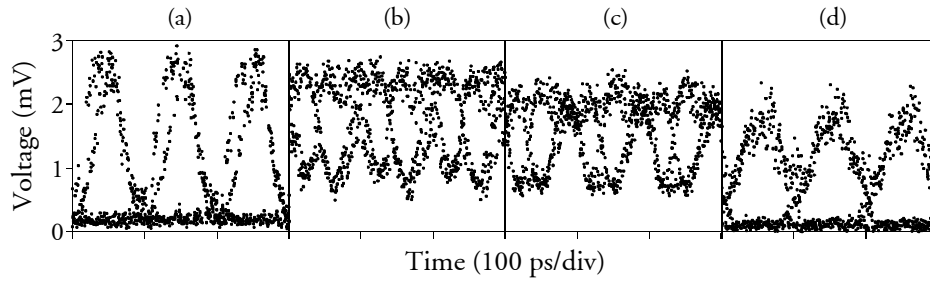
Fig. 4.28: Comparison of eye-diagrams after 25 km transmission over standard SMF for standard conversion and the novel conversion scheme at 10 Gbit/s- Standard scheme with non-inverting- (a) and inverting operation (b), novel scheme with non-inverting- (c) and inverting operation (d).

Thus, it has been demonstrated that the novel scheme operated in a logical inverting mode indeed combines the advantage of a high conversion speed in conjunction with superior transmission capabilities on standard SM fibre. These two characteristics are normally not compatible if the standard conversion scheme is employed, why the novel conversion scheme is advantageous in this respect. However, as the novel scheme requires an additional clock signal, which increases the complexity, the choice between the two schemes is not straightforward. Another factor, which would seem to pose a problem for the practical implementation of the novel scheme is that the clock pulses are required to be comparable in width to the data pulses. Experimental work has shown, however, that the width of the clock pulses may be as low as one fourth of the data pulse width without any noticeable effect on the performance (in the results shown in this section they are equal), a fact that can be exploited for re-timing [Pub17]. As will be discussed in Chapter 5, the standard scheme also offers re-timing through injection of a clock signal instead of CW-light into the common arm (cf. Fig. 4.23a). However, in this case the transmission capabilities of the converted signal will be strongly dependent on the spectral characteristics (e.g., chirp) of the clock signal. This is not the case for the novel scheme, as conversion is performed onto CW-light, thus greatly relaxing the requirements to the clock signal.

4.7 Summary

In this chapter different techniques for wavelength conversion have been compared, with the focus on schemes for interferometric wavelength conversion. It has been concluded that all-optical interferometric wavelength conversion has some clear advantages with respect to, e.g., high-speed performance, wavelength independence, transmission capabilities and cascadability that make it a prime candidate for application in future optical networks.

In the remainder of the chapter, the focus was on experimental results obtained with all-active integrated SOA-based Mach-Zehnder and Michelson interferometers fabricated by Alcatel Opto+. The wavelength independence of the integrated MI was verified at 10 Gbit/s with a preamplified penalty below 1 dB over the entire C-band. Using the standard conversion scheme, which excels in its simplicity and compatibility with both the RZ and NRZ format, 20 Gbit/s conversion using n MZI with 1200 μm long interferometer arms was demonstrated with a penalty of 0.8 dB. Furthermore, a noisy yet open eye-diagram was obtained at 40 Gbit/s using an MZI with long interferometer arms (2000 μm). However, to achieve very good results at bit rates higher than 20 Gbit/s, so far, a scheme to reduce the effect of the slow carrier recovery time in the interferometer arms is necessary. Thus, by applying the differential control scheme, as it is denoted, conversion with a limited penalty of 0.6 dB was achieved at 40 Gbit/s in n MZI. This was, however, at the expense of a format conversion from RZ to NRZ, which, as demonstrated, could be avoided with the use of the MZI with 2000 μm long interferometer arms. Finally, a scheme to increase the IPDR was described and demonstrated at 40 Gbit/s, with an increase from ~4.5 to ~6 dB to follow.

The problem of conversion to the same wavelength was discussed, and a novel type of IWC, namely the dual order mode converter, was proposed as a possible solution; with the DOMO converter, co-directional conversion in one stage without a filter is possible. The performance of a DOMO MZI was investigated at 10 Gbit/s, showing almost wavelength independent operation in the 1530 to 1560 nm range. With non-identical signal and CW wavelengths, a penalty of ~1.2 to 2.4 dB was incurred, while conversion to the same wavelength gave a penalty of 3-4 dB due to non-ideal suppression of the original data signal and lateral mode beating in the interferometer between the data- and CW signal. In addition, the capabilities of the DOMO MZI were demonstrated at 20 Gbit/s, where a noisy yet open eye-diagram was obtained in conjunction with an ISSR of ~27 dB.

Finally, a novel conversion scheme involving the injection of an additional clock signal into the IWC, has been presented. The scheme combines the advantages of good transmission properties and high-speed capabilities. Its feasibility has been verified at 10 Gbit/s and a comparison has been made with the standard conversion scheme, showing results that are comparable to the best for the standard scheme.

Chapter 5

Simple signal processing using IWCs

In the previous chapter the focus was on the application of SOA-based interferometers for all-optical wavelength conversion. Here, it was shown that these devices possess some very attractive characteristics, e.g., wavelength independence, good high-speed performance and transmission properties, that make them good candidates as wavelength converters in future all-optical networks.

In this chapter, the application of IWCs will be taken a step further; their use for simple signal processing will be discussed. The term "simple" is chosen as reference to signal processing in which only a single data signal is injected into the IWC (in conjunction with, e.g., a clock signal), in contrast to the employment of the IWC as a logic gate, which requires the injection of more than one data signal and thus places stricter requirements on the IWC. In Chapter 6, the application of the IWC as a logic gate will be described, and the implementation of more complex functionalities by combining multiple logic functions simultaneously in a single device will be discussed.

In Section 5.1, the focus is on all-optical regeneration. First, the basic concepts of signal regeneration will be explained, whereupon results will be given for simultaneous wavelength conversion and regeneration as well as for 2R regeneration without wavelength conversion using a pass-through scheme. As in Chapter 4, the results are based on all-active MZIs and MIs fabricated by Alcatel Opto+. In Section 5.2 techniques for time-division demultiplexing and multiplexing will be described. Furthermore, results will be given for simultaneous wavelength conversion and (de)multiplexing using a Mach-Zehnder interferometer.

5.1 All-optical regeneration

In the DAVID project, 3R regenerators that enable re-amplification, re-shaping and re-timing of data signals are, as discussed in Section 2.2.2, essential elements in the optical core packet routers. This is because the accumulation of detrimental effects that degrade signal quality during transmission and switching in nodes are among the main limitations to building large-scale optical networks [13,17]. Thus, without all-optical regeneration, large-scale networks must be constructed as transparent all-optical domains of limited size with data traffic between domains enabled through termination of the optical signals and electrical regeneration. To avoid this potential bottleneck, the all-optical regenerator is of great importance, why intensive research activities around the world are focussed on implementation of the first commercial all-optical regenerator.

5.1.1 Introduction to all-optical regeneration

Signal deterioration in future optical networks may typically be caused by loss in, e.g., transmission and fibres couplers in nodes, noise addition in EDFAs and SOAs, signal distortion and jitter in transmission links as well as extinction ratio degradation in optical SOA-based gates. Thus, re-amplification, re-shaping and re-timing are necessary to uphold the signal quality in large-scale networks. Fig. 5.1 shows a deteriorated signal that is regenerated in three steps corresponding to 1R, 2R and 3R regeneration. In the first step re-amplification is performed, typically using an EDFA. Unfortunately, the EDFA also adds noise, why re-amplification must be performed frequently to ensure that the signal-to-noise ratio is kept high. In the second step, re-shaping is performed. As indicated, this involves the suppression of fluctuations on the one-level and zero-level of an amplitude-modulated signal. These fluctuations may, e.g., be caused by noise addition from the EDFAs used for 1R regeneration. The third step involves re-timing of the data signal to remove jitter, which may, e.g., originate from EDFAs as well as during transmission. It can be mentioned that, according to [94], optical networks based solely on EDFA technology are typically limited to 6-10 spans, or a 500-800 km route, before 3R regeneration is necessary.
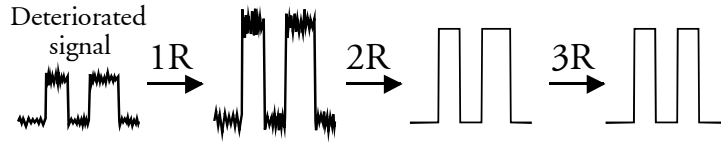
Fig. 5.1: Schematic of the regeneration process for a deteriorated signal. 1R: re-amplification, 2R: re-amplification + re-shaping, 3R: re-amplification + re-shaping + re-timing.

2R regeneration is an inherent attribute of the IWC due to the sinusoidal transfer function. Note that for IWCs, 2R regeneration normally only refers to re-shaping and not re-amplification because net gain is not always ensured. However, an EDFA placed after the IWC would solve this problem, why IWCs are referred to as 2R regenerators. The principle of re-shaping is shown schematically in Fig. 5.2, where a noisy signal is input to the IWC. The sinusoidal transfer function of the IWC is shown together with the transfer function of an ideal decision gate. The horizontal parts of the ideal decision gate ensure that all power fluctuations on the input signal are completely suppressed, while the vertical (input power) level acts as a decision threshold, making it the ideal 2R regenerator for amplitude modulated signals. However, since the IWC's transfer function is sinusoidal and not digital, complete 2R regeneration is not possible. Still, if operated on the flat parts of the transfer function good suppression of power fluctuations is possible, as will be demonstrated in Section 5.1.2.1. Furthermore, if multiple IWCs are cascaded, amplitude restoration combined with decision thresholding can be achieved [95]. This is due to the fact that concatenating the sinusoidal transfer function of the IWC will produce

a response that evolves towards a digital transfer function. Thus, input data signals having power levels above the threshold are transformed to have equal peak powers, while signals with power levels below the threshold will be suppressed effectively.
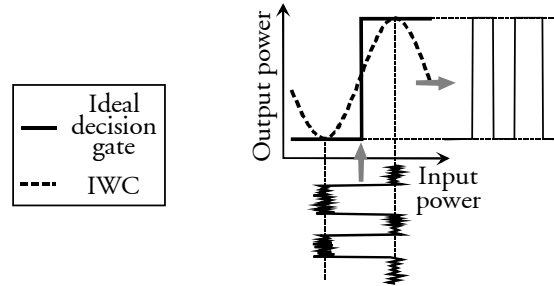
Fig. 5.2: The principle of re-shaping using an IWC. The sinusoidal transfer function of an IWC is compared to the transfer function of an ideal decision gate, which, as shown, completely suppresses input power fluctuations.

The principle of re-timing, which is necessary for 3R regeneration, is shown schematically in Fig. 5.3. The data signal to be re-timed is coupled into an IWC together with a clock signal recovered from the data signal. Through wavelength conversion, the clock signal will effectively sample the data signal, whereby the phase fluctuations on the data signal are converted into amplitude fluctuations on the converted output signal. This is exemplified by the second mark in the data sequence, which is severely mistimed by jitter so that the corresponding clock pulse falls partly outside the window of the data pulse. Thus, the converted output pulse has a reduced peak power, which, however, is partially compensated for through the sinusoidal transfer function of the IWC shown in Fig. 5.2.
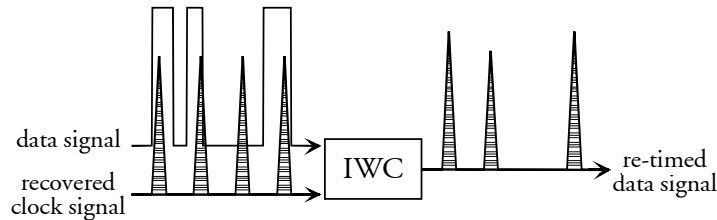
Fig. 5.3: The principle of re-timing using an IWC. A clock signal recovered from data signal is coupled into the IWC in synchronisation with the data signal. In the IWC phase fluctuations are converted to amplitude fluctuations.

It should be noted that the generation of a clock signal, synchronised in frequency and phase to the original data signal, is not a trivial task. For packet-switched applications, where data transmission is not continuous, the main requirement to clock and phase recovery is a fast locking time. No standard method is developed to enable this in the electrical domain. However, some different schemes have been proposed. In [96], a short pulse is generated for every transition from low to high and a subsequent bandpass filter and limiting amplifier allows the generation of a

recovered clock. Unfortunately, the scheme is very temperature sensitive for the NRZ signal format. Another scheme uses parallel versions of a local clock, shifted fractions of a bit period through the use of delay lines, to detect a transition from low to high [97]. Alternatively, within recent years some very impressive results on all-optical clock recovery based on a self-pulsating DFB laser have been demonstrated. When a data signal is injected into the laser, it responds by generating a clock signal at the same rate as the original data signal, providing the frequency is within the laser's locking range. In [98] a self-pulsating laser that locks to a data signal within 1 ns, has a locking range of 40 GHz and synchronises both in frequency and phase has been demonstrated at 10 Gbit/s. Furthermore, the application of the self-pulsating DFB laser for 3R regeneration at 40 Gbit/s has been demonstrated in [14]; transmission over more than 10,000 km in a loop experiment has been enabled by the 40 GHz all-optical clock. It should be mentioned that all the schemes discussed here suffer from the disadvantage of potential clock loss for a long string of transitionless data, why scrambling may be necessary to avoid this.

5.1.2   Simultaneous regeneration and wavelength conversion

For many applications of regenerators, combined wavelength conversion is beneficial. As an example, in the DAVID core packet router architecture (see Fig. 2.4) 3R regenerators that perform simultaneous wavelength conversion are placed at the input and output of the OPR. This enables decoupling between the wavelengths used externally on the transmission link and the wavelengths used internally in the OPR, while keeping the signal quality high. In the DAVID project, the key element in the 3R regenerator is the all-active MZI. In the following, results will here be given on 40 Gbit/s simultaneous regeneration and wavelength conversion using the same MZI device that was employed for the 20 and 40 Gbit/s wavelength conversion experiments presented in Chapter 4. The results are based on [Pub5,Pub7,Pub12].

5.1.2.1   2R regeneration at 40 Gbit/s in an all-active MZI

The set-up for 2R regeneration at 40 Gbit/s is illustrated in Fig. 5.4, which, except for the noise generator, is identical to the one in Fig. 4.13. The noise generator, which consists of an attenuator and EDFA followed by a filter, is used to assess the regenerative capabilities of the MZI. The attenuator allows variation of the input OSNR to the MZI, thus simulating noise accumulation from cascaded EDFAs. The bandpass filter at the output of the EDFA simulates a demultiplexer that would be present in a practical WDM system. Finally, at the output of the converter a part of the signal is tapped off to a spectrum analyser to measure the output OSNR.
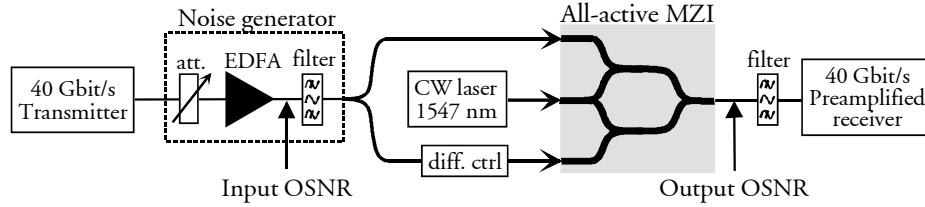
Fig. 5.4: Experimental set-up for assessment of the 2R regenerative capabilities of a 1200 µm long MZI. Except for the noise generator, the set-up is identical to the one in Fig. 4.13 used for 40 Gbit/s differential wavelength conversion.

Fig. 5.5a shows the OSNR in 0.1 nm measured at the input and output of the converter as a function of the input power to the EDFA in the noise generator. In spite of the reduction in input OSNR to the MZI as the EDFA input power is reduced, a high OSNR is preserved at the output of the converter. This is possible since the spectral characteristics of the CW source and the low ASE level of the converter determine the spectrum at the MZI output. In this experiment, the OSNR is kept above 37 dB even for input OSNR levels as low as ~13 dB. Although it is clear that having a high OSNR at the output of the regenerator is a very important factor for cascadability, it must be stressed that the OSNR improvement seen in the experiments does not directly reflect the regenerative capabilities of the MZI, as it contains no information about the output extinction ratio, pulse shape, etc.; penalty measurements, as given in Fig. 5.5b, are necessary to quantify the regenerative capabilities of the IWC. In the figure, the excess penalty with and without the converter inserted is shown as a function of the input power to the EDFA. The excess penalty is depicted in order to focus on the regenerative capabilities of the MZI alone (the insertion penalty is 0.7 dB, cf., Fig. 4.14c). It can be seen that noise suppression is obtained for EDFA input powers below –20 dBm, corresponding to
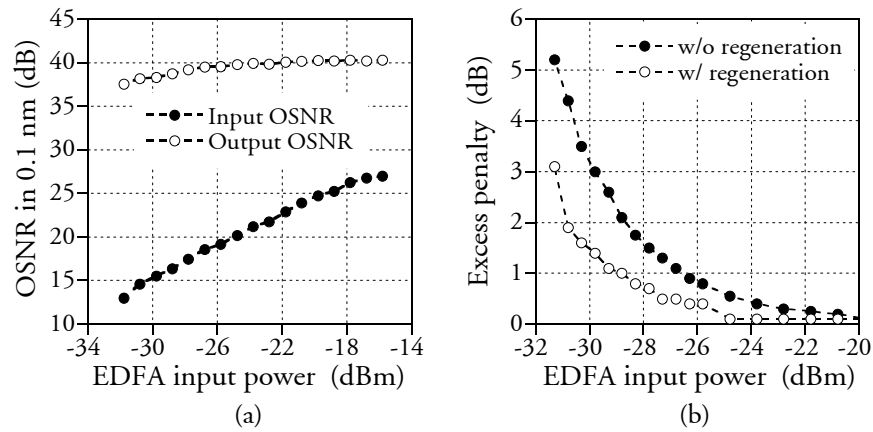
Fig. 5.5: Optical signal-to-noise ratio at the MZI input and output (a) and the excess penalty with and without the regenerator (b) at 40 Gbit/s versus the input power to the EDFA in the noise generator.

input OSNRs below 25 dBm. As an example, for an excess preamplified penalty of 2 dB, more than 2 dB lower input power can be accepted to the EDFA through insertion of the regenerator, corresponding to ~2 dB lower OSNR. This allows for ~10 km longer transmission spans before amplification, assuming a fibre loss of 0.2 dB/km. This regeneration can, apart from increasing the repeater spacing, also be used to relax the power budget or to increase the total transmission distance.

It should be noted that regeneration using the MZI or MI is just as efficient with the standard conversion scheme shown in Fig. 4.2a as with the differential control scheme. Here, the differential scheme is solely used to improve the performance at 40 Gbit/s.

5.1.2.2   3R regeneration at 40 Gbit/s in an all-active MZI

For large-scale networks, 2R regeneration is not sufficient to ensure a good end-to-end performance, as jitter accumulation will be a limiting factor. Thus, 3R regeneration, which involves 2R regeneration combined with re-timing, is necessary. As discussed in Section 5.1.1, all-optical 3R regeneration involves the employment of a clock signal recovered from the data signal. Once this has been generated, the principle of 3R regeneration in an MZI using the differential control scheme is as shown in Fig. 5.6. Note that the differential control block, as shown in Fig. 4.11a, is omitted from the illustration for simplicity. As illustrated, the data signal is split and coupled into the interferometer arms of the MZI as dictated by the differential control scheme, whereas the clock signal is coupled into the common arm in synchronisation with the data signal. The wavelength converted output signal will thus be a 3R regenerated version of the original data signal, where re-shaping and re-timing is enabled as described in Section 5.1.1. Conversion to a clock signal instead of CW-light, as employed for wavelength conversion, has some additional benefits apart from re-timing. Firstly, it is easier to obtain a high output extinction ratio due to the modulation of the clock signal. Secondly, short output pulses can be obtained since the width of the clock pulses determines the width of the converted output pulses. It should be noted that, in analogy to 2R regeneration, 3R regeneration is just as efficient using the standard conversion scheme as the differential scheme shown in Fig. 5.6. Conversion to a clock signal, and therefore 3R regeneration is also applicable for the MI, TOAD, DISC and UNI.
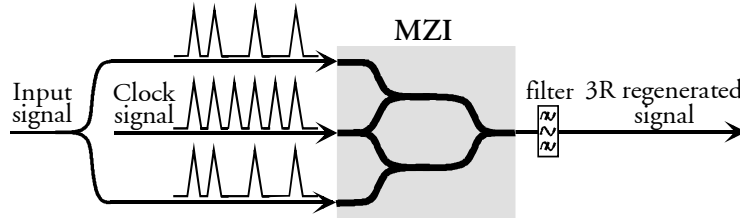
Fig. 5.6: Schematic of the set-up used for 3R regeneration in an MZI.

Fig. 5.7 shows the effect of conversion to clock pulses on the pulse shape of the converted signal. In Fig. 5.7a is shown an eye-diagram achieved with differential conversion to CW-light at 10 Gbit/s (identical to Fig. 4.12c), while Fig. 5.7b shows the result when conversion is performed onto a 10 GHz clock signal. Comparing the two eye-diagrams, it can be seen that, due to the narrow switching window (cf., Section 4.4.1), a limited extinction ratio is achieved when converting to CW-light (a). This is in contrast to the high extinction ratio achieved through conversion to a clock signal (b), which is enabled by the large peak power in the clock pulses and the fact that the MZI can be optimised to ensure a low amplitude level for the converted spaces.
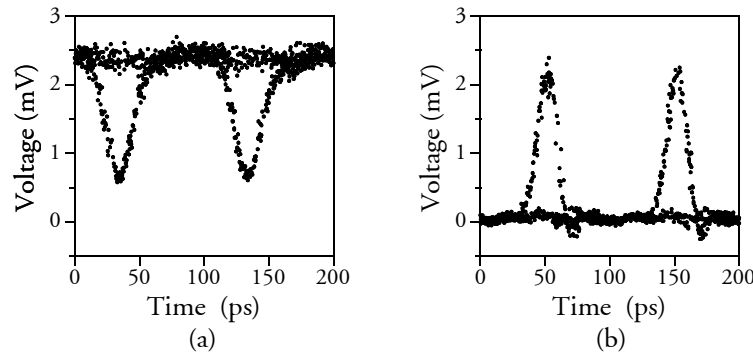
Fig. 5.7: Comparison of eye-diagrams at 10 Gbit/s with differential conversion to CW-light (a) and conversion onto a 10 GHz clock signal (b).

It can also be noted that, because the clock signal determines the shape of the converted signal, pulse inversion is avoided and a narrow pulse width, determined by the width of the clock pulses, is obtained. Thus, when converting to a clock signal, out-of-phase (OOP) and in-phase (IP) operation is only differentiated by whether or not a logical inversion has occurred. This means that IP operation is equivalent to standard conversion with operation on the positive flank of the IWC transfer function (see Fig. 4.23a), while OOP operation corresponds to conversion using the novel scheme with operation on the positive flank (see Fig. 4.23b). As discussed in Section 4.6.2, this means for IP operation that the sign of the chirp is advantageous for transmission on standard single-mode fibre. However, the chirp characteristics for OOP conversion to a clock signal differ from IP conversion using the novel scheme for the following reason: frequency chirp does not occur when the input signal is a space (assuming the clock signal does not cause chirp). For OOP operation the clock pulses are only present in the converted signal when the data signal is a space. Thus, OOP conversion to a clock signal will only inflict minor chirp on the converted signal, making the transmission performance advantageous for longer transmission distances and more or less independent of the dispersion sign. Finally, it should be noted that, in any case, the spectral characteristics of the 3R regenerated signal depends highly on the spectral characteristics of the clock signal. Thus, the technique used to generate the

clock pulses must be chosen wisely to enable good transmission properties and low jitter. For example, as a general trend it can be mentioned that semiconductor-based short pulse lasers are associated with a larger degree of chirp and timing jitter than fibre-based lasers due to carrier modulation. These problems can, however, be alleviated, e.g., through compensation with a chirped grating and active mode-locking using an EA-modulator, as demonstrated in [99].

The performance of the 3R regenerator in Fig. 5.6 is assessed at 40 Gbit/s using a set-up identical to the one in Fig. 5.4, except that the CW source is replaced by a clock signal. The clock signal is generated through modulation of a gain-switched laser at 10 GHz, pulse compression to a FWHM width of 6 ps in a DCF, and subsequent passive optical multiplexing to 40 GHz. Note that no clock recovery is necessary in the experiment, as transmission is not performed. In Fig. 5.8 is shown the 40 Gbit/s back-to-back eye-diagram at 1554 nm (a), the converted and 3R regenerated eye-diagram at 1547 nm (b) as well as the corresponding BER curves (c). As seen, the converted eye-diagram is clear and open with a high extinction ratio and RZ format preservation. The latter is in contrast to the eye-diagram achieved for 40 Gbit/s conversion to CW-light using the same device, where format conversion from RZ to NRZ occurred as a result of the MZI's limited modulation bandwidth (see Fig. 4.14). Note that the small penalty of 0.5 dB is caused by a minor broadening of the base level in the eye-diagram.
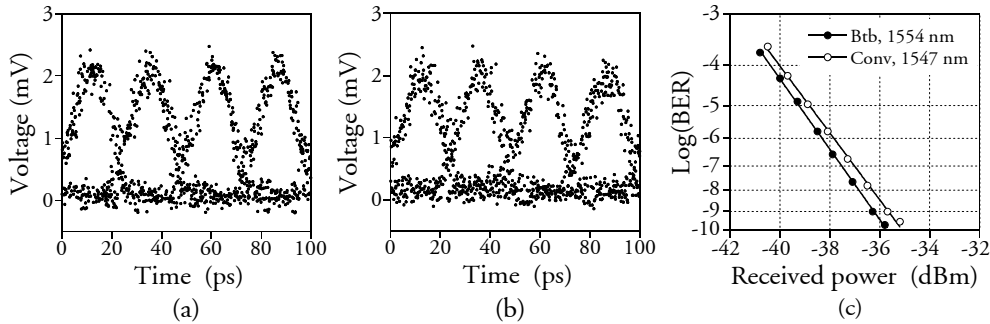
Fig. 5.8: Eye-diagram at 40 Gbit/s of the back-to-back signal (a), after conversion to a clock signal (b) and the resulting BER curves after demultiplexing to 10 Gbit/s.

In the results shown above, the principle of re-timing using an IWC has been demonstrated, but the tolerance towards timing jitter has not been assessed. This has, however, been done at 20 Gbit/s in [100] using a Michelson interferometer. In this paper, the jitter tolerance has been assessed statically by detuning the clock signal with respect to the data signal and measuring the hereby-induced power penalty. It was shown that jitter levels in excess of ±7 ps could be tolerated for a penalty below 1 dB, thus indicating the efficiency of the scheme for 3R regeneration. Moreover, using the DISC, 3R regeneration has been demonstrated at 40 Gbit/s with a jitter tolerance of ±6 ps in [101].

Finally, some very impressive results obtained using the MZI for 3R regeneration should be mentioned: by cascading two MZIs, the first one performing 3R regeneration as discussed above, and the second one performing 2R regeneration as described in Section 5.1.2.1, a very powerful 3R regenerator is obtained because cascading IWC results in a transfer function closer to the ideal decision gate, which improves the noise suppression capabilities (cf., Section 5.1.1). This scheme is employed in the DAVID project with the following configuration: the first stage, which uses the standard conversion scheme for 3R regeneration, is operated on the negative flank of the transfer function, which, as discussed in Section 4.6.2, improves the high-speed performance. The second stage, which uses the differential scheme for 2R regeneration, operates on the positive flank of the transfer function, thus ensuring that the sign of the chirp is beneficial for transmission on SM fibre. Using this dual-stage configuration, 1000 3R regenerators have been cascaded over 170.000 km at 10 Gbit/s using standard conversion in both MZIs [15] and 200 regenerators have been cascaded over 20.000 km at 20 Gbit/s using differential conversion in the second stage [16].

5.1.2.3 Regenerative capabilities of the novel conversion scheme

As mentioned briefly in the previous chapter, the novel conversion scheme, which was the topic of Section 4.6, also possesses regenerative capabilities. This is demonstrated at 10 Gbit/s through insertion of a noise generator at the data input of the converter in Fig. 4.24 (i.e., the upper interferometer arm). In Fig. 5.9a, the input and output OSNR is shown as a function of the input power to the EDFA in the noise generator, while Fig. 5.9b shows the penalty without and with regeneration versus the EDFA input power. As illustrated, a high OSNR above 30 dB is preserved
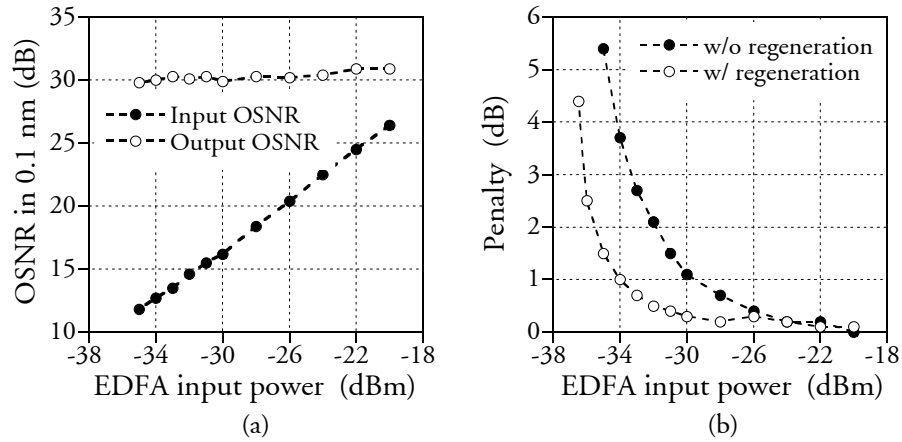

Fig. 5.9: Verification of the regenerative capabilities of the novel scheme- OSNR in 0.1 nm (a) and penalty without and with the regenerator versus the input power to the EDFA in the noise generator.

regardless of the input OSNR, and excellent regenerative capabilities are achieved; a ~4 dB lower input power level to the EDFA can be tolerated at a 2 dB penalty when the regenerator is inserted.

The application of the novel scheme in a 3R regenerator has also been verified in [Pub17], where the regenerator is a two-stage architecture, each employing an all-active MZI. In the first stage, 3R regeneration is performed using the scheme illustrated in Section 5.1.2.1 with standard conversion, while in the second stage the novel conversion scheme is used, as shown in Fig. 4.23b. The second stage enables improved overall re-shaping capabilities due to the excellent regenerative properties demonstrated in Fig. 5.9b, while enabling very good transmission properties and high-speed operation as shown in Section 4.6.2. The good performance was verified in a recirculating loop with 50 km SMF and no dispersion compensation, where more than 300 loop rounds were achieved at 10 Gbit/s without noise and jitter accumulation [Pub17].

5.1.3 2R regeneration without wavelength conversion using the pass-through scheme

So far, schemes for all-optical regeneration presented in this chapter have involved wavelength conversion, which means that additional components such as a CW laser, optical filter, etc. are needed. However, for some applications of regenerators, wavelength conversion may not be desirable, why a scheme for all-optical regeneration without wavelength conversion, as will be presented here, is attractive for complexity and cost reasons.

5.1.3.1 Operating principle of the pass-through scheme

The principle of the pass-through scheme, as it is denoted, is illustrated schematically in Fig. 5.10 with a Mach-Zehnder interferometer (the scheme is identical for the MI). As indicated in Fig. 5.10a, the bias currents I_1 and I_2 are applied to the upper and lower interferometer arm, respectively, and a data signal with the input power P_{in} is coupled into the MZI. The optical signal is split equally to the two interferometer arms, and is combined again at the output of the device. As the optical signal propagates through the SOAs, the gains and phase changes (G_1, ϕ_1) and (G_2, ϕ_2) are induced in the upper and lower arm, respectively, as a function of the input power P_{in} as shown in Fig. 5.10b (upper and middle). As the optical signal recombines at the output, constructive or destructive interference will occur depending on the phase difference between the two arms, as shown in Fig. 5.10b (lower). As seen, the phase difference is constant for P_{in} lower than P_1 and higher than P_2, while it increases for power levels between P_1 and P_2. Thus, by exploiting that the SOA's saturation power is current dependent, a quasi-digital transfer function is achieved. It should be noted that total destructive interference cannot be achieved at low input powers due to the different gain in the two interferometer arms. Furthermore, since the output power is directly proportional

to the input power for low power levels[36], reshaping of spaces will be poorer for the pass-though scheme than for marks, in contrast to 2R regeneration combined with wavelength conversion. The pass-through scheme was first proposed using gain-clamped SOAs (GC-SOAs) as the active elements in the interferometer arms [102]. In GC-SOAs asymmetric biasing results in different saturation powers but equal gains, thus allowing perfect destructive interference at low powers. Unfortunately, GC-SOAs cause relaxation oscillations and therefore signal distortion at bit rates above ~10 Gbit/s (depending on device specifics) [Pub9]. Thus, the practical application of the GC-SOA for the pass-through scheme is limited. Another alternative, which unfortunately has not been tested in practice, is the employment of conventional SOAs of different lengths and effective optical areas, thus allowing equal gain but different saturation input powers for asymmetric biasing [71][37].
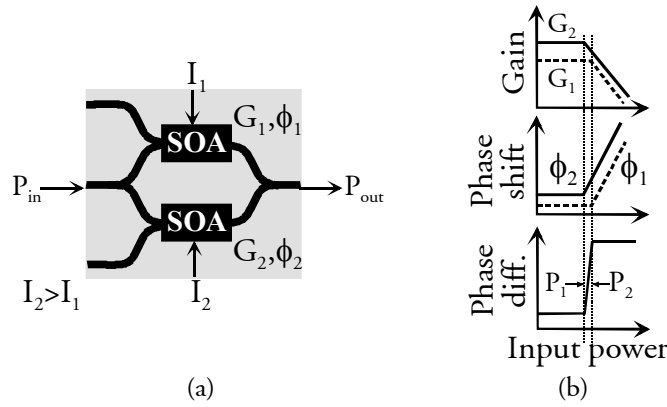
Fig. 5.10: The principle of the pass-through scheme using an MZI- (a) Signal enters and exits the MZI as shown and bias currents are applied to interferometer arms with $I_2 > I_1$. Thus, the gains and phase changes (G_1, ϕ_1) and (G_2, ϕ_2) are induced in the upper and lower arm, respectively. (b) Gain and phase shift in the SOAs and the corresponding phase difference that the signal experiences as a function of the input power.

In the following, 40 Gbit/s regeneration in an MZI will be demonstrated. The results shown are based on [Pub1].

5.1.3.2   2R regeneration at 40 Gbit/s in an all-active MZI

In Fig. 5.11 is shown the set-up for evaluation of the regenerative capabilities of the pass-through scheme at 40 Gbit/s using the all-active MZI with 1200 μm long interferometer arms, which was also employed for the experiments described in

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[36] This can be understood by noting that the transfer function is identical to equation (4.1), except the terms $P_{cw,in}$ and $P_{cw,out}$ should be replaced by P_{in} and P_{out}. Additionally, both the SOA gain and phase change is more or less input power independent for low power levels, why the output power is proportional to the input power.
[37] Here, equal path lengths should be maintained through addition of a passive section to the arm with the short SOA.

Section 5.1.2. As seen, a noise generator is placed at the input to the MZI. However, no filter is placed between the output of the MZI and the 40 Gbit/s receiver, meaning that no ASE-filtering is performed compared to back-to-back.
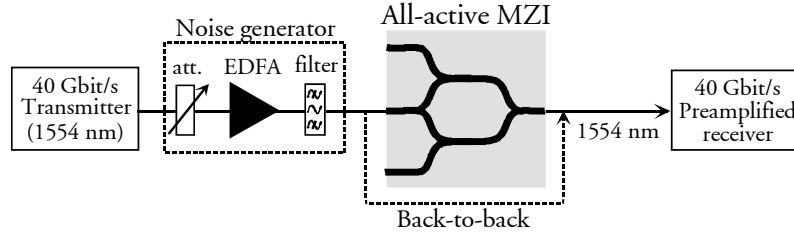
Fig. 5.11: Experimental set-up for assessment of the regenerative capabilities of the pass-through scheme at 40 Gbit/s using an MZI. The signal wavelength is 1554 nm.

Using the experimental set-up shown in Fig. 5.11, the pass-through scheme has been verified at 40 Gbit/s with the results shown in Fig. 5.12. Here, the back-to-back eye-diagram (a) and the eye-diagram obtained at the MZI output (b) are shown together with results of BER measurements after demultiplexing to 10 Gbit/s (c). As indicated by the eye-diagrams, the pass-through scheme has been employed with good result, as the output signal from the MZI is almost identical to the back-to-back signal. Note, by comparing with Fig. 5.12c, that a small penalty of ~0.3 dB is incurred, most likely due to the marginally noisier output eye-diagram. Finally, it can be mentioned that the MZI is inserted without loss; ~5 dBm of optical power was measured both at the input and output of the device. Furthermore, a high output signal-to-noise ratio of approximately 46 dB in 0.1 nm resolution bandwidth is obtained.
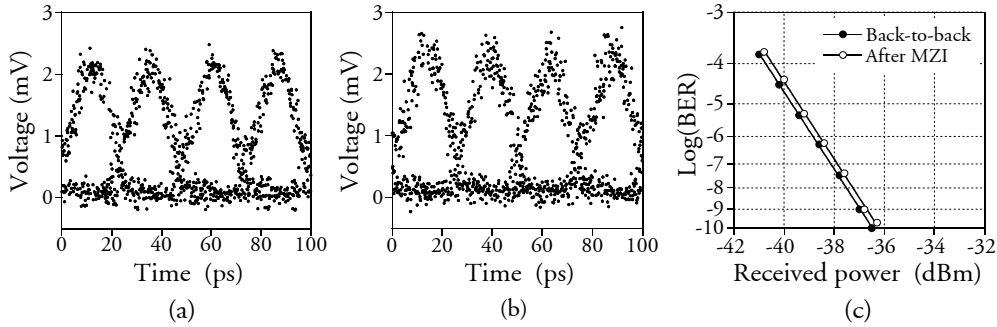
Fig. 5.12: Eye-diagram of the 40 Gbit/s back-to-back signal (a) and output signal from the MZI (b) and the corresponding BER curves after demultiplexing to 10 Gbit/s. The wavelength is 1554 nm.

The regenerative capabilities of the MZI have been assessed at 40 Gbit/s with the results shown in Fig. 5.13a. Here, it can be seen that noise suppression is achieved for EDFA input powers lower than ~18 dB. Furthermore, ~2.5 dB less input power to the EDFA can be accepted at a 2 dB penalty with the pass-through scheme. As shown in Fig. 5.13b, a very attractive effect of the quasi-digital transfer function is a large input

power dynamic range; an IPDR in excess of ~16 dB is achieved at a pre-amplified penalty of 2 dB. In comparison, IWCs used as wavelength converters only have an IPDR of ~3-4 dB due to the sinusoidal transfer function, as discussed in Section 4.4.3.
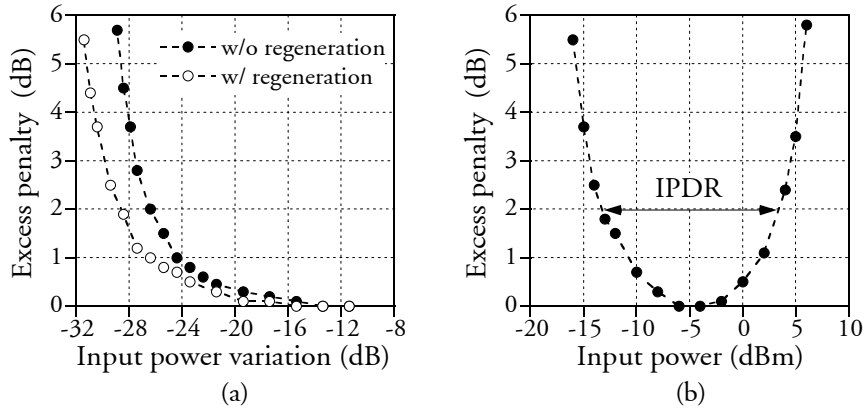
Fig. 5.13: (a) Excess penalty at 40 Gbit/s with and without the pass-through regenerator as a function of the input power to the EDFA in the noise generator. (b) Excess penalty as a function of the input power to the MZI, showing an IPDR in excess of 16 dB at a pre-amplified penalty of 2 dB. The signal wavelength is 1554 nm.

5.2 Simultaneous (de)multiplexing and wavelength conversion

In future extensions of the DAVID project, one may envisage that traffic aggregation at the MAN-WAN interface is not performed in the electrical domain (see Chapter 2), but rather all-optically in so-called photonic gateways through optical time-division multiplexing of lower bit rate data streams to higher bit rates. Furthermore, this single-channel bit rate increase may be combined with WDM to allow an even higher capacity in the WAN. In analogy, the reverse process, which involves all-optical time-division demultiplexing, would be necessary in order to drop traffic to the MAN from the WAN. Thus, the implementation of a photonic gateway involves conversion of a number of low bit rate WDM data streams to a (few) high bit rate OTDM stream(s) and vice versa. This rate adaptation requires a high degree of wavelength and bit rate flexibility, making the IWC an attractive candidate for this purpose.

In this section, application of the all-active MZI for simultaneous wavelength conversion and time-division multiplexing and demultiplexing will be demonstrated. The results are based on [Pub7,Pub27].

5.2.1 All-optical time division demultiplexing

In Fig. 5.14 are shown two different differential schemes for demultiplexing in a MZI. In the upper figure (a) demultiplexing is performed without wavelength conversion through injection of a lower rate clock signal into the interferometer arms of the MZI using the differential control scheme (not shown here) and

injection of the data signal into the common arm. Thus, the clock pulses enable selective switching of the input signal to the output of the MZI; the clock pulses modulate the phase of the lower-rate data channel that they are synchronised to, which enables constructive interference of this specific channel at the MZI output, while the remaining a suppressed. It should be noted that, as for 3R regeneration, clock recovery is required to generate the lower-rate clock signal that is needed for demultiplexing.

An alternative scheme for demultiplexing with simultaneous wavelength conversion is shown in Fig. 5.14b. Here, the data signal to be demultiplexed is injected into the interferometer arms using the differential scheme and the clock signal is coupled into the common arm. Thus, the clock signal functions as a probe, which samples the input signal, whereby the data encoded on the channel synchronised to the clock signal is modulated onto the clock pulses, which are selected at the output using a filter.

There are advantages and disadvantages to both demultiplexing schemes. Concerning the scheme in Fig. 5.14a, the carrier recovery rate is not a critical factor, as the modulation is performed by a lower-rate clock signal. This also means that any potential pattern dependency of the SOAs due to a limited response time will not affect the performance of the scheme. However, the output pulse shape is determined by the input data signal, which may be somewhat degraded in quality when the demultiplexing is performed, thus limiting the quality of the demultiplexed signal. Concerning the scheme in Fig. 5.14b, the response speed of the SOAs must be higher, as the phase modulation is performed by the high-rate data signal. This also means that pattern dependency is an issue. However, the clock pulses, which are most likely of a good quality (high extinction ratio, OSNR, etc.), determine the standard of the corresponding demultiplexed signal, while reshaping is performed due to the sinusoidal transfer function. Thus, 3R regeneration is performed.
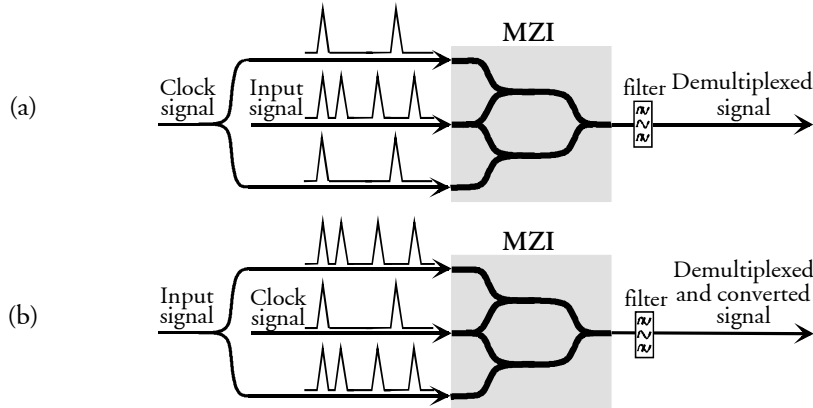
Fig. 5.14: Schematic of two different schemes for all-optical time-division demultiplexing using an MZI. (a) Traditional demultiplexing without wavelength conversion. (b) Simultaneous demultiplexing and wavelength conversion. Note that the differential control scheme is shown without the attenuator and delay-line.

From the above discussion, it is obvious that there exists a trade-off between the two schemes. Although both demultiplexing schemes have demonstrated good results [103,104,105,Pub7], there has not, to the author's knowledge been performed any exhaustive comparison of the two schemes to discern which gives the best performance. However, 80 to 10 Gbit/s demultiplexing has been demonstrated in a conventional MZI with the scheme in Fig. 5.14a [104], while with the scheme in Fig. 5.14b the record rate is limited to 40 to 10 Gbit/s demultiplexing [105,Pub7]. Thus, this seems to indicate that the former scheme, which does not involve wavelength conversion, gives the best high-speed performance, providing the input signal quality is acceptable.

The performance of the scheme shown in Fig. 5.14b for 40 to 10 Gbit/s demultiplexing and wavelength conversion has been assessed experimentally using a set-up similar to the one shown in Fig. 4.13, except that the CW laser has been replaced with a gain-switched DFB laser modulated at 10 GHz. Selection of one of the four 10 Gbit/s data channels to be demultiplexed and synchronisation between the data signal and clock signal is performed by adjustment of an electrical time delay coupled to the RF-input of the gain-switched laser. In Fig. 5.15 (upper) is shown a pulse trace of the 40 Gbit/s input data signal to the all-active MZI. Note that the pulse overlap in the figure is caused by the limited bandwidth of the photodetector (30 GHz); a FWHM pulse width of ~7 ps is employed in the measurements. In Fig. 5.15 (middle) and (lower) are shown two 10 Gbit/s channels that have been demultiplexed by the MZI. Clearly, the demultiplexing has been done successfully; the bit sequences '1011' and '1110' have been selected with a good performance.
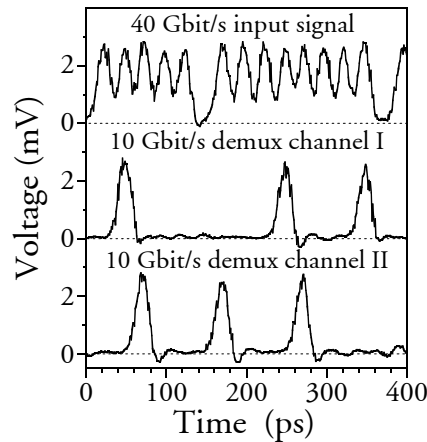
Fig. 5.15: Pulse traces for the 40 Gbit/s input signal (top) and two different demultiplexed and converted 10 Gbit/s channels (middle and bottom). Wavelength conversion has been performed from 1554 to 1547 nm.

In Fig. 5.16 a closer look is taken at the demultiplexing performance, showing the eye-diagram of the wavelength converted and demultiplexed signal (a) and the BER curves for a 10 Gbit/s back-to-back signal and the demultiplexed signal (b). The eye-diagram verifies that an efficient suppression of the other channels has occurred, while the BER curves indicate that the scheme has introduced a 3 dB penalty. It should, however, be noted that this penalty can partly be attributed to the 10 to 40 Gbit/s multiplexing process.
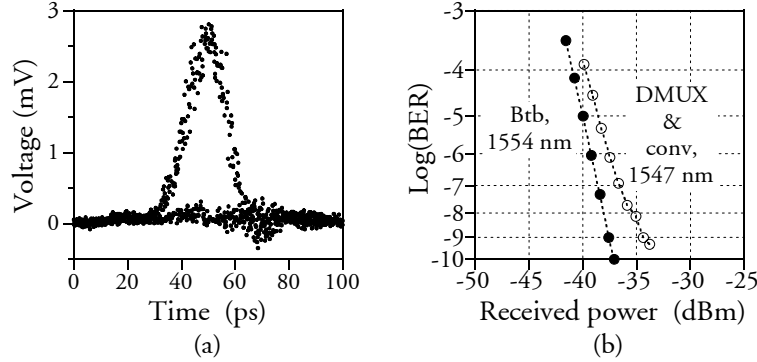
Fig. 5.16: Eye-diagram of the wavelength converted and demultiplexed signal at 10 Gbit/s (a) and BER curves for the back-to-back signal at 10 Gbit/s and the demultiplexed signal (b).

Apart from the MZI, also the MI, TOAD and UNI may be used for demultiplexing. Due to the counter-propagation of the data signal and clock pulses in the TOAD and MI, the operational data rate will, however, be limited for these IWC devices. This is demonstrated experimentally in [106], where the BER performance for 25, 50 and 100 Gbit/s to 12.5 Gbit/s demultiplexing using the UNI and TOAD is compared. For the TOAD, it is seen that as the data pulse period becomes comparable to twice the single-pass transit time in the SOA signal, a BER floor is incurred because a single control pulse interacts with multiple counter-propagating data pulses. This effect, which limits the practical bit rate at which demultiplexing as well as wavelength conversion can be performed, occurs also for the MI, as discussed in Chapter 4.

Finally, it should be mentioned that, apart from the IWC, also SOA-based cross-gain modulation [107] and four-wave mixing [108], as described in Section 4.2, can be used for demultiplexing. However, in these cases signal reshaping does not occur.

5.2.2 All-optical time division multiplexing

In this section, results of simultaneous all-optical 2x10 to 20 Gbit/s multiplexing and wavelength conversion using the 2000 μm long MZI described in Chapter 4 will be given. The experimental set-up is shown in Fig. 5.17: 10 GHz clock pulses

having a pulse width of ~20 ps are generated at 1553 nm and 1560 nm using two gain-switched DFB lasers. The two clock signals are combined and encoded simultaneously at 10 Gbit/s with a 2^{31}-1 PRBS sequence. The obtained data sequences are decorrelated with respect to each other through passive splitting, filtering and delay of one data signal with respect to the other in a standard single-mode fibre. Subsequent interleaving of the two data sequences is performed by passively combining the two sequences after they have been offset one half 10 Gbit/s bit period (i.e., 50 ps) with respect to each other with a variable optical delay. The interleaved data sequences are coupled into port #1 of an all-active MZI, while CW-light at 1545 nm is coupled into port #2. Low input power levels of ~0 dBm for the two data signals and –2.4 dBm for the 1545 nm CW-signal indicate the power-efficiency of the device. At the output, a 20 Gbit/s wavelength converted signal at 1545 nm with –2.0 dBm of power is obtained containing the original data in the two sequences at 1553 and 1560 nm. A filter at the output of port #3 selects the converted signal before detection and BER measurements of the two time-division multiplexed channels separately after demultiplexing to 10 Gbit/s.
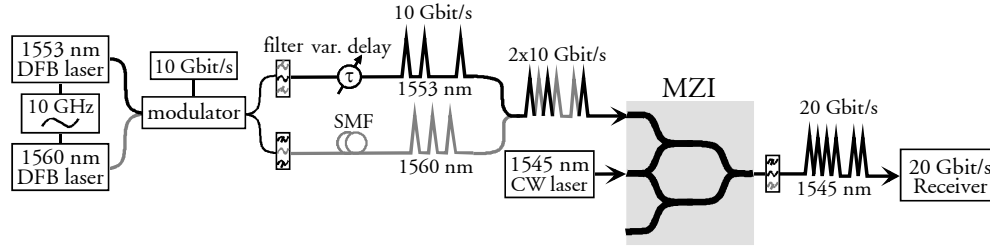
Fig. 5.17: Experimental set-up used for 2x10 Gbit/s to 20 Gbit/s multiplexing.

BER measurements carried out to assess the performance of the 20 Gbit/s time-division multiplexing and wavelength conversion are shown in Fig. 5.18a. The measurements are performed for both of the two 10 Gbit/s channels separately. The open markers indicate results for the 1553 nm channel, while the full markers correspond to the 1560 nm channel. The triangles indicate results for the 10 Gbit/s back-to-back signals and the squares indicate results for the 20 Gbit/s back-to-back signals. The latter are obtained by passive multiplexing of a data signal to 20 Gbit/s followed by 10 Gbit/s BER measurements after demultiplexing. Finally, the circles correspond to results for the 20 Gbit/s multiplexed and wavelength converted signals. As indicated by the BER curves, a small difference in the receiver sensitivity of ~0.3 dB exists for the two 10 Gbit/s data sequences. This may be caused by a combination of slight differences in the pulse width and extinction ratio for the two signals from the gain-switched DFB lasers as well as minor wavelength dependency of the receiver. When comparing results for the 20 and 10 Gbit/s back-to-back signals it is seen that multiplexing to 20 Gbit/s and subsequent demultiplexing is achieved with a pre-amplified penalty of ~0.6 dB. Finally, it is

seen that 20 Gbit/s multiplexing and wavelength conversion in the MZI is obtained with a penalty of ~2.0 dB when comparing with the 20 Gbit/s back-to-back case. This comparison to the 20 Gbit/s back-to-back signal is done in order to ensure a fair assessment of the performance of the MZI at 20 Gbit/s, as it takes the penalty caused by demultiplexing into account in both cases. Note that the difference between the receiver sensitivity for the two channels remains almost unchanged by the wavelength conversion, indicating a low wavelength dependency. In Fig. 5.18b are shown eye-diagrams for the 2x10 Gbit/s input signal to the MZI (upper eye-diagram) and for the 20 Gbit/s wavelength converted output signal at 1545 nm (lower eye-diagram). As seen, a clear and open eye-diagram with a high extinction ratio of ~13 dB is obtained. Furthermore, both channels have been wavelength converted with equally good performance, which was also confirmed through the BER measurements.

(a)   (b)
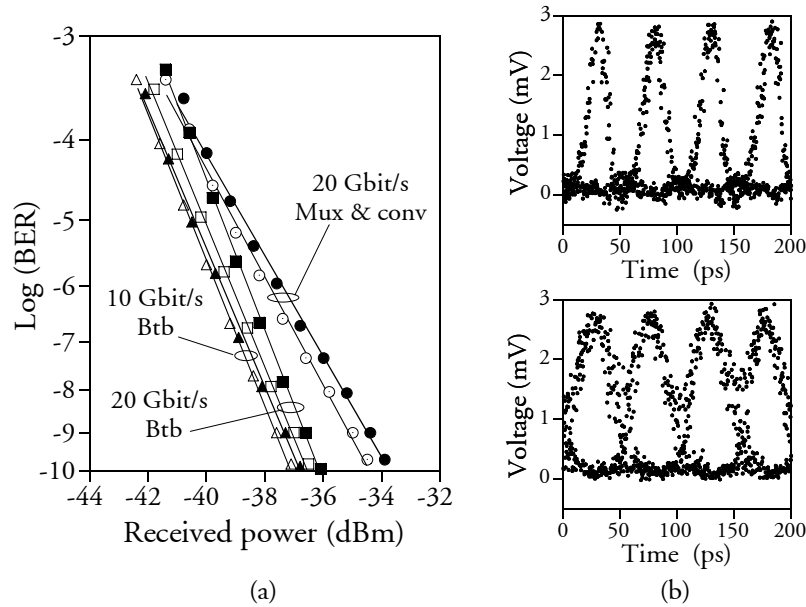
Fig. 5.18: (a) Results of BER measurements- Open markers: 1553 nm channel, full markers: 1560 nm channel. Triangles: 10 Gbit/s back-to-back, squares: 20 Gbit/s back-to-back, circles: signals multiplexed to 20 Gbit/s and wavelength converted. (b) Upper: eye-diagram for 2x10 Gbit/s data signal at MZI input. Lower: 20 Gbit/s converted eye-diagram at MZI output.

The optical spectrum at the output of the MZI is shown in Fig. 5.19. As seen, a high ~38 dB OSNR (in 0.1 nm) was obtained for the 20 Gbit/s multiplexed signal. Finally it should be mentioned that the MZI exhibited very low polarisation dependency both for the data signals and the CW-signal; only minor signal degradation was observed for the worst-case input polarisations.
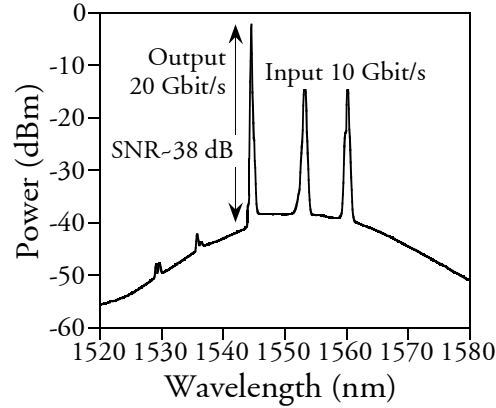
Fig. 5.19: Optical spectrum at the MZI output using a resolution bandwidth of 0.1 nm.

5.3 Summary

In this chapter, the focus has been on applications of the IWC for simple signal processing. In this connection all-optical 2R and 3R regeneration as well as time-division multiplexing and demultiplexing have been investigated.

The principle of 2R and 3R regeneration in an IWC was discussed; it was argued that the sinusoidal transfer function achieved with wavelength conversion enables reshaping, while conversion onto a clock signal recovered from the original data signal enables re-timing. In conjunction with this, methods for optical and electrical clock recovery, which is necessary for 3R regeneration, have been described.

The regenerative capabilities of an all-active MZI have been assessed at 40 Gbit/s using the differential control scheme described in Chapter 4. It was demonstrated that the MZI was capable of preserving the output OSNR above ~37 dB despite an input OSNR that was degraded to as low as ~13 dB by a noise generator. Furthermore, ~2 dB lower OSNR was tolerated for a 2 dB power penalty through insertion of the MZI, clearly demonstrating its capabilities for noise suppression. Furthermore, conversion to a clock signal, which enables 3R regeneration, was demonstrated at 40 Gbit/s. The good performance of the scheme was verified through a high output extinction ratio and a pre-amplified penalty of only ~0.5 dB. Furthermore, conversion to a clock signal enabled preservation of the RZ-format, in contrast to standard conversion to CW-light. Also the regenerative capabilities of the novel conversion scheme described in Chapter 4 were evaluated. Here, excellent regenerative capabilities were achieved at 10 Gbit/s; a ~4 dB lower input power level to the EDFA in the noise generator could be tolerated at a 2 dB penalty when the regenerator was inserted.

Finally, a novel scheme for all-optical regeneration using an IWC was described. The scheme, which is denoted the pass-through scheme, does not require wavelength

conversion, making it more cost-effective and simple than the other techniques described in this chapter. The high IPDR of the scheme (~16 dB at 40 Gbit/s), which is caused by the quasi-digital transfer function, was demonstrated. Furthermore, good noise suppression capabilities were obtained for the pass-though scheme at 40 Gbit/s, quantified by ~2.5 dB lower input power tolerated to the EDFA in the noise generator for a 2 dB penalty.

In addition to regeneration, the performance of the IWC for simultaneous wavelength conversion and time-division (de)multiplexing have also been demonstrated. Both functionalities are of prime importance in future photonic gateways. Using an all-active MZI, 40 to 10 Gbit/s demultiplexing and wavelength conversion was accomplished successfully with a 3 dB penalty. The resulting 10 Gbit/s eye-diagram showed good suppression of the other three channels. Furthermore, 2x10 Gbit/s WDM to 20 Gbit/s time-division multiplexing was performed with a penalty of 2 dB. The small difference in the receiver sensitivity of the two channels in the resulting 20 Gbit/s signal demonstrated the efficiency of the scheme.

Chapter 6

All-optical logic and its applications

In the first generation of all-optical networks, the limited maturity of optics will be the key determining factor for the amount and complexity of all-optical signal processing that is done. Thus, it may be envisaged that the first applications of IWCs in commercial optical networks (providing this component is selected) will be limited to wavelength conversion and regeneration, i.e., the topics of Chapter 4 and 5. The reasons for this are twofold: firstly, these functionalities are the least demanding of the IWC, and secondly, they are key functionalities for implementation of all-optical networks in general. This is also reflected by the discussions given in Chapters 2-5.

When optics reaches a higher level of maturity, making more complex optical signal processing competitive compared to the electronic counterparts, simple functionalities based on all-optical logic may start to find applications in commercial optical networks. This may, for example, be in connection with header recognition and/or -modification in MPLS-based packet switched networks, as described in Chapter 2 for the DAVID network. For example, as will be seen in Section 6.2.1, label swapping, which is a key functionality for the exploitation of MPLS, can be performed in a very simple manner using logic XOR.

In this chapter all-optical logic and its applications in a network perspective will be discussed. In Section 6.1, implementation of all-optical Boolean logic will be described with the focus mainly on IWCs; they can be employed to implement all the Boolean functions NOT, OR, AND and XOR unlike other techniques, which may only be applicable for certain logic functions, as will be seen. Apart from a demonstration of results based on [Pub10,Pub11,Pub23], that have been obtained with an all-active MZI and MI, results of other research groups employing IWCs will also be discussed, along with pros and cons of the different techniques. Finally, in Section 6.2 some applications of optical logic to realise network functionalities in the optical domain will be discussed. Here, results of all-optical MPLS label swapping at 10 Gbit/s based on [Pub20,Pub25] will be presented. Furthermore, three novel ideas that have been filed as patents in collaboration with the Technical University of Denmark will be described, and their potential application in optical networks will be discussed. The novel schemes, which can all be implemented in a single IWC, involve all-optical pattern recognition by bit-wise sampling at multiple wavelengths, optical identification of bit differences in data segments and all-optical bit sequence replacement.

6.1   Boolean logic using IWCs

The simplest of the Boolean functions is the unitary function NOT, which performs a logical inversion of the input data. Thus, simple schemes such as XGM-based wavelength conversion in SOAs (see Fig. 4.1) can be used for implementation of logic NOT. Furthermore, by operating on the negative slope of the IWC's transfer function, as shown in Fig. 4.2 and 4.8, logical inversion can be achieved.

The binary functions such as logic OR, AND and XOR, which involve the injection of two data signals into the IWC, are more challenging to implement than logic NOT, as will be seen in the following. For this reason, accurate experimental validation of a device or technique for all-optical logic must be done through verification of all the combinations in the truth table at the same time, i.e., adjustment of the operating conditions, experimental set-up or partial verification of some combinations in the truth table is not adequate. The motivation for these stringent requirements may be understood by taking the SOA-based IWC as an example: because of the pattern dependency of the SOA, especially at high bit rates, a full performance verification of an IWC-based logic gate requires the employment of true PRBS sequences as the two data signals, and not simply, e.g., one or more clock signals. This is because injection of a clock signal will imply that not all logic combinations of the truth table can be verified at one time. Furthermore, any pattern dependency that the SOA has, especially at high bit rates, may not take effect, meaning that the performance of the gate at the specific rate cannot be fairly evaluated. Thus, if PRBS sequences are not used, the requirements to the device will be relaxed because periodicity can be exploited, meaning that the performance of the device as a logic gate may be overestimated.

6.1.1   Logic OR

Logic OR has not been widely demonstrated optically, perhaps because logic AND and XOR find wider application for simple optical signal processing, as will be discussed in Section 6.2. However, results have been published on both optical logic OR and NOR. In [109] logic NOR was demonstrated in an SOA through exploitation of XGM-based wavelength conversion, while logic OR was demonstrated at 10 Gbit/s using a UNI in [75]. In the following, results on logic OR in an MI, which are based on [Pub10] will be given.

A schematic of the Michelson interferometer and an illustration detailing the principle of operation as an OR gate are shown in Fig. 6.1 together with the OR truth table. As Fig. 6.1a indicates, the two input data streams at the wavelengths $\lambda_{in,1}$ and $\lambda_{in,2}$, respectively, are passively combined and coupled into port #1 of the MI, while CW light at λ_{OR} is coupled into port #2. It should be noted that $\lambda_{in,1}$ and $\lambda_{in,2}$ are different in order to avoid interferometric crosstalk that will degrade the

performance. The power launched into the upper interferometer arm of the MI will depend on the combined power of the two input signals, meaning that the power level for two marks is different than for a mark and a space. As shown in Fig. 6.1b this difference is suppressed by exploiting the sinusoidal transfer function of the interferometric wavelength converter (here shown in dB-scale), as well as gain saturation in the SOA. As seen by comparing with the OR truth table in Fig. 6.1c, the wavelength converted output signal at λ_{OR} will thus correspond to the logical OR of the two input signals. It should be noted that part of the scheme used here to suppress the difference in input power level between two marks and a mark and a space is the same that is exploited for 2R regeneration using an IWC, as discussed in Sections 5.1.1 and 5.1.2.
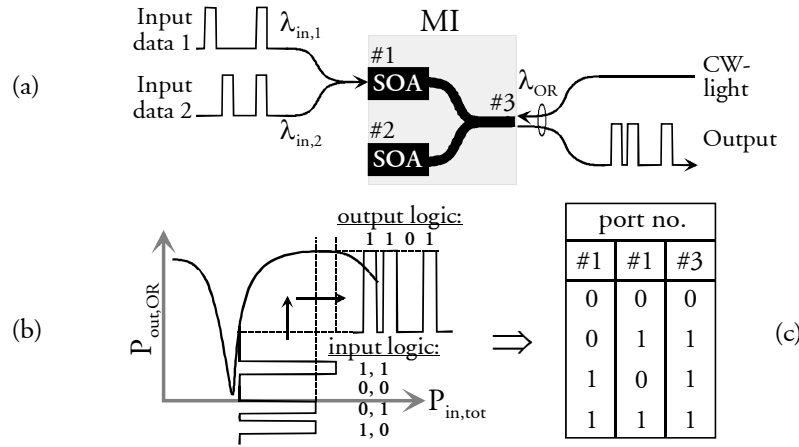
Fig. 6.1: Schematic of an MI used as an OR gate (a). Illustration detailing the principle of operation (IWC transfer function (dB-scale)) (b) and corresponding OR truth table (c).

The performance of the OR gate is assessed at 10 Gbit/s using the experimental set-up shown in Fig. 6.2. In the transmitter, ~26 ps wide pulses are generated at 1546 nm and 1557 nm by two gain-switched DFB lasers, whereupon the signals are externally modulated simultaneously at 10 Gbit/s using a Mach-Zehnder modulator. The data signals are then separated through passive splitting into two arms and subsequent filtering. A variable delay is inserted in the upper arm in order to synchronise the two signals to each other. The 1557 nm data signal in the lower arm is delayed sufficiently compared to the 1546 nm signal (using standard SM fibre) to
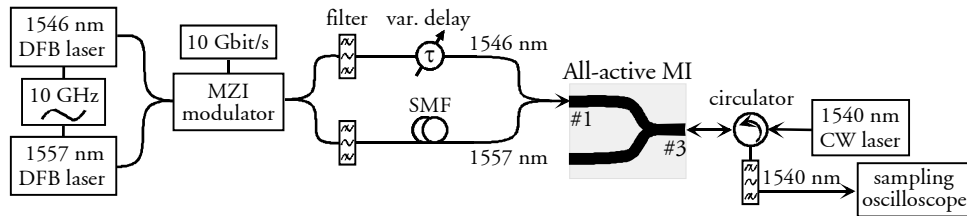
Fig. 6.2: Experimental set-up for verification of logic OR at 10 Gbit/s in a MI.

ensure that the two signal streams are decorrelated with respect to each other before entering the MI at port #1. The CW signal at 1540 nm is injected into the MI at port #3. After cross-phase modulation in the MI, the wavelength converted output signal at 1540 nm is coupled out of port #3, where a filter selects the converted signal before it is observed using a 30 GHz sampling oscilloscope.

In Fig. 6.3a are shown portions of the two input PRBS sequences and the output signal from the MI. As seen in the figure, all of the input signal combinations in the OR truth table in Fig. 6.1c are represented along with the correct output logic, verifying the OR functionality performed at 10 Gbit/s. The good performance of the MI converter as an OR gate is also apparent in Fig. 6.3b, which shows the corresponding OR eye diagram. As indicated, a clear and open eye-diagram is obtained with an extinction ratio of ~12.5 dB. However, it is seen that there exists some pattern dependency; double traces can be seen along the right flanks. The outer trace occurs because the OR signal corresponding to two input marks is a little wider than the OR signal corresponding to an input mark and space, as is also evident from Fig. 6.3a. This is caused by the sinusoidal transfer function of the MI converter, which does not suppress the difference between the two input signal combinations completely. To compensate for this, an operation point is used in which the data signals have been slightly offset with respect to each other, thereby creating the double traces. Finally, it should be noted that the differential scheme, as described in Section 4.4 can also in this case be exploited to improve the high speed performance, if operation at higher bit rates than 10 Gbit/s is desired. Furthermore, concerning the choice of modulation format, it can be mentioned that logic OR works equally well in an MZI or MI with NRZ data signals as well as RZ signals.

(a)   (b)
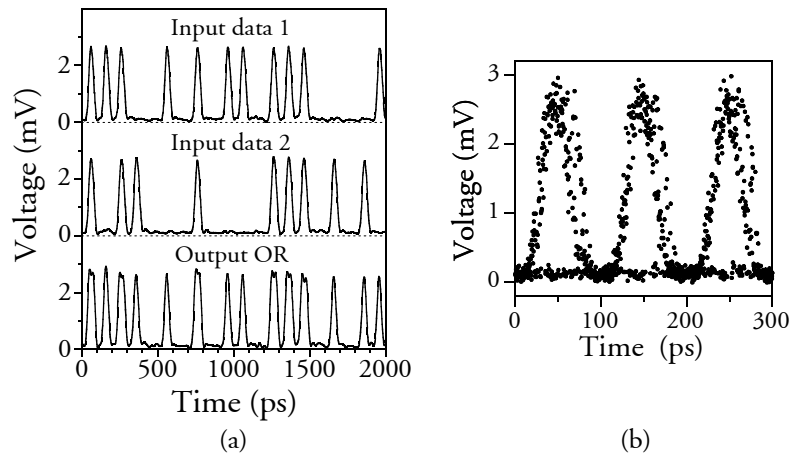
Fig. 6.3: Performance of the MI as a logic OR gate at 10 Gbit/s- (a) Two input PRBS data streams and the resulting output OR signal. (b) Corresponding output OR eye-diagram.

6.1.2 Logic AND

Another important Boolean function is logic AND, which effectively corresponds to the sampling of one signal with another. The principle of logic AND is, e.g., used for optical time division demultiplexing, where the input signals involved are the data signal to be demultiplexed in conjunction with an appropriately chosen lower-rate clock signal, as discussed in Section 5.2.1. When employing the MZI, logic AND can be achieved by coupling the two input signals into port #1 and 3 of the device, respectively, as shown in Fig. 6.4. Thus, if operation is performed on the positive slope of the IWC transfer function (cf., Fig. 4.2b), input data signal 2 (IDS2) will sample input data signal 1 (IDS1), whereby selective switching of the data pulses at λ_{AND} will occur exclusively when IDS1 is a mark. In this way, logic AND is implemented, as seen by comparing with the truth table in Fig. 6.4. It should be noted that logic NAND cannot be implemented using a single IWC; one would assume that operation on the negative flank of the transfer function gives logic NAND, however this is not the case. Instead, a hybrid function, which outputs a mark only when IDS1 is a space and IDS2 is a mark, is achieved (i.e., (**NOT**(IDS1) **AND** IDS2).

port no.		
#1	#3	#4
0	0	0
0	1	0
1	0	0
1	1	1

(a)   (b)
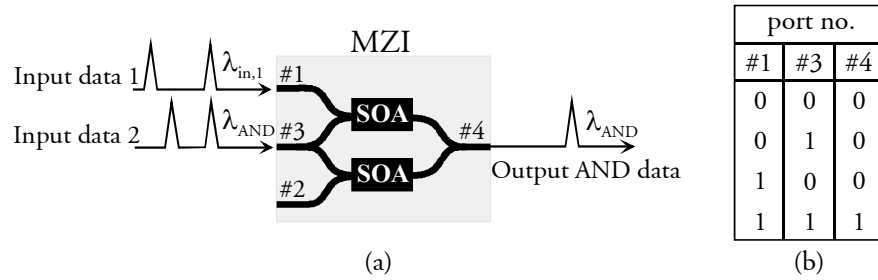
Fig. 6.4: Schematic of an MZI used as an AND gate (a) and corresponding AND truth table (b). Wavelength conversion is performed onto input data signal 2 having the wavelength λ_{AND}.

Logic AND has been verified at 10 Gbit/s with a Michelson interferometer by using the experimental set-up in Fig. 6.2, except the data signal at 1546 nm is coupled into port #3 of the MI instead of CW-light at 1540 nm. In Fig. 6.5a experimentally obtained pulse traces are shown for the two input data signals and corresponding logic AND at the output of the MI. As indicated, all combinations in the truth table in Fig. 6.4a are represented, thus verifying the operation of the MI as an AND gate. The good performance is also evident in Fig. 6.4b, which shows that a clear and open AND eye-diagram is obtained with a very high extinction ratio of ~15 dB. It should be noted that the sparsely represented marks in the eye-diagram are caused by the mark-space ratio of the optical AND signal, which is 1:4 due to the characteristics of the AND truth table.
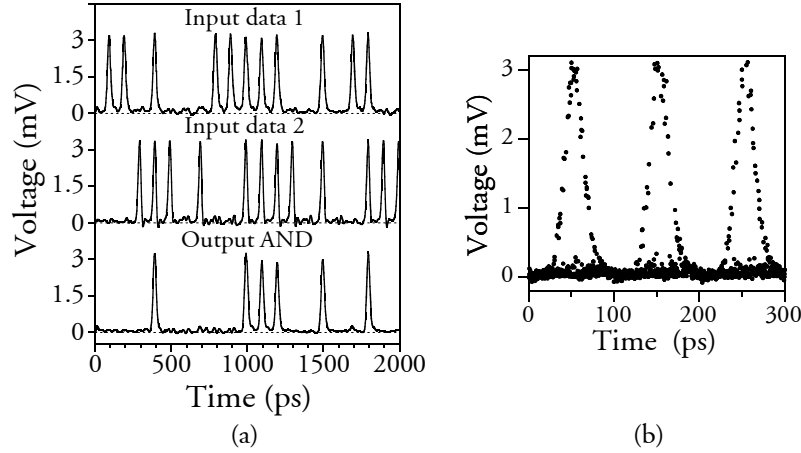
Fig. 6.5: Performance of the MI as a logic AND gate at 10 Gbit/s- (a) Two input PRBS data streams at 1546 nm and 1557 nm and the resulting output AND signal at 1546 nm. (b) Corresponding output AND eye-diagram.

Although, as mentioned previously, the principle of logic AND is analogue to demultiplexing, logic AND is much more challenging to implement for the IWC. This is because, when performing demultiplexing, the pattern periodicity of the clock signal eases the operation, while this is not the case for logic AND as PRBS sequences are employed. Moreover, when performing demultiplexing, often only the selected lower rate channel is of interest, while the degree of suppression of the dropped channels is only of minor concern. Again, this is not the case for logic AND, where the signal quality in all bit slots is of equal importance.

Apart from the results shown above, logic AND has also been demonstrated in an MZI at 20 Gbit/s using two data patterns of a limited length of four bits [110]. Furthermore, the principle of AND in a UNI has been shown in [21] with a 100 GHz clock signal and a 100 Gbit/s data signal as the two input sequences, using the scheme in Fig. 4.5. Finally, it should be noted that four-wave mixing can also be used to implement logic AND by exploiting that effective FWM only occurs when both input signals are marks. Using this scheme, logic AND has been demonstrated at 10 Gbit/s with good results using NRZ PRBS data signals [111].

6.1.3 Logic XOR

Of the Boolean functions mentioned until now, logic exclusive-OR (XOR) may be the most widely applicable for simple optical signal processing. This is because the logic XOR gate is of key importance in decision and comparator circuits as well as for data encryption [112], making all-optical implementation of this device very attractive. Some of the applications of logic XOR, as well as AND, will become apparent in Section 6.2.

A schematic of the MZI and an illustration detailing the principle of operation as an XOR gate are shown in Fig. 6.6 together with the XOR truth table. As Fig. 6.6a indicates, the two input data streams at the wavelengths $\lambda_{in,1}$ and $\lambda_{in,2}$, respectively, are coupled into ports #1 and 2 of the MZI, while CW-light at λ_{XOR} is coupled into port #3. In the MZI the data signals are launched into the two SOAs where they modulate the carrier density and thereby also the refractive index. This causes a phase modulation (ϕ) of the CW-light propagating in the SOAs according to the bit pattern of the input data signals. At the output of the interferometer, the CW-light from the two SOAs interferes either constructively or destructively depending on cosine to the phase difference between the light from the two SOAs ($\cos(\phi_1-\phi_2)$) and is thus controlled by the input data signals. This leads to a wavelength converted output signal at port #4 that corresponds to logic XOR of the two input data signals, as indicated by the truth table shown in Fig. 6.6c.
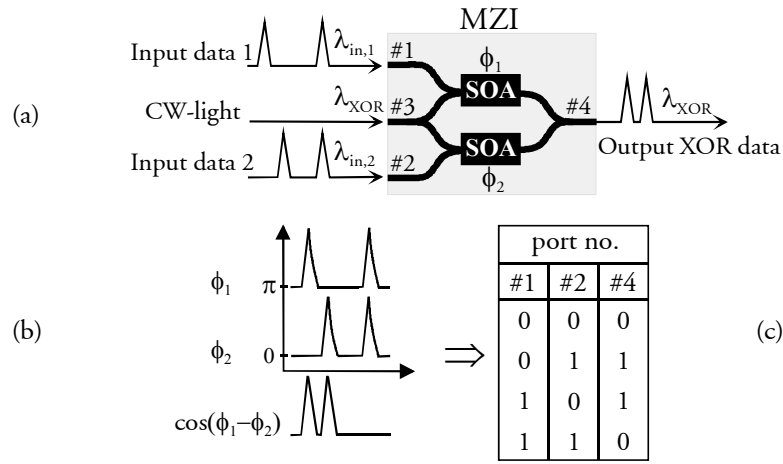
Fig. 6.6: Schematic of MZI used as an XOR gate (a). Illustration detailing the principle of operation (b) and corresponding XOR truth table (c).

The performance of the XOR gate is assessed at 10 Gbit/s using the experimental set-up shown in Fig. 4.24 for the novel conversion scheme as well as the set-up shown in Fig. 6.7. The former is used in order to perform simple BER measurements, while the latter is used to verify that all the combinations in the XOR truth table are represented correctly. As shown in Fig. 6.7, this is achieved in the following way: 10 GHz clock pulses having a width of ~23 ps are generated at 1546 nm using a gain-switched DFB laser, whereupon a LiNbO$_3$ Mach-Zehnder modulator encodes a 10 Gbit/s data signal onto the pulses. The resulting RZ data signal is split equally and coupled into port #1 and 2 of the MZI. The SMF and variable delay shown in the set-up are used to decorrelate and synchronise the data signal with respect to each other, as explained in connection with logic OR. Finally, CW-light at 1554 nm is coupled into port #3, whereupon the input data signals and output XOR signal are observed using a 30 GHz sampling oscilloscope placed at the output of the MZI.
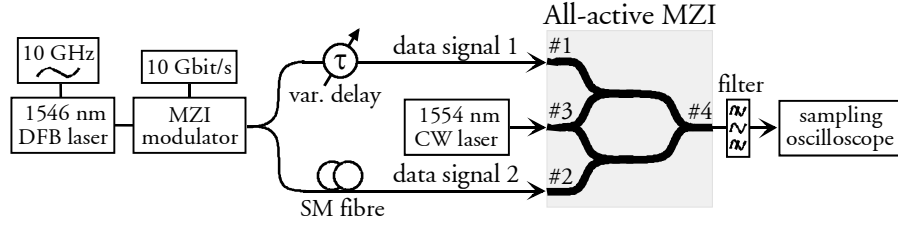
Fig. 6.7: Experimental set-up used to verify the performance of the MZI as a logic XOR gate at 10 Gbit/s. PRBS sequences having a length of 2^{10}-1 are used.

Fig. 6.8a shows portions of the input data sequence, input clock sequence and output signal from the MZI when the set-up in Fig. 4.24 is used. It is seen that injecting a clock signal into one of the interferometer arms instead of a data signal means that the logic XOR operations corresponds to a logical inversion of the input data signal. Thus, the novel conversion scheme, as described in Section 4.6, is based on logic XOR. In Fig. 4.25, BER measurements on the novel scheme were shown at 10 Gbit/s with a negligible preamplified penalty, verifying the good performance. A clock signal is used, as it enables simple BER measurements on the logical inversion of the input data signal using a long bit sequence (2^{11}-1). Of course, BER measurements using a clock signal are not sufficient to verify logic XOR, why the functionality has also been performed on two data sequences at 1546 nm using the set-up in Fig. 6.7. The results are shown in Fig. 6.8b, illustrating pulse traces for the two input data signals and the corresponding XOR signal. As seen, all the combinations in the truth table are verified with good results, indicating the good performance of the MZI as a logic XOR gate.
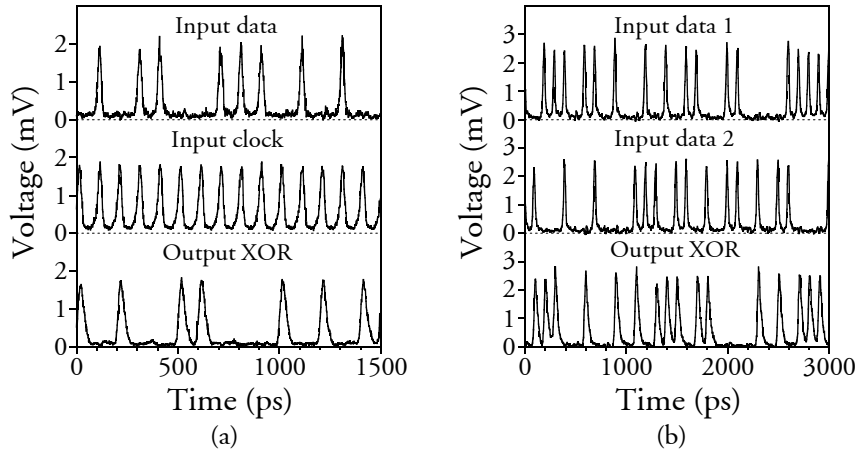
Fig. 6.8: Experimental verification of logic XOR at 10 Gbit/s- (a) Logic XOR of a data- and a clock signal, giving an output corresponding to logic NOT. (b) Logic XOR of two data signals, verifying all combinations in the truth table.

In addition to evaluating the XOR gate at 10 Gbit/s, the performance at 20 Gbit/s has also been investigated using an experimental set-up analogous to the one in Fig. 6.7, except a passive 10 to 20 Gbit/s multiplexer has been added after the modulator to generate a 20 Gbit/s signal.

In Fig. 6.9a are shown the two input data streams and the 20 Gbit/s output XOR signal from MZI. As seen, all of the input signal combinations in the XOR truth table in Fig. 6.6c are represented and the good performance of the XOR gate at this high bit rate is verified. It should be noted, though, that the output XOR pulses are wider than the input pulses due to speed limitations of the MZI. This causes consecutive XOR pulses to overlap partly. This is evident from the XOR eye-diagram shown in Fig. 6.9b, which has a good eye-opening, however with some patterning effects caused by speed limitations. Finally, the optical spectrum at the output of the MZI is illustrated in Fig. 6.9c, which shows that the obtained XOR signal exhibits a high OSNR of ~40 dB (in 0.1 nm bandwidth). The small peaks originating from FWM that can be seen in the spectrum are of no importance, as the signal-to-FWM ratio is in excess of 30 dB before the output filter.

(a)   (b)   (c)
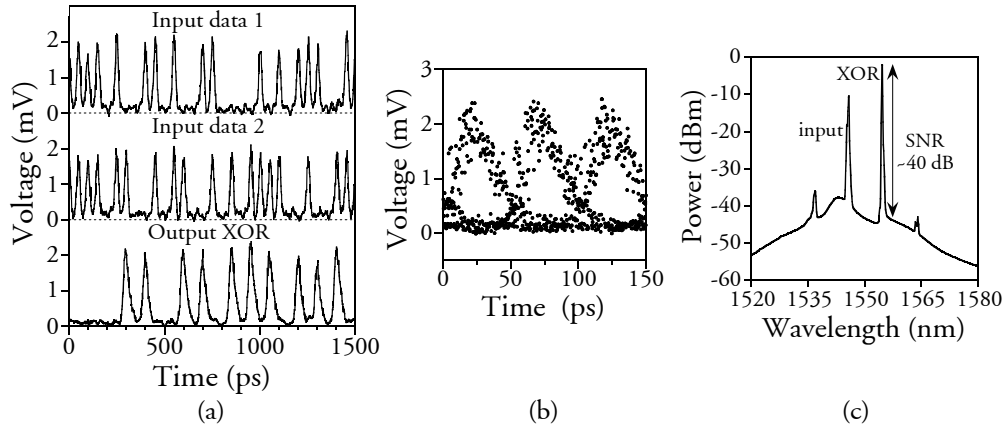
Fig. 6.9: Performance of the MZI as a logic XOR gate at 20 Gbit/s- (a) Two input PRBS data streams at 1546 nm and the resulting XOR signal at 1554 nm. Corresponding XOR eye-diagram (b) and output spectrum in 0.1 nm bandwidth (c).

It should be mentioned that logic XOR has also been verified at 5 Gbit/s in an MZI using the NRZ modulation format [113]. However, the RZ format gives the best performance because, unlike NRZ, transitions occur for multiple successive marks. The consequence of this difference in the two formats can be understood in Fig. 6.10. The figure shows the phase change occurring in the two interferometer arms of an MZI or MI when the data sequences IDS1='…01…' and IDS2='…10…' are injected using the XOR scheme shown in Fig. 6.6a. With the NRZ format, as seen in Fig. 6.10a, fast carrier depletion ensures that the phase change follows the slope of the rising flank of IDS1 (i.e., transition from space to mark). However, for

IDS2, the slow carrier recovery does not follow the slope of the falling flank of IDS2. Due to this discrepancy between the phase change in the two arms, the resulting XOR data sequence '…11…' will be distorted, with a performance degradation to follow. As shown in Fig. 6.10b, this situation does not occur for the RZ format because of the limited duty cycle. This problem with the NRZ format is not as pronounced at low bit rates because the ratio of fall-time to bit slot duration for the data signal is smaller, thus having a negligible effect on the sampling process in the receiver. However, at high bit rates, the speed capabilities of the IWC must be improved, e.g., by employing longer interferometer arms as discussed in Chapter 4, to achieve a good performance. It should also be noted that for the same reason that the NRZ format is problematic for implementation of logic XOR, the performance is also compromised if one of the input signals contains inverted pulses. Thus, if signal processing exploiting logic XOR is employed in an optical network in conjunction with XPM-based wavelength conversion to CW-light, out-of phase operation is undesirable.
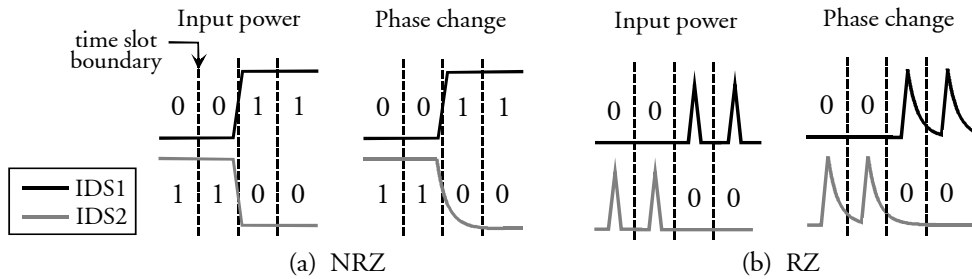
Fig. 6.10: Dependence of logic XOR on the modulation format- the input power and the phase change in the two interferometer arms of an MZI/MI for NRZ (a) and RZ (b) format when a transition from a space to a mark, and vice versa, occurs for IDS1 and IDS2, respectively. IDS1: input data signal 1, IDS2: input data signal 2. Note that any overshoot on the phase for transitions from 0 to 1 is neglected.

Apart from the MZI and MI, also the TOAD and UNI can be used to implement logic XOR. However, in contrast to the MZI and MI, the addition of a clock signal is required if a TOAD or UNI are used. This is because, as discussed in Section 4.2, the nonlinear element in a TOAD (Fig. 4.4) and UNI (Fig. 4.5) consists of only a single SOA, why an additional clock signal must be employed to sample the phase change induced by the two input data signals to the gate. This complicates the practical implementation of the logic gate. By injecting a clock signal into port #3 of the TOAD and data signals into port #1 and 2, respectively, in such a way that the data pulses are interleaved with a $2\Delta\tau$ time shift, 10 Gbit/s logic XOR has been demonstrated in [114] using 16-bit long PRBS sequences. Furthermore, employing a UNI, the principle of logic XOR using a 20 GHz clock signal and 20 Gbit/s data signal as the two input sequences to the gate has been demonstrated in [115] and at 40 GHz with different combinations of a 40 GHz clock signal and no signal as the two inputs to the gate [22].

6.2 Applications of all-optical logic in a network perspective

In the following, four novel schemes for application of all-optical logic in a network perspective will be described. The first scheme has been verified experimentally with the results based on [Pub20,Pub25], while the latter three schemes have been filed as patents, but have not yet been verified experimentally.

One very important criterion that must be fulfilled in order to ensure that optical logic gates exhibit a good performance in a network is synchronisation between the two input data signals, which must be obtained rather precisely. It must be stressed that the requirement of synchronisation is not particular to optical logic, but rather a general requirement for interaction between multiple modulated signals; synchronisation is, e.g., also needed for 3R regeneration as well as time-division demultiplexing, as discussed in Chapter 5.

In a practical network, two different scenarios may be envisaged for the application of optical logic gates, wherein the signal processing required to enable synchronisation differ. In Fig. 6.11a, a data sequence, which is external to the system block containing the optical logic gate, is to be processed logically with a data signal generated internally in the system block. Thus, bit synchronisation between the two data signals requires the internal sequence to be generated in synchronisation with the external sequence. To enable this, clock and phase recovery of the external data signal as well as sequence delineation must be performed. The latter involves recognition of a timing reference in the external signal that indicates the start of the sequence to be logically processed. The conventional approach is to use a code word that is found electronically [116,117]. Alternatively, a reference pulse that is positioned, e.g., at a packet time slot boundary, isolated optically using a logic AND gate and subsequently detected using a photodetector may be employed, as proposed in [118]. Based on the clock, phase and delineation information, the internal sequence can be generated at the correct time, providing phase drift is prevented through appropriate temperature control in the system block. It should be noted that the delay line inserted in the path of the external data signal is used to allow for processing time associated with the clock recovery, delineation, etc.

In the second scenario, as shown in Fig. 6.11b, two data sequences external to the system block are to be processed logically. In this case, clock recovery and delineation of both sequences must be performed. Furthermore, the sequences must be synchronised with respect to each other through appropriately dimensioned bit synchronization block(s). This functionality is analogous to the wander and jitter compensators described in Section 2.2.2 that are used to enable synchronisation to the local clock of the core OPR in the DAVID network. It should be noted, however, that for application with optical logic gates, a much more precise synchronisation at bit level is necessary. This may mean that fibre delay-line based synchronisers may have to be supplemented with very fine synchronisation units, for example based on

a tuneable wavelength converter and highly dispersive fibre that allow very fine wavelength-dependent tuning of the delay [119]. However, due to the complexity of this scheme, it is doubtful whether the scenario in Fig. 6.11b is of interest for practical systems. Fortunately, the scenario in Fig. 6.11a finds much wider application, as will be seen in the following.
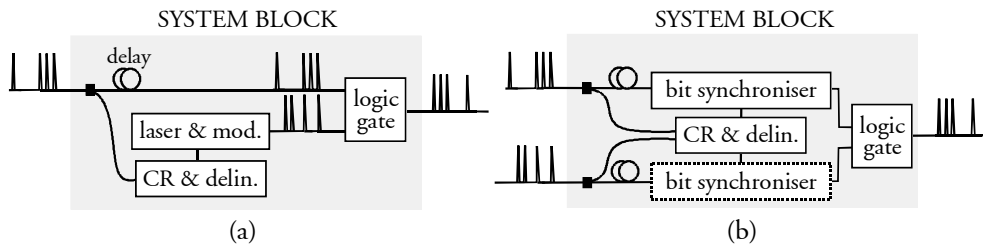
Fig. 6.11: Two different scenarios for application of optical logic gates. CR: clock recovery, delin.: delineation.

6.2.1   All-optical MPLS label swapping

As described in Chapter 2, the DAVID core network relies on optical MPLS to enable fast packet forwarding and flexibility. In order to employ optical MPLS an efficient scheme for all-optical label swapping is required in the optical packet routers (i.e., LSRs). As shown in Fig. 2.7, this is because the label on an incoming packet is replaced with a new value in the packet router as it is forwarded to the appropriate outlet; thus, the forwarding mechanism is based on label swapping. Different methods for all-optical label swapping/header rewriting have been proposed within the last few years. The most straightforward method, which was employed in the KEOPS project [117], is to erase the old header, i.e., using an SOA gate, whereupon a new header, generated through modulation of a laser at the payload wavelength, is added in front of the payload. Although this method seems advantageous due to its simplicity, it has some disadvantages. Firstly, due to the reset time lag of the SOA gates, a guard band must be placed between the header and payload. Furthermore, in the KEOPS switch architecture, the header is erased at the switch input and rewritten at the output. Due to path length variations within the switch node, the new header cannot be positioned precisely with respect to the payload. This must be compensated for by an additional increase in the size of the guard band between the header and payload, which reduces the degree of bandwidth utilisation. Secondly, it is very difficult to ensure that the new header is generated at exactly the same wavelength as the payload- any deviation is problematic if dense WDM is employed. It should be noted, however, that in the KEOPS switch, wavelength conversion is performed at the output, why this may not be a problem in practice. Thirdly, the header information must be stored electronically during the rewriting and packet forwarding process, which to some extent complicates switch management. In order to circumvent one or more of the disadvantages described

above, some alternative schemes for header erasure/rewriting and label swapping have been proposed. In [120] a 2.5 Gbit/s subcarrier multiplexed header is erased using a Fabry-Perot notch filter and subsequently rewritten using an MZ-modulator, while in both [121] and [122], simultaneous header erasure/rewriting and wavelength conversion are demonstrated. In [121] header erasure/rewriting is performed using a two-stage method that employs SOA-based cross-gain modulation followed by cross-phase modulation, while in [122] header replacement is done at 2.5 Gbit/s in a single step using XPM in a fibre-based wavelength converter. In all cases a very special packet format is required; the schemes in [120,121], as well as [123], employ a subcarrier multiplexed header, while in [122] the peak power in the header is required to be ~10 dB less than in the payload. This may prove to be problematic for the practical implementation of the schemes: employment of a subcarrier multiplexed header requires worldwide standardisation, which, to the author's knowledge is not forthcoming at this time. Concerning [122], suppression of the old header is enabled through exploitation of the IWC's sinusoidal transfer function (as in Fig. 4.2b), why efficient suppression is only achieved through a relatively low power level in the header. Again, this requires standardisation and, furthermore, makes the scheme problematic at higher bit rates, where the energy per bit in the header may be too low.

In Fig. 6.12 is shown an alternative scheme for modification of header bits, or label swapping, which employs the interferometric XOR gate as the central element to change selected bits from marks to spaces and vice versa. Label swapping is achieved in the following way: at the packet switch input, a fraction of the signal power in incoming packets is tapped off to the switch management to perform header clock recovery, packet delineation, label reading, etc., -all necessary for any header modifications. Using this information, the changes needed in the existing label to perform the label swapping are found and, at the appropriate time, modulated onto CW-light at a fixed internal wavelength λ_{int}. The optical swapping sequence is coupled into one of the interferometer arms (here, port #2), while the input packet at λ_{in} is coupled into the other. Furthermore, CW-light at the desired output wavelength, λ_{out}, is coupled into port #3. As described in Section 6.1.3, the output packet at λ_{out} will correspond to the logic XOR of the input packet and the swapping sequence. So, a space in the swapping sequence will leave the input data bit unchanged at the output, while a mark will alter the bit in the output packet with respect to the input packet.

Thus, the novel scheme allows combined label swapping/header rewriting and wavelength conversion to be performed on data packets employing a conventional NRZ or RZ packet format and does not require storage of the complete header, but only the fraction that is to be modified. Furthermore, since no header replacement is done, a guard band between the header and payload is not necessary for this scheme, why more efficient use of bandwidth is possible. Also synchronisation between the

label swapping sequence and input data packet should be feasible with only marginal complexity increase; taking the DAVID OPR as an example, label swapping could be implemented in the input or output wavelength converters in Fig. 2.4, e.g., in conjunction with 3R regeneration, which already requires exact phase and clock recovery. Finally, it should be noted that the scheme places no restrictions on the bit-rate of the payload data, which may be variable and is only limited by the speed capabilities of the IWC.
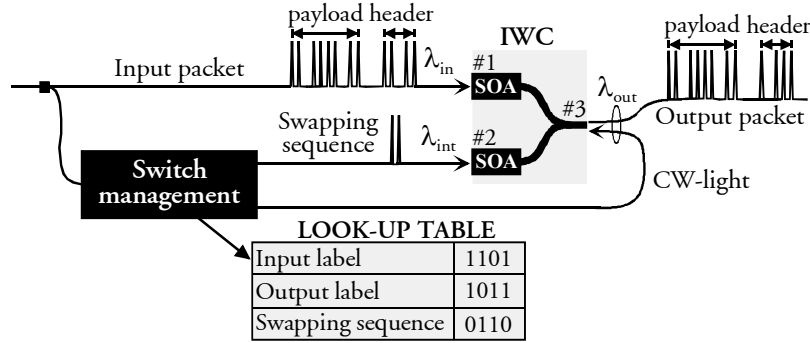
Fig. 6.12: Practical implementation of the label swapping scheme in an MPLS-based switch node. Here, a Michelson interferometer is used as an example.

Fig. 6.13 shows the experimental set-up used to investigate the label swapping scheme at 10 Gbit/s by BER measurements on the output packet sequence. In order to avoid the use of two pattern generators for the input packet sequence and the label swapping sequence, the following scheme has been used: 10 GHz clock pulses having a pulse width of ~30 ps are generated through modulation of CW-light at 1538 nm using an
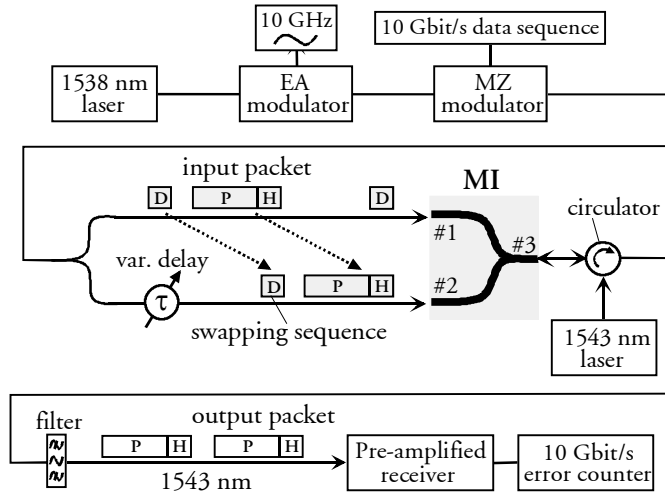
Fig. 6.13: Experimental set-up for verification of the label swapping scheme at 10 Gbit/s using an all-active MI as an XOR gate.

EA-modulator. A 10 Gbit/s data sequence consisting of the input packet sequence followed by a label swapping sequence (D) is encoded onto the RZ pulses using a LiNbO$_3$ modulator. As shown in Fig. 6.13, the signal is passively split into two arms. By subsequently delaying one part appropriately with respect to the other, the swapping sequence will be injected into one arm of the all-active Michelson interferometer in synchronisation with the packet header injected into the other arm. In addition, CW-light at 1543 nm is coupled into the MI at port #3, from where the wavelength converted output packet sequence also exits after logic XOR has been performed. Finally, a filter selects the output packet sequence before detection and error counting.

Fig. 6.14a shows the measured pulse traces of input and output packet sequences. To enable illustration of all bits in the packet sequence clearly at the same time the packet has a limited length of 123 bits with a 23-bit header, a 7-bit guard band and a 93-bit payload. As indicated, the input and output packet sequences are identical except for the bits in the header that have been altered by the label swapping scheme. Note that the variation in the height of the marks is primarily due to the limited resolution of the oscilloscope used and not actual power fluctuations. This is verified in Fig. 6.14b, which shows an enlarged version of the input header and partial payload along with the corresponding label swapping sequence and output header. Four marks in the label swapping sequence change the corresponding bits in the input packet sequence. As the output packet trace indicates, this has been performed successfully; an input mark is changed to an output space and vice versa. Note that, as mentioned previously, a guard band between the header and payload is not necessary for this scheme. Here, it is inserted only to visually separate header and payload.
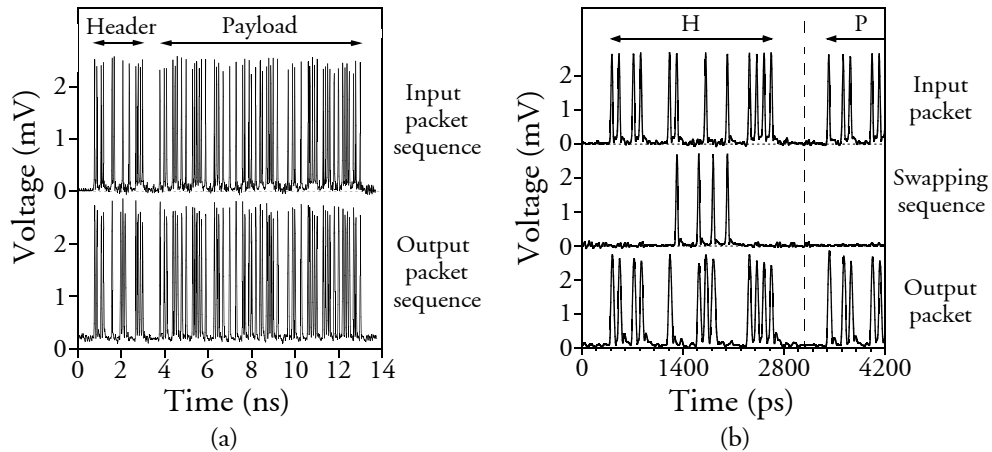
Fig. 6.14: (a) Measured input and output packet sequences. (b) Scheme verification-enlargement of input and output header (H) and partial payload (P) as well as swapping sequence.

To fully verify the performance of the label swapping scheme, bit error rate measurements have been performed on the input and output packet sequences shown in Fig. 6.14a by programming the error detector with the two sequences. In both cases, error counting was done on both the header and payload simultaneously. The results are shown in Fig. 6.16a, indicating that the label swapping is performed with a negligible pre-amplified receiver penalty of 0.4 dB. The clear and open output packet eye diagram shown in Fig. 6.15b demonstrates that the header bits have been altered without signal quality degradation. Furthermore, the high output signal extinction ratio of ~13 dB that is obtained indicates the good performance of the scheme.
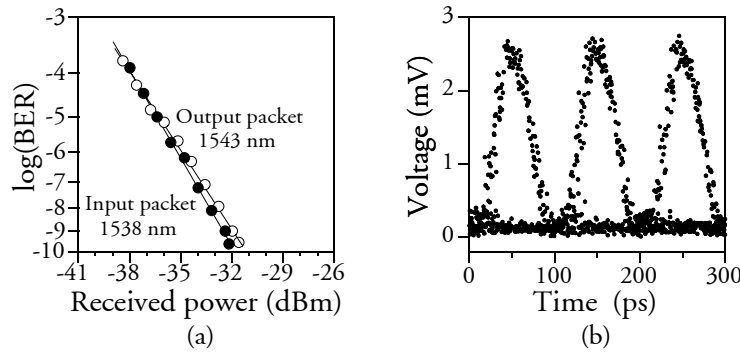
Fig. 6.15: (a) 10 Gbit/s BER measurements on the input and output packet sequences. (b) Eye-diagram for the output packet sequence.

6.2.2 All-optical pattern recognition by bitwise sampling at multiple wavelengths

One of the key processing functionalities in packet switched networks in general is pattern recognition. As described in Section 2.2.3, this is required for MPLS label (address) recognition, which enables packet forwarding in OPRs based on a forwarding table. In [124] pattern recognition has been demonstrated all-optically at 10 Gbit/s using a NOLM-based XOR gate as a comparator, while in [125], it has been performed at 100 Gbit/s using an FWM-based AND gate. However, errors may occur if AND is used, as the logic function, unlike XOR, is unbalanced. This is explained in Fig. 6.16. Assume a pattern containing the sequence 1011 is expected. Thus, a comparator sequence that is the inverse of this sequence, namely 0100, is generated in the case of logic AND, with the result 0000 at the output of the AND gate. Successful recognition of the pattern can be determined through the absence of a power surge to a low-bandwidth photo detector. In Fig. 6.16b (upper) is shown the situation when an incorrect pattern (1001) is input to the AND gate. As indicated, the output of the AND gate is unaltered, meaning this error will not be registered. If XOR is employed, as shown in Fig. 6.16 (lower), the comparator sequence corresponds to the input pattern. In this case, the erroneous data sequence will be detected by the generation of

a pulse at the output of the XOR gate, as shown in Fig. 6.16b (lower). This unambiguity makes the XOR gate superior to the AND gate as a comparator.
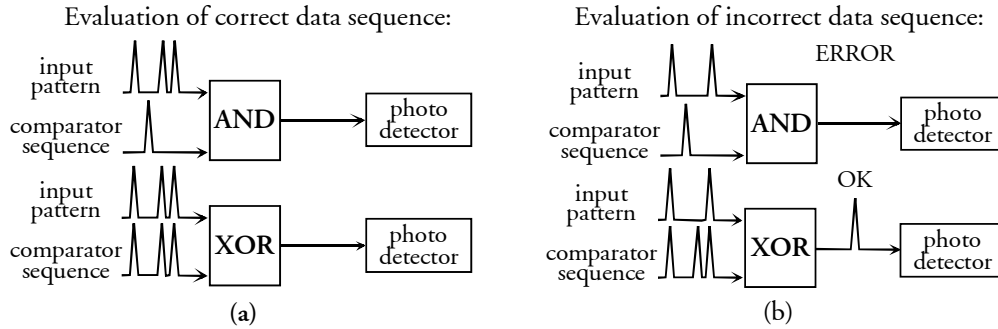
Fig. 6.16: Comparison of pattern recognition when employing logic AND and logic XOR. (a) The correct pattern is injected. (b) An incorrect pattern is injected, thus resulting in erroneous evaluation if an AND gate is used.

Although conventional comparison of an input pattern with a known sequence using a comparator is ideal for some applications as will be seen in Section 6.2.3, it is, however, not optimal for label/address recognition. This is because the content of the label is unknown beforehand- it takes on a value within the set of indices (i.e., set of possible addresses) in the forwarding table (see Section 2.2.3). Straightforward recognition of an unknown label/address employing logic XOR (or AND) as an optical comparator as shown in Fig. 6.16 and [124,125] requires the use of an optical logic gate for each of the possible values of the input label. Hereby the correct label is found as input to the logic gate where the output remains low. Unfortunately, this requires a very large number of logic gates and photodetectors (up to 2^n if n is the number of bits in the label/address), which makes the scheme unscalable, costly and complex to implement optically. As an alternative is conventional electronic label recognition, which, however, becomes problematic at high bit rates as discussed previously. In Fig. 6.17 is shown an optical scheme for pattern recognition that can discern between all possible input patterns unambiguously, scales well with pattern size and operates at high bit rates, thus solving the problems discussed above. The scheme, on which [Pat2] is based, relies on optical bitwise sampling of the input pattern at λ_{data} with control pulses at multiple wavelengths using a logic AND gate (here, an MZI). The scheme may be considered a hybrid of the following: in [105] a technique for OTDM to WDM conversion (i.e., demultiplexing) was demonstrated. Here, a 40 Gbit/s data signal was demultiplexed and wavelength converted to 4x10 Gbit/s WDM channels using the scheme in Fig. 5.14b with four time-shifted 10 GHz clock signals at different wavelengths input to the common arm of the MZI. Moreover, in [126] single-bit recognition was demonstrated using a TOAD-based logic AND gate by injection of one pulse into the TOAD at port #3 (see Fig. 4.4) and the data pattern into port #1.

By combining the two schemes described above as shown in Fig. 6.17, the input pattern is converted from serial to parallel in one step, thus allowing simple unambiguous recognition in the following manner: time-shifted control pulses (here, at λ_1-λ_3) are generated in synchronisation with the label in an optical packet[38]. Each control pulse samples the bit that it is synchronised to, whereby a pulse is generated at the output of the IWC when, and only when, the data bit is a mark if in-phase operation is used. For out-of-phase operation, a pulse will occur when the data bit is a space. A demultiplexer placed at the IWC output separates the signals at the control wavelengths, whereupon each single data bit may be processed independently by low-bandwidth photodetectors. Thus employing IP operation, a power surge will occur when the data bit in question is a mark, while the current from the photodetector will remain low when the bit is a space.
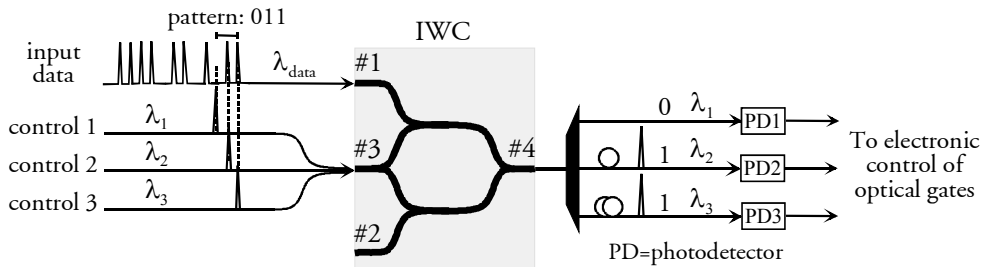
Fig. 6.17: Illustration of scheme for all-optical pattern recognition by bitwise sampling at multiple wavelengths using an IWC-based AND gate (here, an MZI).

The advantages of the scheme are as follows: a single IWC may (in principle) be used to recognise any pattern consisting of *n* bits. Moreover, because the data pattern is converted from serial to parallel, the bandwidth of the subsequent electronic detection and control circuitry is decoupled from the data rate; cheap, low-speed electronics may be used to process a high bit rate optical data signal. As shown in Fig. 6.17, the number of required control pulses, and therefore lasers as well as photodetectors, scales linearly with *n*. It should, however, be noted that an upper limit is set on the pattern length by the IWC itself. Injecting a very large number of control signals into the IWC will cause gain saturation in the SOAs, thus compromising the performance. Although the upper limit to *n* has not been investigated, it must be quite high, as increasing the number control signals causes a linear increase in the base level power, which may be assumed to be significantly lower than the control pulse peak power. If the pattern is too long to recognise using a single IWC, the task may be parallelised further by employing multiple IWCs, each recognising a fraction of the pattern.

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[38] Synchronisation requires prior clock recovery and packet delineation, as discussed in connection with Fig. 6.11.

Moreover, it should be noted that by modifying the scheme shown in Fig. 6.17 slightly, it is possible to reduce the required number of lasers and/or photodetectors. The number of lasers and detectors may be reduced simultaneously by allowing each laser to generate multiple control pulses. Pulses from different sources are interleaved in time so that the neighbouring control pulses still have different wavelengths. This enables fewer photodetectors to be used since each now detects multiple bits instead of just one. However, this component count reduction comes at the expense of a faster response time for each individual photodetector, which increases the cost per detector. Thus, a trade-off exists that must be taken into account.

In another implementation, the input signal configuration is identical to Fig. 6.17, i.e., each laser generates a single control pulse. However, after demultiplexing, bits exiting the IWC are directed to a single photodetector through optical paths (FDLs) having an incremental time difference that is greater than the response time of the detector but shorter than a packet duration. This scheme reduces the number of required detectors considerably at the expense of additional processing time, which means that it is only advantageous in practice if the packet duration is appropriately long.

It may be envisaged in a practical switch block that the scheme in Fig. 6.17 is used to enable subsequent packet forwarding to the correct output. Thus, as illustrated in Fig. 6.18, the low-bandwidth electrical signal at the output of the photodetectors could, for example, be used to control an array of optical gates. As shown schematically in Fig. 6.18, optical label recognition using the scheme in Fig. 6.17 is done on a fraction of the power in the incoming packet. The remainder of the packet is directed towards the optical gate array that performs space-switching. An appropriately chosen optical delay is inserted in order to take the label processing time
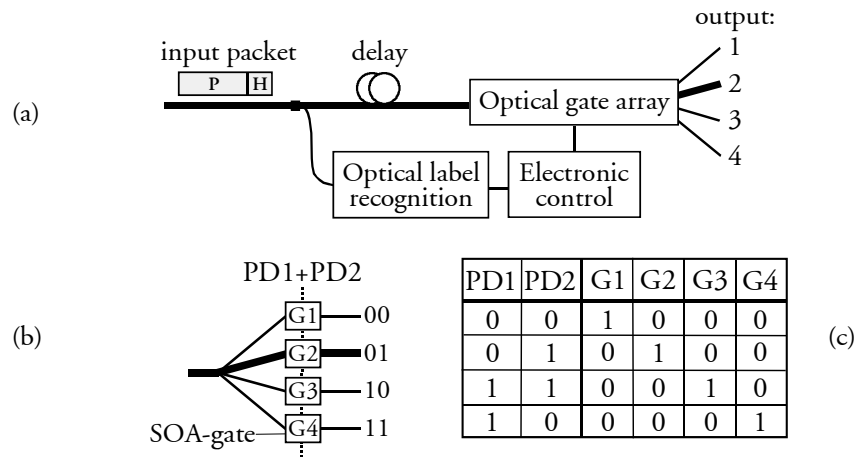
Fig. 6.18: (a) Schematic showing practical implementation of packet forwarding to output 2 based on optical label recognition. Optical gate array configuration (b) and look-up table used for control (c). PD: photodetector, G: gate.

into account. Based on the output signals from the photodetectors in the label recognition block, corresponding to the bits in the label, a simple, low frequency electronic control circuitry reconfigures the optical (SOA) gates appropriately, thus setting up the correct path to the destination output.

In Fig. 6.18b is shown a gate array configuration for self-routing of a packet carrying a 2-bit label, where the terms PD1 and PD2 refer to the two photodetectors required in the label recognition block. In the array, space switching is performed through control of a total of 2^n (=4) gates, which the packet accesses through a splitter. The packet is to be forwarded to output 2 corresponding to the label '01', why a path should be set up as shown by the bold line. The output signals from the two photodetectors are used as entries in a look-up table, which designates which gates (G1-G4) to open ('1') and keep closed ('0'). This table can be made with electronic logic gates in a standard low-speed FPGA[39]. Thus, cost-effective commercial electronics may be used to control the optical packet forwarding functionality, while limiting the required number of optical gates.

6.2.3   Optical identification of bit differences in data segments

As discussed in Section 6.2.2, recognition of an unknown pattern is an important functionality in optical packet-switched networks. However, scenarios that require comparison of an unknown sequence with a known and expected sequence can also be envisaged. This functionality is, e.g., important in connection with forward error correction (FEC), which is a method for dealing with bit errors. By including enough redundant information (i.e., overhead) along with the transmitted data, the receiver is able to deduce either what the transmitted character must have been (error-correcting codes) or simply that an error has occurred (error-detecting codes) [127]. The added overhead may be a check sequence, which is transmitted with the data. Error detection is thus enabled by comparison of an actual transmitted check sequence with the expected sequence by using an XOR gate-based comparator (c.f., Fig. 6.16). In the medium term, it may be envisaged that the payload of an optical packet is encoded at a higher bit rate than the header. Thus, a high bandwidth utilisation and transparent payload switching may be combined with cost-effective electronic header processing. In this connection, electronic header error detection is natural to perform. However, an error-free header does not necessarily imply that the payload is error-free. Firstly, in this scenario the header is terminated at each switch node, why only signal deterioration on a link basis will be detected. This is not the case for the payload, which is switched transparently. Moreover, the high bit rate payload is significantly more sensitive to degradation caused by nonlinear effects in the transmission fibre, pulse broadening due to dispersion, polarisation-mode dispersion, etc., due to the limited bit period and higher peak powers. Thus, it is desirable also to include a payload check sequence, which may be monitored optically, on the fly, for potential bit errors.

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[39] FPGA: Field Programmable Gate Array

So, an optical scheme for comparison of a segment of an input data signal (i.e., the payload check sequence) with a known sequence (i.e., the correct check sequence) is required. This scheme should enable correct evaluation of the data segment, while keeping the output low outside the window of the data segment. If the latter is not fulfilled, the following low-speed (electronic) processing block will need to be informed when to disregard the output from the photodetector, which complicates the control. For this purpose, logic XOR is not ideal, as the XOR gate will generate pulses outside the window of the data segment whenever the input data signal is a mark. Logic AND fulfils the criterion, as the function prevents pulses from being generated outside the window, simply by limiting the comparator sequence to the data segment window. However, as discussed in Section 6.2.2, logic AND cannot detect all errors, as it is unbalanced. Thus, a trade-off occurs between logic AND and XOR for this specific application. Alternatively, the check sequence may be extracted from the remainder of the data sequence using an optical SOA gate, whereupon an optical XOR gate may be used as comparator. However, this requires insertion of guard bands having a duration of some ns in order to compensate for the settling time of the SOA gate, which reduces the bandwidth utilisation and increases the component count.

In Fig. 6.19 is shown a novel scheme, on which [Pat3] is based, which avoids the use of an SOA gate and maintains the advantages of logic AND and XOR, while avoiding the disadvantages. The scheme combines logic AND and XOR in a single IWC in the following manner: using the XOR-mode (see Fig. 6.6), the input data signal at λ_{data} containing the data segment is coupled into the IWC in synchronisation with the comparator sequence at λ_{comp}. Moreover, instead of CW-light, a square control signal is coupled into the common arm at λ_{ctrl}. The transitions of the control signal are timed to correspond to the window of the data segment, whereby the signal effectively performs a gating function. In this way, a comparison is performed between the bits of the data signal and the bits of the comparator sequence over a window defined by the control signal, which can have a duration shorter than the duration of the data and comparator signals. This corresponds to performing the following combined logic operation in a single step:

$$\text{(Input Data } \textbf{XOR} \text{ Comparator Sequence)} \textbf{ AND} \text{ Control Signal} \qquad (6.1)$$

In this manner, a pulse will be generated at the IWC output whenever the data segment- and comparator bits differ. These discrepancies are registered as power surge(s) at the output of a low-speed photodetector.
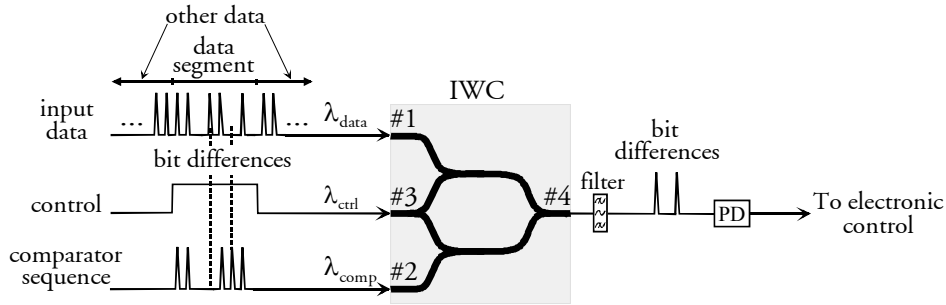
Fig. 6.19: Illustration of scheme for all-optical identification of bit differences in an IWC (here, an MZI). PD: photodetector.

Returning to the application for payload error detection, the scheme may be used to monitor whether the payload check sequence has been distorted. Any modifications will translate into pulses at the output of the IWC. It should be noted that if a low-speed detector and control circuitry is used with the scheme as shown in Fig. 6.19, individual bit errors cannot be resolved; it is only possible to detect whether or not the sequence is error-free. Unless error correction is desired, it is, however, sufficient to know that an error has occurred- no additional advantages are gained through individual error resolution with low bandwidth photodetectors.

Although implementing the scheme with an MZI or MI allows the control signal to have an NRZ-format, this is not possible if the UNI or TOAD is used. However, the high level in the control signal may just as well be replaced by RZ pulses synchronised in time to the other input signals, thus allowing implementation with the TOAD or UNI. Additionally, this will also allow individual resolution of the output pulses from the IWC, if desired; the scheme in Section 6.2.2 may be exploited by using a multi-wavelength pulsed control signal, allowing individual detection of potential errors.

6.2.4 All-optical bit sequence replacement

In practical networks, errors detected in data packets must have management-related consequences, as signal distortion is often caused by equipment malfunction that must be corrected. Thus, the following steps may be taken in connection with error detection:

1. A data packet is transmitted in an optical communication system. The packet contains a check sequence in the payload (or header), which is processed optically in each node in order to evaluate whether an error or signal degradation has occurred during transmission. This may for example be done using the scheme in Fig. 6.19.

2. Error(s) are detected in a packet.

3. Subsequent switch nodes on the packet's path from source to destination are notified that the packet may be corrupted, and where the fault was registered.

This is done by changing the check sequence to a coded message, which may contain information about the identity of the node wherein the fault was registered, as well as any other information of relevance for fault localisation.

4. Network management is notified and steps are taken towards locating the origin of the fault.

5. The source is notified of the error and the packet is retransmitted, depending on QoS requirements and data type.

Thus, the task is to alter the check sequence optically after the error has been detected. This should be done on the fly without electrical termination and without altering any bits in the rest of the packet.

In Fig. 6.20 is illustrated a scheme which serves this purpose and can be implemented in a single IWC. The idea behind the scheme, on which [Pat4] is based, is as follows: the erroneous optical data packet at the wavelength λ_{data} is combined with a deleting sequence at another wavelength, λ_{del}, and the signals are coupled into an interferometer. Note that in the figure the modulation formats RZ and NRZ are used to discern between the data modulated and control parts of the signals- the scheme works on both formats. The deleting sequence, which functions as a gating sequence, is generated so that it is high (logical one) exactly when the check sequence in the data packet occurs, and low (logical zero) at all other times. Additionally, an encoding sequence at λ_{code} is coupled into the interferometer. This sequence consists of a coded message that is synchronised to the check sequence in the data packet and a high level (logical one) at all other times. The result at the output of the interferometer is the original data packet, except that the check sequence is replaced by the coded message. When this message is processed (read) in the subsequent nodes, the occurrence of a fault in the original check sequence will be known. As the three signals are coupled into the interferometer, the data packet with
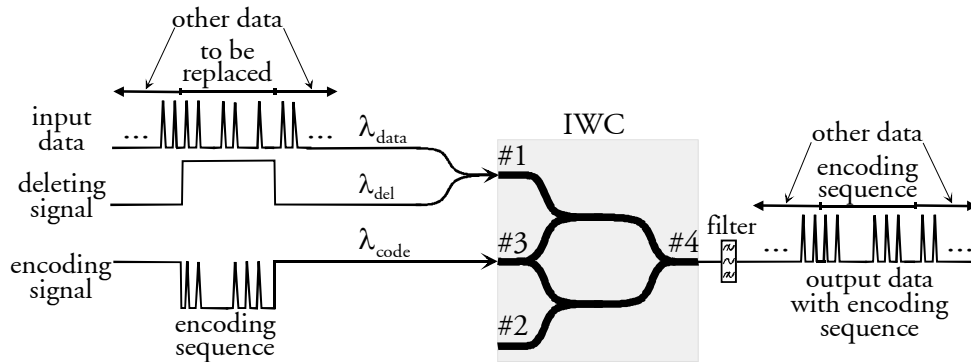
Fig. 6.20: Illustration of scheme for all-optical bit sequence replacement using an IWC (here, an MZI). The encoding signal is shown in a hybrid NRZ-RZ format to differentiate between the data modulated and control parts.

the coded message generated at the interferometer output (at λ_{code}), will correspond to the following Boolean logic function:

$$\text{(Deleting Signal } \textbf{OR} \text{ Input Data)} \textbf{ AND} \text{ Encoding Signal} \qquad (6.2)$$

In practice, this means that the deleting sequence ensures that all of the original check sequence in the data sequence is set to high, without affecting the rest of the data packet and without requiring knowledge of the contents of the corrupt check sequence. The encoding sequence modulates this high level with the coded message, while the rest of the data packet remains untouched.

It should be noted that if the scheme is used for error signalling as described above, the check sequence is replaced with the coded message. Thus, for practical implementation, each switch node should evaluate (e.g., using the scheme in Fig. 6.19) whether the check sequence or a predetermined error signalling sequence is present in the payload. If neither of these sequences is represented, an error has occurred, and the coded error signalling message should be inserted.

The scheme presented here makes encoding of a new sequence possible at an arbitrary place in a data sequence without electrical termination and using a single device. If the scheme is implemented with an MZI or MI, either RZ or NRZ format may be used. However, if a TOAD or UNI is used, only RZ-format is applicable, why the high levels of the encoding- and deleting signals in Fig. 6.20 should be replaced accordingly with RZ-pulses. Finally, it should be noted that because the scheme exploits logic AND, in-phase operation of the IWC must be employed, as discussed in Section 6.1.2.

6.3 Summary

This chapter has focussed on employment of the IWC as a Boolean logic gate. Moreover, practical applications of IWC-based optical logic for more complex signal processing have been described.

Some guidelines for full verification of the performance of optical logic gates have been given and, based on the MZI or MI, schemes for implementation of logic NOT, OR, AND and XOR have been described in detail. Moreover, requirements and limitations of the different IWCs (MZI, MI, TOAD and UNI) as optical logic gates have been discussed.

Using an MI, results have been shown for logic OR at 10 Gbit/s. The scheme is verified through comparison of the two input PRBS sequences with the output signal from the MI, where it was seen that all combinations in the OR truth table were represented. Moreover, a clear and open output eye-diagram with a high extinction ratio of ~12.5 dB verifies the good performance. Using the same Michelson interferometer, logic AND has likewise been verified at 10 Gbit/s with good performance. Again, all combinations in the truth table have been represented

correctly, and a clear and open eye-diagram with a high extinction ratio of ~15 dB has been obtained. Finally, logic XOR has been demonstrated in an MZI at 10 and 20 Gbit/s. Again, very good results are obtained at 10 Gbit/s with full verification of the truth table and a clear and open output eye-diagram. At 20 Gbit/s the XOR operation was also verified, although some patterning effects were present in the eye-diagram due to speed limitations. Moreover, it was discussed that due to the difference in carrier recovery and -depletion time, the NRZ format (applicable with the MZI and MI) does not enable as good a performance as the RZ format.

Subsequently, four novel schemes for applications in a network perspective were described, all of them relying on one or more Boolean functions implemented in a single IWC.

The first scheme, which involves replacement of individual bits in a data sequence using logic XOR, was proposed as a means for MPLS label swapping. The scheme was verified experimentally at 10 Gbit/s with excellent results, including a 13 dB output extinction ratio and a 0.4 dB power penalty.

The second scheme, which is applicable for pattern recognition, employs logic AND for sampling of individual bits at multiple wavelengths, thus converting the pattern from serial to parallel and relaxing the bandwidth requirements to the subsequent detector and electronic control circuitry. Apart from describing the principle of operation of the scheme, some variations that allow a reduction in the component count have been discussed, and a method for employing the scheme for packet self-routing in switch nodes through control of an SOA gate array has been described.

The third scheme enables identification of bit differences in data segments. This can for example be used for detection of errors in data packets at high bit rates. The principle of the scheme, which employs a combination of logic XOR and AND in a single IWC, has been described. It has been argued that if individual resolution of bit errors is not required, a single low-speed photodetector may be used for monitoring, while through combination with the second scheme, individual resolution using multiple photodetectors is possible.

Finally, the fourth scheme enables replacement of a high bit rate data segment optically in a single step by employing a combination of logic OR and AND in an IWC. The principle of operation has been described and its application for error signalling has been discussed.

Chapter 7

Conclusion

In this thesis, it has been argued that as the maturity of optics grows, more and more functionalities will be shifted from the electrical to the optical domain. The main motivation for this shift is that in the optical domain, issues such as power consumption, size and complexity are to a significant degree decoupled from the bit rate, thus enabling the advent of high-capacity networks. Although this evolution has already commenced with the MEMS-based optical cross-connect, it has been discussed that truly intelligent optical networks require the next step to be taken towards all-optical packet switching, which offers flexibility, scalability and high level of granularity. This thesis has been devoted to research areas that enable the realisation of all-optical packet switched networks; all topics are in some way related to the optical wavelength converter and its applications, both for improvement of the traffic performance as well as for signal processing. Although different techniques for wavelength conversion have been discussed, the focus has throughout mainly been on the SOA-based interferometric wavelength converter.

Initially, the implementation of an optical packet-switched network has been discussed, using the European research project DAVID as a case study. After giving an overview of the DAVID network architecture, which includes a MAN as well as a core network part, the focus was directed towards the core optical packet router, which exploits WDM in conjunction with wavelength conversion and an optical fibre-delay line recirculating buffer for contention resolution. A simulation model, that has been developed to investigate the performance of the OPR architecture employed in the DAVID project, has been described, and results gained from the model have been discussed. It has been demonstrated that a recirculating loop buffer is much more robust towards bursty traffic than a fibre delay-line based output buffer; bursty traffic only causes a minor increase in the packet loss rate compared to uniform traffic because the buffer is a shared medium. Subsequently, the packet loss rate of the DAVID OPR has been evaluated under uniform and bursty traffic conditions for a fixed-size- and degenerate loop buffer using the parameters specified within the DAVID concept: a maximum-size switching fabric of 256x256 with 6 ports carrying 32 wavelengths dedicated to transit traffic and up to the remaining 64 switch inlets dedicated to the recirculating loop buffer. It was seen that when the offered load per input channel was reduced from 0.8 to 0.6, a 55% reduction in size of the switching fabric was possible. This indicates the effectiveness of the recirculating loop buffer and demonstrates that splitting the switching fabric into parallel planes may be an effective way to reduce the component count per throughput. Finally, it was noted that for the fixed size loop, keeping the number of

inlets allocated to the loop fixed, but increasing the FDL length can reduce the PLR for bursty traffic. Thus, a performance that converges towards the situation for uniform traffic can be achieved in a very simple manner.

The key component for enabling the good traffic performance demonstrated for the DAVID OPR is the wavelength converter. In this thesis different techniques for wavelength conversion have been compared, with the focus mainly on the performance of the interferometric wavelength converter. The wavelength independence of the IWC was verified experimentally at 10 Gbit/s by a preamplified penalty below 1 dB over the entire C-band. Moreover, using the standard conversion scheme, 20 Gbit/s conversion in an MZI was demonstrated with a penalty of 0.8 dB, and a noisy yet open eye-diagram was obtained at 40 Gbit/s. By applying the differential control scheme a very good performance was achieved at 40 Gbit/s in an MZI, with a limited penalty of 0.6 dB. Finally, a scheme to increase the IPDR by controlling the bias currents to the input arms of an all-active MZI was described and demonstrated at 40 Gbit/s, with an increase in IPDR from ~4.5 to ~6 dB to follow.

The problem of conversion to the same wavelength was discussed, and a novel type of IWC, namely the dual order mode converter, was proposed as a possible solution. The performance of a DOMO MZI was investigated at 10 Gbit/s, showing almost wavelength independent operation from 1530 to 1560 nm. With non-identical signal and CW wavelengths a penalty of ~1.2 to 2.4 dB was incurred, while conversion to the same wavelength gave a penalty of 3-4 dB due to beating with the original data signal. In addition, the capabilities of the DOMO MZI were demonstrated at 20 Gbit/s, where a noisy yet open eye-diagram was obtained.

Finally, a novel conversion scheme involving the injection of an additional clock signal into the IWC has been presented. The scheme combines the advantages of good transmission properties and high-speed capabilities. Its feasibility has been verified at 10 Gbit/s and a comparison of the transmission capabilities has been made with the standard conversion scheme, showing results that are comparable to the best for the standard scheme.

2R and 3R regeneration are also key functionalities in all-optical networks. It has been argued that the sinusoidal transfer function achieved with wavelength conversion in an IWC enables reshaping, while conversion onto a clock signal recovered from the original data signal enables re-timing. The regenerative capabilities of an all-active MZI have been assessed at 40 Gbit/s using the differential control scheme. It was demonstrated that the MZI was capable of preserving the output OSNR above ~37 dB despite an input OSNR that was degraded to as low as ~13 dB by a noise generator. Furthermore, ~2 dB lower OSNR was tolerated through insertion of the MZI, clearly demonstrating its capabilities for noise suppression. Furthermore, conversion to a clock signal, which enables 3R regeneration, was demonstrated at 40 Gbit/s with a high output extinction ratio and a pre-amplified

penalty of only ~0.5 dB. Moreover, conversion to a clock signal enabled preservation of the RZ-format, in contrast to standard conversion to CW-light. Also the regenerative capabilities of the novel conversion scheme were evaluated at 10 Gbit/s; a ~4 dB lower input power level to the EDFA in the noise generator could be tolerated at a 2 dB penalty when the regenerator was inserted.

Finally, a novel scheme for all-optical regeneration using an IWC was described. The scheme, which is denoted the pass-through scheme, does not require wavelength conversion. The high IPDR of the scheme (~16 dB at 40 Gbit/s), which is caused by the quasi-digital transfer function, was demonstrated and good noise suppression capabilities were obtained at 40 Gbit/s, quantified by ~2.5 dB lower input power tolerated to the EDFA in the noise generator for a 2 dB penalty.

In addition to regeneration, the performance of the IWC for simultaneous wavelength conversion and time-division (de)multiplexing have also been demonstrated. Using an all-active MZI, 40 to 10 Gbit/s demultiplexing and wavelength conversion was accomplished successfully with a 3 dB penalty. Furthermore, 2x10 Gbit/s WDM to 20 Gbit/s time-division multiplexing was performed with a penalty of 2 dB.

Finally, the application of the IWC as a Boolean logic gate, important for more complex signal processing, has been demonstrated. Some guidelines for full verification of the performance of optical logic gates have been given and, based on the MZI or MI, schemes for implementation of logic NOT, OR, AND and XOR have been described in detail. Using an MI, results have been shown for logic OR and AND at 10 Gbit/s. In both cases, the functionality was verified through comparison of the two input PRBS sequences with the output signal from the MI, where it was seen that all combinations in the OR and AND truth table were represented. Moreover, a clear and open output eye-diagram with a high extinction ratio of ~12.5 and 15 dB, respectively, verified the good performance. Finally, logic XOR has been demonstrated in an MZI at 10 and 20 Gbit/s. Again, very good results are obtained at 10 Gbit/s with full verification of the truth table and a clear and open output eye-diagram. At 20 Gbit/s the XOR operation was also verified, although some patterning effects were present in the eye-diagram due to speed limitations.

Subsequently, four novel schemes for applications in a network perspective were described. All of them rely on one or more Boolean functions implemented in a single IWC, and all enable important signal processing functionalities in high-speed networks to be implemented all-optically in a simple and cost-effective manner. The latter three have been filed as patents in collaboration with the Technical University of Denmark. The first scheme, which involves replacement of individual bits in a data sequence using logic XOR, was proposed as a means for MPLS label swapping. The scheme was verified experimentally at 10 Gbit/s with excellent results, including a 13 dB output extinction ratio and a 0.4 dB power penalty. The second scheme, which is applicable for pattern recognition, employs logic AND for sampling of

individual bits at multiple wavelengths, thus converting the pattern from serial to parallel and relaxing the bandwidth requirements to the subsequent detector and electronic control circuitry. Apart from describing the principle of operation of the scheme, some variations that allow a reduction in the component count have been discussed, and a method for employing the scheme for packet self-routing in switch nodes through control of an SOA gate array has been described. The third scheme enables identification of bit differences in data segments, which can, for example, be used for detection of errors in data packets at high bit rates. The principle of the scheme, which employs a combination of logic XOR and AND in a single IWC, has been described. It has been argued that if individual resolution of bit errors is not required, a single low-speed photodetector may be used for monitoring, while through combination with the second scheme, individual resolution using multiple photodetectors is possible. Finally, the fourth scheme enables replacement of a high bit rate data segment optically in a single step by employing a combination of logic OR and AND in an IWC. The principle of operation has been described and its application for error signalling has been discussed.

In my opinion, the work in Chapter 6 on all-optical logic and its applications constitutes the most important research contributions of my PhD study and this dissertation.

This thesis has demonstrated the wide application of IWCs as wavelength converters enabling excellent traffic performance, as 2R and 3R regenerators enabling scaleable all-optical networks and as logic gates enabling complex signal processing. Although its versatility and good performance make the IWC very attractive for intelligent all-optical networks, the technological developments of the future are difficult to predict. Many challenges still lie ahead before the IWC is ready for use in commercial networks. For example, reproducibility and control are issues that must be dealt with. Moreover, novel innovative technologies may be developed, which by far supersede the capabilities of the IWC. In this respect, photonic bandgap structures show promising results. Still, at the time of writing, IWCs exhibit the most attractive characteristics by far, making them prime candidates for use in future optical networks, once technological maturity has been reached.

Ph.D. publications and patents

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