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Nanoimprint Lithography of Topology Optimized Photonic Crystal Devices

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Abstract: We demonstrate a nanoimprint process for fabrication of photonic crystal devices. The nanoimprint process, defining stamp patterns in a thin e-beam resist, yields improved pattern replication compared to direct e-beam writing of the devices.

OCIS codes: (130.3120) Integrated optics devices; (220.4000) Microstructure fabrication

The optical performance of photonic crystal (PhC) components is highly sensitive to the nanometer feature sizes of the components. Even small deviations may be devastating for the functionality and/or the target operating frequency. Recently, topology optimization has proven to be a strong tool for the optimization of PhC components [1]. Such optimized structures do, however, require an even higher degree of fidelity in the pattern transfer.

Along with the requirements of obtaining a high aspect ratio between pattern depth and size, these issues form a serious challenge for photonic crystal- and wire-based technologies. Approaches based on direct electron beam lithography (EBL) and a soft etch mask have been successfully demonstrated. However, the low etch resistance of the electron beam resist mask limits this approach to resist thicknesses of 100 nm and above, compromising the lithographic resolution. Application of hard masks or transfer layers also limits the resolution and pattern transfer fidelity. We present a nanoimprint process for fabrication of photonic crystal devices (and other nanoscale applications) in silicon. High resolution and high aspect ratio of the transferred pattern is obtained by exploiting a high-resolution negative EBL resist for silicon stamp fabrication in combination with nanoimprint lithography (NIL) in a thermoplastic resist with high etching resistance.

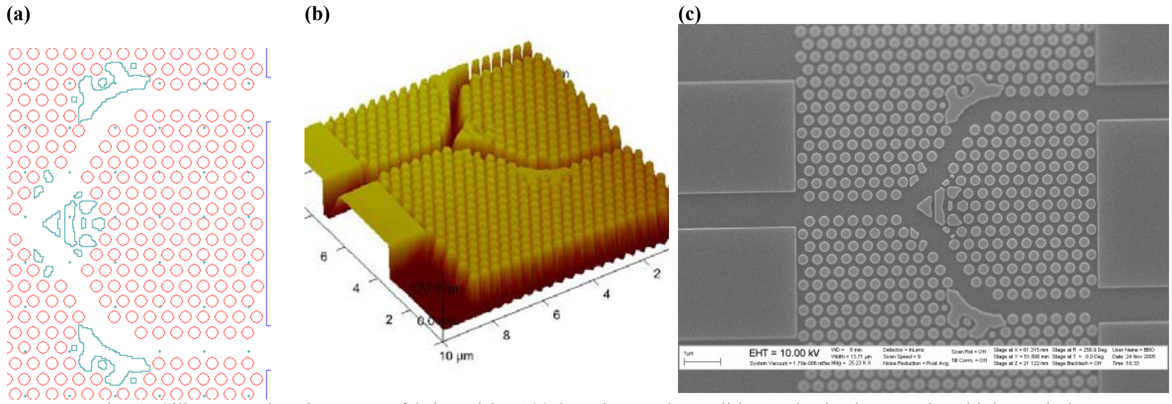

Fig. 1. Silicon nanoimprint stamp, fabricated by 100 kV electron beam lithography in the negative, high resolution resist TEBN-1, and reactive ion etching. The design shown in panel (a) is compared with an AFM image in panel (b) and a scanning electron micrograph picture of the silicon stamp in panel (c).

The silicon stamp is fabricated by 100 kV EBL (JEOL JBX9300FS) in a 50 nm thick film of TEBN-1 [2] on a silicon substrate at an exposure dose of 9 mC/cm^2. The written structures are developed in methyl isobutyl ketone (MIBK) for 20 s, rinsed in isopropyl alcohol (IPA) and subsequently transferred 100 nm into the silicon substrate by a highly anisotropic reactive ion etch [3]. After etching the silicon, any remaining resist is removed in oxygen plasma prior to deposition of an anti sticking layer from a C_4F_8 plasma and imprinting.

An 80 nm thick film of mr-I T85 (4 wt%) is spincoated onto a silicon-on-insulator (SOI) substrate at a spin speed of 3000 rpm and baked at 150°C for 5 min on a hot plate. The stamp is imprinted using an EVG imprint tool (EVG 520HE). The optimum imprint parameters for replication of the PBG structures are found to be: Imprint

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temperature 140°C, imprint time 10 min, and imprint pressure 13 bar. The imprint takes place in vacuum (0.01 mbar) and the stamp and substrate are separated at a temperature of 60°C. The imprint parameters result in a complete filling situation of the stamp in the PBG structured areas, resulting in 100 nm deep holes in the mr-I T85 resist. The nanoimprinted patterns are transferred into the top 320 nm thick silicon layer of a SOI substrate by using an optimized SF_6-based inductively coupled plasma (ICP) etch. The etch selectivity of silicon over mr-I T85 is 9:1 (Silicon:mr-I T85) [4] which allows for pattern transfer of the imprinted holes through the device silicon layer of the SOI substrate.

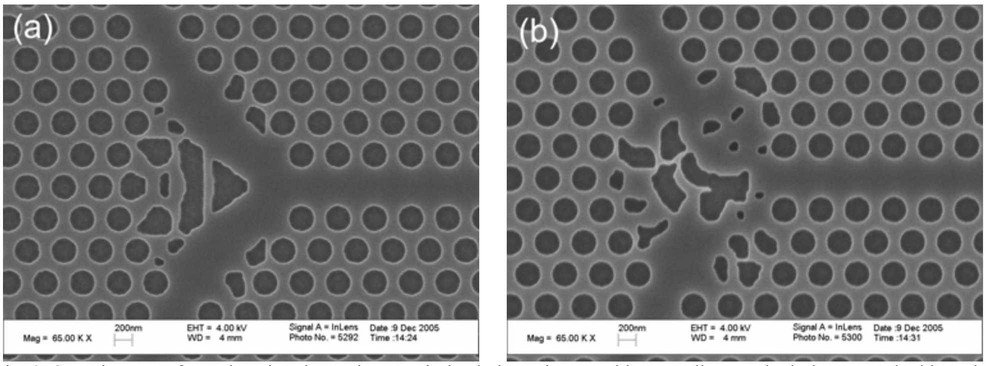

Fig. 2. SEM images of nanoimprinted, topology optimized photonic crystal beam splitters. The holes are etched into the top-silicon layer (thickness 320 nm) of a silicon-on-insulator wafer.

The lithographic result of our imprint process is compared to devices fabricated by direct electron beam writing of the etch mask. For direct writing, the positive resist ZEP520a was exposed at 100 kV, using the same EBL tool as used for stamp fabrication. The ZEP520a resist has a selectivity of ~5 compared to silicon in the ICP etch, hence, a layer of 100-150 nm is necessary to transfer the pattern into the silicon layer. The results are shown in Figure 3, where the detailed and complex features in the central part of a splitter device fabricated by direct EBL (left) and with NIL (right) are compared with each other and with the design pattern (middle). As seen from the figure, the NIL process replicates the nanoscale pattern details with a quality comparable or better than by direct electron beam writing.

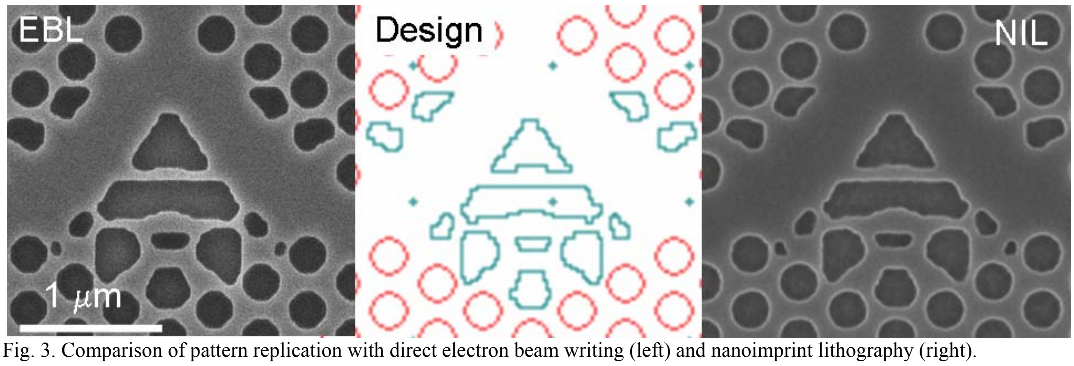

Fig. 3. Comparison of pattern replication with direct electron beam writing (left) and nanoimprint lithography (right).

In conclusion, we have presented a nanoimprint lithography process for photonic crystal devices (and similar pattern transfer applications), based on high resolution 100 kV electron beam lithography in a 50 nm film of the negative resist TEBN-1 for stamp fabrication, thermal nanoimprint in a 100 nm film of mr-I T85 nanoimprint resist, and pattern transfer by reactive ion etching into silicon. A resulting high resolution in combination with high aspect ratio of the transferred pattern is obtained by exploiting the high resolution of TEBN-1 for stamp fabrication and the high etch resistance of the mr-I T85 nanoimprint resist for pattern transfer. The obtained lithographic results of the nanoimprint process match the results obtained by direct electron beam writing of a resist mask for reactive ion etching of the nanostructures

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