DESIGN CONSIDERATIONS FOR WIDE BANDWIDTH CONTINUOUS-TIME LOW-PASS DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTERS

A Thesis

by

ARAVIND KUMAR PADYANA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2010

Major Subject: Electrical Engineering

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ABSTRACT

Design Considerations for Wide Bandwidth Continuous-Time Low-Pass

Delta-Sigma Analog-to-Digital Converters. (December 2010)

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Co-Chairs of Advisory Committee: Dr. Jose Silva-Martinez
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Continuous-time (CT) delta-sigma (ΔΣ) analog-to-digital converters (ADC) have emerged as the popular choice to achieve high resolution and large bandwidth due to their low cost, power efficiency, inherent anti-alias filtering and digital post processing capabilities.

This work presents a detailed system-level design methodology for a low-power CT ΔΣ ADC. Design considerations and trade-offs at the system-level are presented. A novel technique to reduce the sensitivity of the proposed ADC to clock jitter-induced feedback charge variations by employing a hybrid digital-to-analog converter (DAC) based on switched-capacitor circuits is also presented. The proposed technique provides a clock jitter tolerance of up to 5ps (rms). The system is implemented using a 5^{th} order active-RC loop filter, 9-level quantizer and DAC, achieving 74dB SNDR over 20MHz signal bandwidth, at 400MHz sampling frequency in a 1.2V, 90 nm CMOS technology.

A novel technique to improve the linearity of the feedback digital-to-analog converters (DAC) in a target 11-bits resolution, 100MHz bandwidth, 2GHz sampling frequency CT ΔΣ ADC is also presented in this work. DAC linearity is improved by combining dynamic element matching and automatic background calibration to achieve up to 18dB improvement in the SNR. Transistor-level circuit implementation of the proposed technique was done in a 1.8V, 0.18μm BiCMOS process.

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1. INTRODUCTION

1.1 Motivation

Recent developments in mobile computing and broadband wireless communications have led to a strong need for low power and cost effective analog-to-digital converters. Broadband analog-to-digital converters have been identified as a relevant need in the International Technology Roadmap for Semiconductors (ITRS). The quest for higher data rates is leading to the proliferation of standards with larger signal bandwidths. Mobile and broadband wireless standards are increasingly being adopted by the industry.

In order to take advantage of technology scaling and software reconfigurability, the current approach in RF receiver design is to digitize the RF information as close as possible to the antenna and perform most of the signal processing in the digital domain resulting in a flexible and reconfigurable receiver. Figure 1 shows the direct conversion wireless radio receiver architecture.

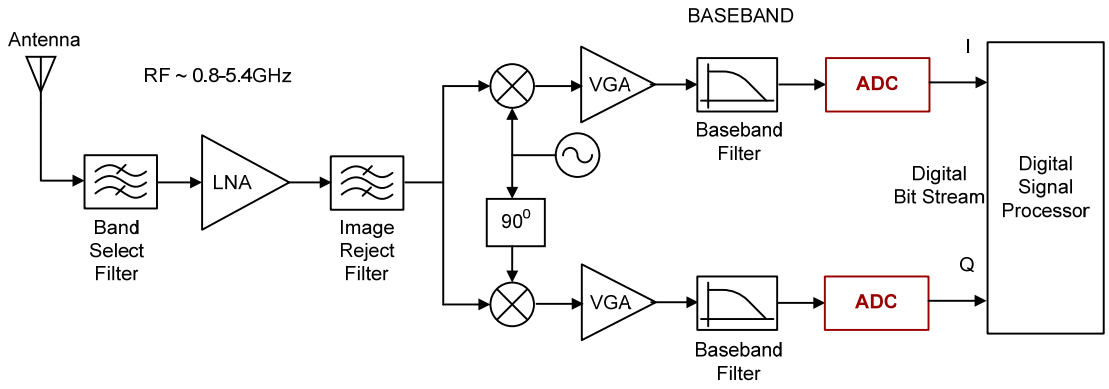

Figure 1. Direct-conversion radio receiver architecture

In the traditional super-heterodyne radio architecture, the received signal is digitized at

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This thesis follows the style of *IEEE Journal of Solid-State Circuits.*

an intermediate frequency after significant analog pre-processing consisting of down-conversion, filtering, and amplification. In the direct-conversion architecture, the received signal is digitized in baseband, with filtering and amplification performed in the digital domain. Hence, direct-conversion (DC) architecture is usually preferred for broadband receivers because of lower power consumption and fewer external components compared to a super-heterodyne approach. However, the reduction in system complexity is at the expense of increased bandwidth, resolution, linearity and dynamic range requirements on the analog-to-digital converter (ADC).

1.2 Application Space

Modern wireless receivers are required to provide support for multiple communication standards on a single chip.

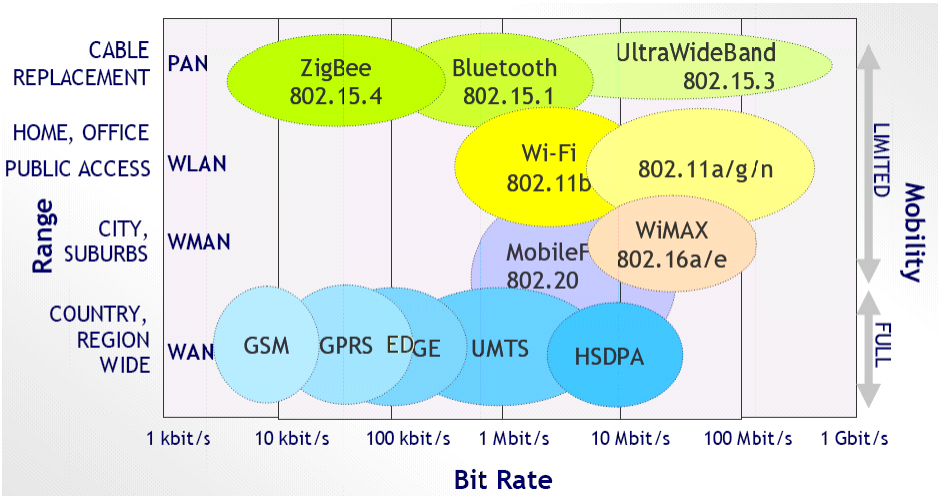


Figure 2. Modern communication standards

As shown in Figure 2, various wireless communication standards are used depending on the mobility range and the data rate. Cell phone communication standards such as GSM (Global System for Mobile communications), GPRS (General Packet Radio Service), EDGE (Enhanced Data rates for GSM Evolution), UMTS (Universal Mobile Telecommunication System), HSDPA (High-Speed Downlink Packet Access)

require full mobility. Communication network standards such as WiMAX (Worldwide interoperability for Microwave Access), WLAN (Wireless Local Area Network), IEEE 802.20 MBWA (Mobile Broadband Wireless Access), ZigBee, Bluetooth, UWB (Ultra Wide Band) require limited mobility.

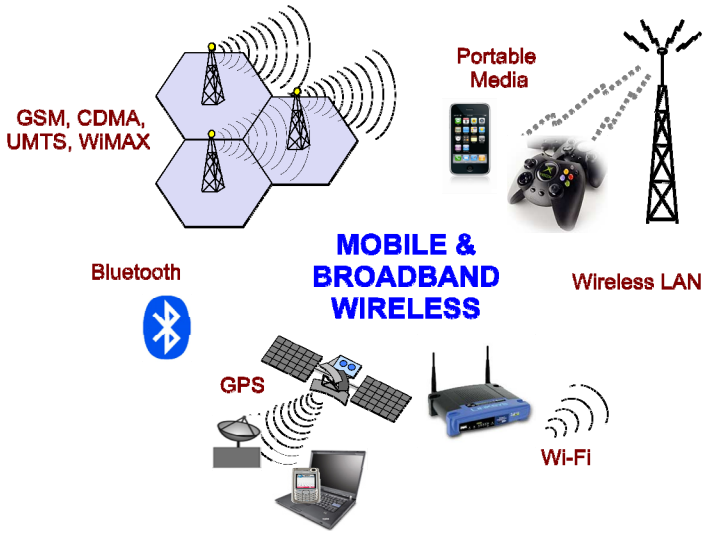


Figure 3. Application space of broadband analog-to-digital converters

The broad application space of analog-to-digital converters is shown in Figure 3. Internet and computer technologies have revolutionized communication and entertainment in recent times. These technologies are expected to be available to a large population in the form of ultra-mobile, wireless internet enabled multimedia devices with low cost, low power analog interface circuits. Broadband wireless networks require high resolution analog-to-digital conversion solutions, especially in multi-standard receiver applications where the desired signal has to be detected in the presence of strong interferers. Direct-conversion receiver solutions offering high resolution over a signal bandwidth have recently been reported [1-10].

1.3 Delta-Sigma ADCs

Delta-Sigma (ΔΣ) ADCs are a popular choice in wireless applications due to their high dynamic range and low power consumption. Delta-Sigma ADCs are broadly classified into two categories, Discrete-time (DT) ΔΣ ADCs that employ switched-capacitor filters, and Continuous-time (CT) ΔΣ ADCs which use continuous-time filters. Due to reduced settling time requirements on the amplifiers used to realize the filters, CT ΔΣ ADCs are more power efficient compared to DT ΔΣ ADCs. Additionally, CT ΔΣ ADCs offer inherent anti-alias filtering. Hence, CT ΔΣ ADCs have emerged as the popular choice for realizing high resolution, high bandwidth ADCs. However, the main drawbacks of CT ΔΣ ADCs are increased sensitivity to clock jitter, susceptibility to time constant variations and excess loop delay. Despite these disadvantages, there has been a tremendous interest in CT ΔΣ ADCs as seen by papers published in the recent literature.

The focus of this work is to develop system-level and circuit-level design techniques for high resolution, wide bandwidth, low power CT ΔΣ ADCs suitable for wireless applications.

1.4 Thesis Organization

This thesis describes the detailed system-level design of a low power (less than 20mW), 12-bit, 20MHz bandwidth CT ΔΣ ADC. A novel hybrid DAC scheme is presented to improve tolerance to clock jitter. Additionally, a linearity enhancement technique for multi-bit digital-to-analog converters implemented for a 12-bit, 100MHz CT ΔΣ ADC is also presented.

Section 2 provides an overview of sampling and quantization in ADCs. The basic principles of operation in ΔΣ ADCs and most critical non-idealities are explained briefly. A literature survey of recently reported work on wideband ΔΣ ADCs is also presented.

Section 3 presents the detailed system-level design methodology of a 12-bit, 20MHz CT ΔΣ ADC and corresponding simulation results.

Section 4 explains the issues of clock jitter in CT ΔΣ ADCs in detail. A clock jitter tolerant hybrid digital-to-analog converter (DAC) architecture is proposed and simulation results are presented.

Section 5 discusses the effects of DAC non-linearity in CT ΔΣ ADCs. DAC linearization techniques are proposed for a multi-bit design used in an 11-bit, 100MHz bandwidth CT ΔΣ ADC. Section 6 presents summary and conclusions.

2. CONTINUOUS-TIME DELTA-SIGMA ADCs

Significant advances in technology have enabled rapid developments in the field of digital signal processing (DSP) which operate on signals that are digital in nature, that is, discrete in time with amplitude quantization. However, real world signals are fundamentally analog in nature, being continuous in time and amplitude. Hence, there is a need for efficiently converting information between the analog and digital domains. The generic block diagram of a mixed-signal system is as shown in Figure 4.

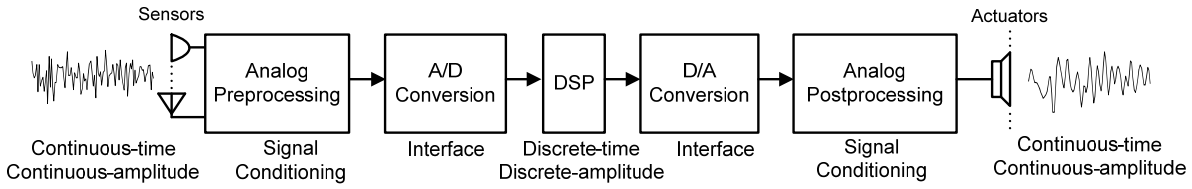


Figure 4. Generic block diagram of a mixed-signal system

2.1 Sampling and Quantization

The generalized block diagram of an analog-to-digital conversion process is illustrated in Figure 5. The analog input signal to the system contains useful information up to a frequency of F_{in}. The input is sampled at a frequency F_s to obtain a discrete-time signal. By Nyquist theorem, in order to avoid loss of information, the sampling frequency F_s should be at least twice the maximum input signal frequency, that is, $2*F_{in}$.

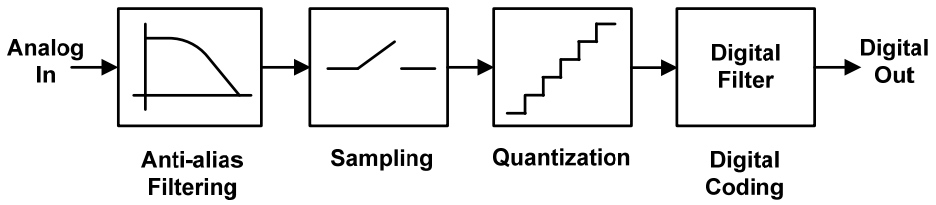


Figure 5. Analog-to-digital conversion

However, frequency components above F_{in} are folded back or aliased into the bandwidth of the input signal, making them indistinguishable from the original signal. Ideally, the anti-alias filter is a brick-wall filter with a cutoff frequency equal to $2*F_{in}$ that completely attenuates input signal frequency components greater than F_{in}. The sampled signal is discrete in time and continuous in amplitude. The quantizer converts the sampled signal into a discrete-time, discrete-level signal by mapping the signal into a finite number of allowable output levels based on the corresponding quantization interval. Assuming that the quantization error has uniform probability density function and provided the quantization errors are sufficiently random in nature, for any N-bit quantizer, the quantization noise power always extends from DC to $F_s/2$ with a mean square value given by [11],

$$\sigma_q^2 = \frac{\Delta^2}{12} \tag{2.1}$$

where the quantization step (Δ) is defined by (2.2) for a reference voltage of $\pm V_{ref}$.

$$\Delta = \frac{2V_{ref}}{2^N - 1} \tag{2.2}$$

In a Nyquist-rate ADC, the sampling frequency is twice the bandwidth of the input signal, that is, $2*F_{in}$. The quantization noise power is assumed to be white with a uniform spectral density distribution between DC and $F_s/2$ as shown in Figure 6. In reality, F_s is chosen to be slightly greater than $2*F_{in}$ in order to relax the requirements on the anti-alias filter.

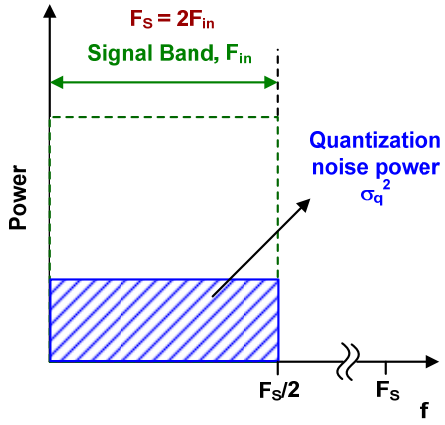


Figure 6. Quantization noise in a Nyquist-rate ADC

For an N-bit Nyquist-rate ADC, the maximum signal-to-quantization-noise ratio is given by,

$$\mathrm{SQNR(dB)} = 6.02\mathrm{N} + 1.76 \tag{2.3}$$

indicating that the resolution of the ADC improves by 1-bit for every 6-dB improvement in SQNR.

2.2 Oversampling and Noise-shaping

As discussed in Section 2.1, the quantization noise power always extends from DC to $F_s/2$ and the total quantization noise power has to satisfy relation (2.1). Hence, if F_s is increased to higher values, the quantization noise power is spread over a larger range of frequencies resulting in a reduction in the total quantization noise over the input frequency range. This principle is exploited in oversampled ADCs where $F_s >> 2*F_{in}$. The total in-band quantization noise power is given by,

$$\mathrm{N}_q^2 = \frac{\sigma_q^2}{\mathrm{OSR}} \tag{2.4}$$

where the oversampling ratio is defined as,

$$\mathrm{OSR} = \frac{F_s}{2F_{in}} \tag{2.5}$$

The maximum SQNR for an oversampled ADC is given by,

$$\mathrm{SQNR(dB)} = 6.02N + 1.76 + 10\log_{10}\mathrm{OSR} \tag{2.6}$$

(2.6) indicates that oversampling improves the ADC performance at the rate of 3dB/octave or equivalently, 0.5bit/octave.

A more efficient way to use oversampling is to shape the spectral density such that most of the quantization noise power is outside the band of interest as shown in Figure 7. The principle of noise-shaping is used in ΔΣ ADCs where the noise in shaped in such a manner so as to not affect the desired signal band. It can be concluded that quantization noise-shaping can be achieved by modifying the original quantization noise with a high-pass transfer function.

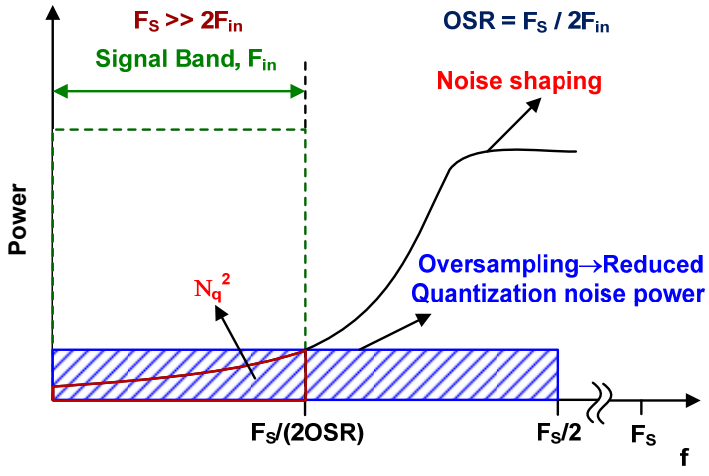


Figure 7. Quantization noise in an oversampled ADC

2.3 Delta-Sigma Analog-to-Digital Converters

2.3.1 Basic Principles

A delta-sigma (ΔΣ) ADC is an oversampled analog-to-digital converter where the quantization noise is shaped to greatly reduce the in-band quantization noise power resulting in a high SQNR within the signal bandwidth. The basic components of a discrete-time ΔΣ ADC are shown in Figure 8 [12].

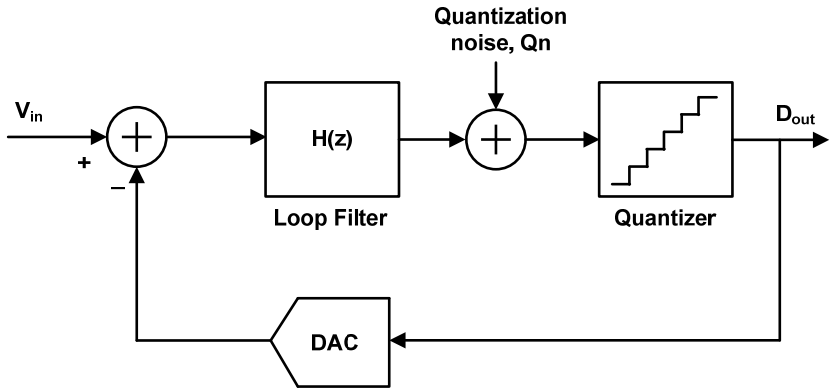


Figure 8. Block diagram of a discrete-time ΔΣ ADC

The system consists of a loop filter in the forward path of the loop, an internal low-resolution ADC and digital-to-analog converter (DAC). Using the linearized z-domain model, the output is given by,

$$\mathrm{V(z)} = \mathrm{STF.\,U(z)} + \mathrm{NTF.\,E(z)} \tag{2.7}$$

where the signal transfer function (STF) and noise transfer function (NTF) are defined as,

$$\mathrm{STF} = \frac{\mathrm{V(z)}}{\mathrm{U(z)}} = \frac{\mathrm{H(z)}}{1 + \mathrm{H(z)}} \tag{2.8}$$

$$\mathrm{NTF} = \frac{\mathrm{E(z)}}{\mathrm{U(z)}} = \frac{1}{1 + \mathrm{H(z)}} \tag{2.9}$$

The digital output is processed by a decimation filter and subsequently passed through additional digital filters to attenuate out-of-band quantization noise to obtain the final output at the Nyquist rate. The loop filter is typically implemented as a low-pass filter resulting in a discrete-time low-pass ΔΣ ADC.

In a first order discrete-time ΔΣ ADC, the loop filter is a first-order integrator with H(z), STF and NTF given by,

$$\mathrm{H(z)} = \frac{\mathrm{z^{-1}}}{1 - \mathrm{z^{-1}}}; \mathrm{STF} = \mathrm{z^{-1}}; \mathrm{NTF} = 1 - \mathrm{z^{-1}} \tag{2.10}$$

(2.10) shows that the signal is only delayed by one sample and hence, appears unaltered at the output whereas the quantization noise is shaped by a first-order high-pass transfer function.

In general, by using a $\mathrm{L^{th}}$ order loop filter, which can be realized by cascading L first order integrators, the quantization noise is shaped more aggressively by a NTF given by,

$$\mathrm{NTF} = (1 - \mathrm{z^{-1}})^{\mathrm{L}} \tag{2.11}$$

The in-band integrated quantization noise power and the maximum SQNR are given by,

$$\mathrm{N_q^2} = \frac{\sigma_\mathrm{q}^2 \pi^{2\mathrm{L}}}{(2\mathrm{L} + 1)\mathrm{OSR}^{2\mathrm{L}+1}} \tag{2.12}$$

$$\begin{aligned} \mathrm{SQNR(dB)} = {} & 6.02\mathrm{N} + 1.76 + (2\mathrm{L} + 1)10 \log_{10} \mathrm{OSR} \\ & - 10 \log_{10} \frac{\pi^{2\mathrm{L}}}{2\mathrm{L} + 1} \end{aligned} \tag{2.13}$$

(2.13) shows that Lth-order noise-shaping improves the ADC performance at the rate of (6L+3)dB/octave or equivalently, (L+0.5)bits/octave.

2.3.2 Discrete-time vs. Continuous-time ΔΣ ADCs

DT ΔΣ ADCs are implemented using switched-capacitor (SC) circuits or switched-current (SI) circuits and are predominantly used for low frequency applications where high resolution is required over very low signal bandwidths. CT ΔΣ ADCs use continuous-time circuits to implement the loop filter and offer several advantages over DT ΔΣ ADCs [13-14].

1. Due to the use of switched capacitor circuits in DT ΔΣ ADCs, the maximum sampling frequency is limited by the achievable op-amp bandwidth and required settling time in the technology. In comparison, CT ΔΣ ADCs impose significantly relaxed requirements on op-amp bandwidths. This implies that for comparable performance, CT ΔΣ ADCs consume significantly lesser power than DT ΔΣ ADCs.
2. In a DT ΔΣ ADC, the input to the system is a sampled signal. Sampling errors at the input appear directly in the digital output, thereby degrading the SNR. In contrast, in a CT ΔΣ ADC, the sampling operation occurs at the input of the quantizer and hence, sampling errors are heavily suppressed by the high in-band loop gain of the preceding filter. Additionally, this also reduces the thermal noise contribution of the first integrator stage as the high frequency thermal noise is filtered substantially by the loop filter before sampling, thereby avoiding aliasing.
3. An explicit anti-alias filter is required at the input of a DT ΔΣ ADC. CT ΔΣ ADCs possess an inherent anti-aliasing characteristic.
4. In a DT ΔΣ ADC, large glitches appear on the op-amp virtual ground node due to switching transients. In contrast, virtual ground nodes can be kept very quiet in CT ΔΣ ADCs.

5. In DT ΔΣ ADCs, integrator time constants are set capacitor ratios which can be controlled to an accuracy of up to 1%. In CT ΔΣ ADCs, integrator time constants are set by resistor-capacitor products which can vary up to 30%. Hence, CT ΔΣ ADCs require tuning and calibration schemes to accurately control the integrator time constants.

2.4 Continuous-time ΔΣ ADCs Non-idealities

Non-idealities in a ΔΣ ADC can be modeled as error signals which introduce noise and distortion into the system and can have drastically different effects based on the point at they are input. Figure 9 shows the error sources at different points in a ΔΣ modulator [15].

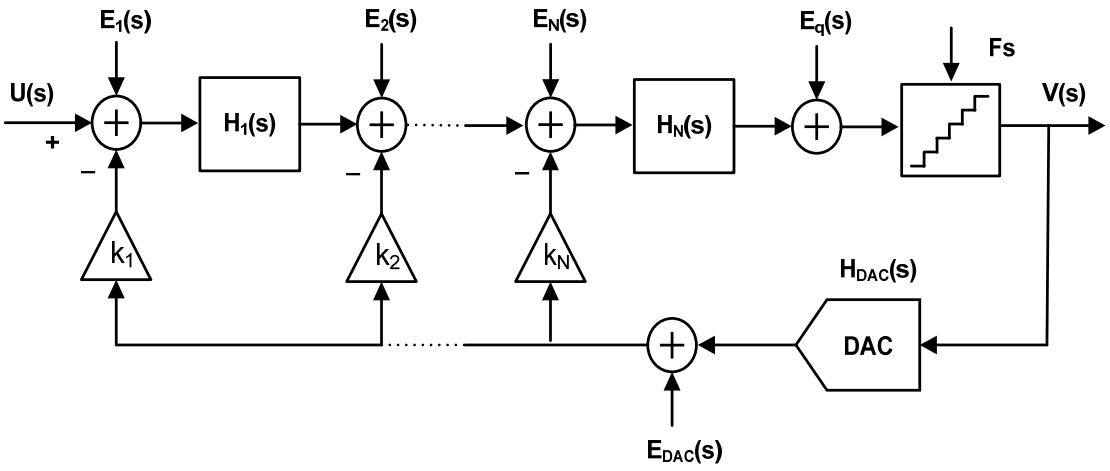


Figure 9. Input locations for non-idealities in a continuous-time ΔΣ ADC

$E_i(s)$ represents the input referred noise and distortion of the corresponding integrator stage $H_i(s)$, $E_q(s)$ represents the errors entering the system at the internal quantizer and $E_{DAC}(s)$ represents the errors of the feedback DAC. A ΔΣ ADC is most sensitive to any error that occurs at the input of the modulator. The transfer function from the error sources at the input of the modulator, that is, E_1 and E_{DAC} to the output is given by,

$$\frac{V}{E_1} = \frac{V}{E_{DAC}} = \frac{H}{1+H} \cong 1 \tag{2.14}$$

where H is the loop filter transfer function.

Hence, the in-band components of the error sources $E_1$and E_{DAC} appear at the output of the modulator without any suppression. The most dominant contributors of E_{DAC} are the errors due to clock jitter and DAC non-linearity. The feedback DAC requires linearity close to the resolution of the overall modulator. The transfer function from E_q to the modulator output is given by,

$$\frac{V}{E_q} = \frac{1}{1+H} \tag{2.15}$$

The in-band components of the errors sources located at other points in the system are less critical. E_q is heavily suppressed by the high in-band loop gain of the preceding filter. Errors E_i (i>1) at the various stages of the loop filter are also suppressed by the in-band gain of the preceding filter stages.

2.4.1 DAC Non-idealities

The most important DAC non-idealities are errors caused due to clock jitter, DAC non-linearity, slew rate of the DAC outputs and errors caused due to excess loop delay.

Clock jitter causes a statistical variation in the edge or duration of the feedback DAC pulse. Since a CT ΔΣ ADC integrates the feedback waveform over time, a statistical variation of the feedback waveform results in a statistical integration error leading to an increase in the in-band noise. Clock jitter is explained in detail in Section 4.

DAC non-linearity is caused when different output levels of the DAC are affected by mismatch. The variation in the feedback levels yields a signal-dependent feedback charge error which is directly fed to the modulator input.

The DAC outputs also exhibit a finite slew rate with unequal rise and fall times which cause an effect similar to inter-symbol interference (ISI). These error sources cause additional noise and tones in the spectrum that fold into the baseband and degrade modulator performance.

Excess loop delay (ELD) is a timing non-ideality which can be considered as a constant delay between the ideal and implemented DAC feedback pulse. ELD can occur due to the finite response time of the DAC outputs to its clock and inputs, and the decision time required by the quantizer which in turn affects the latches used for synchronizing the DAC inputs. ELD causes a variation in the implemented loop filter coefficients and also leads to an increased modulator order, both of which can cause system instability.

2.4.2 Filter Non-idealities

The most important filter non-idealities are due to finite op-amp gain, integrator time constant variation, finite amplifier gain-bandwidth product, finite slew rate, limited output swing, amplifier noise and non-linearity.

Finite DC gain in the op-amp causes all zeros of the NTF to move away from DC, which reduces the amount of attenuation in the baseband. Finite amplifier gain-bandwidth product causes incomplete settling of the integrator outputs leading to an increase in the in-band quantization noise.

Finite amplifier slew rate is a non-linear effect which causes an increase in the harmonic distortion and in-band quantization noise due to the limited current capability of the op-amp output stage.

Limited output swing capability of the op-amps causes a signal-dependent variation in the integrator outputs, thereby introducing non-linearity in the modulator output.

Additionally, circuit noise and non-linearity of the first integrator at the loop filter are particularly important since they significantly contribute to the overall noise floor of the modulator.

One of the major non-idealities of the filter is the integrator time constant error. Integrator time constants are mapped into resistor–capacitor products which are known to vary over process and temperature by up to 30%.

2.4.3 Quantizer Non-idealities

The quantizer is preceded by several high gain stages; hence, ΔΣ ADCs are insensitive to DC offset and non-linearity introduced by the internal quantizer. However, quantizer metastability and signal-dependent quantizer delay causes a random variation in the rising and falling edges of the quantizer outputs resulting in an effect similar to clock jitter, therby causing degradation in the output SNR.

2.5 Literature Survey

As discussed in Section 2.3.2, CT ΔΣ ADCs offer several advantages and consequently have attracted a lot of attention as digital-friendly architecture for ADC since a substantial part of the signal processing is performed in the digital domain. Table 1 shows recently reported wide bandwidth continuous-time ΔΣ ADCs.

Due to the widespread use of CMOS technology for digital applications, it has emerged as the technology of choice for cost-conscious designs as it enables easy integration with further downstream digital processing. This is evident from publications such as [1-5] showing modulator implementations in the most advanced process technology nodes. Additionally, recently reported literature [1-2] propose innovative techniques to utilize the high speed capabilities of nanometric CMOS technologies by using resolution in the time domain compared to the traditional way of representing signals in the voltage domain. Although these CMOS implementations achieve high

resolutions with low power consumption, the bandwidths achieved are limited to the 20-25MHz range.

Table 1. Comparison of prior art on wide bandwidth ΔΣ ADCs

Ref.	Technology	Sampling Freq (Hz)	Bandwidth (Hz)	SNR (dB)	SNDR (dB)	Power (mW)
[1]	65nm CMOS	250M	20M	62	60	10.5
[2]	130nm CMOS	900M	20M	81.2	78.1	87
[3]	90nm CMOS	420M	20M	72	70	27.9
[4]	180nm CMOS	400M	25M	53	52	18
[5]	130nm CMOS	640M	20M	76	74	20
[6]	SiGe HBT	35G	100M	58.9	53.1	350
[7]	SiGe HBT	20G	312.5M	30.5	-	490
[8]	InP HBT	8G	250M	-	40	1800
[9]	InGaAs HBT	18G	500M	-	42	1500
[10]	InGaAs HEMT	5G	100M	43	39	400

Previous works reported in [8-10] have achieved moderate resolutions over very wide bandwidths (>100MHz) with large power consumption. They make use of expensive III-V process technologies which provide very high-f_T transistors with high current capability. However, these technologies are limited in their use to niche applications.

3. SYSTEM-LEVEL DESIGN OF A 12-BIT, 20MHz CT ΔΣ ADC

It is convenient to examine a DT ΔΣ ADC using a mathematical model and hence, easier to simulate on a computer. The prevalence of DT ΔΣ ADCs has led to the development of several tools and extensive design methodologies such as the ΔΣ toolbox for MATLAB [16]. Consequently, a common approach in the design of a CT ΔΣ ADC is to perform the initial design in the DT domain and then use impulse-invariant transformation to obtain an equivalent realization in the CT domain. The design methodology of a CT ΔΣ ADC is presented in detail in this section.

3.1 System-level Design Considerations

3.1.1 Order

The number of integrators used in to realize the loop filter determines the order (L) of the ΔΣ modulator. 2^{nd} order modulators are widely used since they are inherently stable. Higher SQNR can be achieved by increasing the order of the modulator at the cost of reduced stability and robustness to process, voltage, and temperature (PVT) variations.

3.1.2 Oversampling Ratio

It can be noted from (2.13) that the maximum achievable SQNR can be increased by using a higher oversampling ratio (OSR). However, for a given desired signal bandwidth, a higher OSR translates to a higher sampling frequency, which is limited by the f_T of the technology. Also, a higher sampling frequency leads to increased power consumption. Several reported low-power, wide bandwidth modulators use a low OSR typically in the range 8-16 [1], [3-5].

3.1.3 Quantizer Resolution

For a fixed voltage reference, increasing the number of levels in the quantizer reduces the quantization interval and hence, leads to a lower quantization noise and a higher SQNR. Additionally, a higher quantizer resolution also improves the stability of the modulator and tolerance to clock-jitter. However, power and area requirements of quantizer rise exponentially with the number of bits and impose stringent linearity requirements on the feedback DACs.

3.1.4 Maximum Noise Transfer Function Gain

For frequencies outside the signal bandwidth, the NTF gain increases at a rate of 6L dB/octave and reaches a maximum at $F_s/2$. The maximum NTF gain determines the aggressiveness of the noise-shaping and a higher SQNR is obtained by increasing the maximum NTF gain. However, increasing the maximum NTF gain degrades stability and increases sensitivity to clock-jitter.

3.1.5 Maximum Stable Amplitude

The internal quantizer is overloaded if its input is greater than its full-scale reference voltage. Under these conditions, the feedback loop is broken and the internal nodes of the modulator saturate, leading to instability. Hence, the maximum input that can be applied to the ADC must be smaller than the quantizer range and is termed as maximum stable amplitude (MSA). MSA can be increased by increasing the quantizer resolution or reducing the aggressiveness of the noise-shaping.

3.2 System-level Parameters

The target specifications for the low-power, wide bandwidth CT ΔΣ ADC implemented in IBM 90nm CMOS technology in this work are listed in Table 2.

Table 2. Target specifications for the wide bandwidth CT ΔΣ ADC

Performance parameter	Specification
Signal bandwidth	20MHz
Peak SNR/ Effective no. of bits (ENOB)	74dB/12-bit
Power consumption	< 20mW
Clock-jitter tolerance	≤ 7ps rms

The MATLAB ΔΣ toolbox was used to obtain an optimum noise transfer function (NTF) that satisfied the desired specifications. The system-level variables which are available to perform this optimization in the design space are order of the modulator (L), oversampling ratio (OSR), quantizer resolution (N) and maximum NTF gain (NTF_{max}). The total noise contribution at the input of the ADC is due to quantization noise, circuit noise (thermal and flicker), noise due to DAC clock-jitter, amplifier non-linearity and distortion and DAC non-linearity. Assuming that 15% of the total noise contribution is due to the quantization noise, the target SQNR should be approximately 78-80dB.

3.2.1 NTF Realization

In order to reduce noise contribution due to DAC clock-jitter, a novel hybrid DAC scheme using switched-capacitor techniques has been proposed in this work which is explained in great detail in Section 4. However, settling time requirements on the first integrator stage of the loop filter with reasonable power consumption limited the sampling frequency to 400MHz. From (2.5), this value corresponds to an OSR of 10. It was determined through simulations that with an OSR of 10, a 5^{th} order modulator is required to achieve the desired SQNR.

With the modulator order and OSR now fixed, a parametric simulation was performed to determine the optimum values for NTF_{max} and quantizer resolution based

on the system-level considerations discussed in Section 3.1. Figure 10 illustrates a 3-D plot of the peak SQNR vs NTF_{max} and number of quantizer levels. The achievable MSA vs NTF_{max} and quantizer levels is shown in Figure 11.

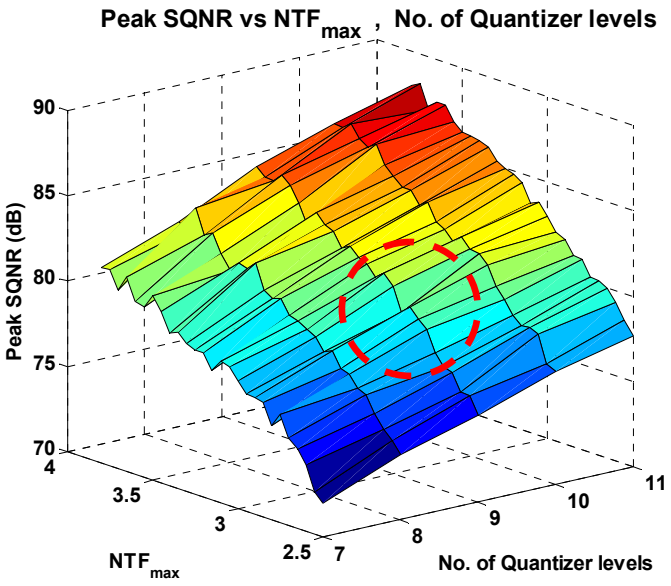


Figure 10. Peak SQNR vs. NTF_{max} and no. of quantizer levels

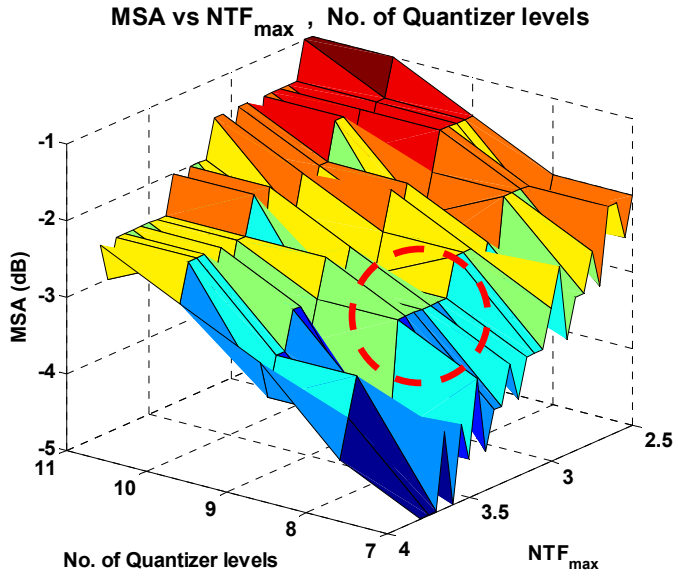


Figure 11. MSA vs. NTF_{max} and no. of quantizer levels

The NTF obtained from the MATLAB ΔΣ toolbox realizes NTF zeros with infinite quality factors. For practical realization, it is desirable to implement NTF zeros with low quality factors in order to minimize the sensitivity to saturation of the internal nodes and also, to minimize sensitivity to PVT variations. The following relationships were applied to the biquadratic terms in the NTF to realize NTF zeros with finite quality factors.

$$\alpha T_s = -\frac{\beta T_s}{\sqrt{4Q^2 - 1}} \tag{3.1}$$

$$r = e^{\alpha} \tag{3.2}$$

$$\begin{aligned} \text{Biquad term} \rightarrow & \left(z - re^{j\beta}\right)\left(z - re^{-j\beta}\right) \\ & = z^2 - (2r\cos\beta)z + r^2 \end{aligned} \tag{3.3}$$

where α maps the z-vector to a point inside the unit circle in the z-plane, β is the normalized NTF zero frequency, Q is the quality factor of the biquad and T_s is the sampling period. A 5th order modulator is realized using two biquadratic sections and a single first order integrator. Using the values for L, OSR, N and NTF_{max} as explained above, a parametric simulation is performed by varying the Q values of the two biquads and calculating the corresponding maximum achievable SQNR as shown in Figure 12. It can be observed that the Q values can be reduced to as low as 2 while still achieving 80dB SQNR. To provide some design margin, Q values of 4 and 3 were chosen for the 10.8MHz and 18.1MHz biquads, respectively. Figures 13 shows the variation of MSA with the Q values of the biquads.

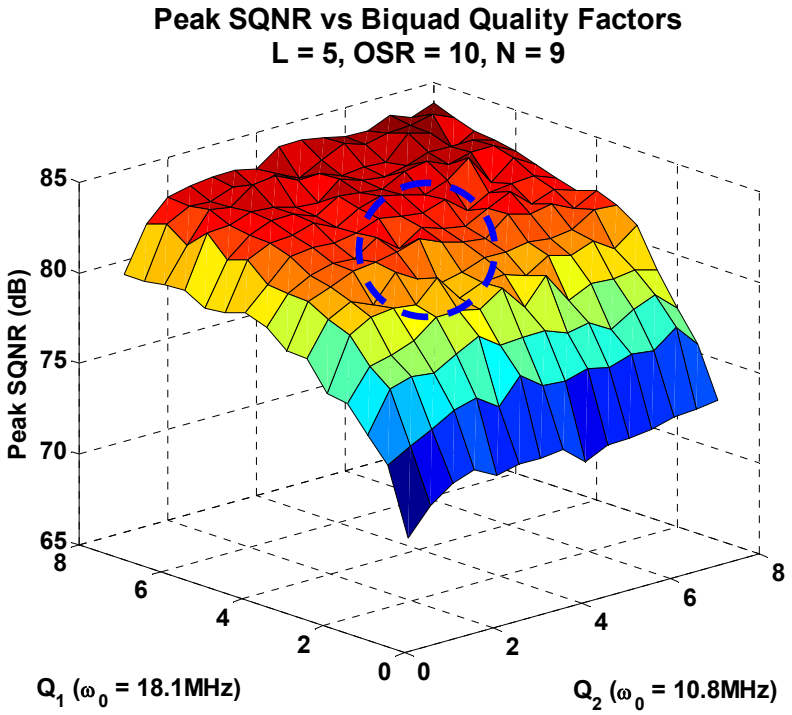


Figure 12. Peak SQNR vs. biquad quality factors

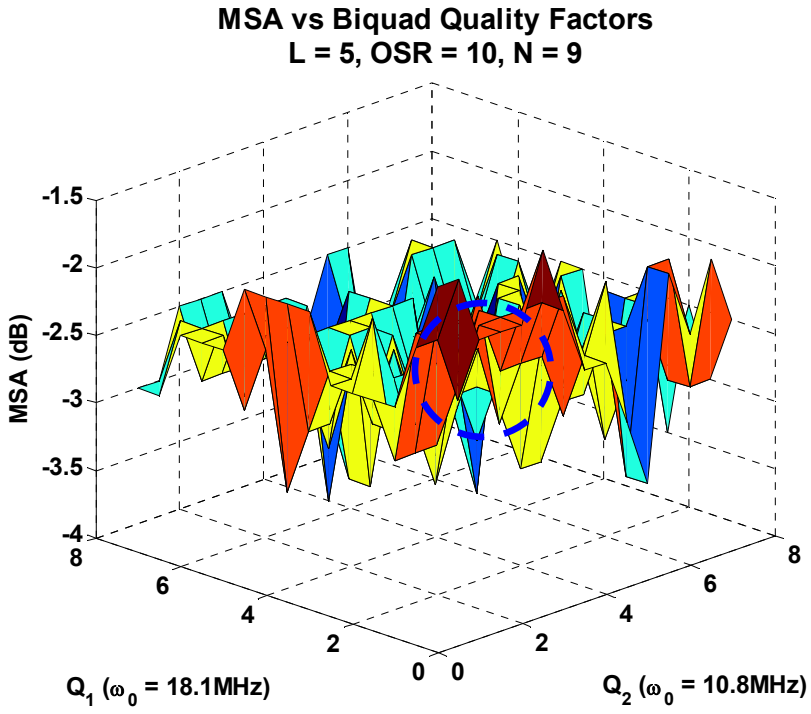


Figure 13. MSA vs. biquad quality factors

The variation of NTFmax with biquad quality factors is shown in Figure 14.

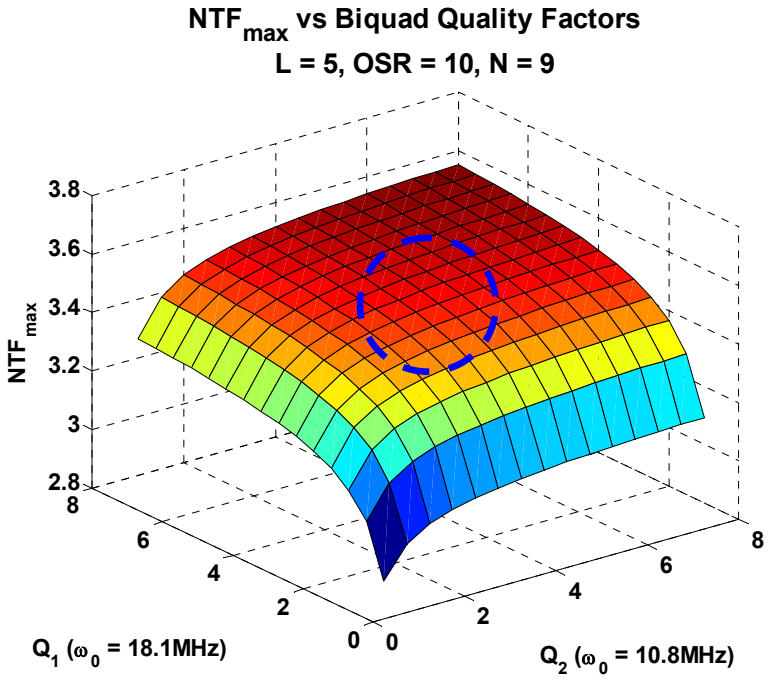


Figure 14. NTF_{max} vs. biquad quality factors

Table 3. System-level parameters for the proposed CT ΔΣ ADC

Parameter	**Value**
Sampling Frequency	400MHz
OSR	10
Signal Bandwidth	20MHz
Order	5
Quantizer levels	9
Peak SQNR	84dB
NTF_{max}	3.5
MSA	-3dBFS

The desired region of operation for the system is also indicated in Figures 10-14. The NTF parameters that results in the desired SQNR are summarized in Table 3. The magnitude response of the NTF is shown in Figure 15.

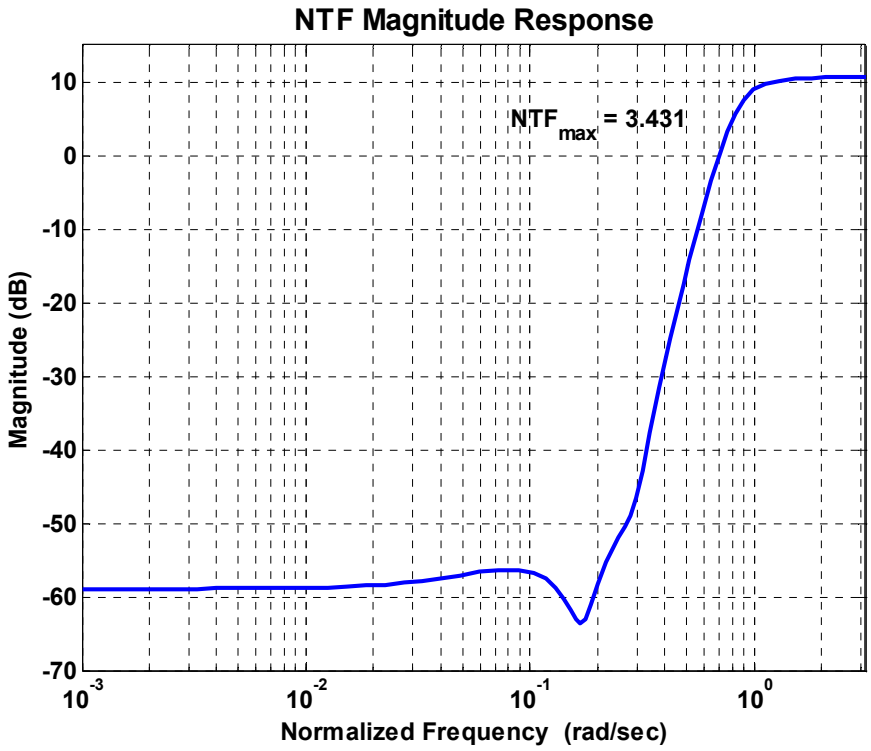


Figure 15. Noise transfer function magnitude response

The discrete-time noise transfer function NTF(z) is given by,

$$\mathrm{NTF}(z) = \frac{(1-0.95z^{-1})(1-1.93z^{-1}+0.95z^{-2})(1-1.83z^{-1}+0.91z^{-2})}{(1-0.45z^{-1})(1-0.91z^{-1}+0.26z^{-2})(1-1.06z^{-1}+0.58z^{-2})} \quad (3.4)$$

NTF(z) represents a 5th-order inverse-chebyshev high-pass filter with a real pole at 3MHz and two pairs of complex poles at 10.1MHz and 18.1MHz with Q values of 4 and 3, respectively. The discrete-time loop filter transfer function L(z) can be calculated from NTF(z) using the relationship,

$$L(z) = \frac{1}{NTF(z)} - 1 \tag{3.5}$$

Hence, the discrete-time loop transfer function is given by,

$$L(z) = \frac{(2.29z^{-1})(1 - 1.31z^{-1} + 0.45z^{-2})(1 - 1.44z^{-1} + 0.75z^{-2})}{(1 - 0.95z^{-1})(1 - 1.93z^{-1} + 0.95z^{-2})(1 - 1.83z^{-1} + 0.91z^{-2})} \tag{3.6}$$

Figure 16 plots the input amplitude vs SQNR of the 5th-order DT ΔΣ ADC implemented using the parameters in Table 3.

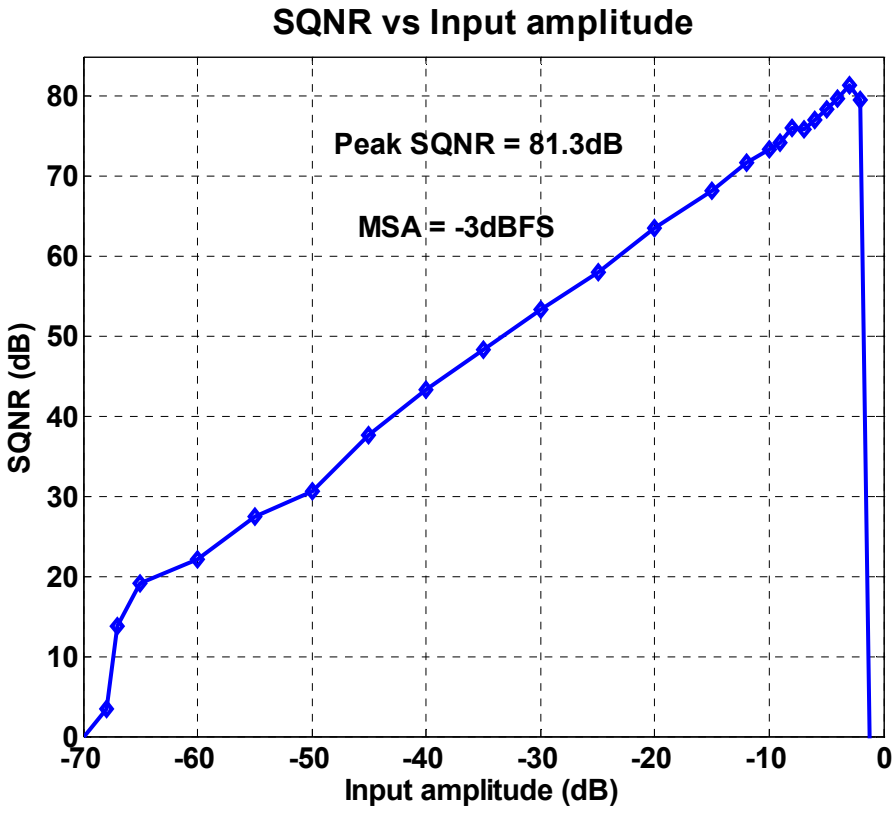


Figure 16. SQNR vs. input amplitude of the discrete-time ΔΣ modulator

As described in Section 2, excess loop delay causes a variation in the loop filter coefficients and may cause system instability. In order to compensate for ELD, the loop filter coefficients have to be adjusted depending on the amount of delay. The procedure to incorporate ELD during the computation of L(z) is described in [5], [17]. An excess loop delay of one clock cycle is considered in this design. The modified L(z) is obtained by factoring out one sample delay from (3.6) and is given as (3.7),

$$\begin{aligned} & L_2(z) \\ & = 2.29 \\ & + \frac{(4.49)(1 - 1.43z^{-1} + 0.53z^{-2})(1 - 1.57z^{-1} + 0.79z^{-2})}{(1 - 0.95z^{-1})(1 - 1.93z^{-1} + 0.95z^{-2})(1 - 1.83z^{-1} + 0.91z^{-2})} \end{aligned} \tag{3.7}$$

The constant term represents the coefficient of the feedback path around the quantizer as described in [17]. The latter part of the transfer function represents the discrete-time equivalent of the continuous-time loop filter transfer function which has to be realized. The procedure to obtain the continuous-time loop filter transfer function and the corresponding loop filter coefficients is described next.

3.3 DT-to-CT Transformation

3.3.1 Impulse-invariant Transformation

A DT ΔΣ modulator has a CT equivalent which can be obtained by performing a mapping from the z-domain to the s-domain. A DT ΔΣ modulator and its corresponding CT equivalent produce the identical sequences of output bits when the same inputs are applied to both modulators. This can be guaranteed if the inputs to their quantizers are the same at sampling instants [14], that is,

$$x(n)_d = x(t)|_{t=nT_s} = x(n)_c \tag{3.8}$$

The open-loop structures of the DT and CT ΔΣ modulators obtained by opening the loop at the DAC input is shown in Figure 17.

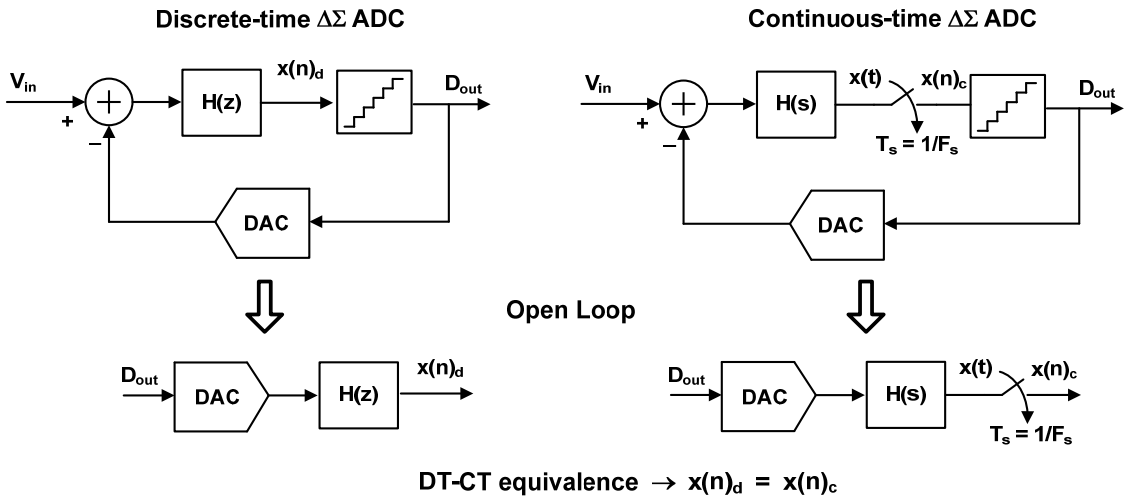


Figure 17. Open loop equivalence of DT and CT ΔΣ ADCs

(3.8) is satisfied if the impulse responses of the two structures in Figure 17 are equal. This result can be expressed in the frequency domain as,

$$Z^{-1}[L_2(z)] = L^{-1}[H_{DAC}(s)\,L(s)]|_{t=nT_S} \tag{3.9}$$

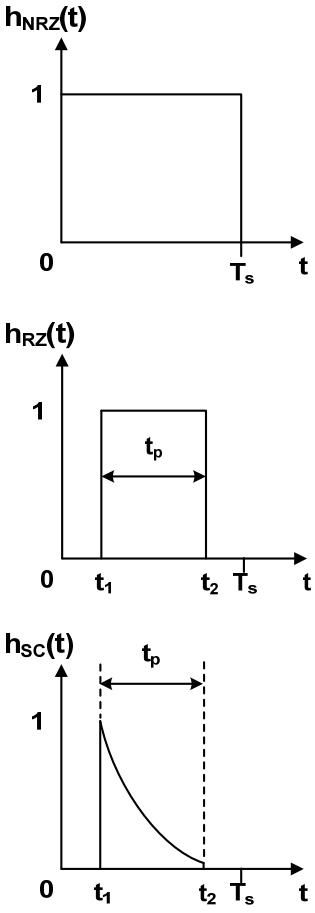
or in the time domain as,

$$l(n) = \{h_{DAC}(n) * l(t)\}|_{t=nT_S} \tag{3.10}$$

where $H_{DAC}(s)$ and $h_{DAC}(n)$ represent the s-domain transfer function and impulse response of the DAC, respectively. Since this transformation yields identical impulse responses in the DT and CT domains, it is called impulse-invariant transformation.

3.3.2 DAC Pulse Shapes

It can be observed from $H_{DAC}(s)$ term in (3.9) that the loop transfer function depends on the type of DAC pulse shape. Hence, the NTF of a CT ΔΣ ADC is determined by the type of the DAC pulse shape and affects ADC performance. In a DT ΔΣ ADC, the feedback signal is applied by charging a capacitor to a reference voltage and discharging it onto an integrating capacitor in the loop filter. On the other hand, the feedback signal is continuously integrated over time in a CT ΔΣ ADC and hence, the ADC is sensitive to any deviation of the feedback signal from its ideal value [15]. Some commonly used DAC impulse responses and their Laplace transforms are illustrated in Figure 18.



$$h_{NRZ}(t) = \begin{cases} 1, & 0 \le t \le T_S \\ 0, & otherwise \end{cases}$$

$$H_{NRZ}(s) = \frac{1 - e^{-sT_S}}{s}$$

$$h_{RZ}(t) = \begin{cases} 1, & t_1 \le t \le t_2 \\ 0, & otherwise \end{cases}$$

$$H_{NRZ}(s) = \frac{e^{-st_1}(1 - e^{-st_p})}{s}$$

$$h_{SC}(t) = \begin{cases} e^{-(t-t_1)/\tau}, & t_1 \le t \le t_2 \\ 0, & otherwise \end{cases}$$

$$H_{NRZ}(s) = \frac{e^{-st_1}\left(1 - e^{-st_p(s+1/\tau)}\right)}{\left(s + \frac{1}{\tau}\right)}$$

Figure 18. Common DAC impulse responses and Laplace transforms

Rectangular-shaped DAC pulse shapes are easier to implement. However, they are more susceptible to timing errors such as clock-jitter. Several recently reported work use exponentially-shaped DAC feedback pulses to improve tolerance to clock-jitter.

The continuous-time loop filter transfer function can be obtained from (3.7) by using the 'd2c' command in MATLAB. For a NRZ DAC pulse shape, the continuous-time equivalent of (3.7) is given by,

$$H(s) = 2.3 + \frac{(1.3\times10^{9})(s^{2}+2.5\times10^{8}s+2.1\times10^{16})(s^{2}+9.5\times10^{7}s+4.1\times10^{16})}{(s+2.1\times10^{7})(s^{2}+1.7\times10^{7}s+4.6\times10^{15})(s^{2}+3.8\times10^{7}s+1.3\times10^{16})} \quad (3.11)$$

The constant term represents the coefficient of the direct path around the quantizer. The second term in (3.11) represents the continuous-time loop filter transfer function.

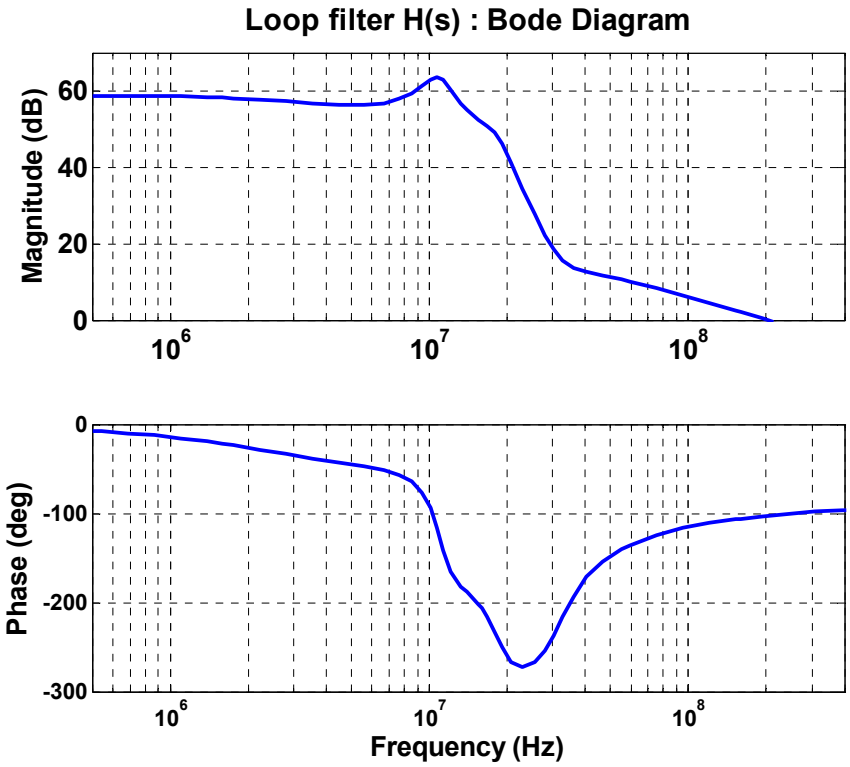


Figure 19. CT loop filter magnitude and phase responses

H(s) provides a DC gain of 58dB and a minimum in-band gain of 43dB which are sufficient to suppress quantization noise and other non-idealities. The magnitude and phase response of H(s) are shown in Figure 19.

3.4 CT ΔΣ ADC Architectures

Stability in a higher order loop filter can be achieved by using either feedforward or feedback architecture as shown in Figure 20.

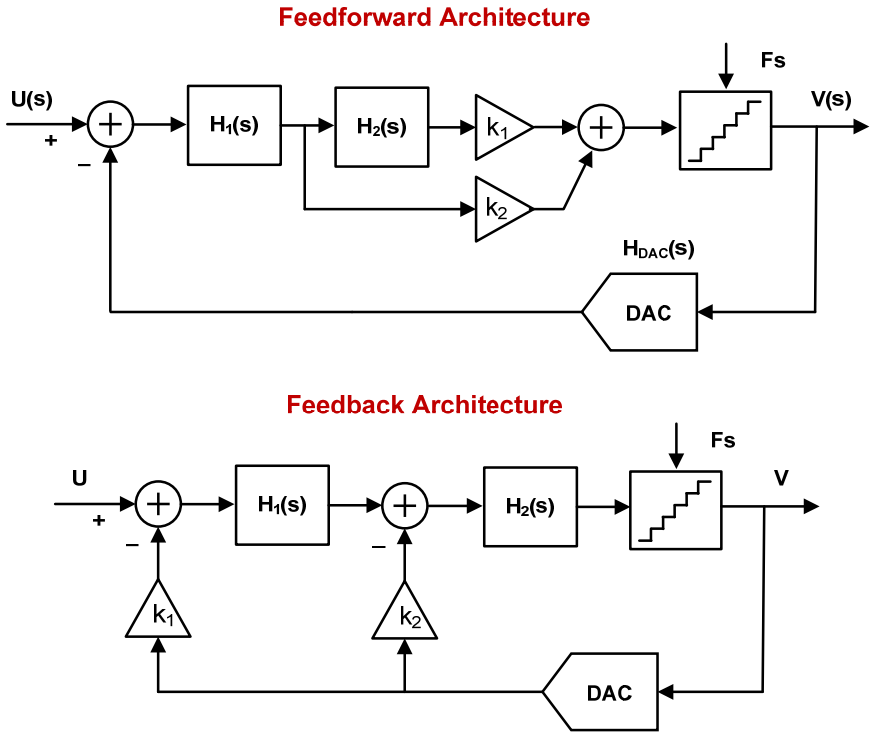


Figure 20. CT ΔΣ ADC architectures

In feedforward architecture, the input to the loop filter consists of primarily the quantization noise. Consequently, due to the lower internal signal swings, the first stage of the loop filter can have high gain and hence, noise and linearity requirements of the later stages can be relaxed resulting in a low power implementation. Additionally, only one feedback DAC is required which eases the complexity and area requirements.

However, the signal transfer function (STF) provides only 1st order attenuation for high frequency alias and also contains out-of-band peaking which reduces the stable input range of the modulator for adjacent channels. This loop filter architecture also requires a high speed summing stage which increases the power consumption significantly.

In comparison, in feedback architecture, each integrator output has a significant amount of input signal. To avoid clipping, lower integrator coefficients have to be used which translates to larger capacitors. Hence, the first stage can have only a moderate gain which necessitates higher bias currents in the later stages to as to reduce their input-referred noise and non-linearity contribution. This architecture required multiple feedback DACs to implement the loop filter, thereby increasing system complexity. However, an Nth-order filter implemented in feedback architecture provides Nth-order attenuation to high frequency blockers.

In this work, feedforward architecture was chosen due to its low implementation complexity.

3.5 Loop Filter Implementation

A block diagram representation of the 5th-order continuous-time loop filter with feed-forward architecture is shown in Figure 21.

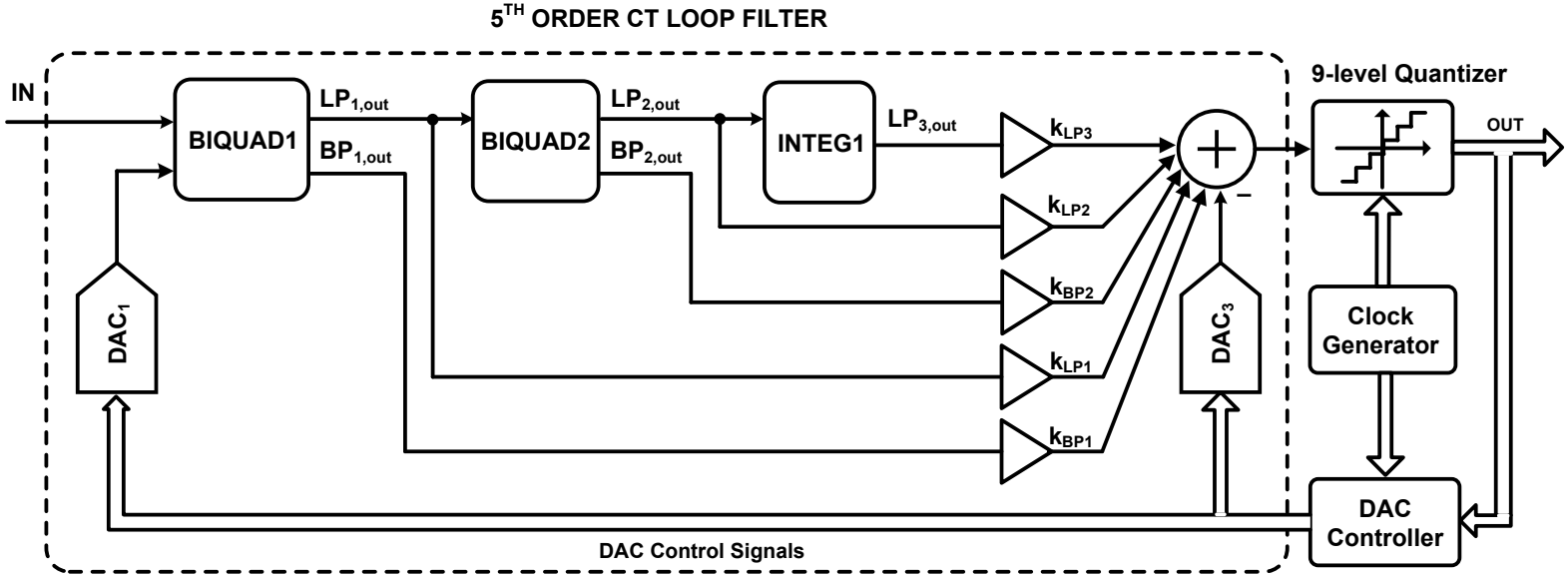


Figure 21. 5th-order CT loop filter with feedforward architecture

The 5th-order filter can be realized by cascading two biquadratic sections and a single first order lossy integrator stage. Multiple feed-forward paths are tapped from the outputs of each integrator stage, weighed and summed using a summing amplifier. The performance requirements of the loop filter are summarized in Table 4.

Table 4. Performance requirements of the CT loop filter

Block	**Order**	**DC Gain dB**	**Cut-off freq. MHz**	**Q**	**IM3 dB**	**SNR dB**
BIQUAD1	2	20	18.4	3	-78	74
BIQUAD2	2	20	10.8	4	-60	60
INTEG1	1	19	3.2	-	-60	60
Filter	5	59	20	-	< -76	72

The quality factors for the biquads are chosen to minimize sensitivity to saturation at internal nodes for step changes in the input signal and for practical realization. The gain in the first stage is chosen as a tradeoff between the requirement to suppress noise (thermal and flicker) and distortion of the subsequent stages. The first stage also has the maximum bandwidth in order to suppress thermal noise from the later stages. The overall input referred noise of the filter is designed to be dominated by the input resistance of the loop filter and the first integrator. The amplifiers in the loop filter also need to have minimum possible excess phase to minimize the excess loop delay.

The first integrator stage is the most critical to the overall performance of the ADC since errors introduced at its input appear directly at the digital output of the modulator without any suppression and limit the overall resolution of the ADC. In order to satisfy noise and linearity specifications, the first op-amp has the largest power consumption in the entire filter. The summing amplifier is on the direct path around the quantizer and hence, is a critical component to loop stability and is also expected to consume large power.

The 5th-order noise-shaping loop filter is realized using active-RC integrators implementing two biquadratic sections with complex poles and a first order lossy integrator section implementing a low frequency pole. The Tow-Thomas biquadratic filter structure is used to realize each second order section as shown in Figure 22. The SIMULINK model used to emulate the second order section is also shown in Figure 23.

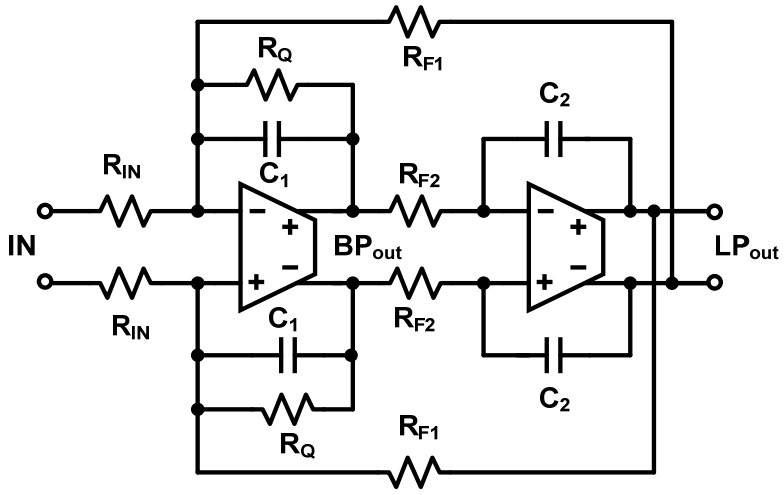


Figure 22. Biquadratic section implementing complex NTF zero

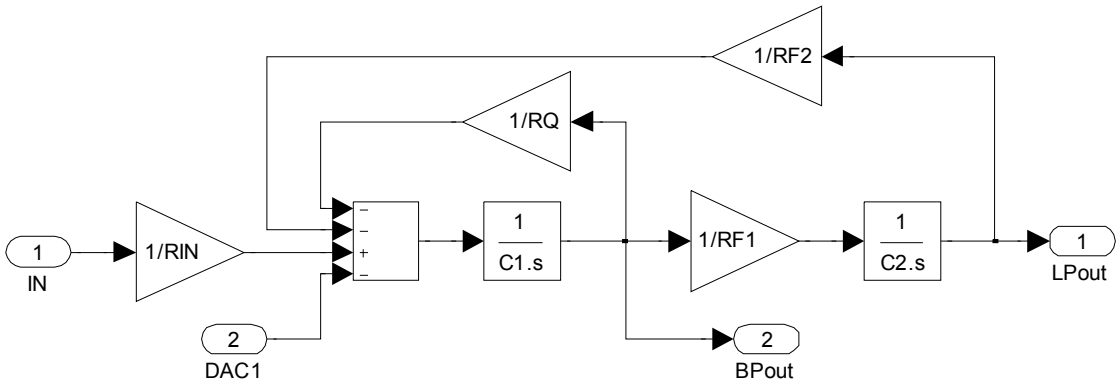


Figure 23. SIMULINK block diagram of biquadratic section

The transfer functions from the input to the low-pass and band-pass outputs of the biquad are given as,

$$H_{LP2}(s) = \frac{(R_{F1}/R_{IN})}{1 + sC_2\frac{R_{F1}R_{F2}}{R_Q} + s^2C_1C_2R_{F1}R_{F2}} \tag{3.12}$$

$$H_{BP2}(s) = \frac{sC_2R_{F2}(R_{F1}/R_{IN})}{1 + sC_2\frac{R_{F1}R_{F2}}{R_Q} + s^2C_1C_2R_{F1}R_{F2}} \tag{3.13}$$

The component values can be determined using the relationships given by,

$$\omega_0 = \sqrt{\frac{1}{R_{F1}R_{F2}C_1C_2}} \tag{3.14}$$

$$Q = \frac{R_Q}{\sqrt{R_{F1}R_{F2}}}\sqrt{\frac{C_1}{C_2}} \tag{3.15}$$

$$A_{DC} = \frac{R_{F1}}{R_{IN}} \tag{3.16}$$

where ω_0, Q and A_{DC} are the resonant frequency, quality factor and DC gain of the biquad, respectively. Using (3.14)-(3.16), the component values used in the two biquads are calculated as shown in Table 5.

Table 5. Component values for the implementation of the biquads

Component Parameter	**Biquad 1** (ω_0 **= 18.4MHz, Q = 3)**	**Biquad 2** (ω_0 **= 10.8MHz, Q = 4)**
R_{IN}	865.8Ω	1.46kΩ
R_{F1}, R_{F2}	8.65kΩ	14.6kΩ
R_Q	25.9kΩ	58.6kΩ
C_1, C_2	1pF	1pF

The 1st-order section of the loop filter is implemented using a lossy integrator as shown in Figure 24.

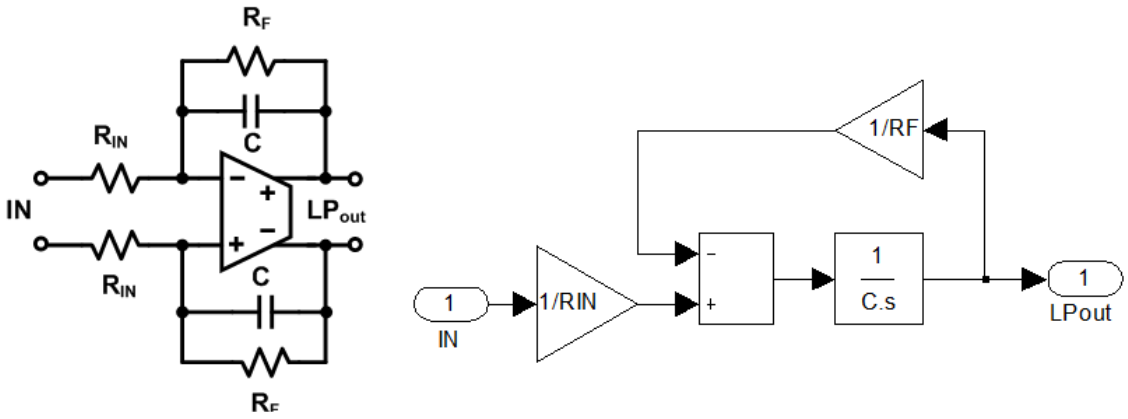


Figure 24. First order lossy integrator and SIMULINK model

The transfer function to the output of the integrator is given by,

$$H_{LP3}(s) = \frac{R_F}{R_{IN}}\left(\frac{1}{1 + sR_FC_1}\right) \tag{3.17}$$

The corner frequency (ω_0) and DC gain (A_{DC}) are given by,

$$\omega_0 = \frac{1}{R_F C_1} \tag{3.18}$$

$$A_{DC} = \frac{R_F}{R_{IN}} \tag{3.19}$$

Using (3.18)-(3.19), the component values for the 1st-order section can be obtained as shown in Table 6.

Table 6. Component values for the implementation of the 1st order lossy integrator

Parameter	**Value**
R_{IN}	5.47kΩ
R_F	48.7 kΩ
C	1pF

The SIMULINK model of the complete system consisting of the 5th-order continuous-time loop filter with feed-forward compensation paths, 9-level quantizer and DAC is shown in Figure 25.

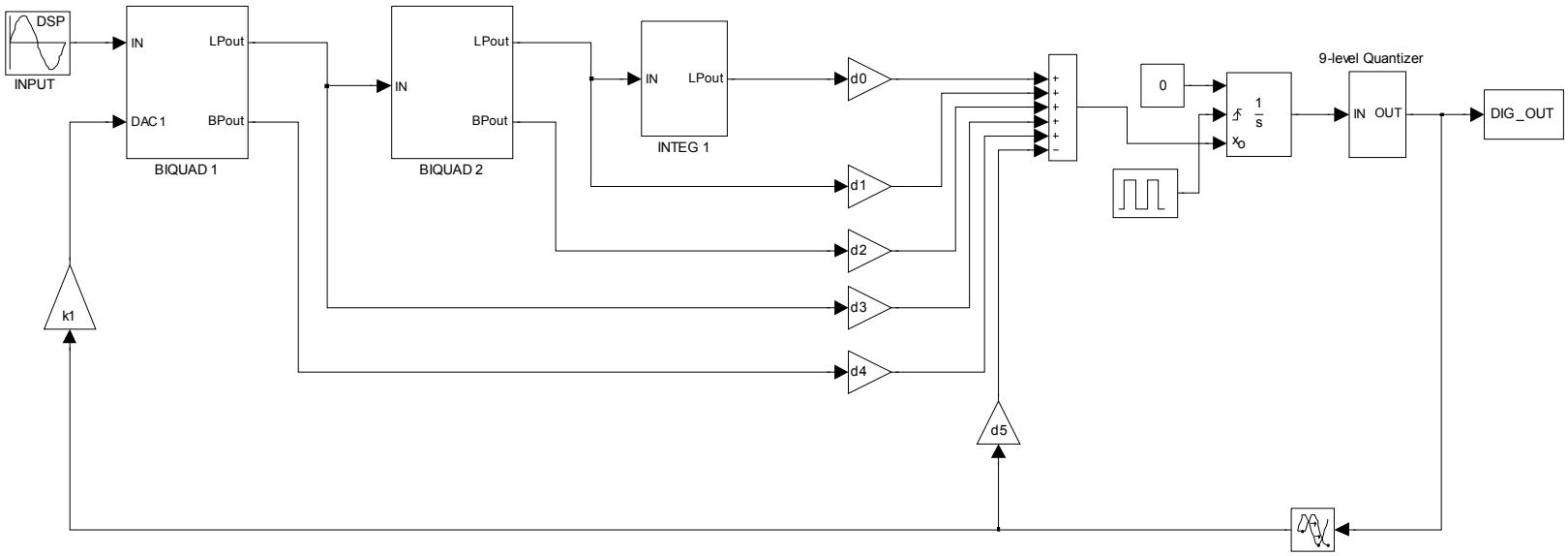


Figure 25. SIMULINK block diagram with NRZ feedback DAC

3.6 Synthesis of Loop Filter Coefficients

As described in Section (3.3), the CT equivalent of the DT loop filter can be calculated using equation (3.9) by assuming a specific DAC pulse shape. The method of impulse-invariant transformation can be applied to pulse shapes which have a simple frequency domain representation such as NRZ DAC pulse waveform. However, for more complex DAC pulse shapes such as SCR-DAC shown in Figure 18, manually manipulating the Laplace transforms is a tedious process. This method is even more substantially complex for higher order loop filters. For higher order loop filters, simulation-based design methodology proposed in [18] can be used. This method exploits the linear time-invariance property of the CT loop filter. The total output response of any LTI system is the sum of its natural and forced responses. From (3.11), the denominator of the loop filter transfer function determines the natural response of the filter. Impulse –invariant transformation can be used to obtain the CT equivalent from the DT transfer function.

The numerator of the transfer function in (3.11) determines the forced response of the system. In case of a loop filter with feed-forward compensation, the summed output of multiple feed-forward paths contributes to the forced response of the system, which is different for various DAC pulse shapes.

Figure 26 shows the SIMULINK model of the 5^{th}-order CT loop filter for calculation of loop filter coefficients.

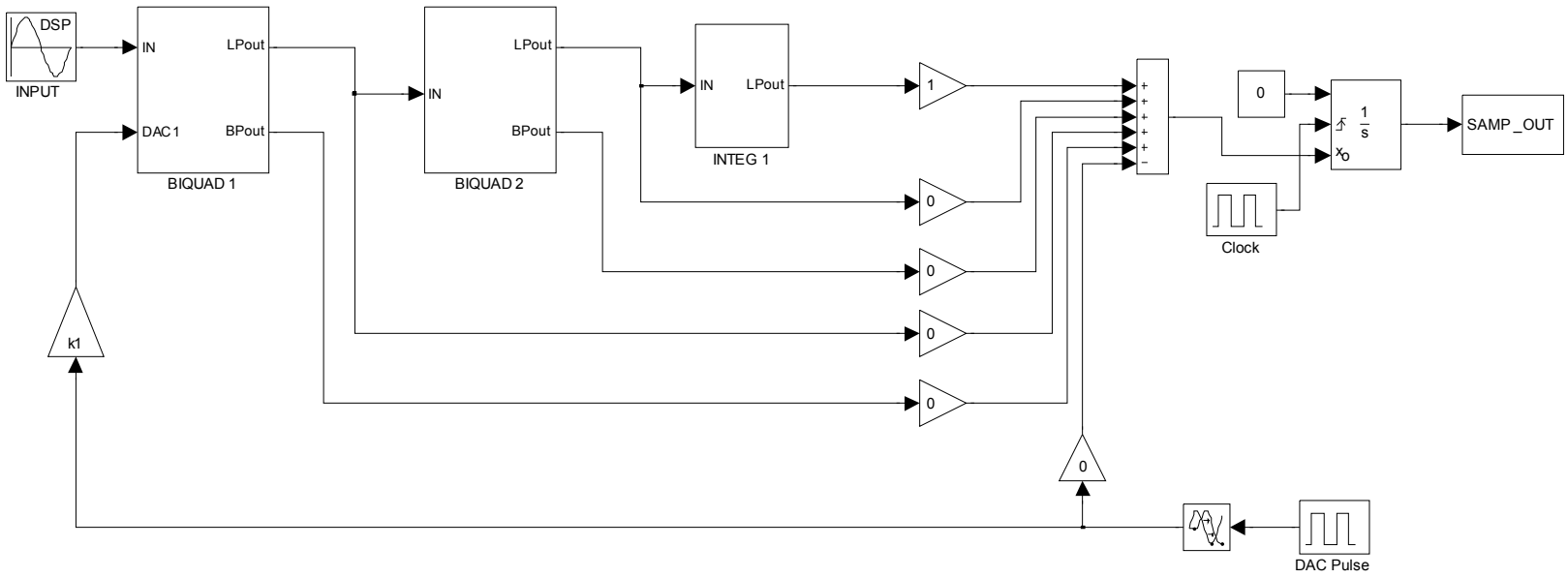


Figure 26. Simulink block diagram for calculation of loop filter coefficients

As shown in Figure 26, an n^{th}-order path consists of n-integrators from the DAC input to the input of the quantizer. Let $h_n(k)$ represent the impulse response of the n^{th}-order path and d_n represent the corresponding coefficient. Since the CT loop filter is an LTI system, the coefficients are independent of each other and the total impulse response of the system must be the equal to the linear combination of the impulse responses of each path, that is,

$$h(k) = \sum_{n=0}^{n=5} d_n h_n(k) \tag{3.20}$$

The impulse response $h_d(k)$ of the DT loop filter L(z) can be calculated from (3.20). Equating $h_d(k)$ and (3.20), a set of linear equations given by (3.21) can be constructed and solved to determine the loop filter coefficients d_n.

$$\sum_{n=0}^{n=5} d_n h_n(k) = h_d(k) \quad , \quad k = 0,1,2,3,4,5 \tag{3.21}$$

Table 7 lists the feed-forward coefficients calculated using the simulation-based synthesis technique.

Table 7. Feed-forward coefficients for the loop filter

Coefficient	**Value**
d0	0.74
d1	1.92
d2	0.98
d3	3.01
d4	1.12
d5	2.28

3.7 Verilog-A Modeling

The entire system was modeled using Verilog-A HDL to facilitate rapid porting of system-level design from SIMULINK to Cadence Design environment. Op-amps with a DC gain of 50dB and closed-loop bandwidth of 1GHz were found to be adequate to achieve the overall ADC specifications. The full-scale input of the system is 200mV (peak). The component values for the loop filter have been derived in Section 3.5. The component values for the summing stage of the loop filter are listed in Table 8. The feedback DAC is implemented using a NRZ pulse shape with a full-scale output current of 231μA. However, the actual implementation uses an exponentially-shaped DAC pulse as described in Section 4.

Table 8. Component values for the summing stage of the loop filter

Parameter	Value
R_1	6.75kΩ
R_2	2.61kΩ
R_3	5.11kΩ
R_4	1.66kΩ
R_5	4.46kΩ
R_F	5kΩ

The schematic of the complete system is illustrated in Figure 27.

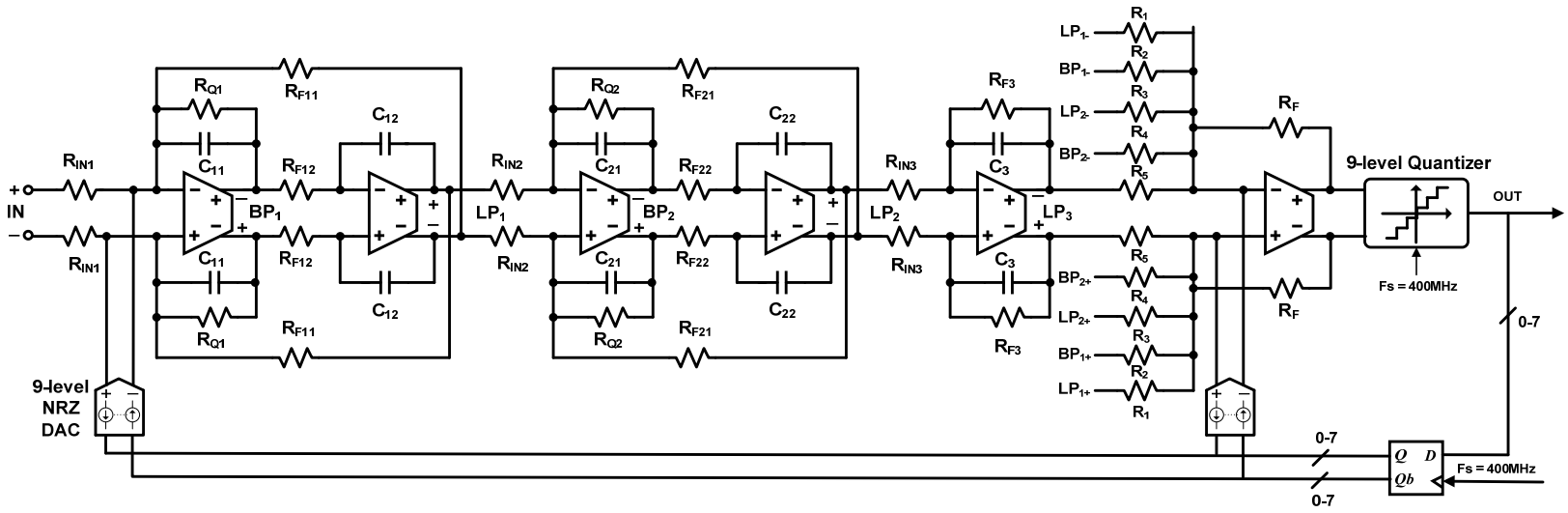


Figure 27. Schematic of the CT ΔΣ modulator

3.8 Simulation Results

The power spectral density of the proposed 5th-order ΔΣ ADC output is shown in Figure 28. The input signal is a -3dBFS sine wave at 4.88MHz. The SQNR over the 20MHz signal bandwidth is 82dB.

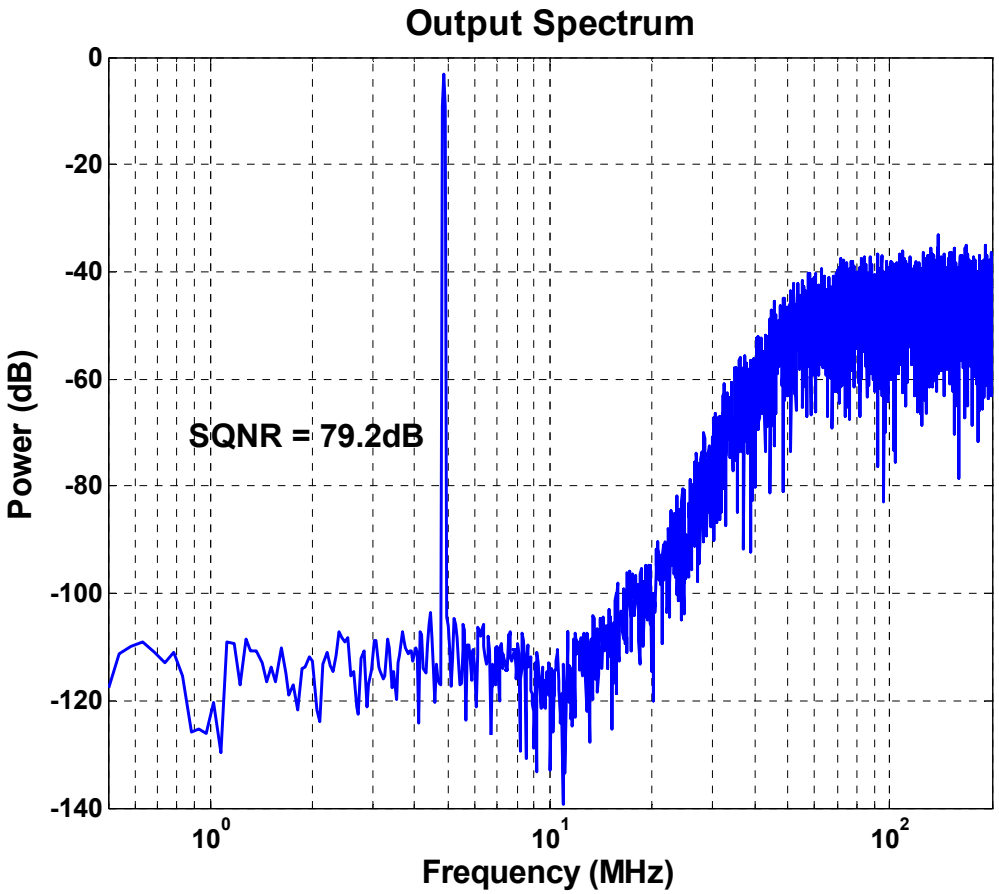


Figure 28. Modulator output spectrum for a -3dBFS in-band signal at 4.88MHz

4. CLOCK JITTER-TOLERANT HYBRID MULTI-BIT DAC

4.1 Introduction

Clock jitter causes the rising and falling edges of a clock signal to deviate from its ideal sampling instants. Timing errors in the clock cause an error in the sampling time and appears at the ADC output as a noise component. The power of these errors adds directly and raises the noise floor of the ADC output. Clock jitter limits ADC performance as the clock frequency is increased. This section discusses the effects of clock jitter in CT ΔΣ ADCs. A novel method is proposed to improve the clock jitter performance of the wideband ADC discussed in Section 3.

4.1.1 Clock-jitter in CT ΔΣ ADCs

The sources of jitter error in a typical CT ΔΣ modulator are shown in Figure 29. In a CT ΔΣ modulator, errors due to clock jitter can be modeled as error sources at the input of the quantizer and at the output of the feedback DAC.

In a CT ΔΣ ADC, the signal is sampled at the output of the loop filter and hence, sampling errors are indistinguishable from quantization noise and undergo noise-shaping. However, since the transfer function from the feedback DAC to the modulator output is same as the STF, jitter introduced into the system at the feedback DAC appears at the output without any noise-shaping and hence, degrades the SNR. The jitter noise power at the modulator output is dependent on the jitter variance and the magnitude of the DAC pulse at the clock transition.

The relevant forms of jitter for a rectangular-shaped feedback DAC pulse are shown in Figure 30 [19]. The clock phase-noise causes each clock edge to deviate from its nominal position, resulting in both pulse-width (PW) and pulse-position (PP) variations, depending on the frequency of the phase noise.

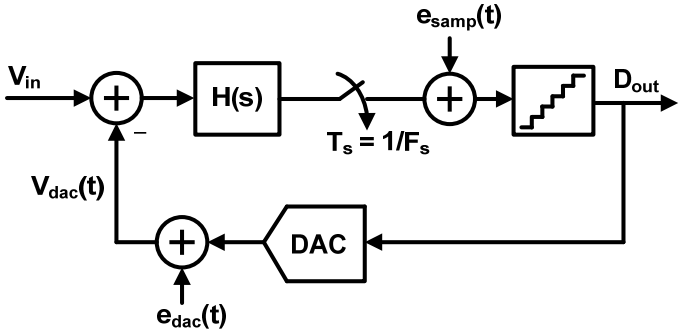


Figure 29. Sources of jitter-induced errors in a CT ΔΣ modulator

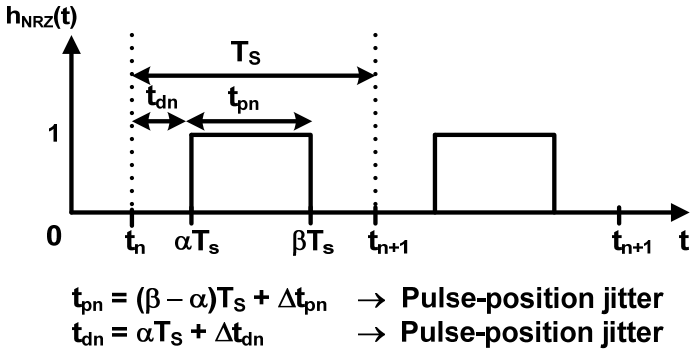


Figure 30. Clock-jitter errors for a rectangular feedback DAC pulse

Pulse-width (PW) jitter causes a random variation in the amount of charge fed back per clock cycle resulting in a voltage error at the output of the first integrator stage. This error is not noise-shaped and hence, is the dominant source of performance degradation due to clock jitter. PW variations are caused due to the wideband phase noise of the clock generator which modulates the high power density regions of the DAC input outside the signal bandwidth, mainly quantization noise and out-of-band ADC input signals, to within the signal bandwidth, thereby raising the total in-band noise.

Phase noise close to the clock frequency will be strongly correlated from one clock edge to another, thereby moving the position of a number of consecutive clock edges in the same direction with respect to the ideal sampling instants resulting in pulse position (PP) jitter. PP jitter results in a random variation in the integration interval of a

constant amount of charge. It was shown in [20] that the amplitude errors in the loop-filter caused by PP errors are at least 1st order noise-shaped.

4.1.2 SNR Limitation due to Pulse-width Jitter

The jitter noise power at the output of the modulator is dependent on the shape of the feedback DAC current waveform. Figure 31 depicts the pulse width jitter in a continuous-time modulator with switched-current (SI) and switched-capacitor (SC) DACs. In the SC-DAC, the variation of the amount of charge that is transferred per clock cycle due to the variation in timing is relatively low. However, in the SI-DAC case, this amount of charge varies linearly with the variation in timing. Consequently, the SI-DAC is more sensitive to clock jitter than the SC-DAC.

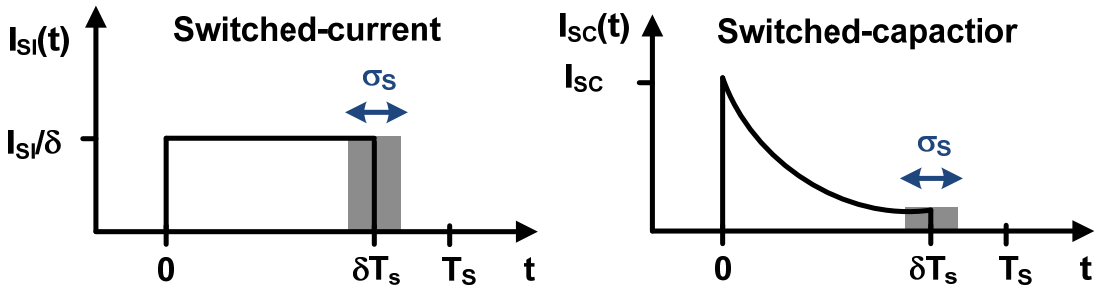


Figure 31. Pulse-width jitter error in SI and SC DACs

The SJNR in a CT ΔΣ ADC with SI-DAC and -3dBFS maximum input signal amplitude is given by [21],

$$\mathrm{SJNR_{SI}} = 10\log\left(\frac{\delta \cdot \mathrm{OSR}}{4 \cdot \mathrm{F_s^2} \cdot \sigma_s^2}\right) \tag{4.1}$$

where δ is the non-return-to-zero interval such that the return-to-zero interval is given as RZ = 1-δ, OSR is the oversampling ratio, F_s is the sampling frequency, σ^2_s is the

variance of the clock jitter. For a NRZ-DAC, the SJNR can be calculated by setting $\delta = 1$ in (4.1). For a RZ-DAC, $\delta < 1$ in (4.1) means that the SJNR for a RZ-DAC is lesser than that for a NRZ-DAC.

The SJNR in a CT ΔΣ ADC with SC-DAC and -3dBFS maximum input signal amplitude is given by,

$$\mathrm{SJNR_{SC}} = 10\log\left(\frac{\delta \cdot \mathrm{OSR}}{4 \cdot \mathrm{F_s^2} \cdot \sigma_s^2}\left(\frac{e^{\delta\cdot\alpha} - 1}{\delta \cdot \alpha}\right)^2\right) \tag{4.2}$$

where α is defined as,

$$\alpha = \frac{T_s}{\tau} \tag{4.3}$$

which gives the number of settling time constants $\tau = RC$ relative to Ts.

With constant OSR, time jitter, sample frequency and RTZ (return-to-zero) interval, the improvement from a switched current to SC feedback DAC is given by,

$$\Delta\mathrm{SJNR} = \mathrm{SJNR_{SC}} - \mathrm{SJNR_{SI}} = 20\log\left(\frac{e^{\delta\cdot\alpha} - 1}{\delta \cdot \alpha}\right) \tag{4.4}$$

(4.4) shows that the SJNR improvement is only dependent on the product of δ and α, which gives the effective settling of the DAC. Also, when $\tau << Ts$, $\alpha \to \infty$ and the SC current settles completely before the end of the clock cycle. Since PW jitter is completely eliminated in this case, an infinite improvement in SJNR is achieved.

Since the integrated feedback charge are equal for the SI and SC DACs, the peak feedback current for an SC DAC is significantly higher which imposes large slew rate and gain-bandwidth requirements on the op-amp used in the first integrator stage.

In this work, a hybrid multi-bit DAC is proposed which combines the advantages of clock jitter tolerance offered by SC-DACs and the relaxed slew rate and speed requirements of the SI-DACs.

4.2 Previous Work on Clock-jitter Tolerant CT ΔΣ ADCs

Several different techniques have been reported in literature to reduce the clock-jitter sensitivity in CT ΔΣ ADCs. A low power modulator with single-bit SC-DACs has been designed in [19], however, the input signal bandwidth is in the kHz range. A single-bit SC DAC for a GSM/UMTS receiver with up to 3.84MHz bandwidth and 4.5mW power consumption has been designed in [21]. However, the proposed technique is not suitable for a low OSR and wide-bandwidth CT ΔΣADC due to large power requirements in the loop filter. A 20MHz bandwidth CT band-pass modulator with 4-bit SC-DAC has been reported in [22], however, the power consumption exceeds 50mW. A switched-shaped-current (SSI) DAC has been proposed in [23] where the DAC pulse shape is similar to a SI-DAC during initial part of the clock cycle and exponentially decaying towards the end of the clock cycle, realized using capacitor discharge through a biased transistor. However, the method requires good control over process parameters for successful circuit implementation. A switched-capacitor-switched-resistor (SCSR) has been implemented in [24] at the expense of significant complexity and power consumption in the control circuits necessitating extensive tuning.

In addition to these techniques, system-level ideas have also been proposed in [25-26] to improve clock-jitter tolerance in CT ΔΣ modulators. A technique to filter out high frequency jitter noise in the feedback signals using FIR-DACs is proposed in [25]. However, these extra blocks add excess loop delay and increase the implementation complexity for a multi-bit DAC structure. An interesting approach to significantly reduce clock-jitter error is proposed in [26] where fixed-width pulses generated using digital logic is applied to the DAC. However, the effect of phase noise contribution from the digital logic needs to be investigated further.

4.3 Proposed Clock-jitter Tolerant Hybrid Scheme

4.3.1 Hybrid DAC Pulse Shape

As explained in Section 4.2, the SI-DAC implementation results in reduced peak feedback currents and relaxes the slew rate requirements on the amplifier used in the first integrator stage, with the optimal case being for a NRZ-DAC. On the other hand, SC-DAC imposes stringent design requirements on the amplifiers, however, offers excellent jitter performance. Hence, it can be concluded that with a hybrid (HYB) DAC pulse shape, it is possible to achieve the advantages of both SI-DACs and SC-DACs by shaping the feedback DAC pulse to behave as an NRZ-DAC for a portion of the clock period and as an SC-DAC for the remainder of the cycle. Figure 32 compares the pulse shapes for NRZ, SC and HYB DACs.

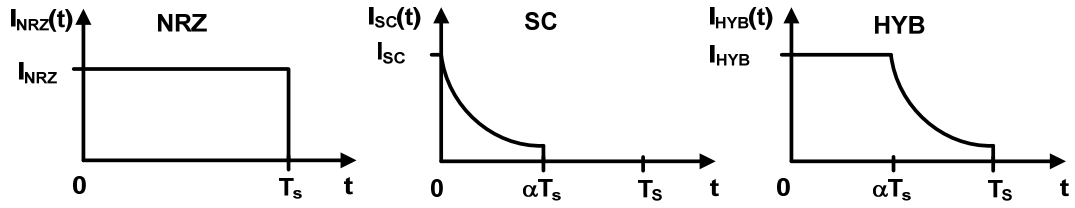


Figure 32. NRZ, SC and HYB DAC pulse shapes

The total feedback charge for an NRZ-DAC pulse is given by,

$$Q_{NRZ} = I_{NRZ} \cdot T_S \tag{4.5}$$

For a SC-DAC, the total feedback charge can be similarly calculated by integrating the current waveform from αT_s to T_s,

$$Q_{SC} = \int_{\alpha T_s}^{T_s} I_{SC} \cdot e^{-(t-\alpha T_s)/\tau} \cdot dt = I_{SC} \cdot \tau \cdot \left(1 - e^{-(1-\alpha)T_s/\tau}\right) \tag{4.6}$$

where $\tau = RC$ is the discharge time constant.

Similarly, for the proposed HYB-DAC, the total feedback charge can be calculated as,

$$\begin{aligned} Q_{HYB} &= \int_0^{\alpha T_s} I_{HYB} \cdot dt + \int_{\alpha T_s}^{T_s} I_{HYB} \cdot e^{-(t-\alpha T_s)/\tau} \cdot dt \\ &= I_{HYB}\left[\alpha T_s + \tau \cdot \left(1 - e^{-(1-\alpha)T_s/\tau}\right)\right] \end{aligned} \tag{4.7}$$

To assure the same gain from the input to the output of the modulator for various possible implementations of the feedback DAC, the integrated feedback charge must be identical, that is,

$$Q_{NRZ} = Q_{SC} = Q_{HYB} \tag{4.8}$$

Hence, the ratio of the peak SC and HYB current to the NRZ current can be obtained as,

$$\frac{I_{SC}}{I_{NRZ}} = \frac{T_S}{\tau \cdot (1 - e^{-(1-\alpha)Ts/\tau})} \tag{4.9}$$

$$\frac{I_{HYB}}{I_{NRZ}} = \frac{T_S}{\alpha T_S + \tau \cdot (1 - e^{-(1-\alpha)Ts/\tau})} \tag{4.10}$$

Assuming $\alpha = 0.5$ and $\tau = 0.1T_s$, (4.9)-(4.10) can be calculated as,

$$\frac{I_{SC}}{I_{NRZ}} = 10.07 \tag{4.11}$$

$$\frac{I_{HYB}}{I_{NRZ}} = 1.67 \tag{4.12}$$

It is apparent that from (4.9)-(4.10) that the peak HYB current is approximately 6 times smaller than the peak SC current. Moreover, the peak HYB current is only 1.6 times the peak NRZ current resulting in moderately higher slew rate and speed requirements on the amplifiers.

4.4 System-level Modeling of the HYB-DAC With Clock-jitter

The simplest method to characterize the clock-jitter performance of a CT ΔΣ ADC is to replace the ideal clock by a jittered clock with the required rms timing jitter. However, this method increases the simulation time drastically. An alternate and fast approach has been proposed in [27] where the jitter error is modeled as an error in the feedback charge injected by the DAC. For the HYB-DAC the error charge can be modeled changing the signal amplitude by a constant amount over the fixed window at the end of a clock period. The required change in signal amplitude is given by,

$$e_{j,HYB}(n) = y(t)|_{t=nT_s} \cdot \frac{\Delta t(n)}{T_S} \tag{4.13}$$

where y(t) is the DAC output signal.

The MATLAB model of the active-RC, 5th-order feed-forward CT ΔΣ ADC with the proposed clock-jitter tolerant HYB-DAC is shown in Figure 33. The HYB-DAC is modeled using pulse generators and a first order s-domain transfer function where ‘tau’ is the discharge time constant. The model was simulated for different amounts of clock-jitter and the corresponding SNR of the modulator output was calculated.

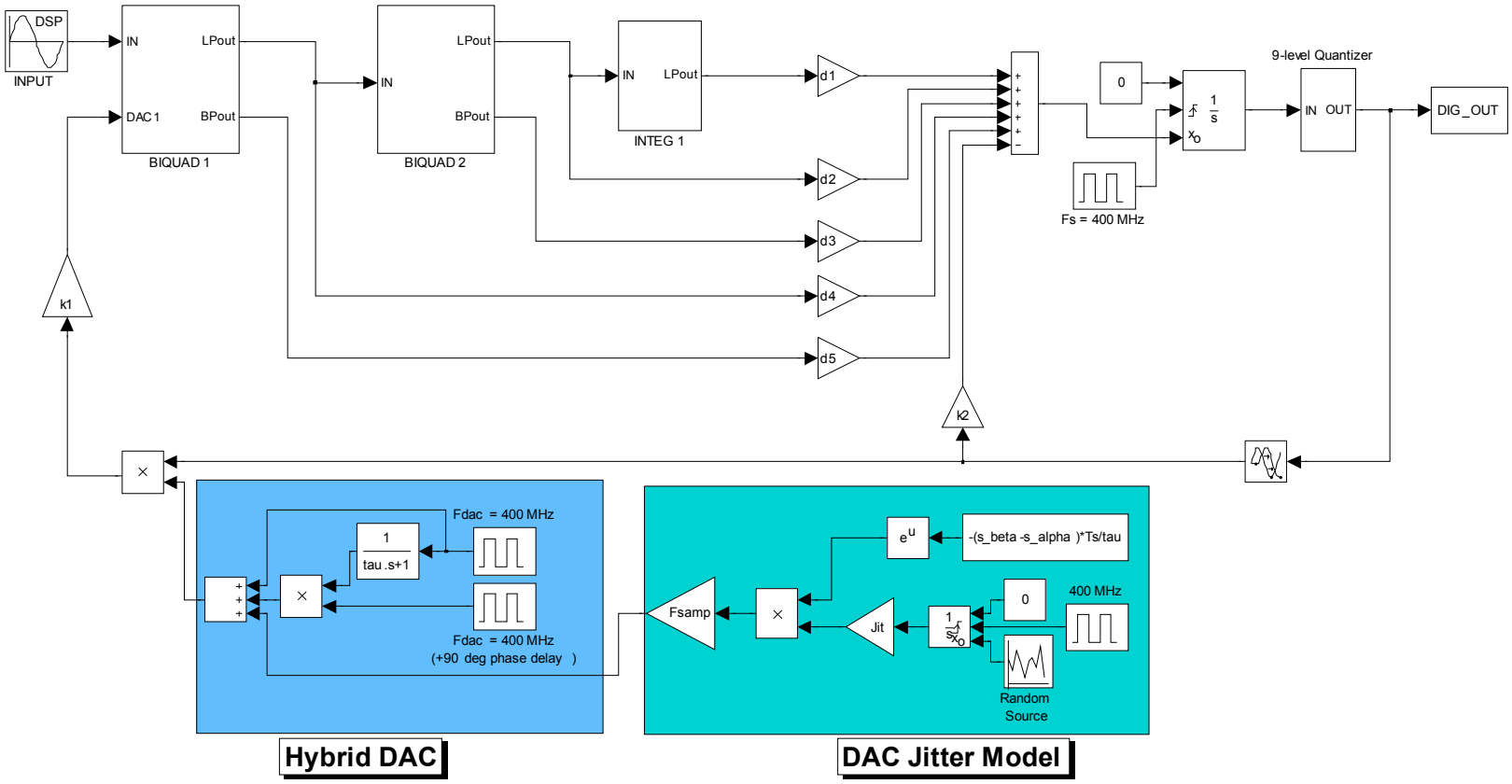


Figure 33. SIMULINK model of the clock jitter-tolerant CT ΔΣ ADC

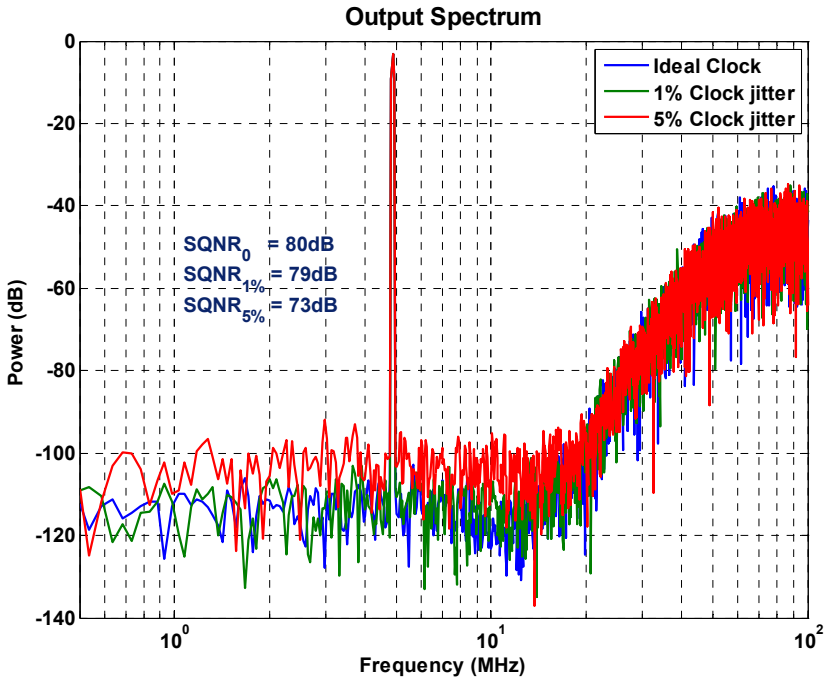


Figure 34. Output spectrum with and without clock jitter for hybrid DAC

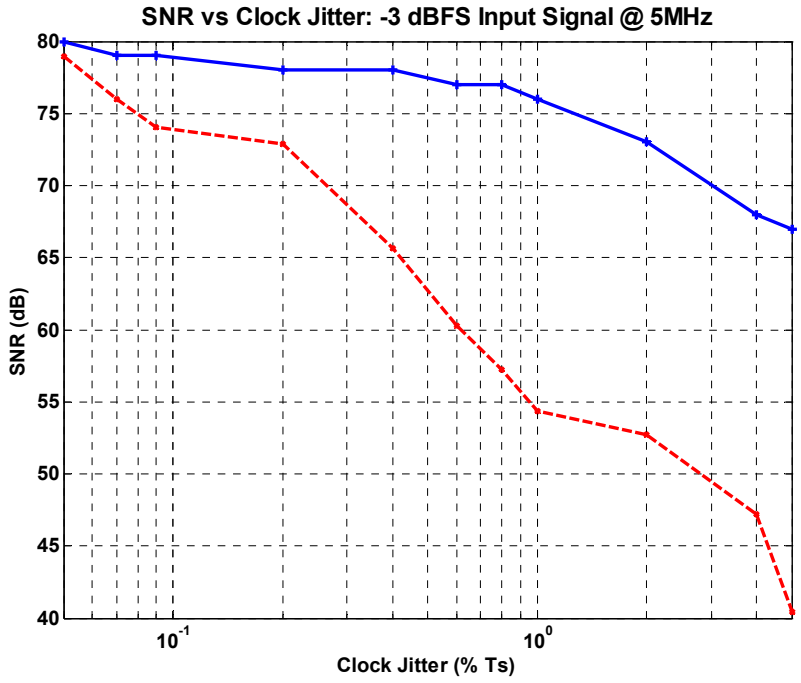


Figure 35. System-level performance of the clock jitter-tolerant hybrid DAC

Figure 34 compares the output spectra without clock-jitter and with 1% clock jitter. Figure 35 compares SNR vs % jitter for NRZ and HYB DACs. It can be observed that in case of HYB-DAC, there is only a marginal SNR degradation for up to 1% clock-jitter.

4.5 Circuit-level Implementation

4.5.1 DAC Architecture

The proposed multi-bit hybrid DAC with nine output levels is illustrated in Figure 36. Capacitors C_1, C_2, C_3 are binary-weighted in order to implement seven of the output levels of the DAC. The unit-weighted capacitor C_4 realizes the additional two levels of the DAC.

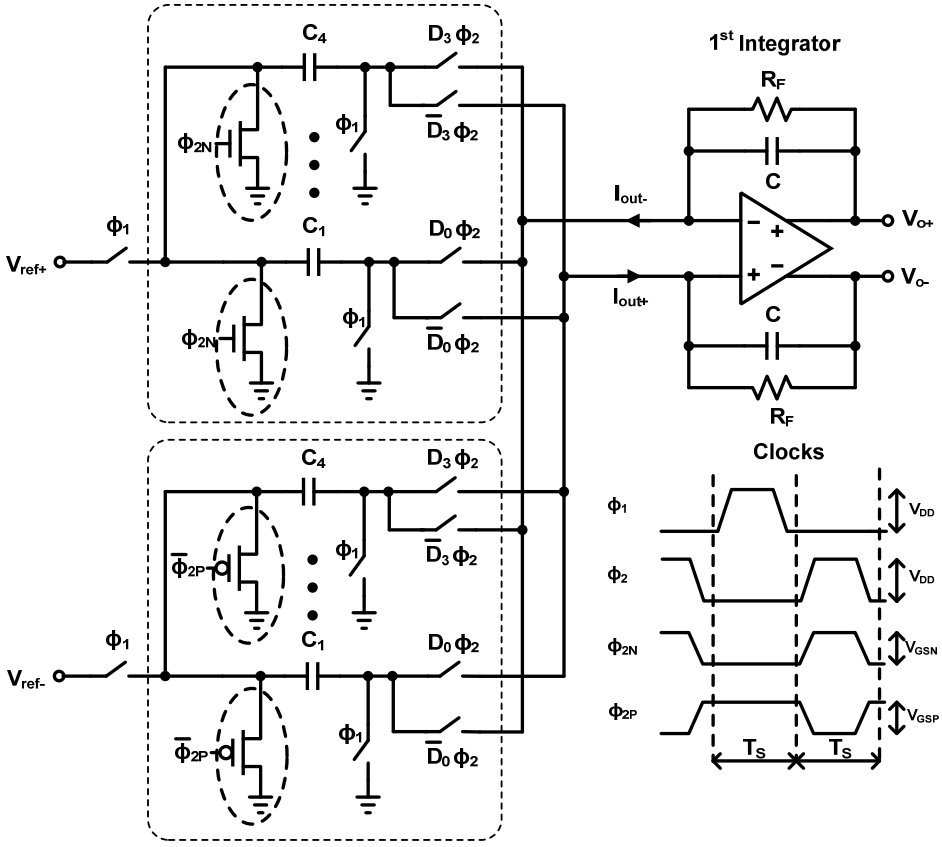


Figure 36. Multi-bit hybrid DAC architecture with one capacitor bank

As highlighted in Figure 36, NMOS and PMOS transistors are used to realize the fully-differential DAC current pulses since those switches operate as current sources for a portion of each discharge cycle. In traditional switched-capacitor circuits, half the clock cycle is used for charging the capacitors while the remaining half clock cycle is used for discharging the capacitors.

In order to reduce the peak currents of the switched capacitor pulse shape, it is desirable to increase the discharge time up to the entire clock cycle. Such a modification implies that multiple capacitor banks need to be used for the correct operation of the DAC. Using multiple capacitor banks provides an added advantage of randomizing the mismatches inherent in multi-bit digital-to-analog conversion. Hence, the proposed HYB-DAC scheme offers inherent dynamic element matching (DEM) that improves overall DAC linearity. DEM is discussed in detail in Section 5 where another multi-bit DAC design for a wideband CT ΔΣ modulator is discussed.

A DAC controller circuit ensures that only one bank of capacitors is selected during a given clock cycle. Capacitor banks are charged to the reference voltage when not selected by the controller.

The DAC coefficient is implemented by connecting the binary weighted capacitors to the inverting or non-inverting terminal of the op-amp to implement the relationship given by,

$$V_0(nT) = V_0(nT - T) - \sum_{i=1}^{4} A_{1i} V_{REF} \tag{4.14}$$

where A_{1i} (= $\pm C_i/C$) is the digital DAC input and R_F is large. When enabled by the DAC controller, the DAC capacitors are either coupled or cross-coupled to the first integrator depending on the binary data from the encoder.

The design of the switch highlighted in Figure 35 is now discussed. The proposed Hybrid DAC operation is obtained by strategically modifying the control signal to the Φ_{2N} switch. The basic principle of operation is depicted in Figure 37.

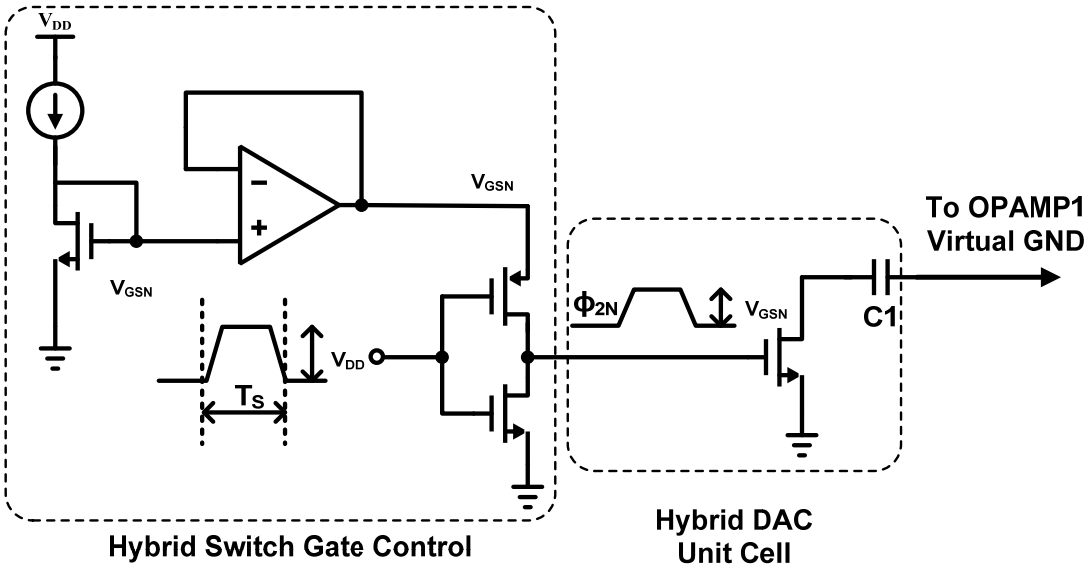


Figure 37. Hybrid DAC pulse shape generation

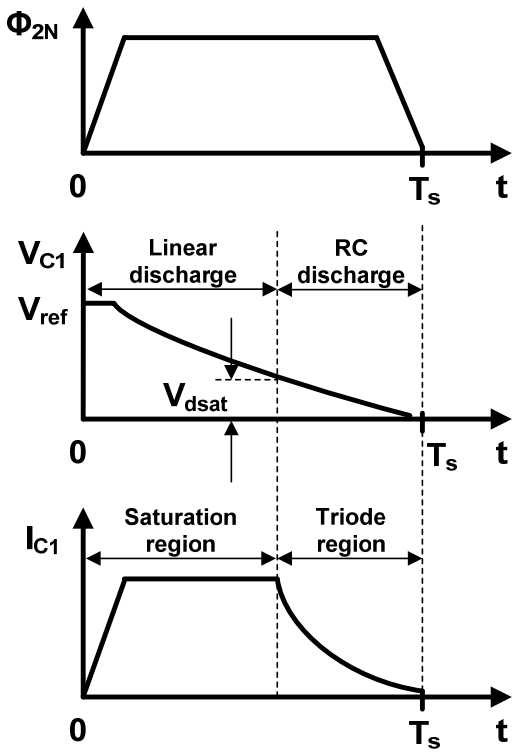


Figure 38. Operation of the hybrid DAC switch

The right hand side plate of C_1 is connected to the virtual ground of the op-amp corresponding to the first stage of the loop filter. The main concept is to maintain the operation of the transistor in saturation region (operating as a current source) while discharging the capacitor. For that reason, the gate of this transistor is switched between GND and V_{GSN}.

When Φ_{2N} goes high, the transistor is turned on and the capacitor starts discharging. As shown in Figure 38, for the time when the overdrive voltage of the NMOS transistor $V_{DSAT} = (V_{GSN}-V_t)$ is less than V_{REF}, the transistor operates in the saturation region and hence, behaves as a current-mode circuit, thereby limiting the peak current and discharging the capacitor linearly. This operation resembles the operation of the SI-DAC discussed earlier. When the capacitor voltage decays below V_{DSAT} of the Φ_{2N} transistor, it operates in the triode region and operates as a resistor. Thus, the current now discharges the capacitor C_1 exponentially. This scheme results in significantly lower peak currents than the traditional switched-capacitor DACs while also providing excellent jitter performance. Hence, this hybrid DAC combines the low jitter performance of Switched capacitor (SC) and lower peak current of non-return-to-zero (NRZ) DACs.

4.5.2 Design Considerations

The proposed CT ΔΣ ADC is implemented in a 1.2V, 90nm CMOS process. In a nanometric technology, severe channel length modulation and short channel effects degrade the output impedance of the native device. The proposed HYB-DAC scheme relies on the high output impedance of the switch transistor when operating as a current source and the triode region switch resistance to generate the exponentially decaying portion of the feedback DAC current. Hence, these switches must be designed appropriately. In order to reduce channel length modulation effects, a large length L is chosen for the transistor used to implement the hybrid switch. However, increasing the length of the transistor also increases its triode region resistance which may cause the feedback DAC current to not settle completely by the end of the discharge cycle, thereby

increasing the jitter noise power. Additionally, a larger L also increases the gate-source capacitance which would require larger power dissipation in the driver circuit. From simulations, a length of 0.5µm for the hybrid switch was found to be a good trade-off between the aforementioned issues.

The width of the transistor used in the hybrid switch can be determined using a setup consisting of a single transistor and the unit capacitor of the DAC with initial conditions of V_{REF} = 575mV across its plates. Using a fixed length of 0.5µm and a fixed gate-source voltage, the width of the transistor is swept and to generate the set of plots shown in Figure 39. A similar setup is used to determine the optimum dimensions of the PMOS transistor used to implement the hybrid switch, as shown in Figure 40.

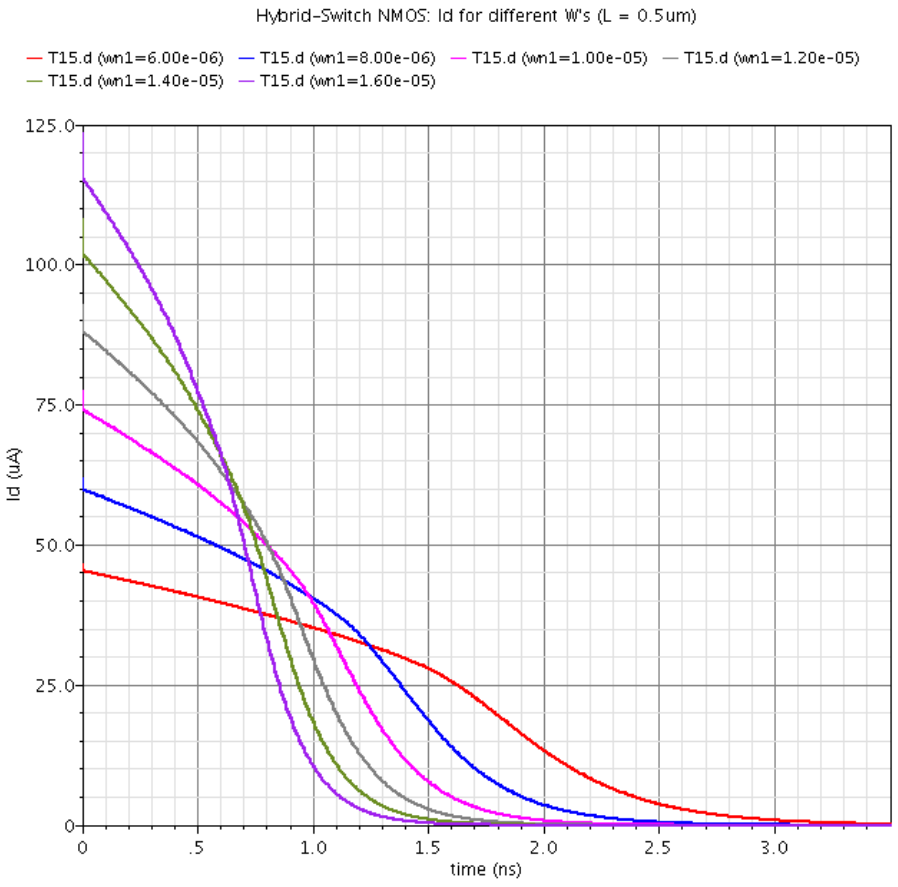


Figure 39. Determination of dimensions for the NMOS hybrid-switch

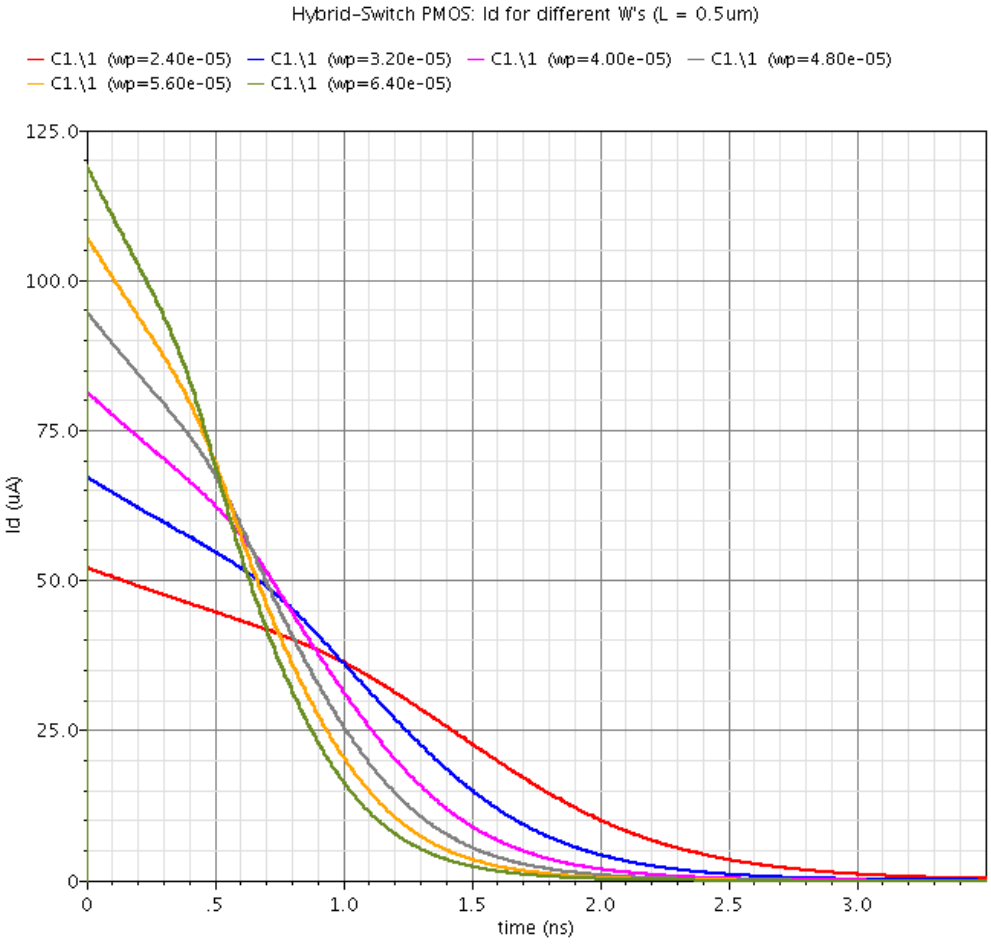


Figure 40. Determination of dimensions for the PMOS hybrid-switch

Table 9. Dimensions of NMOS and PMOS hybrid switches

Hybrid-switch type	**W / L**
NMOS	12um / 0.5um
PMOS	48um / 0.5um

Table 10. Multi-bit hybrid DAC design parameters

Parameter	Value
C_1, C_4	125fF
C_2	250fF
C_3	500fF
V_{cm}	600mV
V_{REF+}	V_{cm} + 575mV
V_{REF-}	V_{cm} - 575mV

Since the sampling frequency is 400MHz, it is desirable to discharge most of the capacitor voltage by the end of a clock cycle, that is, at 2.5ns. The dimensions of the NMOS and PMOS transistors used to implement the hybrid switches are listed in Table 9. The design parameters of the multi-bit hybrid DAC are summarized in Table 10.

4.6 Simulation Results

The proposed clock-jitter-tolerant multi-bit hybrid DAC was used to implement the 9-level feedback DAC for the active-RC, 5^{th}-order feed-forward compensation CT $\Delta\Sigma$ ADC discussed in Section 3. Figure 41 shows the schematic of the complete system. Since the feedback DAC should not inject any charge when its input is mid-rail, additional digital logic has been used in the feedback path. The full-scale input of the system is 200mV (peak).

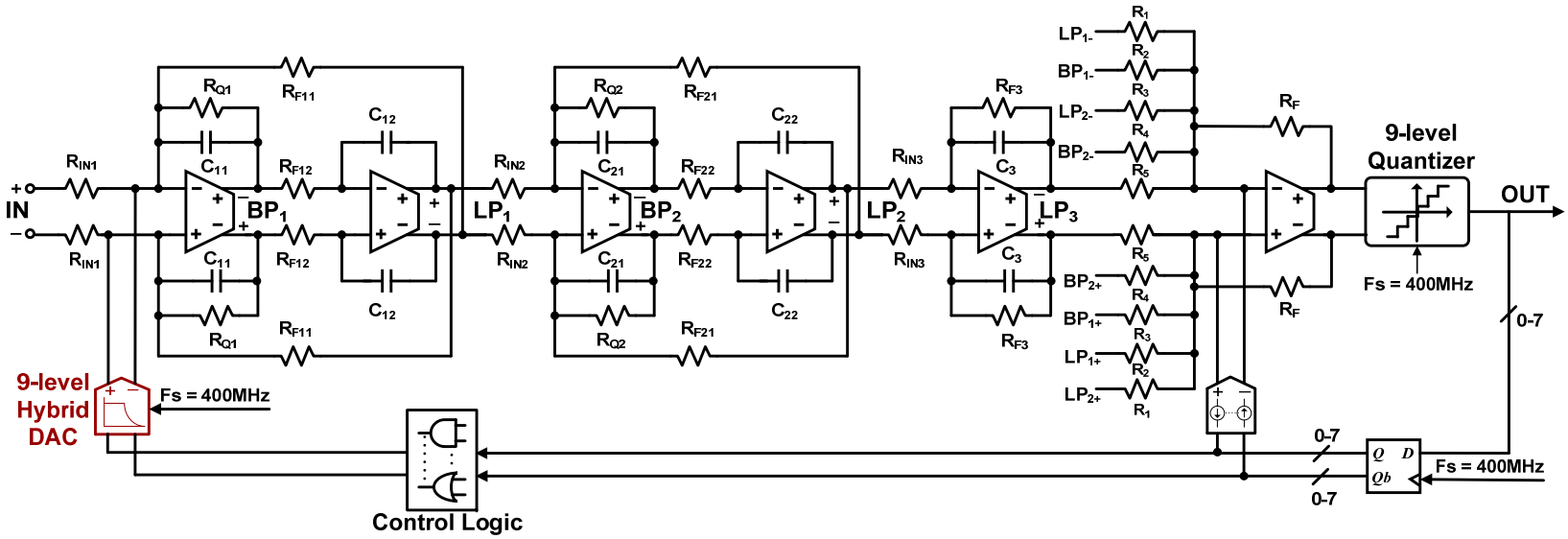


Figure 41. Schematic of the proposed clock-jitter tolerant 5th-order CT ΔΣ ADC

The component values for the loop filter have been derived in Section 3.5. The component values for the summing stage of the loop filter are listed in Table 11.

Table 11. Component values for the summing stage of the loop filter

Parameter	Value
R_1	6.75kΩ
R_2	2.61kΩ
R_3	5.11kΩ
R_4	1.66kΩ
R_5	4.46kΩ
R_F	5kΩ

Figure 42 illustrates the peak currents for various implementations of the feedback DAC. The results match closely with the theoretical analysis in Section 4.3. It is to be noted that to allow a fair comparison, the SC-DAC also has a discharge cycle equal to one complete clock period, although in conventional SC circuits, the discharge time is equal to half a clock cycle.

The SNR vs % clock jitter performance is characterized in Figure 43. It can be observed from Figure 43 that the proposed HYB-DAC improves the SNR by approximately 25dB when compared to NRZ-DAC for clock jitter up to 5ps (rms). The linearity of the HYB-DAC depends on the mismatches between the DAC capacitors. However, the use of multiple capacitor banks provides an inherent randomization. Moreover, capacitors can be matched to less than 0.05% (greater than 11 bits) through proper sizing and layout techniques.

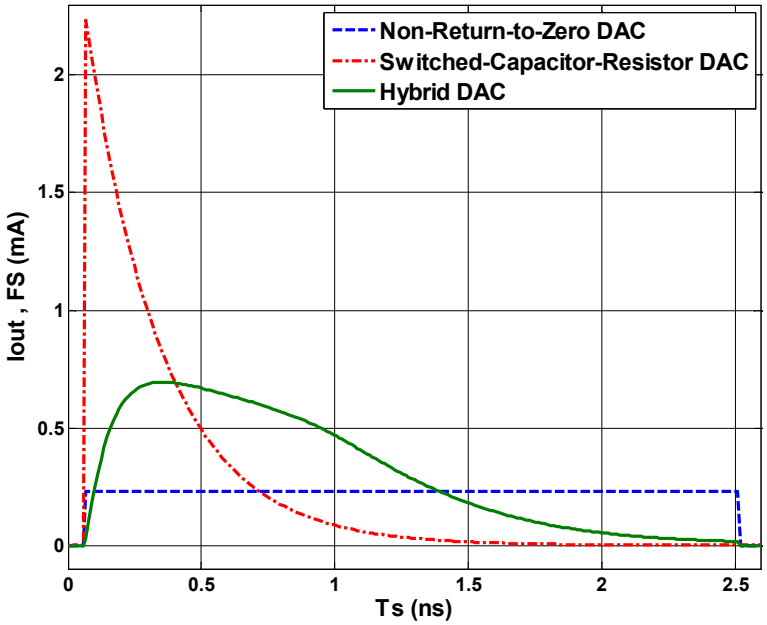


Figure 42. Comparison of DAC full-scale output currents

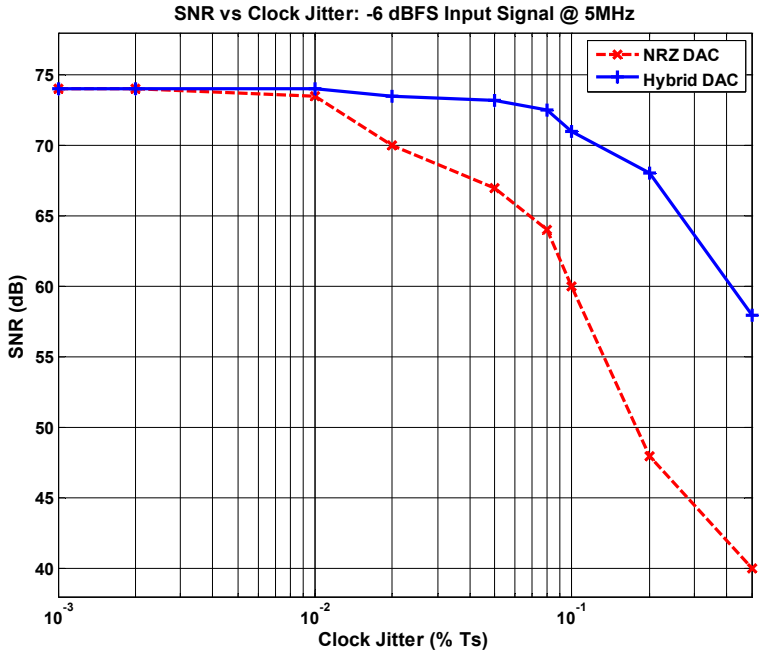


Figure 43. SNR vs. % jitter for NRZ and hybrid DACs

A plot of signal to noise ratio (SNR) and the signal to noise-plus-distortion ratio (SNDR) for various input signal amplitudes is shown in Figure 44. The proposed CT ΔΣ ADC performance is summarized in Table 12.

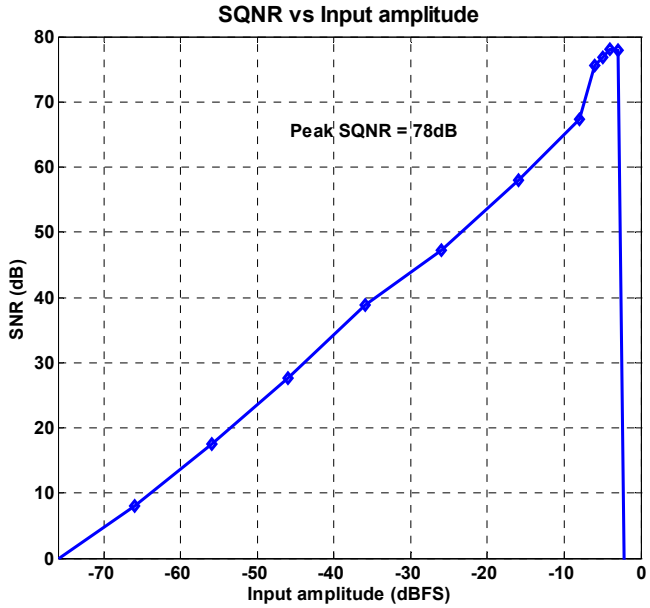


Figure 44. SNR vs. input amplitude for the CT ΔΣ ADC

Table 12. Performance summary of the proposed CT ΔΣ ADC

Parameter	**Value**
Sampling Frequency	400MHz
Bandwidth	20MHz
Peak SNDR	74dB
THD	< -76dB
Dynamic Range	73dB
Power	< 20mW
Technology	1.2V, 90nm

5. MULTI-BIT DAC DESIGN FOR A 11-BIT, 100MHz CT ΔΣ ADC

High resolution and wide bandwidth ΔΣ ADCs are implemented at low oversampling ratios to avoid achieve lower power consumption. Consequently, high resolution is obtained by using multi-bit quantizers and DACs. However, multi-bit DACs are inherently non-linear due to device mismatch and PVT variations. This section discusses the design of a highly linear, 3-bit digital-to-analog converter for a 5^{th}-order CT ΔΣ modulator with 11 bits resolution, 100MHz bandwidth and 2GHz sampling frequency in a 1.8V, 0.18µm BiCMOS process.

5.1 Effect of DAC Non-linearity in CT ΔΣ ADCs

The general block diagram of a CT ΔΣ modulator with a non-linear DAC in the feedback path is shown in Figure 45.

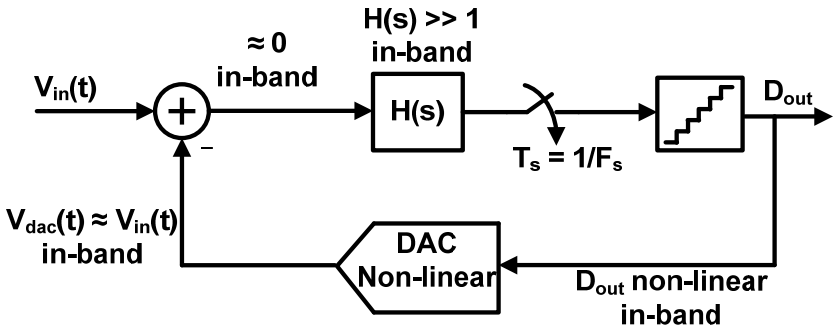


Figure 45. DAC non-linearity effects in CT ΔΣ ADCs

Due to the feedback action of the loop and large in-band loop gain in the loop filter, the error signal, which is the difference between the input signal and the DAC output, is close to zero for in-band signals. Since the DAC is non-linear, the output of the modulator is non-linearly related to the input signal within the signal band. Hence, DAC non-linearity directly appears as in-band non-linearity of the overall modulator, thereby

degrading the signal-to-noise-plus-distortion ratio of the overall modulator. Thus, even a low resolution feedback DAC requires linearity better than the overall modulator.

Dynamic element matching (DEM) and calibration are popular linearization techniques to reduce the effects of DAC nonlinearity. In DEM, different DAC elements are used for the same modulator output code in a random manner based on some algorithm which results in mismatch errors being averaged over time. Individual level averaging (ILA) [27], data weighted averaging (DWA) [28], and butterfly scrambler [29] are some of the commonly used DEM techniques. Traditionally, circuits for performing DEM typically appeared within the feedback path, thereby adding excess loop delay and degrading the stability. In order to avoid this effect, DEM circuitry has been implemented external to the feedback path in recently reported work in literature [1-5].

Calibration circuits used for the linearization of multi-bit DACs typically require an accurate reference to which all the DAC elements are calibrated. Calibration methods are very effective and linearity of up to 14 bits has been reported by using calibration [30-31].

5.2 System-level Specifications

The system-level architecture of the proposed 5^{th}-order CT $\Delta\Sigma$ is shown in Figure 46. The 5^{th}-order loop filter consists of transconductance amplifiers with passive LC sections. A 9-level quantizer is used and 5 feedback DACs implement the loop filter in feedback architecture.

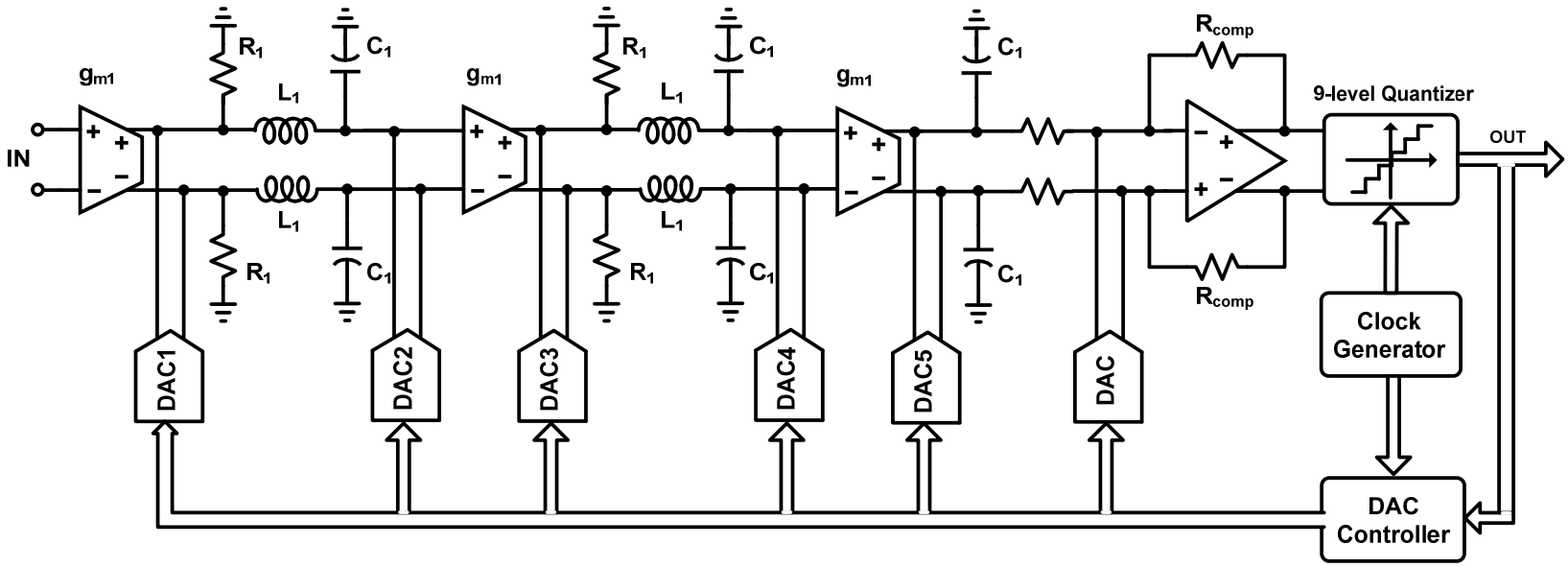


Figure 46. System-level block diagram of the CT ΔΣ modulator

The target specifications of the ADC are listed in Table 13.

Table 13. System-level specifications of the CT ΔΣ ADC

Parameter	Specification
SNDR	72 dB – 78 dB
Signal Bandwidth	100MHz
Power	< 0.5W
Quantizer resolution	9 levels
Sampling Frequency	2GHz
Supply Voltage	1.8V

In order to adjust the loop coefficients for excess loop delay, a direct feedback path is implemented around the quantizer using DAC_6. The use of this fast path requires that the feedback signals from the DACs be ready exactly one period after the sampling instant at the quantizer, that is T_s = 500ps. Assuming that the quantizer data is already available at $T_s/2$ = 250ps, the DAC has 250ps to generate the feedback signals. Current mode DACs were chosen due to the inherent high speed operation and also due to the fact that the input to the ADC is a current signal. Among these feedback DACs, multi-bit DACs 1 and 2 (and to a certain extent DAC_3) are the dominant contributors of non-linearity. Typically, either Dynamic Element Matching (DEM) or Self-Calibration techniques are employed inside the feedback path of the ADC. The conventional method is to place these blocks inside the feedback path between the quantizer and the DACs. However, any extra block in the feedback path will add additional delay.

This work discusses DEM and Self-calibration techniques for designing multi-bit DACs in high speed delta-sigma ADCs. The linearization techniques have been implemented for DAC_1 since its linearity is most critical to the overall resolution of the modulator.

5.3 Multi-bit DAC Architecture with DEM and Self-calibration

The proposed architecture for the Multi-bit DAC is as shown in Figure 47. Dynamic element matching is done by the shifter and PN-sequence generator blocks. The DEM scheme is explained in detail in Section 5.3.1. The 9-level DAC can be implemented using 8 current cells. However, in order to incorporate continuous background calibration, an extra dummy current cell is implemented so that the dummy current cell replaces the current cell that is being calibrated. The outputs of the shifter are applied to a set of 1-to-2 demultiplexers which are controlled by a 9-bit ring counter operating at the calibration clock frequency. As shown in Figure 47, when CAL_i = '1', current cell i is under calibration and the corresponding output S_{outi}, i = 0, 1,…,7 of the shifter is routed to the dummy current cell. The outputs of the DEMUX logic are applied to a synchronization block consisting of D-flip flops. The design of the synchronization circuits is discussed in Section 5.3.2. The calibration methodology and design details are explained in Section 5.3.3.

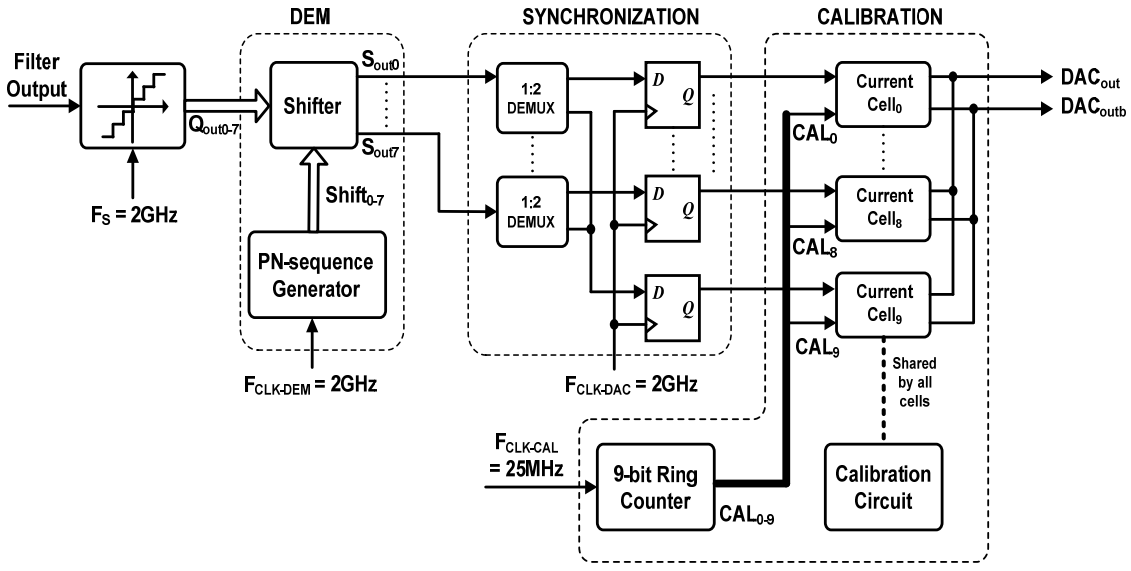


Figure 47. Proposed 3-bit DAC architecture with DEM and self-calibration

5.3.1 Dynamic Element Matching

Figure 48 shows the DEM scheme and its operation in greater detail. The main design consideration was to minimize the circuitry between the quantizer and the DAC inputs in order to obtain maximum operational speed and minimum excess loop delay.

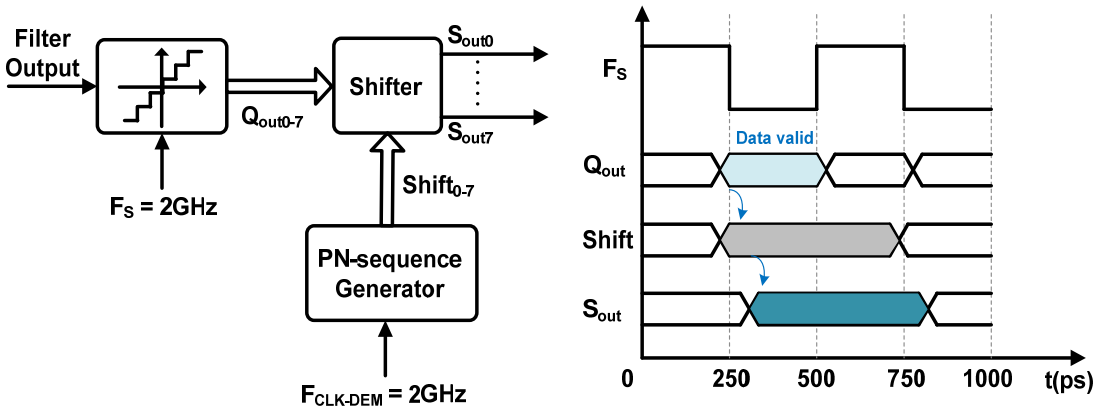


Figure 48. Implementation of high speed DEM scheme

The DEM is accomplished by a *Shifter* and a *PN-Sequence Generator*. The shifter performs a rotate-right shift on its inputs. The PN-generator indicates to the shifter the number of bits by which the shifter has to rotate its inputs. In order to maximize the effectiveness of the DEM block, the data from the quantizer (which is available at $T_s/2$ = 250ps) has to be shifted during each clock, that is, at $F_{CLK\text{-}DEM}$ = 2GHz. Hence, the PN-sequence generator also has to provide the *Shift* signals at 2GHz with the signals being ready at $T_s/2$ = 250ps within each clock period.

5.3.1.1 Shifter

The shift logic is implemented using an 8-bit funnel shifter. The operation of the funnel shifter can be explained by a 4-bit funnel shifter example as shown in Figure 49. Z_0-Z_3 represent the input lines while the lines S_0-S_3 indicate the amount of shift and S_{out0}-S_{out3} are the output lines. For correct operation of the shifter, only one of S_0-S_3 lines

is logic '1' at any given instant. For example, if $S_{out2} = 1$, the corresponding NMOS switches are ON and, $Z_0 = Q_{out0}$, $Z_1 = Q_{out1}$, $Z_2 = Q_{out2}$, $Z_3 = Q_{out3}$, $Z_4 = Q_{out0}$, $Z_5 = Q_{out1}$, $Z_6 = Q_{out2}$ which means that, $S_{out0} = Z_2 = Q_{out2}$, $S_{out1} = Z_3 = Q_{out3}$, $S_{out2} = Z_4 = Q_{out0}$, $S_{out3} = Z_5 = Q_{out1}$. Hence the input data $\{Q_{out3}, Q_{out2}, Q_{out1}, Q_{out0}\}$ has been shifted right by 2 positions to $\{Q_{out1}, Q_{out0}, Q_{out3}, Q_{out2}\}$.

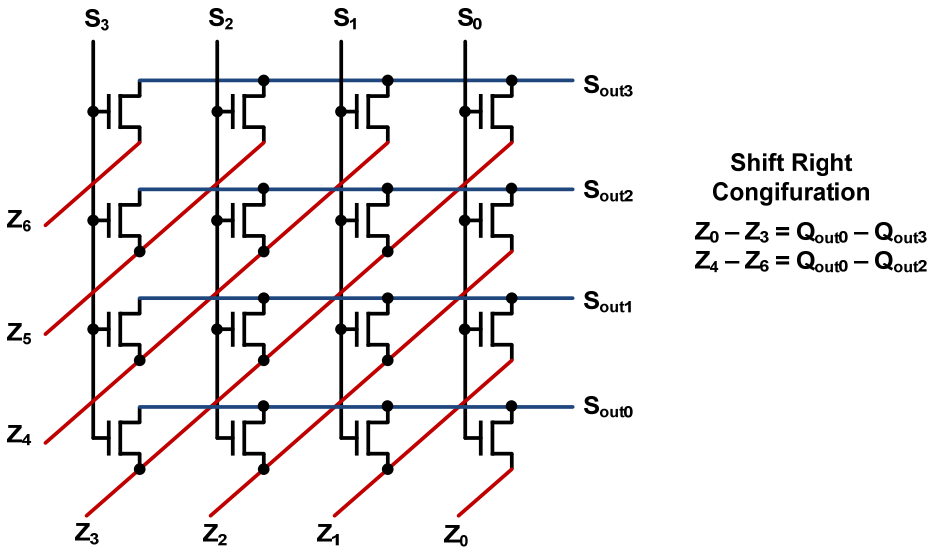


Figure 49. 4-bit funnel shifter example with shift-right configuration

The schematic of the 8-bit funnel shifter is shown in Figure 50. The operation of an 8-bit funnel shifter is similar. In the actual implementation, transmission gates are used as the switches to ensure that both high and low logic levels from the quantizer outputs are switched to output without degradation in the voltage levels. However, if the quantizer output signals are generated using current-mode logic (CML), then this requirement can be relaxed. An important design consideration is the sizing of the switches used in the funnel shifter. If the switch size is increased, the delay from the inputs to the outputs of the shifter decreases. However, this also increases the load on the *Shift* signals from the PN-generator.

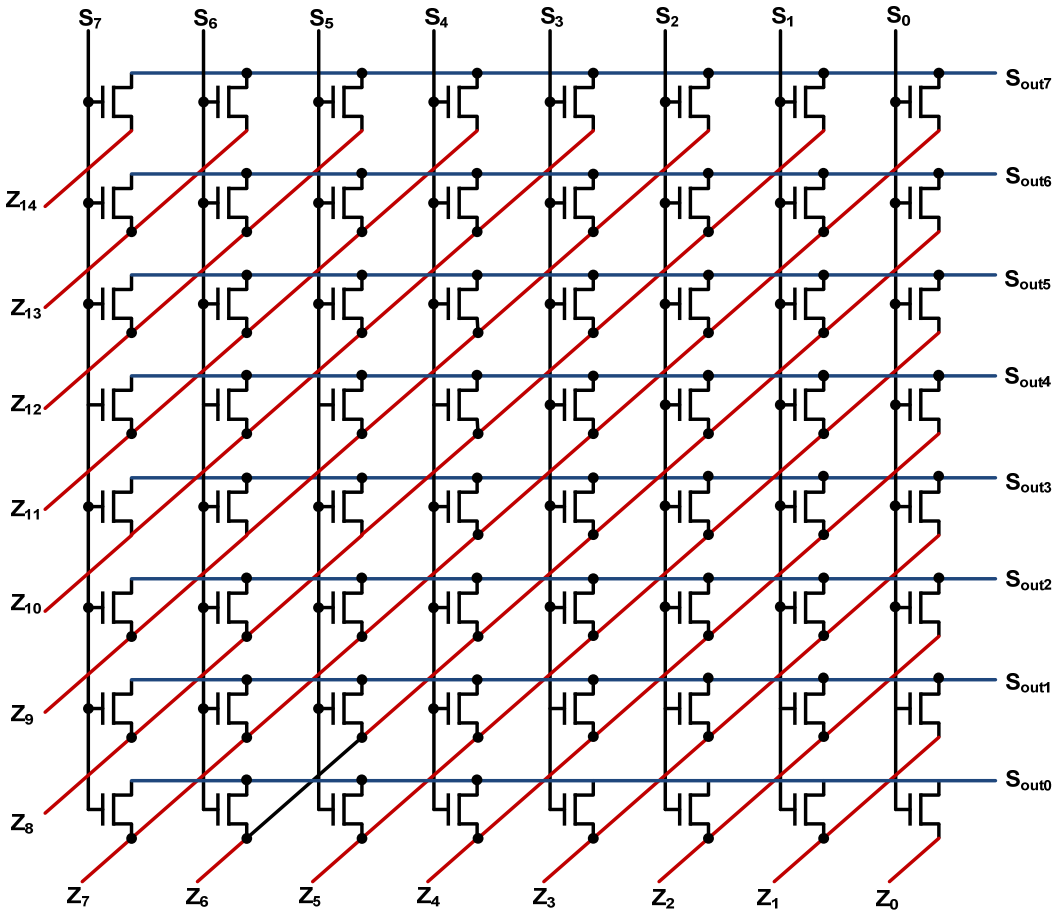


Figure 50. 8-bit funnel shifter implementation

From simulation, the delay through the shifter block was found to be approximately 60ps.

5.3.1.2 PN-sequence Generator

The PN-sequence generator generates a maximal-length sequence based on the 3rd order primitive polynomial given as,

$$P(x) = x^3 + x^2 + 1 \qquad (5.1)$$

The block diagram representation of (5.1) is shown in Figure 51.

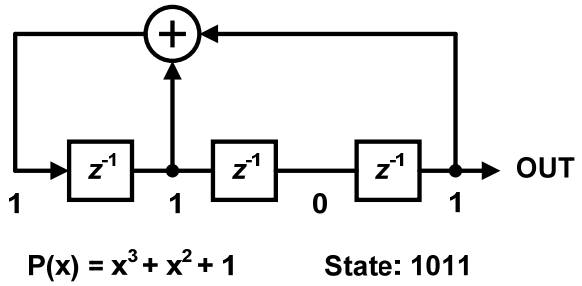


Figure 51. PN-sequence generator block diagram

The polynomial in (5.1) generates the states 1, 4, 6, 7, 3, 5, 2, 1…, etc. Hence, the PN-sequence generator has to output a logic '1' on its output lines in the order $Shift_1$, $Shift_4$, $Shift_6$, $Shift_7$, $Shift_5$, $Shift_2$, $Shift_1$, …, etc. A direct circuit-level implementation of Figure 50 can be done using flip-flops to implement the delay elements, an XOR gate to implement the addition operation and a 3-to-8-decoder to map the output to a 1-out-of-8 code. However, the resulting implementation was found to be slow and not suitable to be operated at 2GHz. A simple and straightforward implementation would be to use a 7-bit Ring Counter with the Shift signals tapped in the order in which the PN-sequence states are generated.

In the actual implementation, an *8-bit Ring Counter* has been used to incorporate the $Shift_0$ state, that is, if $Shift_0$ = logic '1', no shifting operation is performed on the input signals which means that DEM operation is disabled. The circuit diagram of the PN-sequence generator is as shown in Figure 52.

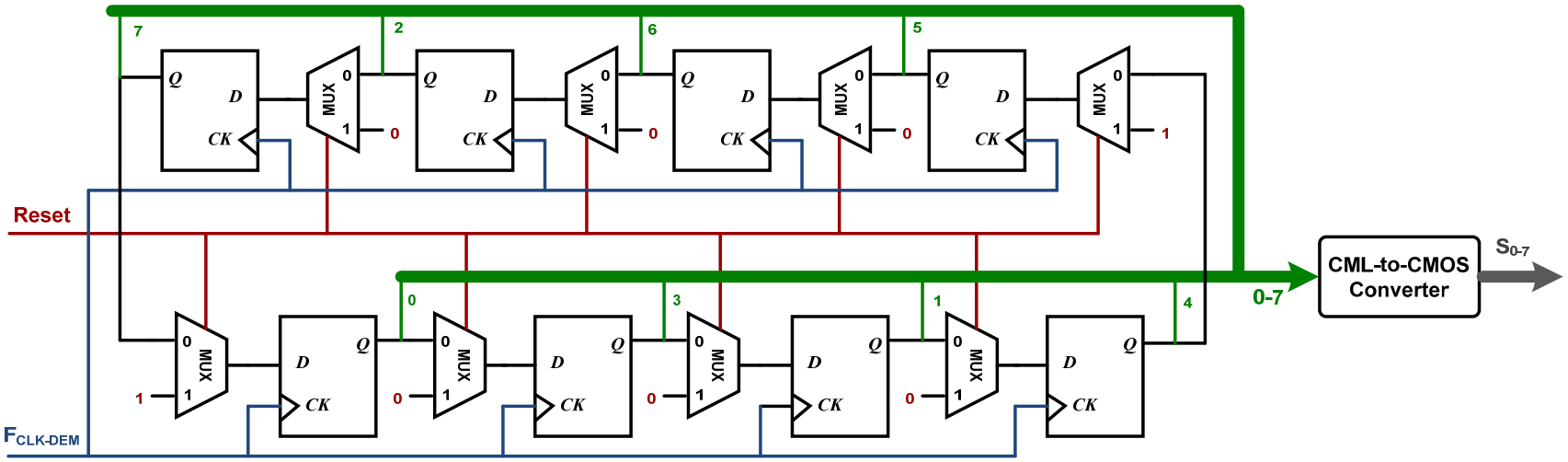


Figure 52. Implementation of the PN-sequence generator

Table 14 lists the different states of the PN-sequence generator.

Table 14. PN-sequence generator truth table

Shift							
S_7	**S_6**	**S_5**	**S_4**	**S_3**	**S_2**	**S_1**	**S_0**
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0
0	0	0	0	0	1	0	0

The PN-sequence generator should provide rail-to-rail signals for switching the transmission gates in the shifter. It was found that a 2GHz CMOS ring counter in 0.18um cannot satisfy the requirements for this design. Hence, CML logic is used to implement the ring counter and a *CML-to-CMOS converter* is used at the outputs to generate the desired rail-to-rail *Shift* signals. The schematic of the CML-to-CMOS converter is shown in Figure 53. The component values for the CML-to-CMOS converter are listed in Table 15.

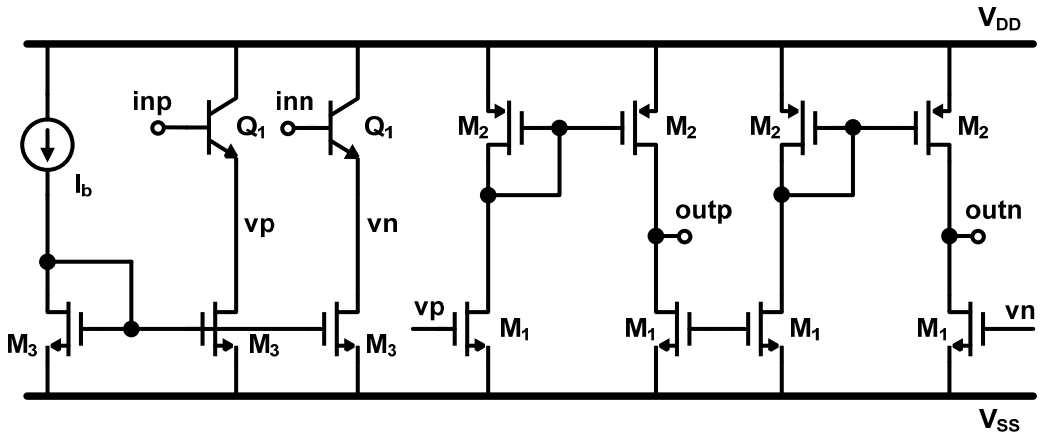


Figure 53. CML-to-CMOS converter schematic

Table 15. Component values for CML-to-CMOS converter

Device	Dimensions
M_1	5µm/0.18µm
M_2	2*(5µm/0.18µm)
M_3	4*(5µm/0.18µm)
Q_1	W_E = 0.2µm, L_E = 0.76µm, m = 2
I_b	300µA

From simulations, the total delay through the DEM scheme was found to be approximately 160ps. This value is below the total feedback path delay requirement of 250ps as explained in Section 5.2. The remaining available time is required to meet the setup time requirements of the D-Flip-flops used in the synchronization circuits as explained in the next section.

5.3.2 Synchronization Circuit

All the current cells in the 9-level DAC have to generate the currents simultaneously in response to the input signals. Any mismatch in the timing of the signals driving the current-steering switches will give rise to non-linearity at the DAC

outputs. Hence, the outputs of the shifter are retimed using a set of CML D-Flip-flops. Low-voltage triple-tail architecture is used to implement the DFFs as shown in Figure 54 [31]. The component values for the DFF are listed in Table 16.

Table 16. Component values for D-flip-flop

Device	**Dimensions**
M_1	4*(8µm/0.18µm)
Q_1	W_E = 0.2µm, L_E = 0.76µm, m = 1
Q_2	W_E = 0.2µm, L_E = 10.16µm, m = 4
I_b	800µA

The low-voltage triple-tail latch architecture shown in Figure 54 has smaller propagation delay than conventional CML latch architectures due to the lesser number of stacked levels of transistors. However, base current leakage and glitches in the outputs are some of the disadvantages of this architecture. Base current leakage can be reduced by sizing up the CLK transistors, but this will increase the clock load. Glitches can be reduced by using low-swing clocks with high crossing point.

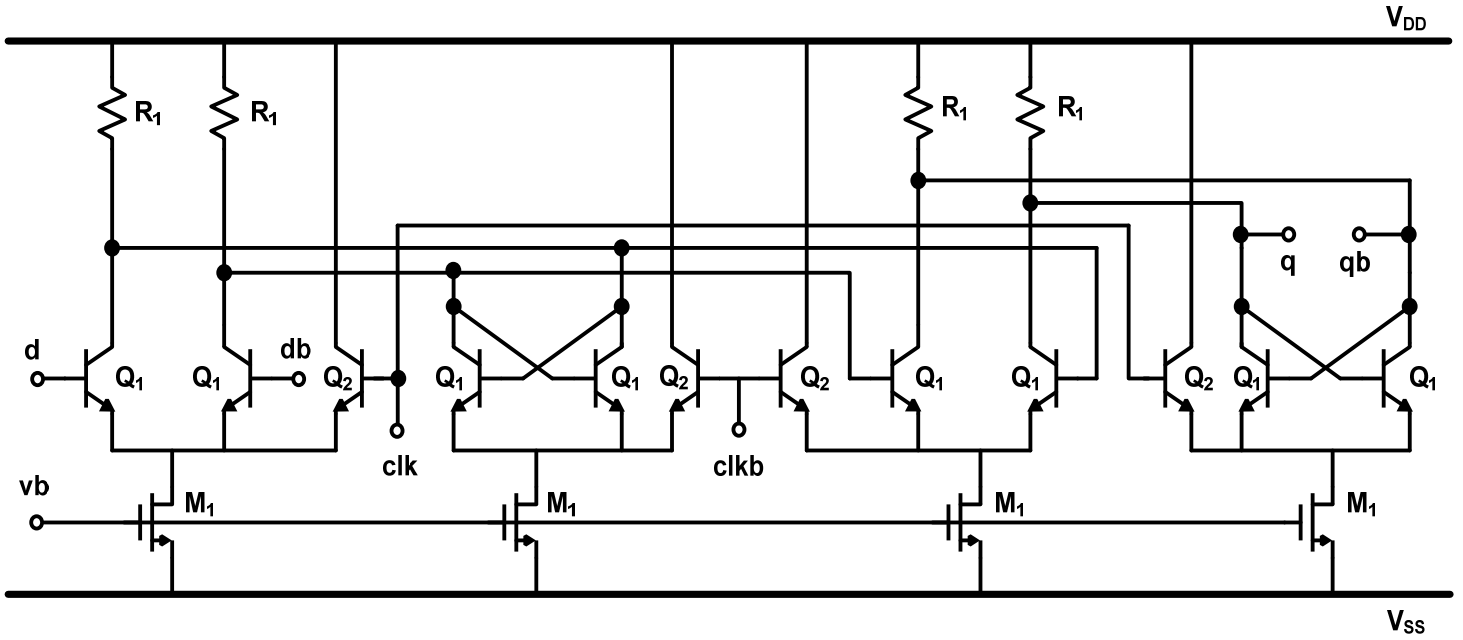


Figure 54. Schematic of the triple-tail high speed D-flip-flop

5.3.3 Self-calibration

The current cells can be closely matched to a desired value by calibrating each current cell with a precise reference current source. The principle of current calibration is illustrated in Figure 55. When the cell is being calibrated, switch S_{CAL} is closed and S_{out} is open, and the reference current flows into the two transistors M_1 and M_2. Since M_2 is connected as an MOS diode, its gate-to-source voltage adapts so that the drain current of M_2 equals the difference between I_{ref} and I_{M1}. When the calibration is completed, S_{CAL} is open and S_{out} is closed, and the current cell can be used as a normal current-steering cell. Since V_{gs2} remains stored on the gate-to-source capacitance of M_2, the sum of the currents of M_1 and M_2 remains equal to I_{ref}.

The calibration loop for an individual current cell is as shown in Figure 56. The calibration loop consists of two parts: the *Calibration Reference* which is shared by all current cells, and *Current Source* that is being calibrated. A super buffer is used in the calibration reference to precisely set the desired drain voltage on M_6. Ideally, this voltage has to be set equal to the common mode output voltage on the current steering switches M_4 and M_5.

Each current source is split into two parts; a *Coarse Current Source* M_1 carrying 97% of the reference current I_{ref}, and a *Fine Current Source* M_2. When CAL = '1', M_4 and M_5 are disabled, M_6-M_8 are ON and I_{ref} flows into the current source, charging up the gate-to-source capacitance C_{gs} of the fine current source M_2. When the calibration is complete, CAL = '0' and M_6-M_8 are switched OFF. Dummy switches M_9-M_{12} are used to minimize the effects of charge injection.

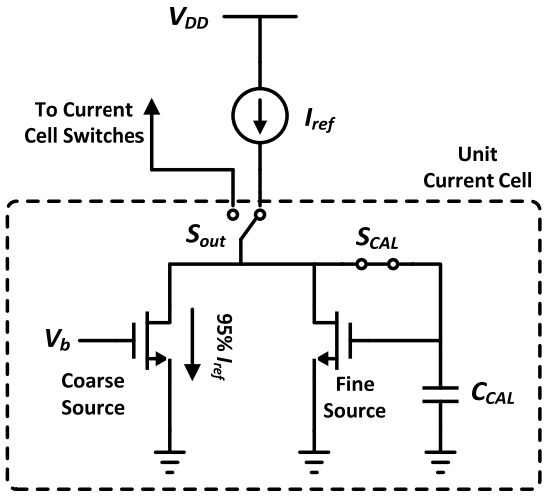


Figure 55. Current calibration principle

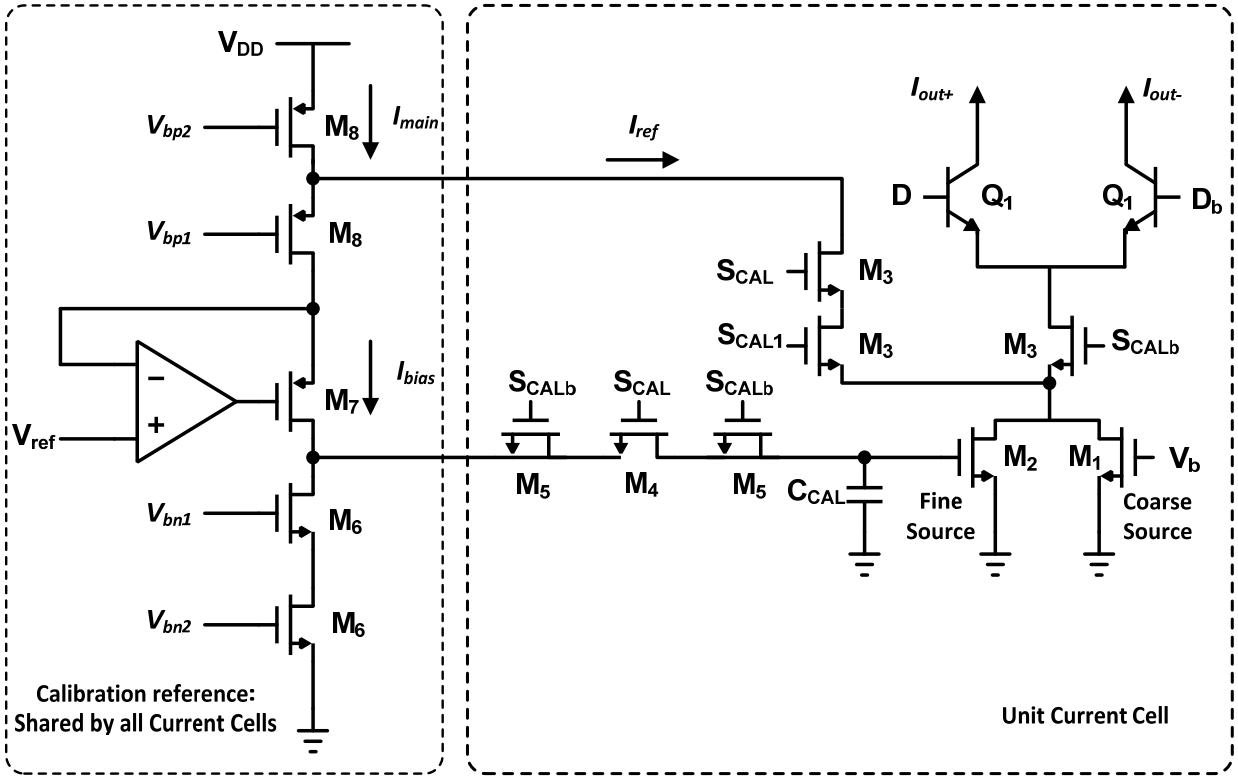


Figure 56. Schematic of the automatic background self-calibration technique

The time required for calibrating each current cell is approximately 40ns. Hence, the calibration signals are generated by a 25MHz clock. The component values for the self-calibrated current cell and calibration reference are listed in Table 17.

Table 17. Component values for self-calibrated current cell and reference

Device	Dimensions
M_1	16µm/2µm
M_2	24.8µm/0.18µm
M_3	4*(6µm/0.18µm)
M_4	5µm/0.18µm
M_5	2.6µm/0.18µm
M_6	4µm/0.18µm
M_7	4*(3µm/0.18µm)
M_8	10*(9µm/0.18µm)
Q_1	W_E = 0.2µm, L_E = 0.76µm, m = 1
I_b	610µA
I_{bias}	100µA
I_{main}	745µA
V_{ref}	600mV

5.4 Current Cell Design

5.4.1 Matching Considerations for Current Source Transistors

Random error sources influence the static cell current and are caused by the random variations inherently present in a CMOS manufacturing process. Several mechanisms contribute to this random mismatch which can be reduced by increasing the area of the matched transistors [32]. The relationship between area and current mismatch is described by,

$$WL = \left(\frac{I_d}{\sigma_{\Delta I_d}}\right)^2 \left[A_\beta^2 + \frac{4A_{V_t}^2}{(V_{gs} - V_t)^4}\right] \tag{5.2}$$

where I_d is the drain current, A_β and A_{Vt} are technology parameters provided by the foundry, $\sigma_{\Delta Id}^2$ is the variance of the current source mismatch. Using (5.2), the required active area for sufficient matching can be calculated.

The dimensions of the current source transistors for a given technology and overdrive voltage are given by,

$$W^2 = \frac{1}{2K_P\left(\frac{\sigma_{\Delta I_d}}{I_d}\right)^2}\left[\frac{A_\beta^2}{(V_{gs} - V_t)^2} + \frac{4A_{V_t}^2}{(V_{gs} - V_t)^4}\right] \tag{5.3}$$

$$L^2 = \frac{K_P}{2I_d\left(\frac{\sigma_{\Delta I_d}}{I_d}\right)^2}\left[A_\beta^2(V_{gs} - V_t)^2 + 4A_{V_t}^2\right] \tag{5.4}$$

A higher overdrive voltage would provide better area efficiency at the expense of reduced swing at the output. A larger area results in greater parasitic capacitances which limit the speed of operation. Hence, there exists a trade-off between overdrive voltage and speed of operation. Table 18 lists the total areas and dimensions of the current cells for all DACs designed for the proposed system.

Table 18. Dimensions and total area for different feedback DACs

DACi	Unit current	(W/L), m=4	Total area, μm^2
DAC1-coarse	610uA	203µ/3.84µ	7795
DAC1-fine	35uA	48µ/16µ	7680
DAC2	1.55mA	323µ/2.4µ	6976
DAC3	960uA	255µ/3µ	6885
DAC4	790uA	231µ/3.36µ	6985

5.4.2 Output Impedance of Current Cell

The output impedance of each current cell should be sufficient to achieve the desired linearity across the entire Nyquist range. The impedance Z_{imp} seen in the drain of the switch transistors of each current cell has to be made large so that its influence on the INL specification of the D/A converter is negligible. The relationship between Z_{imp} and the achievable INL specification is given by [32],

$$\mathrm{INL} = \frac{I_{unit} R_L^2 N^2}{4 Z_{imp}} \tag{5.5}$$

where I_{unit} is the LSB current, R_L is the load resistance, N is the number of current cells.

The relation between the SFDR specification and the corresponding output impedance requirement is expressed as [32],

$$\mathrm{SFDR} = 20 \log_{10}\left(\frac{4 Z_{req}}{N R_L}\right) \tag{5.6}$$

For the DAC1 current cell, R_L=25Ω with a linearity requirement of 12 bits. Using (5.5)-(5.6), Z_{imp} = 31kΩ and Z_{req} = 225kΩ.

The cascode configuration of the switch and current source has sufficiently high impedance greater than 700kΩ over the 100MHz signal bandwidth to achieve the linearity specifications.

5.5 Simulation Results

The complete system was simulated with the transistor-level implementation of the proposed linearization schemes and feedback DACs, and Verilog-A implementation of the filter and 9-level quantizer blocks. The full-scale input of the system is 200mV (peak). The modulator output spectrum for various configurations of the system is shown in Figure 57.

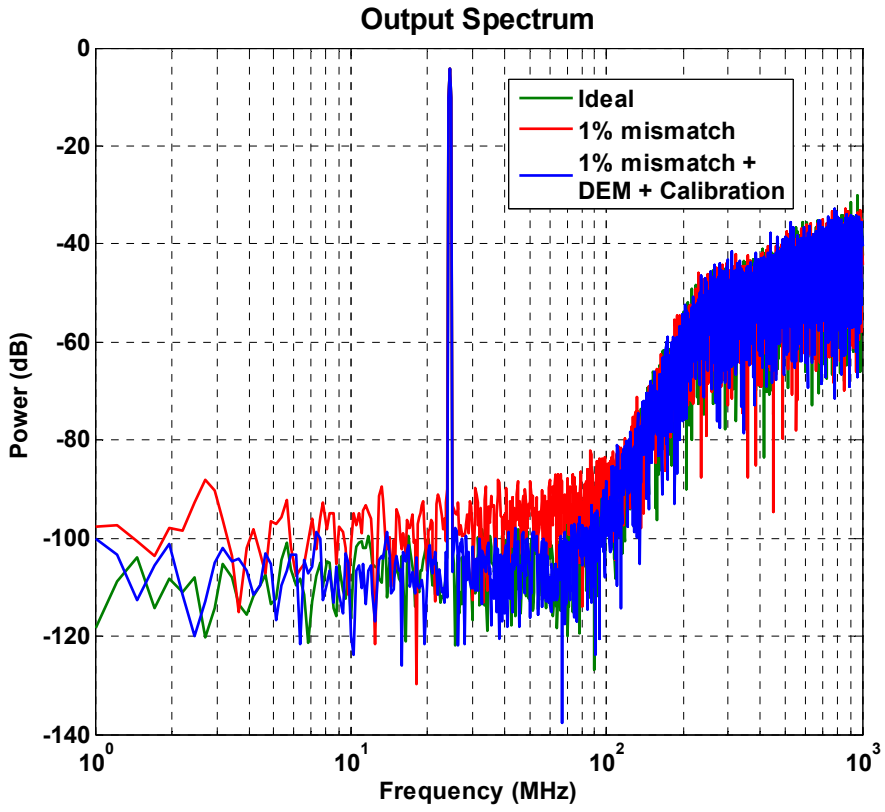


Figure 57. Output spectrum with and without linearization schemes

Table 19 lists the peak SNR at the output of the modulator for different configurations of the system.

Table 19. Performance summary of the proposed linearization schemes

Mismatch	**DEM**	**Self-calibration**	**SNR (dB)**
N	N	N	73.8
Y	N	N	55
Y	Y	N	63.6
Y	N	Y	70
Y	Y	Y	72.7

Y-Yes, N-No

The unit current sources were designed for 1% mismatch. It can be observed that with only the DEM scheme activated, the SNR of the system improves by approximately 8dB. With only the calibration scheme activated, the SNR of the system improves by 15dB. With both DEM and self-calibration schemes activated, the SNR of the system is only almost equal to the ideal SNR with no mismatch. Hence, a 3-bit DAC with 12-bit linearity with 100MHz bandwidth and operating at 2GHz clock frequency has been designed.

6. CONCLUSIONS

System-level and circuit-level design considerations for high resolution, wide bandwidth continuous-time delta-sigma ADCs were presented in this work. A detailed and systematic design procedure for a 12-bit, 20MHz bandwidth continuous-time delta-sigma ADC was demonstrated. Methods for optimum selection of design variables in the parameter space and choice of loop filter architecture were explained. MATLAB and Cadence simulation results were also presented for the proposed delta-sigma modulator.

The problem of clock jitter in continuous-time delta-sigma ADCs was explained. A novel hybrid DAC pulse-shaping technique was proposed to improve clock jitter tolerance of the 12-bit, 20MHz bandwidth continuous-time delta-sigma ADC prototype. Theoretical analysis was performed to demonstrate the benefits of relaxed op-amp requirements offered by the proposed technique. A detailed design procedure for the circuit-level implementation of the 3-bit hybrid DAC in 90nm, 1.2V CMOS technology was presented. Simulation results of the circuit implementation showed that the proposed technique provided a jitter tolerance of up to 5ps (rms).

Techniques to improve the linearity of the feedback multi-bit DACs implemented for a 11-bit, 100MHz bandwidth continuous-time delta-sigma ADC operating at a sampling frequency of 2GHz were presented. In particular, a novel DAC linearization scheme was proposed which employed both dynamic element matching and self-calibration of the current sources while minimizing excess loop delay. Design procedure for determining optimum dimensions for the DAC current sources to achieve the matching and linearity requirements were also explained. The 3-bit current-steering DACs were implemented in 0.18μm CMOS technology. It was shown that the proposed linearization scheme achieved a SNR performance approximately equal to the ideal value.

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