OSCILLATOR ARCHITECTURES AND ENHANCED FREQUENCY SYNTHESIZER

A Dissertation

by

SANG WOOK PARK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	José Silva-Martinez
	Laszlo Kish
	Duncan M. Walker
Head of Department,	Costas Georghiades

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ABSTRACT

Oscillator Architectures and Enhanced Frequency Synthesizer. (December 2009)

Sang Wook Park, B.S., Yonsei University, Korea;

M.S., Yonsei University, Korea

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

A voltage controlled oscillator (VCO) that generates a periodic signal whose frequency is tuned by a voltage is a key building block in any integrated circuit system. A sine wave oscillator can be used for a built-in self testing where high linearity is required. A bandpass filter (BPF) based oscillator is a preferred solution, and high quality factor (Q-factor) is needed to improve the linearity. However, a stringent linearity specification may require very high Q-factor, and is not practical to implement. To address this problem, a frequency harmonic shaping technique is proposed. It utilizes a finite impulse response filter improving the linearity by rejecting certain harmonics. A prototype SC BPF oscillator with an oscillating frequency of 10 MHz is designed and measurement results show that linearity is improved by 20 dB over a conventional oscillator.

In radio frequency area, preferred oscillator structures are an LC oscillator and a ring oscillator. An LC oscillator exhibits good phase noise but an expensive cost of an inductor is disadvantageous. A ring oscillator can be built in standard CMOS process, but suffers due to a poor phase noise and is sensitive to supply noise. An RC BPF

oscillator is proposed to compromise the above difficulties. An RC BPF oscillator at 2.5 GHz is designed and measured performance is better than ring oscillators when compared using a figure of merit. In particular, the frequency tuning range of the proposed oscillator is superior to the ring oscillator.

VCO is normally incorporated with a frequency synthesizer (FS) for an accurate frequency control. In an integer-N FS, reference spur is one of the design concerns in communication systems since it degrades a signal to noise ratio. Reference spurs can be rejected more by either the lower loop bandwidth or the higher loop filter. But the former increases a settling time and the latter decreases phase margin. An adaptive lowpass filtering technique is proposed. The loop filter order is adaptively increased after the loop is locked. A 5.8 GHz integer-N FS is designed and measurement results show that reference spur rejection is improved by 20 dB over a conventional FS without degrading the settling time. A new pulse interleaving technique is proposed and several design modifications are suggested as a future work.

DEDICATION

To my beloved wife Shin Ah and son John Shinhyeok,

my father Boo Keun and to the memory of my mother Kyeong Hee.

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CHAPTER I

INTRODUCTION

1.1. Background and Motivation

A signal generating circuit is one of the most important building blocks in analog, digital and mixed-signal designs. A generated signal is used to provide an input tone of a device under test (DUT) for the built-in self test (BIST) or a reference clock of any type of digital gates. In communication systems, it is served as a local oscillator (LO) that is used for frequency translations through the mixer. In the application where a signal is used for a reference input such as BIST, a desired waveform would be sinusoidal and a distortion is important. On the other hand, a clock signal for digital gates, jitter and the period accuracy are critical while a distortion is not a concern. Furthermore, in radio frequency (RF) applications, phase noise becomes the most important factor since its operation is interpreted mainly in the frequency domain.

A preferred oscillator architecture for a sine wave generation is a bandpass filter (BPF) based oscillator. It consists of a BPF with an amplifier on a positive feedback path. Since a BPF is a frequency selective circuit, the signal taken from the BPF output exhibits a sinusoidal shape. The linearity of generated signal is proportional to the frequency selectivity, known as quality factor (Q-factor), of BPF, and it is desired to

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This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

increase a Q-factor to improve the signal linearity. However, it is required more power consumption as well as large spread of components and more complicated structure to enhance a Q-factor.

The most popular oscillator architecture for RF applications is mainly either a LC oscillator or a ring oscillator. A LC oscillator exhibits good phase noise, but a fabrication cost is expensive due to an inductor and it consumes a large chip area. A narrow frequency tuning range is another downside of a LC oscillator. A ring oscillator can be built in a standard CMOS process with a small silicon area, and a frequency tuning range is very wide compared with a LC oscillator. However, a ring oscillator has poor phase noise performance and it is sensitive to a power supply induced noise.

A spurious tone of a frequency synthesizer in RF wireless communication systems is coupled with an interferer and degrades the system signal to noise ratio (SNR). In an integer-N frequency synthesizer that is preferred structure due to simplicity and small power consumption, a reference spur is one main concern. The improved design of the phase frequency detector (PFD) and the charge pump can reduce the magnitude of spur. Also, in a system perspective, a narrow loop bandwidth improves a rejection of a reference spur, but at the cost of a slow settling. Higher order loop filter is also beneficial, but phase margin is decreased. In this work, enhanced design techniques and system structures are proposed and investigated to address and compromise the challenges discussed above.

1.2. Organization

Chapter II begins with general design considerations of the voltage controlled oscillator (VCO) and the frequency synthesizer. A theoretical background of an oscillating circuit is introduced and several design issues of the VCO are discussed. Phase noise in the VCO is formally explained through mathematical expressions. Behaviors of the frequency synthesizer are given using a linear phase model of a phase locked loop (PLL). Design trade-offs between a number of design parameters are carefully considered.

In Chapter III, we propose a non-linear shaping switched-capacitor (SC) oscillator with enhanced linearity. One main purpose of the proposed oscillator is to improve linearity by rejecting harmonics. An effective finite-impulse response (FIR) filtering technique is proposed, and a SC-bandpass filter (BPF) based oscillator is implemented with the proposed technique as well as a conventional topology oscillator. Measurement results show the proposed oscillator improves the harmonic distortion by at least 20 dB over a conventional oscillator.

Chapter IV presents RC BPF-based RF VCO. The concept of implementing the RF VCO by adopting RC BPF is explained, and the design optimization in terms of phase noise and power consumption is discussed. A prototype oscillator operating at 2.5 GHz is implemented and experimental results show better figure of merit (FOM) among other publicated ring oscillators.

Chapter V focuses on reducing reference techniques in integer-N frequency synthesizers by proposing an adaptive lowpass filtering technique. A 5.8 GHz integer-N charge pump based frequency synthesizer is designed and measurement results are shown. With a proposed technique, the reference spur suppression is improved by 20 dB over a conventional frequency synthesizer. Further techniques and modifications on existing frequency synthesizer are proposed and demonstrate the performance improvement through simulations. Chapter VI concludes this work.

CHAPTER II

GENERAL DESIGN CONSIDERATIONS OF VOLTAGE CONTROLLED OSCILLATOR AND FREQUENCY SYNTHESIZER

2.1. Voltage Controlled Oscillator

2.1.1. Voltage Controlled Oscillator Basics

An oscillator is an electronic circuit that produces a periodic signal. The period of an oscillator is determined by the property of an oscillator circuit, and often, is required to be varied by an external control. If the oscillation frequency is controlled by a voltage input, it is called a voltage/current controlled oscillator (VCO/CCO). In the electronic circuit designs, the Barkhausen stability criterion is used to determine if an electronic circuit will oscillate. It provides necessary conditions for oscillation of linearized systems. The Barkhausen criterion is widely used in the design of electronic oscillators, and also in the design of general feedback circuits to prevent them from oscillating.

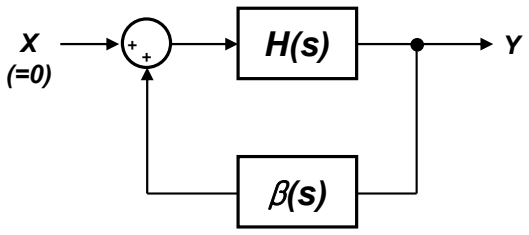


Figure 1. Linearized feedback system.

Figure 1 shows a block diagram of the linearized feedback system where *H(s)* is the transfer function of the input *X(s)* and output *Y(s)*, i.e. *H(s) = Y(s) / X(s)*, and *β(s)* is the feedback gain, thus the product of *H(s)* times *β(s)* is the loop gain around the feedback loop of the system. The closed loop transfer function becomes

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1-\beta(s)H(s)} \tag{2-1}$$

According to Barkhausen criterion, the system will sustain steady-state oscillations only if:

$$\left|H(s)\beta(s)\right| = 1 \tag{2-2}$$

$$\angle H(s)\beta(s) = 2\pi n,\ n \in 0,1,2,.... \tag{2-3}$$

The equation (2-2) states that the absolute magnitude of the loop gain is equal to unity, and (2-3) indicates that the total phase shift around the loop is zero or an integer multiple of 2π. Satisfying the condition of both (2-2) and (2-3), there will be a periodic signal with stable amplitude at the output *Y* without any signal at the input *X*. Practically, the absolute magnitude of the loop gain is designed greater than one initially forcing the system to start the oscillation. Once the oscillation is established, a certain limiting operation is done on the feedback gain *β* causing the averaged loop gain remains one. Then, the oscillator output amplitude can be stable. The location of poles and zeros of

the open loop and closed loop can be illustrated using a particular example of *H(s)* and *β(s)*. Assuming *H(s)* is a second-order bandpass filter (BPF) and *β(s)* is a linear gain of *β* as

$$H(s) = \frac{ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \qquad (2\text{-}4)$$
$$\beta(s) = \beta$$

where ω_0 is a center frequency, Q is a quality factor (Q-factor), k is a gain factor of a BPF, and β is a linearized feedback gain. *H(s)* has one zero at the origin and two poles at the left half plane (LHP). Depending on the value of Q, two poles can be either two real poles or conjugated poles. The location of poles and zero of H(s) in (2-4) is plotted in Figure 2 (a). In a closed loop, the feedback gain β pushes the open loop poles toward a right half plane (RHP). As seen in Figure 2 (b), two poles are on the imaginary axis (jw-axis) when $|H(s)\beta(s)| = 1$, and they are placed into RHP when $|H(s)\beta(s)| > 1$.

Due to the cost and effectiveness, the VCO is often required to be designed and integrated using CMOS process with other circuit blocks. Among the many VCO architectures, the bandpass filter (BPF)-based oscillator is the one of most popular structures. The BPF inherently satisfies the phase condition (2-3) of the Barkhausen criteria since its phase response varies from positive to negative degree crossing zero degree at the center frequency of the BPF. Hence, the oscillation frequency is determined by the center frequency of the BPF.

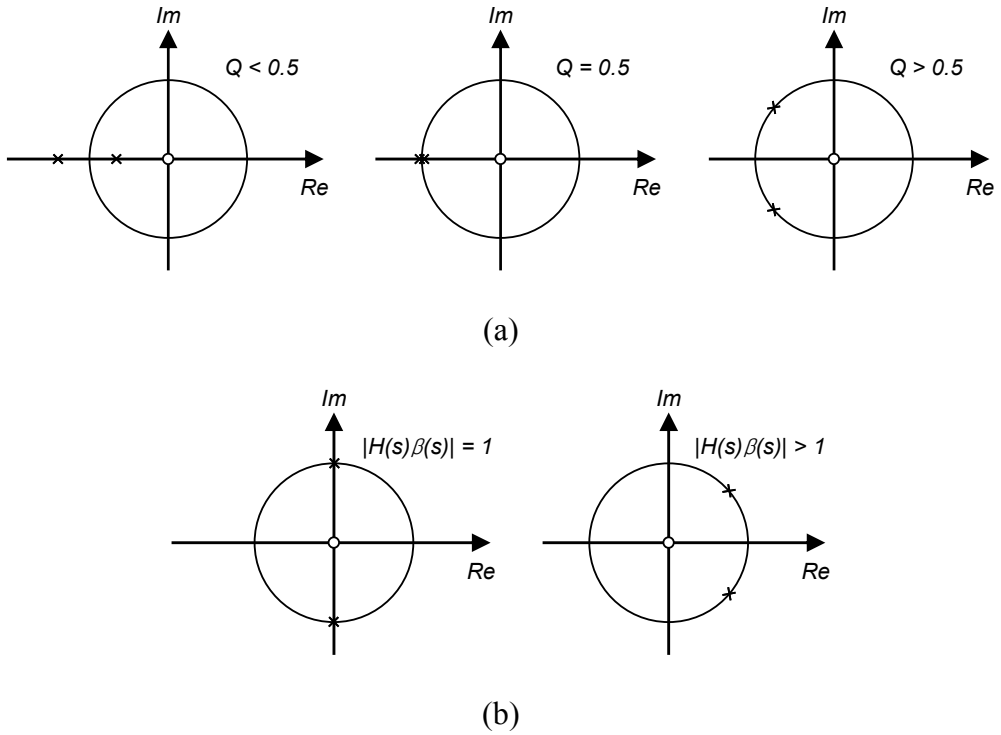


Figure 2. The location of poles and zero. (a) Open loop H(s). (b) Closed loop.

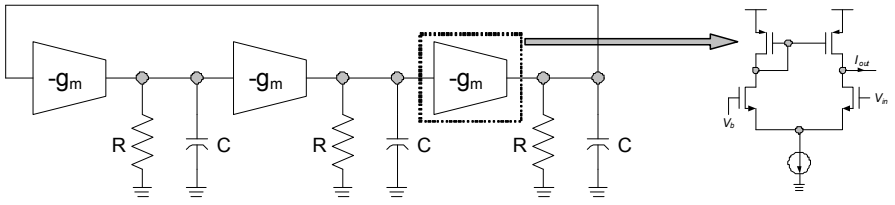
The BPF can be implemented by the active-RC circuits, the switched-capacitor (SC) circuits or the passive elements. To satisfy the condition of (2-2), the feedback gain β is implemented with an operational amplifier (op-amp) or even a limiting amplifier to ensure enough gain. Since the BPF is the frequency selective filter and the frequency selectivity (Q-factor) can be designed high, the oscillator output signal can have small harmonic components yielding good performance of total harmonic distortion (THD). Therefore, this type of oscillator can be used for the applications where excellent signal purity is required.

For a clock generation or wired communication systems, a ring oscillator is preferred structure due to the simple design and wide frequency tuning range. A ring oscillator consists of many delay stages and the oscillation period is determined by twice of the sum of delays from each stages. A delay stage is often implemented using an inverter that contributes 90º phase shift at most. Hence, the minimum number of delay stage should be 3 to satisfy (2-3). A ring oscillator can be built using the standard CMOS process so that the implementation cost is very cheap.

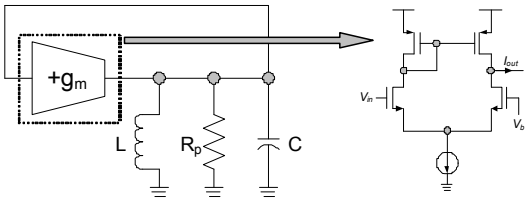
In many radio frequency (RF) wireless communication systems, an LC oscillator is preferred due to the excellent phase noise performance. The LC oscillator is a special type of the BPF-based oscillators since it requires a passive inductor. Since an inductor is not provided in standard CMOS process and it takes huge silicon area, its fabrication cost is expensive. Also, Q-factor of an inductor is not good due to the parasitic effects. However, an LC oscillator is still attractive due to the ability of high frequency oscillation and a good phase noise. Phase noise of LC oscillators is normally significantly smaller than that of ring oscillators. According to reported oscillators operating in GHz frequency range, phase noise of LC oscillators exhibit better phase noise performance than ring oscillators by 20 ~ 50 dB.

2.1.2. Design Considerations of the VCO

The key performance parameters of the VCO can be categorized depending on the applications. For the VCO for a sinusoidal signal generation, a total harmonic distortion would be the most important factor, while timing jitter is critical for the clock generation VCO. Jitter is the deviation from the ideal timing of an event and is composed of deterministic jitter (DJ) and random jitter (RJ). DJ is jitter with a non-Gaussian probability density function and is always bounded with specific causes. RJ is jitter that is not bounded and can be described by a Gaussian probability distribution. RJ is characterized by its standard deviation value. Since jitter is a timing error within a system, the accumulation of jitter will eventually lead to data errors.



(a)



(b)

Figure 3. Linearized model of oscillators. (a) 3-stage ring oscillator. (b) LC oscillator.

The frequency tuning range is also important for the VCO design. It is normally dependent on the VCO structure, and a ring oscillator typically exhibits very wide tuning range compared to other architectures.

Consider two different oscillator architectures, a 3-stage ring oscillator and an LC oscillator as seen in Figure 3. A single-ended transistor-level implementation of negative and positive gm is also shown in Figure 3 and this implementation can be used for a low-frequency operation. An oscillating frequency of each oscillator can be calculated as

$$\omega_{0,ring} = \frac{\sqrt{3}}{RC} \tag{2-5}$$

$$\omega_{0,LC} = \frac{1}{\sqrt{LC}} \tag{2-6}$$

Note that for the general case of *n* (odd) stages, the oscillating frequency becomes

$$\omega_{0,ring} = \frac{\tan\left(180^\circ / n\right)}{RC} \tag{2-7}$$

Normally, a resistor in a ring oscillator is implemented with transistors and is used for frequency tuning. Assuming C is constant, tuning range of ring oscillator is calculated from (2-5) as

$$\frac{\omega_{0,ring,\max}}{\omega_{0,ring,\min}} = \frac{R_{\max}}{R_{\min}} \tag{2-8}$$

where R_{min} and R_{max} are the minimum and maximum adjustable resistance, respectively. In case of an LC oscillator, frequency tuning is done by adjusting C because it is usually not allowed to tune the inductance. In addition, only a part of C can be used to tune the frequency since C is decomposed of a fixed C (C_{fixed}) as well as a variable C (C_{var}). Assuming C_{min} and C_{max} are the minimum and maximum adjustable C_{var}, tuning range of an LC oscillator is calculated from (2-6) as

$$\frac{\omega_{0,LC,\max}}{\omega_{0,LC,\min}} = \sqrt{\frac{C_{fixed} + C_{\max}}{C_{fixed} + C_{\min}}} \tag{2-9}$$

To quantify tuning ranges of each oscillator, consider a specific numerical example. If we assume a realistic case such as $R_{max} / R_{min} = 5$, $C_{max} / C_{min} = 5$, $C_{fixed} = C_{max}$, and applying them into (2-8) and (2-9) yields

$$\begin{aligned} &\frac{\omega_{0,ring,\max}}{\omega_{0,ring,\min}} = 5 \\ &\frac{\omega_{0,LC,\max}}{\omega_{0,LC,\min}} = \sqrt{10/6} = 1.3 \end{aligned} \tag{2-10}$$

It is known that with a specific example, a frequency tuning range of a ring oscillator is 3.8 (= 5/1.3) times greater than that of an LC oscillator.

Like any other circuit blocks, power consumption and silicon area should also be considered in designing the CMOS VCO. Silicon area is normally dominated an inductor in case of an LC oscillator since an inductor takes much larger area than any other devices. To compare silicon areas used in an LC oscillator and a ring oscillator as seen in Figure 3, consider a specific example. Assuming both oscillators operating at 2.5 GHz and a capacitor of 500 fF is used for both oscillators, required inductor and resistor can be calculated using (2-5) and (2-6).

$$R = \frac{\sqrt{3}}{\omega_0 C} = \frac{\sqrt{3}}{2\pi \cdot 2.5GHz \cdot 500\,fF} = 220\Omega \tag{2-11}$$

$$L = \frac{1}{\omega_0^{\,2} C} = \frac{1}{(2\pi \cdot 2.5GHz)^2 \cdot 500\,fF} = 8.1nH \tag{2-12}$$

(2-11) is a resistor needed for a ring oscillator of Figure 3 (a) and (2-12) is an inductor for an LC oscillator of Figure 3 (b). Since silicon area of each device is varied in different technology, consider TSMC 0.18 μm CMOS process. Figure 4 shows layout and size of each device, and A_L, A_C and A_R denote the size of inductor, capacitor and resistor, respectively. Ignoring the area of transistors, total silicon area of a ring oscillator (A_{Ring}) and an LC oscillator (A_{LC}) can be calculated as

$$A_{Ring} = 3 \cdot \left(A_R + A_C \right) = 1395 \mu m^2 \tag{2-13}$$

$$A_{LC} = A_L + A_C = 221320 \mu m^2 \tag{2-14}$$

As calculated in (2-13) and (2-14), an LC oscillator is 160 times larger than a ring oscillator in terms of a silicon area.

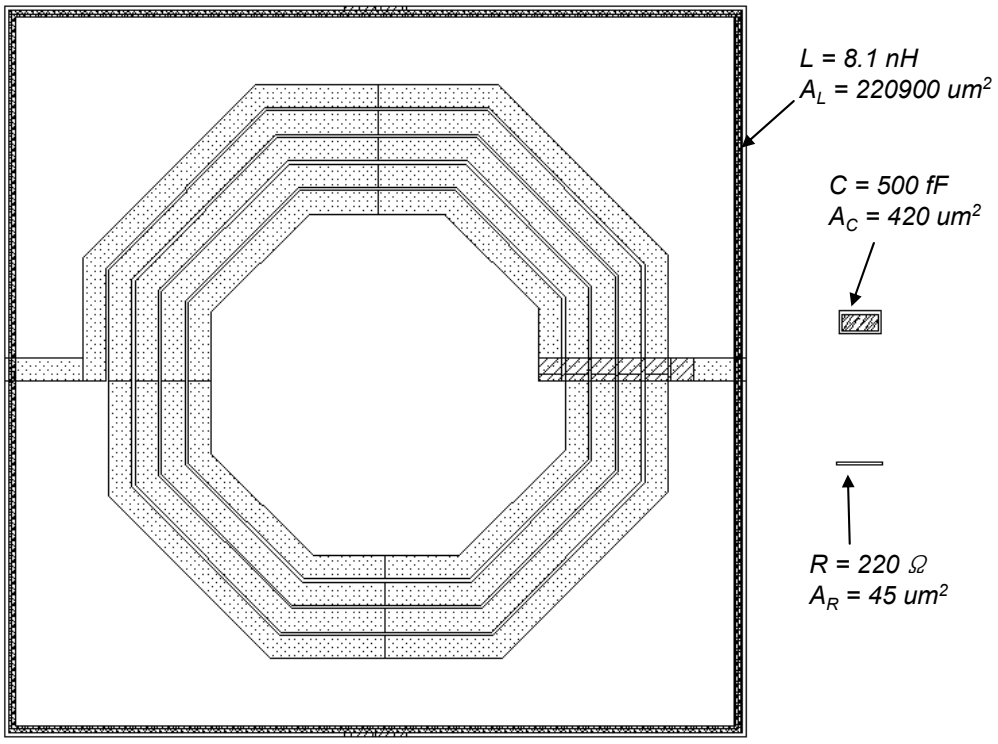


Figure 4. Layout and size of inductor, capacitor and resistor.

A power consumption of both oscillators can be calculated considering an open loop gain at the oscillation frequency of each oscillator should be 1 according to (2-2). Open loop transfer functions are

$$H_{Ring}(j\omega) = \left(\frac{g_m R}{1 + j\omega RC} \right)^3 \tag{2-15}$$

$$H_{LC}(j\omega) = \frac{g_m R_p}{1 + jR_p(\omega C - 1/\omega L)} \tag{2-16}$$

Applying (2-5), (2-6) to (2-15), (2-16) and equalizing gain at ω_0 to 1 yields

$$g_{m,Ring} = \frac{2}{R} \tag{2-17}$$

$$g_{m,LC} = \frac{1}{R_p} \tag{2-18}$$

Note that as ω_0 increases with a fixed C, a power consumption of a ring oscillator is also increased as expressed in (2-17) while a power consumption of a LC oscillator, (2-18), is not frequency dependent.

In RF communication applications, phase noise is main design concern since it degrades the signal purity and increases the signal to noise ratio (SNR) requirement of whole system. Among all design aspects of the VCO mentioned above, phase noise is a unique feature of the VCO. Usually, a phase locked loop (PLL) is used together with the VCO to enhance the frequency accuracy and a long-term stability. However, phase noise of the VCO is not rejected by a PLL.

2.1.3. Phase Noise of the VCO

The term phase noise is widely used to describe random frequency fluctuations of the VCO output signal. Phase noise is usually measured as a skirt around the carrier frequency in frequency-domain spectrum. In time-domain measurement, it is appeared as variations of zero-crossing point. Phase noise may be specified in a number of ways but it can be described using mathematical expressions. Suppose that the VCO output signal is an ideal sine wave that contains only one frequency component. It can be expressed

$$V_{osc}(t) = V_o(1 + A(t))\sin(\omega_0 t + \theta(t)) \tag{2-19}$$

where V_o is the nominal amplitude of the signal, ω_0 is a carrier frequency in radian, and $A(t)$ and $\theta(t)$ denote amplitude and phase variation, respectively. $A(t)$ is generated from non-linear behavior of active devices such as transistors and $\theta(t)$ comes from noises in electronic elements. Note that amplitude variations $A(t)$ can be well controlled with several circuit techniques, and it can be considered as constant over time. Hence, its effect on phase noise through the AM to PM transform can be ignored compared to phase variation [1]. In the discussion that follows, we will assume that $A(t) << 1$.

Frequency spectrum of $\theta(t)$ depends on its noise source, but it is assumed here to be a single frequency tone with the amplitude of A_θ at the frequency of ω_m, $\theta(t) = A_\theta \sin(\omega_m t)$. Assuming the constant amplitude V_0, (2-19) becomes

$$\begin{aligned} V_{osc}(t) &= V_o \sin(\omega_0 t + A_\theta \sin(\omega_m t)) \\ &= V_o \sin(\omega_0 t)\cos(A_\theta \sin(\omega_m t)) + V_o \cos(\omega_0 t)\sin(A_\theta \sin(\omega_m t)) \end{aligned} \tag{2-20}$$

Under a narrow band condition such that $A_\theta << 1$ rad, $\cos(A_\theta \sin(\omega_m t)) \approx 1$ and $\sin(A_\theta \sin(\omega_m t)) \approx A_\theta \sin(\omega_m t)$ that yields the output of the oscillator, (2-20) [2],

$$\begin{aligned} V_{osc}(t) &\cong V_o \sin(\omega_0 t) + V_o \cos(\omega_0 t) A_\theta \sin(\omega_m t) \\ &= V_o \sin(\omega_0 t) + \frac{V_o A_\theta}{2}\left[\sin((\omega_0 + \omega_m)t) - \sin((\omega_0 - \omega_m)t)\right] \end{aligned} \tag{2-21}$$

It can be seen from the equation (2-21) that V_{osc} contains a fundamental carrier tone at ω_0 and two side bands at the offset frequency ω_m from ω_0 with the amplitude scaled by factor of $A_\theta / 2$ from the amplitude of carrier. The spectrum is shown in Figure 5.

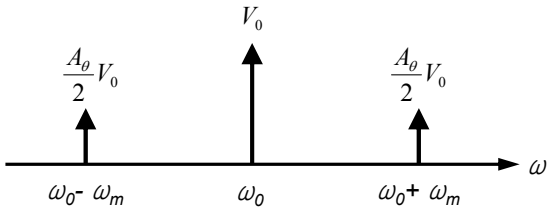


Figure 5. Appearance of sidebands at VCO output.

Power spectral density (PSD) is used to evaluate the carrier and noise power. Only noise power should be normalized by its bandwidth since a carrier is considered as a discrete tone. Single sideband phase noise $\pounds\{\omega_m\}$ is specified in dBc/Hz at a given

frequency offset ω_m from the carrier. The unit dBc/Hz indicates that phase noise measured as relative noise power within 1 Hz bandwidth to the carrier power.

$$£\{\omega_m\} = 10 \times \log\left(\frac{P_{noise}(1Hz\ BW\ at\ \omega_m\ offset)}{P_{carrier}} \right) \tag{2-22}$$

Suppose that Figure 6 is the VCO output spectrum if the measurement is done by a spectrum analyzer. A spectrum analyzer uses a resolution bandwidth (RBW) to calculate a power of spectrum by integrating power spectral density within RBW. Suppose a measured spectrum of Figure 6 such that P_1 is a measured power at $\omega_0 \pm \omega_m$ and RBW is a resolution bandwidth of a spectrum analyzer, then its power spectral density should be P_1 / RBW. If a carrier power at ω_0 is P_0, then phase noise is

$$£\{\omega_m\} = 10 \times \log\left(\frac{P_1}{RBW \times P_0} \right) \tag{2-23}$$

Usually, phase noise is measured using the automatic measurement option in a spectrum analyzer. But, this option does not provide good results when a standalone VCO is measured in which a carrier frequency varies a lot in time. In this case, an equation (2-23) can be used to measure phase noise. This method is useful because it uses a direct snapshot of frequency spectrum fixed at a time. A continuous curve of phase noise can be plotted by taking noise powers as varying the offset frequency ω_m.

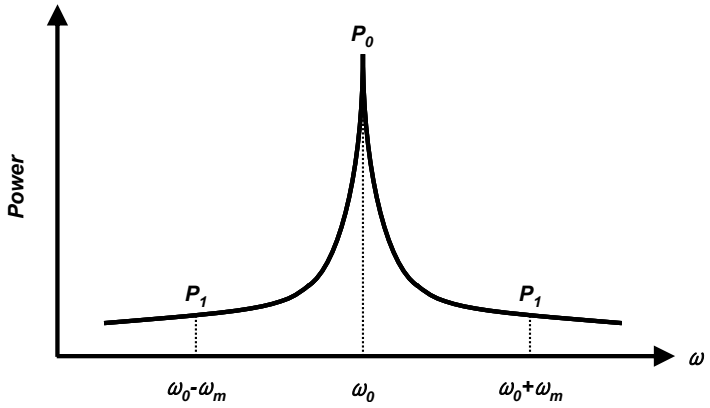


Figure 6. VCO output spectrum of a spectrum analyzer.

There have been several approaches to characterize phase noise in CMOS VCO. Leeson proposed a simple calculation methodology based on a linear time-invariant (LTI) model [3]. More intuitive result using a transfer function in a feedback system based on LTI model was proposed by [4]. Although Leeson's formula includes many characteristics of real oscillators, no formal proof was given by Leeson and his formula includes a noise factor as a "fit" factor [5]. Nevertheless, many design insights provided by phase noise theories with nonlinearity and time-varying aspects [1, 6, 7] can be estimated and explained using LTI oscillator modeling. Also, several publications have been reported that phase noise measurement results can be expected using linear modeling less than 1-4 dB difference [4, 8, 9].

On the other hand, Hajimiri proposed more accurate calculation method with the impulse sensitive function (ISF) by utilizing a linear time variant (LTV) [1]. The major difference between Leeson's LTI modeling and this model, is its time-varying nature. It also assumes linearity for the noise-to-phase transfer function [10] and this linear

relationship was verified by simulations in [1]. ISF is an empirical function that should be determined by a simulation, and is different from each circuit. Determination of the ISF is most straightforwardly performed by replacing the noise sources in an oscillator with impulsive sources of small width and measuring the resultant phase shift. It should be noted that the injected charge and phase variation must have a linear relationship, and injecting too much charge would violate this linear relationship. Since ISF is a periodic function and its period is same with the period of oscillator, repeating this process by injecting the impulse at various times during a period and measuring the resultant phase shift allows the ISF to be calculated [10]. This method is the most accurate one and can be performed using circuit simulators.

2.2. Frequency Synthesizer

2.2.1. Introduction to the Frequency Synthesizer

A frequency synthesizer is a circuit block capable of generating a signal at a specific frequency. The output frequency f_{out} is given as a fixed input reference frequency f_{ref} multiplied by a certain dividing factor N which can be varied by the external control signal ($f_{out} = f_{ref} \times N$). Depending on the type of N (integer or fractional number), frequency synthesizer is called as an integer-N or fractional-N synthesizer. In communication systems, the output signal of the frequency synthesizer (known as local oscillator, LO) is used for the purpose of frequency translation through the mixer. It

down-converts the received RF signal to intermediate frequency (IF) band in the receiver chain, and up-converts IF signal to RF signal which can be transmitted by the transmitter. The frequency accuracy requirement in RF wireless communication system is very strict, normally tens of ppm, which enforce the VCO to be controlled by a certain feedback system. The most popular technique of frequency synthesizer for this purpose is based on the use of PLL. The structure of PLL is similar to the differential amplifier in a negative feedback that cancels out the difference of the input signal and the feed backed output signal. The accuracy of the error is proportional to the amplifier gain. In the PLL, the phase of the input reference clock signal is compared with that of the VCO output signal through a negative feedback. The loop is locked in phase when both phases of the input and output signal are aligned together. The frequency synthesizer is based on the PLL, but it employs the frequency divider and the input reference signal is compared with the divided signal in frequency from the VCO.

2.2.2. Transfer Function of the Frequency Synthesizer

Figure 7 shows the block diagram of a frequency synthesizer linearized in phase-domain. It consists of the phase detector (PD), the loop filter (LF), the VCO and the divider (DIV). Φ_{out} denotes the VCO output phase and, after DIV, it becomes Φ_{div} and Φ_{div} is compared with the input phase Φ_{in}. The output of PD is labeled as V_{PD} in voltage, however its unit can be a current depending on the structure of PD and LF. The VCO gain is K_{VCO}/s since K_{VCO} is a frequency gain and a phase is calculated as the integration

of a frequency. LF has a frequency-dependent gain that includes one pole at the origin and one zero to stabilize the loop.

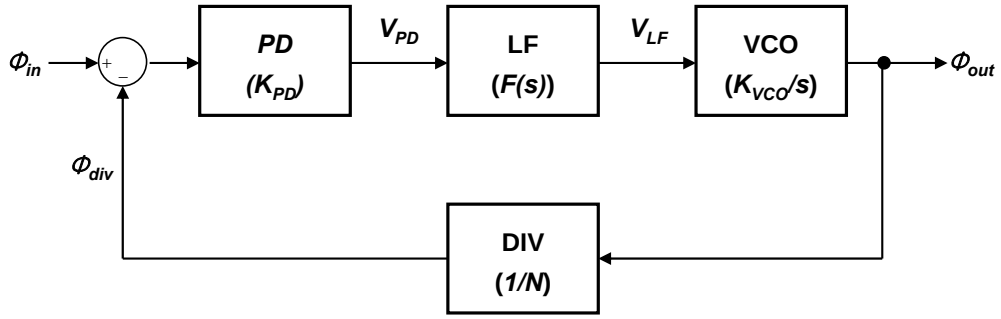


Figure 7. Block diagram of frequency synthesizer.

The type of system refers to the number of poles in the open loop gain located at the origin, i.e. the number of ideal integrators in the PLL. The order of the system refers to the degree of the characteristic equation or the denominator of the closed loop transfer function. In this case, since the PLL has two ideal integrators (one in LF and the other in VCO) and two poles, the PLL is called as type-II second-order. To enhance the spur rejection, another pole is added to LF making PLL type-II third-order which is the most popular structure in the frequency synthesizer. Suppose that the transfer function of LF is

$$F(s) = \frac{1 + s/\omega_z}{s(1 + s/\omega_p)} \tag{2-24}$$

If the loop is open at the output of DIV, then the open loop gain $G(s)$ of Φ_{div} / Φ_{in} can be calculated using the gain of each block. Also, the closed loop transfer function $H(s)$ can be calculated using the open loop gain $G(s)$,

$$G(s) = \frac{\Phi_{div}}{\Phi_{in}} = \frac{K_{PD} \cdot F(s) \cdot K_{VCO}}{N \cdot s} = \frac{\omega_n^{\,2}(1 + s/\omega_z)}{s^2(1 + s/\omega_p)} \tag{2-25}$$

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/\omega_n^{\,2} + s^3/(\omega_p \omega_n^{\,2})} \tag{2-26}$$

where $\omega_n^{\,2} = K_{PD}K_{VCO} / N$. If the natural frequency ω_n is assumed to be much lower than the pole frequency ω_p, then (2-26) can be simplified to be a second-order equation as

$$H(s) \cong = \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/\omega_n^{\,2}} \tag{2-27}$$

In some cases, the loop filter in (2-24) is simplified without ω_p making (2-26) equal to (2-27) as a second-order system. A second-order system has better phase margin than a third-order system, at the cost of a poor spur suppresion.

2.2.3. Design Issues of the Frequency Synthesizer

Stability

Since the frequency synthesizer is a feedback system, the stability is a critical design issue. One of the ways to evaluate the stability of the PLL is to measure the gain margin. A feedback system will become unstable if the magnitude of the open loop response of the system exceeds unity at the frequency for which the open loop phase shift is equal to ±180º. The magnitude of the open loop response at this point is referred to as the gain margin. However, in case of the open loop function described here in (2-25), the gain margin is not relevant since a phase shift never be equal to ±180º.

The Hurwitz criteria can also be used to test the stability. A denominator of the closed loop equation of (2-26) is a characteristic equation. According to the Hurwitz criteria, following conditions must be met for asymptotic stability:

(1) All coefficients must be positive.

(2) $\frac{1}{\omega_p \omega_n^2} < \frac{1}{\omega_z \omega_n^2}$

A condition (1) is satisfied automatically and a condition (2) yields $\omega_p > \omega_z$. However, this is not enough to evaluate the stability of the PLL and the phase margin should be carefully considered from the open loop transfer function $G(s)$. Poor phase margin makes the system unstable and leads the system to oscillate even with small perturbations. In this case, the frequency synthesizer is not capable of generating the signal with a desired frequency. The phase margin can be calculated from (2-25).

Suppose that ω_c is the crossover frequency at which the magnitude of G(s) is equal to 1, $|G(j\omega_c)| = 1$. The phase margin (PM) can be calculated from the phase response of the open loop transfer function (2-25) as

$$\text{PM} = \angle G(j\omega_c) = \tan^{-1}(\omega_c / \omega_z) - \tan^{-1}(\omega_c / \omega_p) \tag{2-28}$$

The transfer function (2-25) can be greatly simplified if ω_z and ω_p are equally spaced from ω_c by the equal ratio-distance (α^2) [11],

$$\begin{aligned} \omega_z &= \omega_c / \alpha^2 \\ \omega_p &= \omega_c \times \alpha^2 \end{aligned} \tag{2-29}$$

Substituting (2-29) into (2-28) yields

$$\text{PM} = \angle G(j\omega_c) = \tan^{-1}(\alpha^2) - \tan^{-1}(1/\alpha^2) \tag{2-30}$$

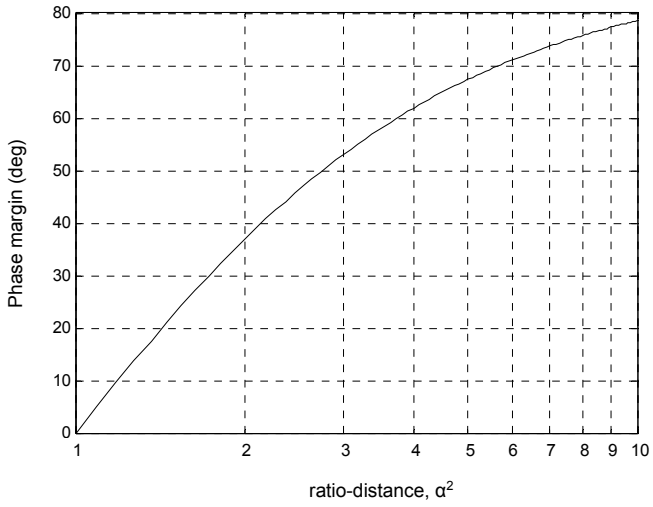


Figure 8. Ratio-distance α^2 versus phase margin.

Figure 8 shows the phase margin as α^2 is varied. When α^2 = 2, 4, 8, phase margins are 37º, 62 º, 76 º, respectively.

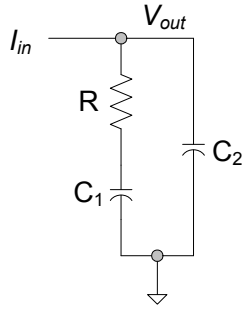


Figure 9. LF structure.

The implementation of α^2 is related to the parameters in LF. If the structure of LF is the one in Figure 9, the transfer function Z(s) becomes

$$Z(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{1}{\frac{1}{R + 1/sC_1} + sC_2} = \frac{1 + sRC_1}{s(C_1 + C_2 + sRC_1C_2)} \tag{2-31}$$

If $C_1 >> C_2$, then (2-31) is simplified as

$$Z(s) \cong \frac{1 + sRC_1}{sC_1(1 + sRC_2)} \tag{2-32}$$

Equating the pole and zero of (2-32) with those in (2-24) yields $\omega_z = 1 / RC_1$ and $\omega_p = 1 / RC_2$. Applying these equations to(2-29), α^2 becomes

$$\alpha^2 = \sqrt{\frac{\omega_p}{\omega_z}} = \sqrt{\frac{C_1}{C_2}} \tag{2-33}$$

(2-33) indicates that higher α^2 requires higher capacitor ratio between C_1 and C_2 resulting in larger silicon area. For example, if α^2 is designed as 4, then C_1 / C_2 should be 16. $\alpha^2 = 4$ is practically considered as optimized since it yields a descent phase margin of 62º and the settling time as will be discussed in the following section.

Another stability limit comes from the structure of the frequency synthesizer. The most popular structure is to implement PD in Figure 7 with a digital gate phase frequency detector (PFD) and a charge pump (CP). In this structure, PFD compares the phases and CP operates in every input reference cycle, which is the discrete nature of the

PFD and CP. This puts a critical stability limitation on the input reference frequency ω_{ref} and the natural frequency ω_z. In [12], Gardner has derived the characteristic equation (denominator of the transfer function) of the sampled PLL in the z-plane using a linearized, sampled analysis.

$$\begin{aligned} D(z) &= (z-1)^2 + (z-1)\frac{2\pi K'}{\omega_{ref}/\omega_z}\left[1+\frac{2\pi}{\omega_{ref}/\omega_z}\right] + \frac{4\pi^2 K'}{(\omega_{ref}/\omega_z)^2} \\ &= z^2 - 2r\cos\theta \cdot z + r^2 \end{aligned} \tag{2-34}$$

$$r^2 = 1 - \frac{2\pi K'}{\omega_{ref}/\omega_z}, \quad \cos\theta = \frac{2 + \frac{2\pi K'}{\omega_{ref}/\omega_z}\left[1+\frac{2\pi}{\omega_{ref}/\omega_z}\right]}{2\sqrt{1-\frac{2\pi K'}{\omega_{ref}/\omega_z}}}$$

where $K' = \omega_n^2 / \omega_z^2$ and ω_{ref} is a reference frequency in radian. (2-34) was derived from the second-order PLL, but it is also valid for the third-order PLL if the same assumption, $C_1 >> C_2$ which is used to derive (2-32) from (2-31), is made. The loop stability can be evaluated by examining the locations of the poles of the z-domain transfer function, i.e. the zeros of D(z) in (2-34).

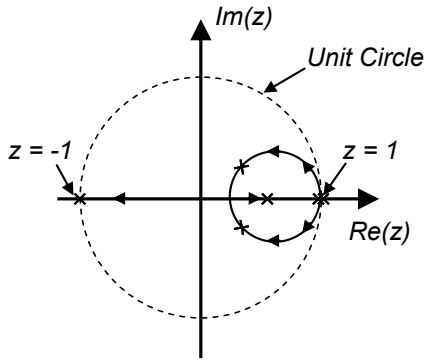


Figure 10. Root locus plot in z-plane.

The root locus shows pole locations in the z-plane for varying *K'* as sketched in Figure 10. The two poles start at z = 1 for *K'* = 0 and move on a circle as conjugate poles. For larger *K'*, the poles become real poles and they lie on the real axis. One pole moves towards the center of the locus circle and the other pole approaches towards z = -1. This pole crosses the unit circle when

$$K' = \frac{1}{\frac{\pi}{\omega_{ref}/\omega_z}\left(1+\frac{\pi}{\omega_{ref}/\omega_z}\right)} \tag{2-35}$$

(2-35) is the stability limit for K' and the loop can be stable for smaller K' than the value of (2-35).

$$K' < \frac{1}{\frac{\pi}{\omega_{ref}/\omega_z}\left(1+\frac{\pi}{\omega_{ref}/\omega_z}\right)} \tag{2-36}$$

Considering $K' = \omega_n^2 / \omega_z^2$, $\omega_n^2 = \omega_z \omega_c$, (2-36) becomes

$$\frac{\omega_c}{\omega_{ref}} < \frac{1}{\pi\left(1 + \frac{\pi}{\omega_{ref} / \omega_z}\right)} \tag{2-37}$$

Substituting (2-29) into (2-37) yields

$$\frac{\omega_c}{\omega_{ref}} < \frac{\sqrt{\alpha^2\left(\alpha^2 + 4\right)} - \alpha^2}{2\pi} \tag{2-38}$$

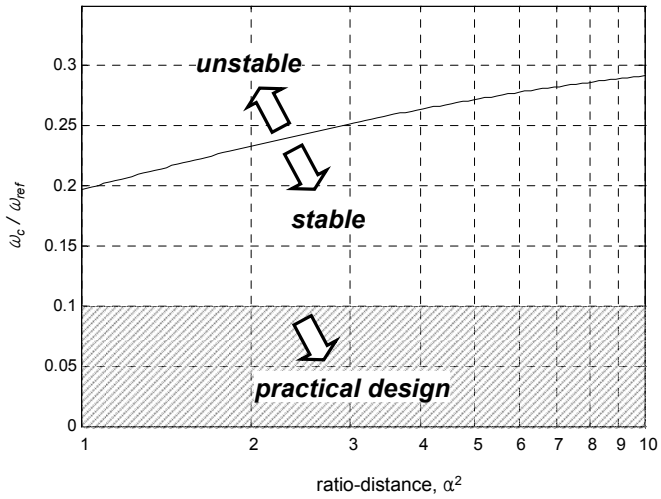


Figure 11. Stability boundary for ω_c / ω_{ref} versus α^2.

According to (2-38), a stability boundary can be determined by the ratio of ω_c over ω_{ref} when α^2 varies, and the result is plotted in Figure 11. Although (2-38) states the exact

stability boundary due to the sampling nature, commonly ω_c is chosen below one tenth of ω_{ref} to guarantee stability considering the design margin and process variations.

$$\omega_c \cong \frac{\omega_{ref}}{10} \tag{2-39}$$

Settling Time

The settling time t_s is defined as an elapsed time that the frequency synthesizer is settled to final steady state within a certain amount of error. An analytical solution of the settling time can be achieved from the approximated second-order equation of (2-27). A second-order solution is used here since it provides simpler and more intuitive results. Rewriting (2-27) as

$$H(s) \cong \frac{\omega_n^{\,2}}{\omega_z} \frac{s+\omega_z}{s^2 + \frac{\omega_n}{\omega_z}\omega_n s + \omega_n^{\,2}} = \frac{2\zeta\omega_n\left(s+\frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \tag{2-40}$$

where a damping factor $\xi = \omega_n / (2\omega_z)$. Poles of (2-40) can be real or complex poles depending on a damping factor ξ as

$$\omega_{p1,p2} = \begin{cases} -\omega_n\left(\xi \pm j\sqrt{1-\xi^2}\right) & \xi < 1 \\ -\omega_n\xi & \xi = 1 \\ -\omega_n\left(\xi \pm \sqrt{\xi^2-1}\right) & \xi > 1 \end{cases} \tag{2-41}$$

If the output frequency step Δf is given to the system as an input, then corresponding output frequency step response would be [13]

$$\Delta f_{out}(s) = \Delta f \frac{H(s)}{s} = \Delta f \frac{2\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s\left(s^2 + 2\zeta\omega_n s + \omega_n{}^2\right)} \tag{2-42}$$

(2-42) can be decomposed using the poles defined in (2-41) as

$$\Delta f_{out}(s) = \Delta f\left(\frac{1}{s} + \frac{\omega_{p1}/\left(\omega_{p1}-\omega_{p2}\right)}{s-\omega_{p1}} - \frac{\omega_{p2}/\left(\omega_{p1}-\omega_{p2}\right)}{s-\omega_{p2}}\right) \tag{2-43}$$

Substituting (2-41) to (2-43) yields

$$\Delta f_{out}(s)=\begin{cases}\Delta f\left(\dfrac{1}{s}+\dfrac{\omega_{p1}/j2\omega_n\sqrt{1-\xi^2}}{s-\omega_{p1}}-\dfrac{\omega_{p2}/j2\omega_n\sqrt{1-\xi^2}}{s-\omega_{p2}}\right) & \xi<1\\ \Delta f\left(\dfrac{1}{s}-\dfrac{1}{s-\omega_n}+\dfrac{\omega_n}{(s-\omega_n)^2}\right) & \xi=1\\ \Delta f\left(\dfrac{1}{s}+\dfrac{\omega_{p1}/j2\omega_n\sqrt{\xi^2-1}}{s-\omega_{p1}}-\dfrac{\omega_{p2}/j2\omega_n\sqrt{\xi^2-1}}{s-\omega_{p2}}\right) & \xi>1\end{cases} \quad (2\text{-}44)$$

Applying the inverse Laplace transform to (2-44), it becomes the time-domain function as

$$\Delta f_{out}(t)=\begin{cases}\Delta f\left(1+\dfrac{\omega_{p1}e^{-\omega_{p1}t}-\omega_{p2}e^{-\omega_{p2}t}}{j2\omega_n\sqrt{1-\xi^2}}\right) & \xi<1\\ \Delta f\left(1-e^{-\omega_n t}(1-\omega_n t)\right) & \xi=1\\ \Delta f\left(1+\dfrac{-\omega_{p1}e^{-\omega_{p1}t}+\omega_{p2}e^{-\omega_{p2}t}}{2\omega_n\sqrt{\xi^2-1}}\right) & \xi>1\end{cases} \quad (2\text{-}45)$$

Substituting (2-41) to (2-45) yields

$$\Delta f_{out}(t) - \Delta f = \begin{cases} \Delta f e^{-\xi\omega_n t}\left(\dfrac{\xi}{\sqrt{1-\xi^2}}\sin\left(\omega_n\sqrt{1-\xi^2}\,t\right) - \cos\left(\omega_n\sqrt{1-\xi^2}\,t\right)\right) & \xi < 1 \\ -\Delta f e^{-\omega_n t}\left(1-\omega_n t\right) & \xi = 1 \\ \Delta f e^{-\xi\omega_n t}\left(\dfrac{\xi}{\sqrt{1-\xi^2}}\sinh\left(\omega_n\sqrt{\xi^2-1}t\right) - \cosh\left(\omega_n\sqrt{\xi^2-1}t\right)\right) & \xi > 1 \end{cases} \tag{2-46}$$

As t is increased to the settling time t_s, $\Delta f_{out}(t)$ becomes close enough to the final value of Δf within the settling accuracy δ.

$$\left|\Delta f_{out}(t_s) - \Delta f\right| = \delta \tag{2-47}$$

Substituting (2-46) to (2-47) and solving yields the settling time t_s expressed as [13, 14],

$$t_s \cong \begin{cases} \dfrac{1}{\xi\omega_n}\ln\dfrac{\Delta f}{\delta f\sqrt{1-\xi^2}} & \xi < 1 \\ \dfrac{1}{\xi\omega_n}\ln\dfrac{\Delta f}{\delta} & \xi = 1 \\ \dfrac{1}{\left(\xi-\sqrt{\xi^2-1}\right)\omega_n}\ln\dfrac{\Delta f\left(\xi+\sqrt{\xi^2-1}\right)}{2\delta\sqrt{1-\xi^2}} & \xi > 1 \end{cases} \tag{2-48}$$

Considering the additional pole effect in addition to (2-40), the actual settling time would be longer than (2-48). The important observation from (2-48) is that if a damping

factor ξ is fixed, then the loop bandwidth ω_c is proportional to the natural frequency ω_n, as a result, the settling time is inversely proportional to ω_c. A damping factor ξ can be expressed as a function of a ratio-distance α^2. Using the relationships $\xi = \omega_n / (2\omega_z)$, $\omega_c = \alpha\omega_n$, $\omega_z = \omega_c / \alpha^2$, a damping factor becomes

$$\xi = \frac{\alpha}{2} \tag{2-49}$$

A damping factor is usually determined by considering the loop stability, but it also contributes to change the settling time. Figure 12 shows the settling time normalized to ω_n versus α^2. From this plot, it can be concluded that the settling time is minimized around $\alpha^2 = 4$ where the system is critically damped, and dividing y-axis value by ω_n yields actual settling time. If a damping factor is greater than 1, $\alpha^2 > 4$ from (2-49), from Figure 8 and Figure 12, the system has a good phase margin (greater than 62º) at cost of an increased settling time.

For a numerical example, consider IEEE 802.15.4 ZIGBEE standard. It has to cover 2405 – 2480 MHz with a 5 MHz step. A required settling time is 192 μs with 40 ppm accuracy [15]. From the specifications, some parameters can be set as Δf = 75 MHz, δ = 4 ppm and f_{ref} = 5 MHz. For optimal phase margin and settling time, a damping factor is set to 1, $\xi = 1$, which leads to ratio-distance of 4, $\alpha^2 = 4$ from (2-49). Since f_{ref} = 5 MHz, maximum possible loop bandwidth f_c = 500 KHz.

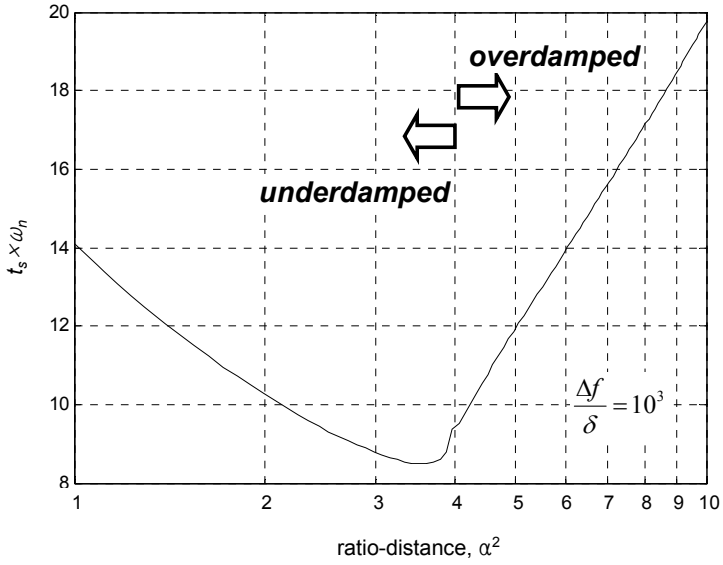


Figure 12. Normalized settling time as a function of α^2.

A natural frequency f_n becomes 250 KHz using the relationship of $f_n = f_c / \alpha$. Calculating a settling time using (2-48), t_s = 18 μs which is well below than the specification of 192 μs. Even though considering a settling time margin from (2-48), it can be known that a loop bandwidth f_c can be reduced by 10 times, f_c = 50 KHz that yields t_s = 180 μs, according to the settling time specification.

Noise

The noise is main design concern of the frequency synthesizer. Since it consists of a number of building blocks, each noise source can be identified as shown in Figure 13. Φ_{n1} is a noise source added to a reference input, and since a crystal oscillator is normally used for a reference input, Φ_{n1} can be referred to a noise of a crystal oscillator.

It also includes noise coming from a frequency divider block. Since Φ_{n2} is a noise source added to the frequency synthesizer output, it is phase noise of a VCO. V_{n1} is denoted to be added at the output of LF, hence it is a output noise from LF.

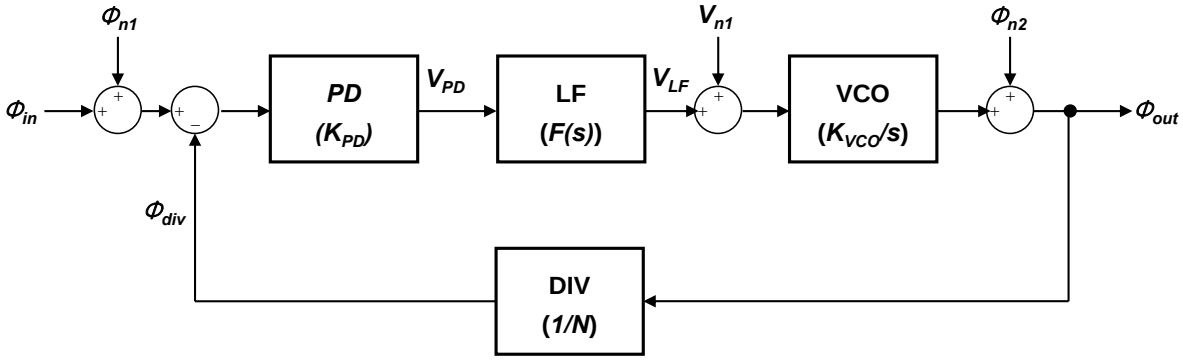


Figure 13. Frequency synthesizer with noise sources.

All buildings generate noise and these noises are appeared as the output phase noise via corresponding transfer functions. Figure 13 shows three main noise sources: the input noise, the noise between the LF and VCO, and the VCO output noise. The PD and DIV also generate noises at their outputs, but they are easily referred to the input noise using the linear transform. The transfer functions from individual noise sources to the output phase noise can be expressed as

$$H_1(s) = \frac{\Phi_{out}}{\Phi_{n1}} = \frac{NK_{PD}K_{VCO}F(s)}{N \cdot s + K_{PD}K_{VCO}F(s)} \tag{2-50}$$

$$H_2(s) = \frac{\Phi_{out}}{V_{n1}} = \frac{N \cdot K_{VCO}}{N \cdot s + K_{PD}K_{VCO}F(s)} \tag{2-51}$$

$$H_3(s) = \frac{\Phi_{out}}{\Phi_{n2}} = \frac{N \cdot s}{N \cdot s + K_{PD} K_{VCO} F(s)} \tag{2-52}$$

If LF is assumed to be (2-24) which has one pole at the origin, another pole and a zero, then (2-50), (2-51) and (2-52) become

$$H_1(s) = \frac{\Phi_{out}}{\Phi_{n1}} = \frac{NK_{PD}K_{VCO}(1 + s/\omega_z)}{Ns^2(1 + s/\omega_p) + K_{PD}K_{VCO}(1 + s/\omega_z)} \tag{2-53}$$

$$H_2(s) = \frac{\Phi_{out}}{V_{n1}} = \frac{NK_{VCO}s(1 + s/\omega_p)}{Ns^2(1 + s/\omega_p) + K_{PD}K_{VCO}(1 + s/\omega_z)} \tag{2-54}$$

$$H_3(s) = \frac{\Phi_{out}}{\Phi_{n2}} = \frac{Ns^2(1 + s/\omega_p)}{Ns^2(1 + s/\omega_p) + K_{PD}K_{VCO}(1 + s/\omega_z)} \tag{2-55}$$

The behaviors of each transfer function can be intuitively estimated by examining the absolute gain at DC and infinite frequency. $|H_1(0)|$ = N and $|H_1(j\infty)|$=0 mean that $H_1(s)$ is a low-pass filter with DC gain of N. For $H_2(s)$, $|H_2(0)|$ = 0 and $|H_2(j\infty)|$=0, hence it is a band-pass filter with a center frequency around ω_c and the gain is proportional to K_{VCO}. $H_3(s)$ is a high-pass filter with a pass-band gain of 1 since $|H_3(0)|$ = 0 and $|H_3(j\infty)|$=1.

MATLAB simulation can be used to plot above transfer functions under specific conditions. Suppose that a dividing factor N is 1000, the normalized loop bandwidth ω_c = 1, ratio-distance α^2 of 4, $K_{PD}K_{VCO}$ = 250 and K_{VCO} = 50. The results applying these assumptions into (2-47), (2-48) and (2-49) are plotted in Figure 14.

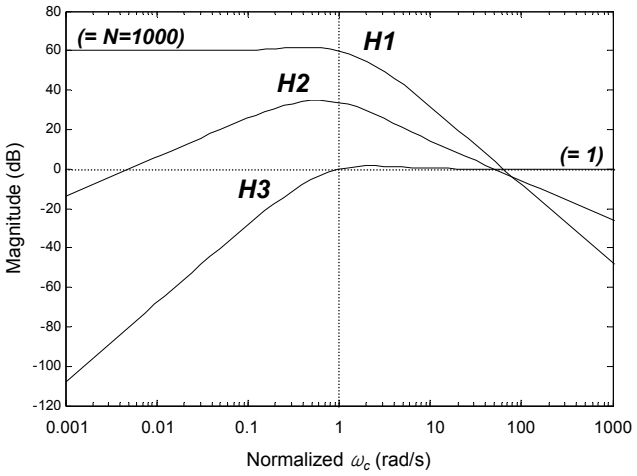


Figure 14. Noise transfer functions.

It should be mention that close-in noise (noise within the loop bandwidth) is dominated by the input noise and is multiplied by the dividing factor N. The VCO noise dominates the noise above the loop bandwidth. Also, the noise at the VCO input around the loop bandwidth is multiplied by the VCO gain K_{VCO} and appeared at the VCO output. Figure 14 indicates that the loop bandwidth should be optimized depending on the dominant noise source in the loop.

Divider Structure

The purpose of divider block in the frequency synthesizer is to divide the VCO frequency or phase with the predefined dividing factor N and provide it to the PFD. Since the PFD compare the phases of the input reference signal and the divider output at every reference cycles, the frequency of the divider output should be exactly matched

with the reference frequency. Normally, the dividing factor N is set by the external digital bit so that the VCO output frequency can be tuned by adjusting N. The divider can be categorized into two main architectures depending on the number type of N. An integer-N divider uses an integer number of N while N is a fractional number in a fractional-N divider.

The most popular structure of an integer-N divider is to have a dual-modulus prescaler whose modulus is controlled by two counters. Depending on the numbers in the prescaler and two counters, the total dividing factor is determined. At every N VCO cycles, the divider output is repeated and the N is an integer number. On the other hand, a fractional-N divider divides the VCO frequency by (N+1) during K VCO cycles and N during (F-K) VCO cycles. Hence, an average dividing number during F divider cycles is ((N+1)K + N(F-K)) / F = N + K/F.

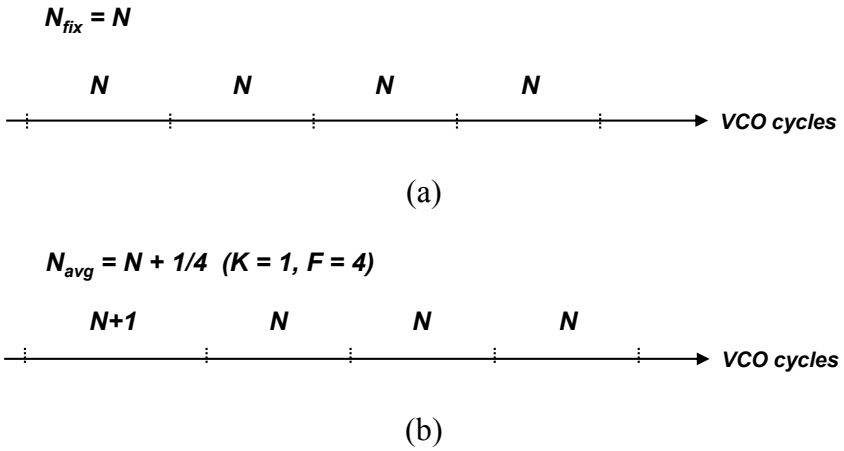


Figure 15. Operation of dividers. (a) Integer-N. (b) Fractional-N.

Figure 15 depicts how the divider counts the VCO cycles. Shown in Figure 15 (a), an integer-N divider counts the same N VCO cycles always. Figure 15 (b) shows a fractional-N divider case when K = 1 and F = 4, and in this case, the dividing factor becomes N + 1/4. If the same pattern as shown in Figure 15 (b), then a fractional spur at lower frequency than a reference frequency will arise and it is hard to remove. A sigma-delta modulator is used to randomize the place of (N+1) VCO cycles part to push fractional spurs to higher frequency.

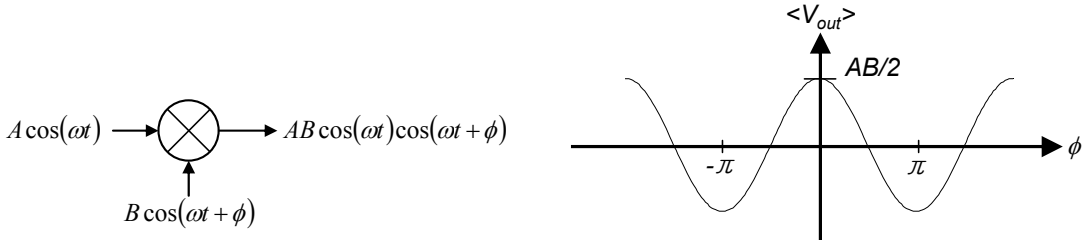
A fractional-N dividing factor provides a good design flexibility at a given frequency specification, allowing higher reference frequency. This is because that the maximum reference frequency in an integer-N divider is limited to the greatest common divisor (GCD) of the minimum channel frequency and the channel spacing [14]. For an example, suppose that the frequency synthesizer should cover U-NII upper frequency band with 20 MHz channelization. Frequencies in this band are 5745 MHz, 5765 MHz, 5785 MHz, 5805 MHz and 5825 MHz. If an integer-N divider is used, the reference frequency is f_{ref} = GCD(5745 MHz, 20 MHz) = 5 MHz, and N = 1149. In case of a fractional-N divider, one of the possible dividing factors can be 5745 MHz / 20 MHz = 287 + 1/4. Hence, a fractional divider can be designed such as N = 287, K = 1 and F = 4 with f_{ref} = 20 MHz. Comparing f_{ref} and N in both dividers, a fractional-N divider allows higher f_{ref} and lower N than an integer-N divider. The benefits of a fractional divider can be described such that high f_{ref} and low N yield a fast settling time and low close-in phase noise, respectively. However, an integer-N divider is still attractive and preferred due to the simple structure and lower power consumption.

Phase – Frequency Detector

The role of the phase detector (PD) is to produce a signal which is linearly proportional to the phase error between two input signals, i.e. a reference input signal and a signal from divider. The output can be various forms such as timing pulses, voltage waveforms or current signals, depending on the type of next block.

Phase detectors can be implemented in different ways and one of the possible architecture is analog mode phase detector using multiplier. As shown in Figure 16, if two inputs are Acos(ωt) and Bcos($\omega t+\phi$), then the PD output is

$$V_{out} = AB\cos(\omega t)\cos(\omega t+\phi) = \frac{AB}{2}\left[\cos\phi - \cos(2\omega t+\phi)\right] \qquad (2\text{-}56)$$



(a) (b)

Figure 16. Multiplier as PD. (a) Diagram. (b) Averaged output.

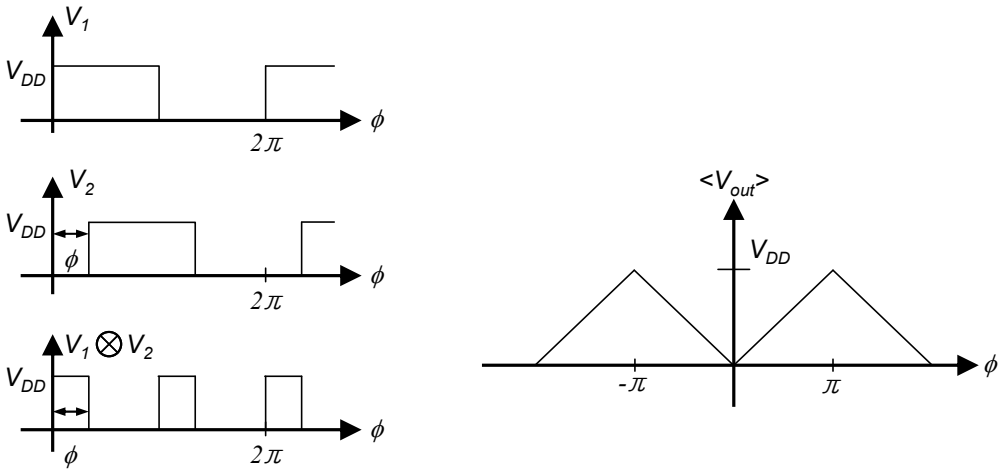
Note that (2-56) has DC component which is related to the phase detection. The average output of PD is

$$\langle V_{out} \rangle = \langle AB\cos(\omega t)\cos(\omega t + \phi) \rangle = \frac{AB}{2}\cos\phi \tag{2-57}$$

PD gain "constant" is a function of the phase angle and is given by [16]

$$K_{PD} = \frac{d\langle V_{out} \rangle}{d\phi} = \frac{-AB}{2}\sin\phi \tag{2-58}$$

Alternative architecture is to use digital exclusive–OR (XOR) gate as a PD. Since required inputs are digital signals, XOR-gate PD is a digital PD.



(a) (b)

Figure 17. XOR-gate as PD (a) Inputs and output. (b) Averaged output.

Figure 17 (a) shows inputs and output waveforms of XOR-gate PD. If V_2 has a phase difference of ϕ from V_1, the averaged resulting out $<V_{out}> = 2\phi V_{DD} / 2\pi$. Hence, PD gain is

$$K_{PD} = \frac{d\langle V_{out} \rangle}{d\phi} = \frac{V_{DD}}{\pi} \tag{2-59}$$

The most popular structure among several phase detectors is the phase-frequency detector (PFD) [17]. It is a sequential PFD and is based on D-type fli-flop (DFF). Two DFF's are used and each input signals are connected their clock port while D-input is tied to V_{DD}, and both DFF's are reset when two outputs are high.

The operation of this PFD is depicted in Figure 18. V_1 and V_2 are inputs and V_{o1} and V_{o2} are DFF outputs correspondingly. Resulting out is taken from the difference of V_{o1} and V_{o2}, $V_{out} = V_{o1} - V_{o2}$. Figure 18 (a) is the case when V_1 leads V_2, and (b) is the case when V_2 leads V_1. Therefore, the gain of this PFD is

$$K_{PD} = \frac{d\langle V_{out} \rangle}{d\phi} = \frac{V_{DD}}{2\pi} \tag{2-60}$$

This PFD often used with charge pump circuit (CP) and each PFD output, V_{o1} and V_{o2}, are control signal to the switches in CP. If the current source in CP is I_{CP}, then total gain includes I_{CP} and it becomes

$$K_{PD} = \frac{I_{CP}}{2\pi} \tag{2-61}$$

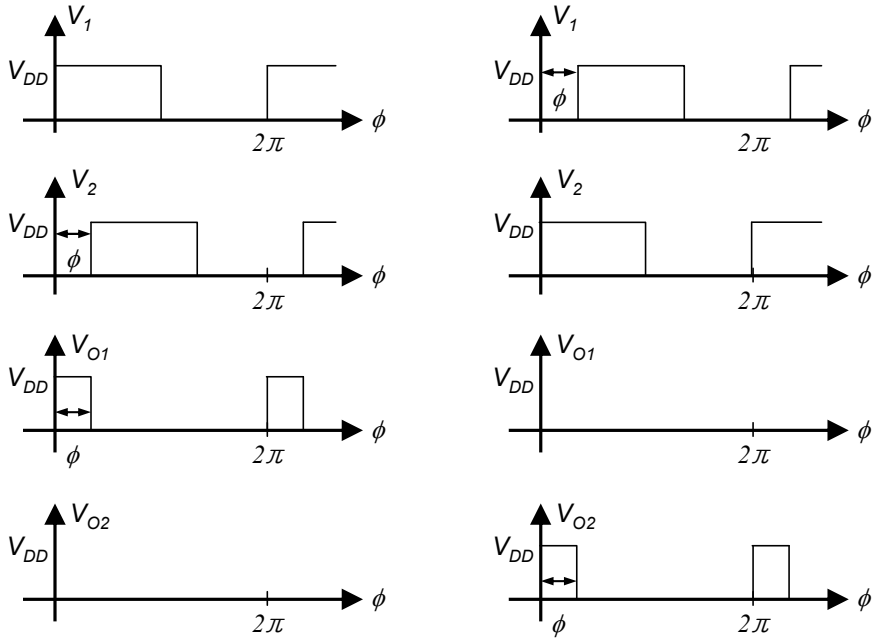


Figure 18. DFF based sequential PFD. (a) Input waveforms for positive ϕ. (b) Input waveforms for negative ϕ. (c) Averaged output.

2.3. Conclusion

Several aspects in designing the VCO and the frequency synthesizer have been described. The VCO is the key building block and phase noise is the most critical performance parameter in RF communication applications because phase noise of the VCO is not rejected even with employing the PLL. THD is the key issue for the VCO for the built-in testing, and the jitter is important for clock generation VCO.

The frequency synthesizer incorporates the VCO with a negative feedback to tune the output frequency in very accurate way. When the frequency synthesizer is designed, the stability and settling time should be carefully examined, and noise transfer functions should be considered to count all various noise sources. The divider architecture also should be carefully chosen to optimize the frequency synthesizer design.

CHAPTER III

NON-LINEAR SHAPING SC OSCILLATOR WITH ENHANCED LINEARITY

3.1. Introduction

Sine-wave oscillators [18, 19] are essential parts in many electronic systems and in a host of applications. It can be used in measurement, testing instrumentation and telecommunication systems [20], [21]. Integrating the oscillator with the other circuit blocks on a single chip makes it easy and reliable to implement several applications including built-in testing [22]. Although there are various methods to realize an oscillator, a band-pass filter (BPF)-based oscillator is an attractive and practical implementation due to its many advantages such as the possibility of tuning the oscillation frequency by means of changing the center frequency (f_0) of the BPF [23], and the fact that the oscillation amplitude can be controlled with the help of a comparator [24]. A BPF with a center frequency below 10 MHz can be implemented with conventional switched-capacitor (SC) design techniques if the Q-factor value is not very large (< 10). SC design technique is preferred because of its accuracy, simple implementation and reduced sensitivity to process and temperature variations. Due to these attractive features, SC BPF-based oscillator has been used for several industrial applications such as dual-tone multi-frequency (DTMF) signal generator [25]. However, an SC circuit is difficult to be used for high frequency applications requiring a very high clock frequency since there are significant limitations on the speed of switches and

amplifiers. Another limitation is the chip area which is mostly consumed by capacitors that is a key cost factor for SC circuits. Conventional approaches to minimize the frequency harmonics of the SC BPF-based oscillator requires a high quality-factor (Q-factor) BPF, which involves high capacitor spread and, hence, leads to large silicon area [26]. Several efforts to obtain high Q-factor BPF that does not have such increased capacitor spread have been proposed using a double-sampling [26] and a cascaded N-path filter structure [27]. However, these approaches are sensitive to the mismatch among different paths [27] and still require a large silicon area compared to a low Q-factor BPF [26]. Other techniques reduce the allowed signal bandwidth and require a more complex digital section [28]. Recently, non-linear shaping for enhanced linearity for a mixer has been reported [29]. In this work, a technique based on non-linear shaping of the frequency spectrum is proposed to improve the linearity of SC BPF-based oscillator without requiring a high Q-factor BPF.

3.2. Background of BPF-Based Oscillator

3.2.1. Oscillator with Conventional Comparator

The block diagram of a conventional SC BPF-based oscillator is shown in Figure 19. A BPF with high selectivity (Q-factor) is used together with a two-level comparator yielding a sinusoidal signal (V_{out}). The feedback through the comparator should be positive and, due to its high gain, the poles of the closed loop are initially placed at the

right half plane causing the oscillation to start. Due to the nonlinear action of the comparator, the poles are placed on the unit circle on the z-plane [24], or on the $j\omega$-axis in the s-plane if a continuous-time filter is used [30].

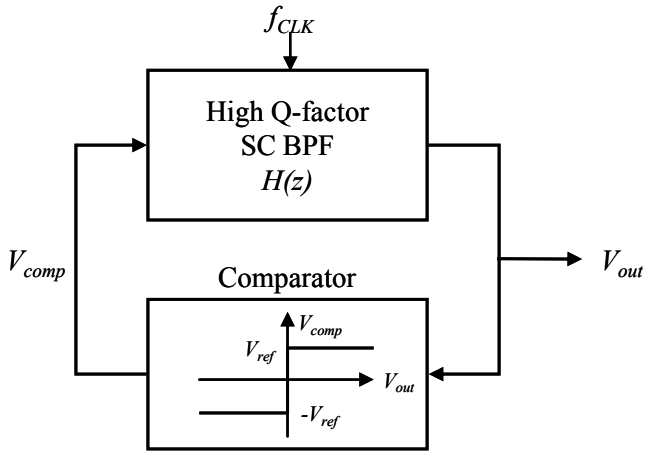


Figure 19. Block diagram of conventional BPF-based SC oscillator.

Assume *H(z)* in Figure 19 is a second-order BPF and a comparator is replaced with a linear feedback gain β. The open loop transfer function of a second-order BPF, *H(z)* can be expressed as

$$H(z) = \frac{k\left(1 - z^{-2}\right)}{1 - 2r\cos\theta z^{-1} + r^2 z^{-2}} \tag{3-1}$$

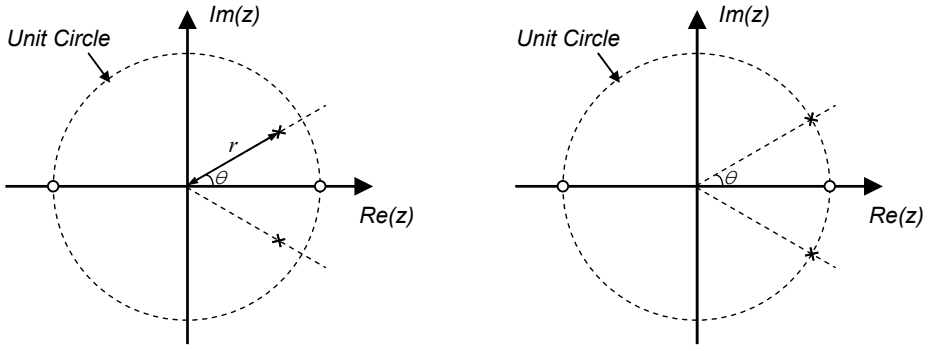
where k is a gain factor, and r and θ are magnitude and angle of poles assuming two poles $z_{p1,2} = re^{\pm j\theta}$. The location of poles and zeros is plotted in Figure 20 (a). To maintain the stability of a BPF, two poles should be inside of the unit circle, $r < 1$. If a BPF of

(3-1) forms a positive feedback with a linear gain of β, a closed loop transfer function $H_{closed}(z)$ becomes

$$H_{closed}(z) = \frac{k}{1-k\beta} \frac{1-z^{-2}}{1-\frac{2r\cos\theta}{1-k\beta}z^{-1}+\frac{r^2+k\beta}{1-k\beta}z^{-2}} \tag{3-2}$$

Barkhausen conditions can be applied to (3-2) such that poles of a closed loop equation should be on the unit circle. A modified radius of poles from (3-2) due to a feedback gain β is the coefficient of z^{-2} of a denominator in (3-2) and should be 1.

$$\frac{r^2+k\beta}{1-k\beta} = 1 \tag{3-3}$$



(a) (b)

Figure 20. Location of poles and zeros. (a) Open loop. (b) Closed loop.

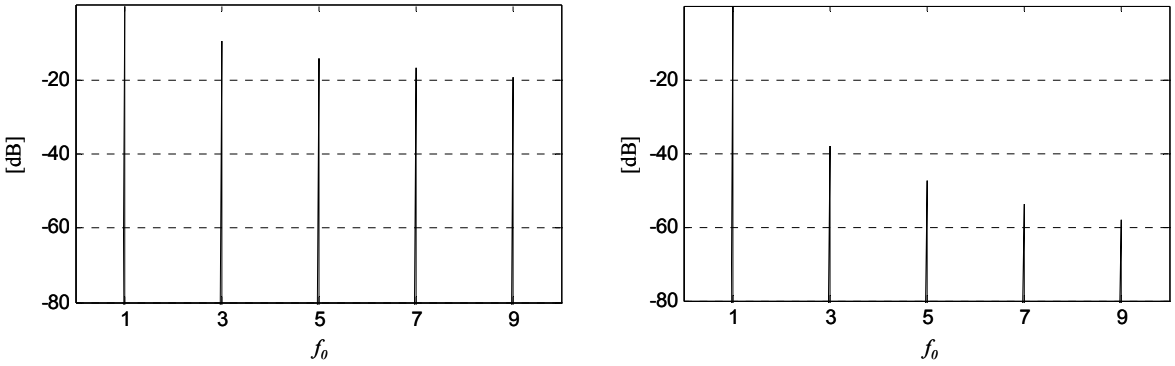
Figure 20 (b) shows the location of poles and zeros of a closed loop equation (3-2) when the condition of (3-3) is satisfied. Rewriting (3-3) for β gives the oscillation condition such as

$$\beta = \frac{1 - r^2}{2k} \tag{3-4}$$

It can be known that poles of a BPF initially inside of the unit circle, and once a positive feedback is formed with a gain of β, poles are moved toward outside of the unit circle.

The oscillation frequency can be tuned if the technique of tuning the center frequency of SC BPF is applied [31], and wide tuning range can be achieved at the expense of silicon area. Furthermore, the amplitude at the output of the comparator (V_{comp}) is always limited by V_{ref} regardless of the amplitude of V_{out} assuming it is high enough to activate the comparator. For a given ± V_{ref}, the amplitude of V_{out} is controlled by the gain of the BPF. Assume that V_{out} in Figure 19 is a sinusoidal wave and the comparator converts it into a symmetric square wave (V_{comp}). This square wave will have a fundamental tone at the center frequency of the BPF, as well as an infinite number of odd harmonics. Under the very high Q-factor assumption, only the fundamental tone is passed while all the other harmonics are filtered out by the BPF and, hence, V_{out} should ideally be a sinusoidal signal. However, due to the finite Q-factor of the BPF, the harmonics adjacent to the center frequency of the BPF are present at the output, which give rise to nonlinearities in V_{out} and thus the total harmonic distortion (THD) is

degraded. To illustrate this, Figure 21 shows a MATLAB behavioral simulation where the Q-factor was set to 10 and a second-order BPF was used. The nth harmonic distortion of a second-order BPF-based oscillator's output signal, V_{out}, can be approximated [24] as $HD(n) \approx 1 / (n^2 Q)$, where Q is the quality-factor of the BPF. Note that nth harmonic of V_{comp} that is a square wave, is $HD(n) = 1 / n$.



(a) (b)

Figure 21. Simulated frequency spectrum of (a) V_{comp} and (b) V_{out} for Q=10 and the second-order BPF.

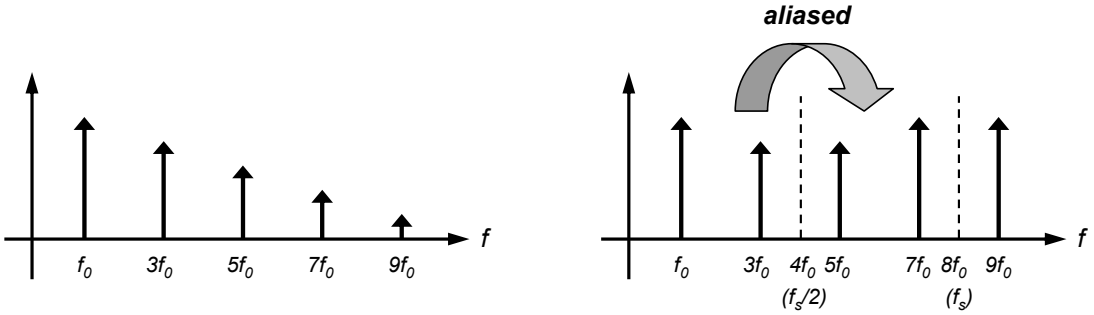
If Figure 21 (a) and (b) are analyzed in continuous time, THD can be calculated by adding all harmonic to infinite index distortions such as

$$THD = \sqrt{HD_3^{\,2} + HD_5^{\,2} + ... + HD_{2n+1}^{\,2} + ...} \qquad (3\text{-}5)$$

Applying $HD(n)$ of V_{comp} and V_{out} to (3-5), THD can be expressed as

$$THD_{\_Vcomp} = \sqrt{\frac{1}{3^2}+\frac{1}{5^2}+\frac{1}{7^2}+\ldots} = \sqrt{\sum_{k=1}^{\infty}\frac{1}{(2k+1)^2}} = \sqrt{\frac{\pi^2}{8}-1} \tag{3-6}$$

$$THD_{\_Vout} = \frac{1}{Q^2}\sqrt{\frac{1}{3^4}+\frac{1}{5^4}+\frac{1}{7^4}+\ldots} = \frac{1}{Q^2}\sqrt{\sum_{k=1}^{\infty}\frac{1}{(2k+1)^4}} = \frac{1}{Q^2}\sqrt{\frac{\pi^4}{96}-1} \tag{3-7}$$



(a) (b)

Figure 22. Frequency spectrum. (a) Continuous-time. (b) Discrete-time with sampling frequency of $8f_0$.

As shown in Figure 22 (a), in a continuous-time system, there is no boundary in frequency, all harmonics to infinite index should be considered to calculate THD. However, in a discrete-time system, harmonics beyond the half of sampling frequency are aliased from lower frequency and same harmonic behavior is repeated in every sampling frequencies. As shown in Figure 22 (b), if the ratio of sampling frequency f_s

and fundamental frequency f_0 is 8, only the third harmonic is relevant and should be considered for THD.

Figure 23 depicts the behavior of the third-order harmonic distortion (HD3) with respect to the Q-factor. As shown, a Q-factor of 10 results in a HD3 of -39 dB and, for a HD3 of -55 dB, a Q-factor as large as 60 is needed. Thereby, the oscillator harmonic distortion is a function of the Q-factor of the BPF and hence, a high Q-factor is required for a low distortion oscillator.

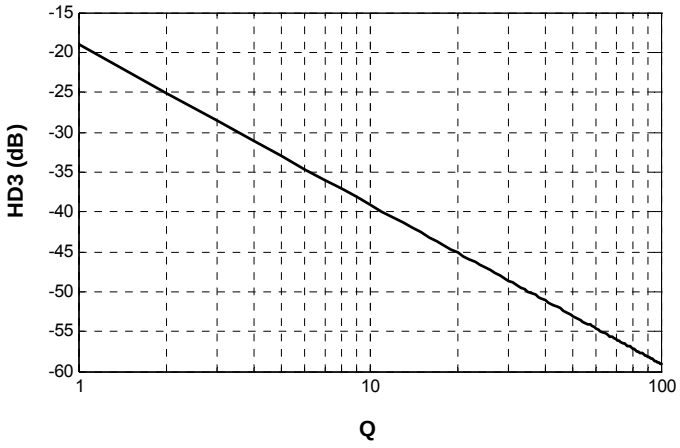


Figure 23. HD3 versus Q-factor value of a second-order SC BPF.

3.2.2. Oscillator with Multi-Level Comparator

In the conventional oscillator of Figure 19, the comparator generates the square wave which has a full family of odd harmonics as well as the fundamental tone as illustrated in Figure 21 (a). Higher than fifth-order harmonics are easily rejected by the

BPF, hence their contribution to linearity performance of the oscillator can be neglected. Thus, the linearity of the oscillator is mainly determined by the third- and fifth-order harmonics since they are close to the fundamental tone and have high magnitudes. This paper proposes an approach where the linearity of the oscillator is improved without requiring a high Q-factor BPF. This is accomplished by non-linear shaping which consists of a harmonic-suppression mechanism in a multi-level comparator. The operation of the multi-level comparator modifies the square wave signal's harmonic contents such that its output completely eliminates the third- and fifth-order harmonics. Therefore, the harmonics in the oscillator's output, V_{out} in Figure 19, are not only dependent on a Q-factor of the BPF but also suppressed by a multi-level comparator.

As shown in the section 3.2.3, by optimally determining the height and width of the waveform signal in a four-level comparator, the third- and fifth-order harmonics can be perfectly cancelled. The derived optimal values of the height and width of the step are $\sqrt{2}$ and *T/8*, respectively, where *T* is the time period of the comparator's output signal. To verify the harmonic-canceling action in a four-level comparator, MATLAB simulations were done and the results are shown in Figure 24. Mathematical expressions of the waveforms in Figure 24 (a) and (b) are derived as (3-16) and (3-17) in section 3.2.3, respectively.

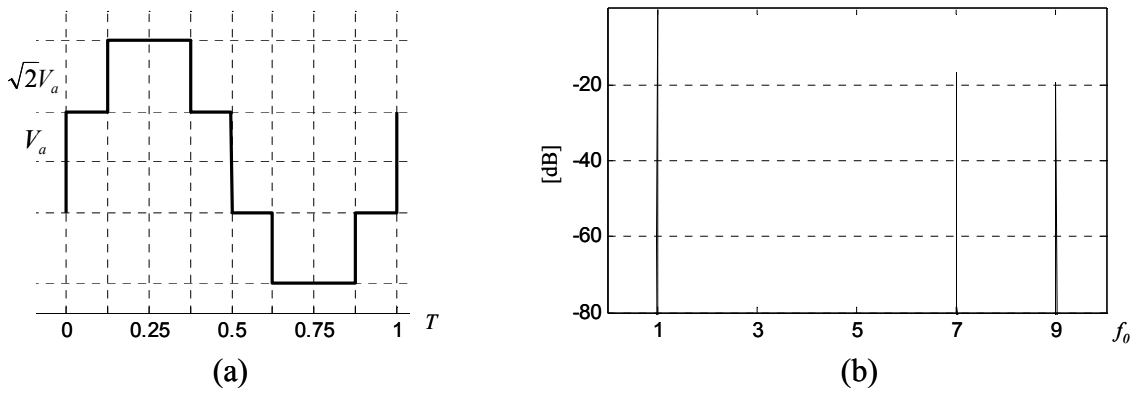


Figure 24. Waveform of four-level comparator yielding low distortion. (a) Time domain. (b) Frequency spectrum.

The conceptual idea for a four-level comparator is shown in Figure 25. The output *f(t)* consists of a square wave, $f_S(t)$, with a fundamental frequency f_0 and two shifted signals versions of $f_S(t)$. For an optimal non-linear shaping, each level of the output signal in Figure 25 should be consistent with the relationship in the amplitudes ($1:\sqrt{2}$) and delays ($\pm T/8$), as derived in the section 3.2.3.

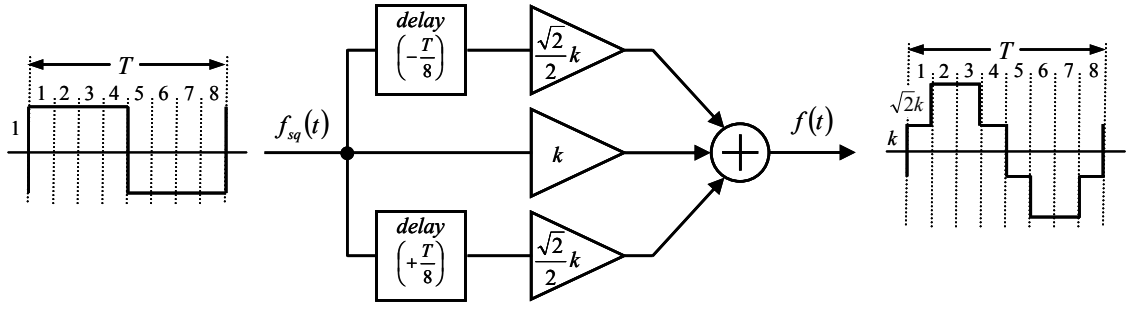


Figure 25. Conceptual diagram of a four-level square wave generator.

In discrete-time circuits, the multi-level comparator is implemented by a finite impulse response (FIR) filter. The FIR filter generates zeros at the optimal locations resulting in low harmonic distortion. It can be shown that with the optimal sampling frequency and FIR coefficients, the frequency spectrum can be shaped advantageously. As stated in the section 3.2.4, the linearity improvement obtained with the four-level comparator can be extended to a (2^{m+1})-level comparator with m > 1. In that case, a time delay t_d equal to $T/(2^{m+2})$ is required to cancel out all harmonic components below $(2^{m+2}-1)$.

3.2.3. Frequency Spectrum Analysis on Four-Level Comparator

The spectrum of a square wave consists of the fundamental frequency and an infinite number of odd harmonics. A square wave $f_{sq}(t)$ with an amplitude of V_a and a period of T and its Fourier transform $F_{sq}(\omega)$ can be expressed as

$$f_{sq}(t) = V_a \frac{4}{\pi} \sum_{k=1,3,5,..}^{\infty} \frac{1}{k} \sin(k\omega_0 t) \tag{3-8}$$

$$\Im\{f_{sq}(t)\} = F_{sq}(\omega) = V_a \frac{4}{\pi} \frac{j}{2} \sum_{k=1,3,5,..}^{\infty} \frac{1}{k} [\delta(\omega + k\omega_0) - \delta(\omega - k\omega_0)] \tag{3-9}$$

where $\omega_0 = 2\pi / T$. Suppose that three different square waves having different amplitudes and time delays are summed together.

$$f(t) = V_a f_{sq}(t) + kV_a f_{sq}(t - t_d) + kV_a f_{sq}(t + t_d), \quad 0 < t_d < T/4 \tag{3-10}$$

where t_d is a time delay. Fourier transform of (3-10) yields

$$F(\omega) = V_a(1 + 2k\cos(t_d\omega))F_{sq}(\omega) = H(\omega)F_{sq}(\omega) \tag{3-11}$$

where $H(\omega)$ is the ratio of $F(\omega)/ F_{sq}(\omega)$. Since it is supposed that $f_{sq}(t)$ is a square wave, $F_{sq}(\omega)$ has frequency components only at $(2n+1)\omega_0$ which denotes the harmonic components for $n \geq 1$, where n is an integer and ω_0 is a fundamental frequency in radians. Evaluating the transfer function $H(\omega)$ at corresponding odd harmonic frequencies, $H((2n+1)\omega_0)$ yields

$$H((2n+1)\omega_0) = V_a\{1 + 2k\cos(t_d(2n+1)\omega_0)\} \tag{3-12}$$

From (3-12), $n = 1$ and $n = 2$ yield $H(3\omega_0)$ and $H(5\omega_0)$.

$$H(3\omega_0) = V_a\{1 + 2k\cos(t_d 3\omega_0)\}, \quad H(5\omega_0) = V_a\{1 + 2k\cos(t_d 5\omega_0)\} \tag{3-13}$$

k and t_d can be selected to the values such that $H(3\omega_0) = H(5\omega_0) = 0$. Solving (3-13) yields $t_d\omega_0 = \pi/4$. Recalling $\omega_0 = 2\pi/T$, the critical values of k and t_d are obtained.

$$t_d = T/8, \quad k = 1/\sqrt{2} \tag{3-14}$$

Note that $k = 1/\sqrt{2}$ is equivalent to $k = \cos(t_d\,\omega_0)$ when $t_d = T/8$. With the condition of (3-14), evaluating (3-12) for $n = 0, 1, 2, 3$ gives

$$H(\omega_0) = H(7\omega_0) = 2V_a, \quad H(3\omega_0) = H(5\omega_0) = 0 \tag{3-15}$$

Using the condition of (3-14), (3-10) and (3-11) can be expressed general mathematical expressions as

$$\begin{aligned} f(t) &= V_a\left[f_{sq}(t) + \left(1/\sqrt{2}\right) f_{sq}(t - T/8) + \left(1/\sqrt{2}\right) f_{sq}(t + T/8)\right] \\ &= V_a \frac{4}{\pi} \sum_{k=1,3,5,..}^{\infty} \frac{1}{k} \begin{bmatrix} \sin(k\omega_0 t) + \left(1/\sqrt{2}\right)\sin\left(k\omega_0 (t - T/8)\right) \\ + \left(1/\sqrt{2}\right)\sin\left(k\omega_0 (t + T/8)\right) \end{bmatrix} \\ &= V_a \frac{4}{\pi} \sum_{k=1,3,5,..}^{\infty} \left[1 + \sqrt{2}\cos(k\pi/4)\right] \frac{1}{k} \sin(k\omega_0 t) \end{aligned} \tag{3-16}$$

$$F(\omega) = V_a \frac{4}{\pi} \frac{j}{2} \sum_{k=1,3,5,..}^{\infty} \left[1 + \sqrt{2}\cos(k\pi/4)\right] \frac{1}{k} \left[\delta(\omega + k\omega_0) - \delta(\omega - k\omega_0)\right] \tag{3-17}$$

Equations (3-16) and (3-17) show that with a particular condition of (3-14), certain harmonics can be rejected while maintaining other harmonics. For instance, if the second and third coefficients of the first equation in (3-10) are negative, then resulting harmonic cancellation would be different.

$$f(t) = V_a\left[f_{sq}(t) - \left(1/\sqrt{2}\right)f_{sq}(t - T/8) - \left(1/\sqrt{2}\right)f_{sq}(t + T/8)\right] \tag{3-18}$$

$$F(\omega) = V_a\left(1 - \sqrt{2}\cos\left(\frac{\pi}{4}\frac{\omega}{\omega_0}\right)\right)F_{sq}(\omega) \tag{3-19}$$

When $\omega = \omega_0$ and $\omega = 3\omega_0$, (3-19) becomes

$$\begin{aligned} &F(\omega_0) = 0 \\ &F(3\omega_0) = 2V_a F_{sq}(3\omega_0) = j\frac{4V_a}{\pi}\left[\delta(\omega + 3\omega_0) - \delta(\omega - 3\omega_0)\right] \end{aligned} \tag{3-20}$$

Same analysis can be performed using z-transform in discrete-time systems. If the sampling time T_S is normalized to t_d, (3-10) is represented as

$$f(n) = V_a f_{sq}(nT_S) + kV_a f_{sq}((n-1)T_S) + kV_a f_{sq}((n+1)T_S) \tag{3-21}$$

Z-transform of (3-21) yields

$$F(z) = kV_a z\left(1 + \frac{1}{k}z^{-1} + z^{-2}\right)F_{sq}(z) = H(z)F_{sq}(z) \tag{3-22}$$

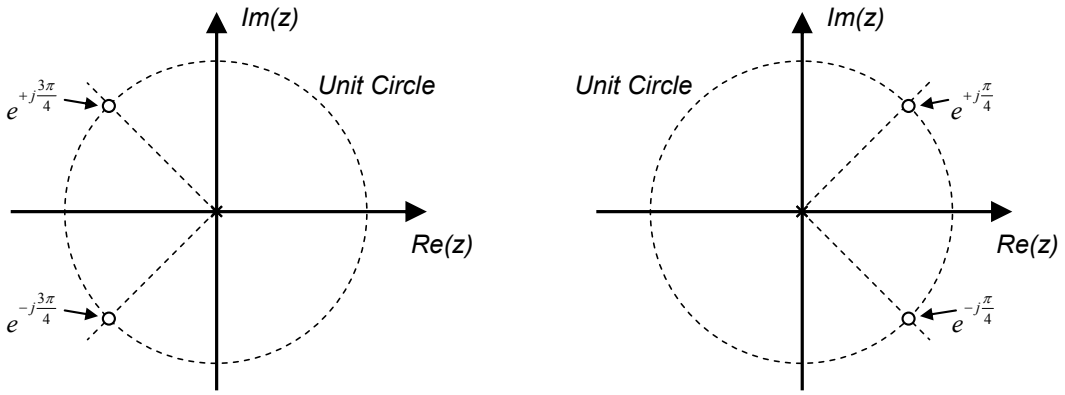
Defining $H(z)$ as $F(z)$ / $F_{sq}(z)$, $H(z)$ in (3-22) becomes

$$H(z) = \frac{1}{\sqrt{2}} V_a z\left(1 + \sqrt{2} z^{-1} + z^{-2}\right) \tag{3-23}$$

H(z) of the case that a fundamental tone is rejected as stated in (3-18), can be expressed as

$$H(z) = \frac{1}{\sqrt{2}} V_a z\left(1 - \sqrt{2} z^{-1} + z^{-2}\right) \tag{3-24}$$

Pole-zero map of (3-23) and (3-24) are plotted in Figure 26 (a) and (b), respectively.



(a) (b)

Figure 26. Pole-zero location. (a) $H(z)$ of (3-23). (b) $H(z)$ of (3-24).

(3-23) has zeros at $z = e^{\pm j3\pi/4}$ as depicted in Figure 26 (a). Since the sampling frequency is chosen as $8\omega_0$ that corresponds to 2π from (3-23), zeros frequencies correspond to $3\omega_0$

and $5\omega_0$ in the range of $0 \le \omega \le 2\pi$. It can be noted that (3-23) has the same property that is stated in (3-15).

3.2.4. Non-Ideal Effects and Generalization of Multi-Level Comparator

Non-ideal effects on multi-level comparator can be considered as the deviation of k and t_d from their optimized values. Hence, the ideal values of k and t_d can be replaced with $(\Delta_m + 1)k$ and $(\Delta_p + 1)\, t_d$, respectively, where Δ_m and Δ_p are the magnitude and phase error factors. Substituting these values in (3-10) and using (3-15), (3-16) becomes

$$H\left((2n+1)\omega_0\right) = V_a\left\{1 + (1+\Delta_m)\sqrt{2}\cos\left((2n+1)(1+\Delta_p)\frac{\pi}{4}\right)\right\} \tag{3-25}$$

From (3-11) and (3-25), HD3 is not cancelled and becomes

$$HD3 = \frac{|F(3\omega_0)|}{|F(\omega_0)|} = \frac{1}{3}\frac{|H(3\omega_0)|}{|H(\omega_0)|} = \frac{1}{3}\frac{\left|1 + \sqrt{2}(1+\Delta_m)\cos\left(\frac{3\pi}{4}(1+\Delta_p)\right)\right|}{\left|1 + \sqrt{2}(1+\Delta_m)\cos\left(\frac{\pi}{4}(1+\Delta_p)\right)\right|} \tag{3-26}$$

Figure 27 shows the plot of HD3 versus Δ_m and Δ_p. Note that even for a 10% of Δ_m and 5% of Δ_p, the HD3 is below -19 dB than that of the conventional square wave. Sensitivity analysis can be done for (3-26) to find out the optimal condition. However, as

shown in Figure 27 (c), (3-26) does not have the local minima for Δ_m or Δ_p. HD3 is monotonically decreased as Δ_m or Δ_p is decreased.

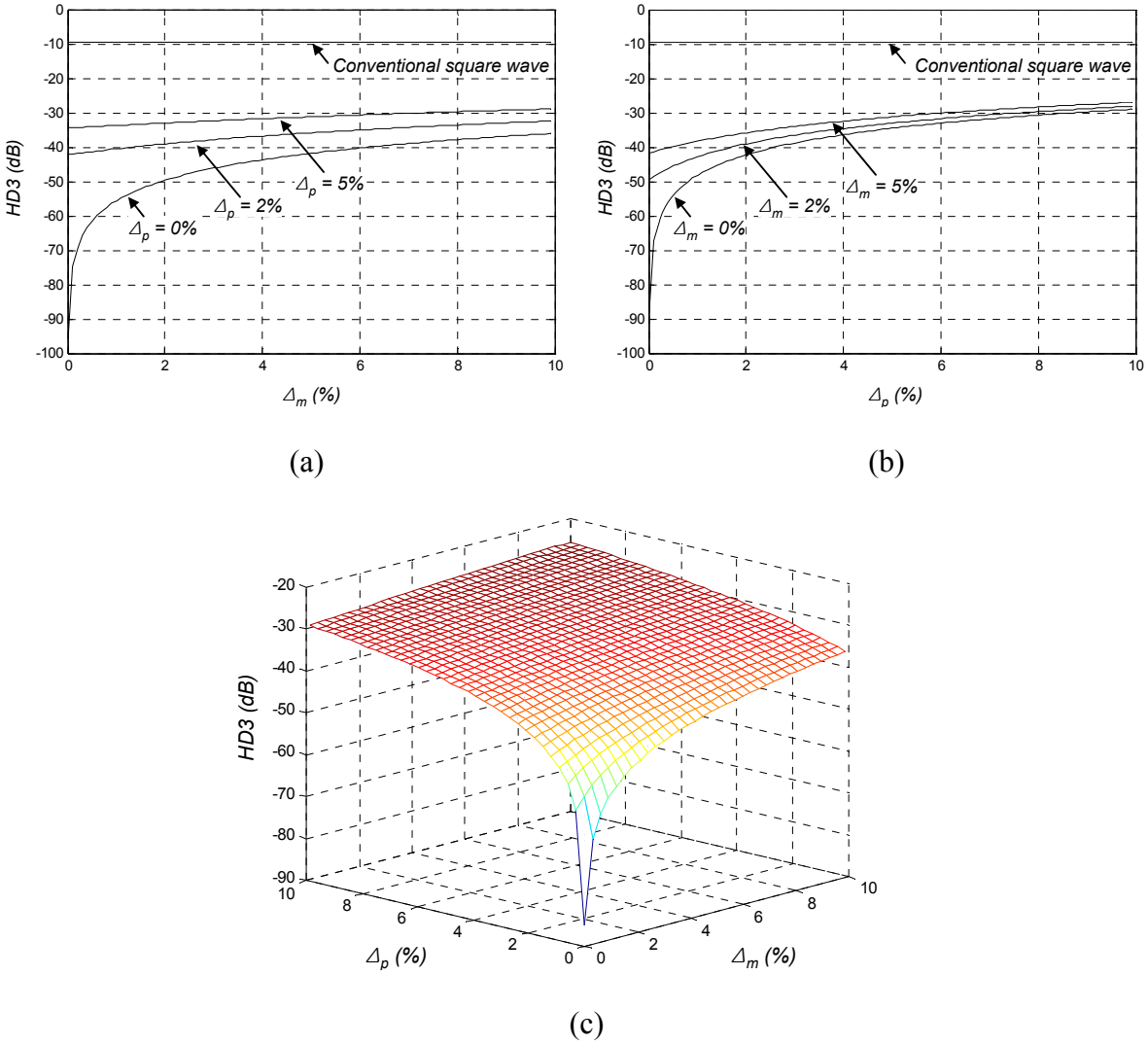


Figure 27. HD3 versus non-ideal magnitude factor Δ_m and phase factor Δ_p. (a) HD3 vs. Δ_m. (b) HD3 vs. Δ_p. (c) 3-d plot.

The concept of a multi-level square wave can be extended to any number (2^{m+1}) of levels. Then, (3-10) becomes

$$f(t) = V_a f_{sq}(t) + \sum_{i=1}^{2^m-1} \left\{ k_i V_a f_{sq}(t - t_{di}) - k_i V_a f_{sq}(t + t_{di}) \right\}, \quad 0 < t_{di} < \frac{T}{4} \tag{3-27}$$

where m is a positive integer. Total number of levels is always 2^{m+1} and the Fourier transform of (3-27) yields

$$F(\omega) = V_a \left(1 + 2 \sum_{i=1}^{2^m-1} k_i \cos(t_{di}\omega) \right) F_{sq}(\omega) \tag{3-28}$$

Now, t_{di} and k_i can be carefully chosen in similar way to (3-14) as

$$t_{di} = \frac{T}{2^{m+2}} i, \quad k_i = \cos\left(\frac{2\pi}{2^{m+2}} i \right) \tag{3-29}$$

With the optimal values of (3-29) and the fact that $F_0(\omega)$ has only odd harmonics, (3-28) can be written

$$\begin{aligned} & F\left((2n+1)\omega_0 \right) \\ & = V_a \left\{ 1 + 2 \sum_{i=1}^{2^m-1} \left[\cos\left(\frac{2\pi}{2^{m+2}} i \right) \cdot \cos\left((2n+1) \frac{2\pi}{2^{m+2}} i \right) \right] \right\} F_{sq}\left((2n+1)\omega_0 \right) \end{aligned} \tag{3-30}$$

(3-30) is a generalized form of a frequency spectrum of a multi-level square wave and it gives two important properties that the number of levels is 2^{m+1} and first non-zero harmonic appears at $(2^{m+2}-1)\omega_0$. Figure 28 depicts frequency spectrum at each case of m. As m is increased, the number of levels is increased and the first harmonic appears at higher frequency.

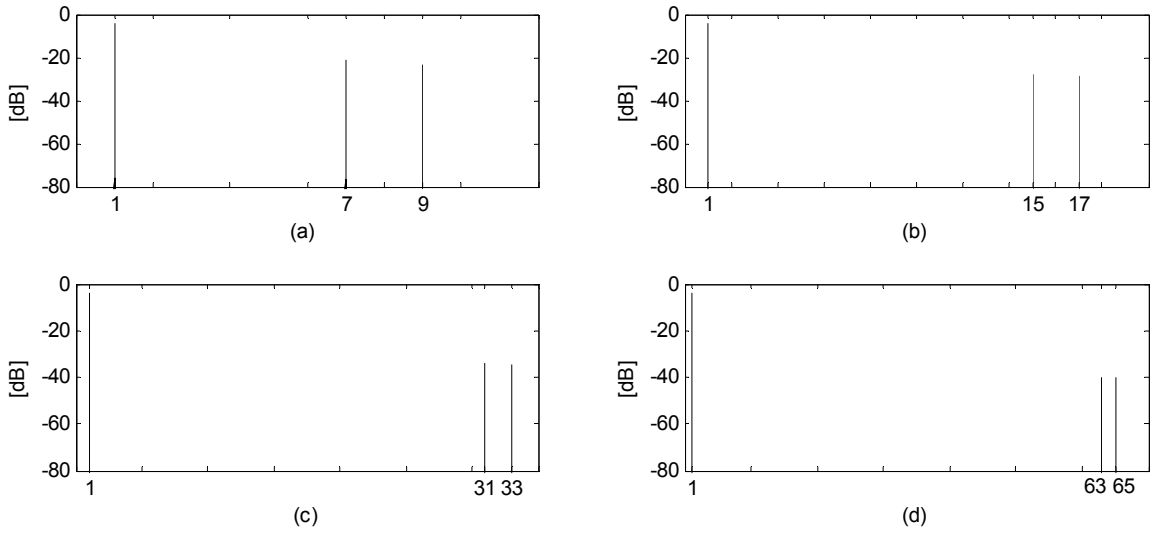


Figure 28. Frequency spectrum of (3-30): (a) m=1. (b) m=2. (c) m=3. (d) m=4.

Using the concept of FIR filter derived at (3-23) and (3-24) and depicted in Figure 26, it can be used to set any harmonics as dominant. (3-24) is the one example to set the third harmonic rejecting the fundamental tone. In this case, minimum required sampling rate f_{sample} / f_0 is 8 since $4f_0$ (= f_{sample} / 2) is next harmonic frequency to $3f_0$. If the fifth harmonic is desired, minimum sampling rate f_{sample} / f_0 is 12. Then, multiple

numbers of zeros can be placed on every odd harmonic frequency except for a desired harmonic. In case that fifth harmonic is desired, a design procedure can be as follows.

1) Half of sampling frequency must be higher than fifth harmonic. This also determines unit delay in time as a sampling time.

$f_s / 2 = 6f0 \Rightarrow f_s = 12f0$

$t_d = T_s = T / 12$

2) Place zero on every odd harmonic except for fifth harmonic frequency.

$z_{1,2} = e^{\pm j\pi/6}$, $z_{3,4} = e^{\pm j3\pi/6}$

3) Place with half number of zeros at the origin for balanced delay.

$p_{1,2} = 0$

4) Build H(z).

$$H(z) = \frac{1}{z^2}\left(z - e^{+j\pi/6}\right)\left(z - e^{-j\pi/6}\right)\left(z - e^{+j3\pi/6}\right)\left(z - e^{-j3\pi/6}\right)$$

$$= \frac{1}{z^2}\left(z^2 - \sqrt{3}z + 1\right)\left(z^2 + 1\right)$$

$$= z^2 - \sqrt{3}z + 2 - \sqrt{3}z^{-1} + z^{-2}$$

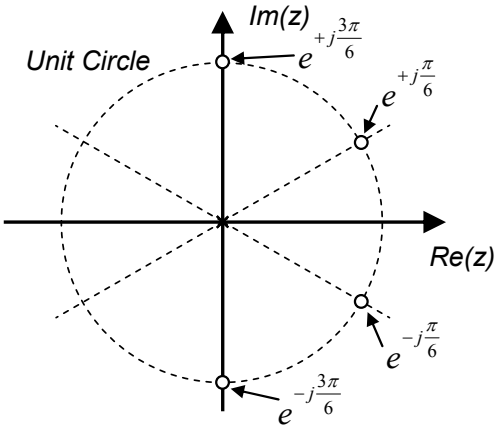
5) Build the system in time domain.

$$f(t) = f_{sq}(t - 2T/12) - \sqrt{3}f_{sq}(t - T/12) + 2f_{sq}(t)$$

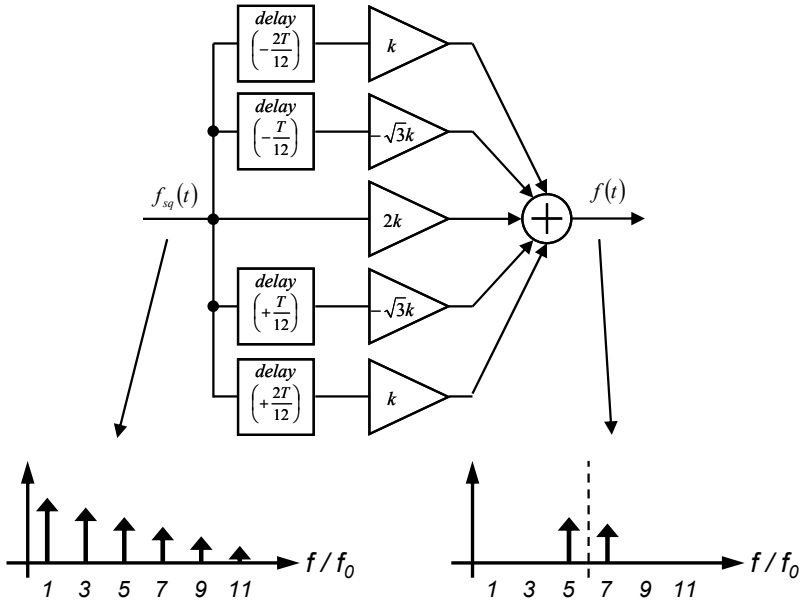
$$- \sqrt{3}f_{sq}(t + T/12) + f_{sq}(t + 2T/12)$$

Figure 29 (a) shows a pole-zero map that is determined at step 2) and 3). Note that there are two poles at the origin to equalize delays in time, however they have no contribution

on any magnitude or phase transfer function. Figure 29 (b) depicts the system diagram explained at step 5).



(a)



(b)

Figure 29. FIR passing only fifth harmonic. (a) Pole-zero map. (b) System diagram.

3.3. Circuit Implementation of Four-Level Comparator

In order to provide the delayed square-wave signals with a proper timing as stated in the Section 3.2, Figure 30 depicts a practical implementation of a four-level comparator, which is full compatible with SC circuits.

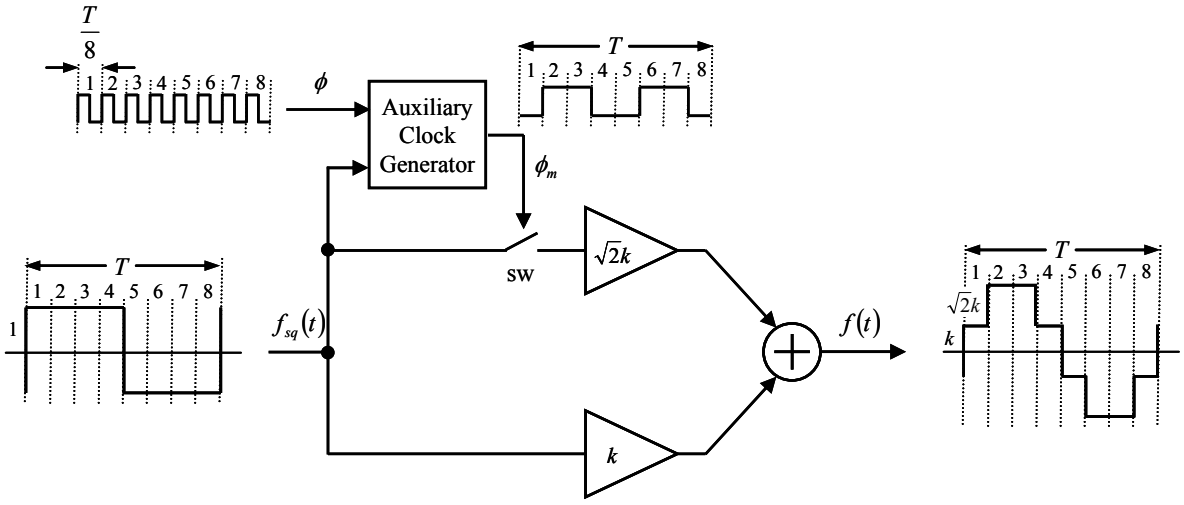
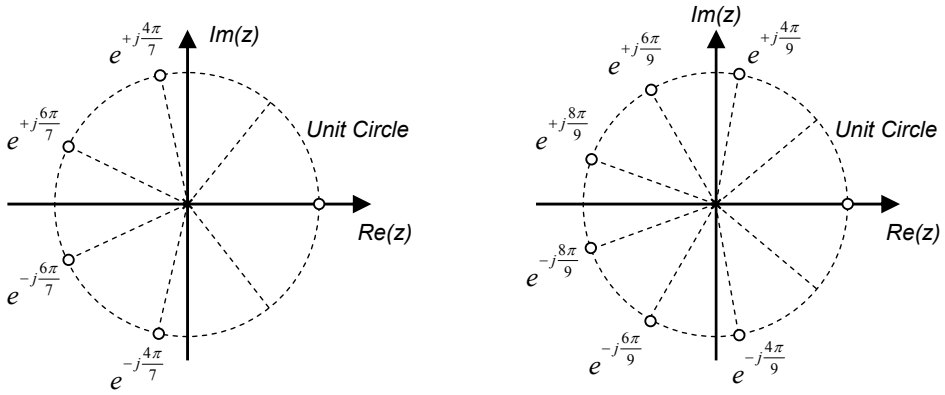


Figure 30. Diagram on implementation of a four-level square wave generator.

The sampling rate (the ratio of clock and fundamental frequency f_{clock} / f_0) sets the delay time resolution, and higher rate extends the Nyquist rate having more relevant number of harmonics. However, higher clock frequency introduces practical difficulties in designing switches and amplifier if needed. As shown in Figure 30, by using the master clock signal (φ) and the fundamental square-wave signal $f_{sq}(t)$, an auxiliary clock signal generator provides a control signal (φ_m) in order to operate the switch denoted as sw. When the switch sw is turned on, i.e., φ_m is in its high state, the additional path generates

the positive part ($+k\sqrt{2}|f_S(t)|$) at the time intervals of '2' and '3' (equivalent to *2T/8* and *3T/8*), and the negative part ($-k\sqrt{2}|f_S(t)|$) at the time intervals of '6' and '7'. After adding those signals at t = *3T/8*, *f(t)* becomes $k\left(1+\sqrt{2}\right)f_S(t)$, as shown in Figure 30. When the switch sw is turned off, i.e., φ_m is in its low state, *f(t)* is $kf_S(t)$. Note that the additional path with the switch sw generates the signal equivalent to $\sqrt{2}k\left|f_S(t-T/8)+f_S(t+T/8)\right|$.

The circuit shown in Figure 30 works well in case that the master clock period is T / n where n is multiple of 8, i.e. n = 8, 16, 24, …. If n is any integer other than multiples of 8, then the required number of conjugate zeros is increased resulting in complicated implementation.



(a) (b)

Figure 31. Pole-zero map. (a) $T_s = T / 7$. (b) $T_s = T / 9$.

As shown Figure 25, if n = 8, then only one pair of conjugate zero is needed at $e^{j\pm 3\pi/8}$ and the number of paths is 3. If n = 7, for instance, one real zero at 1 and two pairs of conjugate zeros are needed at $e^{j\pm 4\pi/7}$ and $e^{j\pm 6\pi/7}$, as plotted in Figure 31 (a), and 6 delayed

gain paths are required. If n = 9, required zeros are at 1, $e^{j\pm 4\pi/9}$, $e^{j\pm 6\pi/9}$ and $e^{j\pm 8\pi/9}$, as plotted in Figure 31 (b), and 8 delayed gain paths are needed.

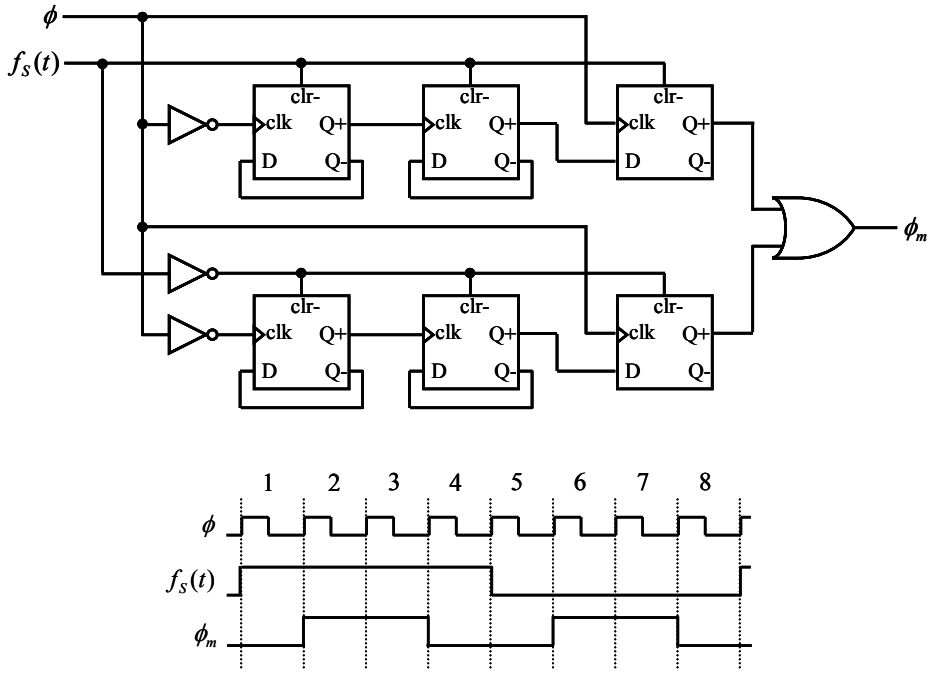


Figure 32. Auxiliary clock generator.

Figure 32 shows a low-cost implementation of the auxiliary clock signal generator required by the circuit in Figure 30. The fundamental square wave $f_S(t)$, i.e., the output of comparator, provides negative-clear (CLR-) signal to D-type flip-flop (DFF). When CLR- is high, DFF starts the frequency dividing operation. When $f_S(t)$ is high, the first two DFF's of the upper path divide the frequency of φ by 4. The last DFF delays the signal by one period of φ. The lower path is active when $f_S(t)$ is low and φ is processed in the same way. By combining the two paths with an OR gate, φ_m is

generated. By using CLR- of the DFF, φ_m can be synchronized with $f_S(t)$ and becomes high at the exact position (at the time intervals of '2', '3', '6' and '7'). Note that Figure 32 works only for the case that a clock frequency is multiples of 8 times higher than the fundamental frequency.

3.4. Switched-Capacitor BPF-Based Oscillator Implementation

The maximum clock frequency should be determined considering the requirement of the multi-level square wave generator. For the optimal HD3 cancellation, a clock frequency needs the multiple of 8 times of the oscillation frequency (10 MHz in our case). In this work, a clock frequency of 80 MHz was chosen since the speed limitation of switches and operational-amplifiers (Op-Amps) emerges with higher over sampling [31]. An SC implementation of the second-order BPF in Figure 19 is shown in Figure 33 [31]. V_{comp}^{+} and V_{comp}^{-} are the comparator outputs in Figure 19 and they determined the amplitude V_{out}^{+} and V_{out}^{-} with the BPF gain. The BPF includes a two-integrator loop and the BPF realization is obtained by feeding the input signal, coming from the comparator, into the damped integrator. The BPF in Figure 33 is a low-Q structure and C_3, in the damped integrator, mainly determines the Q-factor of BPF. Since this work has a design target to have a modest Q-factor value of 10, partial positive feedback [32] through C_5 is used for Q-boosting to avoid the high capacitor spread.

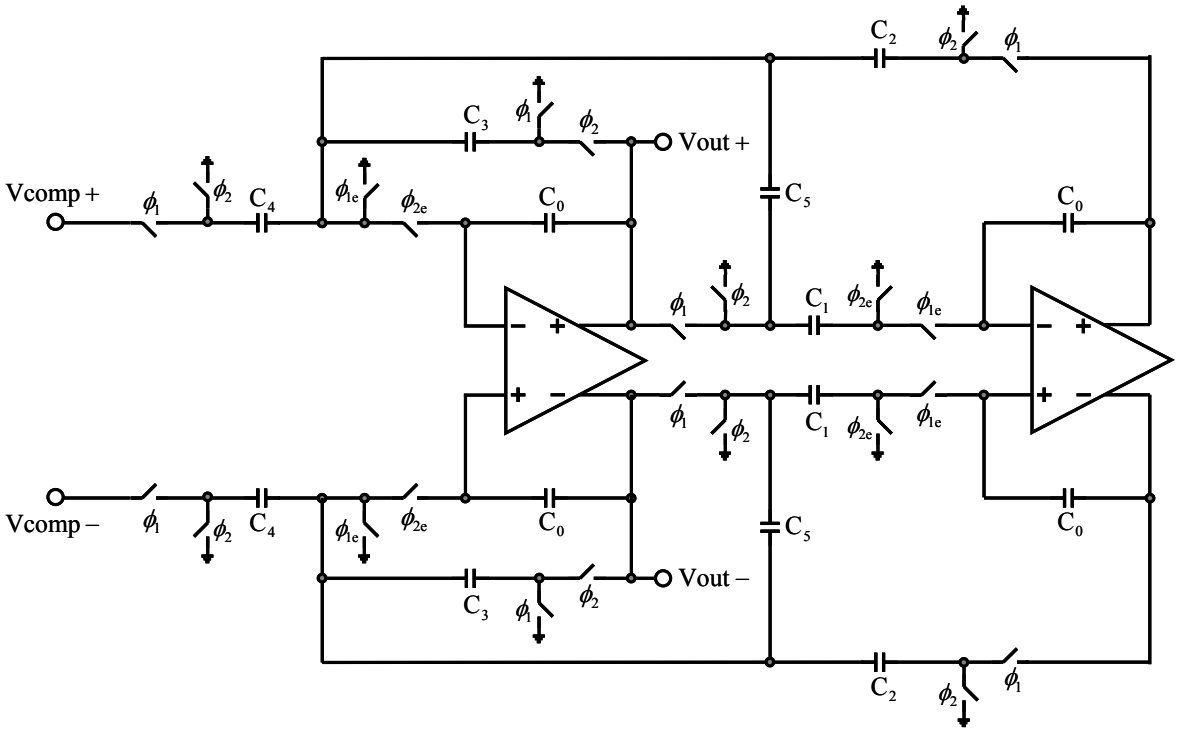


Figure 33. Conventional SC BPF implementation in Figure 19.

It uses two non-overlapping clock phases denoted as ϕ_1 and ϕ_2, and the early clock (ϕ_{1e} and ϕ_{2e}) are used for the switches that are close to amplifier input to reduce charge injection [33]. Also, for maximum cancellation of even harmonics, fully differential structure is adopted. The transfer function of the BPF in Figure 33 has two complex poles and one zero at z = 1, and can be expressed as,

$$H(z) = \frac{K_4}{1+K_3} \frac{z^{-1}\left(1-z^{-1}\right)}{1+\dfrac{K_1K_2-K_3-K_5-2}{1+K_3}z^{-1}+\dfrac{1+K_5}{1+K_3}z^{-2}} \tag{3-31}$$

where $K_1 = C_1/C_0$, $K_2 = C_2/C_0$, $K_3 = C_3/C_0$, $K_4 = C_4/C_0$ and $K_5 = C_5/C_0$.

Note that the number of zero and location can be different depending on the mapping method from s-domain to z-domain. Mapping method is used to translate the information in s-domain to z-domain and can be categorized as the exact mapping and approximated mapping. The exact mapping transforms s-domain to z-domain by using the equation as

$$z = e^{sT_s} \tag{3-32}$$

From (3-32), it can be known that a real number in s-domain defines the radius in z-domain, hence a negative real number (LHP) in s-domain can be placed inside of the unit circle in z-domain. An imaginary number in s-domain that is the frequency information is translated to the angle in z-domain. Although the exact mapping method accurately transforms any poles and zeros in s-domain to z-domain, it is not the linear transform due to the nature of exponential. In the situations where the circuit operates in very low frequency compared to the sampling frequency, the exact mapping can be approximated by using a linear equation. In the approximation, there are bilinear, backward and forward mapping. Each method transform left half plane (LHP) in s-domain to z-domain in different ways. Bilinear mapping maps to the inside of the unit circle, backward mapping maps to the inside of the circle centered at z = 1/2 with a radius of 1/2. In forward mapping, LHP in s-domain is mapped to the left side of z = 1. Mapping equation of each method can be expressed as

$$\text{Bilinear:}\quad s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{3-33}$$

$$\text{Backward:}\quad s = \frac{1}{T_s}\frac{z-1}{z} \tag{3-34}$$

$$\text{Forward:}\quad s = \frac{1}{T_s}(z-1) \tag{3-35}$$

where T_s is a sampling period. Assuming a second-order BPF transfer function in s-domain is

$$H(s) = \frac{cs}{s^2 + as + b} \tag{3-36}$$

where a, b and c are arbitrary coefficients. Applying (3-33), (3-34) and (3-35) to (3-36) yields different zeros such as

$$\text{Bilinear:}\quad z_{z1} = +1,\ z_{z2} = -1 \tag{3-37}$$

$$\text{Backward:}\quad z_{z1} = +1,\ z_{z2} = 0 \tag{3-38}$$

$$\text{Forward:}\quad z_{z1} = +1 \tag{3-39}$$

Figure 34 shows mapping equations, mapped s-domain LHP to z-domain and pole-zero map of second-order BPF using each mapping equations.

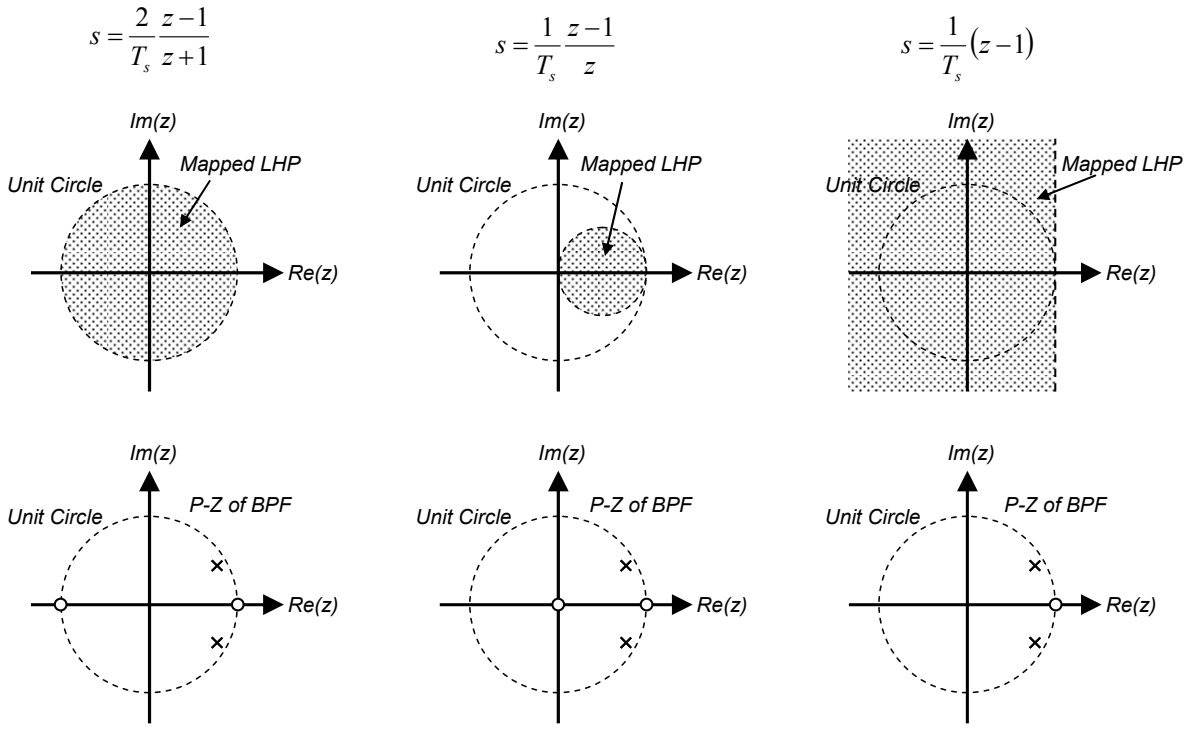


Figure 34. Approximated mapping equation, mapped LHP and pole-zero map of second-order BPF. (a) Bilinear. (b) Backward. (c) Forward.

Among different mapping methods, bilinear mapping provides a reasonable accuracy over all sampling rate. In backward mapping, stable area is more conservative than bilinear since LHP is mapped into the circle inside of the unit circle. In forward mapping, some of stable conditions in s-domain violate the stability in z-domain at the cost of less number of zero.

In the close loop (oscillator) of the open loop equation (3-31), as shown in Figure 31, a transfer function and its characteristic equation D(z) can be expressed as

$$H_{closed}(z) = \frac{H(z)}{1-\beta H(z)}$$

$$= \frac{\frac{K_4}{1+K_3} z^{-1}\left(1-z^{-1}\right)}{1+\frac{K_1K_2-K_3-K_5-2}{1+K_3} z^{-1}+\frac{1+K_5}{1+K_3} z^{-2}-\frac{\beta K_4}{1+K_3}\left(z^{-1}-z^{-2}\right)} \tag{3-40}$$

$$D(z) = 1+\frac{K_1K_2-K_3-K_5-2-\beta K_4}{1+K_3} z^{-1}+\frac{1+K_5+\beta K_4}{1+K_3} z^{-2} \tag{3-41}$$

where β is the gain of the comparator which, for simplicity in analysis, is assumed to be a linear amplifier. The characteristic equation (3-41) can be rewritten as [34],

$$D(z) = 1-2r\cos\theta z^{-1}+r^2 z^{-2} \tag{3-42}$$

where $2r\cos\theta = -\left(K_1K_2-K_3-K_5-2-\beta K_4\right)/\left(1+K_3\right)$ and $r^2 = \left(1+K_5+\beta K_4\right)/\left(1+K_3\right)$.

From (3-42), the oscillation condition $r \geq 1$, yields $\beta K_4 \geq K_3 - K_5$ and this is always true because the comparator has a very high gain, β. With such a high gain β, the circuit becomes initially very unstable and when the poles lie on the unit circle, V_{out} reaches a steady state with constant amplitude in a very short time, regardless of the initial conditions. However, an initial start-up of an oscillation can be suffered from any non-ideal effect under certain conditions because the main feedback loop is a hard-limiting nonlinear positive feedback [24]. This problem is solved with a partial non-limiting

positive feedback via C_5. Providing a sufficient positive feedback through C_5 causes oscillation to start.

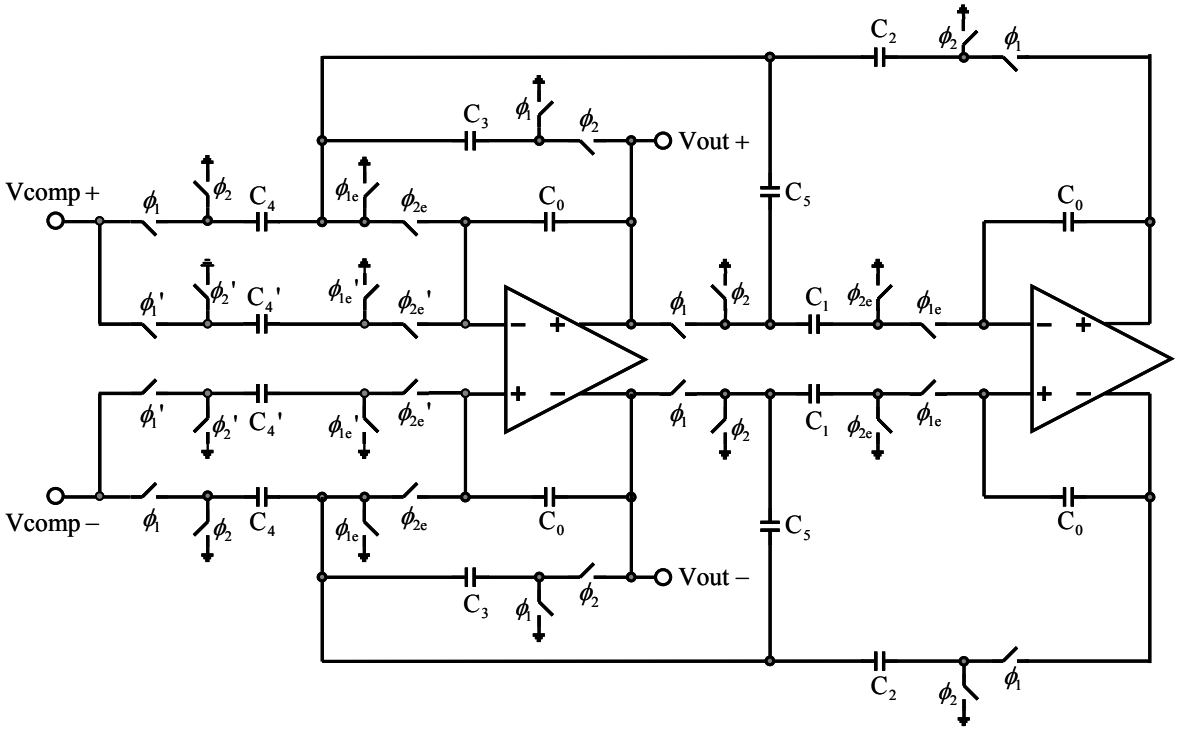


Figure 35. Proposed SC BPF implementation with an imbedded four-level square wave generator.

Table 1. Capacitor values for Figure 33 and Figure 35.

Capacitor	C_0	C_1	C_2	C_3	C_4	C_4'	C_5
Value	2 pF	2.2 pF	2.2 pF	1.2 pF	0.3 pF	0.4 pF	0.5 pF

Figure 35 shows the proposed BPF including the four-level square wave generator. Capacitors used in both Figure 33 and Figure 35 are shown in Table 1. These capacitors can be usually determined by mapping transform from s-domain to z-domain. The design procedure of SC filter can be summarized as:

1) Design analog filter in s-domain and determine poles and zeros in s-domain.
2) Transform poles and zeros in s-domain to z-domain using appropriate mapping method.
3) Choose a specific filter structure which determines a transfer function.
4) Compare coefficients in step 2) and 3), and match them by determining corresponding capacitors.
5) Approximate capacitors to integer multiples of the unit capacitor to enhance the matching property in layout.

If a second-order BPF is assumed, then the transfer function in s-domain is

$$H(s) = \frac{k_s s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{3-43}$$

where k_s is a gain factor, Q is a quality-factor and ω_0 is a center frequency in rad/s. In this work, $\omega_0 = 2\pi \times 10$ MHz and Q = 10. Then zero and poles of (3-43) are

$$\omega_z = 0$$
$$\omega_{p1,p2} = 10^7 \times \left(-0.3142 \pm j6.2753\right) \tag{3-44}$$

Since sampling rate in this work is designed to be 8, the exact mapping method is used for better accuracy. Using the mapping equation of (3-32), a center frequency and (3-44) can be transformed in z-domain as

$$z_0 = e^{j\frac{\omega_0}{8\times10^7}} = 0.7071 + j0.7071$$
$$z_z = 1 \tag{3-45}$$
$$z_{p1,p2} = e^{\frac{\omega_{p1,p2}}{8\times10^7}} = 0.6805 \pm j0.6792$$

Using (3-45), a transfer function in z-domain is

$$H(z) = k_z \frac{z^{-1}\left(1 - z^{-1}\right)}{1 - 1.361 \cdot z^{-1} + 0.9245 \cdot z^{-2}} \tag{3-46}$$

where k_z is a gain factor. A magnitude of H(z) at z_0 is designed to be 1 and k_z can be determined as

$$k_z = \left| \frac{1 - 1.361 \cdot z_0^{-1} + 0.9245 \cdot z_0^{-2}}{z_0^{-1}\left(1 - z_0^{-1}\right)} \right| = 0.07 \tag{3-47}$$

Substituting (3-47) to (3-46) yields a complete transfer function in z-domain as

$$H(z) = 0.07 \frac{z^{-1}\left(1 - z^{-1}\right)}{1 - 1.361 \cdot z^{-1} + 0.9245 \cdot z^{-2}} \tag{3-48}$$

By comparing (3-31) and (3-48) and assuming $K_1 = K_2$ in (3-31) for design convenience, we can determine all variables. The unit capacitor is designed as 200 fF considering process variations. The integrator capacitor C_0 and smallest capacitor C_4 are determined as 2 pF and 300 fF, respectively. Note that the resolution of capacitor is 100 fF that can be implemented by connecting two unit capacitors in series. By rounding off all capacitors to multiples of 100 fF, all capacitors can be determined. Since it is critical to have minimum mismatch to the capacitor ratio, all capacitors should be drawn by the unit capacitors and can be placed within the capacitor block. A layout diagram of a capacitor block is shown in Figure 36.

This, together with a conventional two level comparator, forms the proposed low distortion oscillator. Note that only two additional SC branches, in comparison to Figure 33, are added to implement the multi-level comparator.

A capacitor C_4' injects additional charge at the time intervals '2', '3', '6' and '7' in Figure 30. The optimal ratio of C_4' / C_4 is designed as $\sqrt{2}$, and with C_4 = 0.3 pF as shown Table 1, C_4' should be 0.4243 pF. It is rounded to 0.4 pF in Table 1, and this gives a finite error to HD3 rejection as will be seen in measurement results.

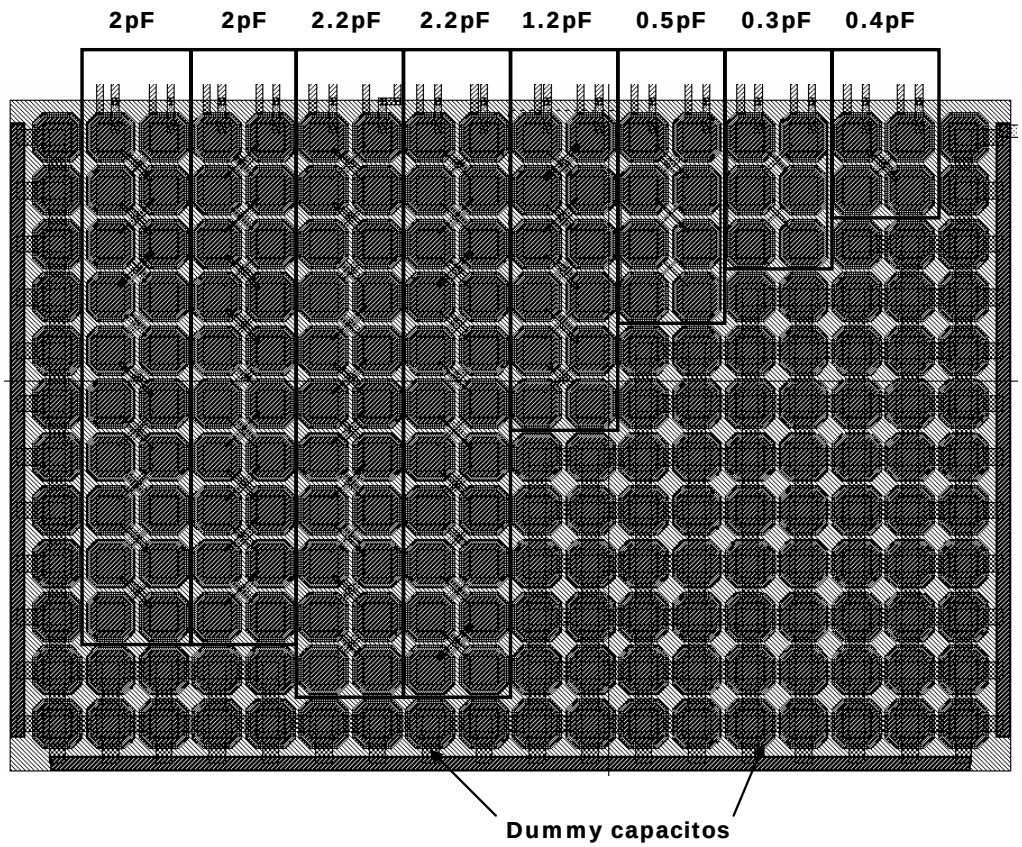


Figure 36. Layout diagram of capacitor block.

Figure 37 shows the clocks used in the proposed oscillator. Typical two-phase, non-overlapping clock scheme is used for all clocks. Also, each clock, ϕ_1, ϕ_2, ϕ_1' and ϕ_2' are paired with the early clock, ϕ_{1e}, ϕ_{2e}, ϕ_{1e}' and ϕ_{2e}' to minimize the influence of the clock feedthrough [34]. A signal dependent input offset due to the clock feedthrough can be removed by applying the early clocks for the switches connected to the amplifier input. When the switches at the amplifier input are opened, clock feedthrough occurs but since the switch terminals are at ground potential, this feedthrough is independent of signal level. When the other switch is open afterwards, no clock feedthrough can occur

because the switch at the amplifier input is already opened and there is no current path [35]. As shown in Figure 37, clocks (ϕ_1', ϕ_2', ϕ_{1e}' and ϕ_{2e}') used in these branches become active when ϕ_m is high and have the same clock phase with ϕ_1, ϕ_2, ϕ_{1e} and ϕ_{2e}, respectively. Due to the four-level square wave generator, the effective input signal of the BPF in Figure 35 does not have the third- and fifth-order harmonics, thus the linearity is significantly improved with respect to the conventional SC BPF-based oscillator. Observe that the additional cost in area and power of the multi-level comparator is minimum.

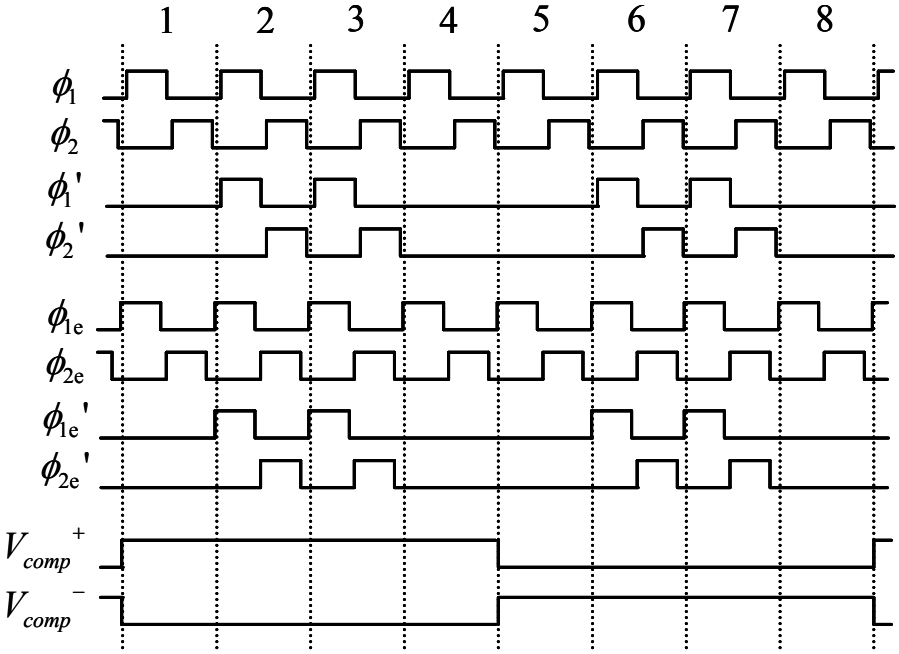


Figure 37. Clocks used in the proposed oscillator.

Ideally, a four-level comparator cancels the third- and fifth-order harmonics. However, under real circumstances of the circuit operation, SC BPF-based oscillator performances suffer from various non-ideal effects such as non-exact ratio between levels ($\sqrt{2}$), non-accurate delay ($t_d = T/8$) of additional square waves, finite rise-fall time at level transition and non-50% duty ratio of each square waves. A significant non-ideal effect is due to the ratio mismatch (Δ_m) between the magnitudes of levels. This is determined by the ratio of the capacitors and requires a non-integer value of $\sqrt{2}$. The error in delay (Δ_p) can be considered not less sensitive than the magnitude error because a delay is determined through the master clock. However, it is affected by the jitter because a delay is also associated with a comparator. Any phase error due to non-accurate result from a comparator causes the error on delay. It is shown in appendix B that, even for 10% of Δ_m and 5% of Δ_p, the improvement of HD3 is nearly 19 dB with respect to the conventional oscillator.

A finite gain bandwidth (GB) affects the performance of SC BPF [36]. A general rule of thumb on requirement of the GB of amplifier is [31]

$$a \cdot GB \cdot T_s < 5 \tag{3-49}$$

where a is the capacitor ratio between the sum of all the feedback capacitors (C_f) divided by the sum of all capacitors connected to the input terminal of Op-Amp (C_i) and can be expressed as

$$a = \frac{\sum C_f}{\sum C_i} \tag{3-50}$$

Since there are two Op-Amps in Figure 35, *a* should be evaluated to each amplifier.

$$a_1 = \frac{C_0 + C_3 + C_5}{C_0 + C_2 + C_3 + C_4 + C_4' + C_5} = 0.56$$
$$a_2 = \frac{C_0}{C_0 + C_1} = 0.47 \tag{3-51}$$

a_1 is for a lossy integrator and a_2 is for a lossless integrator in Figure 35.

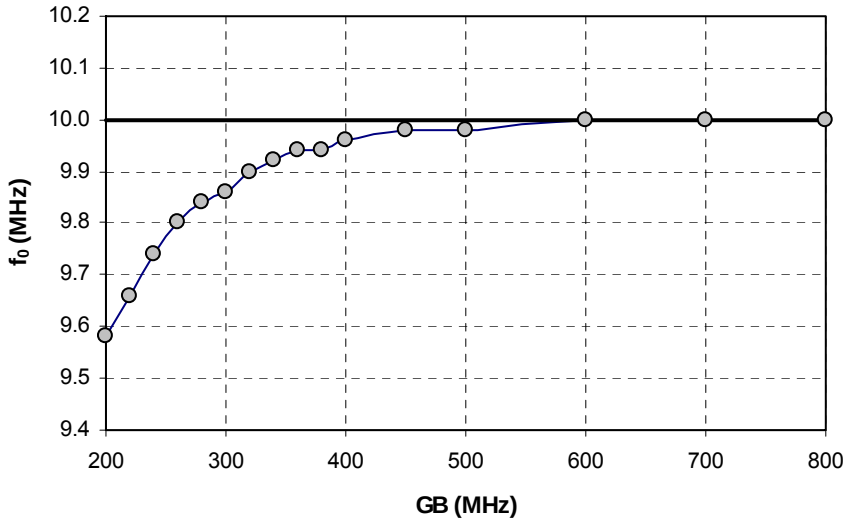


Figure 38. Simulated f_0 versus GB.

Since two identical amplifiers are used for a design convenience, smaller a (a_2) dominates over a_1 to determine the minimum required GB. Considering Ts = 1 / 80 MHz and substituting a_2 in (3-51) into (3-49) yields the minimum GB as 135 MHz. Cadence periodic steady-state (PSS) simulation is performed using ideal Op-Amps with variable GB and the result is plotted in Figure 38. As GB is increased, simulated f_0 is close to the ideal value of 10 MHz, and higher than 450 MHz of GB yields less than 2 % error.

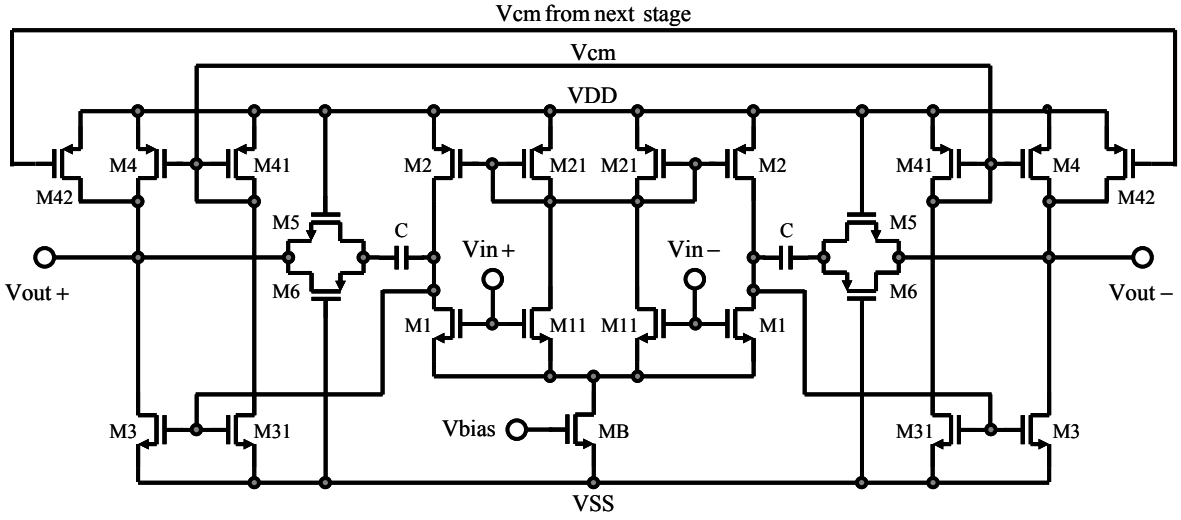
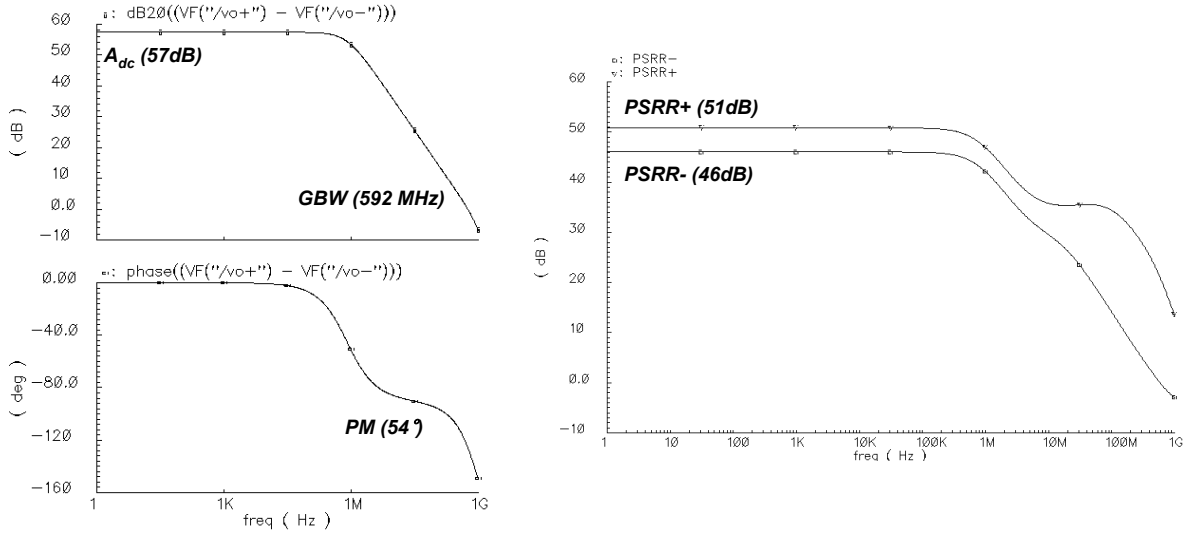


Figure 39. Fully-balanced fully-symmetric 2-stage amplifier schematic [37].

The Op-Amp is designed [31], [34] to have 57 dB, 592 MHz and 54° of DC gain, gain-bandwidth product and phase margin, respectively. The topology is a two-stage Miller-compensated structure, and is depicted in Figure 39. Transistors M11 and M21 form the common-mode feed-forward (CMFF) circuit to the first stage. CMFF to the second stage is implemented by transistors M31 and M41, and transistor M42 provides a common-mode feed-back control to the second stage [37]. Power supply is ±1.65 V and power

supply rejection ratio on V_{DD} and V_{SS} (PSRR+ and PSRR-) are simulated as 51 dB and 46 dB respectively as shown in Figure 40.



(a) (b)

Figure 40. Op-Amp simulation results. (a) Differential gain and phase response. (b) Power supply rejection ratio.

For a comparator, a one-stage differential amplifier [34] is designed as a pre-amplifier followed by 3-stage digital inverters as shown Figure 41. Outputs of inverters are used to control the switch that passes the external reference voltage V_{REF} to the final output voltage V_{COMP}. Using comparator output to control the hard-limiting switch enables to control the output amplitude precisely [24].

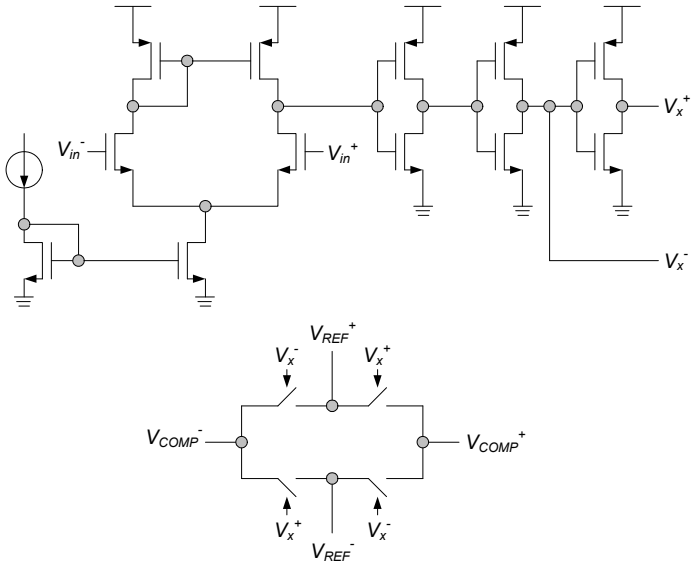
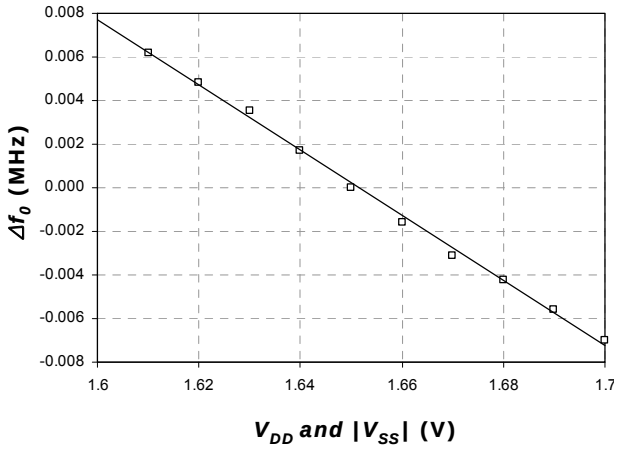


Figure 41. Schematic diagram of comparator [24].

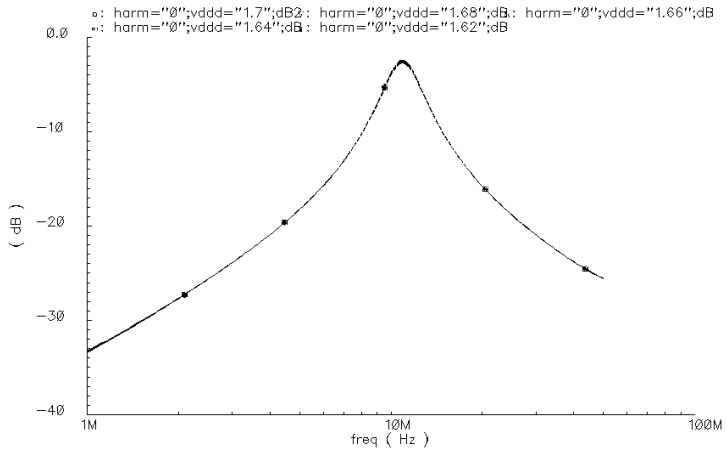
Although the oscillation frequency (f_0) tuning is not included in this work, it should be mentioned that the f_0 can be tuned without changing a master clock frequency (f_C) by adopting digitally-programmable capacitor arrays (DPCAs) [38]. By using one or two binary-weighted DPCAs, f_0 can change in power-of-two steps which lead to f_C/f_0 integer ratios and, hence, a jitter performance is not affected.

Power supply sensitivity of a BPF in Figure 33 is simulated when V_{DD} and $|V_{SS}|$ are varied 1.6 ~ 1.7 V, and results are shown in Figure 42. A center frequency sensitivity for power supply is -0.15 MHz/V (= $\Delta f_0 / \Delta V_{DD}$). Transfer function gain is simulated using periodic steady-state analysis in Cadence, and the results for different power supplies are plotted Figure 42 (b). A variation power supply voltage is appeared as a common-mode variation of an amplifier contributing deviations of a BPF behavior from an ideal case. Since power supply values are changed in this simulation, it represents DC

point of PSR of a BPF. The results show that this SC-BPF is not sensitive to power supply variation. This is due to high value of power supply (3.3 V), however it can be a serious problem in low-voltage environment.



(a)



(b)

Figure 42. Power supply sensitivity of BPF in Figure 33. (a) Center frequency variation. (b) Gain of transfer function variation.

3.5. Low-Voltage Design Techniques in SC Circuit

As CMOS technology continuously scales down, new design techniques are needed to tolerate low voltage headroom. A supply voltage keeps being reduced in advanced technologies while a threshold voltage is not scaled with same factor. In a switched capacitor circuit, MOS switches will encounter severe overdrive problems since their gate is controlled by Vdd. When a switch processes a signal with large amplitude, a CMOS switch is used to deal with this problem. However, as shown in Figure 43, if V_{DD} and V_{SS} are scaled down such that $V_{TN} + |V_{TP}| > V_{DD} + |V_{SS}|$, then it would not possible to turn the switch on, even if a CMOS transmission gate is used [39].

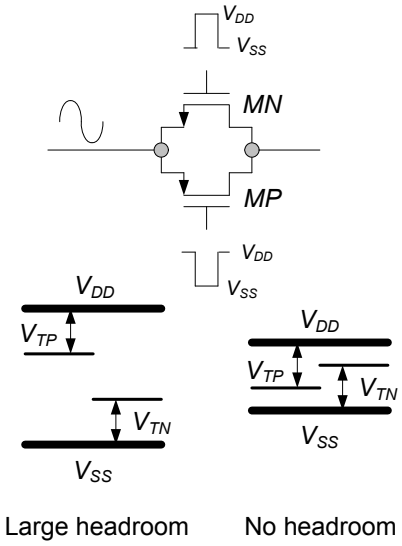
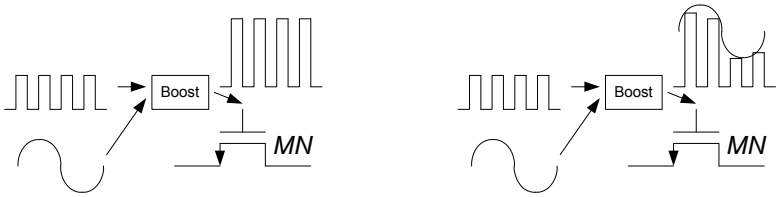


Figure 43. No headroom problem of CMOS switch in low-voltage environment.

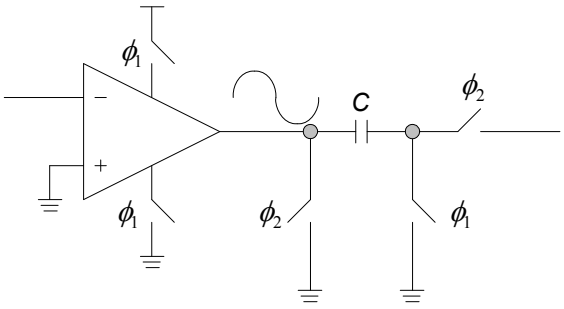
There have been several approaches to bypass this problem. One uses a boosted clock to obtain high-swing clock [40], as shown in Figure 44 (a), usually doubling the voltage amplitude of a clock signal. Since a voltage boosting is done by internal circuit, this solution can be used where a supply voltage is restricted by an external source and a gate oxide of a transistor can tolerate a doubled clock voltage. However, this technique cannot be used if gate oxide is very thin and its breakdown voltage is lower than $2V_{DD}$, which is the case in the advanced low-voltage CMOS technology. To overcome this difficulty, a bootstrapped clock method is introduced [41, 42]. Unlike previous clock boosting, the clock is boosted depending on the input signal voltage, as depicted in Figure 44 (b). Since the input signal is applied on the source of a transistor and a clock is to the gate, this technique makes a constant Vgs for a switch transistor avoiding gate oxide breakdown problem. However, temporary high voltage glitches taking place before a channel is formed may affect a long-term reliability. This technique also increases the circuit complexity involved in the implementation of a good bootstrapped switch [39].

Another alternative is to switched op-amp technique [43] that is shown in Figure 44 (c). This technique is called switched op-amp because it is based on the replacement of the critical switches with op-amps which are turned on and off. It does not require voltage multiplier for a clock boosting and results in a very low voltage operation. However, this approach suffers from some short-comings. Specifically, the increased settling time introduced by the required power-up / power-down of the op-amp output stage slows down the operation and limits the maximum clock rate [39].

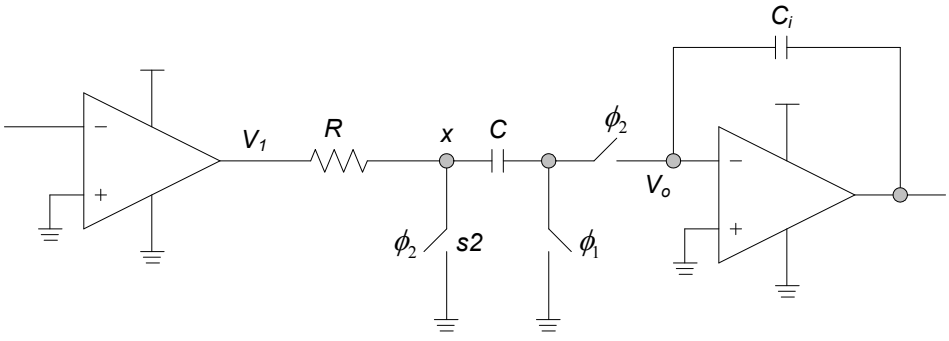
The last approach shown in Figure 44 (d) is switched-RC technique [44] in which the critical switches are replaced with passive resistors. With a passive resistor, the linearity of the input sampling would be improved. And, since the op-amp is always operating, there is no issue regarding the settling time related to the op-amp.



(a) (b)



(c)



(d)

Figure 44. Low-voltage switch techniques. (a) Clock boosting with a fixed ratio. (b) Clock bootstrapping. (c) Switched Op-amp. (d) Switched-RC.

The replaced passive resistor R introduces a gain error in the case of integrator as shown in Figure 44 (d). During the ϕ_2 phase, the charge stored in C is transferred to C_i and V_x would be determined by the ratio of R and the on resistance of the MOS sitch s_2.

Assuming high oversampling ratio where $V_1(n + 1/2)$ can be approximated to $V_1(n)$, V_x at the ϕ_2 phase can be expressed as

$$V_x\left(n+\frac{1}{2}\right)=\frac{R_{on,s2}}{R+R_{on,s2}}V_1\left(n+\frac{1}{2}\right)\approx\frac{R_{on,s2}}{R+R_{on,s2}}V_1(n) \tag{3-52}$$

V_o at this phase becomes

$$V_o\left(n+\frac{1}{2}\right)=V_o(n)+\frac{C}{C_i}V_1(n)-\frac{C}{C_i}\frac{R_{on,s2}}{R+R_{on,s2}}V_1(n) \tag{3-53}$$

The gain error associated with this is [44]

$$Gain\,Error=\frac{C}{C_i}\frac{R_{on,s2}}{R+R_{on,s2}} \tag{3-54}$$

(3-54) suggests that the gain error can be reduced by making resistor R much larger than $R_{on,s2}$. However, large R also degrades the sampling accuracy due to the increased RC

constant in the ϕ_1 phase. Therefore, R should be carefully determined considering the design trade-off between the gain error and the sampling accuracy [44].

3.6. Experimental Results

The proposed SC BPF-based oscillator using the BPF of Figure 35, auxiliary clock generator of Figure 32 and a conventional two-level comparator, along with a two-phase non-overlapping clock generator to provide the necessary clock signals, was designed and implemented. In order to compare the improvement of the linearity with a multi-level comparator, a conventional SC BPF-based oscillator using the BPF of Figure 33 was designed as well. Both of oscillators are exactly the same except for the four-level comparator in the proposed oscillator. The chip was fabricated in 4-metal double-poly TSMC 0.35um technology and thanks to the MOSIS Educational Program. Each BPF has a center frequency of f_0 = 10 MHz, a Q-factor of 10 and a master clock frequency of f_C = 80 MHz. The microphotograph of the fabricated chip is shown in Figure 45. The silicon area is 0.20 mm^2 for the proposed SC BPF-based oscillator and 0.18 mm^2 for the conventional SC BPF-based oscillator. The power consumption of the proposed oscillator is 20.1 mW while 19.8 mW is consumed by the conventional oscillator. Two OP-Amps in the BPF consume 16.5 mW and 3.3 mW is consumed by a comparator.

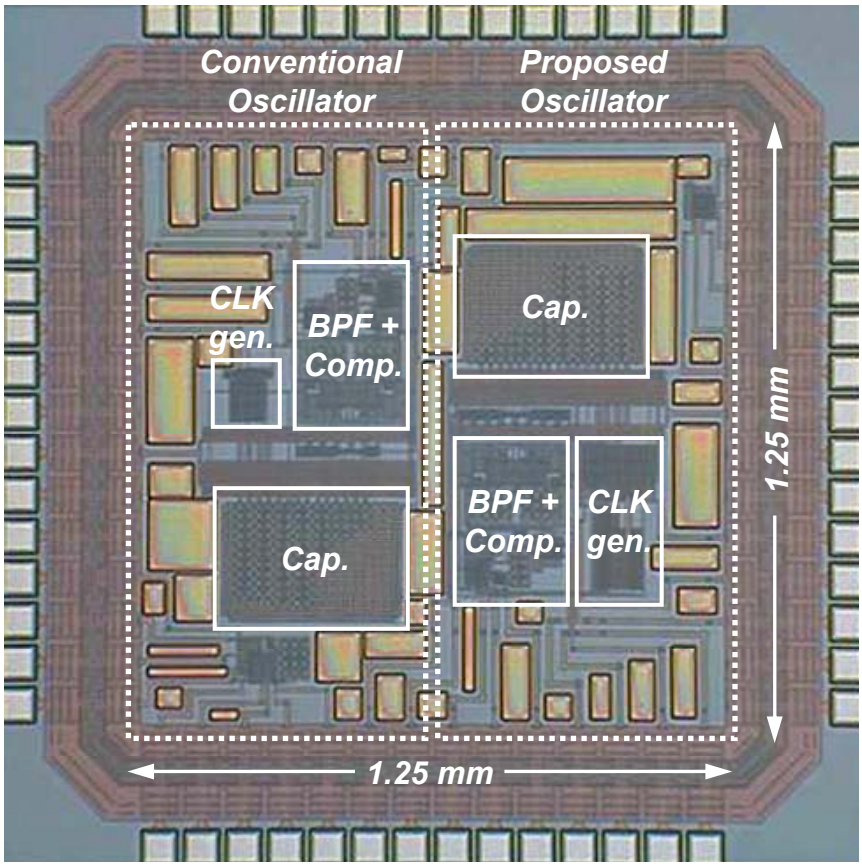


Figure 45. Chip microphotograph of oscillators.

The designed circuit is encapsulated using TQFP-64 package. It has 64 pins and a lead pitch is 0.5 mm and, a body size is 10 mm x 10 mm. TQFP package is widely used because of the cheap manufacturing cost and convenient soldering however, its applications are limited to low frequency, usually below than GHz due to parasitic effects. The printed circuit board (PCB) was designed and fabricated for the measurement of the chip. The picture of PCB is shown in Figure 46.

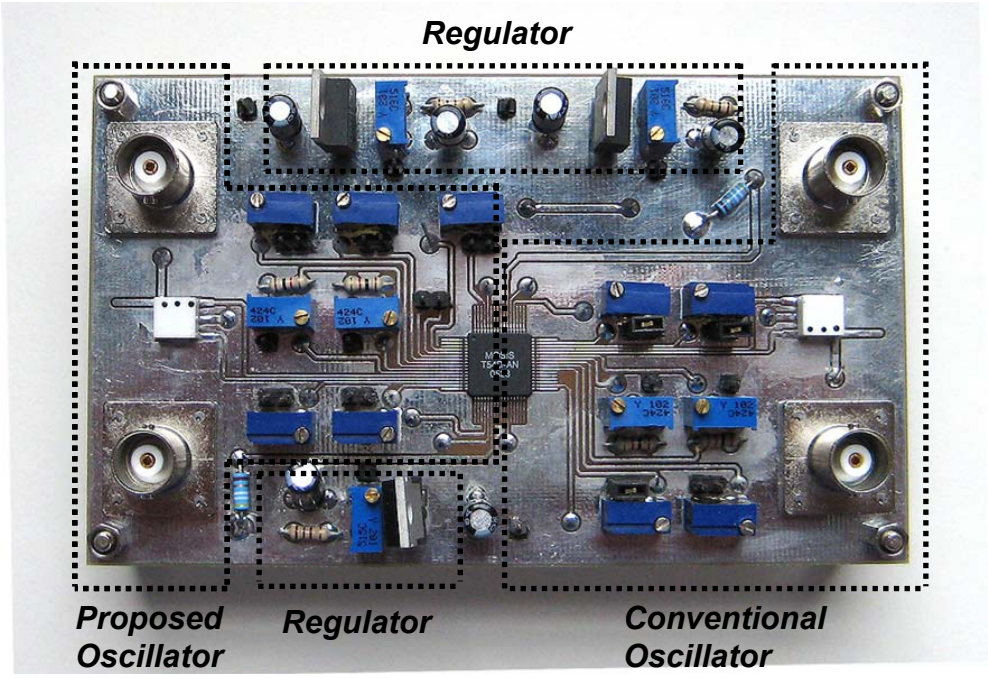


Figure 46. PCB for oscillator testing.

The PCB was fabricated on the industry standard 0.062” FR-4 laminate and two metal layers (top and bottom) are used for conductors. Since it includes the proposed oscillator as well as a conventional oscillator, every components including pin assignments is placed in symmetrical way.

Each oscillator has two variable voltage regulator blocks to provide separate supply voltage to the analog block and the digital block. Big capacitors (10 μF) were used for a bypassing to enhance the supply voltage filtering. The oscillator output is taken as a differential signal amplified by an open-drain buffer inside of the chip. They should be converted to a single-ended signal and terminated with a 50 Ω impedance due to the spectrum analyzer requirement. A transformer with balanced and unbalanced (Balun) ports was used for this purpose. However, an impedance matching is not as

critical issue as in a low-noise amplifier or a power amplifier in oscillators. Each bias was generated by variable resistors (potential meters).

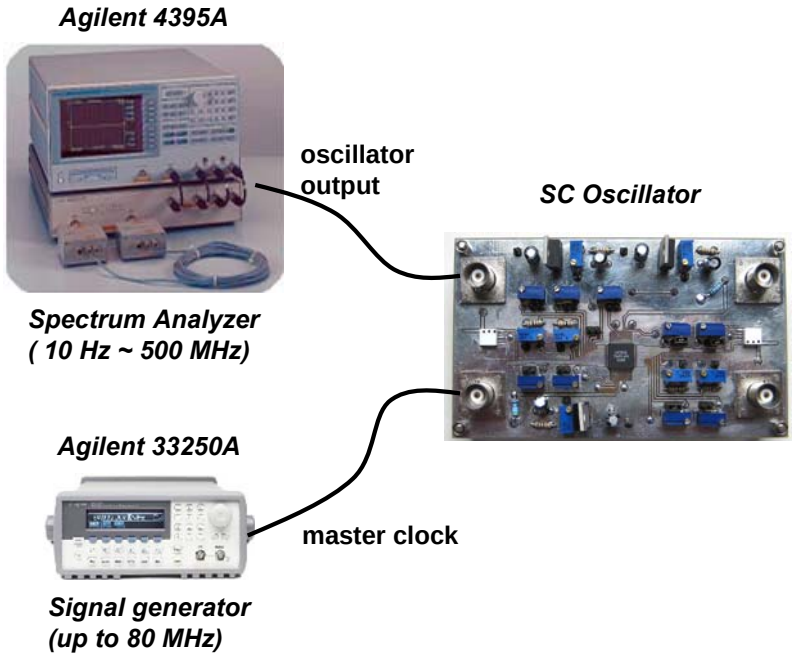


Figure 47. Testing SC oscillator setup.

The test setup for measurement is illustrated in Figure 47. For a master clock generation, Agilent 33250A signal generator is used. It is able to generate any shape of signal up to 80 MHz. The oscillator output is measured using Agilent 4395A spectrum analyzer that can be used up to 500 MHz.

For the testing, all parasitic effects through the buffer and the pad frame were de-embedded by measuring the stand-alone buffer as shown in Figure 48.

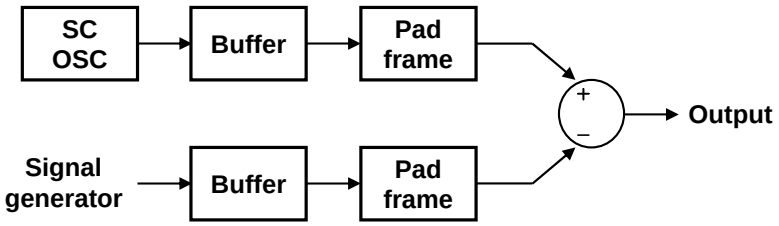
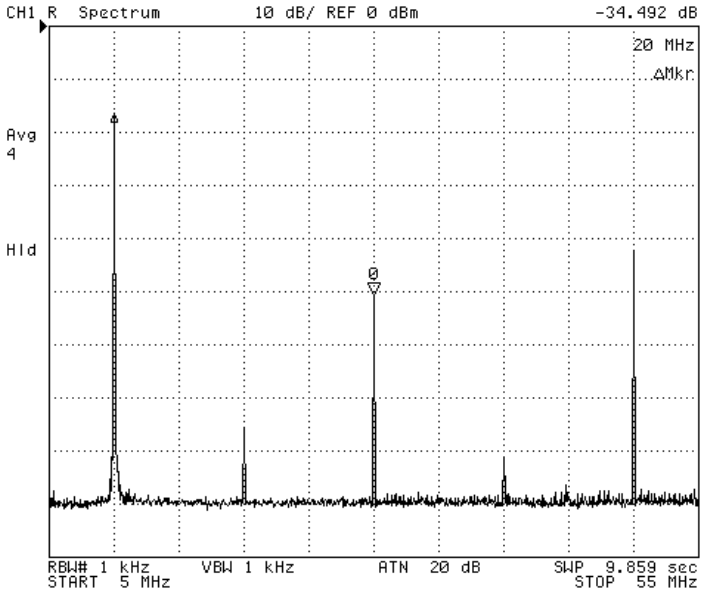
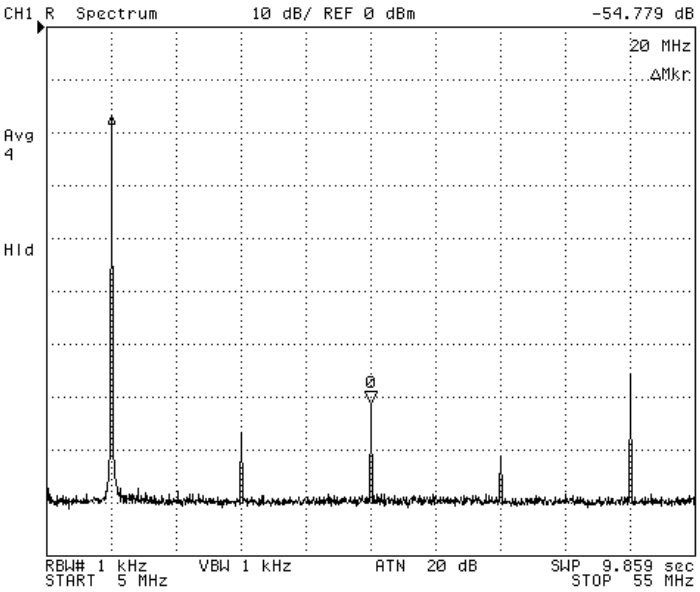


Figure 48. De-embedding with a stand-alone buffer.

Frequency spectrums for both oscillators (conventional and proposed) are shown in Figure 49. Since the clock frequency is 80MHz, all the frequency components beyond 40MHz are aliased from low frequency due to the sampling nature of the SC circuit. Due to this, only the third-order harmonic is considered as meaningful and, hence, HD3 is measured. Figure 49 (a) shows the frequency spectrum of conventional SC BPF-based oscillator yielding HD3 of -34.5dB. Figure 49 (b) is the frequency spectrum of the proposed SC BPF-based oscillator and -54.8dB of HD3 was achieved, which shows that 20dB of HD3 was improved by the proposed four-level square wave generator.

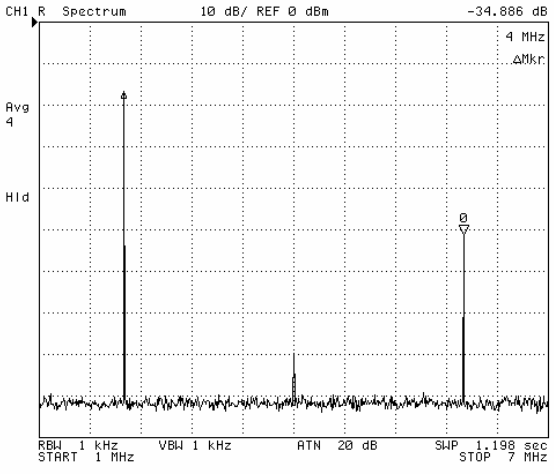


(a)

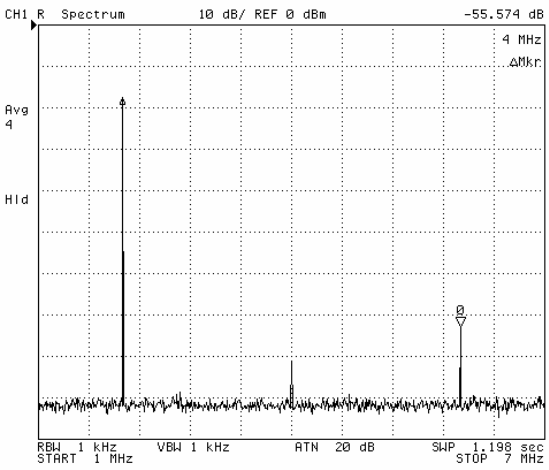


(b)

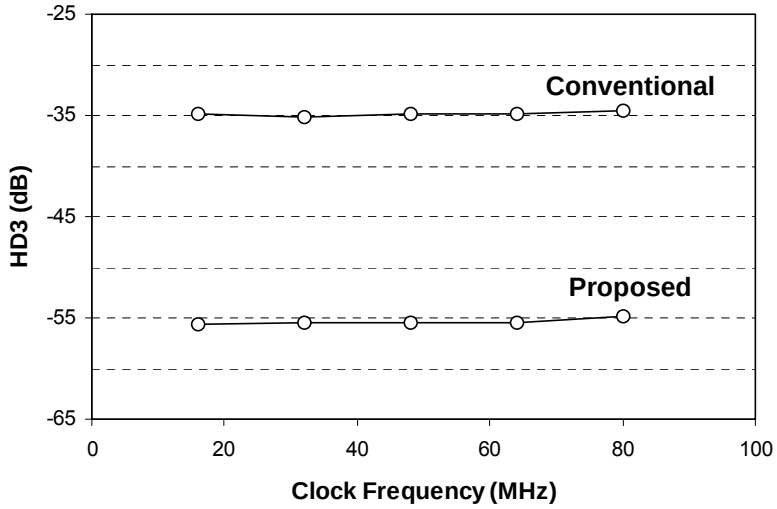
Figure 49. Frequency spectrum for a 10 MHz oscillation frequency. (a) Conventional SC oscillator. (b) Proposed SC oscillator.



(a)



(b)



(c)

Figure 50. Additional experimental results. (a) Conventional SC oscillator at f_{CLK} = 16 MHz. (b) Proposed SC oscillator at f_{CLK} = 16 MHz. (c) HD3 comparison at different clock frequencies.

HD3 was also measured while varying f_0 from 2 MHz to 10 MHz by changing f_C from 16 MHz to 80 MHz and, an almost constant HD3 improvement of 20dB was observed with respect to the conventional case as shown in Figure 50. HD3 improvement of the proposed oscillator over the conventional oscillator is mainly determined by the accuracy of the ratio between the two multiplying factors, which is $\sqrt{2}$ in our case, as showed in Figure 30. This ratio is represented by the ratio of integers because a multiplying factor is implemented by the multiple numbers of the unit capacitor. In this work, to reduce the spread of capacitor values, the ratio of 4:3 (=1.33) was chosen to achieve the ratio which roughly approximates to $\sqrt{2}$ (=1.4142) for the minimum area expense. The ratio of 1.33 yields a non-ideal magnitude factor (Δ_m) of 6% and degrades the third-order harmonic rejection as shown in Figure 27. Since the oscillator output is measured at the BPF output, HD3 will be suppressed 34 dB (= $10\times log(nQ) = 10\times log(3\times 10)$) more [24] from the value suggested in Figure 27 which is the BPF input.

Although other ratios such as 10:7 (=1.4286) and 17:12 (=1.4167) are more close to the desired value (1.4142), the trade-off between the spread of capacitor values and accuracy is depicted in Figure 27. Observe that a small amount of the second order harmonic (approximately -77 dBm) is seen in Figure 49 (a) and (b), which is due to mismatch in the fully differential circuit and other non-ideal effects.

Table 2. Performance summary and comparison with other published solutions.

Parameters	This work (Proposed)	This work (Conventional)	[45]	[38]	[46]
Maximum clock frequency	80 MHz	80 MHz	10 MHz	100 MHz	800 MHz
Maximum output frequency	10 MHz	10 MHz	1 MHz	25 MHz^{+}	400 MHz^{++}
Design Technique	SC BPF (2nd-order)	SC BPF (2nd-order)	SC BPF (4th-order)	DDFS	DDFS
Q-factor	10	10	85	N/A	N/A
THD, SFDR* @ Output frequency	-54.8 dB @ 10 MHz	-34.5 dB @ 10 MHz	-72 dB @ 1 MHz	42.1 dBc* @ 1.56 MHz	55 dBc* @ 8 MHz
Active area	0.2 mm^2	0.18 mm^2	0.12 mm^2	1.4 mm^2	1.47 mm^2
Technology	0.35 um CMOS	0.35 um CMOS	0.35 um CMOS	0.5 um CMOS	0.35 um CMOS
Power consumption	20.1 mW	19.8 mW	23 mW	8 mW	174 mW
Power supply	3.3 V	3.3 V	3 V	2.7 V	3.3 V

$^{+, ++}$ At the maximum output frequencies, SFDR is 17 dBc^{+} and 23 dBc^{++}.

* SFDR is presented instead of harmonic distortions.

Table 2 compares the measured performance with other published solutions including direct digital frequency synthesizer (DDFS) [38], [46]. In case of DDFS, spurious-free dynamic range (SFDR) is taken to compare distortions. The proposed SC oscillator shows higher maximum frequencies than the other SC oscillator [45] and, less active area and lower distortion compared to [38] and [46] with a comparable spectral purity.

3.7. Conclusions

A non-linear shaping technique based on a multi-level comparator for SC BPF-based oscillator has been proposed. Its property of rejecting the third- and fifth-order harmonics improves the overall linearity in SC BPF-based oscillator compared with the conventional SC BPF-based oscillator. A simple implementation of a multi-level square wave generator with minimum additional area (10% of the total area) is also proposed. Both the conventional and the proposed oscillators were designed and fabricated to compare the linearity properties. For both oscillators with equal Q-factor of 10, the improvement of 20dB on HD3 was achieved with the proposed oscillator yielding -54.8dB while -34.5dB was measured from the conventional oscillator. Further linearity improvement can be obtained by increasing the accuracy of the step magnitude of the multi-level comparator at the expense of extra area.

CHAPTER IV

RF OSCILLATOR BASED ON A PASSIVE RC BANDPASS FILTER

4.1. Introduction

The phase-locked loop (PLL) is a key building block in many high-speed systems [47-53] as it accurately generates desired frequency tones. Inside the PLL, the voltage-controlled-oscillator (VCO) is the circuit that generates the tone at a specific frequency which is tunable by a control voltage. The most suitable oscillator type depends on the application: e.g. for the radio frequency (RF) communication systems, the LC oscillator is preferable due to its excellent phase noise performance [4]. However, in CMOS process, an inductor is expensive because it is not a standard device and takes a significant silicon area. In some cases, an LC oscillator is more than one hundred times bigger than a ring oscillator. In many modern CMOS processes, a thick copper metal is used for an inductor instead of a standard aluminum to improve a quality factor (Q-factor), which also increase the fabrication cost. Also, the accuracy and flexibility of a model can be problematic for the designer because the design parameters are typically limited to insure a better model accuracy.

Ring oscillator can provide an alternative where phase noise requirements are not stringent since phase noise performance of a ring oscillator is normally 30 ~ 50 dB worse than a LC oscillator [1, 54, 55]. A ring oscillator can be built with cheap fabrication costs, as it does not require an inductor. In addition, ring oscillators have a

wide frequency tuning range and can be used for applications where large frequency range should be covered. For examples, TV receiver requires 41 ~ 960 MHz range (184%), satellite TV front-end needs 950 ~ 2150 MHz (77 %), and the range for DVB-T is 470 ~ 860 MHz (59 %) [5]. However, the phase noise and jitter performance is not as good as an LC oscillator, and ring oscillators are sensitive to power supply noise [56]. Furthermore, the oscillating frequency is limited by the number of stages as the total period is twice the sum of the stage delays. The minimum number of stages is typically three, since the phase at the unity gain frequency is not sufficient if the standard two-stage topology is used. There have been several approaches to decrease the number of stages to increase the maximum oscillation frequency and decrease the power consumption [52, 57, 58]. However, even if an active inductance is used, one still needs at least two stages, because the load is low-pass, contributing only 90º phase. Also, since the inductance is introduced by using active devices [52], the oscillation frequency is vulnerable to process variations. There are other approaches to increase the maximum oscillation frequency of a ring oscillator using different delay paths [59-61]. However, the improvement in frequency is not as significant as reducing the number of delay stages.

In this work, an RC bandpass filter (BPF)-based oscillator is proposed. Since the load is a BPF-type, it provides a sufficient phase with only one stage. Because the oscillation frequency is determined by a BPF made of passive resistors and capacitors, the frequency is immune to power supply noise [56]. A Wien-Bridge oscillator [62] is a classical oscillator that uses a BPF property using passive resistors and capacitors.

However, the oscillation frequency is limited by the gain-bandwidth product (GBP) of an operational amplifier (OP-amp), as a result, a Wien-Bridge oscillator is not practical in GHz frequency ranges. In RF applications, a preferred BPF-based oscillator is a LC oscillator because the LC-tank exhibits a BPF property. In the proposed oscillator, an RC BPF is employed to avoid using an expensive inductor.

The chapter is organized as follows: Section 4.2 explains the theory and background behind the BPF-based oscillator; Section 4.3 discusses the BPF-based oscillator implementation and practical performance limitations; Section 4.4 presents measurement results; Section 4.5 explores a quadrature oscillator using two anti-phase coupled oscillators and a ring structure of band-pass filters for an arbitrary phase generation; and section 4.6 concludes.

4.2. Background of BPF-Based Oscillator

Figure 51 shows a conventional block diagram of a BPF-based oscillator. A BPF is used together with a positive feedback amplifier yielding an oscillating signal (V_{out}). The BPF is assumed to be a second-order system and characterized by a center frequency ω_0, a quality-factor (Q-factor) Q and a coefficient k.

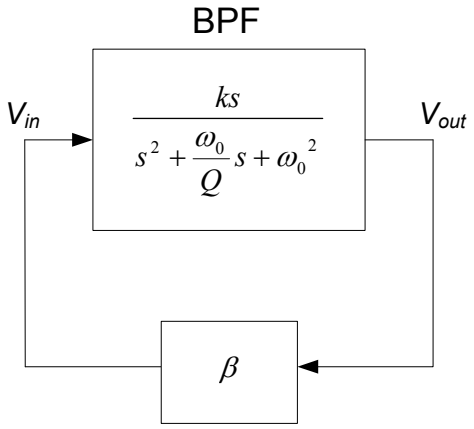


Figure 51. Block diagram of a BPF-based oscillator.

The BPF has one zero at DC and two poles; its phase response varies from +90º to -90º and crosses 0º at ω_0, which is a sufficient phase condition for oscillation. Two poles are initially placed at the left-half plane (LHP) and pushed toward right-half plane (RHP) by the positive feedback with a loop gain β. Poles in a closed loop can be found by solving characteristic equation that is $s^2 + (\omega_0 / Q - \beta k)s + \omega_0^2 = 0$ .If β is large enough, then the two poles are displaced to the RHP since a real part of poles becomes positive and the oscillation is established. Tuning ω_0 of the BPF tunes the oscillation frequency. The minimum required value of β is determined by Q i.e. $\omega_0 / (kQ)$.

The frequency selectivity of the BPF is inversely proportional to Q, indicating that high Q reduces the phase noise of an oscillator [3, 4]. To prove the effect of Q on phase noise, a feedback system as shown in Figure 52 is assumed. Here, an open loop transfer function becomes 1 at a center frequency ω_0 by setting $k = \omega_0 / Q$ and $\beta = 1$.

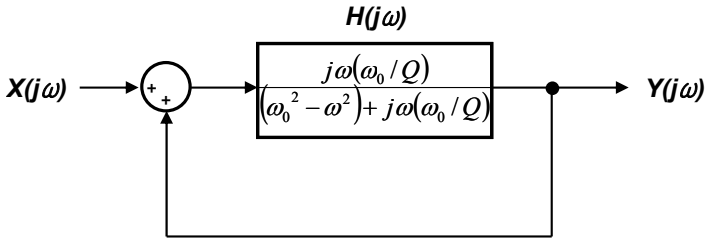


Figure 52. Linear oscillatory system.

$$H(j\omega_0) = 1 \tag{4-1}$$

Let $H(j\omega)$ expressed as $H(j\omega) = A(\omega)\exp[j\Phi(\omega)]$, then its derivative can be expressed as

$$\frac{dH}{d\omega} = \left(\frac{dA}{d\omega} + jA\frac{d\Phi}{d\omega}\right)\exp(j\Phi) \tag{4-2}$$

Evaluating (4-2) at $\omega = \omega_0$ yields,

$$\left.\frac{dH}{d\omega}\right|_{\omega=\omega_0} = \left(\left.\frac{dA}{d\omega}\right|_{\omega=\omega_0} + jA(\omega_0)\left.\frac{d\Phi}{d\omega}\right|_{\omega=\omega_0}\right)\exp(j\Phi(\omega_0)) = j\left.\frac{d\Phi}{d\omega}\right|_{\omega=\omega_0} \tag{4-3}$$

since $dA/d\omega|_{\omega = \omega 0} = 0$, $A(\omega_0) = 1$ and $\Phi(\omega_0) = 0$. Phase of a transfer function in Figure 52 and it derivative are

$$\Phi(\omega) = 90^\circ + \tan^{-1}\frac{(\omega_0 / Q)\omega}{\omega^2 - {\omega_0}^2} \tag{4-4}$$

$$\frac{d\Phi}{d\omega}=\frac{\dfrac{\omega_0/Q}{\omega^2-{\omega_0}^2}-\dfrac{2(\omega_0/Q)\omega^2}{\left(\omega^2-{\omega_0}^2\right)^2}}{1+\left(\dfrac{(\omega_0/Q)\omega}{\omega^2-{\omega_0}^2}\right)^2}=\frac{(\omega_0/Q)\left(\omega^2-{\omega_0}^2\right)-2(\omega_0/Q)\omega^2}{\left(\omega^2-{\omega_0}^2\right)^2+\left((\omega_0/Q)\omega\right)^2} \tag{4-5}$$

$$\left.\frac{d\Phi}{d\omega}\right|_{\omega=\omega_0}=\frac{-2(\omega_0/Q){\omega_0}^2}{\left((\omega_0/Q)\omega_0\right)^2}=\frac{-2Q}{\omega_0} \tag{4-6}$$

Note that (4-5) is referred as a group delay. The close loop transfer function in Figure 52 is

$$H_{CL}(j\omega)=\frac{Y}{X}(j\omega)=\frac{H(j\omega)}{1-H(j\omega)} \tag{4-7}$$

For frequencies close to the carrier, $\omega=\omega_0+\Delta\omega$, the open loop transfer function becomes

$$H(j\omega)\approx H(j\omega_0)+\Delta\omega\frac{dH}{d\omega} \tag{4-8}$$

and with (4-1) and the assumption of $|\Delta\omega\ dH/d\omega| << 1$, the close loop transfer function is

$$H_{CL}\left[j(\omega_0+\Delta\omega)\right]=\frac{Y}{X}\left[j(\omega_0+\Delta\omega)\right]=\frac{H(j\omega_0)+\Delta\omega\dfrac{dH}{d\omega}}{1-H(j\omega_0)-\Delta\omega\dfrac{dH}{d\omega}}=\frac{-1}{\Delta\omega\dfrac{dH}{d\omega}} \tag{4-9}$$

(4-9) indicates that a noise component at $\omega=\omega_0+\Delta\omega$, is multiplied by $-1/(\Delta\omega\ dH/d\omega)$ when it appears at the output of the oscillator. This also means that the noise power spectral density is shaped by

$$\left|H_{CL}\left[j(\omega_0+\Delta\omega)\right]\right|^2=\left|\frac{Y}{X}\left[j(\omega_0+\Delta\omega)\right]\right|^2=\frac{1}{(\Delta\omega)^2\left|\frac{dH}{d\omega}\right|^2} \tag{4-10}$$

Substituting (4-3) and (4-6) to (4-10) yields

$$\left|H_{CL}\left[j(\omega_0+\Delta\omega)\right]\right|^2=\left|\frac{Y}{X}\left[j(\omega_0+\Delta\omega)\right]\right|^2=\frac{1}{(\Delta\omega)^2\left(\frac{2Q}{\omega_0}\right)^2}=\frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4-11}$$

(4-11) indicates that any noise sources within the oscillator can be refered to the input, and they will be shaped by (4-11) and appeared at the output. It can be concluded from (4-11) that high Q reduces the phase noise of an oscillator.

A popular BPF-based oscillator at low frequencies is a Wien-bridge oscillator shown in Figure 53 [62]. An Op-amp is used for positive feedback and its voltage gain is A_v. The oscillation frequency (O.F.) and the oscillation condition (O.C.) are determined from the open loop transfer function as

$$\frac{V_{out}}{V_{in}}(s)=\frac{\frac{1}{RC}s}{s^2+\frac{3}{RC}s+\left(\frac{1}{RC}\right)^2}$$
$$O.F.:\ \omega_0=1/(RC) \qquad (4\text{-}12)$$
$$O.C.:\ A_v\geq 3$$

However, this approach is only valid at very low frequency of operation (< 1% of the Op-amp bandwidth) [63].

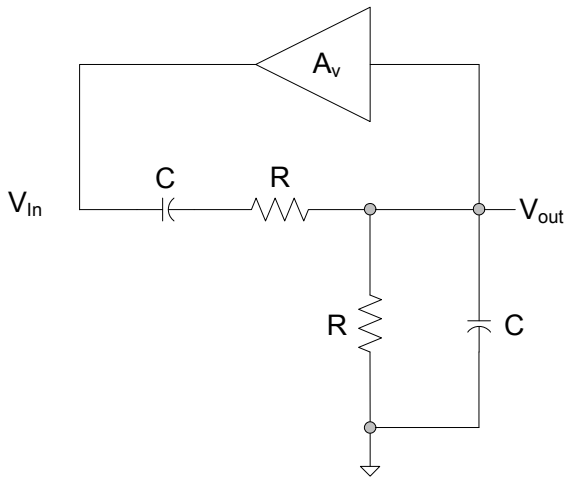


Figure 53. Block diagram of Wien-bridge oscillator.

Assuming an Op-amp is a one-pole system with a dc gain A_v and a cut-off frequency ω_p,then (4-12) becomes [63]

$$O.F.:\ \omega^2=\frac{{\omega_0}^2}{1+3A_v(\omega_0/\omega_p)}$$
$$O.C.:\ A_v\geq\frac{3}{1-(\omega_0/\omega_p)(1-\omega^2/{\omega_0}^2)} \qquad (4\text{-}13)$$

It is easy to show that the coupling between two equations in (4-13) procduces the maximum operation frequency. In this particular case, the maximum frequency is bounded by 16.67% of the GBP of the Op-amp [63]. Due to this limitation, Wien-bridge oscillator is not suitable for high frequency.

To overcome this frequency limitation, an oscillator using an operational transconductance amplifier (OTA) was proposed in [64] as shown in Figure 54.

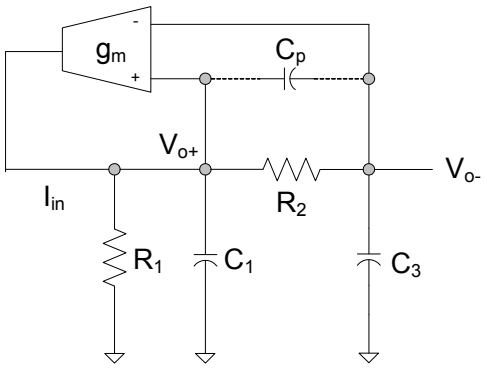


Figure 54. Oscillator diagram using a differential transconductance amplifier.

Since an OTA does not have a low impedance output stage and can be implemented as a simple structure, it is possible to operate at higher frequencies than an Op-amp. An open loop transfer function from I_{in} to a differential output voltage V_o^+-V_o^- and a closed loop equation are

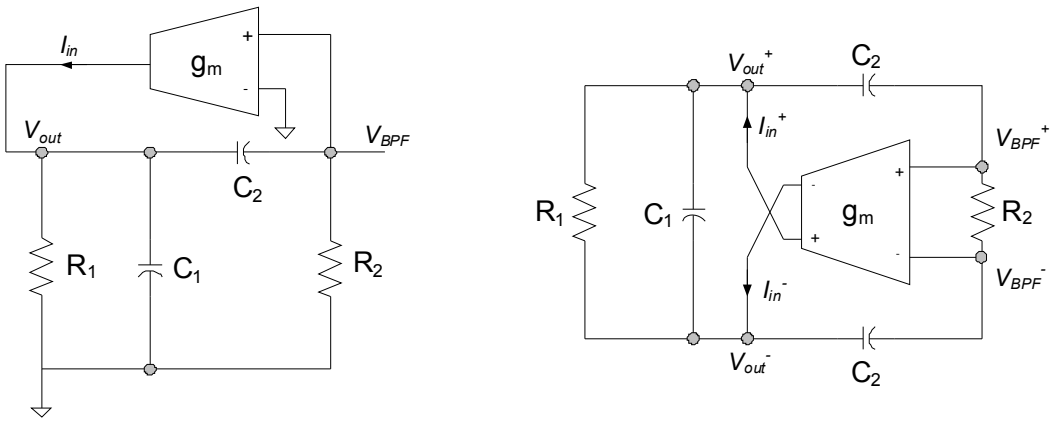
$$H_{Z_0}(s)=\frac{V_o^+-V_o^-}{I_{in}}=\frac{\frac{1}{C_1}s}{s^2+\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}s+\frac{1}{R_1C_1R_2C_2}}$$
$$H_{Z_0,CL}(s)=\frac{\frac{1}{C_1}s}{s^2+\left(\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}-\frac{g_m}{C_1}\right)s+\frac{1}{R_1C_1R_2C_2}} \quad (4\text{-}14)$$

Applying Barkhausen criterion to (4-14) yields the oscillation frequency and condition as

$$O.F.:\ \omega_0=\frac{1}{\sqrt{R_1C_1R_2C_2}}$$
$$O.C.:\ g_m\geq\frac{1+C_1/C_2+R_2/R_1}{R_2} \quad (4\text{-}15)$$

However, this oscillator requires both negative and positive feedback and, the oscillation frequency is sensitive to the mismatch between the two different feedbacks. Also, there is a parasitic capacitance at the input of the OTA that modifies the transfer function.

Figure 55 (a) shows the block diagram of a single-ended version of the proposed oscillator. An OTA with a positive gain is easily implemented by a fully differential structure as shown in Figure 55 (b). An RC BPF is incorporated with a feedback through the single input OTA. A feedback gain β in Figure 51 is g_m in the proposed oscillator.



(a) (b)

Figure 55. Block diagram of a proposed oscillator (a) Single-ended version (b) Fully differential version.

The open loop transfer function of the BPF yields,

$$H(s) = \frac{V_{BPF}}{I_{in}} = \frac{\frac{1}{C_1}s}{s^2 + \frac{1 + C_1/C_2 + R_2/R_1}{R_2 C_1}s + \frac{1}{R_1 C_1 R_2 C_2}} \tag{4-16}$$

The feedback through the OTA must be positive and the OTA gain (g_m) should be large enough to initially place the poles of the closed loop at the RHP causing the oscillation to start. A closed loop equation H_{CL}(s) and a characteristic equation D(s) are

$$H_{CL}(s)=\frac{H(s)}{1-g_m H(s)}=\frac{(1/C_1)s}{D(s)}$$
$$D(s)=s^2+\left(\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}-\frac{g_m}{C_1}\right)s+\frac{1}{R_1C_1R_2C_2} \quad (4\text{-}17)$$

The oscillation frequency that is set by the BPF center frequency ω_0, and the minimum requirement for g_m ($g_{m,min}$) are given by,

$$\omega_0{}^2=\frac{1}{R_1C_1R_2C_2},\qquad g_{m,\min}=\frac{1+C_1/C_2+R_2/R_1}{R_2} \quad (4\text{-}18)$$

The Q-factor, an important design parameter for a BPF-based oscillator, yields,

$$Q=\frac{\sqrt{(C_1/C_2)\cdot(R_2/R_1)}}{1+C_1/C_2+R_2/R_1} \quad (4\text{-}19)$$

Note that if resistors and capacitors are chosen as $R_1 = R_2 = R$ and $C_1 = C_2 = C$ for design convenience, then $\omega_0 = 1/(RC)$, $g_{m,min} = 3/R$ and $Q = 1/3$. Rewriting (4-19) as

$$Q=\frac{\sqrt{x_C\cdot x_R}}{1+x_C+x_R} \quad (4\text{-}20)$$

where $x_C = C_1 / C_2$ and $x_R = R_2 / R_1$. The maximum condition of (4-20) can be found by solving the partial derivation of (4-20) to x_R,

$$\frac{\partial Q}{\partial x_R} = \frac{0.5\sqrt{x_C / x_R}}{1 + x_C + x_R} - \frac{\sqrt{x_C x_R}}{\left(1 + x_C + x_R\right)^2} = 0 \quad \Rightarrow \quad x_R = 1 + x_C \tag{4-21}$$

Applying the result of (4-21) to (4-20) yields

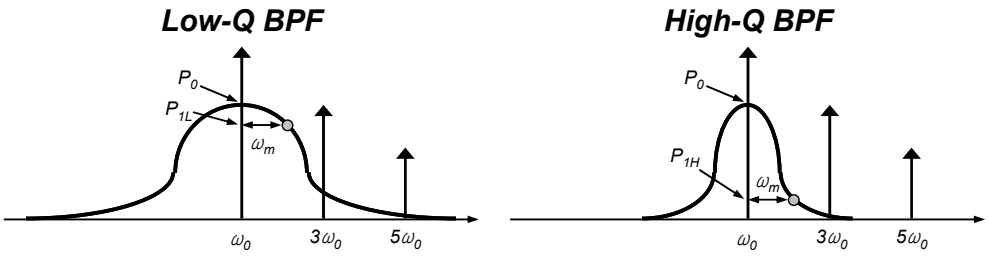
$$\begin{aligned} Q &= \frac{\sqrt{x_C \cdot \left(1 + x_C\right)}}{2\left(1 + x_C\right)} \\ \frac{dQ}{dx_C} &= \frac{1}{4\sqrt{x_C \cdot \left(1 + x_C\right)^3}} \end{aligned} \tag{4-22}$$

Q in (4-22) is a monotonic function to x_C, and its maximum can be achieved only when x_C is infinite since its derivative over x_C becomes zero when x_C is infinite. Hence, the maximum Q is 0.5.

$$Q_{\max} = \left.\frac{\sqrt{x_C \cdot \left(1 + x_C\right)}}{2\left(1 + x_C\right)}\right|_{x_C \to \infty} = \frac{1}{2} \tag{4-23}$$

From (4-23), it can be concluded that the maximum achievable Q-factor is 0.5 when both R_2/R_1 and C_1/C_2 are infinite.

As Q-factor is increased, the BPF has higher frequency selectivity. As expressed in (4-11), at a given oscillating frequency ω_0 and a frequency offset ω_m, the output will be decreased for higher Q. Hence, the total harmonic distortion (THD) and phase noise performance of the oscillator are improved [3, 65, 66] as illustrated in Figure 56.



(a) (b)

Figure 56. Q-factor in BPF. (a) Low-Q. (b) High-Q.

Leeson has derived the following equation to explain phase noise in a feedback oscillator [3] as given at (4-24).

$$L\{\Delta\omega\} = 10 \cdot \log\left(\left[1 + \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right]\frac{FkT}{P}\right) \tag{4-24}$$

where F is noise factor, k is Boltzman constant, T is absolute temperature and P is a carrier power. According to the equation of (4-24), phase noise at a moderate offset frequency is improved by 3.5 dB when Q is improved from 0.333 to 0.5.

The BPF can be implemented in various ways using an Op-amp with passive R and C (active-RC) [67, 68] or an OTA with C (gm-C) [69]. Although the above implementations using amplifiers have many advantages such as a high Q-factor and frequency tunability, they are not practical for RF applications, because the BPF cannot be operated at RF frequencies, and the additional active devices increase the noise. The simplest form of a passive BPF with large Q is an LC BPF, which has been popular in many RF applications due to its relatively high Q-factor. However, having an inductor in CMOS process increases the fabrication cost and takes a significant silicon area. Some techniques have been proposed to replace a passive inductor with an active inductor [52], but the circuit behaves as an inductor only under certain conditions and is sensitive to process variations since it relies on a transconductance, plus the additional power consumption. Power supply noise sensitivity is also a design concern in oscillator circuits. There are several approaches on characterizing the effect of power supply noise on phase noise and jitter of LC oscillators and ring oscillators [55, 56, 70, 71]. In oscillators with differential structures, power supply noise effect is usually suppressed as it is seen as common-mode noise. However, due to the asymmetric waveform and the presence of non-linear capacitors, noise spectra around DC or multiples of the oscillation frequency are mixed to the vicinity of the oscillation frequency [55].

4.3. Circuit Implementation of the RC BPF-Based Oscillator

The block diagram in Figure 55 shows the proposed oscillator and a single-ended version of Figure 55 (a) can be implemented using a positive g_m showin in Figure 57. However, this is not suitable for a high frequency operation due to a parasitic pole of a current mirror.

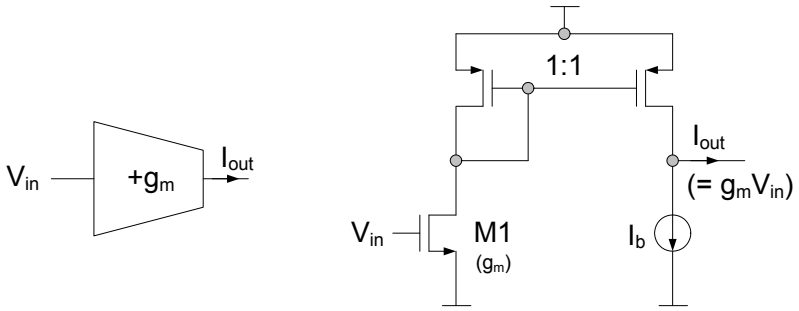


Figure 57. Implementation of a single-ended positive gm.

As shown in Figure 55 (b), a fully differential oscillator can be implemented using a cross-coupled transistor pair and Figure 58 depicts a transistor-level schematic of this proposed oscillator. R_1, R_2, C_1 and C_2 form a BPF, and transistors *MN* and *MP* take the voltage at the output of the BPF (V_{BPF}^{+} and V_{BPF}^{-}) and transform these voltages to currents which are fed back to the BPF. For positive feedback, a fully differential circuit is used. The oscillator output is taken from V_{out}^{+} and V_{out}^{-} as they have larger amplitude than the BPF output (V_{BPF}^{+} and V_{BPF}^{-}).

$$H_1(s) = \frac{V_{BPF}^{+} - V_{BPF}^{-}}{V_{out}^{+} - V_{out}^{-}}(s) = \frac{s}{s + \frac{1}{R_2 C_2}} \tag{4-25}$$

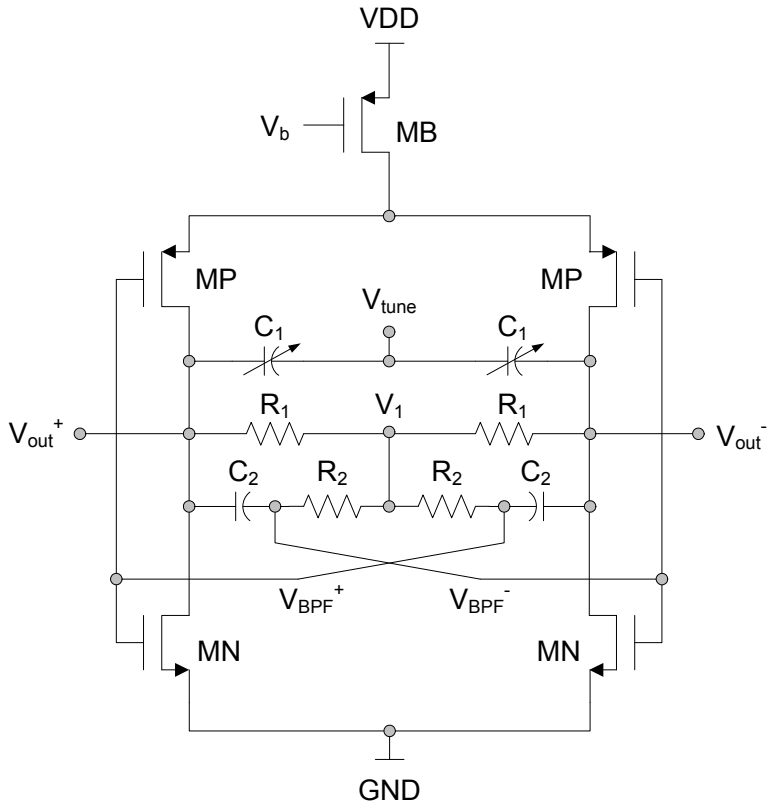


Figure 58. Schematic of the proposed fully differential RC BPF-based oscillator.

Figure 59 plots a magnitude of H_1 when R_2 = 300 Ω and C_2 = 190 fFlocating a pole at 2.8 GHz. At this frequency, $|H_1(s)|$ is -3 dB.

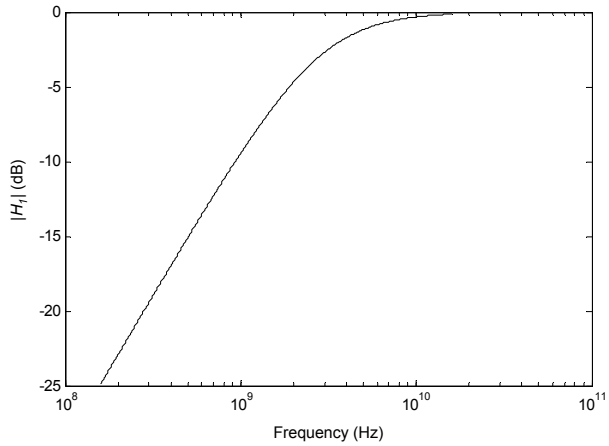


Figure 59. Magnitude plot of H_1(s) in (4-25).

Transistor *MB* is used to bias *MN* and *MP* and also provides a shielding effect from power supply noise. Only PMOS *MB* is used for a current source due to its low flicker noise property. A low power supply voltage limits the use of both NMOS and PMOS current source. The common-mode voltage of V_{out}^{+} and V_{out}^{-} (V_1) is sensed by R_1, and is used to bias the gate voltages of *MN* and *MP* through R_2. Once g_m of *MN* and *MP* are set larger than the minimum requirement given by (4-18), then the oscillation starts and the oscillation frequency is fixed at ω_0 as described in (4-18). When the oscillation is in steady-state, an effective g_m is very non-linear due to non-linear saturation and is different from g_m at the operating point. Recall that g_m acts both as a linear element as well as a limiter (non-linear) element to set the poles on the $j\omega$ axis. Also, the process variation affects the actual g_m and might set the poles in the LHP, thus a good approach could be to set $g_m = g_{m,min} + \Delta g_m$, where Δg_m value can be based on the worst case process variations. In this design, g_m at the operating point is set to 3 times higher than the minimum required g_m.

The oscillation frequency deviates from the ideal value due to parasitic effects. First, parasitic capacitances (C_{DB} of *MN* and *MP*) and the finite output resistance (R_{out} of *MN* and *MP*) at V_{out}^{+} and V_{out}^{-} should be considered. Fortunately, they do not generate additional poles or zeros and can be absorbed by C_1 and R_1, respectively. Also, since the outputs are taken from these nodes, the input capacitance of a buffer or any circuit connected to these nodes should be included when calculating parasitic capacitances.

The second parasitic effect is the input capacitance (C_{gs}) of *MN* and *MP*, which are effectively in parallel with R_2, because V_1 is a virtual ac ground. If a parasitic capacitance C_p is included as shown in Figure 60, (4-16) becomes

$$H'(s) = \frac{\frac{1}{C_1 k_p} s}{s^2 + \frac{1 + R_2/R_1 + (C_1/C_2)(1 + C_p/C_1)}{R_2 C_1 k_p} s + \frac{1}{R_1 C_1 R_2 C_2 k_p}} \tag{4-26}$$

where $k_p = 1+(C_p/C_1)(1+C_1/C_2)$ and C_p represents all parasitic capacitances connected to the BPF output. From (4-26), the oscillating frequency, Q-factor and $g_{m,min}$ become

$$\omega_0{}'^2 = \frac{1}{R_1 C_1 R_2 C_2 \left(1+\left(C_p/C_1\right)\left(1+C_1/C_2\right)\right)}$$
$$g_{m,\min}{}' = \frac{1+R_2/R_1+\left(C_1/C_2\right)\left(1+C_p/C_1\right)}{R_2} \qquad (4\text{-}27)$$
$$Q' = \frac{\sqrt{\left(C_1/C_2\right)\cdot\left(R_2/R_1\right)}}{1+R_2/R_1+\left(C_1/C_2\right)\left(1+C_p/C_1\right)} \times \sqrt{1+\left(C_p/C_1\right)\left(1+C_1/C_2\right)}$$

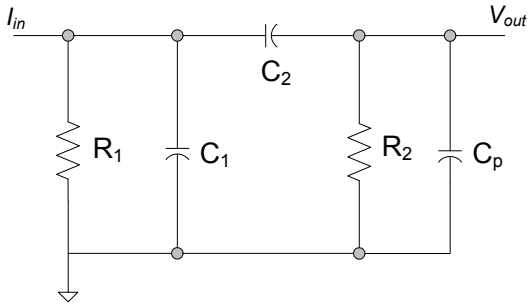
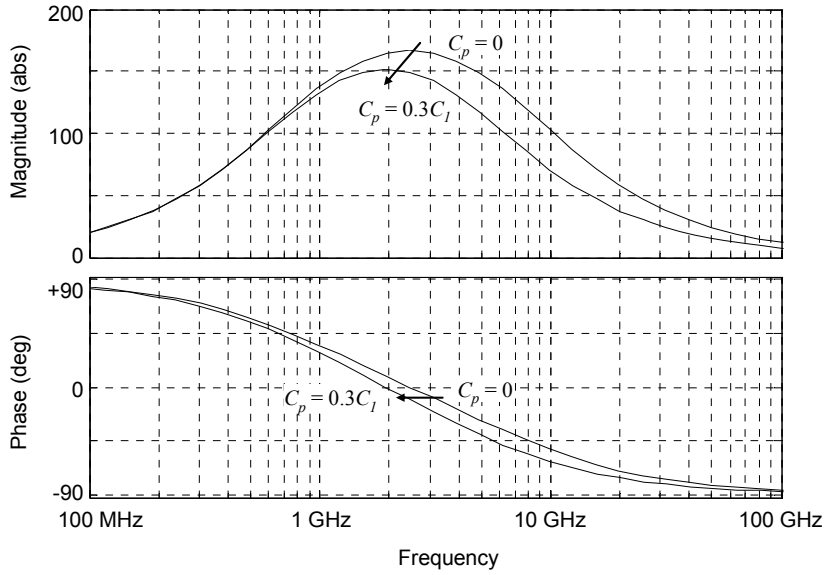
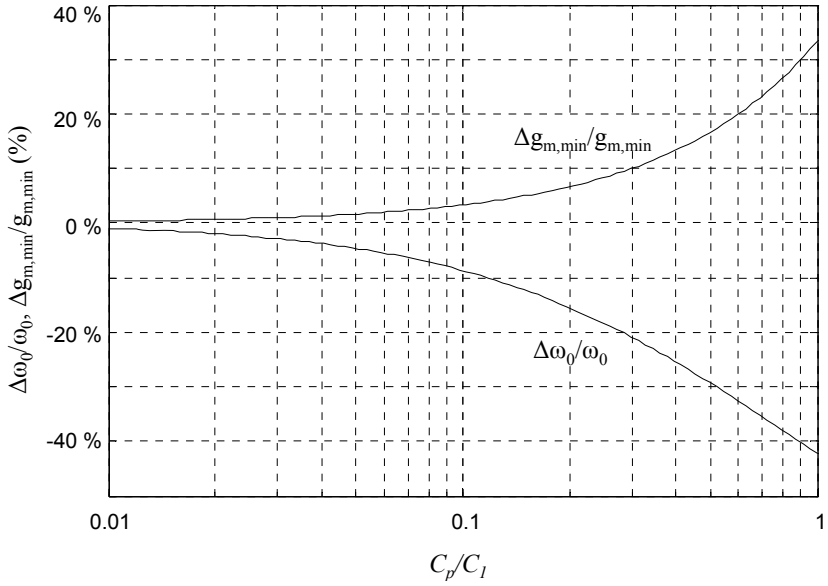


Figure 60. RC BPF with a parasitic capacitance C_p.

Note that C_p does not introduce additional poles or zeros i.e. (4-26) still has the same biquadratic form as (4-16). Equation (4-26) suggests that if $C_p/C_1 << 1$ and $C_p/C_2 << 1$, then the effect of C_p can be ignored. C_p is proportional to the size of *MN* and *MP* and, as $g_{m,min}$ and ω_0 are increased, C_p is increased and C_1 should be decreased, hence, C_p/C_1 cannot be ignored anymore. To evaluate the deviation of ω_0 and $g_{m,min}$, suppose that a BPF is designed with $R_1 = R_2 = 300\ \Omega$ and $C_1 = C_2 = 210$ fF so that ω_0 is normally 2.5 GHz. Figure 61 (a) depicts the deviation of the transfer function when $C_p = 63$ fF (30 % of C_1) is introduced. Center frequency ω_0 moves 20 % (from 2.45 GHz to 1.94 GHz) and $g_{m,min}$ increases 10 % (from 6 mA/V to 6.6 mA/V).



(a)



(b)

Figure 61. BPF performance deviation due to Cp (a) Transfer function (b) ω_0 and $\Delta g_{m,min}$.

In Figure 61 (b) plots the changes in ω_0 and $g_{m,min}$ as C_p/C_1 varies from 1 % to 100 %. When C_p/C_1 = 10 %, ω_0 and $g_{m,min}$ change by 8 % and 4 %, respectively. As shown in

Figure 61 (b), the relationship of ω_0 and $g_{m,min}$ to C_p/C_1 is monotonic, and performance deviations are less than 1 % when C_p/C_1 = 1%.

In actual design, C_p is related to transistor sizes. In this work, C_p was measured as 40 fF. Given C_p as 40 fF and assuming $R_1 = R_2$ = 300 Ω and both capacitors are same ($C_1 = C_2 = C$), a required C for 2.5 GHz of an oscillating frequency is calculated using (4-27).

$$\left(2\pi \times 2.5 \times 10^{9}\right)^2 = \frac{1}{300^2 C^2 \left(1 + 2 \times \left(40 \times 10^{-15}/C\right)\right)} \tag{4-28}$$

Solving (4-28) yields C = 176 fF that is quite practical to accurately implement in this process. Note that if C_p is not considered, the required C for 2.5 GHz is 212 fF.

4.3.1. A Design Optimization for the Minimal Noise and Power Consumption

The objective of the section is to describe an optimal design of resistors and capacitors of the band pass filter in terms of the minimum noise and power consumption. Consider a linearized, open-loop model of the proposed oscillator shown in Figure 62.

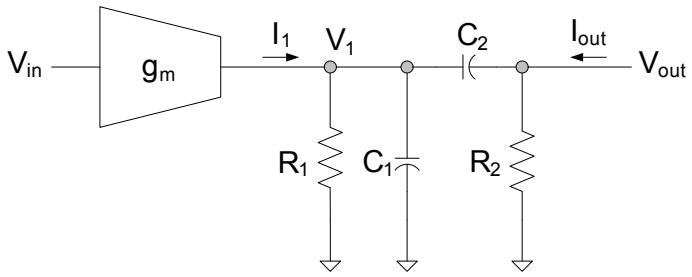


Figure 62. Block diagram of the linearized open-loop model of the proposed oscillator.

The key design parameters are resistor and capacitor ratios:

$$k_R = \frac{R}{R_1} = \frac{R_2}{R}, \quad k_C = \frac{C_1}{C} = \frac{C}{C_2} \tag{4-29}$$

where R and C are design variables determined by the oscillation frequency. Note that, once R and C are fixed, the oscillation frequency is not changed by varying k_R and k_C. Hence, the open-loop transfer function is given by

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{k_C C} s}{s^2 + \frac{1 + k_R{}^2 + k_C{}^2}{k_R k_C RC} s + \left(\frac{1}{RC}\right)^2} \tag{4-30}$$

From (4-30), the oscillation frequency (ω_0), a Q-factor (Q) and the minimum required g_m ($g_{m,min}$) are calculated as

$$\omega_0 = \frac{1}{RC}, \quad Q = \frac{k_R k_C}{1 + k_R{}^2 + k_C{}^2}, \quad g_{m,\min} = \frac{1 + k_R{}^2 + k_C{}^2}{k_R R} \tag{4-31}$$

Note that ω_0 is determined by only R and C, not by k_R and k_C. In Figure 62, a current injected to node V_{out} (I_{out}) can be referred to the current injected to node V_1 (I_1) at ω_0 with a following transfer function.

$$\left| \frac{I_1}{I_{out}} (j\omega_0) \right|^2 = \left(1 + k_C{}^2\right)^2 + \left(k_R k_C\right)^2 \tag{4-32}$$

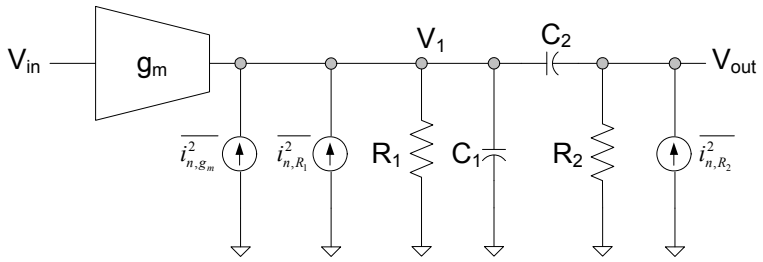


Figure 63. Individual noise current source in Figure 62.

Figure 63 shows various noise current sources. $\overline{I_{n,R_2}{}^2}$ is injected to the V_{out} node while $\overline{I_{n,R_1}{}^2}$ and $\overline{I_{n,g_m}{}^2}$ are injected to the V_1 node, and using (4-32), $\overline{I_{n,R_2}{}^2}$ associated with R_2 can be referred to the V_1 node. Assuming $g_m = g_{m,min}$, the total output noise current at the V_1 node is,

$$\begin{aligned}\overline{I_{1,total}{}^2} &= \frac{4kT}{R_1} + 4kT\gamma g_m + \frac{4kT}{R_2}\left(\left(1+k_C{}^2\right)^2 + \left(k_R k_C\right)^2\right) \\ &= \frac{4kT}{R}\left(1+k_C{}^2+\gamma\right)\left(k_R + \frac{1+k_C{}^2}{k_R}\right)\end{aligned} \tag{4-33}$$

where γ is the factor to be 2/3 for long-channel transistors and larger value for a short-channel transistors. A total input-referred noise voltage can be calculated from (4-31) and (4-33),

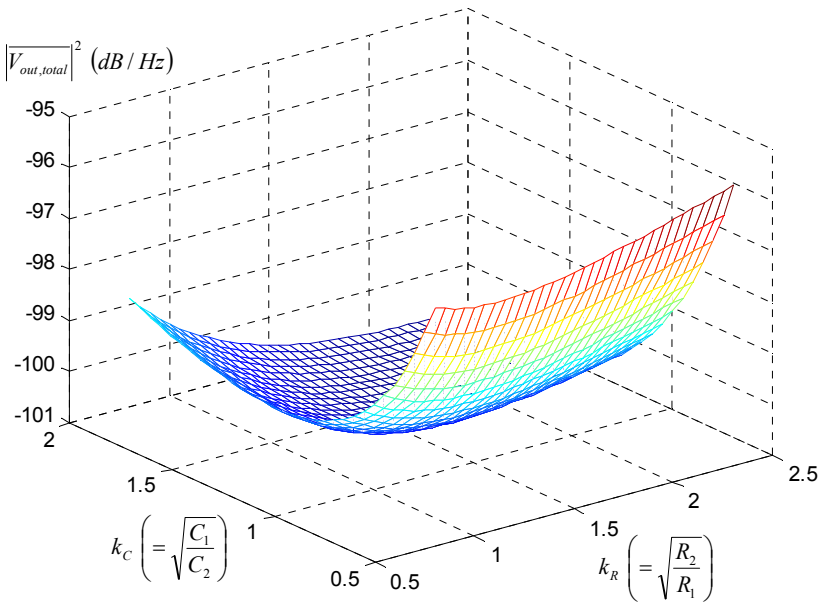
$$\overline{V_{in,total}{}^2} = \frac{\overline{I_{1,total}{}^2}}{g_{m,\min}{}^2} = \frac{4kTRk_R{}^2}{\left(1+k_R{}^2+k_C{}^2\right)^2}\left(1+k_C{}^2+\gamma\right)\left(k_R + \frac{1+k_C{}^2}{k_R}\right) \tag{4-34}$$

A noise shaping function in the linearized VCO model at frequencies close to ω_0 is determined in [4] and derived in (4-11),

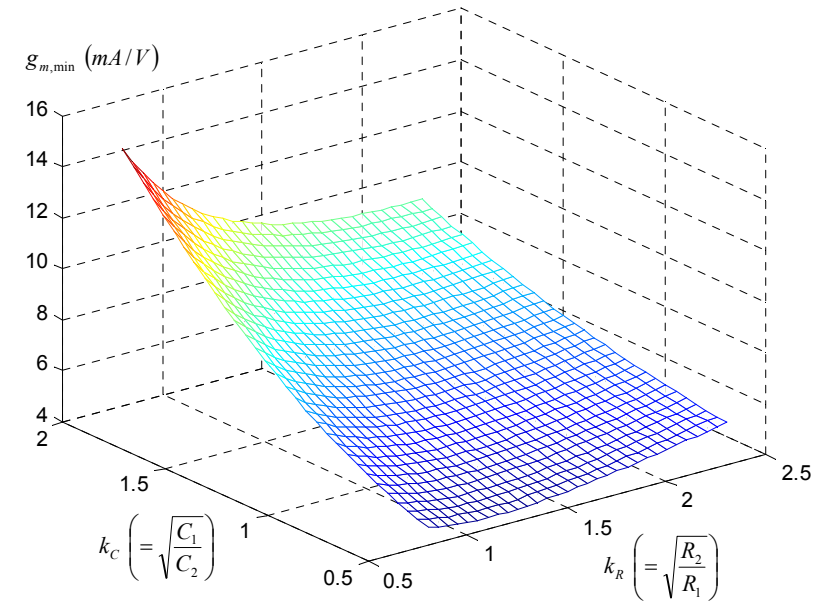
$$\left|\frac{V_{out}}{V_{in}}\left[j\left(\omega_0+\Delta\omega\right)\right]\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4-35}$$

Hence, the total output noise voltage can be calculated using (4-31), (4-34) and Q equation in (4-35),

$$\left|\overline{V_{out,total}}\left[j\left(\omega_0+\Delta\omega\right)\right]\right|^2 = \frac{kTR}{k_C{}^2}\left(1+k_C{}^2+\gamma\right)\left(k_R + \frac{1+k_C{}^2}{k_R}\right)\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4-36}$$



(a)



(b)

Figure 64. VCO performance versus k_R and k_C. (a) Total output noise voltage. (b) $g_{m,min}$.

Figure 64 shows 3-d plots of a total output noise voltage and $g_{m,min}$ in (4-31) when k_R and k_C are varied. It should be mentioned that both $g_{m,min}$ and (4-36) reach to their minimum values with a following condition.

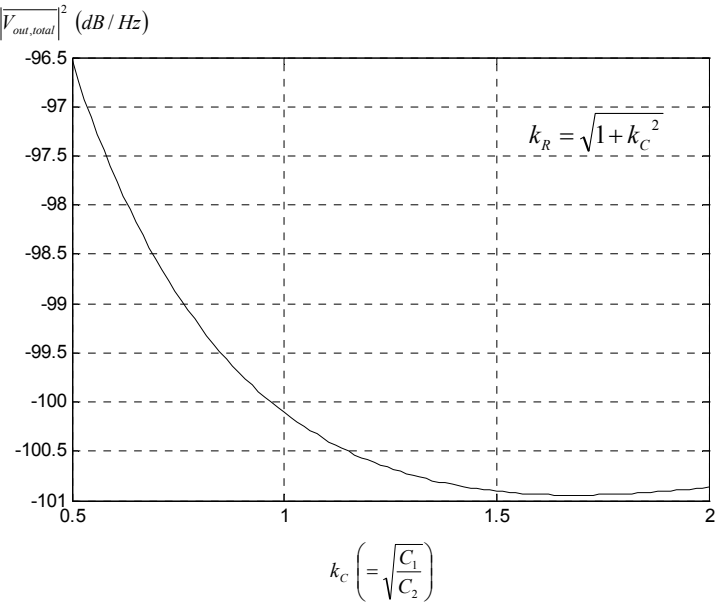
$$k_R^{\,2} = 1 + k_C^{\,2} \tag{4-37}$$

Applying (4-37) to (4-36) and (4-31) simplifies them to one-variable equations (k_C) as,

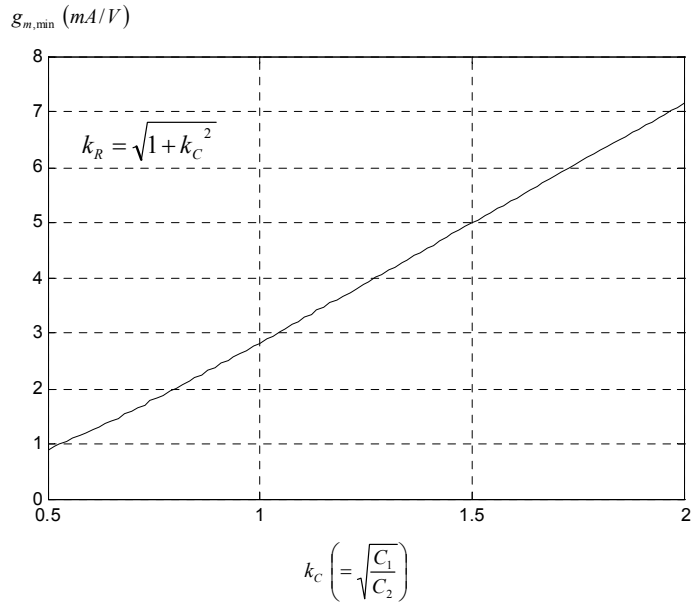
$$\begin{aligned} \left|\overline{V_{out,total}}\left[j(\omega_0 + \Delta\omega)\right]\right|^2 &= \frac{kTR}{k_C^{\,2}}\left(1 + k_C^{\,2} + \gamma\left(2\sqrt{1 + k_C^{\,2}}\right)\left(\frac{\omega_0}{\Delta\omega}\right)^2\right. \\ g_{m,\min} &= \frac{2k_C^{\,2}}{R\sqrt{1 + k_C^{\,2}}} \end{aligned} \tag{4-38}$$

(4-38) represent a total output noise voltage and $g_{m,min}$ optimized for k_R and they are functions of only k_C.

Figure 65 depicts (4-38) versus k_C. From (4-37) and (4-38), a total output noise voltage becomes minimal when k_C = 1.68 and k_R = 1.96 and, is rapidly increased when k_C is less than 1. Meanwhile, $g_{m,min}$ is monotonically increased as k_C is increased. Therefore, a design trade-off can be made and, the optimal design can considered as k_C = 1 and $k_R = \sqrt{2}$ implying C_1=C_2 and R_2=$2R_1$.



(a)



(b)

Figure 65. VCO performance versus k_C when k_R is optimized. (a) Total output noise voltage. (b) $g_{m,min}$.

A design optimization has been performed to achieve minimal noise and power consumption. The optimal ratio of resistors and capacitors has been derived as $R_2/R_1 = C_1/C_2 + 1$. When this condition is met, the design trade-off between a total output noise voltage ($|V_{out}|^2$) and $g_{m,min}$ can be made by adjusting a capacitor ratio, k_C ($=\sqrt{C_1/C_2}$). $|V_{out}|^2$ rapidly increases when $k_C < 1$, while $g_{m,min}$ monotonically increases as k_C is increased. Although the optimal condition, $R_2/R_1 = C_1/C_2 + 1$, indicates the optimal design for ideal components with $C_p = 0$, the actual ratio will be significantly different to account for nonzero C_p.

4.3.2. Power Supply Noise Sensitivity

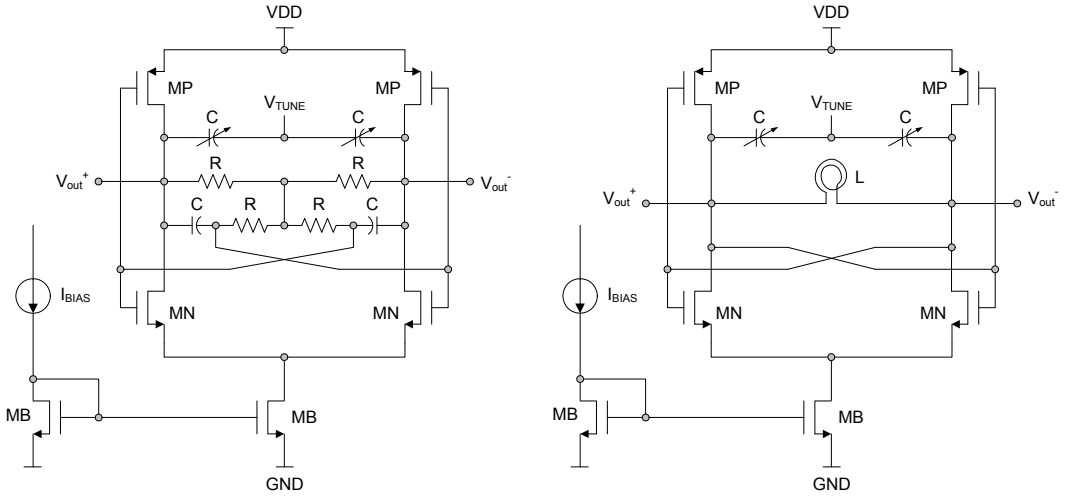
The power-supply-induced phase noise, under the assumption of a narrowband frequency modulation and assuming a noise source of $V_n\cos(\omega_n)$ exists on the power supply, is given by

$$L\{\omega_n\} = 10\log\left[\frac{1}{4}\left(\frac{K_{VDD}V_n}{\omega_n}\right)^2\right] \tag{4-39}$$

where K_{VDD} is the power supply frequency pushing factor defined as $\Delta\omega / \Delta V$ (rad/V), and V_n and ω_n are the amplitude and frequency of a noise signal on the power supply, respectively. Note that K_{VDD} is frequency dependent, and its frequency behavior depends on the regulating circuit providing the oscillator V_{DD}. However, K_{VDD} at dc is a good

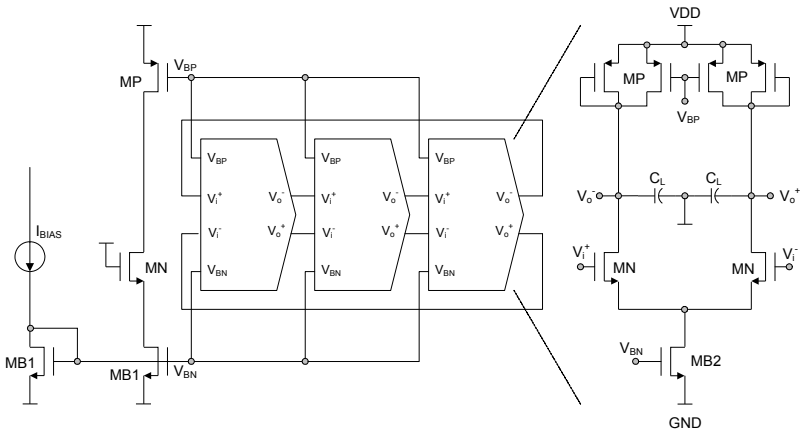
indication of the power supply noise sensitivity, allowing for simpler comparison among oscillator architectures.

It is difficult to precisely control and measure ripples on the power supply due to decoupling capacitors and parasitic bond wire inductance. Hence, simulations are used to compare the supply noise sensitivity of the proposed oscillator with a ring oscillator as well as an LC oscillator.

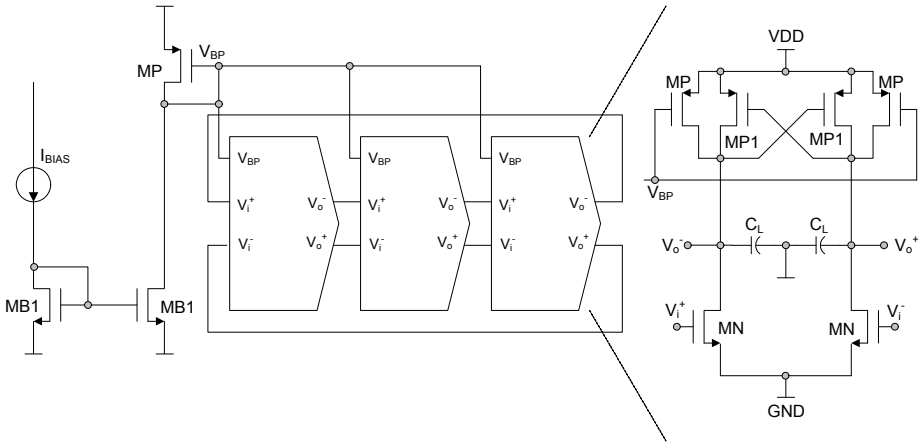


(a) (b)

Figure 66. Oscillators for power supply noise sensitivity comparison. (a) RC BPF-based oscillator. (b) LC oscillator. (c) Ring oscillator1. (d) Ring oscillator2 [72].



(c)



(d)

Figure 66. Continued.

All oscillators shown in Figure 66 are designed to operate at 1 GHz. An LC oscillator in Figure 66 (b) is identical to the proposed oscillator in Figure 66 (a) except that a passive RC-BPF is replaced with an LC-tank. The same NMOS current bias circuit,

MB in Figure 66 (a) and (b), and MB1 and MB2 in Figure 66 (c) and (d), is used to be consistent with each other. For a control voltage of varactors (V_{tune}) in Figure 66 (a) and (b), an ideal voltage source referred to ground is used in the simulation. We designed three-stage, differential ring oscillators using a Maneatis delay cell [73] as depicted in Figure 66 (c) and a Lee-Kim delay cell [72] as shown in Figure 66 (d). V_{DD} (nominally 1.3 V) is swept from 1.2 V to 1.4 V.

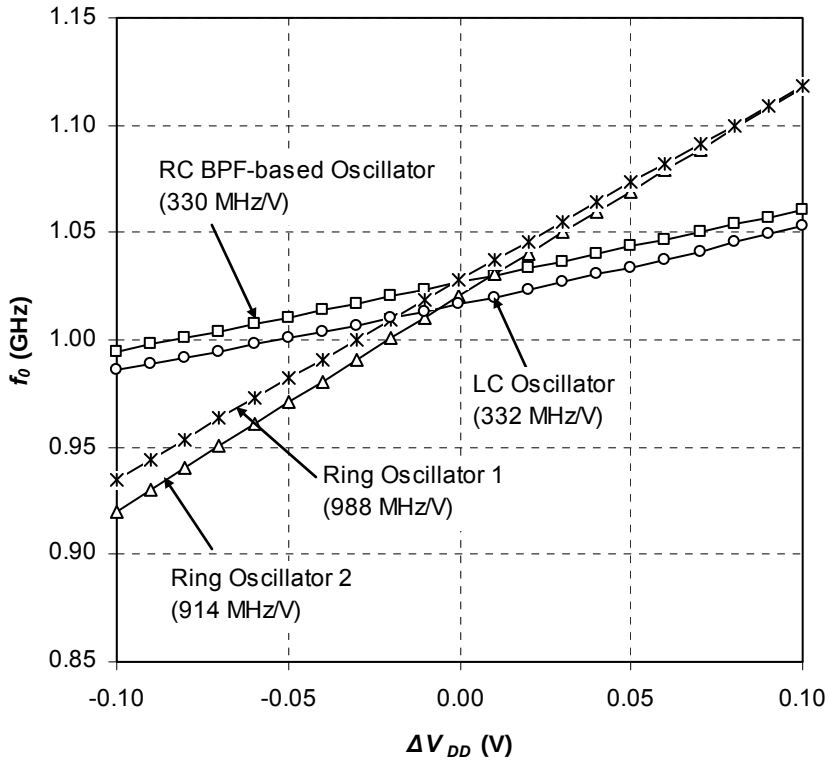


Figure 67. Oscillation frequency sensitivity over power supply voltage perturbation.

K_{VDD} is measured as 988 MHz/V and 914 MHz/V from two ring oscillators while the proposed oscillator and an LC oscillator exhibit 330 MHz/V and 334 MHz/V respectively, as shown in Figure 67. Applying this result to (4-39), the power supply noise sensitivity of the proposed oscillator improves 9.5 dB and 8.8 dB over each ring oscillators.

The proposed oscillator could have wider ω_0 tuning range than an LC oscillator. This is because that, in the proposed oscillator, both R and C can be adjusted, while in an LC oscillator, typically only the C can be tuned. Switched L using a multi-tapped inductor can be used to extend the tuning range of an LC oscillator, but is less practical because it requires a non-standard device.

4.4. Experimental Results

The proposed RC BPF-based oscillator was designed and implemented. The chip was fabricated in 8-metal double-poly UMC 0.13 μm technology through the UMC university program. The designed values of resistors and capacitors are listed in Table 3.

N-type poly resistors are used for R_1 and R_2, and Metal-Insulation-Metal (MIM) capacitor for C_2. C_1 is built with a MOS-type varactor for frequency tuning purposes. In addition, C_1 is decomposed to two different sizes of varactors for the tuning flexibility. The oscillator is designed to have a center frequency of f_0 = 2.5 GHz and the Q-factor of BPF is designed to be 0.33. R_1 and R_2 are drawn with a interleaved layout to decrease

process variation effect and improve the matching. C_1 is designed less than C_2 to account parasitic capacitances connected to the output node.

Table 3. Resistors and capacitors in Figure 58.

	Value	*W / L*	*Type*
R_1, R_2	300 Ω	(2 × 2 μm) / 10 μm	N-type poly
C_1	50 *fF* (Fine tuning) 70 *fF* (Coarse tuning)	24 μm / 0.18 μm 24 μm / 0.25 μm	MOS-type varactor
C_2	190 *fF*	11 μm / 11 μm	MIM capacitor

In addition, all transistors are built on a separated well using guard rings to improve the isolation from the common substrate noise. An open-drain buffer was designed to drive the external RF balun on the printed-circuit-board (PCB) to convert the differential signal to a single-ended signal. The unbalanced port of the balun is 50 Ω to match the spectrum analyzer.

The microphotograph of the fabricated chip is shown in Figure 68. The silicon area is 0.006 mm^2 and the power consumption of the proposed oscillator is 2.8 mW from a V_{DD} of 1.3 V.

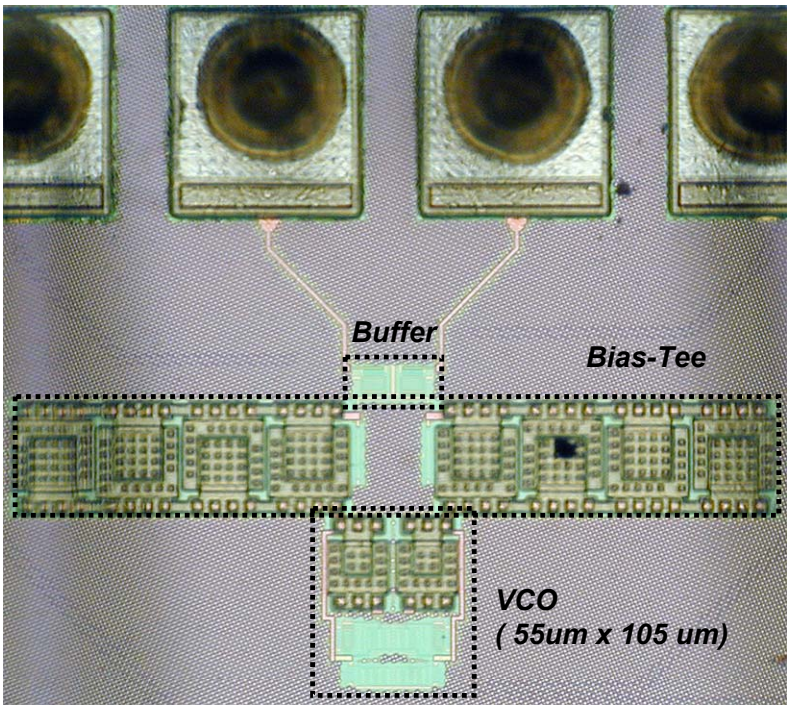


Figure 68. Chip micro photograph.

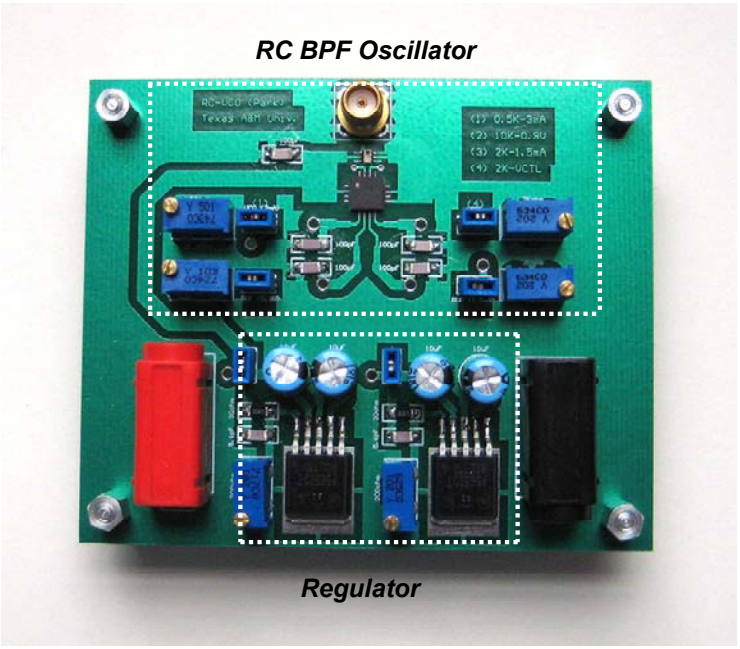


Figure 69. PCB for RC BPF-based oscillator testing.

The designed circuit is encapsulated using QFN-16 open cavity package. It has 16 pins and a lead pitch is 0.65 mm and, a body size is 5 mm x 5 mm. QFN package is preferred in many RF applications due to small parasitic effects. It has pins at the bottom side of a package instead of exposed leads, hence the parasitics related to the leads can be minimized.

QFN is used for the applications up to several GHz. Also, QFN provides a ground paddle that is a big metal plane under the chip. A ground paddle has the minimum impedance seen from the inside circuit since it can be connected with shorter and multiple bonding wires. Due to the big foot print, a ground paddle can operate with a high power environment. The printed circuit board (PCB) was designed and fabricated for the measurement of the chip. The picture of PCB is shown in Figure 69. It includes a voltage regulator block with NCP565 linear regulator chip that provides a lower output voltage than a conventional LM317 regulator chip. Minimum output voltage of NCP565 is 0.9V while a conventional LM317 can generate minimum voltage of 1.25 V. Its output voltage can be adjusted down to 0.9 V which is low enough for several low-voltage circuits. A 4-pin switch is used for discrete tunings and potential metes are used for a continuous fine tuning as well as biasing current source. An RF balun (HHM1520) is used to convert the differential output signals to a single-ended signal that drives a 50 Ω spectrum analyzer. SMA connector is used for a connection with RF cables and is placed with the minimum distance from a balun to minimize any couplings effect and parasitics. In close to RF signal path, a ground plane is not placed to improve a shielding.

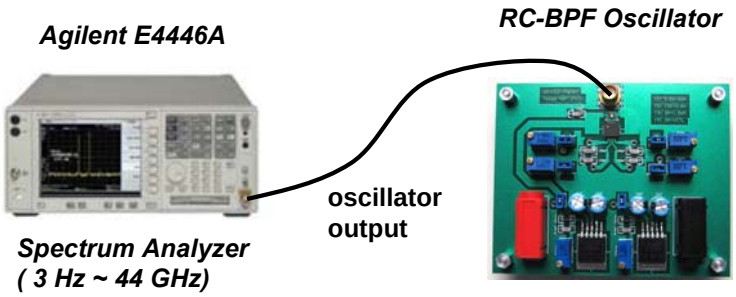
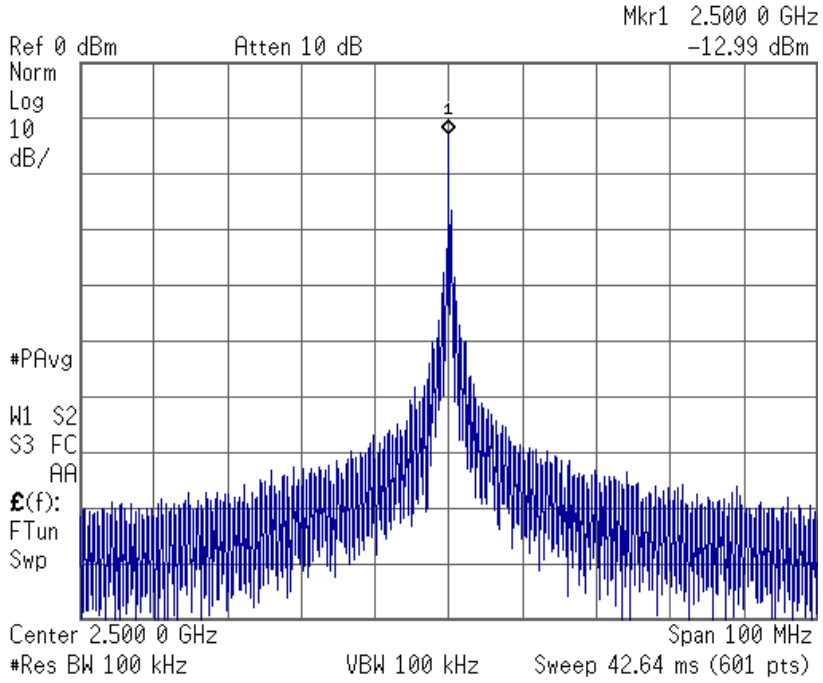


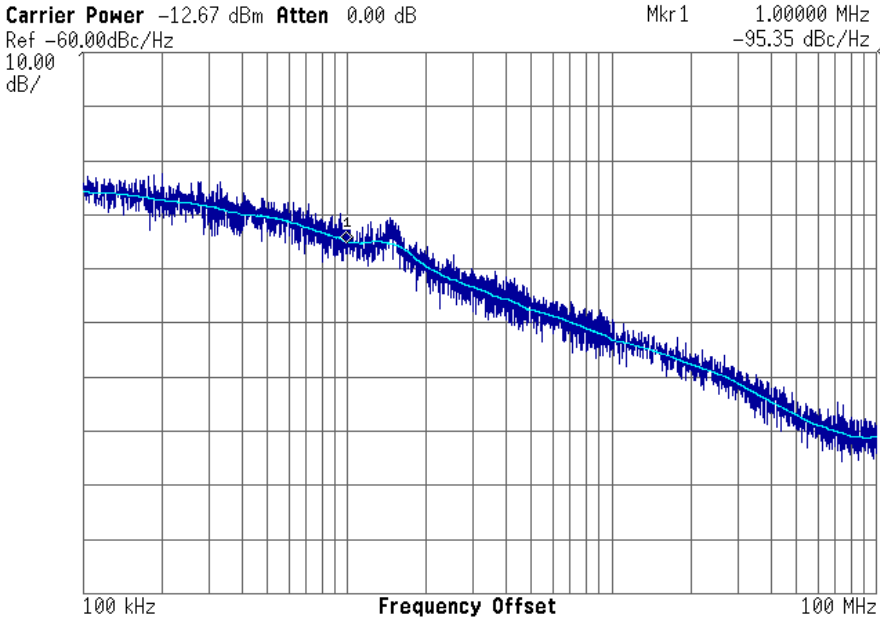
Figure 70. Test set-up for measurement.

Figure 70 shows the test set-up for the measurement of oscillating tones and phase noise. Agilent E4446A spectrum analyzer which can be used up to 44 GHz is used. The frequency spectrum and phase noise measured at 2.5 GHz using the test set-up as shown in Figure 70, are shown in Figure 71. At 1 MHz offset frequency, -95.4 dBc/Hz of phase noise was measured.

A measured frequency tuning result is shown in Figure 72. The oscillation frequency is tuned by adjusting C_1 in Figure 72. Since C_1 was decomposed by two different sized MOS-type varactors, a family of tuning curves can be achieved. In Figure 72, V_{tune} is a fine tuning voltage of C_1 and V_{tune2} is a coarse tuning voltage of C_1. A covered frequency was measured from 2.25 GHz to 2.75 GHz. K_{VCO} was measured as 308 MHz/V, and is calculated from the slope measured at the linear region of the curve (V_{tune} = 0.6 V).



(a)



(b)

Figure 71. Measured results (a) Frequency spectrum at 2.5 GHz (b) Phase noise spectrum.

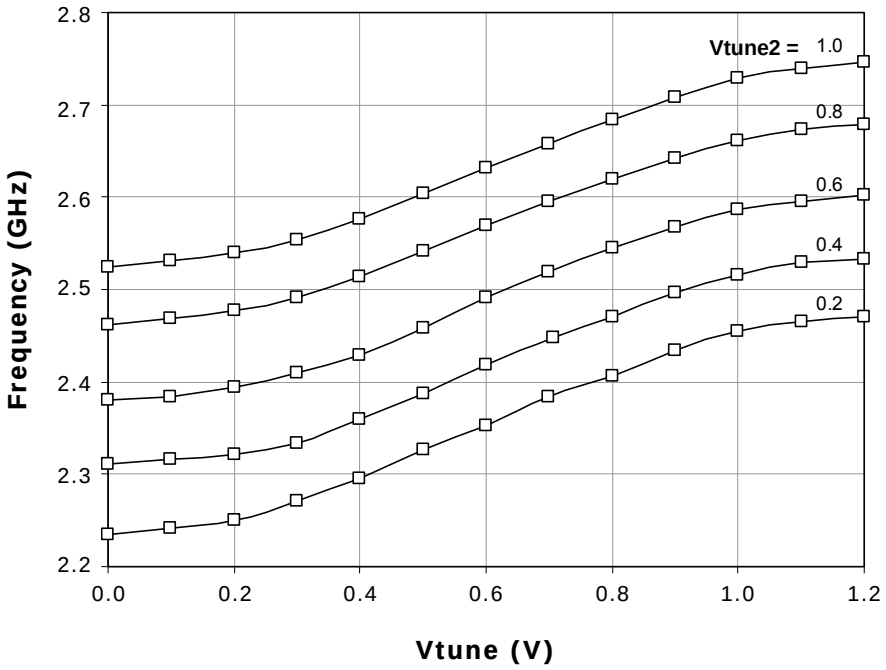


Figure 72. Measured frequency tuning result.

Table 4 compares the performance of the proposed oscillator with other published solutions running at frequency around 2.5 GHz. A normalized phase noise has been typically defined as a figure of merit (FOM) for oscillators:

$$FOM = \frac{1}{PN(\omega_m)P_{VCO,mW}}\left(\frac{\omega_{OSC}}{\omega_m}\right)^2 \tag{4-40}$$

where $P_{VCO,mW}$ is the total VCO power consumption in mW and ω_m is the offset frequency where a phase noise was measured. The proposed oscillator shows good phase

noise and small power consumption resulting in a FOM of -159 dB, better than the previously reported oscillators in Table 4.

Table 4. Performance summary and comparison with other published solutions.

	This Work	[52]	[74]	[75]	[76]
Frequency (GHz)	2.5	2.5	2.4	1.6	2.45
Power (mW)	2.86	10	15	33	19.20
Phase noise @ 1 MHz offset (dBc/Hz)	-95.4	-80	-97	-102	-96
Type	RC BPF	2-stg. Ring	3-stg. Ring	2-stg. Ring	2-stg. Ring
Process	0.13 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.12 μm CMOS	0.28 μm CMOS
FOM* (dB)	-159	-124	-153	-151	-151

* FOM is defined as (4-40) [77].

4.5. Additional Works and Future Research

4.5.1. Quadrature Generation

In addition to a differential signal, a quadrature signal is widely used in most of modern communication standards. In case that phase or frequency modulation schemes

are used, a quadrature mixing is required to extract the information contained in both sides of spectra [78]. It can be also used in “half-rate” clock recovery circuits as well as in frequency detectors for random data [2].

A quadrature signal consists of 4 signals having a phase difference of 90º. A ring oscillator can easily generate a quadrature signal if a number of stages is multiple of 4 (in single-ended version) or of 2 (in differential version) as each outputs are equally spaced. However, this is not the case of BPF-based oscillator since they yield zero phase-shift between inputs and outputs.

A passive poly-phase network conformed of integrated resistors and capacitors can be used for a quadrature signal. This technique effectively generates a quadrature signal from a differential signal, and higher order of the phase shift network yields more accurate 90º shift. A drawback of this technique is that there is the insertion loss of -3 dB per stage and a signal is more attenuated as the number of stage is increased. Another technique for quadrature signal generation is the use of a VCO running at twice the desired frequency and a divide-by-2 circuit using flip-flops. The accuracy of 90º phase is normally known as good but is affected by the matching of the flip-flops in the frequency divider and the duty cycle error of the VCO output [79]. Also, since a VCO and the frequency divider should operate in high frequency, power consumption is increased.

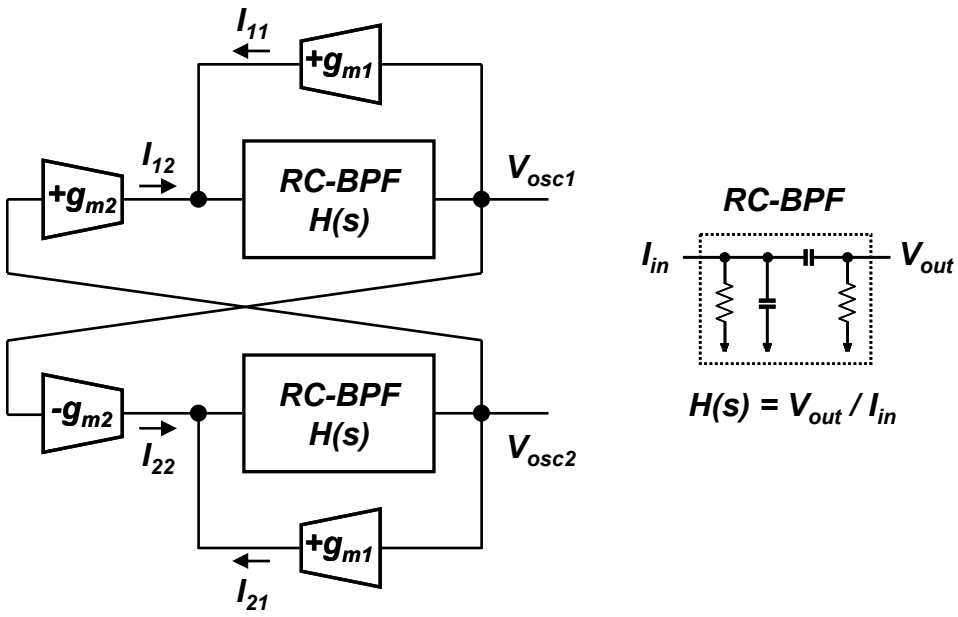


Figure 73. Antiphase coupling of two RC-BPF oscillators.

A coupling technique is also common for a quadrature signal generation in BPF-based oscillators. Figure 73 depicts the antiphase coupled RC-BPF oscillators. Each oscillator comprised of RC-BPF with a positive feedback through "$+g_{m1}$". *H(s)* is an impedance transfer function of BPF. V_{osc1} and V_{osc2} are the output voltages of each oscillator. g_{m2} is a coupling transconductance and one of them has a negative gain resulting in antiphase coupling.

To understand the operation, a linear analysis can be performed as

$$\begin{aligned} V_{osc1} &= H(s)g_{m1}V_{osc1} + H(s)g_{m2}V_{osc2} \\ V_{osc2} &= H(s)g_{m1}V_{osc2} - H(s)g_{m2}V_{osc1} \end{aligned} \tag{4-41}$$

Rewriting (4-41) yields

$$\begin{aligned}(1-H(s)g_{m1})V_{osc1} &= H(s)g_{m2}V_{osc2}\\ (1-H(s)g_{m1})V_{osc2} &= -H(s)g_{m2}V_{osc1}\end{aligned} \tag{4-42}$$

Assuming V_{osc1}, $V_{osc2} \neq 0$, and dividing upper equation by lower one of (4-42), we arrive at $V_{osc1}^2 + V_{osc2}^2 = 0$, hence $V_{osc1} = \pm jV_{osc2}$, confirming the phase difference between V_{osc1} and V_{osc2} is ±90º.

In Figure 73, to maintain oscillation, V_{osc1} is aligned with I_{11}, and V_{osc2} and I_{21} have a zero phase shift. This can be done if new oscillating frequency ω_{osc} deviates from the previous oscillating frequency ω_0 such that a phase of H(s) at ω_{osc} cancels the phase of a total input current. Considering only upper part of Figure 72, a total input current of a RC-BPF is $I_{11}+I_{12} = (g_{m1}+jg_{m2})V_{osc1}$, and $V_{osc1} = H(s)(g_{m1}+jg_{m2})V_{osc1}$. Phase of $H(s)$ at ω_{osc} becomes

$$\angle H(j\omega_{osc}) = -\tan^{-1}\left(\frac{g_{m2}}{g_{m1}}\right) = -\tan^{-1}(k_g) = -\theta \tag{4-43}$$

where $k_g = g_{m2}/g_{m1}$ is a coupling factor and θ is a deviation angle. $H(s)$ can be generalized by a second-order BPF using (4-16) as

$$H(s) = \frac{\frac{1}{C_1}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4-44}$$

where ω_0 and Q are defined in (4-18) and (4-19). Applying (4-44) into (4-43) leads

$$90° - \tan^{-1}\left(\frac{(\omega_0 / Q)\omega_{osc}}{{\omega_0}^2 - {\omega_{osc}}^2}\right) = -\tan^{-1}\left(k_g\right) \tag{4-45}$$

Rewriting (4-45) gives

$$\frac{(\omega_0 / Q)\omega_{osc}}{{\omega_0}^2 - {\omega_{osc}}^2} = \tan\left(90° + \tan^{-1}\left(k_g\right)\right) = -\frac{1}{k_g} \tag{4-46}$$

New oscillating frequency ω_{osc} due to antiphase coupling is calculated by solving (4-46) as

$$\frac{\omega_{osc}}{\omega_0} = \frac{k_g}{2Q} + \sqrt{1 + \left(\frac{k_g}{2Q}\right)^2} \tag{4-47}$$

From (4-47), it can be known that ω_{osc} is greater than ω_0 because a phase response of a BPF should be negative as seen at (4-43). (4-47) also indicates that an oscillation frequency of antiphase coupled oscillator can be tuned by adjusting a coupling factor. In addition to a coupling factor, a deviation from the original oscillation frequency is inversely proportional to a Q-factor of a BPF as plotted in Figure 74.

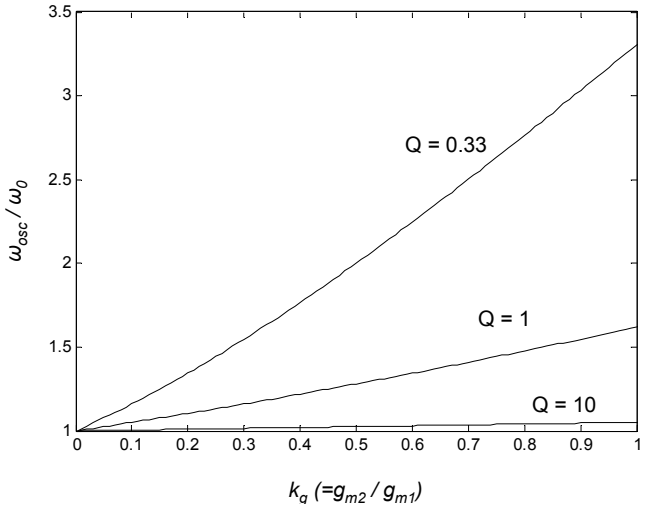
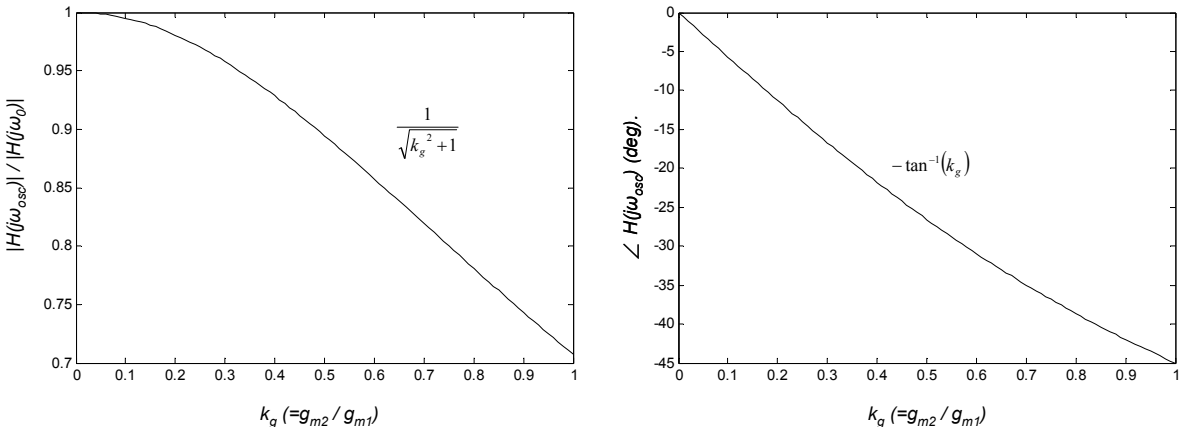


Figure 74. Oscillation frequency deviation versus a coupling factor.

In Figure 70, three different Q-factors are depicted and it can be known that with 25 % of g_{m2}/g_{m1}, $\omega_{osc} = 1.5\omega_0$ when Q = 0.33. However, when Q = 10 that is a similar to a LC oscillator, ω_{osc} does not much deviate from ω_0. As ω_{osc} deviates from ω_0, a carrier power becomes attenuated since a BPF has the maximum magnitude response when a phase response is zero. This limits the frequency tuning range of an antiphase coupled oscillator. A magnitude response at ω_{osc} normalized by the maximum magnitude at ω_0 can be calculated by applying (4-47) into (4-44).

$$\frac{|H(j\omega_{osc})|}{|H(j\omega_0)|} = \frac{\frac{1}{Q}\frac{\omega_{osc}}{\omega_0}}{\sqrt{\left(1-\left(\frac{\omega_{osc}}{\omega_0}\right)^2\right)^2+\left(\frac{1}{Q}\frac{\omega_{osc}}{\omega_0}\right)^2}} = \frac{1}{\sqrt{k_g{}^2+1}} \tag{4-48}$$



(a) (b)

Figure 75. Coupling factor versus (a) Normalized magnitude response. (b) Phase response.

Figure 75 shows a normalized $|H(j\omega_{osc})|$ and a phase response versus a coupling factor. To compare a magnitude and a phase response, an RC-BPF and a LC-BPF are designed with a center frequency of 2.7 GHz approximately, as depicted in Figure 76.

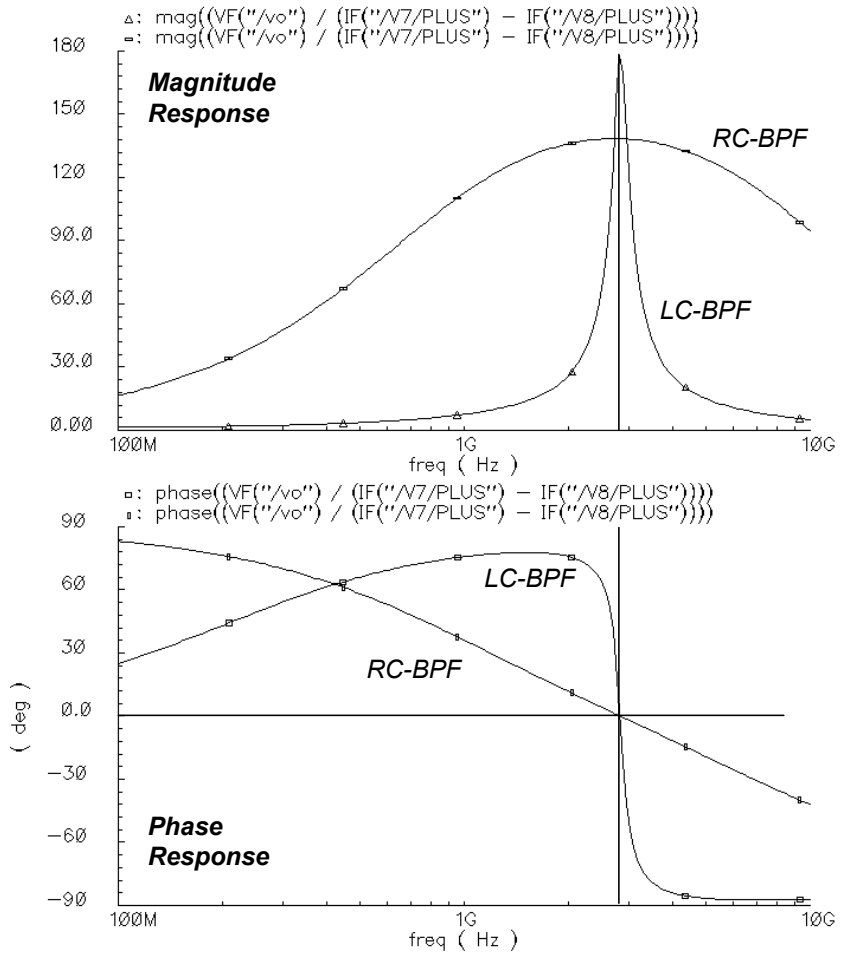
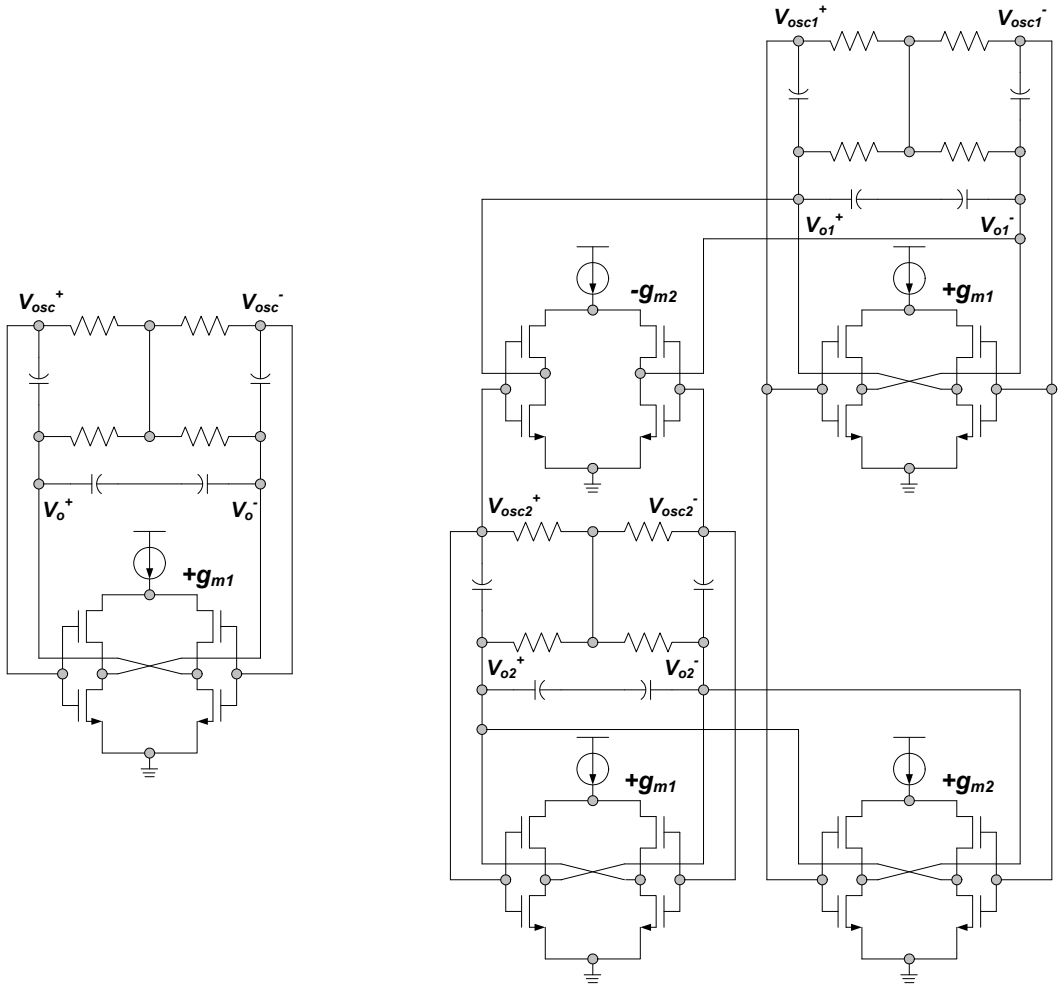


Figure 76. Magnitude and phase response of RC-BPF and LC-BPF.

A Q-factor of each BPF is designed as 0.33 in RC-BPF and 10 in LC-BPF, respectively. Note that a center frequency of each BPF in Figure 76 has set to 2.7 GHz considering that an oscillating frequency will be 2.5 GHz when a feedback is formed due to additional load capacitor. As shown in a phase response plot of Figure 76, a slope of RC-BPF around zero phase crossing point is much lower than that of LC-BPF, which enables wide frequency tuning range when two oscillators are antiphase coupled.

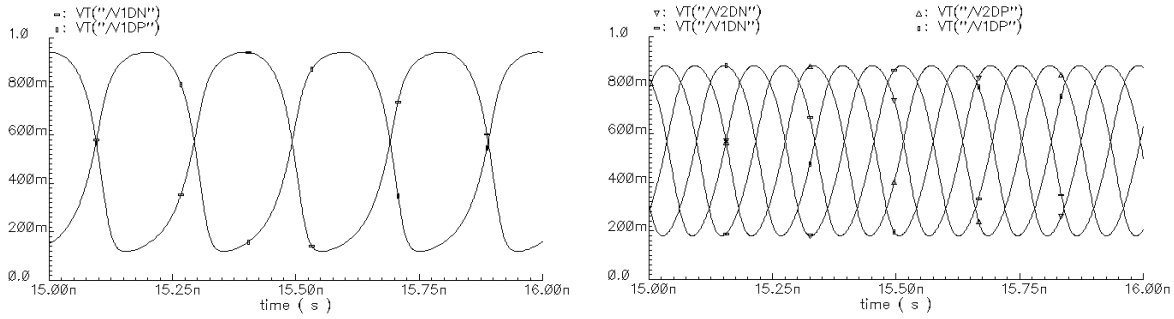


(a) (b)

Figure 77. Schematic diagram of RC-BPF oscillator. (a) Single oscillator. (b) Antiphase coupled oscillator.

To examine a quadrature signal generation and a frequency tuning behaviors, a single oscillator running at 2.5 GHz is designed using a RC-BPF. An antiphase coupled oscillator using two single oscillators is also designed. Schematic diagrams of both oscillators are depicted in Figure 77, and simulation results are plotted in Figure 78. It

should be mentioned that voltage waveforms in Figure 78 are taken from the inputs of BPF, i.e. V_o^+, V_o^-, V_{o1}^+, V_{o1}^-, V_{o2}^+ and V_{o2}^- in Figure 77 because those nodes exhibit higher voltage amplitudes than the output node of BPF. In Figure 78 (a), differential signals (V_o^+ and V_o^-) whose frequency is around 2.5 GHz is shown. Figure 78 (b) is quadrature signals (V_{o1}^+, V_{o1}^-, V_{o2}^+ and V_{o2}^-) and its frequency is around 4.2 GHz due to an antiphase coupling. Amplitude of Figure 78 (a) is higher than Figure 78 (b) since a BPF has the maximum impedance at 2.5 GHz.



(a) (b)

Figure 78. Simulation result of oscillators in Figure 77. (a) Single oscillator. (b) Antiphase coupled oscillator.

A coupling factor is determined to 40% which leads to θ of 22º according to (4-43). Table 5 summarizes the performance comparison of a single RC-BPF oscillator and an antiphase coupled oscillator.

Table 5. Comparison of a single oscillator and a coupled oscillator.

Parameter	Single oscillator	Coupled oscillator
f_{osc}	2.52 GHz	4.17 GHz
Output phases	0º, 180º	0º, 90º, 180º, 270º
Output amplitude	807 mV	700 mV
Power consumption	2.2 mA	6.1 mA
Phase noise @ 1 MHz	-96.5 dBc/Hz	-88.7 dBc/Hz

4.5.2. Variable Phase Ring Oscillator

A proposed RC-BPF can be used to form a phase shifter if cascaded multiple stages are connected. As seen in Figure 79 (a), when N delay stages are connected and form a feedback without an external phase shift, a phase shift at each delay stage becomes zero resulting in zero phase shift through overall oscillator. This satisfies a phase condition of Barkhausen criteria and an oscillation frequency is set to the frequency where a phase response becomes zero. In case that an external phase shift ($-N{\cdot}\Delta\Phi$) exists on a feedback path, as seen in Figure 79 (b), a cascaded delay stages would compensate this by generating a negative polarity of an external phase shift ($+N{\cdot}\Delta\Phi$) [80].

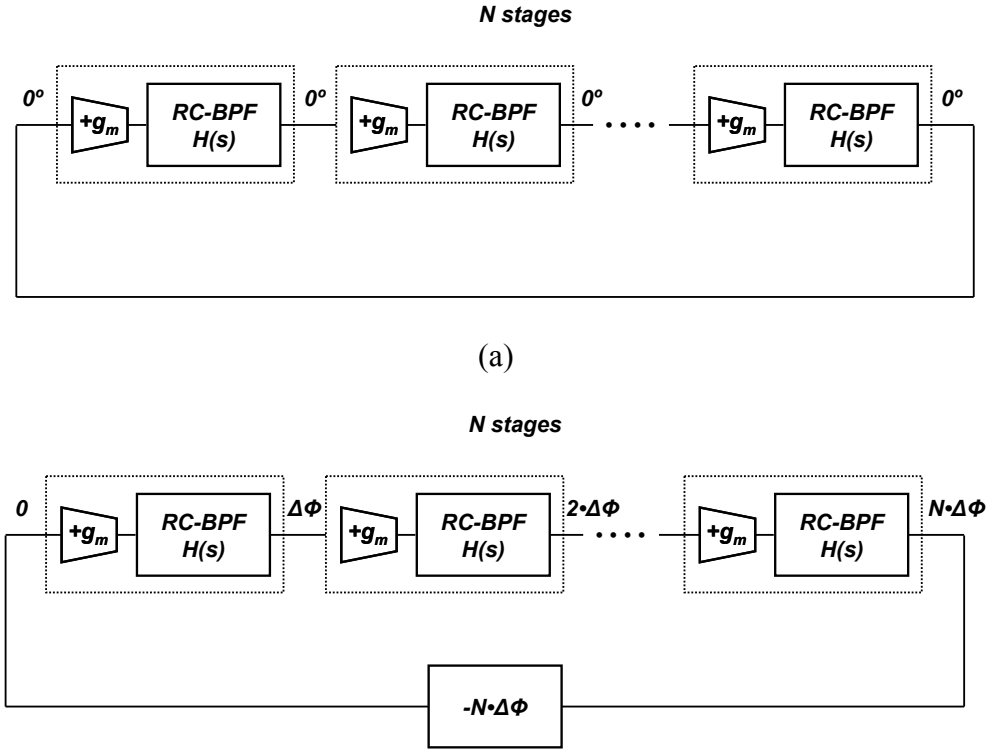


Figure 79. Cascaded N RC-BPF delay stages. (a) Without external phase shift. (b) With external phase shift.

The structure proposed in [80] used LC-BPF for a delay cell, and for an external phase shift, a duplicated cascaded delay stages are used. Note that a BPF exhibits a negative phase response at frequencies higher than a center frequency, as seen in Figure 76. The structure of Figure 79 (b) is able to generate an arbitrary phase shift depending on the amount of an external phase shift. A phase shift in a BPF can be introduced by adjusting its center frequency and the relationship between a frequency and a phase has a negative slope. This leads to a negative phase shift if a center frequency is increased. On the other

hand, a positive phase shift can be achieved when a center frequency is decreased. The phase array structure proposed in [80] used an LC-BPF for each delay stage that consumes large silicon area. Replacing LC oscillator with RC-BPF oscillator results in huge area saving.

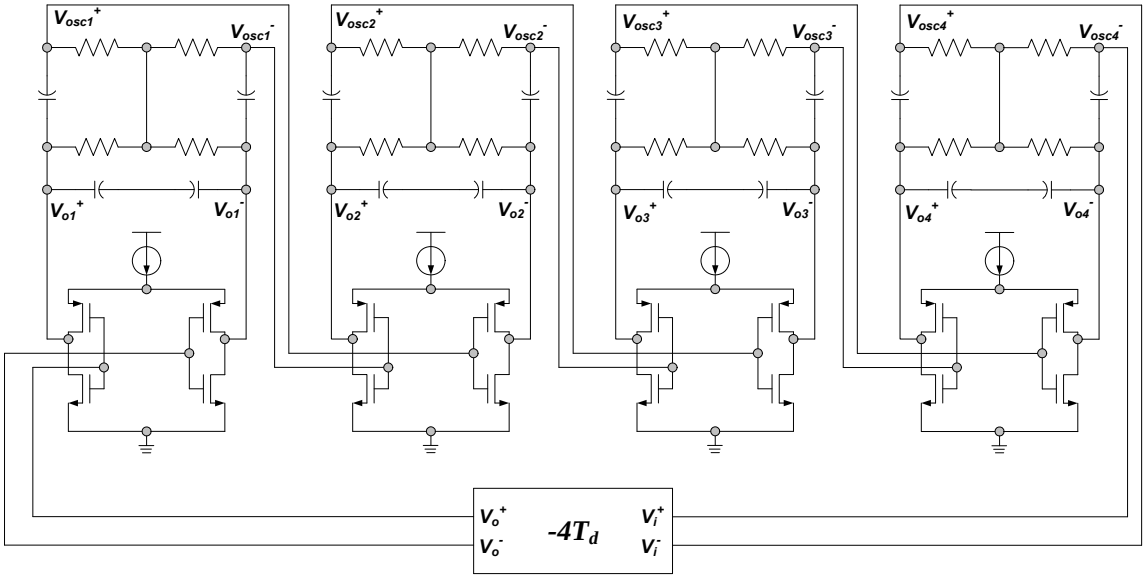


Figure 80. Schematic diagram 4-stage tunable phase shift generator with RC-BPF.

Figure 80 shows a schematic diagram of 4-stage tunable phase shift generator using RC-BPF. An external delay of $-4T_d$ is given using an RC all-pass filter (APF) as shown in Figure 81. A voltage transfer function in Figure 81 is

$$\frac{V_o^+ - V_o^-}{V_i^+ - V_i^-}(s) = \frac{1 - sR_aC_a}{1 + sR_aC_a} \tag{4-49}$$

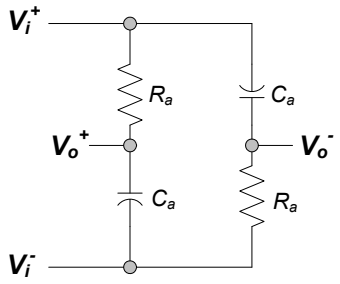
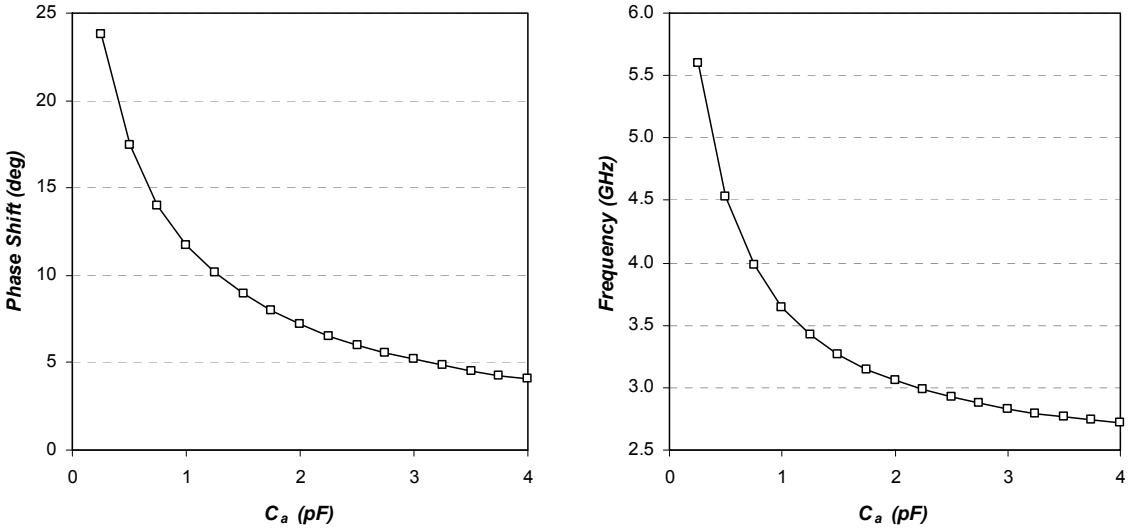


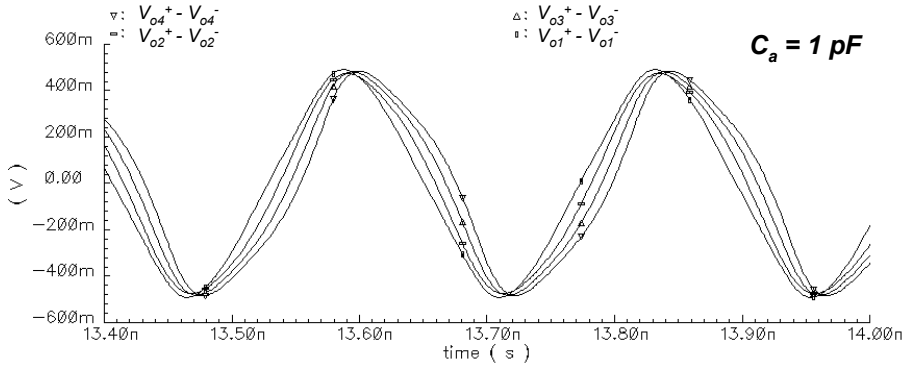
Figure 81. All-pass filter using RC.

An RC-APF provides a phase shift from 0 to -180° while a fixed magnitude gain of 1 for all frequencies, and a phase shift can be tuned by adjusting C_a.

In case that a phase shift of $-4T_d$ is given in the loop as depicted in Figure 80, each BPF stage must generate a delay of T_d to yield a zero phase shift around a loop for sustaining an oscillation. A phase shift per each stage can be tuned by adjusting an external phase shift. Figure 82 (a) plots a phase shift per stage versus C_a in an APF that has a fixed R_a = 100 Ω. As variable C_a tunes a delay in APF, a phase shift in each BPF stage is also tuned. It should be mentioned here that, when a phase shift is introduced to an RC-BPF, a frequency also deviates from the original frequency as plotted in Figure 82 (b) due to a low-Q. This is well described in a phase response of an RC-BPF in Figure 76. Unlike an LC-BPF that has a very sharp transition at around a zero phase, an RC-BPF needs a large amount of frequency deviation for a given phase variation. Figure 82 (c) shows voltage waveforms of each BPF when C_a is set to 1 pF.



(a) (b)



(c)

Figure 82. Tuning behavior. (a) Phase shift per stage vs. C_a. (b) Oscillating frequency vs. C_a. (c) Transient plot for each BPF output when C_a in APF is 1 pF.

4.6. Conclusions

This section has described an RC BPF-based oscillator suitable for RF applications. A prototype oscillator operating at 2.5 GHz was designed, and

measurement results have validated the proposed idea. Since the proposed oscillator is based on BPF, the phase noise shaping behavior is closer to that of an LC oscillator. In particular, the presented oscillator is less sensitive to supply noise than a ring oscillator. Also, by avoiding the use of inductors, the silicon area is more than one hundred times smaller than a commensurate LC oscillator.

CHAPTER V

FREQUENCY SYNTHESIZER WITH AN ENHANCED SPUR REDUCTION

5.1. Introduction

Frequency synthesizers generate periodic signals with accurately defined frequencies. It usually consists of a voltage-controlled oscillator (VCO) which generates tones and a feedback control loop that adjust a frequency of a VCO. This control loop uses phase information to acquire a desired output frequency so that it is called Phase-Locked Loop (PLL). In many RF communication systems, frequency synthesizers serve as an integral part of transceivers providing local oscillator (LO) signals. High performance frequency synthesizers often require fast settling times (to switch between channels) and low reference spurs (as dictated by wireless standards) simultaneously. However, there is always a trade-off between these two parameters. During the locked phase of the PLL, the non-idealities present in the phase frequency detector (PFD) and the charge pump (CP) results in ripples on the input control voltage of a VCO. The periodic nature of these ripples produces spurs at the output of the VCO which appear at integer multiples of the reference frequency (ω_{ref}), measured from the carrier frequency [6].

The magnitude of the spurs depends on a VCO gain, the amount of filtering, the value of the reference frequency and, the design of the PFD and CP, as well. Lower reference spur levels can be achieved by utilizing higher order loop filters and, [81] and

[82] have demonstrated a reasonable spur level as below -65 dBc with third-order loop filters. However, higher order loop filters decrease a phase margin of the loop making the system unstable and high overshoot voltages. A smaller loop bandwidth and VCO gain also help to reduce spurs at the cost of the increased settling time and reduced frequency range, respectively [83]. Dual loop architectures have been proposed to overcome the tradeoff between the settling time and spur reduction [84]. The main drawbacks in using this approach are the complicated system design and the instability that may occur due to the change of the loop dynamics. Another method is to move the reference spur from ω_{ref} to $N\omega_{ref}$ through the use of N-path delay elements, so the spur is shifted to a higher frequency [85]. This approach requires the use of the exact delay elements, which are practically difficult to implement. Also randomizing the delay shift has the effect of spreading the spur into a Sinc function, which does not provide enough spur suppression [85].

In this work, a spur reduction technique is used to disengage the trade-off between the settling time and spur suppression, hence giving the designer enough flexibility to optimize the design of the PLL to achieve the settling time and spur suppression requirements.

5.2. Background of Reference Spurs

5.2.1. Spur Effect on the Receiver Systems

Spurs in frequency synthesizer are the key performance parameter related to a spectral purity besides phase noise. Phase noise is due to various noise sources dithering the exact output frequency and its magnitude is monotonically decreased as offset frequency is increased. On the other hand, spurs are sharp tones and placed at certain offset frequencies. Depending on the divider structure, spurs are called either reference or fractional spurs. In many RF communication systems, integer-N frequency synthesizer architectures are preferred over fractional-N based architectures due to their design simplicity. In case of integer-N frequency synthesizers, reference spurs are main concern. Reference spurs are defined as unwanted sidebands whose frequencies are multiples of a reference frequency away from a fundamental tone. Reference spurs often degrades the system signal-to-noise ratio (SNR) requirement especially in narrow-band systems where channel frequencies are crowded within a small frequency band. This effect in RF receiver system is depicted in Figure 83.

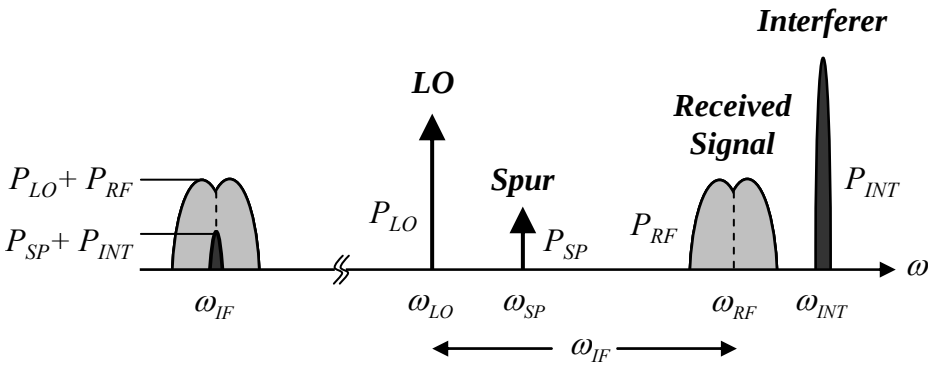


Figure 83. Effect of a reference spur and interferer in RF receiver system.

Suppose a spur at ω_{SP} (P_{SP}) is existed along with a LO carrier at ω_{LO} (P_{LO}) at the frequency synthesizer output, while the received signal at ω_{RF} (P_{RF}) is accompanied by an inteferer at ω_{INT} (P_{INT}). After a down-conversion mixing operation, in IF band, there would be the desired channel from the received signal down-converted with LO carrier. If $\omega_{INT} - \omega_{SP} = \omega_{IF}$, then the interferer is also convolved with a spur and falls into the IF band. The specification of spur can be calculated from the system SNR requirement and SNR at IF band, (P_{RF} + P_{LO}) - (P_{INT} + P_{SP}), [14].

$$P_{SP} - P_{LO} < P_{RF} - P_{INT} - SNR_{\min} \tag{5-1}$$

where P_{SP}-P_{LO} denotes the power of spur relative to the carrier as in dBc and SNR_{min} is the minimum required SNR which can be calculated by the relationship of bit error rate (BER) and SNR in specific communication standards. For example, Bluetooth standard specifies an interferer of 30 dB over the received signal at 2 MHz offset and SNR_{min} is 18

dB assuming a BER of 10^{-3}. Applying these numbers to (5-1) results in the amount of a spur suppression of -48 dBc at 2 MHz offset frequency [14].

5.2.2. Origins of Reference Spurs

Spurs can be generated by several sources including a power supply coupling, a substrate coupling, a reference clock coupling and non-idealities in the PFD and CP blocks. Spurs due to couplings are the most difficult problem for a designer to deal with as it is not predicted in circuit level simulations. Sometimes, this coupling effect is appeared even on PCB where a reference clock line is adjacent to a VCO control voltage line. This issue will be discussed in section 5.5.2.

Other than coupling effects, spurs can arise from non-idealities of individual building blocks, especially the PFD and CP as depicted in Figure 84. In Figure 84 (a), V_{REF} is a reference clock voltage and V_{DIV} is a voltage signal from a frequency divider. Phases of rising edges of each signal is compared at the PFD and, according to the input phase error, the PFD generates V_{UP} and V_{DN} to turn on I_{UP} or I_{DN} respectively. When PLL is locked in phase, the phase error becomes zero and rising edges of V_{REF} and V_{DIV} arrive simultaneously resulting in no change on V_{UP} or V_{DN}. However, in actual PFD implementation, there is a fixed delay, $\Delta t_{d,PFD}$ as shown in Figure 84 (b), in the reset path of the PFD, hence V_{UP} and V_{DN} have finite pulse widths. This delay is inserted on purpose in order to avoid a dead-zone problem [86].

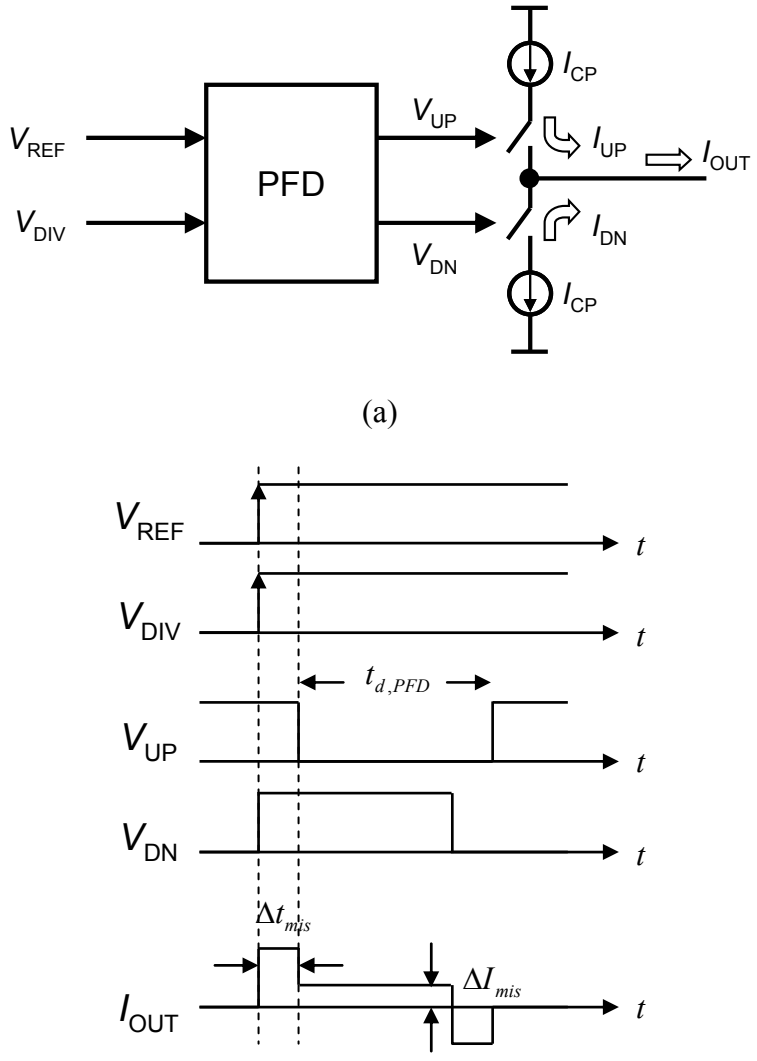


Figure 84. Spurs due to PFD and CP. (a) Block diagram of PFD and CP. (b) Timings of associated signals.

There might be mismatches in the PFD and CP due to the imperfections of each block. Since the PFD consists of logic gates, a timing mismatch can arise between the rise and fall time. The CP also contributes to a timing mismatch in case that the switch

for I_{UP} is PMOS and NMOS is used for the switch for I_{DN}. Those effects can be lumped into one design variable which is shown as Δt_{mis} in Figure 84 (b). A mismatch between I_{UP} and I_{DN} in the CP is also a key issue in the CP design. As transistors for current sources have finite output impedance, a desired current is not exactly mirrored depending on the settled CP output voltage. This effect becomes more serious in low-voltage design where a cascade structure cannot be used due to insufficient voltage headroom. ΔI_{mis} in Figure 84 (b) denotes a current mismatch between I_{UP} and I_{DN}.

Therefore, I_{OUT} has a certain pulse width even in the perfect locked condition and, by the following loop filter, is filtered and converted to a voltage waveform that is a control voltage of the VCO. Note that resulting ripples on the VCO control voltage is periodic and its fundamental frequency is a reference frequency since the PFD compares the input phases at every reference cycles.

5.2.3. Frequency Modulation of Reference Spurs

As the ripple on the VCO control voltage is periodic, its frequency spectrum can be expressed with Fourier series,

$$V_{cnt}(t) = \sum_{i=1}^{n} a_i \cos(i\omega_m t) \tag{5-2}$$

where a_i is Fourier coefficient of *i-th* harmonic and ω_m is the radian frequency of the ripple on the VCO control voltage. (5-2) ignores dc component since it is related to the VCO output fundamental frequency and not used for the frequency modulation analysis. a_i in (5-2) is determined by the pulse width and amplitude and, in most cases, a_1 is the most significant coefficient because it is adjacent to VCO output fundamental tone and the suppression of magnitude by the loop filter is minimum among other harmonics. Also, its frequency is same with the channel space and the VCO frequency modulation effect is most significant due to the interferer at the adjacent channel. Hence, from following analysis, only a_1 will be considered. Since VCO output frequency is determined by V_{cnt} and VCO gain (K_{VCO}), the VCO output phase is an integral of V_{cnt} multiplied by K_{VCO}. The VCO output voltage can be calculated as

$$V_{out}(t) = V_o \cos\left(\omega_0 t + K_{VCO}\int V_{cnt}(\tau)d\tau\right) \tag{5-3}$$

where V_o is an amplitude of the VCO output voltage and ω_0 is a free running frequency. Substituting (5-2) into (5-3) considering only a_1 for simplicity yields

$$V_{out}(t) = V_o \cos\left(\omega_0 t + \frac{K_{VCO}a_1}{\omega_m}\sin(\omega_m t)\right) \tag{5-4}$$

If $\omega_m << \omega_0$, then narrowband FM approximation can be used and (5-4) becomes

$$V_{out}(t) \cong V_o\left(\cos(\omega_0 t) + \frac{K_{VCO}a_1}{2\omega_m}\{\cos((\omega_0 + \omega_m)t) + \cos((\omega_0 - \omega_m)t)\}\right) \qquad (5\text{-}5)$$

(5-5) shows that there are spurious tones at the offset frequency of ω_m from ω_0 along with a fundamental tone at ω_0. The ratio of the amplitude of spurious tone relative to the carrier tone is given as

$$A_{sp} = \frac{K_{VCO}a_1}{2\omega_m} \quad (dBc) \qquad (5\text{-}6)$$

Figure 85 shows the VCO model with its control voltage (V_{cnt}) and output voltage (V_{out}). If V_{cnt} can be modeled as square pulses with a period of T_m, the frequency spectrum has harmonics at every multiples of f_m (= $1/T_m$) and their amplitude is a_i where i is an index number of harmonics. A periodic pulse train modulates the VCO output voltage, hence VCO out frequency has spurious tones at the offset frequency of f_m from the carrier frequency f_0.

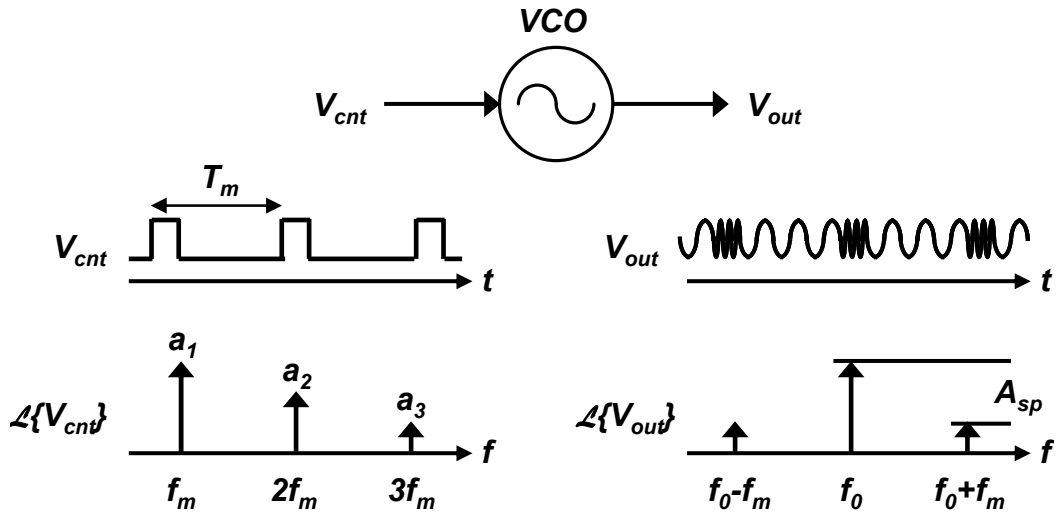


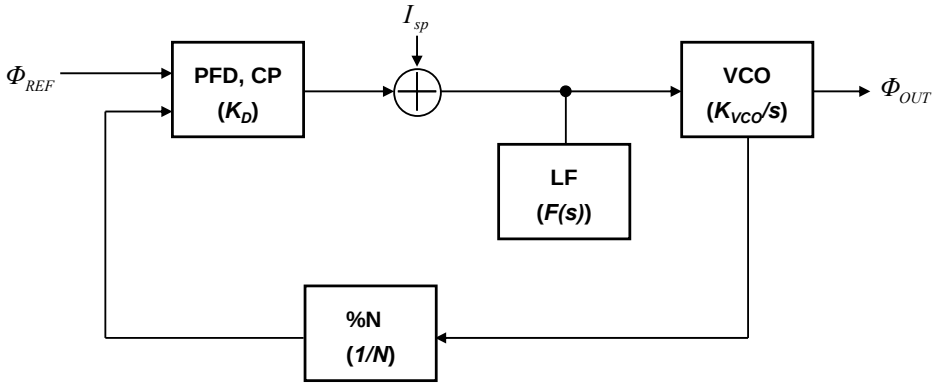
Figure 85. VCO model and its frequency modulation due to a periodic signal on the control voltage.

(5-6) indicates the amplitude of spurs can be reduced by decreasing K_{VCO} and increasing f_m. However, those parameters are usually determined by the system requirements such that small K_{VCO} limits the frequency tuning range and f_m is set by the minimum channel space to generate every required channel frequencies. And, to minimize V_{cnt} coefficients (a_i), especially a_1, also decreases the spurs amplitude. It can be done by optimizing the design of PFD and CP or with a smaller loop bandwidth at the cost of an increased settling time.

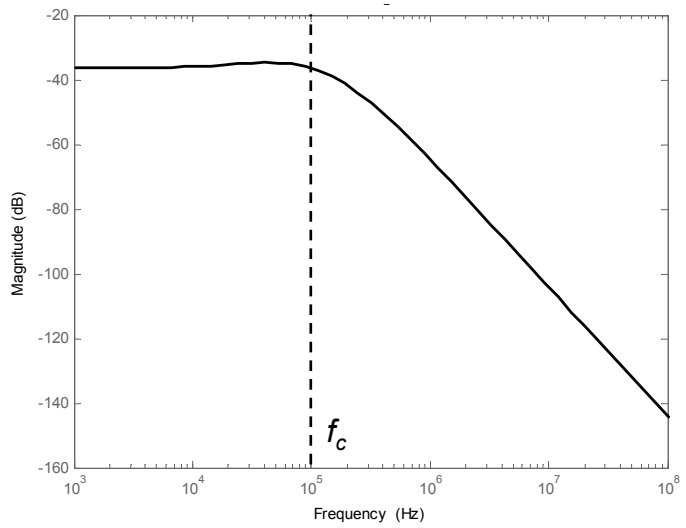
5.3. The Proposed Adaptive Low-Pass Filtering Technique

As discussed in section 5.2.2, the source of reference spurs (ripples on the VCO control voltage) is periodic in locked condition with the reference period. Due to the

periodic nature, its frequency spectrum consists of a fundamental tone at the reference frequency and its harmonics. In integer-N frequency synthesizers, a reference frequency is usually set by the minimum channel spacing and it is at least ten times higher than the loop bandwidth due to the loop stability issues [12].



(a)



(b)

Figure 86. Linearized PLL with a spur source I_{sp}. (a) Block diagram. (b) Transfer function of I_{sp} and Φ_{out} assuming a second-order LF.

Figure 86 (a) shows a linearized PLL model with a spur source current I_{sp} that is located at the charge pump out. Each building block has a gain for a linear analysis. A transfer function from a spur source current to the output phase can be calculated as

$$\frac{\phi_{OUT}(s)}{I_{SP}(s)} = \frac{K_{VCO}F(S)}{S + K_D K_{VCO} F(S)/N} \tag{5-7}$$

The loop filter in the feedback loop provides a low-pass filter behavior and any frequency components existed beyond its bandwidth is suppressed. Assuming that the loop filter is second order with two poles and one zero, it exhibits 40 dB/decade suppression against any tones beyond the second pole. Figure 86 (b) depicts the case when the loop bandwidth is set to 100 KHz and the loop filter has two poles at DC and 400 KHz and a zero at 25 KHz. It indicates that, as the loop bandwidth is decreased having more space to the reference frequency, spurs will be more suppressed by the filtering action of a closed-loop.

However, small loop bandwidth makes a feedback system slower, as a result, the settling time is increased. Also, for a small loop bandwidth, a non-zero pole and a zero frequency in the loop filter should be decreased, which requires huge resistor and capacitors taking large silicon area. Increasing the order of loop filter also improves the spur suppression. It can be accomplished by adding more poles. In this case, the frequency of added poles should be carefully determined to minimize the phase margin degradation and normally, its frequency is higher than original pole. Hence, the required

additional silicon area is not as serious as in the previous case. However, this method degrades the phase margin and the system has higher overshoot during a transition.

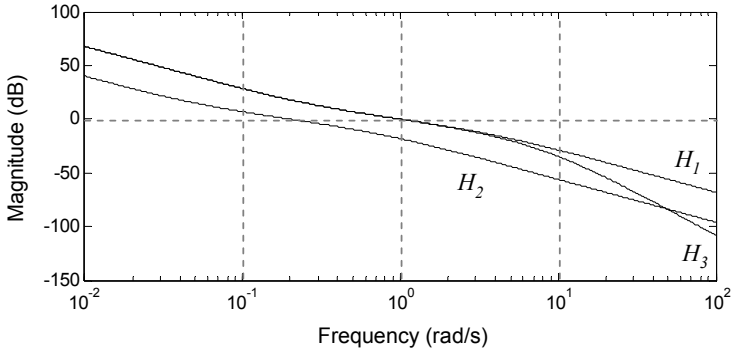
The effects on the spur suppression by varying loop dynamics can be demonstrated using MATLAB simulations. Assuming the type-II third-order PLL whose frequency is normalized to 1 rad/s and the damping factor of 1, its transfer function (H_1) can be expressed as,

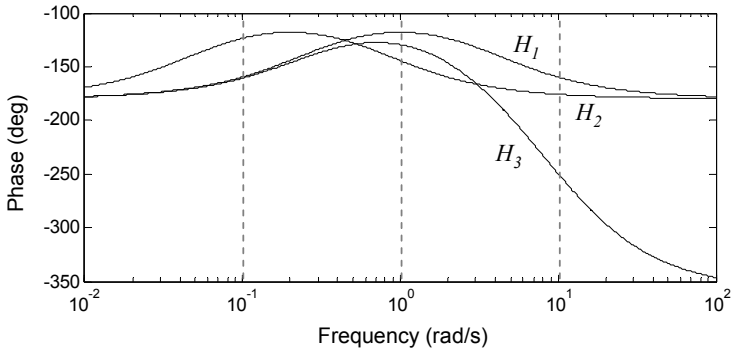
$$H_{1,open}(s) = \frac{(1+4s)}{4s^2(1+s/4)} \tag{5-8}$$

where a non-zero pole is placed at 4 rad/s and a zero at 1/4 rad/s yielding the phase margin of 62º. If a reference frequency is 50 rad/s, the ripple suppression by the loop will be -56 dB. If a loop bandwidth is decreased by factor of 5 (H_2), this suppression is improved to -84 dB. Also the same improvement can be achieved by adding two poles at 10 rad/s (H_3) which is 2.5 times higher than a non-zero pole.

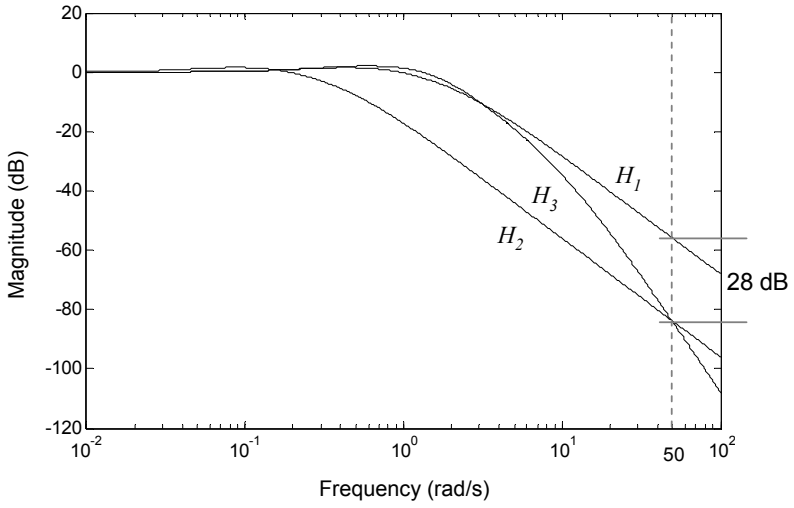
$$H_{2,open}(s) = \frac{(1+20s)}{100s^2(1+5s/4)} \tag{5-9}$$

$$H_{3,open}(s) = \frac{(1+4s)}{4s^2(1+s/4)(1+s/10)^2} \tag{5-10}$$



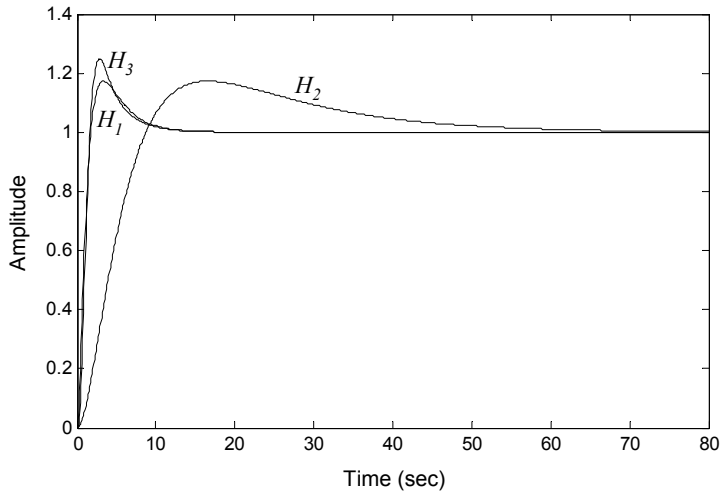


(a)



(b)

Figure 87. Transfer function plot of (5-8), (5-9) and (5-10). (a) Open-loop transfer function. (b) Closed-loop transfer function. (c) Step response.



(c)

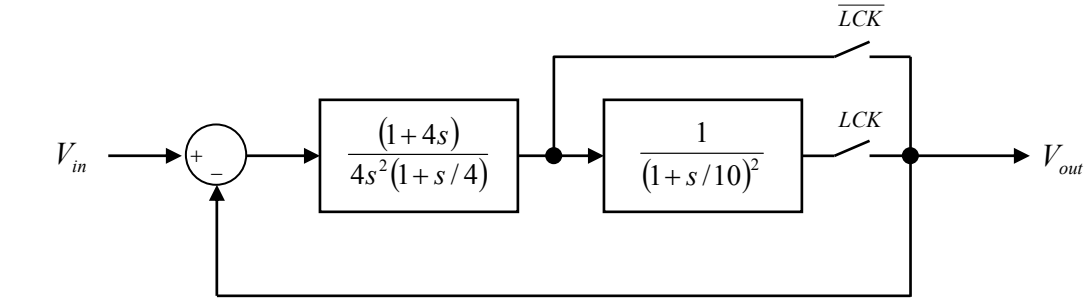
Figure 87. Continued

A bode-plot of (5-8), (5-9) and (5-10) are plotted in Figure 87 (a) and the magnitude response is depicted in Figure 87 (b). In above figures, H_2 is a shifted version toward a zero frequency of H_1 with the same phase margin, while the phase margin is degraded in H_3. Figure 87 (c) shows a step response and the settling time in H_1 and H_3 are very close each other while very slow in H_3 because the settling time is inversely proportional to the loop bandwidth. H_3 has a higher overshoot than H_1 and H_2 which can increase settling time in a low-voltage design since it limits the dynamic range of the charge pump. Additionally, if a loop filter is made of a resistor and two capacitors, in H_2 where the bandwidth is scaled down by factor of 5, the required size for one of the capacitors is increased by factor of 25 that requires huge silicon area according to the control theory [11].

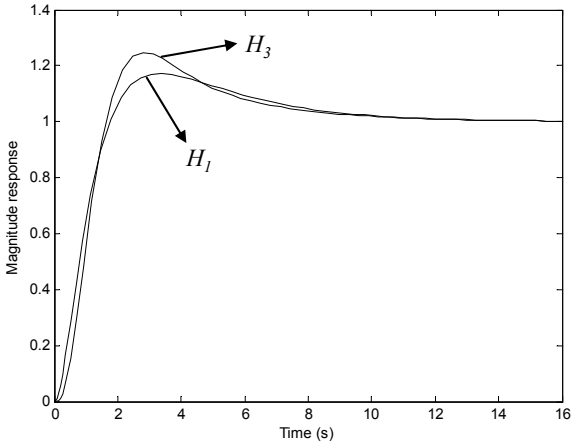
It is worth to mention that the spur suppression is measured during the steady status of the loop (after the loop is locked) and the overshoot is the loop behavior during the transition. These facts lead to the idea that the system H_1 and H_3 can be adaptively switched each other depending on the loop status. During the transition, the system behaves as H_1 that gives the small overshoot and good phase margin and, after the loop is locked, it is switched to H_3 yielding the good spur suppression without huge additional silicon area like the case of H_2.

The conceptual block diagram in which the loop order is adaptively changed is shown in Figure 88 (a). The additional second order low-pass filter is added on the loop when *LCK* is high. *LCK* is the output of the lock detector that monitors the loop status and issues *LCK* signal when the error between the input and the feedback signal is within the specific range. Figure 88 (b) depicts the step response of H1 (type-II third-order) and H3 (type-II fifth-order). H3 shows the higher order loop behavior such as a high overshoot while H1 is a typical third-order loop. Figure 88 (c) is the step response of the system shown in Figure 88 (a) where the loop order is adaptively changed assuming the loop is locked at $t = 9\ s$. When $t < 9\ s$, it exhibits the same response with H1 while it follows H3 behavior when $t > 9\ s$.

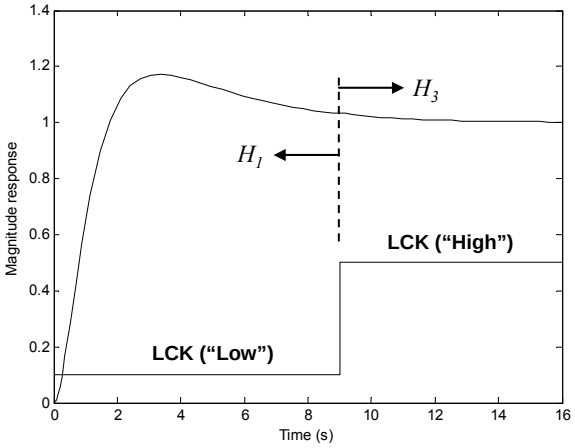
As a conclusion, if the loop order can be switched to higher order after the loop is locked, the system can have good spur suppression without a high overshoot as in higher order loop and the additional huge silicon area as in low loop bandwidth system.



(a)



(b)



(c)

Figure 88. Adaptive loop order system. (a) Conceptual block diagram. (b) Step response of H1 and H3. (c) Step response of Figure 88 (a).

5.4. System Level Design of the Proposed Integer-N Frequency Synthesizer

An integer-N frequency synthesizer with the proposed enhanced reference spur suppression techniques was designed and characterized. The covered frequency band was chosen to be compatible with IEEE 802.16 standard (WiMax) [87]. A part of the

frequency band in WiMax standard is located at the upper Unlicensed National Information Infrastructure (U-NII) band when a regulatory domain is USA.

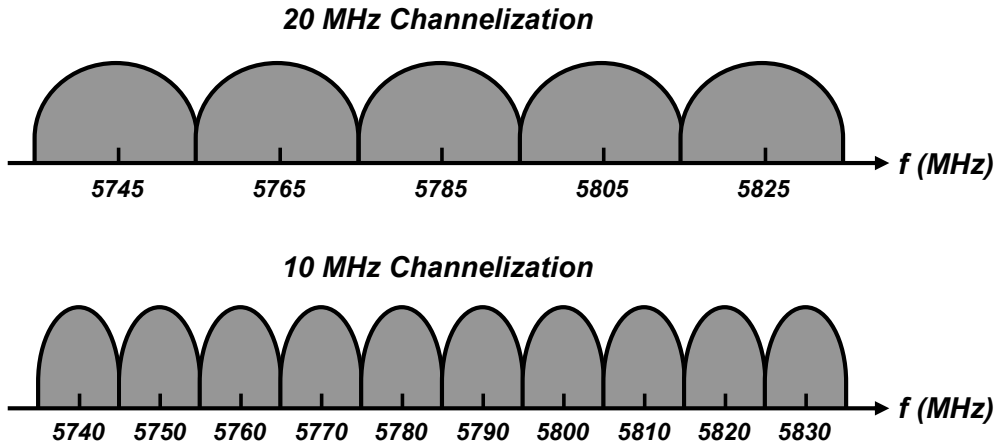


Figure 89. Channelizations with 10 MHz and 20 MHz in U-NII band in USA [87].

As shown in Figure 89, the U-NII upper band in USA has two canalizations, 10 MHz and 20 MHz. The output frequency range of the frequency synthesizer was determined as 5740 MHz ~ 5830 MHz with 5 MHz of a channel space in order to cover both 10 MHz and 20 MHz channelizations.

Since the purpose of this work is to prove the proposed idea for an enhancement of reference spurs suppression, other parameters of a frequency synthesizer, such as a phase noise, a reference spur level and settling time, are not determined as mandatory specifications.

5.4.1. The Conventional Loop Parameter Design Procedure

The loop parameter was designed as a conventional type-II third-order PLL as shown in Figure 90 since the proposed techniques to enhance a suppression of reference spurs can be added without modifying the existing conventional design.

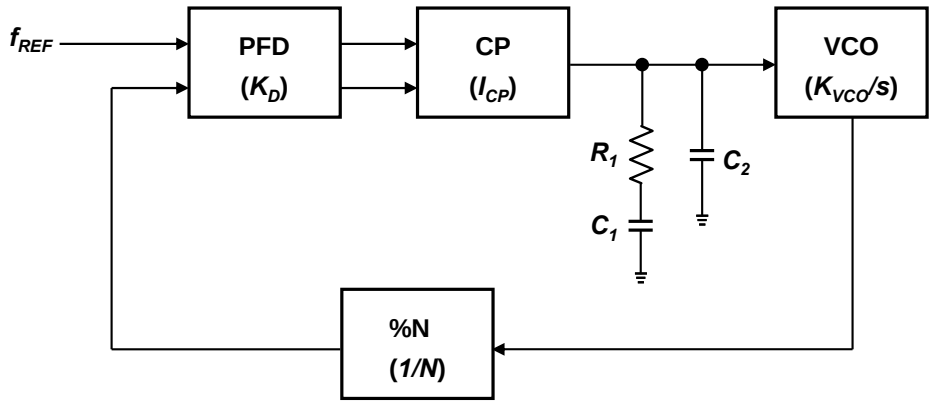


Figure 90. Conventional type-II third-order PLL with an additional low-pass filter.

The loop parameters design procedure is as follows [14].

(1) The first step is to determine the reference frequency f_{REF}. 5 MHz was chosen as f_{REF} as discussed above in order to cover the upper U-NII band in USA.

(2) Determine the loop bandwidth frequency (the crossover frequency, ω_c) as 2π × 100 KHz that is fifty times lower than f_{REF}. The maximum allowed ω_c is ten times lower than f_{REF} according to Gardner's stability limit [12]. However, lower ω_c allows enough frequency room to place additional poles not

degrading phase margin significantly unless it violates the settling time requirement.

(3) Damping factor (ζ) of 1 was selected. Normally a critically damped loop (ζ=1) works best for the optimal settling time and loop stability. Note that there may be confusions between a pseudo-damping factor (ζ') in the third-order loop and a damping factor of second-order approximation (ζ) [88] because the loop is the third-order system. In this work, the second-order approximation (ζ) is used for a damping factor.

(4) The non-zero pole frequency (ω_p) and the zero frequency (ω_z) are placed at 4 and 1/4 times resulting the placement ratio of $\alpha^2 = 4$. These conditions, $\omega_p = \omega_c \times 4 = 400$ KHz and $\omega_z = \omega_c / 4 = 25$ KHz, yield a phase margin of 62º. Note that the third-order loop transfer function will slightly over-damped with a pseudo-damping factor of ζ'=1.5.

(5) The natural frequency ω_n is given as $\omega_n = \omega_c / (2\zeta) = 2\pi \times 50$ KHz.

(6) The averaged dividing ratio N can be calculated from the median of output frequency range divided by the reference frequency. $N = (f_{max} + f_{min}) / (2 \times f_{REF}) = (5740 + 5830) / 5 = 1157$. Note that if N is calculated from the median output frequency, the phase margin is degraded when a frequency synthesizer is working at the highest frequency. On the other hand, if N is taken from the highest output frequency, then the settling time performance is degraded when the system works at the lowest frequency. Normally, in narrow band

application where the variation of N is not large, the averaged dividing ratio works well in terms of the stability and the settling time.

(7) Assuming the VCO gain $K_{VCO} = 2\pi \times 240$ MHz and the charge pump current $I_{CP} = 60$ μA, the passive elements in the loop filter can be calculated as $C_1 = (I_{CP}K_{VCO}) / (2\pi N\omega_n^2) = 128$ pF, $R_1 = 1 / (\omega_{z1}) = 50$ KΩ and $C_2 = 1 / (\omega_p C_1) = 8$ pF.

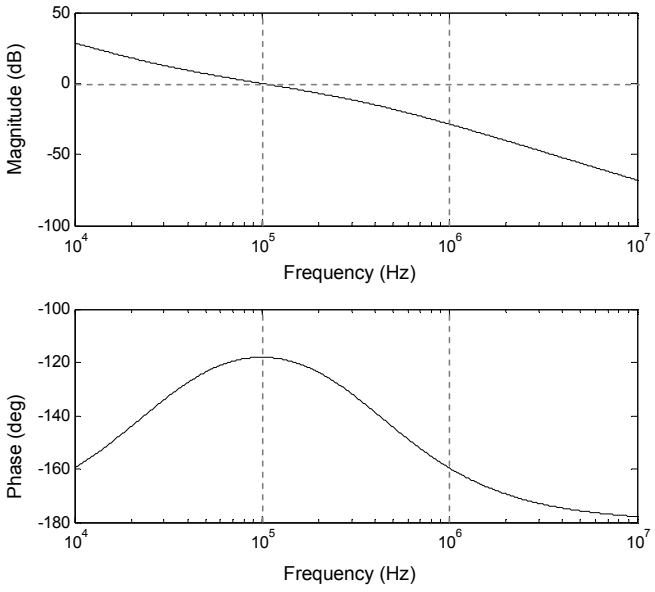
(8) The settling time can be estimated from ζ and ω_n using the second-order closed-loop transfer function. The second-order loop is used as it provides simple solutions as well as intuitive results. Assuming the initial frequency $f_0 = 5740$ MHz, the frequency step $\Delta f = 90$ MHz and the settling accuracy δ = 8 ppm, in a critically-damped system, the settling time is $t_s \approx ln(\Delta f / \delta f_0) / (\zeta \alpha\omega_n) = 24.1$ μs. Since the calculated settling time is estimated from the second-order loop system, the actual settling time will be increased as the additional poles are introduced during the transition of the loop.

Table 6 summarizes the loop parameters designed in the above procedures.

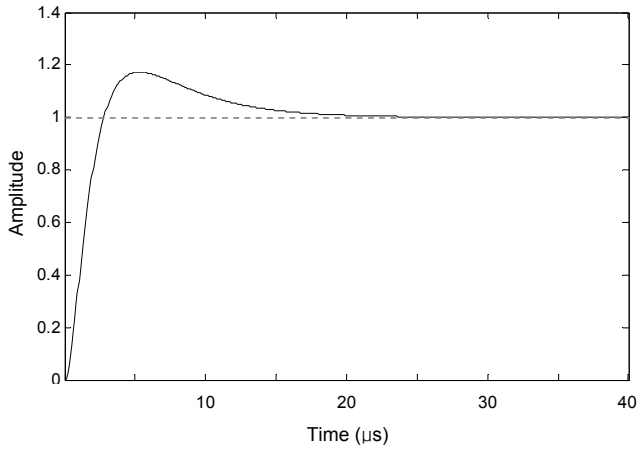
Table 6. Summarized table for the designed loop parameters.

Parameter	Designed value
$f_{out,min}$, $f_{out,max}$	5740 MHz, 5830 MHz
f_{REF}	5 MHz
N	1157
ζ	1
ω_c, ω_n	$2\pi \times 100$ KHz, $2\pi \times 50$ KHz
ω_p, ω_z	$2\pi \times 400$ KHz, $2\pi \times 25$ KHz
R_1	50 KΩ
C_1	128 pF
C_2	8 pF
Phase margin	62 º
K_{VCO}	$2\pi \times 240$ MHz/V
I_{CP}	60 μA
Settling time	24.1 μs

Figure 91 is the simulation results based on a linear system using loop parameters shown in Table 6.



(a)



(b)

Figure 91. Transfer function plot of a designed loop using Table 6. (a) Magnitude and phase response of an open-loop transfer function. (b) Step response of a closed-loop transfer function.

The above design of a type-II third-order loop works during the transition, and once the loop is locked, the system is switched to a type-II fifth-order loop. Since higher-order loop is enabled after the loop is settled, it does not experience big frequency jumps except for disturbances due to noises or glitches. However, its loop stability through a phase margin should be examined in order to make sure the loop would be in stable status.

5.4.2. The Additional Low-Pass Filter

Along with the conventional type-II third-order PLL, the additional LPF is added to improve the reference spur suppression. Since the reference frequency is 5 MHz and the non-zero pole of the loop filter (ω_p) is 400 KHz in this design, two additional poles are placed at 1 MHz considering the design trade-off between the improvement of reference spurs and the phase margin degradation.

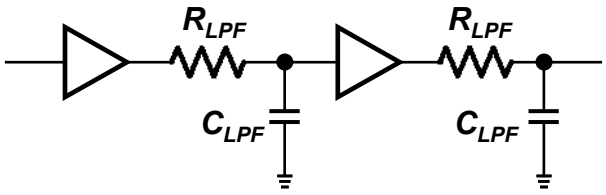
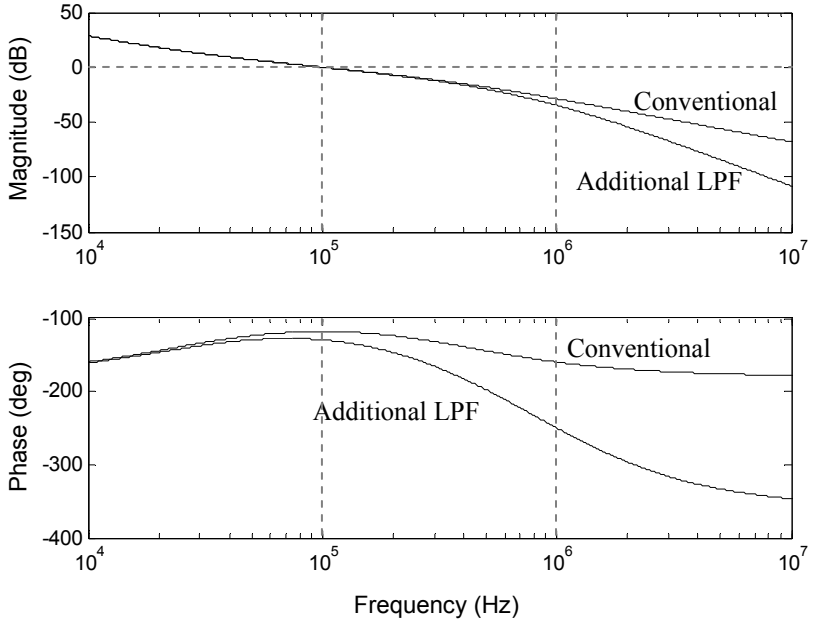


Figure 92. The additional LPF.

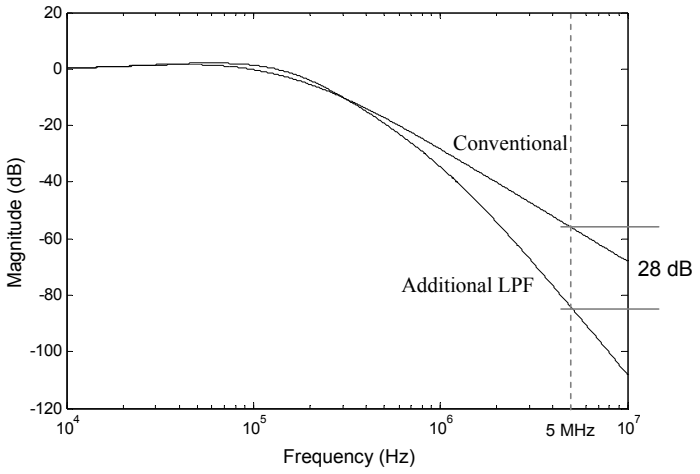
Figure 92 shows a buffered second-order RC LPF. A buffered RC-LPF structure is chosen for the design convenience as the pole frequency is easily calculated from *R*

and C. The pole of this LPF is $\omega_{LPF} = 1 / (R_{LPF} \times C_{LPF})$, and two poles of each stages are exactly overlapped. For $\omega_{LPF} = 2\pi \times 1$ MHz, R_{LPF} and C_{LPF} are determined to be 80 KΩ and 2 pF, respectively.

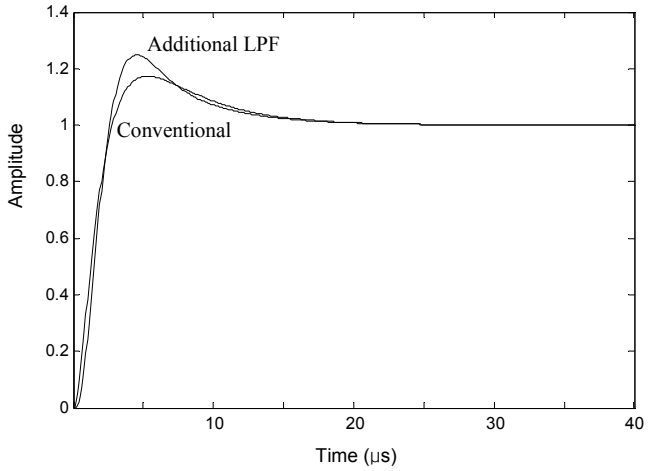


(a)

Figure 93. Transfer function plot for conventional PLL and proposed PLL (Conventional + Additional LPF). (a) Magnitude and phase response of an open-loop transfer function. (b) Magnitude of a closed-loop transfer function. (c) Step response of a closed-loop transfer function.



(b)



(c)

Figure 93. Continued.

With the additional two poles at 1 MHz, the phase margin is decreased from 62º to 51º while the suppression of reference spurs is improved 28 dB over the conventional architecture as depicted in Figure 93. A decreased phase margin is appeared as an increased overshoot in a step response of a closed-loop system (shown in Figure 93 (c)).

5.4.3. System Architecture of the Proposed Frequency Synthesizer

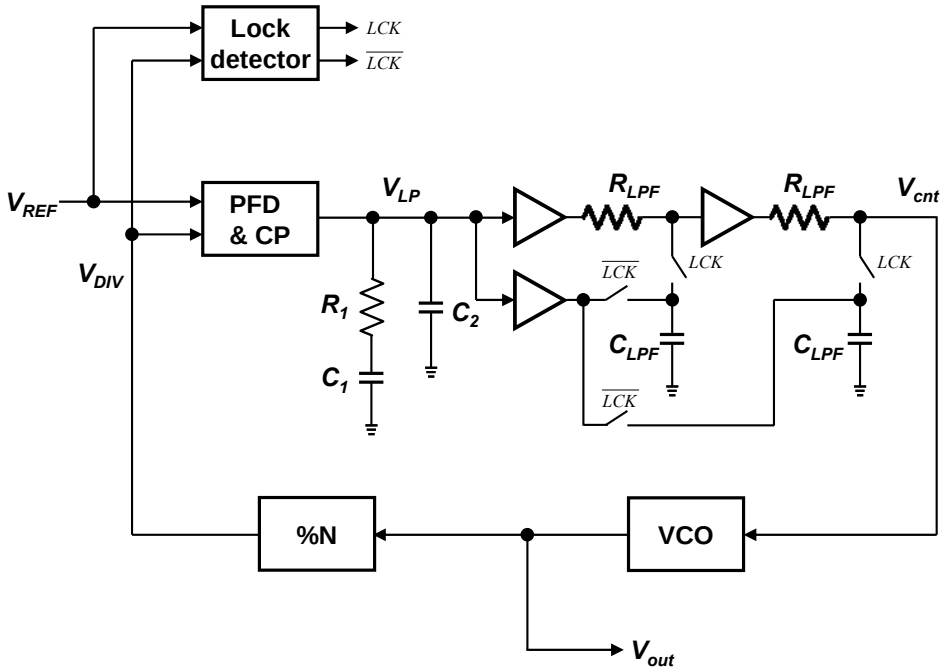


Figure 94. Architecture of the proposed frequency synthesizer.

Figure 94 is a block diagram of the proposed frequency synthesizer. It consists of a conventional frequency synthesizer and the additional LPF that is controlled by the lock detector. The lock detector compares the phase error of V_{REF} and V_{DIV} like the PFD. If the phase error is within a certain value for multiple consecutive numbers, the lock detector issues its output, LCK and $\overline{LCK}$. LCK connects C_{LPF} to R_{LPF} and enables the additional LPF by closing the switch between the resistors and capacitors. During $\overline{LCK}$ is on, the top plates of C_{LPF} follow the voltage of the loop filter (V_{LP}) through the buffer. It can be done by putting the buffer between V_{LP} and C_{LPF} with switches controlled by

$\overline{LCK}$. This buffer also isolates C_{LPF} from V_{LP}, hence the charge pump current is not used to charge C_{LPF}. This pre-charging C_{LPF} prevents a voltage disturbance when LCK suddenly connects C_{LPF} to R_{LPF}, as a result, it minimizes a voltage glitch when the loop changes its order.

5.5. Building Block Designs

5.5.1. Phase Frequency Detector (PFD)

The fundamental role of the phase frequency detector (PFD) is to compare the phases of two inputs, V_{REF} (a reference clock) and V_{DIV} (the divider output), and converts the phase error of two inputs into the associated pulses to switch a charge pump. The pulse width is proportional to the amount of input phase difference. There are several types of phase error detectors, but the most popular for frequency synthesizer applications is the phase-frequency detector (PFD) [12].

Figure 95 shows the topology of the PFD used in this work. It is the NAND-based tri-state PFD that consists of two D-type flip-flops (DFFs), an AND gate and a delay element. It generates two outputs, V_{UP} and V_{DN}, corresponding to a positive and negative phase error. Twp outputs of the PFD turn on the charge pump in the way of pumping current into the loop filter when V_{UP} is high and drawing the current out of the loop filter during V_{DN} is on. Hence, the transfer function of the PFD and the charge pump can be linear across the zero phase error.

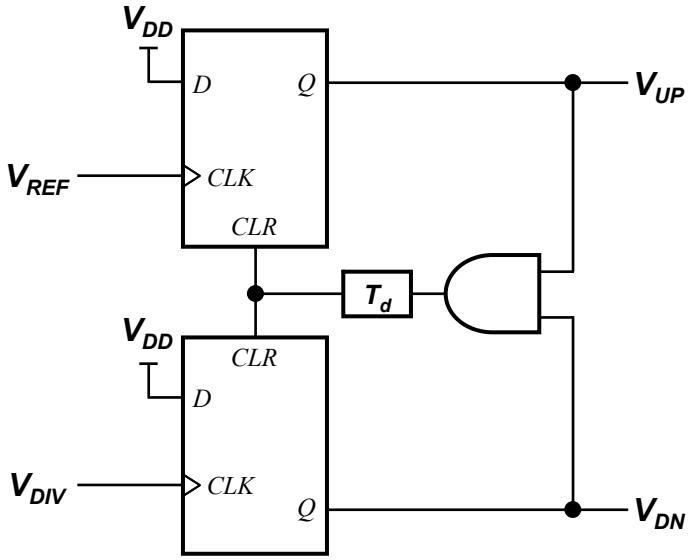


Figure 95. Topology of the phase frequency detector.

The operation of the PFD shown in Figure 95 is as follows. If V_{REF} comes first, it turns on V_{UP} and V_{UP} stays until V_{DIV} comes and resets DFF and V_{UP}. V_{DN} will be on in the same way if V_{DIV} comes first. Note that the DFFs in Figure 95 are designed as rising-edge triggered, hence only the rising edges in V_{REF} and V_{DIV} are used and a duty ratio is ignored. When the loop starts working, V_{REF} or V_{DIV} will always lead the other with big phase errors, as a result, DC component is generated performing the frequency acquisition. When the phase error becomes small, the value of delay (T_d) is critical to avoid a dead-zone problem. In this design, T_d is set to 100 ns which is long enough to turn on the charge pump switches.

5.5.2. Charge Pump (CP) and Loop Filter (LF)

The charge pump is formed by a current source I_{CP}, two currents source transistors (MBN and MBP) and two switches (MN and MP). Note that MP is a PMOS transistor and is controlled by $\overline{V_{UP}}$ that is complementary to the PFD output V_{UP}. It pumps a current (I_{CP}) into the loop filter when both $\overline{V_{UP}}$ and V_{DN} is low resulting the positive I_{out}. On the other hand, when $\overline{V_{UP}}$ and V_{DN} is high, it draws I_{CP} from the loop filter resulting the negative I_{out}.

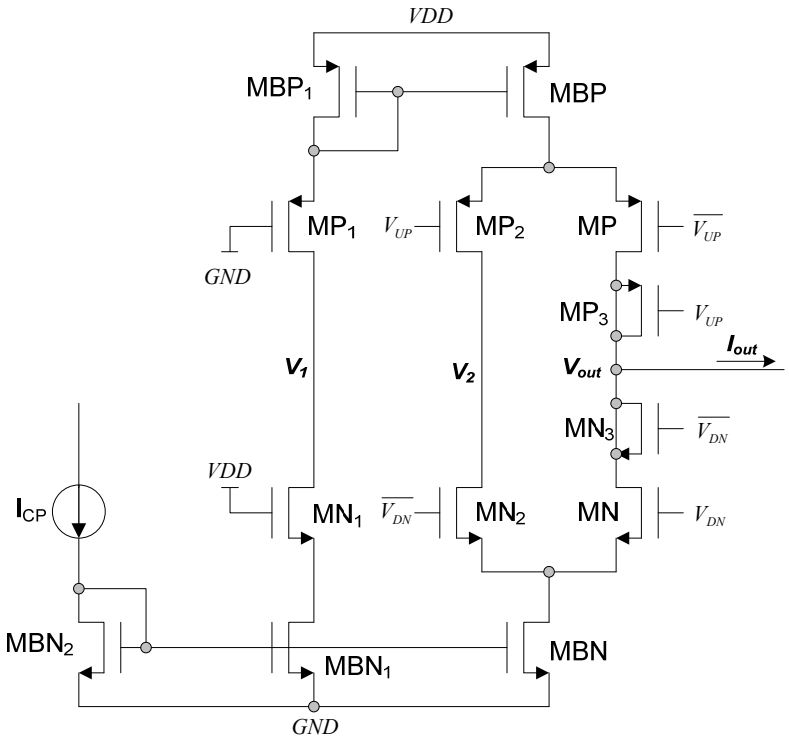


Figure 96. Schematic diagram of the charge pump.

The amount of I_{CP} is set by a current source and is mirrored to MBN and MBP. A current mirroring to MBP is done by a self-bias circuit including two additional transistors, MN_1 biased to *VDD* and MP_1 biased to *GND*. MN_1 and MP_1 are always turned on and V_1 is usually set to the middle point between VDD and GND. It indicates that if V_{out} is similar to V_1, then the current balance of MBN and MBP becomes maximal.

After the loop is locked, MN and MP are off in most of time and turned on during very short time (the delay in the PFD reset path – the rising time of MN and MP). When MN and MP are off, MN_2 and MP_2 are on instead. It keeps MBN and MBP turned on all the time for the fast turn-on time, and avoids charging the parasitic capacitance at the drain of MBN and MBP.

MN_3 and MP_3 are dummy transistors to minimize the charge injection problems. When MN and MP are turned off, without dummy transistors, the half of the remaining charge on the transistor's channel will be injected to V_{out} causing the voltage offset error. MN3 and MP3 generate the opposite polarity of this charge by the complementary signals and cancel the injected charges. The dummy transistors also help to minimize the glitch on the V_{out}.

For better current matching, MBN and MBP are usually built with a cascade structure. However, in this work, a cascade topology is not used since *VDD* is limited to 1.3V. Instead, long channel transistors are used for MBN and MBP to minimize a channel length modulation.

The loop filter consists of a resistor and two capacitors. Designed values of resistor and capacitors are listed in Table 6. Since the loop filter always works regardless of the loop status, it doe not require any switches.

A resistor (R_1) is determined to be 50 KΩ. It uses N-type poly resistor which provides a good accuracy compared to a diffusion-type or nwell-type resistor. R_1 is decomposed to 16 pieces of 3.125 KΩ and surrounded by dummy resistors to increase accuracy by minimizing proximity effect. W/L of each slide is 1.5 μm / 18.53 μm that is 3 times wider than the minimum width (Wmin = 0.5 μm) to decrease the effect of process variations.

Two capacitors (C_1 and C_2) are designed to be 128 pF and 8 pF, respectively. If the damping factor of the loop is 1 (critically damped), C_1 is 16 times larger than C_2, and depending of the loop bandwidth, C_1 would be too big to implement with a passive capacitor. In this case, C_1 is implemented using the capacitor multiplier or even the external capacitor. However, the capacitor multiplier is often suffered by process variations, and the external capacitor is affected by parasitics associated with bonding wires and PCB. In this work, fortunately, both C_1 and C_2 are moderate sizes allowing the implementation using the metal-insulator-metal (MIM) capacitor. MIM capacitor is the most accurate capacitor in CMOS process and its accuracy is better than poly-insulator-poly (PIP) capacitor or MOS capacitor. Also, MIM capacitor is placed far from the substrate yielding the small parasitic capacitance. For better matching in the layout, both capacitors are drawn using the same unit capacitor. The unit capacitor is determined to be 500 fF and its size is W / L = 18 μm / 18 μm. Hence, C_2 can be implemented by 16

unit capacitors and 16 × 16 unit capacitors for C_1. In the layout, the top (or bottom) plate of a unit capacitor is connected to the bottom (or top) plate of the adjacent ones to cancel the unequal parasitic capacitances from the top and bottom plates.

To save the silicon area, the capacitors are implemented by base-band devices, not by RF devices which usually come with a bulky guard rings. A total size for both C_1 and C_2, including all dummy capacitors and connections, is 400 μm × 440 μm.

5.5.3. Voltage Controlled Oscillator (VCO)

Figure 97 shows a schematic diagram of the VCO in this work.

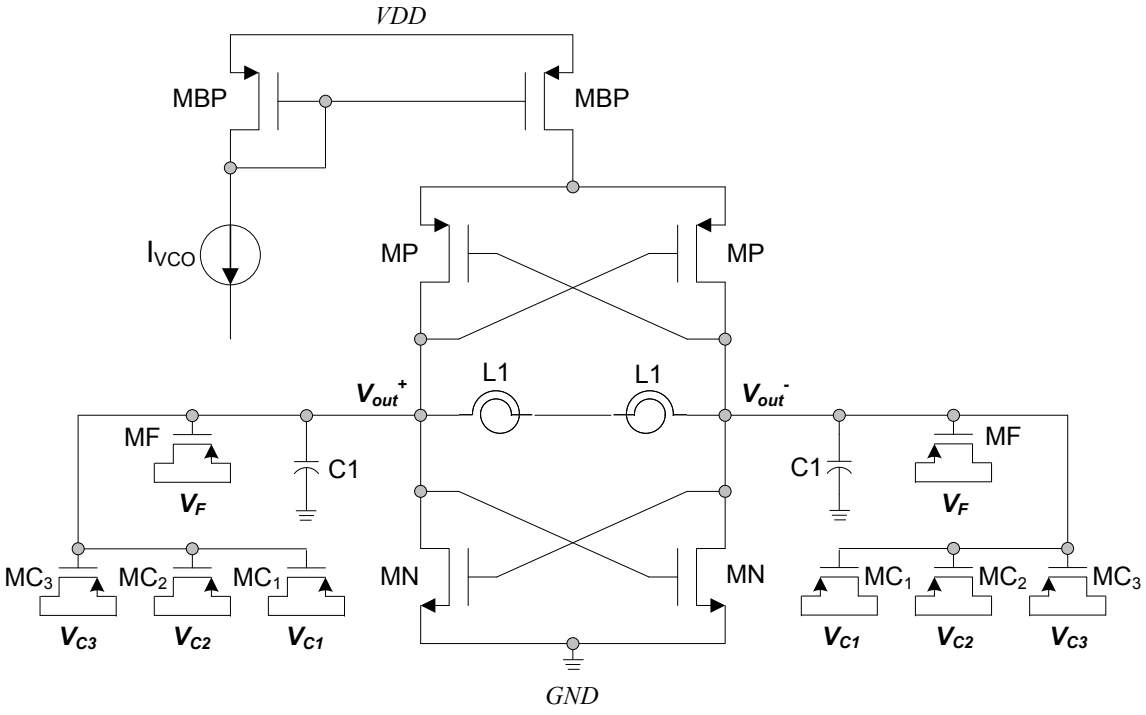


Figure 97. Schematic of a VCO.

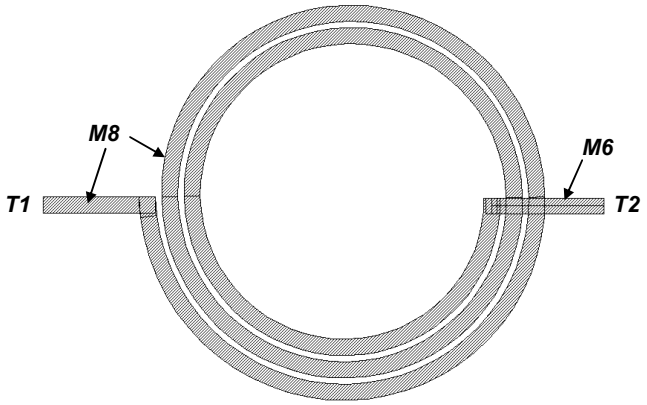
As discussed in a previous section 5.4, the target frequency range is 90 MHz (5.74 ~ 5.83 GHz) that is approximately 1.6 % of the minimum frequency of 5.74 GHz. In addition, since the purpose of this work is to demonstrate the improvement of the reference spur suppression, the phase noise at the 5 MHz (a reference frequency) of an offset frequency should be low enough. With the above requirements (narrow tuning range and low phase noise) enforce us to employ an LC oscillator rather than a ring oscillator. The VCO is implemented with a LC-tuned tank compensated by negative resistors as shown in Figure 97.

The inductor (L1) is implemented with a spiral CMOS inductor and designed parameters are listed in Table 7.

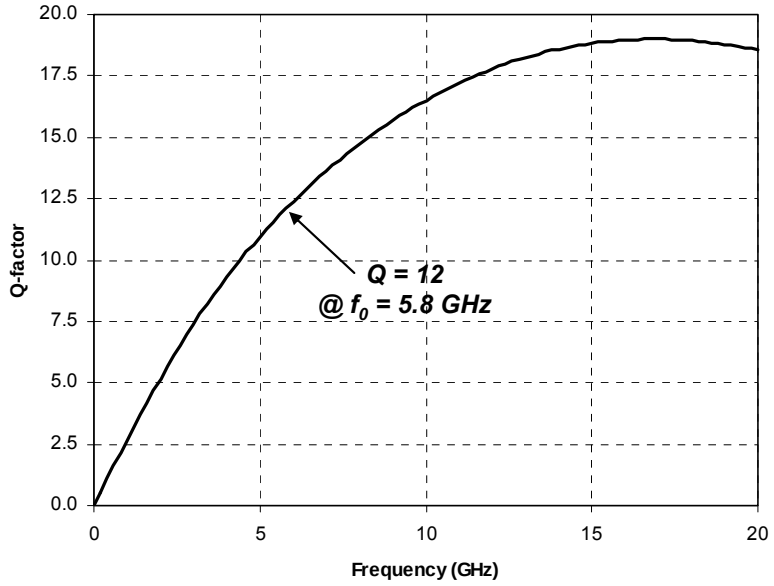
Table 7. Design parameters of L1 in Figure 97.

Metal layer	Metal 8
Inductance	0.9 nH
Q-factor (@ 5.8 GHz)	12
Outer diameter	100 μm
Metal width	4 μm
Metal space	1.5 μm
# of turns	2.5

It utilizes a special thick top metal (Copper with a thickness of 2 μm) with a circular shape for lower resistance and high Q-factor. Also, it is placed on nwell which is tied up *VDD* for better isolation from substrate noises.



(a)



(b)

Figure 98. A single-ended inductor (L1). (a) Layout view. (b) Simulated Q-factor.

In a differential VCO structure, it is better to use a differential version of an inductor for better matching. However, only single-ended version of inductors were available when this work is done. Figure 98 (a) is a layout view of the designed L1. A

common problem of a single ended inductor is the asymmetric parasitics between terminals. As shown in Figure 98, the underpass is tapped out using the metal layer which is 2-layer lower (M6) than the top metal (M8) at T2 side. Hence, T2 will experiences a cross-talk through parasitic capacitors. In order to solve this problem, a pair of single ended inductor is used where all asymmetric parasitics will be balanced with two separate inductors. However, using two separate inductors increases a silicon area. A designed inductance is 0.88 nH with the Q-factor of 12 at 5.8 GHz as shown in Figure 98 (b). A self resonant frequency of this inductor is predicted to be 45 GHz that is much higher than the operating frequency with a good safety margin.

Table 8. Design parameters of capacitors in Figure 97.

Device	Type	Capacitance	W	L
C1	MIM capacitor	244 fF	12.5 μm	12.5 μm
MF	PMOS varactor	30 ~ 80 fF	11 × 5 μm	1.5 μm
MC1	PMOS varactor	9 ~ 43 fF	2 × 5 μm	0.36 μm
MC2	PMOS varactor	18 ~ 80 fF	4 × 5 μm	0.36 μm
MC3	PMOS varactor	36 ~ 151 fF	8 × 5 μm	0.36 μm

Capacitors are breakdown to several pieces: a fixed MIM capacitor (C1), a PMOS varactor for a fine tuning (MF) and binary-weighted PMOS varactors for a discrete tuning (MC_1, MC_2 and MC_3). The type and values of capacitors are listed in Table 8.

PMOS varactor (MF) is used for a fine frequency tuning. The gate is connected to RF node of the VCO, and the bulk is tied up to *VDD*. Source/drain is connected

together with the control voltage coming from the loop filter. The DC level of the gate is set by a common-mode voltage on the differential output node of the VCO. The effective capacitance seen from the gate is varied by the voltage difference between the gate and the source/drian. Assuming 0.6 V of the gate voltage on the MF transistor, the designed capacitance is varied from 30 fF to 80 fF by adjusting the source/drain voltage from 0V to 1.3 V. MC1, MC2 and MC3 are PMOS varactor for discrete frequency tuning purposes. Their oxide size is binary weighted as shown in Table 8 yielding a total capacitance of these capacitor bank is controlled by 3-bit digital signals (*VC1/2/3*).

The simulation result of the designed VCO including the following buffer is shown in Figure 99. It shows 8 discrete tuning curves due to 3-bit digital control, and the target frequency range is located in the middle of tuning curves. An individual tuning curve provides a 2.6 % of tuning range satisfying the required frequency range (1.6 %) with a good margin. Also, the additional 3-bit discrete tuning curves extend the tuning range to 13.9 % which is large enough to account for process variations.

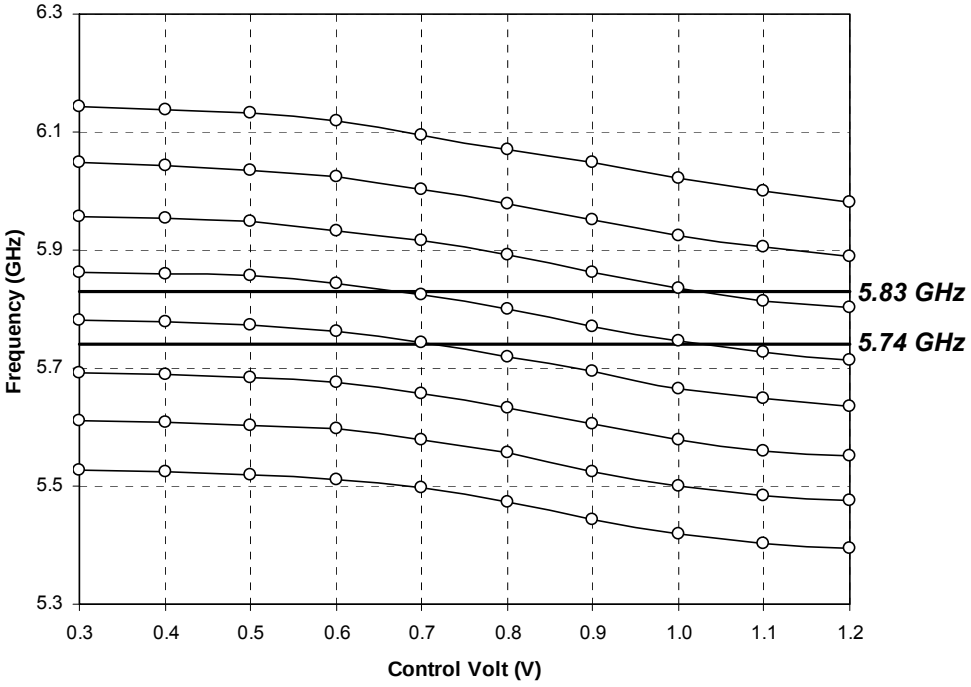


Figure 99. Simulated VCO frequency range.

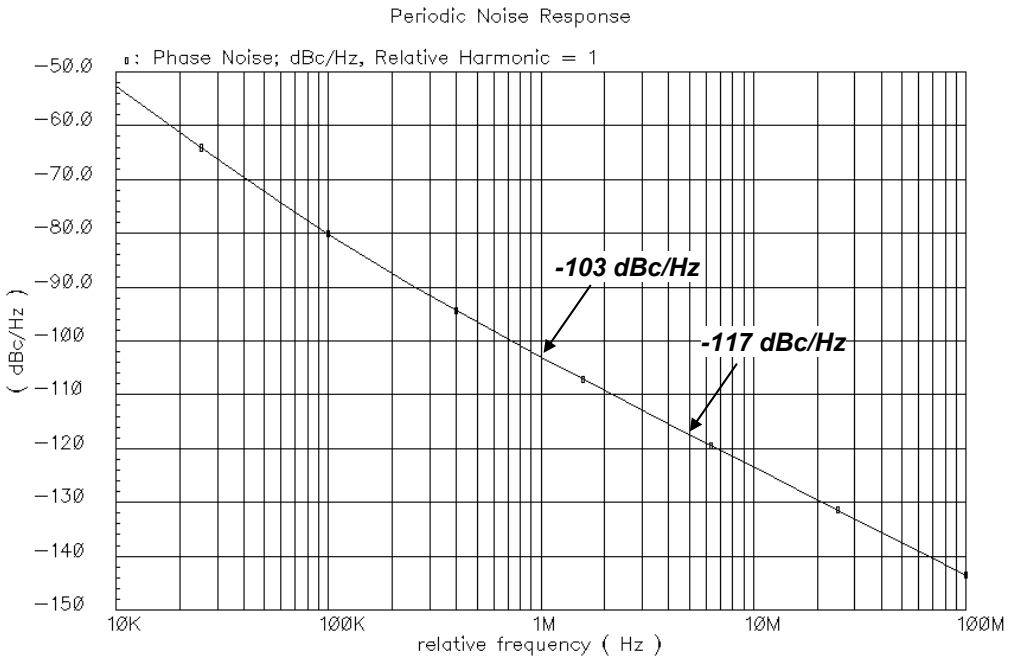


Figure 100. Phase noise simulation result.

Phase noise is simulated in the case when the oscillating frequency is 5.8 GHz and the result is shown in Figure 100. Phase noise simulation is performed using the periodic steady state (PSS) analysis in the spectreRF simulator. It yields -103 dBc/Hz at 1 MHz offset and -117 dBc/Hz at 5 MHz offset which is the reference frequency.

5.5.4. Programmable Integer-N Frequency Divider

Next the VCO, the following block is the frequency divider. It takes the high frequency VCO output and generates low frequency output signal. The dividing ratio of the input and output frequencies is defined as $N = f_{in} / f_{out}$ where f_{in} denotes the VCO output frequency and f_{out} is the divider output frequency. fout should be the same with the reference frequency f_{REF} so that the PFD can perform the phase comparison and the loop can be locked. Depending on the number type of the dividing ratio N, the architecture of the frequency divider is different. If N is a fractional number, the frequency divider is called the fractional-N divider. The fractional-N divider can perform the fractional-N dividing by taking the average the frequencies during the multiple cycles, and as a result, it generates spurs at lower frequencies. To suppress fractional spurs, it adopts the sigma-delta modulator for the frequency control. The sigma-delta modulator generally pushes the quantization errors into higher frequencies yielding the suppression on fractional spurs. The fractional-N divider can provide high resolution output by the fractional dividing, and give the flexibility for the designers. But, it requires a complicated structure and large power consumptions due to the sigma-delta

modulator. Therefore, an integer-N frequency divider is preferred when all possible dividing factors are integer numbers.

The pulse-swallow frequency divider is the most popular structure in integer-N frequency dividers, and the block diagram is shown in Figure 101 [78].

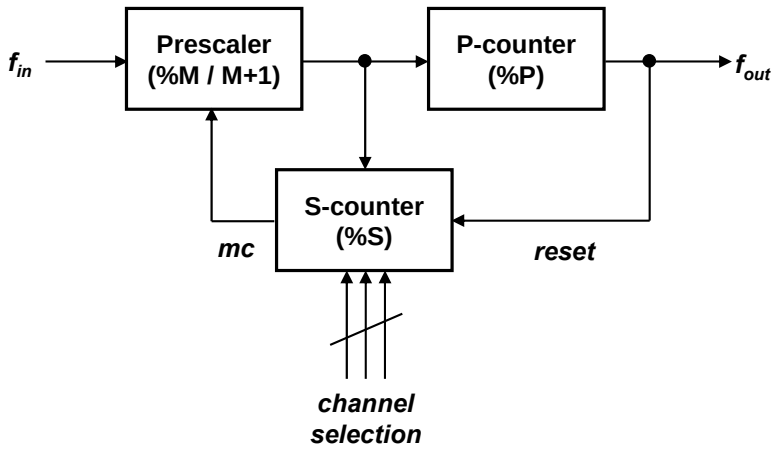


Figure 101. Pulse-swallow frequency divider.

It consists of a prescaler, a program counter (P-counter) and a swallow counter (S-counter). The prescaler deals with the highest frequency signal coming out of the VCO, and divides the input frequency by M or M+1 depending on the status of the modulus control (*mc*) bit. The P-counter divides the prescaler output frequency by fixed P, and its output is the final divider output. When the P-counter counts a complete P cycles, it initialize all counters and the divider block starts its operation again. The S-counter also divides the prescaler output frequency by S, and when it counts S cycle, it generates the output *mc* controlling the dividing factor in the prescaler. The number S is

set by the channel selection bits. The frequency divider shown in Figure 101 operates as follows:

(1) Assume that the count number P is always bigger than the count number S (P > S).

(2) The prescaler starts with the modulus of M+1.

(3) The S-counter counts the number of cycles in the prescaler output. When it counts S cycles, it enables mc bit and the prescaler changes its modulus to M.

(4) The P-counter also counts the number of cycles in the prescaler output. When it counts P cycles, it reset all counters and the overall operation of the entire divider block is repeated.

From above observations, the required number of cycles at the divider input is calculated as the sum of two phases: (M+1)×S (during *mc* = 0) and M×(P-S) (during *mc* = 1). Therefore, the total dividing factor N is (M+1) ×S + M×(P-S) = M×P + S, as depicted in Figure 102.

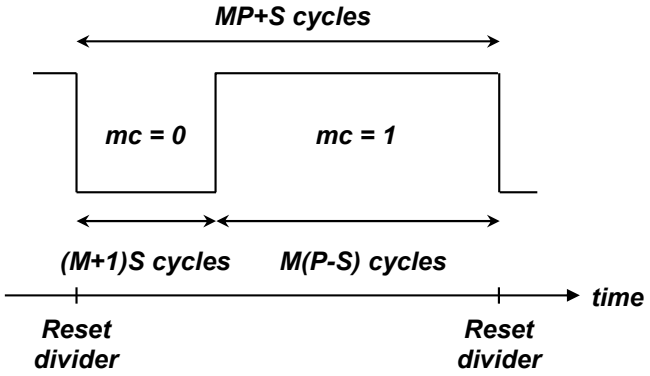


Figure 102. Waveform of the modulus control (*mc*) bit.

In this work, the reference frequency is 5 MHz, and the minimum and maximum output frequencies are 5740 MHz and 5830 MHz, respectively. Hence, the required N is varied from 1148 (= 5740 % 5) to 1166 (= 5830 % 5). The range of N is 18 indicating the channel selection should be at least 5 bits. The modulus of the prescaler is determined to be 7 (M = 7), and the factor of the P-counter is also determined to be 162 (P = 162). As a result, the factor of the S-counter would be from 14 to 32. Table 9 summarizes the results.

Table 9. Designed parameters in the frequency divider in Figure 101.

Device	Type
f_{in}	5730 MHz 5830 MHz
f_{out}	5 MHz
N	1148 1166
M	7
P	163
S	7 25

The prescaler is a dual-modulus divider and it takes the VCO output as an input. A dual-modulus of %7/8 is implemented by the %3/4 block followed by the additional %2 block and a control logic as shown in Figure 103.

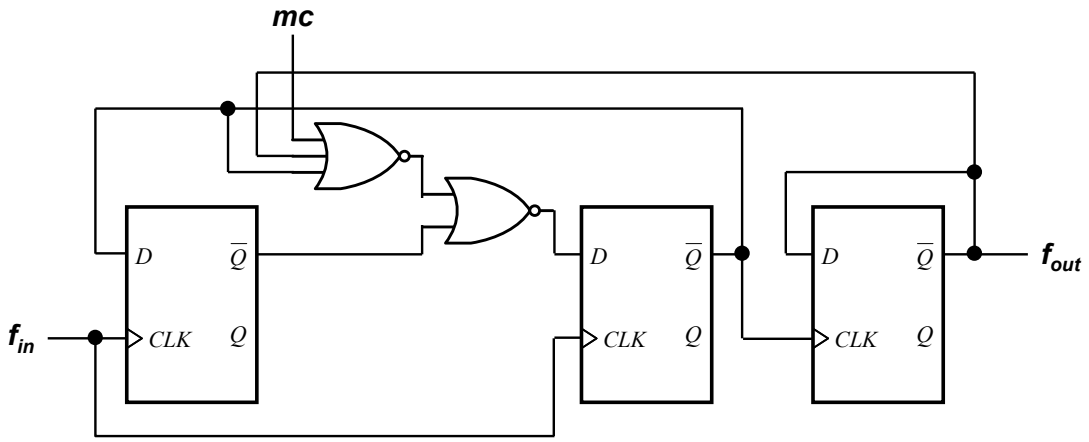


Figure 103. Prescaler block diagram.

The prescaler in Figure 103 performs the frequency division by 8 when *mc* = 1, and it changes the division factor to 7 when *mc* = 0. Since D-type flip-flops should be incorporated with the high frequency VCO output, they are implemented by a current-mode logic (CML) structure. A CML topology provides a fast operation at the cost of high power consumption.

Both P-counter and S-counter can be built by static logic gates since they are working with low frequency signals. The P-counter consists of an 8-bit ripple counter to account for P = 162 and a control logic for the initializing since P is not power of two number. The S-counter takes the channel selection bits as an input and sets the number S by using several logic circuits.

5.5.5. Lock Detector

A block diagram of the lock detector is shown in Figure 104. Two DFFs at the input compare the phase error of V_{REF} and V_{DIV}, and V_1 becomes high when the phase error is within the error windows set by the pre-defined delay T_d. V_1 is fed into the following 8-bit counter clocked by V_{REF}, and LCK is changed to be high if V_1 maintains as high during 8 reference cycles. A multi-bit counter prevents the false alarm when the phase error is within error window during the frequency acquisition. If the phase error becomes bigger than the pre-defined error, then V_1 goes low and the counter is immediately reset yielding $LCK = 0$ without waiting 8 reference cycles.

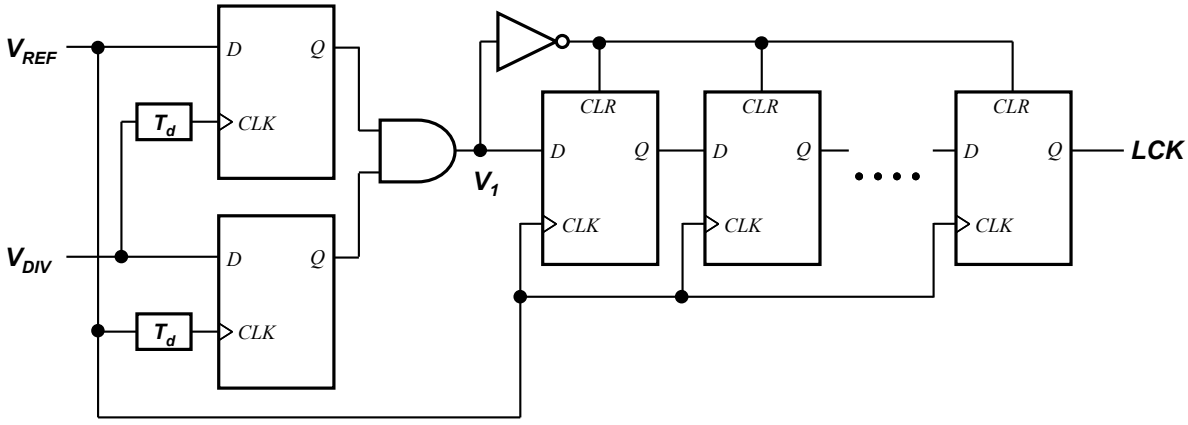


Figure 104. Lock detector block diagram.

5.6. Testing and Measurements

5.6.1. QFN Package and PCB Design

The proposed frequency synthesizer shown in Figure 94 was designed and implemented. The chip was fabricated in 8-metal double-poly UMC 0.13 μm technology through the UMC university program. The chip occupies a die area of 1.86 ×1.2 mm^2, and the active area is 0.34 mm^2. The frequency synthesizer consumes 9mW with a 1.3 V power supply under the normal operation.

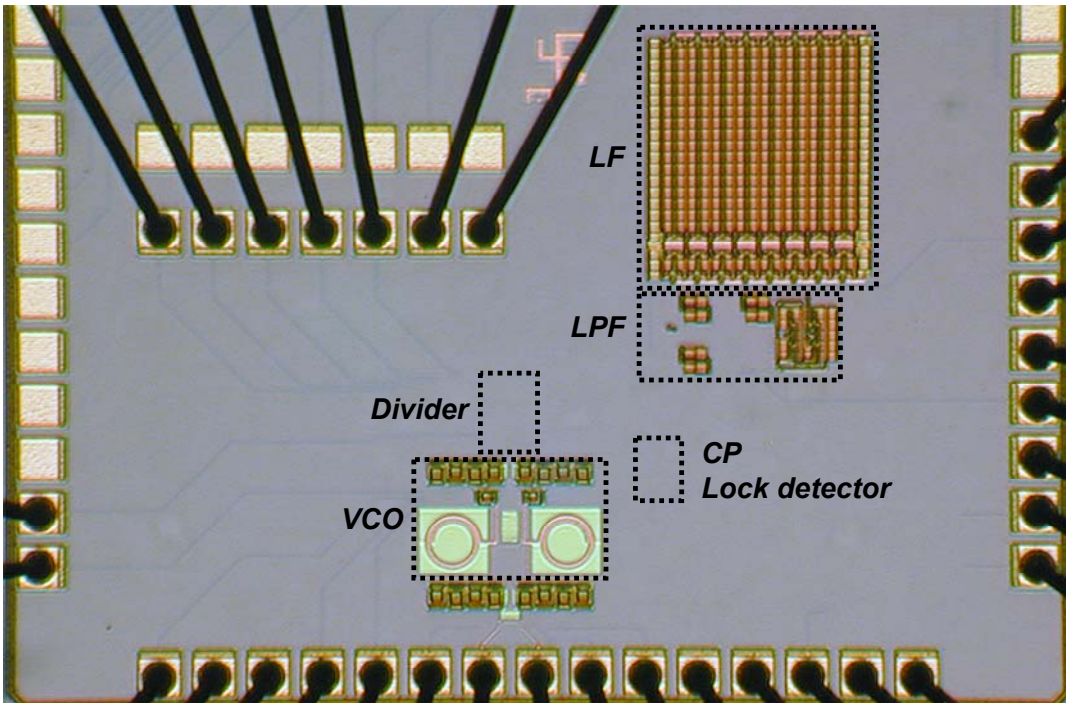


Figure 105. Chip micro photograph.

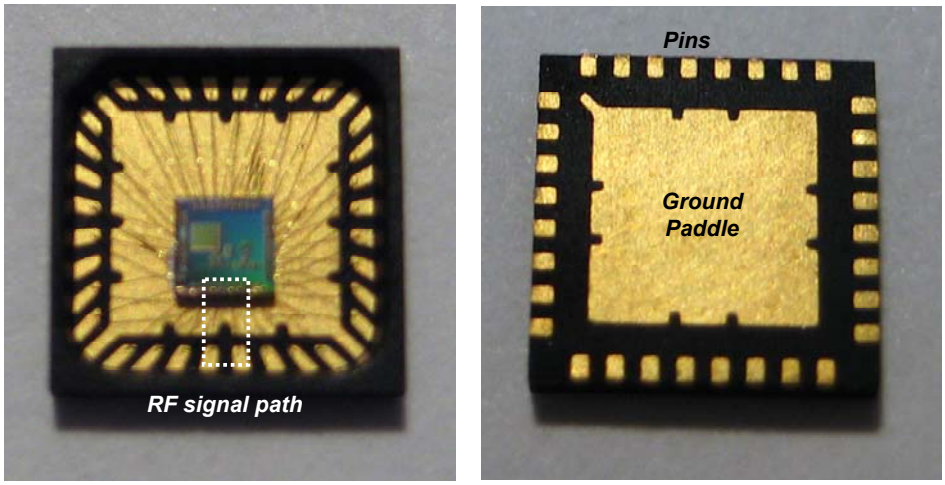
The chip micro photograph is shown in Figure 105. Each building block is labeled since they are not visible except for the top metal layer from the top due to the automatic dummy metal filling that is done during the fabrication.

The VCO is a LC oscillator operating at 5.8 GHz frequency band and two separate single-ended inductors are used for an inductor part. The VCO is followed by an open-drain buffer that converts the VCO output voltage waveform to the current. The output current is then converted again to the voltage waveform through the external balun which drives the 50 Ω spectrum analyzer. The open drain buffer is preferred since the current is immune to the parasitic effect on the bonding wires rather than the voltage. The length of the RF signal path through the VCO, buffer and pad is designed as short as possible to minimize the loss and the cross-talk with other signals.

The frequency divider is also placed closed to the VCO block because the front-end of the divider (prescaler) works at a RF frequency. The rest of the divider block (P-counter and S-counter) is considered as a baseband block and they are not as sensitive to the signal path length as other RF blocks. Also, the PFD, lock detector and charge pump blocks are placed together. The capacitors C_1 and C_2 in the loop filter are 128 pF and 8 pF, respectively. They are implemented as on-chip capacitors using MIM capacitor, and occupy 0.17 mm^2 of die area.

The designed circuit is encapsulated using QFN-56 open cavity package. It has 56 pins and a lead pitch is 0.5 mm and, a body size is 8 mm x 8 mm. The photo of QFN-32 package is shown in Figure 106. The advantage of the QFN package is that is capable of working up to several GHz due to small parasitics compared to other packages. As

seen in Figure 106, QFN package also provides a ground paddle which is a big metal area connecting inside and outside of the package, and the impedance through the paddle is very low.



(a) (b)

Figure 106. QFN package. (a) Top view. (b) Bottom view.

The ground paddle allows multiple bonding wire connections which can minimize the bonding wire parasitic effect as the multiple wires can be connected in parallel. For the connection to the PCB, the QFN has surface-mounted type pins under the package without the external leads. The chip can be place in such a way that RF signal path can be shortened as shown in Figure 106 (a). A location of the chip is moved down from the center and the pads those carry RF signal are close to the edge so that the length of the associated bonding wires can be minimized.

The PCB was designed and fabricated for the measurement of the frequency synthesizer chip. The picture of PCB is shown in Figure 107. It includes a low-voltage regulator block with NCP565 linear regulator chip that can generate DC voltage down to 0.9 V. To improve the isolation between the building blocks, three separate regulator circuits are used to provide dedicated VDDs to the analog block, the digital block and the RF block. The length of the RF signal path from the package and a balun to SMA connector is designed to be as short as possible, which helps to minimize the loss and prevent the coupling from any other noise sources to the RF signal path.

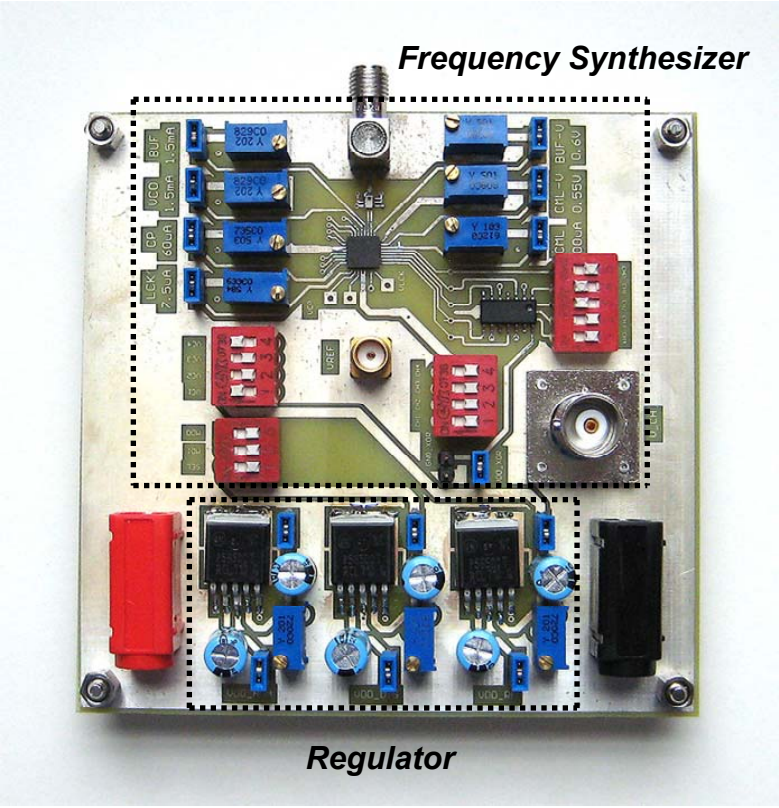
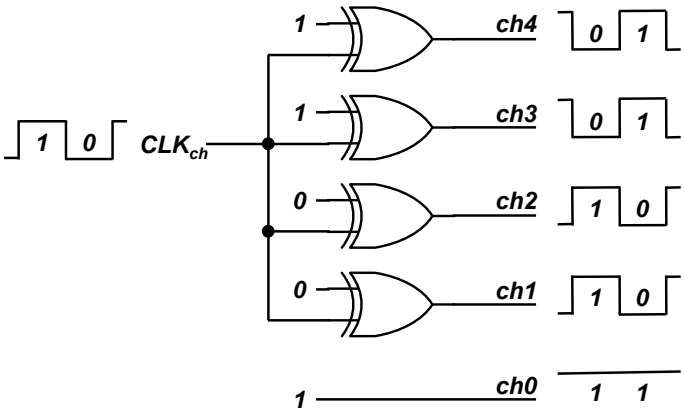


Figure 107. PCB for the frequency synthesizer chip testing.

A RF balun converts the differential signals to a single-ended signal and provides a 50 Ω output impedance on the unbalanced port which drive a 50 Ω spectrum analyzer. For a balanced port, it has a center tap connected up to *VDD* to bias the open drain buffer. In this work, TDK HHM1570 is used for a RF balun. It is a surface mount device (SMD) type multilayer balun, and covers the frequency range of 4.9 GHz ~ 5.95 GHz with less than 0.5 dB of insertion loss.

A reference clock is applied through a SMA connector, and it is placed close to the chip to minimize spurs. Since a reference clock path usually carries a large swing signal, it should be isolated from any other sensitive signal, e.g. the VCO control voltage signal.

The channel selection bits are generated using the multi-bit discrete switch. A required channel selection number can be defined manually by connecting associated bits to *VDD* or *GND*. This works well in the measurement with a fixed channel selection number. However, if we want to measure the settling time, the channel selection bits should be changed between the maximum and minimum channel number automatically. It can be done by applying the additional low frequency clock whose period should be long enough than a frequency synthesizer's settling time.



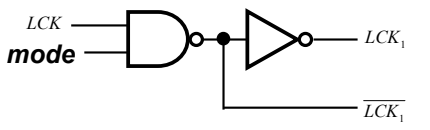
CLK_{ch}	S	fout
1	00111 (= 7)	5.74 GHz
0	11001 (=25)	5.83 GHz

Figure 108. Generation channel selection bits with 4-bit XOR for the settling time measurement.

According to Table 9, the minimum and maximum channel numbers (S) are 7 and 25, corresponding to 00111 and 11001 in binary numbers, respectively. As shown in Figure 108, channel selection bits can be generated by employing the external clock (CLK_{ch}) and setting the XOR input. When CLK_{ch} = 1, the channel selection number bit is 7 (= 00111, in binary), and 25 (= 11001) when CLK_{ch} = 0. On the PCB, a 4-input XOR gate is used with a 5-bit switch to preset the needed numbers. The clock CLK_{ch} is applied to a BNC connector.

5.6.2. Measurement Setup

A designed frequency synthesizer has two operation modes depending on the status of the adaptive LPF. As seen in Figure 109, the selecting mode is done by either bypassing lock detector outputs or disabling them.



mode	LCK_1	Operation
0	0	Conventional
1	LCK	Proposed

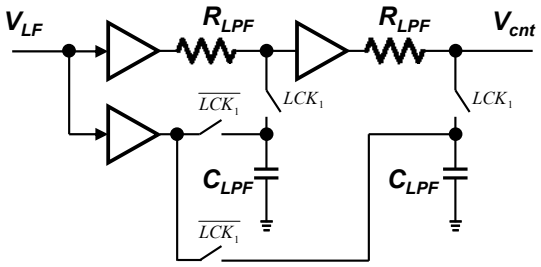
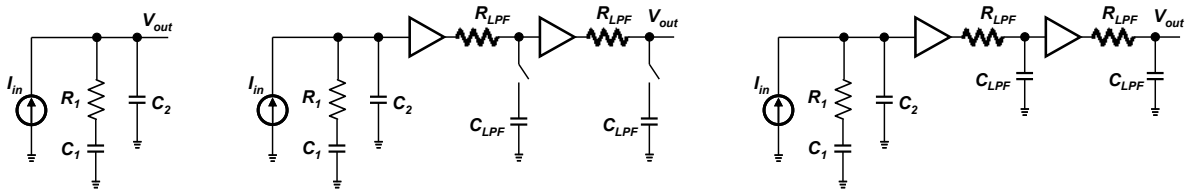


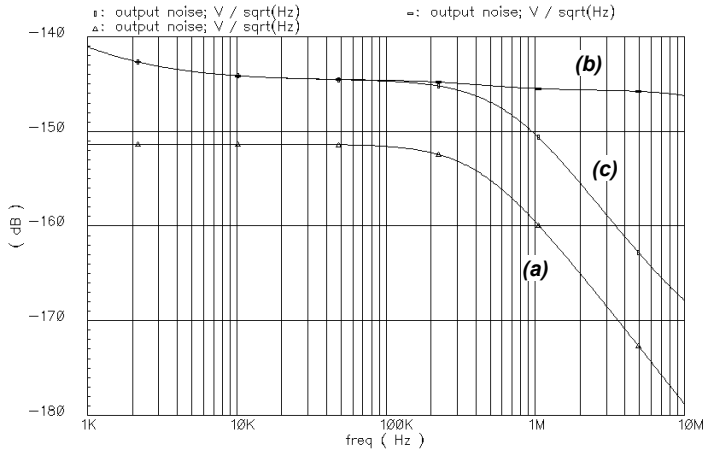
Figure 109. Operation mode of a frequency synthesizer.

When *mode* = 0, LCK_1 is always 0 and C_{LPF} is disconnected from R_{LPF}. In this conventional mode, V_{cnt} follows V_{LF} and the frequency synthesizer would work as a conventional type-II third order PLL. However, comparing to the real conventional PLL where V_{LF} is bypassed to V_{cnt}, two buffers and resistors (R_{LPF}) existed on the signal path resulting in the additional noise. On the other hand, when *mode* = 1, the additional LPF is adaptively controlled by *LCK* and the frequency synthesizer works as a proposed mode. To evaluate the added noise due to the buffers and resistors, a noise simulation was performed in three different configuration using spectreRF in three different modes.

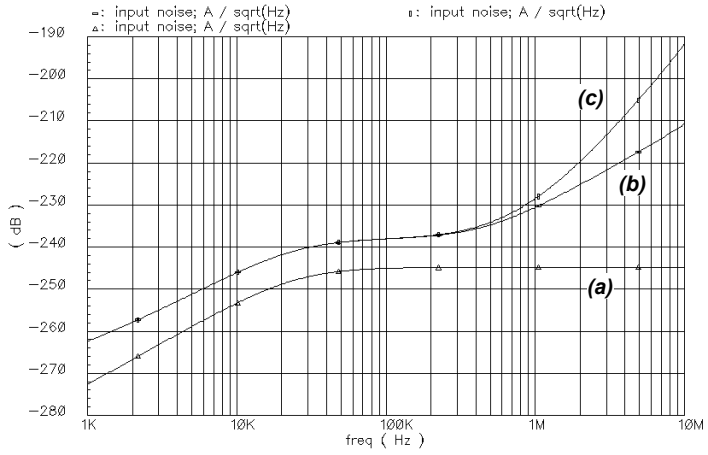
Seen from Figure 110, (a) is an original LF only case, (b) is a conventional operation mode and (c) is a proposed mode. Although C_{LPF} is adaptively controlled by *LCK* in a proposed mode, C_{LPF} is assumed to be connected in this simulation because phase noise is the PLL behavior in locked status. The total output noise is plotted in Figure 110 (d). In case of (a) and (c), total noise is band-limited due to the poles, while the noise from R_{LPF} is not band-limited in case of (b). Both (b) and (c) has 8 dB higher noise than (a), and a flicker noise from the buffer is seen below than 10 KHz.



(a) (b) (c)



(d)



(e)

Figure 110. Noise simulation results of the loop filter and the additional LPF. (a) LF only. (b) Conventional mode. (c) Proposed mode. (d) Output noise. (e) Input referred noise.

To understand the effect of these noises, the output noise is referred to the input current source and plotted as the input referred noise in Figure 110 (e). (b) and (c) still maintains 8 dB higher noise than (a) below than the loop bandwidth (100 KHz in our case). The difference between (b) and (c) in higher frequency will not affect the VCO output phase noise since it is out of the loop bandwidth and will be filtered out.

5.6.3. Measurement Results

First, the free running VCO frequency is measured by forcing its control voltage by an external voltage source. The frequency is measured within entire tuning voltage range and varying all combinations of discrete tunings.

The measurement result turns out that the VCO frequency band is shifted down by 18 % compared to the post layout simulation. This is due to the underestimation of all parasitic inductances as well as capacitances in the simulation. The measurement result is plotted and compared with the simulation result in Figure 111. The lowered VCO free running frequency enforces us to adjust a reference frequency so that the PLL can be locked. As a result, the reference frequency is set to 4.48 MHz instead of 5 MHz, and the improvement of spur suppression would be decreased than the expectation since the reference frequency is decreased.

The VCO output spectrum is measured by the spectrum analyzer and plotted in Figure 112. The carrier frequency is measured as 5.11 GHz and a reference spur is seen at 4.48 MHz offset frequency from the carrier frequency. The proposed frequency

synthesizer improves the spur suppression by 20 dB over the conventional mode. The improvement was expected as 28 dB in Figure 93 (b), and is decreased due to the lower reference frequency.

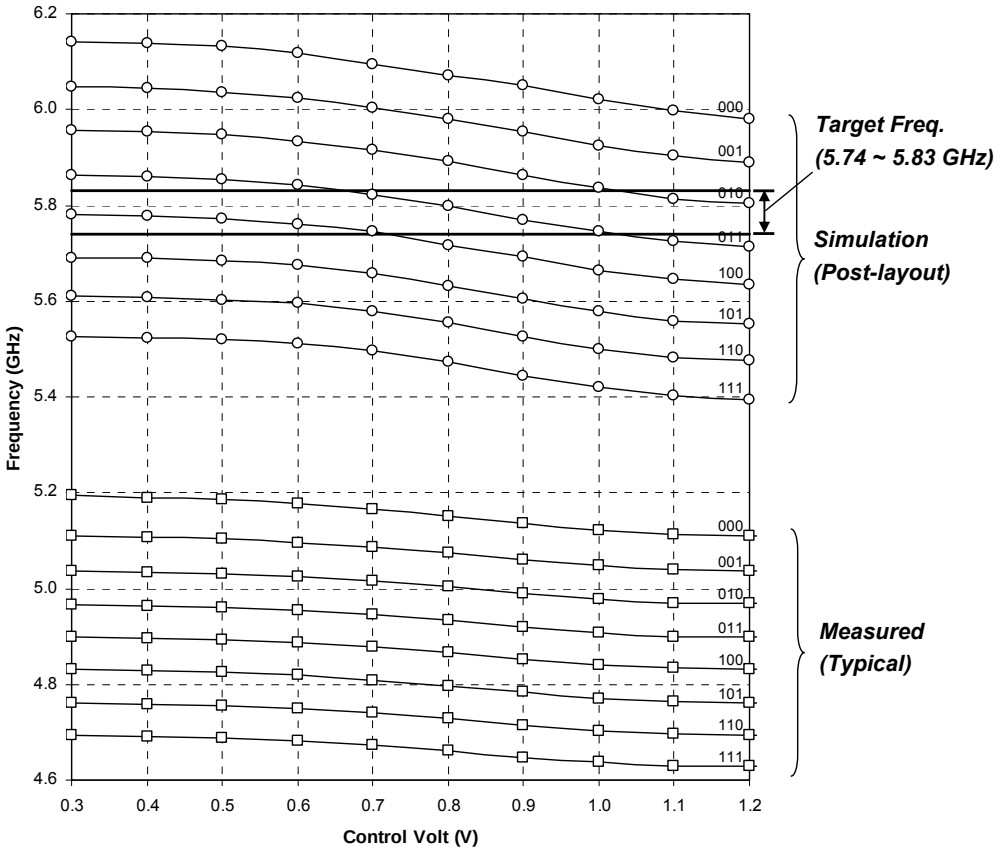
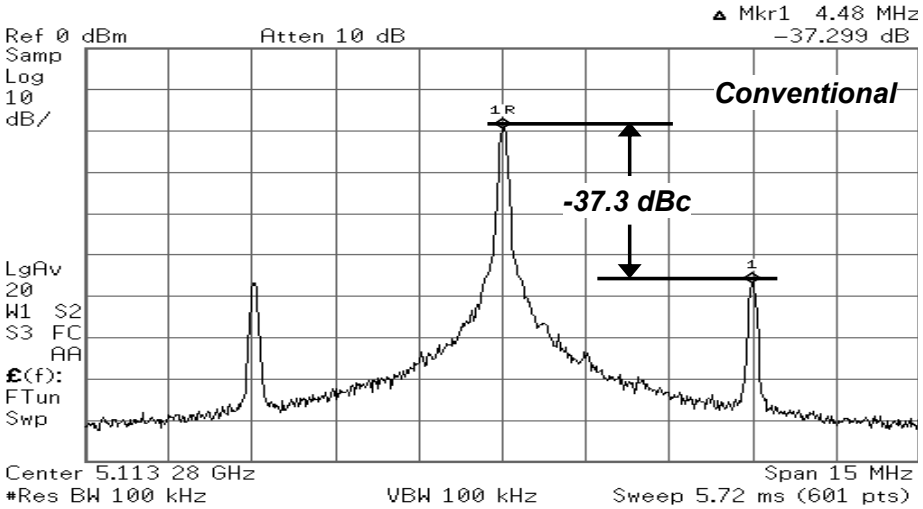


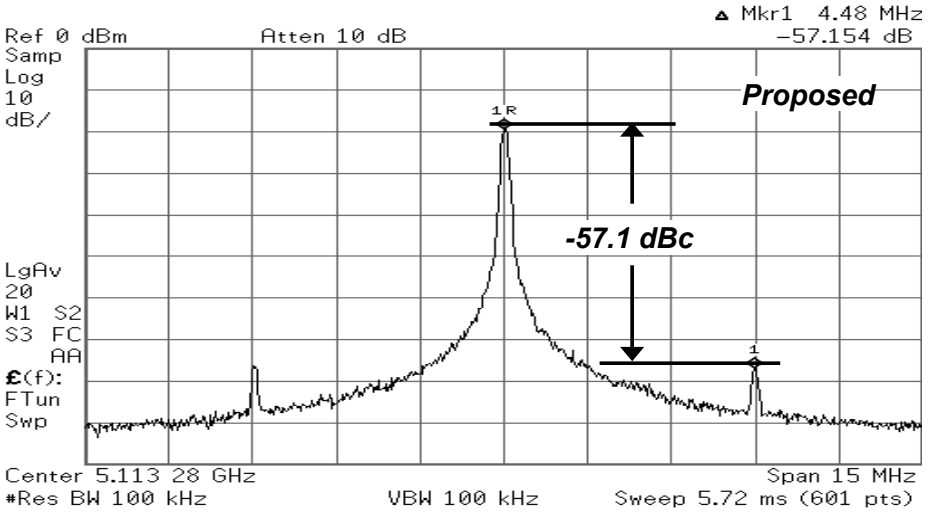
Figure 111. VCO free running frequency.

A locking transient behavior is measured using the oscilloscope, and the result is shown in Figure 113. Before the *LCK* signal becomes high, the proposed frequency synthesizer exhibits the same behavior with the conventional one including the

overshoot. After *LCK* goes high, the loop response shows the higher order system. The settling time is measured as 40 μs and 44 μs in the conventional and proposed synthesizers, respectively. The settling time in the proposed one is increased by 10 % .

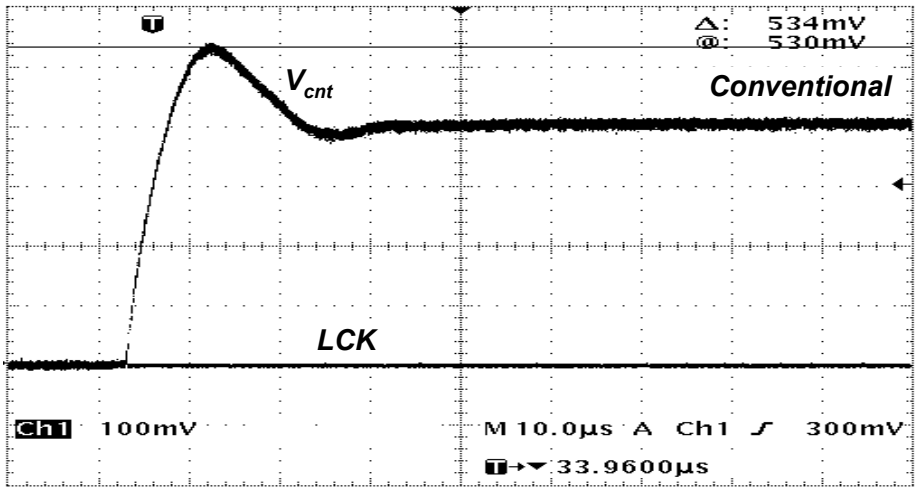


(a)

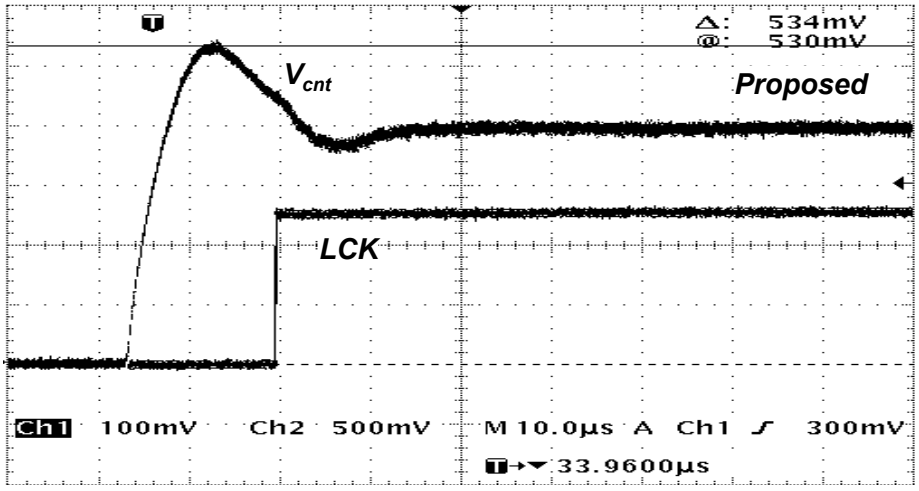


(b)

Figure 112. Measured 5.11 GHz frequency spectrum. (a) Conventional. (b) Proposed.

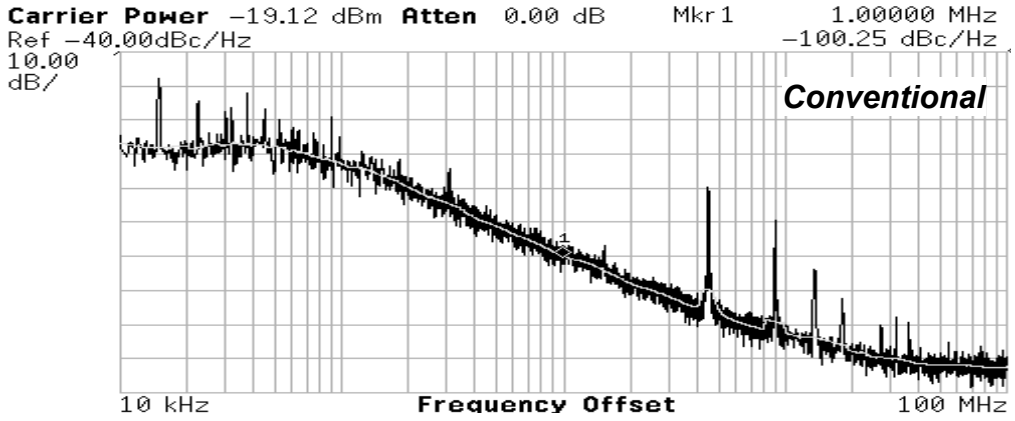


(a)

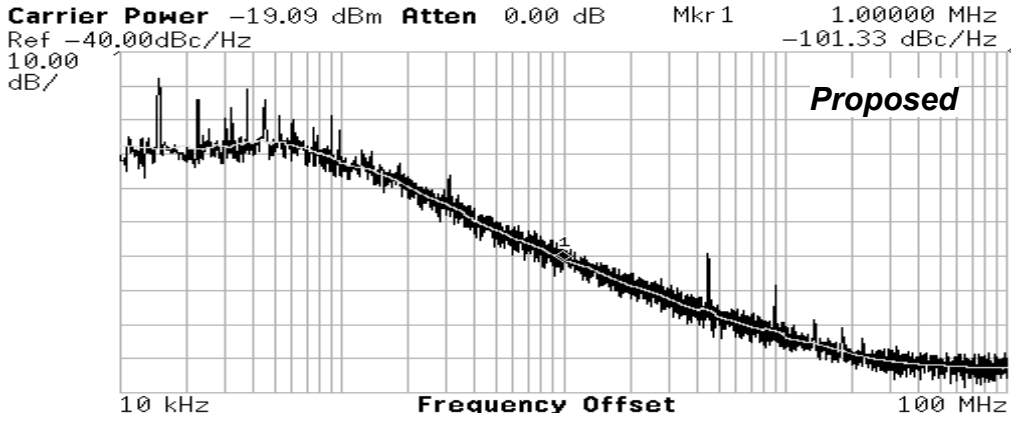


(b)

Figure 113. Locking transient behavior. (a) Conventional. (b) Proposed.



(a)



(b)

Figure 114. Phase noise of the PLL in locked status. (a) Conventional. (b) Proposed.

Phase noise in locked status is measured and plotted in Figure 114. At 1 MHz offset, phase noise difference on both frequency synthesizers is 1 dB. It can be known that the proposed frequency synthesizer does not add a significant phase noise out of the loop bandwidth. Phase noise within the loop bandwidth (in-band phase noise) might be different as expected in Figure 110, but it is not accurately measured due to the accuracy limitation of the equipment.

Table 10. Performance summary and comparison with other published solutions.

	This Work (Proposed)	This Work (Conventional)	[85]	[89]	[90]	[82]
Frequency (GHz)	5.11 ~ 5.19	5.11 ~ 5.19	4.8	5.23 ~ 6.16	4.9 ~ 5.95	5.14 ~ 5.7
Phase noise (dBc/Hz)	-101 @1 MHz	-100 @1 MHz	-104 @1 MHz	-113 @1 MHz	-110 @1 MHz	-116 @1 MHz
Spur (dBc)	-57 @4.48 MHz	-37 @4.48 MHz	-55 @1 MHz	-74 @20 MHz	-66 @40 MHz	-70 @10 MHz
Settling time (μs)	44	40	--	76	--	100
Power (mW)	9	9	18	36	--	13.5
Process	0.13 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.25 μm CMOS

The measurement results are summarized and compared to the other published works in Table 10. The proposed technique improves the suppression of a reference spur by 20 dB over the conventional frequency synthesizer. In Table 10, and [90] do not specify the settling time which plays a role in the spur suppression. This is because the longer settling time means the lower loop bandwidth resulting in the better spur suppression. Also, the reference frequency is important to compare the spur suppression performance. The higher reference frequency is more suppressed because it becomes far

from the loop bandwidth. Considering the settling time and the reference frequency, the spur suppression of the proposed technique is better than the other works in Table 10.

5.7. Further Improvement

Although we have demonstrated that the proposed adaptive lowpass filtering technique improved the reference spur suppression, the magnitude of a reference spur is still not impressive compared to other works. This motivates the further improvement of the frequency synthesizer design.

5.7.1. The Proposed Architecture

Figure 115 shows the block diagram of the proposed frequency synthesizer. There are several modifications from the previously proposed design shown in Figure 94. V_{CLK} is the master clock whose frequency is 4 times higher than the reference frequency. V_{REF} is the reference clock and is generated by the frequency divider block (%4), and V_{DIV} is the divider output. The pulse interleaver is introduced at the front-end, and the PFD takes the inputs, selected by the lock detector output (*LCK*), from either the pulse interleaver outputs or bypassed the original signals (V_{REF} and V_{DIV}). The buffer between two R_{LPF}s in the adaptive LPF is removed to decrease the coupling through the power supply of the buffer.

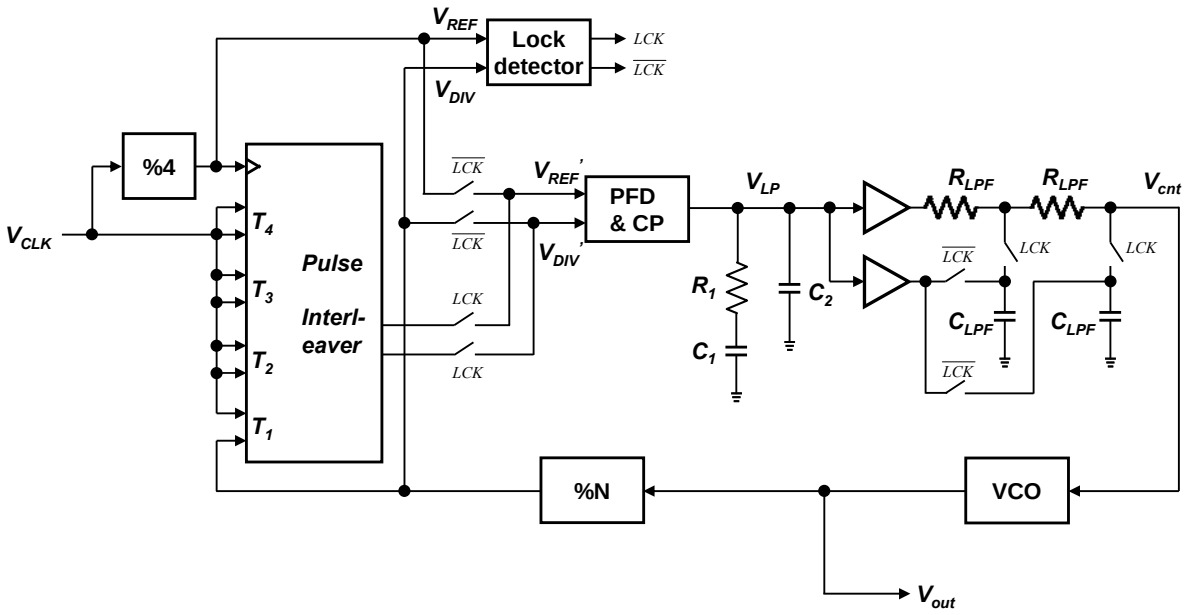


Figure 115. Block diagram of the proposed frequency synthesizer.

5.7.2. Pulse Interleaver

As shown in Figure 99 (b), reference spurs are suppressed by the loop that exhibits the low pass filtering behavior. It indicates that the amount of suppression is affected by the reference spur frequency as well as the loop order and, higher reference frequency will give more suppression. However, the maximum reference frequency is limited by the system specification such as the minimum channel space. The previous work [85] proposed the distributed PFDs/CPs with N-delayed paths. Using this technique, the effective frequency of the ripples on the control voltage of a VCO hence, spurs are more suppressed by the loop filter.

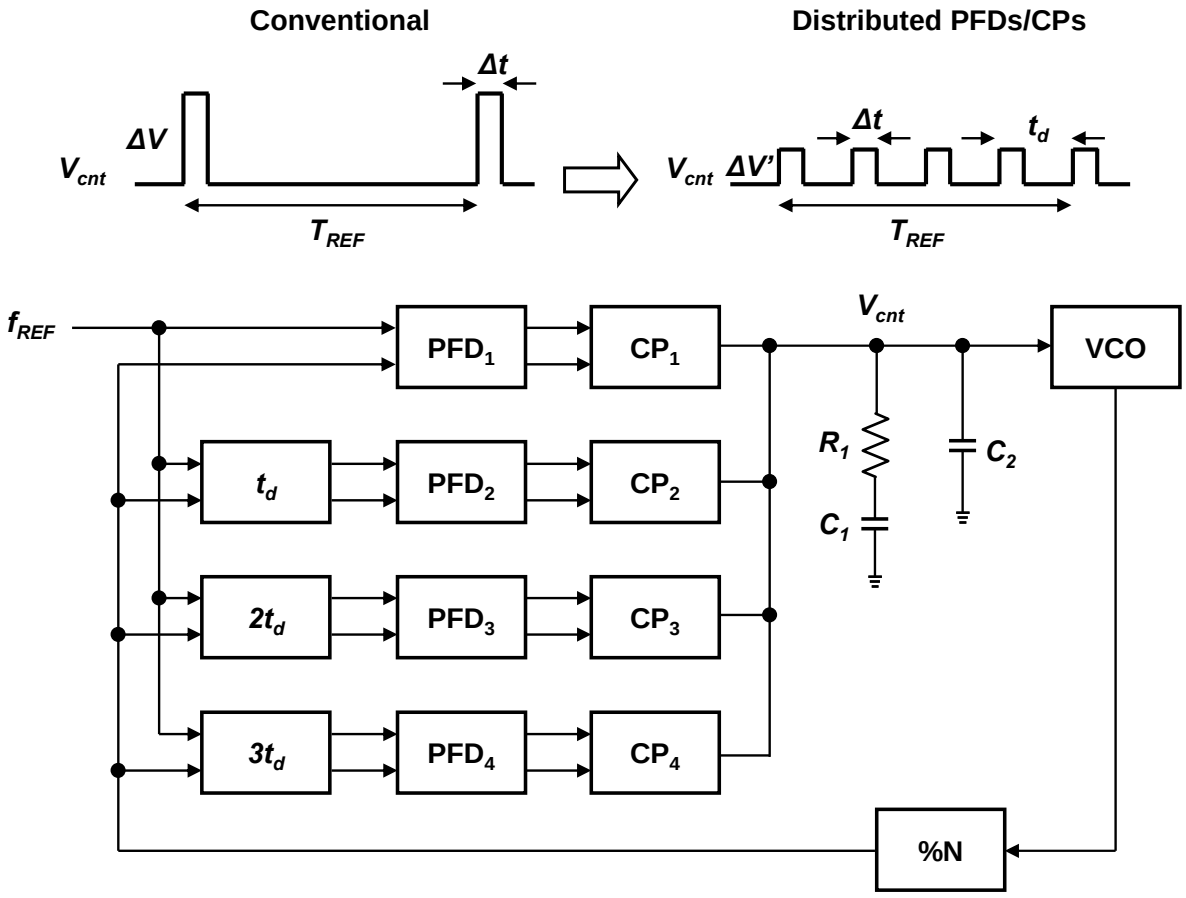
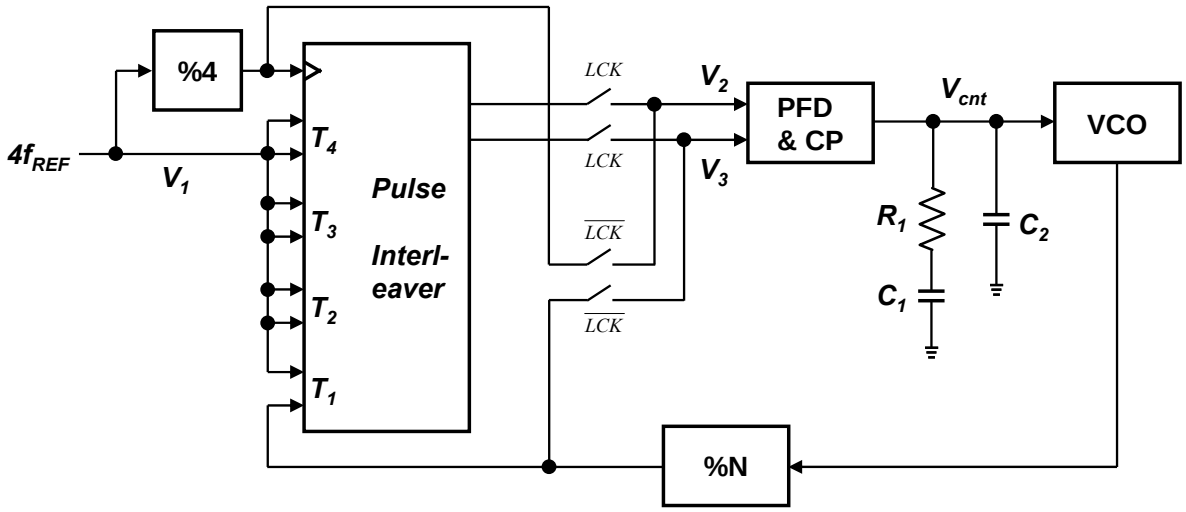


Figure 116. Integer-N frequency synthesizer with distributed PFDs and CPs.

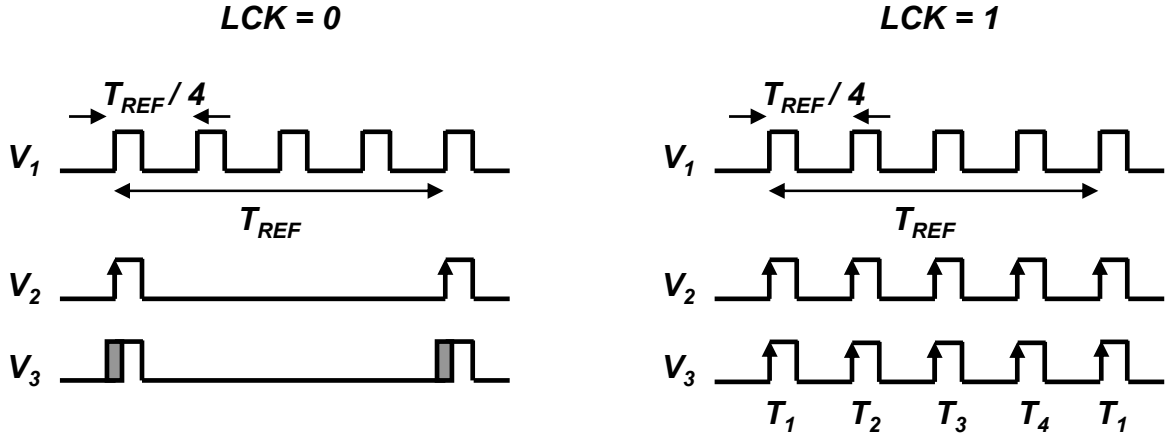
Figure 116 is an integer-N frequency synthesizer with distributed PFDs and CPs when the number of delayed paths is 4. In this case, t_d should be set to $T_{REF} / 4$ and, the effective frequency of V_{cnt} becomes 4 times higher than the conventional case. Δt is determined by the non-idealities of PFD and CP as discussed in the section 5.2.2. Due to the low pass filtering of the loop filter, the amplitude of V_{cnt} ripple reduced from ΔV (conventional) to $\Delta V'$ (distributed PFDs/CPs). However, this technique suffers from non-accurate t_d and the mismatches between different paths such as delays in PFDs and gains

of CPs, resulting in only 3 dB improvement of the spur suppression over a conventional frequency synthesizer from measurement results [85].

To overcome these implementation difficulties, the technique of the pulse interleaving in time-domain is proposed. A block diagram employing *Pulse Interleaver* in an integer-N frequency synthesizer is shown in Figure 117 (a). When $LCK = 0$, the whole loop operates like the conventional loop. After loop is locked and *LCK* becomes 1, the *Pulse Interleaver* path is active and the frequency of V_{cnt} becomes multiplied by 4 yielding the smaller amplitude than the conventional case. The operation of *Pulse Interleaver* can be explained with voltage waveforms in Figure 117 (b) and (c). During the transition, the phase of V_3 (the output of a divider) is controlled by the loop and keeps changing. After the loop is locked in phase, the rising edge of V_3 is aligned with that of the master clock (V_1) and both edges are taken by *Pulse Interleaver* in T_1 phase. In other phases (T_2, T_3 and T_4), the rising edge of V_1 is taken and fed to the PFD input. Since both inputs of the PFD come from the same V_1, the phase error is zero, which emulates the locked state.



(a)



(b) (c)

Figure 117. Proposed pulse interleaver incorporated *LCK* signal. (a) Block diagram of an integer-N frequency synthesizer. (b) Waveforms of V_1, V_2 and V_3 when *LCK = 0*. (c) Waveforms of V_1, V_2 and V_3 when *LCK = 1*.

If, in locked state, the phase error between the divider output and V_1 is zero, a frequency spectrum at f_{REF} is perfectly cancelled and transferred to at $4f_{REF}$. However,

there may be a finite phase error due to various noise sources even though the phase error is suppressed by the whole loop gain in locked states, giving the non-zero power on the frequency spectrum at f_{REF}. This is depicted in Figure 118 where a charge pump output current (I_{CP}) rather than V_{cnt} is plotted to exclude the frequency-dependent filtering effect on the loop filter.

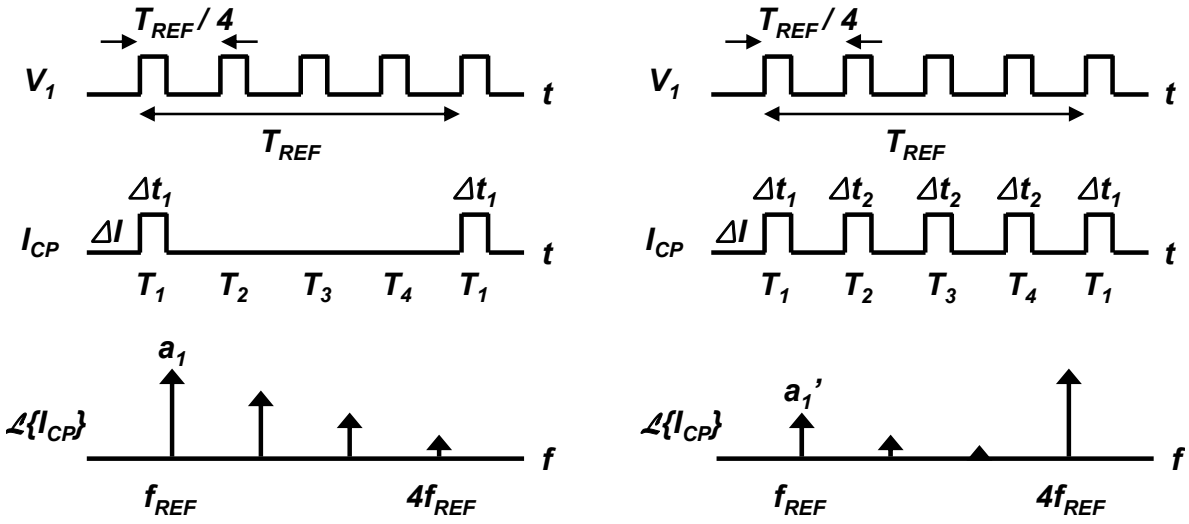


Figure 118. Waveforms of V1 in Figure 117 (a), charge pump output current and its frequency spectrums. (a) Conventional. (b) Proposed.

In Figure 118 (a), I_{CP} has a pulse width of Δt_1 that includes a finite non-zero phase error between the reference and divider output signals. ΔI is a lumped model including all non-ideal effects in the PFD and CP. Frequency spectrums of I_{CP} has a fundamental tone at f_{REF} and its magnitude a_1 can be calculated as

$$a_1 = \frac{2\Delta I}{\pi}\sin\left(\frac{\pi\Delta t_1}{T_{REF}}\right) \tag{5-11}$$

Figure 118 (b) depicts the case when the proposed *Pulse Interleaver* is used. Δt_2 represents the lumped error in the PFD and CP when the phase error is zero and, Δt_1 is appeared at every fourth cycle of $T_{REF}/4$. If Δt_1 becomes same as Δt_2, there would be no frequency tone at f_{REF} yielding the perfect canceling at f_{REF}. However, due to the delay error between Δt_1 and Δt_2, the magnitude of the frequency tone at f_{REF} (a_1') is

$$a_1' = \frac{2\Delta I}{\pi}\left(\sin\left(\frac{\pi\Delta t_1}{T_{REF}}\right) - \sin\left(\frac{\pi\Delta t_2}{T_{REF}}\right)\right) \tag{5-12}$$

The magnitude differences between a_1' and a_1 would become to the spur suppression improvement since both a_1' and a_1 are filtered by the loop filter and translated to the VCO control voltages. Comparing a_1' with a_1, the improvement of the spur suppression can be expressed as,

$$20\log_{10}\left(\frac{a_1'}{a_1}\right) \cong 20\log_{10}\left(\frac{\alpha}{1+\alpha}\right) \tag{5-13}$$

where α is the delay error and is defined as $(\Delta t_1 - \Delta t_2)/\Delta t_2$ and assuming $\Delta t_1 << T_{REF}$ and $\Delta t_2 << T_{REF}$. For example, even with α = 0.1 (10% delay error), the proposed

architecture still yields the spur suppression is improved by 21 dB over the conventional architecture. The calculation results are plotted in Figure 119.

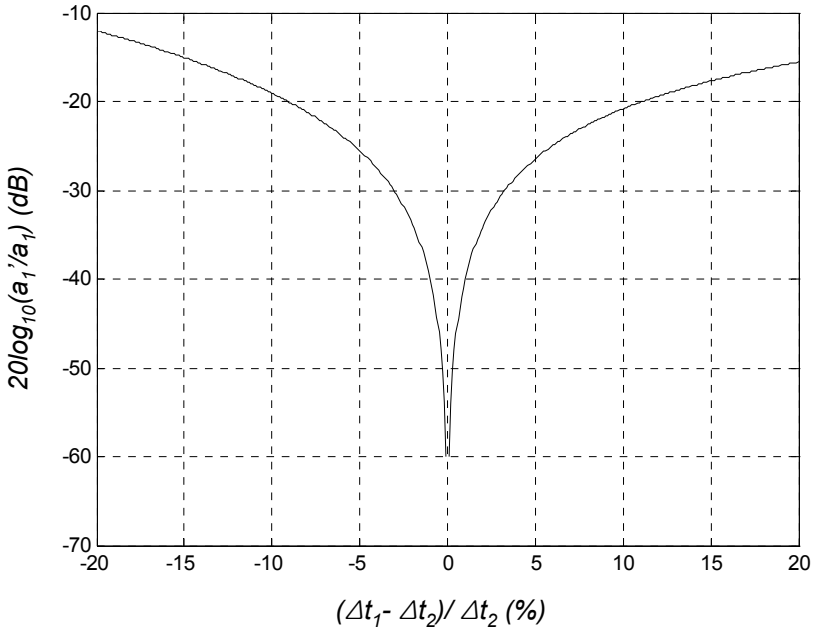


Figure 119. Percentage of delay error versus degradation of the spur.

5.7.3. Charge Pump

A modified charge pump design is depicted in Figure 120. It employs an amplifier with a negative feedback between V_{out} and V_1, and V_1 is forced to follow V_{out} due to this amplifier. Considering the locked status, the left side branch (V_1 side) is turned on at the most of time allowing the current source transistors (MBN and MBP) being always turned on for a fast operation. V_1 is determined by the magnitude of a

current (I_{CP}) and the channel length modulation effect on the transistors MP and MN, while V_{out} that is determined by the settled output frequency.

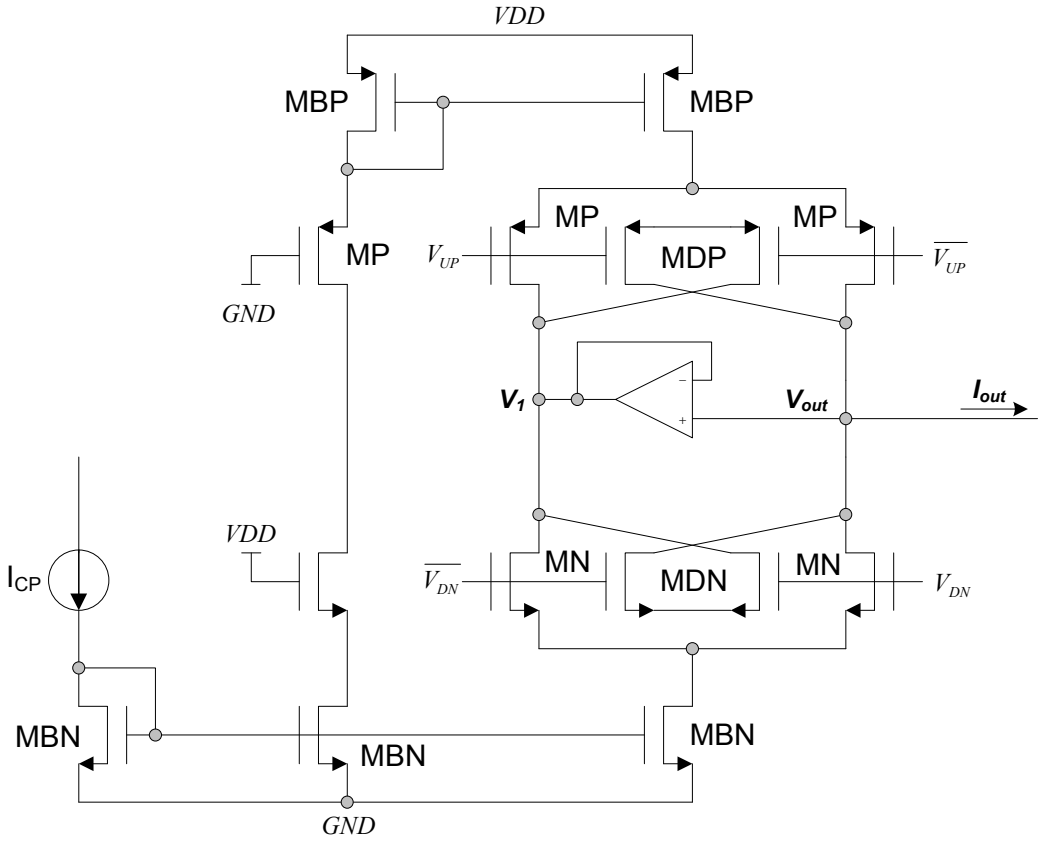


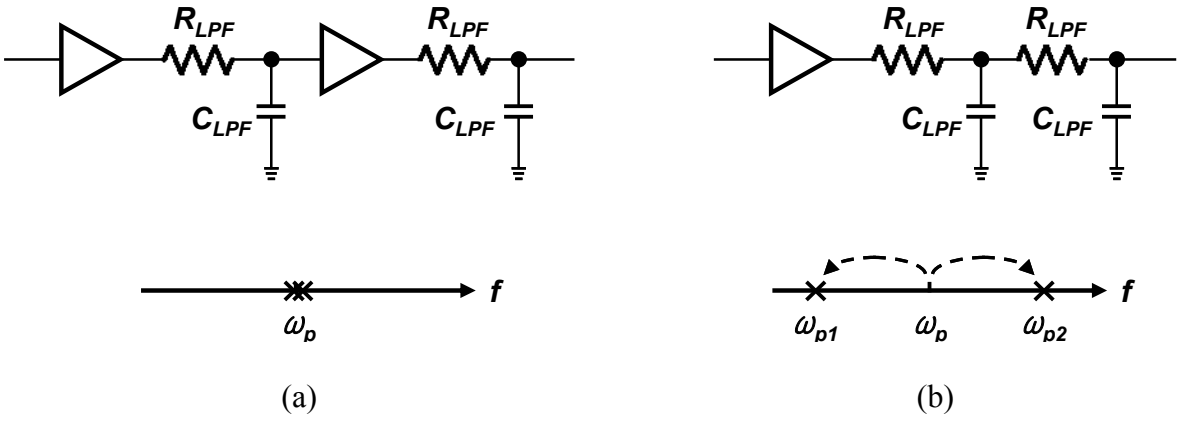
Figure 120. Schematic diagram of the modified charge pump.

During the short time, defined by the delay time in the PFD, the right side branch (V_{out} side) takes over the current from the left side. At this time, if V_1 is different from V_{out}, it generates short-time glitches to compensate the charge difference. The feedback amplifier decreases these glitches by setting V_1 very closed to V_{out}, and as a result,

improves the spur suppression. This technique is called boot-strap [91]. Dummy transistors of MDN and MDP are also used to minimize the charge injection problem.

5.7.4. Additional Low-Pass Filter

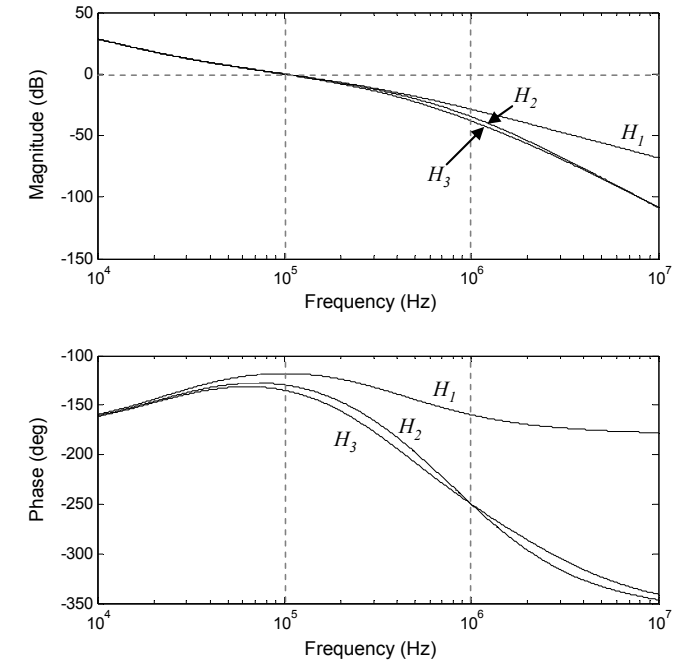
The additional low-pass filter (LPF) is designed with a buffer at the input to avoid a loading effect to the loop filter. It allows a simple and intuitive design of LPF at the cost of a power consumption and noise from a buffer. Since this work aims to maximize the spur suppression, the second-order LPF with two poles is placed.



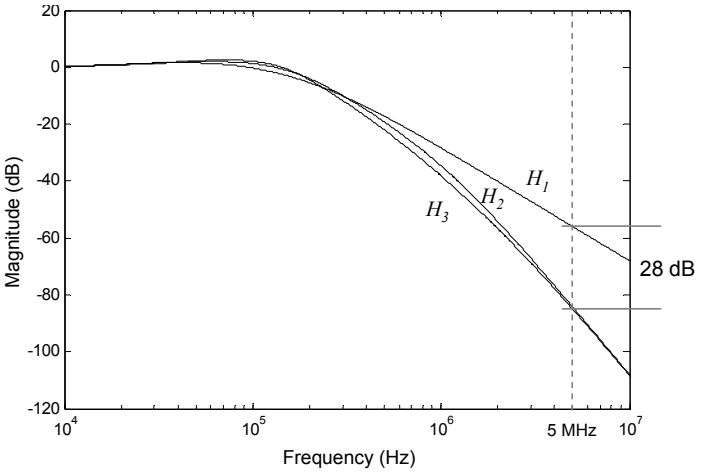
(a) (b)

Figure 121. The second-order LPF. (a) Overlapped two poles with two buffers. (b) Splited two poles with one buffer.

As seen in Figure 121 (a), if a buffer is used between two RC LPFs, two real poles are overlapped at one frequency that is given as $\omega_p = 1 / (R_{LPF}C_{LPF})$. In this work, ω_p is determined to $2\pi \times 1$ MHz and, $R_{LPF} = 80$ KΩ and $C_{LPF} = 2$ pF.

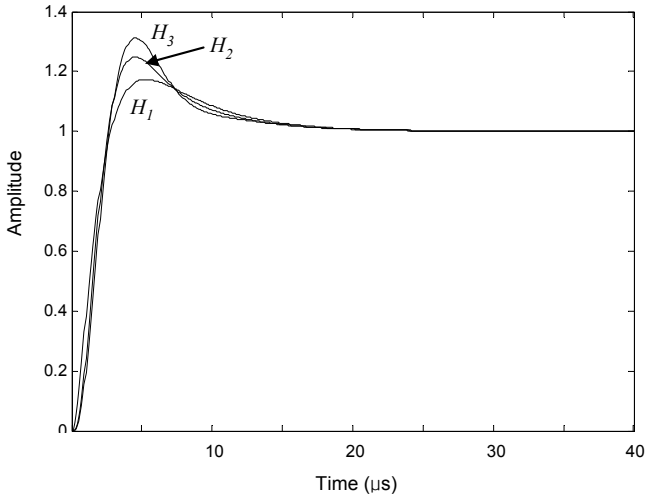


(a)



(b)

Figure 122. Transfer function plot for H1 (Conventional), H2 (Conventional + Two-buffer LPF) and H3 (Conventional + One-buffer LPF). (a) Magnitude and phase response of an open-loop transfer function. (b) Magnitude of a closed-loop transfer function. (c) Step response of a closed-loop transfer function.



(c)

Figure 122. Continued.

The LPF with two buffers can be simplified as one buffer LPF as seen in Figure 121 (b). In this case, overlapped poles (ω_p) are separated to two real poles (ω_{p1}, ω_{p2}) with the relationship of $\omega_p^2 = \omega_{p1} \times \omega_{p2}$. By adding the LPF, a phase margin will be degraded from the conventional loop while a reference spur is more suppressed. In case of the two-buffer LPF, a phase margin is measured as 51º and the one-buffer LPF yields a phase margin of 46º while it was 62º of the conventional loop. The one-buffer LPF more degrades a phase margin because one of the separated poles approaches to ω_p. For the improvement of the suppression of a reference spur at 5 MHz is 28 dB in both cases. In step response of each system, the amount of overshoot is most critical in the one-buffer LPF due to a degraded phase margin. These results are shown in Figure 122 where H1

represents the conventional type-II third-order loop, H2 is the type-II fifth-order loop with a two-buffer LPF and H3 is the type-II fifth-order loop with an one-buffer LPF.

5.7.5. Voltage Controlled Oscillator

The VCO design is modified since we have observed the significant frequency drop from measurements. A schematic diagram of the new design is shown in Figure 123. In modified design, a differential-type inductor is used as it becomes available in the design kit. A differential structure helps to decrease unexpected parasitics by minimizing the needed connections.

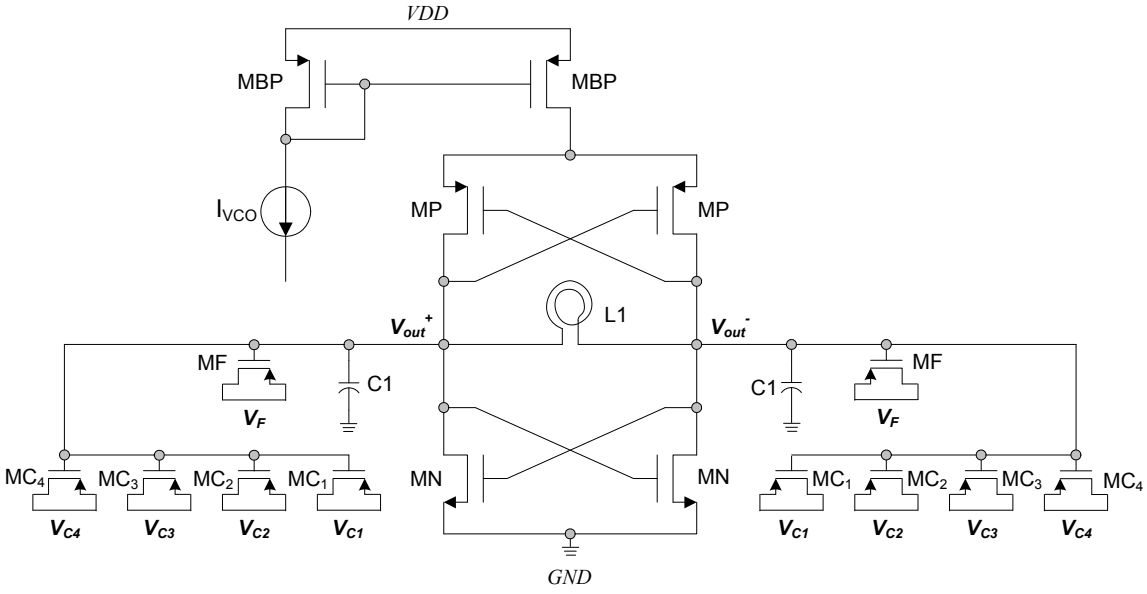
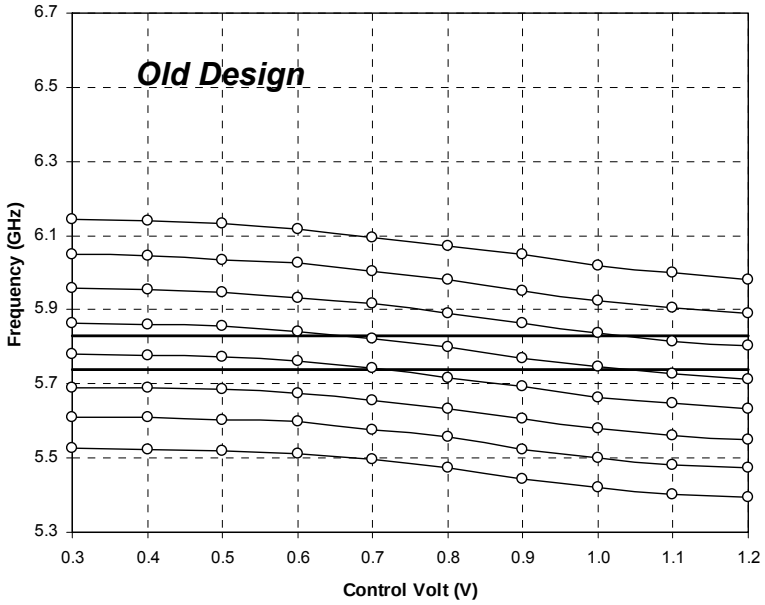
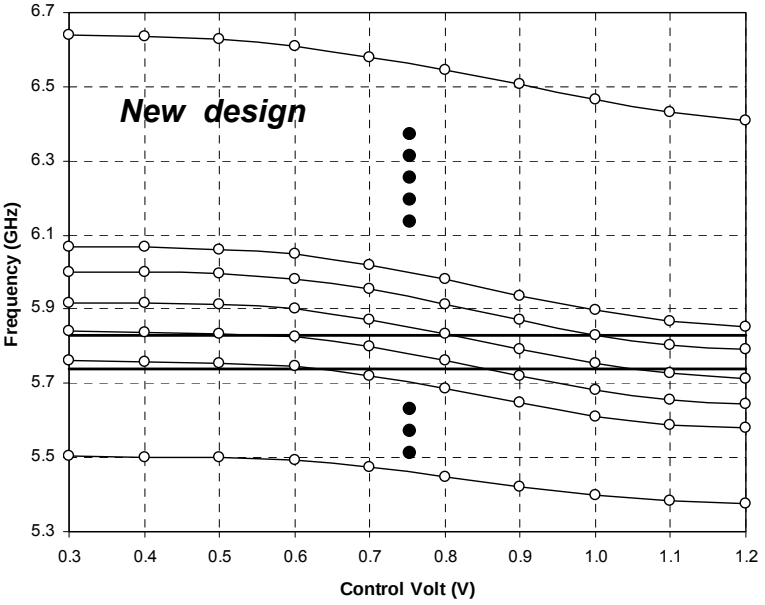


Figure 123. Modified VCO schematic diagram.



(a)



(b)

Figure 124. Post layout simulation results of the VCO frequency. (a) Old design. (b) New design.

Post-layout simulation is performed and the results are plotted in Figure 124. In the new design, the number of discrete tuning bits is increased to 4 resulting in 16 discrete tuning curve. To extend the frequency tuning range, the inductance of L1 is decreased as well. The post-layout simulation result from the new design exhibits the frequency tuning range is extended to 24 % (5.37 ~ 6.67 GHz) from 13.9 % of the previous design. Other aspects of the VCO, such as the VCO gain, phase noise, are similar to the previous design.

5.7.6. Status of the Improved Design

The modified architecture of the proposed frequency synthesizer is designed using UMC 0.13 μm CMOS process. The design is completed and the performance is verified through the post-layout simulation. Currently, this design is waiting to be submitted.

5.8. Conclusion

An adaptive additional lowpass filtering technique to reduce the reference spurs for integer-N based frequency synthesizers has been proposed. Its property of controlling the order of loop filter depending on the loop status improves the reference spur rejection compared with the conventional frequency synthesizer. An integer-N frequency synthesizer which is capable of selecting the conventional and proposed operation mode

was designed and fabricated to compare the reference spur suppression. The improvement of 20 dB on the reference spur rejection was achieved with the proposed frequency synthesizer yielding -57 dBc while -37 dBc was measured from the conventional frequency synthesizer. Another pulse interleaving technique and other improvement on the individual building blocks for further improvement on the spur rejection were proposed and the new designed frequency synthesizer is ready to be submitted for a fabrication.

CHAPTER VI

CONCLUSION

In this dissertation, we discussed several aspects in designing the VCO and the frequency synthesizer. Phase noise of the VCO was examined with numerical expressions. Various design parameters in the frequency synthesizer were investigated.

A non-linear shaping technique based on a multi-level comparator for SC BPF-based oscillator has been proposed. Its property of rejecting the third- and fifth-order harmonics improves the overall linearity in SC BPF-based oscillator. The proposed oscillator was fabricated in CMOS 0.35 μm process. HD3 was measured as -54.8 dB that is improved by 20dB over the conventional oscillator. Further linearity improvement can be obtained by increasing the accuracy of the step magnitude of the multi-level comparator at the expense of extra area.

An RC BPF-based oscillator suitable for RF applications was proposed and described. A prototype oscillator operating at 2.5 GHz was designed, and measurement results have validated the proposed idea. Since the proposed oscillator is based on BPF, the phase noise shaping behavior is closer to that of an LC oscillator. In particular, the presented oscillator is less sensitive to supply noise than a ring oscillator. Also, by avoiding the use of inductors, the silicon area is more than one hundred times smaller than a commensurate LC oscillator.

Finally, an adaptive additional lowpass filtering technique to reduce the reference spurs for integer-N based frequency synthesizers was proposed. An additional RC lowpass filter next to the loop filter was adaptively introduced, hence the reference spur is more suppressed without a serious stability degradation. An integer-N frequency synthesizer which is capable of selecting the conventional and proposed operation mode was designed and fabricated to compare the reference spur suppression. The improvement of 20 dB on the reference spur rejection was achieved with the proposed frequency synthesizer yielding -57 dBc while -37 dBc was measured from the conventional frequency synthesizer. Another pulse interleaving technique and other improvement on the individual building blocks for further improvement on the spur rejection were proposed and the new designed frequency synthesizer is ready to be submitted for a fabrication.

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VITA

Sang Wook Park was born in Seoul, Korea. He received the B.S. and M.S. degree in electronic engineering from Yonsei University, Seoul, in 1993 and 1996, respectively. In 1996, he joined LG Semicondutor, Korea, where he was engaged in SPICE modeling of CMOS 0.35um, 0.5um and 64M DRAM process. From 1999 to 2002, he was with HYNIX Semiconductor, Korea, where he was involved in the characterization of CMOS RF devices in 0.25um and 0.18um processes. His research interests include frequency synthesizers, high-speed and low-power analog IC design, and RF IC design for wireless communication. Since 2002 he worked towards his Ph.D. at the Analog and Mixed Signal Center, at Texas A&M University. He received his Ph.D. in 2009. During his doctoral program he was involved in the design of VCO and frequency synthesizers for wireless communication receivers.

He can be reached through the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843. His email is: parksw00@tamu.edu.