MILLIMETER-WAVE CONCURRENT DUAL-BAND BiCMOS RFIC TRANSMITTER FOR RADAR AND COMMUNICATION SYSTEMS

A Dissertation

by

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ABSTRACT

This dissertation presents new circuit architectures and techniques for improving the performance of several key BiCMOS RFIC building blocks used in radar and wireless communication systems operating up to millimeter-wave frequencies, and the development of an advanced, low-cost and miniature millimeter-wave concurrent dual-band transmitter for short-range, high-resolution radar and high-rate communication systems.

A new type of low-power active balun consisting of a common emitter amplifier with degenerative inductor and a common collector amplifier is proposed. The parasitic neutralization and compensation techniques are used to keep the balun well balanced at very high frequencies and across an ultra-wide bandwidth. A novel RF switch architecture with ultra-high isolation and possible gain is proposed, analyzed and demonstrated. The new RF switch architecture achieves an ultra-high isolation through implementation of a new RF leaking cancellation technique. A new class of concurrent dual-band impedance matching networks and technique for synthesizing them are presented together with a 25.5/37-GHz concurrent dual-band PA. These matching networks enable simultaneous matching of two arbitrary loads to two arbitrary sources at two different frequencies, utilizing the impedance-equivalence properties of LC networks that any LC network can be equivalent to an inductor, capacitor, open or short at different frequencies. K- and Ka-band ultra-low-leakage RF-pulse formers capable of producing very narrow RF pulses in the order of 200 ps with small rising and falling

time for short-range high-resolution radar and high-data-rate communication systems are also developed.

The complete transmitter exhibiting unique characteristics obtained from capabilities of producing very narrow and tunable RF pulses with extremely RF leakage and working concurrently in dual bands at 24.5 and 35 GHz was designed. Capability of generating narrow and tunable RF pulses allows the radar system to flexibly work at high and multiple range resolutions. The extremely low RF leakage allows the transmitter to share one antenna system with receiver, turn on the PA at all time, comply the transmitting spectrum requirements, increase the system dynamic range, avoid harming to other systems; hence improving system size, cost and performance. High data-rate in communication systems is achieved as the consequence of transmitting very narrow RF pulses at high rates. In addition, the dissertation demonstrates a design approach for low chip-area, cost and power consumption systems in which a single dual-band component (power amplifier) is designed to operate with two RF signals simultaneously.

DEDICATION

To my beloved wife Bao-Ngoc Huynh and daughters Minh Thu and Minh Phuong

For all their love and unwavering support

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CHAPTER I

INTRODUCTION

1.1 Background and Motivation

Wireless systems including communication and radar-based sensor networks play a very important role in our information-age society in many areas, from public service and safety, consumer, industry, transportation, sports, gaming and entertainment, asset and inventory management, banking to government and military operations. Today, we can easily access voice, data and entertainment information at almost every corner on the globe, from short range Bluetooth and WiFi networks, to long range cellular and satellite networks. Varieties of wireless sensor and radar networks have been employed to collect or sense remote information.

Ultra-wideband (UWB), pulse-based or orthogonal frequency-division multiplexing (OFDM), systems have been potential solutions for the requirement of the modern wireless networks and received significant interests from various academic and industrial organizations, particularly after the FCC's approval in 2002 for unlicensed uses of UWB devices within the 3.1-10.6 GHz frequency band [1]. The multiband OFDM technique was accepted as the industrial standard for very high data rate communication systems in Dec. 2005 [2], while the pulse-based UWB system has been demonstrating as a low complexity and power consumption solution for radar systems with the capability of high precision and resolution in detection and location [3]-[4]. UWB systems transmit and receive signals with extremely low-power spectral densities

across an ultra-wide band spectrum. This effectively produces extremely small interference to other radio signals while maintains excellent immunity to interference from these signals. UWB devices can therefore work within frequencies already allocated for other radio services, thus helping to maximize this dwindling resource. Additionally, UWB techniques have lower power requirements, less multi-path problems, and enhanced resolution and locating precision, as compared to more conventional continuous wave (CW) approaches. Various UWB components and systems have been developed for different applications [5], [6]-[8]. In [5], an on-chip CMOS transmitter having capability of transmitting 250-ps monocycle impulses for heart-rate detection systems is presented. In [6], a CMOS transceiver is designed for an OFDM-based communication system working at high data rate of 480 Mb/s.

While the current UWB frequency range (3.1-10.6 GHz) meets the present and near-future projections for wireless networking, it may pose some potential problems with respect to device size, increasingly congested spectrum and precision location in very crowded areas for envisioned future wireless networking, which require billions of wireless sensors and devices. The demand for increasing wireless transfer capacity and speed, far exceeding those provided in the traditional microwave frequency band from 1 to 30 GHz, with minimum interference, has led the wireless industry to focus on higher, previously unallocated spectrums. The millimeter-wave (MMW) regime, from 30-300 GHz, is the logical solution to meet this demand.

Based on Shannon's Theorem, the maximum data-rate of a communication known as channel capacity, *C*, is related to the system frequency bandwidth, *BW*, and the signal-to-noise ratio, *SNR*, in the following manner [9]

$$C = BW \cdot \log_2 (1+SNR) \tag{1.1}$$

This equation shows that more information can be transmitted over wider bandwidth channel. The signal bearing information is usually modulated around a carrier frequency for proper propagation, and more bandwidth is available around higher carrier frequencies.

In July 2003, the IEEE 802.15.3 standard for Wireless Personal Area Network (WPAN) was considered for use of 7-GHz bandwidth of unlicensed spectrum around 60 GHz which enables very high data-rate applications such as high-speed internet access, streaming content downloads, and wireless short-range device connection [10]. The envisioned connectivity of a 60 GHz wireless network is shown in Fig. 1.1 [11]. In October 2003, the FCC opened the MMW spectrum in the 71-76 GHz, 81-86 GHz and 92-95 GHz bands for commercial wireless broadband communications, and hence opening opportunities for high-speed wireless communications and networking at extremely high frequencies. Particularly, the FCC also permits unlicensed indoor use of the 92-94 GHz and 94.1-95 GHz bands by non-federal government users. The 22-29-GHz and 77-GHz frequency bands were also allocated for short-range and long-range automotive radar applications [12]. Fig. 1.2 shows possible applications of short range automotive radar systems [13].

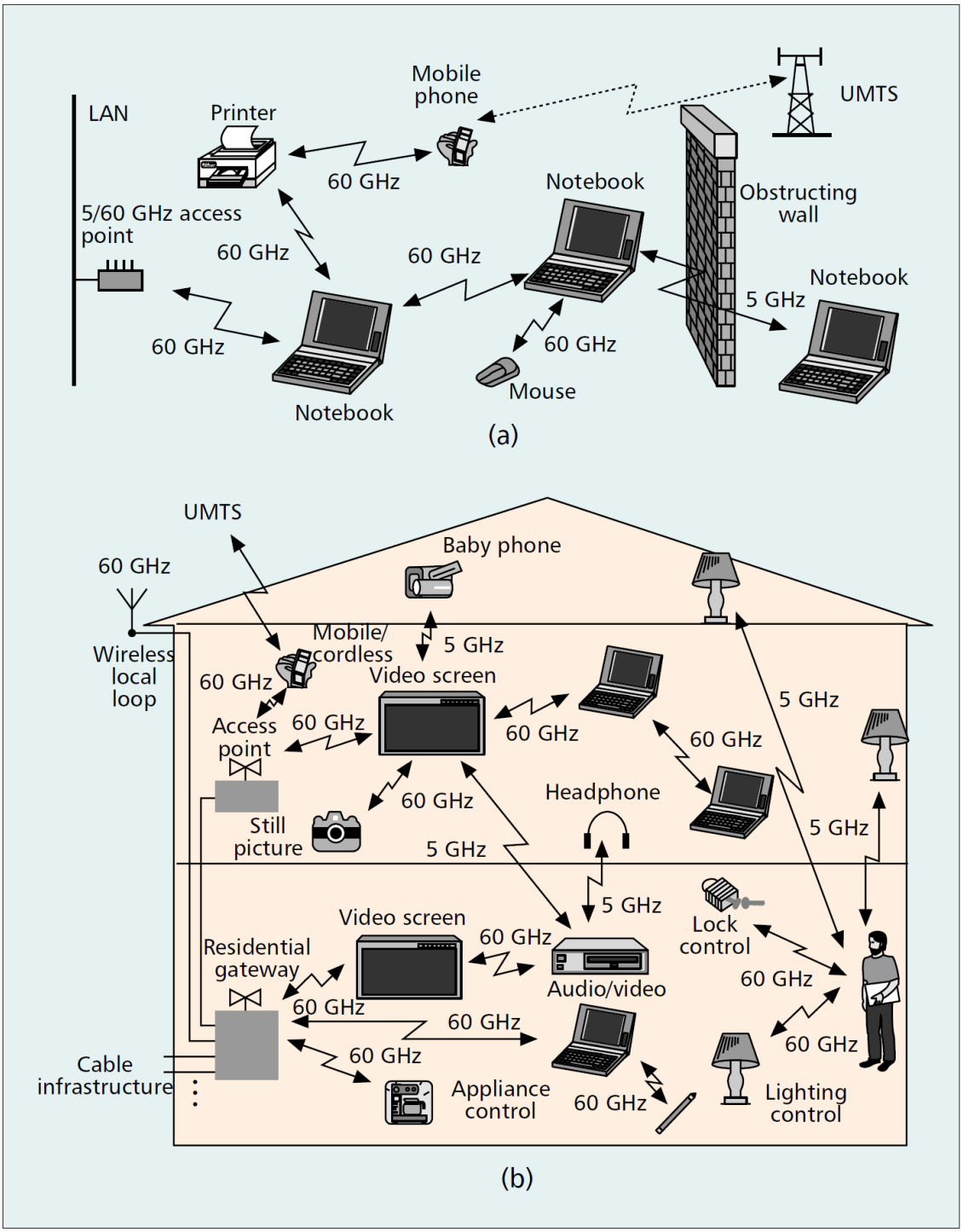


Fig. 1.1. Envisioned connectivity of a 60 GHz wireless network.

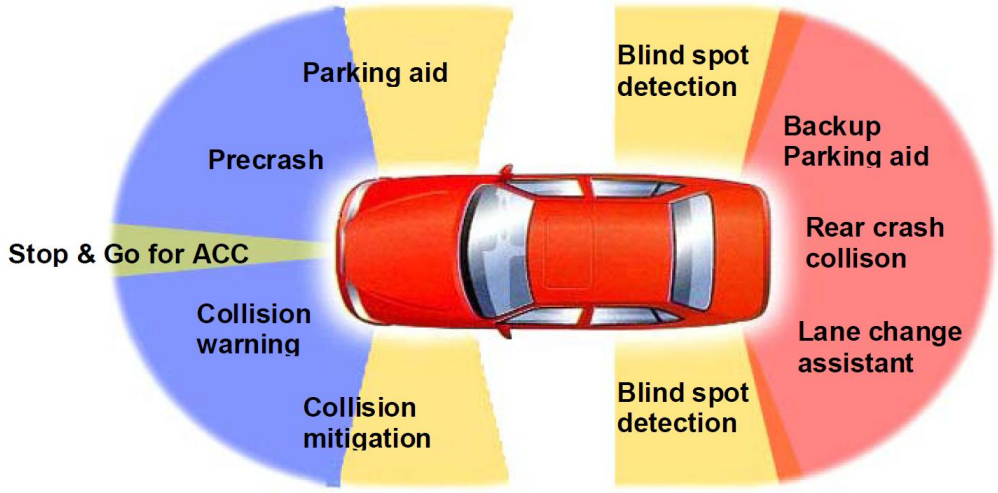


Fig. 1.2. Possible applications of short range automotive radar systems.

At MMW frequencies, antennas and circuits are very small, making feasible compact and low-cost deployment of sensor and communication networks. MMW antennas have high directivity and gain, helping relax the RF power requirement and eventually the power consumption of transmitters, which are valuable for wireless networks. The high directivity of MMW antennas also minimizes the possibility of interference between sensors in the same geographic area. A greater number of highly directive antennas can thus be placed than less directive antennas in a given area, resulting into higher reuse of the spectrum and higher density of sensors, as compared to lower frequencies. MMW antennas have narrow beam-width and hence enhance the resolution for locating purposes. Radio waves in the MMW spectrum have relatively high attenuation due to the oxygen absorption and can therefore travel only within short distances (less than a few miles) which make the MMW suitable for high speed and short range communication system. This limited traveling range also helps increase the

frequency re-use – the ability of operating many sensors or communication devices on the same frequency within the same geographic area with minimum interference. Deployment of large networks of wireless sensors and communication devices within crowded areas is thus further feasible.

Compound III-V semiconductors with active devices such as GaAs MESFETs, PHEMT, InP HEMT, GaAsMHEMT, GaAs HBT, InP HBT have traditionally dominated the millimeter wave spectrum over the past several decades. Although these technologies offer very good performance at MMW frequencies, they are quite expensive and have low manufacturing yields, and thus offer limited integration possibilities. Today, with the drive to low-cost, compact, high-volume applications such as automotive radar, sensor and communication devices along with scaling to sub-100 nm dimensions, the group IV semiconductors including Si and SiGe are rapidly moving up to frequencies that were once the exclusive domain of the III-V semiconductors. Si transistors nowadays are small and fast enough to operate into the tens of GHz, thus vying for countless radar and communication applications in these frequency bands. Silicon-based CMOS (and related BiCMOS, SiGe, etc.) radio frequency (RF) integrated circuits (ICs) and systems have advanced significantly and can perform at very high frequencies. CMOS RF ICs have lower cost and better abilities for direct integration with digital ICs (and hence better potential for complete system-on-a-chip) as compared to those using III-V compound semiconductor devices. CMOS RF ICs are also small and low-power, making them suitable for battery-operated sensors and communication

devices. CMOS RF ICs are thus very attractive for transceivers and, in fact, the principal choice for commercial wireless markets nowadays.

Advanced concurrent multiband radar and communication systems simultaneously working on multiple frequency bands provide more capabilities and numerous advantages as compared to the single-band counterparts. More functionality can be clearly seen in the fact that more information is transmitted and received, and more remote targets are sensed simultaneously on multiple channels. Working on multiple frequencies makes the systems more robust with the fluctuation of propagation environment such as severe multi-path fading, urban settings, mountainous terrains or frequency-dependence attenuation. Multi-band operations can be implemented using a single system leading to substantial benefits including reduced circuit size, low cost and low power consumption. However the design of multiband systems is challenging and requires new techniques to design the components having optimized performances at multi-bands concurrently.

In order to meet the high demand of short-range radar and communication systems in the future, the development of miniature, low-cost, low-power MMW transmitters capable of high-resolution, precise and fast location detection, and high data rate communication is needed. The new system should effectively utilize the newly opened MMW spectrums, exploit the unique characteristics of UWB and work in multi-bands concurrently.

In this dissertation, a millimeter-wave concurrent dual-band transmitter working in K and Ka bands for short-range high-resolution radar and high-rate communication

systems is proposed and developed. The proposed transmitter is designed using SiGe BiCMOS technology and concurrently works at two different frequencies, resulting in low-cost, miniature, and low-power consumption systems. The developed concurrent dual-band transmitter can be used for numerous cost-effective and multi-functionality applications such as short-range high-data-rate communications, sensing, imaging, automotive radar, personnel and item tracking, and RFID.

1.2 Short Range Radar System

Radar (Radio Detection And Ranging) has a long history dating back to the date in 1886 when Heinrich Hertz experimentally demonstrated the similarity of radio and light wave and the reflection of radio wave from metallic and dielectric objects [14]. Many decades later, radar systems were developed independently and simultaneously in several countries. Today, radar systems have been used on the ground, in the air, on the sea and in space for many applications from weather observation, sensing to law enforcement and guidance and safety for airplanes, ships and automotives.

1.2.1 Radar System Overview

A radar system is used to detect and characterize the targets, basically consisting of three main components: a transmitter, a receiver, and an antenna system as shown in Fig. 1.3.

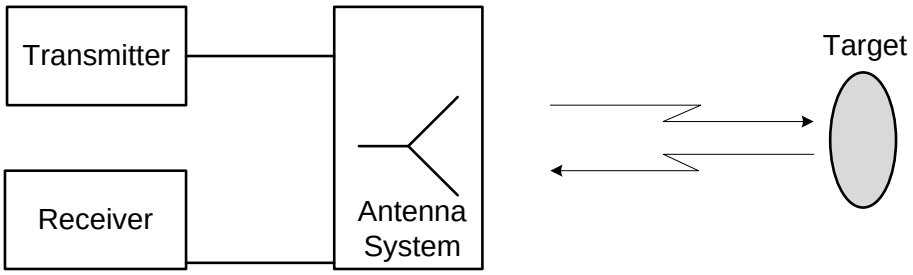


Fig. 1.3. Radar subsystems. A radar system consists of three subsystems: a transmitter, a receiver and an antenna system.

Transmitter

The transmitter transmits a signal which can be a continuous wave (CW) or pulsed signal. The transmitting signal is incident to a target and reflected back to the antenna system. The receiver receives the reflected signal, determines the presence of the target, and extracts other information such as range and velocity.

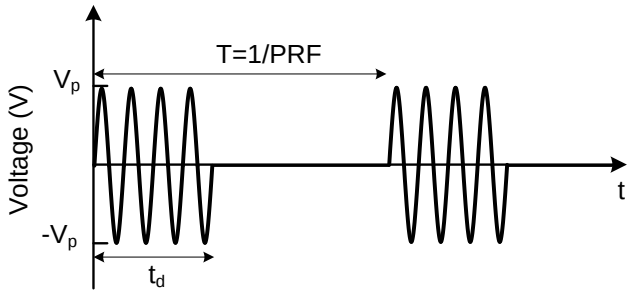


Fig. 1.4. RF pulse signal.

Radar systems operate over an extremely wide range of frequencies in the RF, microwave and millimeter-wave regimes, up to 300 GHz [14]. The radar signal can be in continuous-wave (CW) or pulsed waveform. A CW transmitter sends a continuous radio frequency (RF) signal, while a pulsed transmitter broadcasts a train of RF pulses or

impulses with a system-defined carrier frequency, pulse repetition frequency (PRF), and duty cycle. The PRF is the frequency at which the RF pulses or impulses are transmitted, and is reversely proportional to T, where T is the time between transmitted pulses, as shown in Figure 1.4. The duty cycle of RF pulses is defined as the ratio of t_d/T, where t_d is the transmitted pulse width.

CW radar systems are generally simpler than pulsed radar systems in terms of hardware and signal control since they are always on. However, the detection of signal in the CW radar is more difficult due to the high RF leakage from transmitter to receiver. In a pulsed system, the transmitter and receiver are never on simultaneously, making it easier to detect a returned signal at the expense of increased hardware and signal complexity. A pulsed radar signal can be incoherent or coherent. To be coherent there must be a deterministic phase relationship for the carrier from pulse to pulse. This can be accomplished by switching a CW carrier on and off.

The waveform modulation can be included in both CW and pulsed transmitters. Various modulation schemes can be used including the phase, frequency and amplitude modulation, or a combination of modulation types. For pulsed systems, the modulation can be applied within each pulse over the time period t_d. With the included signal modulation functionality, the transceiver in radar systems can be used in communication systems.

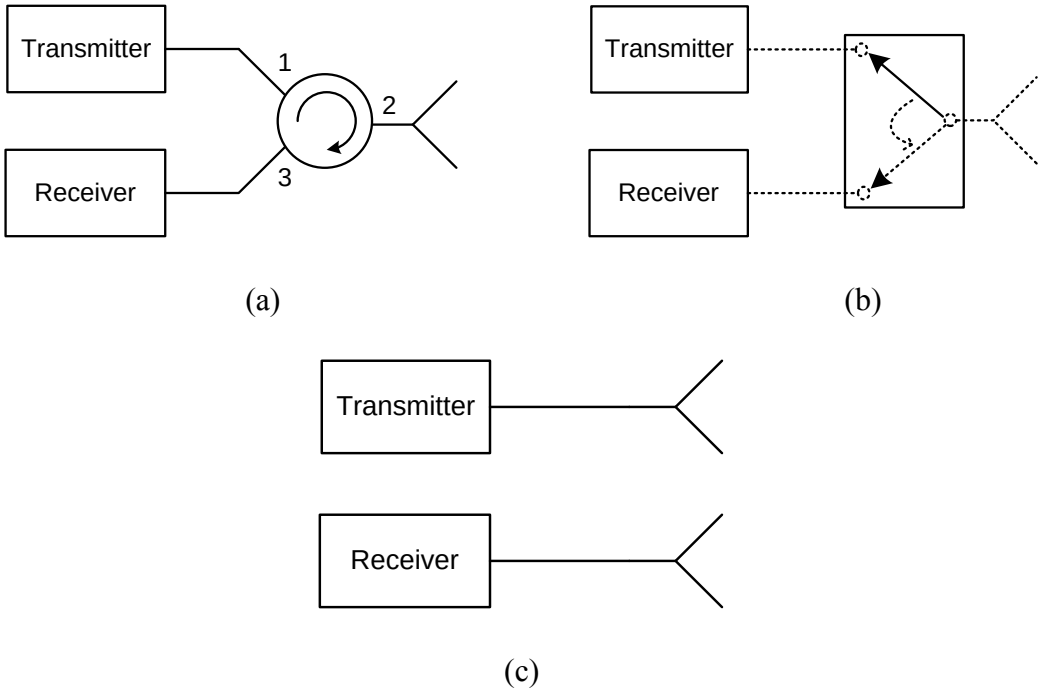


Fig. 1.5. Antenna systems. Antenna systems can consist of one antenna using circulator (a) or T/R switch (b), or two separate antennas (c).

Antenna system

Radar antenna systems can consist of a single antenna commonly used for both transmission and reception, a pair of antennas for transmission and reception, or an array of antennas. A single antenna can be used for pulsed systems, but is normally avoided in CW systems [14]. A single antenna and two antennas systems are illustrated in Fig. 1.5. When a single antenna is employed, a circulator or transmit/receive (T/R) switch is used to connect the transmitter, antenna system, and receiver. In circulator implementation as shown in Fig. 1.5 (a), the transmitting signal passes from port 1 to 2 of the circulator, but not port 3; as such, the transmitting signal does not reach the receiver. If a target is present, the reflected signal is received by the antenna system and passed from port 2 to

3 of the circulator, but not port 1; as such, the received signal is passed to the receiver but not the transmitter, with the assumption of the idea circulator. Realistically, there will be a finite isolation between circulator ports, leading to a finite isolation between the transmitter and receiver. Since the transmitted signal is normally much larger than the received signal, it is critical that the circulator provides sufficient isolation between ports 1 and 3 to allow the receiver to detect the received signal without being jammed by the transmitted signal that leaks through the circulator. The same situation applies to the T/R switch implementation, which requires the high isolation for the T/R switch in the reception mode. If separate transmit and receive antennas are used, the high intrinsic isolation between the antennas minimizes the leakage from the transmitter to the receiver through the antenna system. Finally, for systems requiring high antenna gain and directivity, antenna arrays can be used [15]. The transmitter and receiver can share an antenna array or use separate arrays. Antenna arrays are used extensively in radio astronomy and synthetic aperture radar (SAR) applications [14].

Receiver

The radar receivers amplify, filter, and down-convert the received signal to the intermediate frequency (IF) or baseband signal, from which the target can be correctly characterized. Fig. 1.6 shows the basic radar receiver architecture consisting of a LNA, band pass filter (BPF), mixer, low pass filter and variable gain amplifier (VGA). As the first stage in the receiver, the LNA should exhibit high gain and a low noise figure to maintain a low noise figure for the whole receiver. The band pass filter sets the RF

bandwidth of the receiver and limits the receiver noise. The down-converter mixer converts the received signal frequency to the IF band or DC by mixing the received signal with the local oscillation (LO) signal. In a coherent radar system, the receiver's LO is synchronized with the transmitter LO; coherent systems are common in modern radar systems. Upon down-conversion to the IF band, the signal is filtered and amplified. The IF low pass filter (LPF) sets the final noise bandwidth for the receiver. The output of the receiver is then digitized, and digital signal processing is applied.

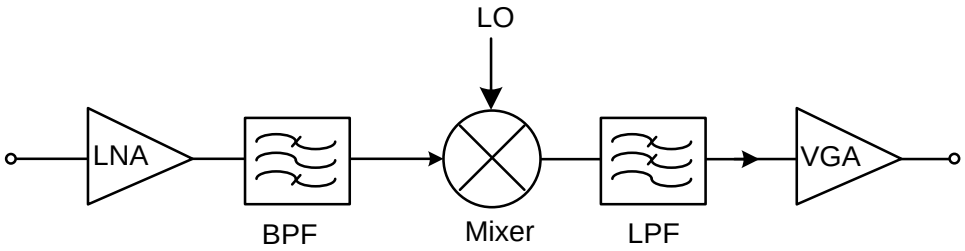


Fig. 1.6. Basic radar receiver architecture.

1.2.2 Short Range Pulse Radar System

In recent years, the short-range radar has found many applications in automotive, sensing, imaging and ground penetration systems. Main functionalities of short range radar systems include the detection, range and track of the static and moving targets. With advantages of high range accuracy, clutter reduction, multipath resolution and transmit-receive isolation relax [12], the pulsed radar architecture is also perhaps one of the simplest architectures to implement, thus potentially making it the most cost effective.

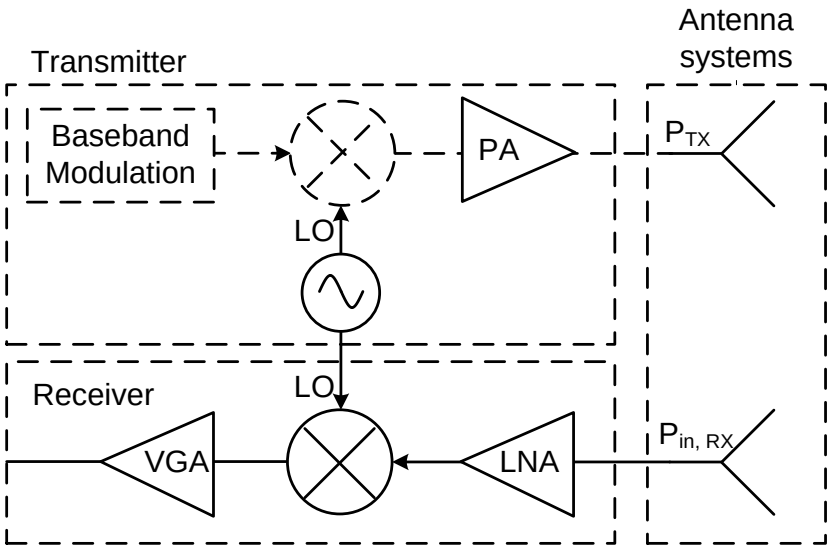


Fig. 1.7. Basic pulsed radar system architecture.

The typical pulsed radar architecture is illustrated in Fig. 1.7. A baseband impulse is generated from the baseband modulation circuit and applied to the IF port of the up-converter mixer to mix with the LO signal generated from an oscillator. The resulting RF-pulse signal, as shown in Fig. 1.4, occupies a bandwidth of approximately $1/t_d$, where t_d is the width of the baseband impulse; the precise bandwidth will depend on the shape of the impulse envelope [14]. It is common to illustrate the baseband impulse as a rectangular pulse, but the Gaussian shape can be used to suit the radar requirements of spectrum compliance.

If the transmitted RF pulse is reflected by a static or moving target, then the returned signal can be detected by the receiver, and the target information is extracted. The receiver often employs the range gates in the RF front-end to range the targets. The range-gate defines the length of time the receiver is “on” and can receive signals. Range

gating allows the radar user to select a single target range to observe. When open, the range gate allows normal signal detection; when closed, it attenuates the received signal so that it is not detectable [14]. The range-gate pulse width is normally matched to the transmitted pulse width.

The minimum detectable range of the pulsed radar systems is limited by the transmitted pulse width, t_d. The transmitter and receiver are never on simultaneously, and the receiver cannot be turned on until after the transmitter completes its transmission, leading to a minimum detectable range of $R_{min} = \frac{c\, t_d}{2}$; where c is the velocity of light in air.

Unlike CW radars, the pulsed radar system does not transmit a continuous signal, and, assuming a rectangular pulse envelope, the average power is equal to $P_p \frac{t_d}{T}$, where P_p is the peak power of the signal. For a given average power, the required peak power of a short-pulse signal is high compared to other radar signals, due to its low duty cycle (t_d/T). However, for short-range radar systems, the power requirements are relatively low, so a high peak power may not be a concern.

Pulsed radar systems provide the natural target resolution and clutter rejection due to range gating in the transmitter and receiver respectively [14]. Since both the transmitter and receiver are pulsed, transmit-receive isolation requirements are also simpler to meet than with a CW system.

Radar Equations

The received power at the input of the radar receiver is calculated using radar equation

$$P_r = \frac{P_t.G_{tx}G_{rx}.\lambda^2.\sigma}{(4\pi)^3.R_{max}^4} \tag{1.2}$$

where P_{rx} in is the power at the input of the receiver, P_{tx} is the power at the output the transmitter, G_{tx} is the transmit antenna gain, G_{rx} is the receive antenna gain, λ is the wavelength of the carrier frequency, σ is the radar cross section (RCS) of the target, and R is the range to the target [14].

The maximum range of the radar system is calculated from (1.2) as

$$R_{max} = \left(\frac{P_t.G_{tx}G_{rx}.\lambda^2.\sigma}{(4\pi)^3.P_{r,min}} \right)^{\frac{1}{4}} \tag{1.3}$$

where R_{max} is the maximum target range and $P_{r,min}$ is the minimum detectable power at the input of the receiver. The expression demonstrates the relationship between the target range, transmitted power, and minimum detectable received power. Increasing the transmitted power and/or decreasing the minimum detectable received power increases the maximum range of the radar.

The minimum signal to noise ratio for a single pulse at the output of the receiver, $SNR_{o,min}$ is calculated as

$$SNR_{o,min} = \frac{SNR_{in,min}}{F} \tag{1.4}$$

where $SNR_{in,min}$ is the minimum signal to noise ratio for a single pulse at the input of the receiver and F is the noise figure of the receiver. Making use of (1.2) and (1.4), $SNR_{o,min}$ is calculated as

$$SNR_{o,min} = \frac{EIPR_{pk}.G_{rx}.\lambda^2.\sigma}{(4\pi)^3.K.T_a.BW.F.R_{max}^4} \quad (1.5)$$

where K is the Boltzmann constant (1.38e-23 J/K), T_a is the antenna temperature, and B is the noise bandwidth of the receiver.

1.2.3 Signal Modulation

Signal modulation schemes can be implemented in pulsed radar systems to support the data communication. On-Off-Key modulation (OOK), Pulse Position Modulation (PPM), Pulse Amplitude Modulation (PAM) and Bi-phase modulation (BPM) are the most widely used for this objective; the transmitting information can be coded by changing the pulse position, shape or polarity.

On-Off-Key Modulation (OOK)

OOK is the simplest modulation method where information bits "1" or "0" is represented with the presence or absence of a pulse. The demodulation of the OOK signal can be done by the power detection. The major disadvantage of OOK is that it is less immunized to noise, interference and multipath fading, therefore it will be difficult to determine if the detected signal is the fading/noise or transmitted pulse.

Pulse Position Modulation (PPM)

Information bit in the PPM is identified by whether the RF pulse exists in a delayed position from regular time or not. PPM can be used in a M-ary system in which two or more bits can be grouped together to form a symbol. Multiple symbols are coded using different delay values for the pulse positions. The advantage of PPM is that the pulse position will appear to be random on the time domain, which translates into a smoothly spread spectrum on the frequency domain.

Pulse Amplitude Modulation (PAM)

Multiple symbols in the M-ary systems can be transferred using different RF pulse amplitudes. This requires the gain of the pulse generator output driver be programmable. High data rate can be achieved with PAM using increased number of amplitude levels. However, the pulses will be very close to each other and more susceptible to noise and interference while larger pulses will require more power for amplification. OOK actually is the simplest case of PAM.

Bi-Phase Modulation (BPM)

In BPM, the bits "1" or '0" is transmitted using 180-degree out of phase RF signals. BPM is less sensitive with noise as compared to amplitude-based modulation schemes. The requirement for accurate timing control is also not as stringent as PPM.

Figure 1.8 summarizes and compares different modulation schemes mentioned in this section. The information bits to be transmitted are “1 0 1 0”.

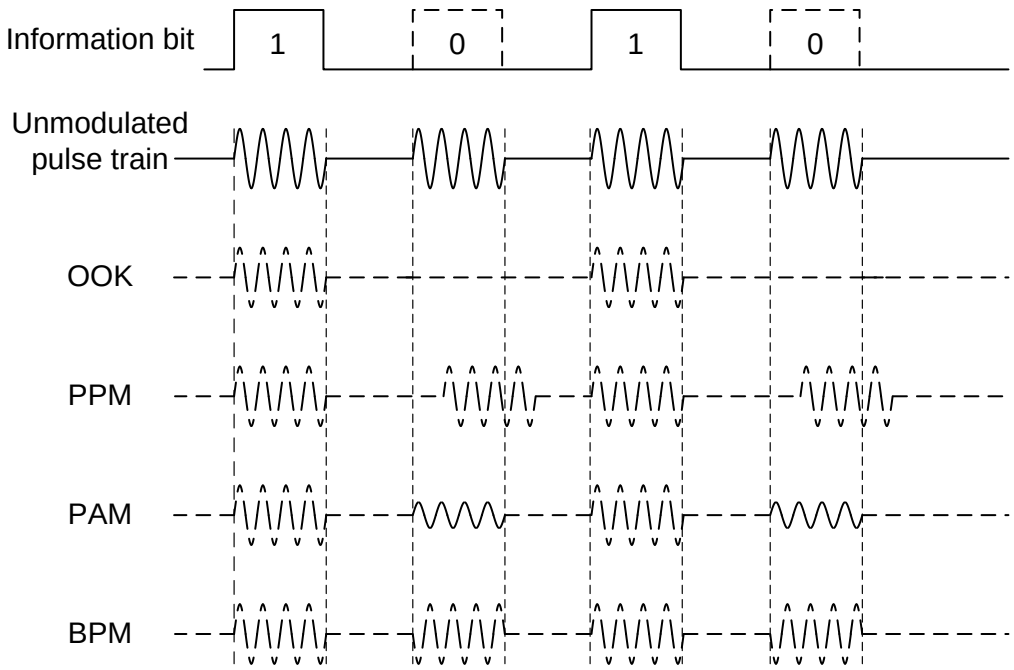


Fig. 1.8. Illustration of different modulation schemes.

1.3 Transceiver Architecture for Short Range Radar and Communication Systems

Based on the presented modulation schemes, it has been shown that a system architecture including the functionality of data modulation can be used for both radar and communication systems. Fig. 1.9 shows such a system described in [16]. In the communication mode, the transmitter sends out a RF pulse train modulated using any scheme in Fig. 1.8. The receiver generates a series of RF pulses with exactly the same shape and intervals, called template signal, to correlate with received pulses in order to detect the transmitted information. The received signal time delay is normally unknown between two communicating users, a synchronization process is needed to align the

template pulse train and received signal, which is the function of the synchronization loop.

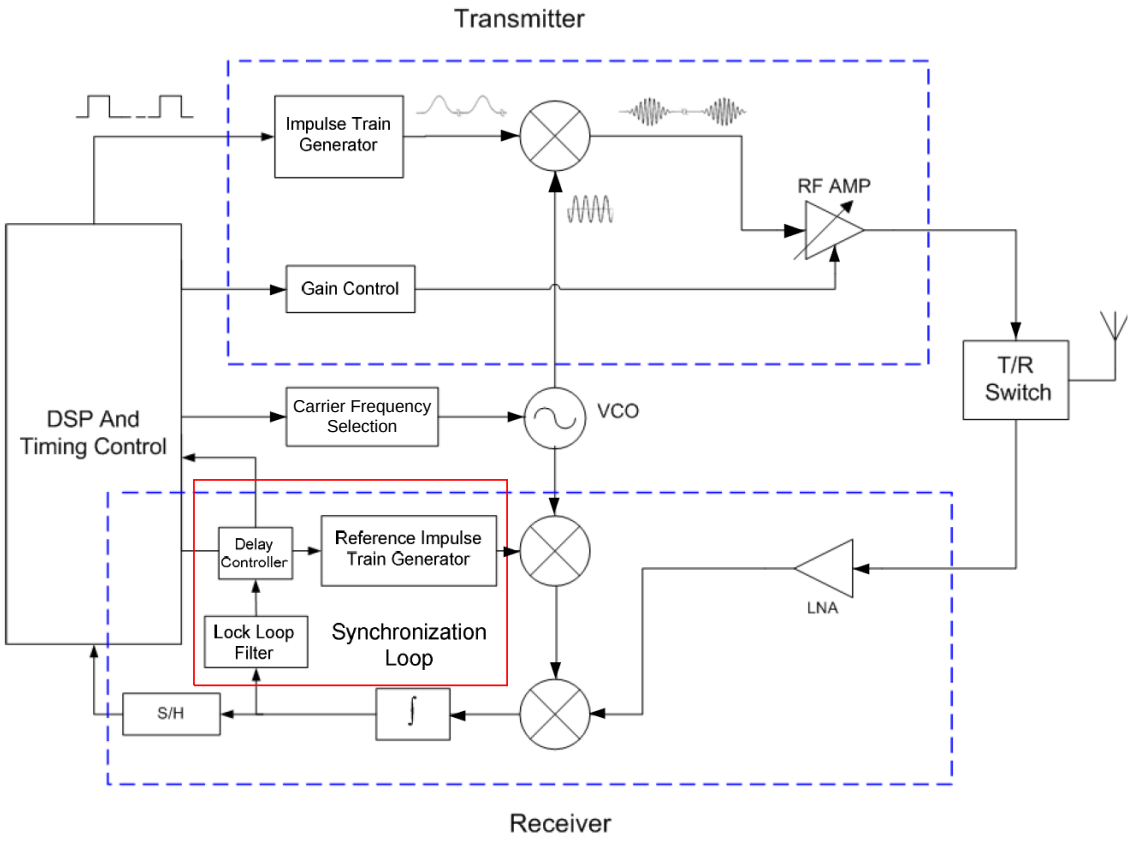


Fig. 1.9. System architecture used for both radar and communication systems.

In the radar mode, the transmitter periodically broadcasts RF pulses with a lower pulse repetition frequency (PRF). The same mechanism is used in the receiver to detect the received signals as in the communication mode. That is, the same transmitted signal will be used as the template signal at receiver side to correlate with the received signal,

except that the delay time is known of multiple of the time gate which is equal to the pulse width.

1.4 Dissertation Organization

This dissertation presents several new circuit architectures and techniques to improve performance of some key CMOS and BiCMOS RFIC circuits operating at RF, microwave and millimeter-wave frequencies, and the development of a new millimeter-wave concurrent dual-band transmitter working at K and Ka bands for short-range radar and communication systems.

Chapter II begins with an overview of mixer fundamentals, and then presents complete designs and measurements of two SiGe up-conversion mixers using active double-balanced Gilbert cells. Design procedure, parameter trade-off, simulation, and layout issues are discussed. Chapter III presents novel circuit architectures for ultra-wideband active baluns. The techniques for parasitic neutralization and compensation used to keep the active baluns well-balanced over a wide frequency range from DC up to millimeter-wave regimes are analyzed in detail. In chapter IV, a new RF switch architecture possessing ultra-high isolation and possible gain is introduced. In this new architecture, the RF leakage cancellation technique is implemented to significantly improve the isolation of the switch. A graphical analysis based on the insertion loss and isolation contours enabling selection of the optimum sizes for transistors in the series-shunt switches is also presented. In addition, several techniques for improving RF switch performance are covered, such as using deep-n-well transistors, floating transistor body

and using synthetic transmission lines. Chapter V presents a new class of concurrent dual-band impedance matching networks along with the technique for synthesizing them, and the detailed design of a new millimeter-wave concurrent dual-band power amplifier. Chapter VI describes the design of a new SiGe BiCMOS concurrent dual-band transmitter for short-range high-rate communication and high-resolution radar systems. The detailed design of some building blocks including image reject filters, RF-pulse formers, pulse generators and PRF clock generator is presented. In Chapter VII, the contribution of this dissertation is summarized.

CHAPTER II

UP-CONVERSION MIXER

This chapter begins with an overview of mixer fundamentals, and then presents complete designs and measurements of two SiGe up-conversion mixers using active double-balanced Gilbert cells. The designed mixers works as source generators to produce 24.5- and 35-GHz CW signals for the transmitter. Design procedure, parameter trade-off, simulation, and layout issues are discussed.

2.1 Introduction

Mixers are used to perform the frequency conversion by multiplying two signals in wireless systems. In the receiver, the mixer down-converts the receiving signal from the radio frequency (f_{RF}) to baseband or intermediate frequency (f_{IF}). On the other hand, in the transmitter, the mixer up-converts the transmitting signal from the baseband or intermediate frequency to radio frequency. The mixers are also used as source generators to synthesize the very high frequencies signals from low-frequency signals.

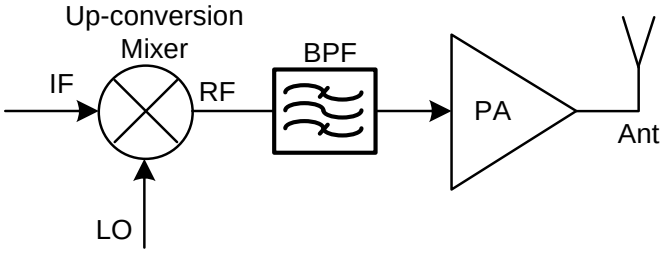


Fig. 2.1. Simple transmitter architecture using up-conversion mixer.

As shown in Fig 2.1, the up-conversion mixer translates the transmitting signal from the low frequency, f_{IF}, to high frequency, f_{RF}, by multiplying it with a local oscillator (LO) signal. The RF signal is then amplified by the power amplifier and transmitted using the antenna. The up-conversion mixer is an important building block in the transmitter since it determines the performance of the transmitting signal, and hence the system. The transmitted RF signals are required to be free of spur and in high power. To this end, the up-conversion mixer needs to exhibit high gain, low noise, high linearity, high port-to-port isolation and high sideband suppression.

This chapter begins with basic principles of mixers, and then presents the analysis of the active balanced mixers. Finally, two up-conversion mixers using the double-balanced Gilbert mixer cells are designed and measured.

2.2 Mixer Fundamentals

The fundamental operation of a mixer is the multiplication of two signals to generate other signals with converted frequencies. Fig 2.2 shows the basic model of an up-conversion mixer multiplying the IF and LO signals. From basic trigonometry, the product of two sinusoid signals produces the sum and difference frequencies at the RF output port as

$$V_{RF} = \frac{A_{IF}A_{LO}}{2}\left(\cos(\omega_{IF} + \omega_{LO}) + \cos(\omega_{IF} - \omega_{LO})\right) \tag{2.1}$$

where A_{IF} and ω_{IF} are the amplitude and frequency of the IF signal, and A_{LO} and ω_{LO} are the amplitude and frequency of the LO signal, respectively.

Based on the operating frequency of systems, the higher sideband component of $\frac{A_{IF}A_{LO}}{2}\cos(\omega_{IF}+\omega_{LO})$ or lower sideband component of $\frac{A_{IF}A_{LO}}{2}\cos(\omega_{IF}-\omega_{LO})$ is selected.

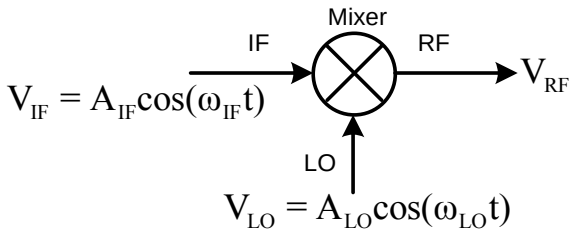


Fig. 2.2. Ideal multiplier model showing fundamental operation of a mixer.

Mixers can be implemented using nonlinear or commutating (switching) circuits. The nonlinearity-based mixers employ the cross-modulation in nonlinear devices to perform the mixing. On the other hand, commutation-based mixers employ the switching mechanism to change periodically the sign of the input signal under the control of a large LO signal.

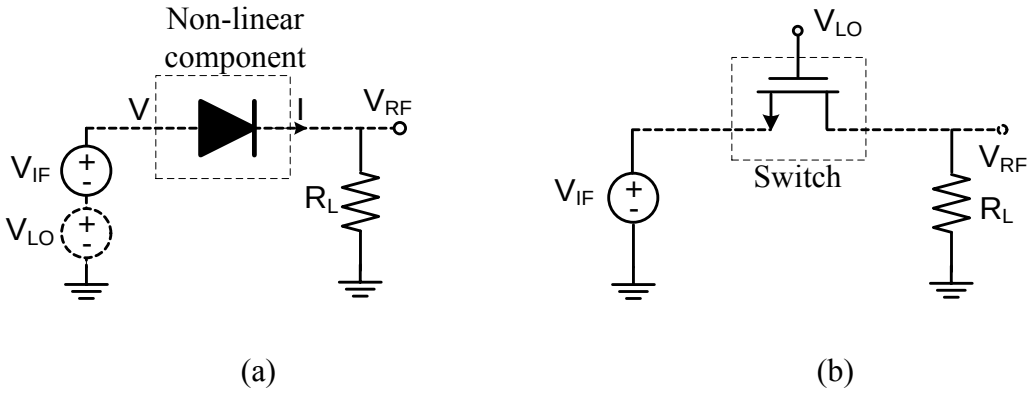


Fig. 2.3. Implementation of mixers using nonlinear (a) and switch (b) circuits.

Transistors or diodes can be used as nonlinear components to implement non-linearity based mixers. The two signals to be mixed are combined and applied to the nonlinear circuits. Fig. 2.3 (a) shows a mixer using the nonlinear characteristic of diode. The I-V characteristic of the nonlinear circuit can be presented as

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + \cdots \tag{2.2}$$

where V is the sum of the IF and LO signals. Based on the equation (2.2), the obtained RF signal consists of the sum, difference and other unwanted frequency components. A filter following the mixer selects the wanted RF signal. In the another implementation using transistors, two mixing signals can be applied separately to two control inputs, for example, to the base and emitter of bipolar transistors or to the gate and source of field-effect transistors.

In commutation-based mixers, switches are turned on and off by a squared wave LO signal, and the RF signal is obtained from the polarity-commutated IF signal when the switches periodically are on and off at the LO frequency. The RF signal then is the product of the IF signal and a unipolar or bipolar square wave with the frequency of ω_{LO}, for balanced or unbalanced mixers, respectively. Fig. 2.3(b) shows an unbalanced mixer based on switching.

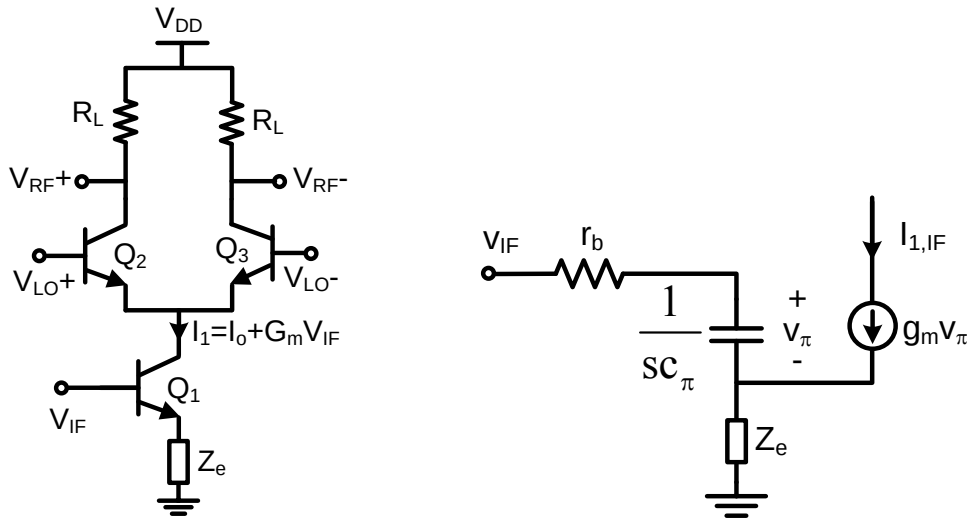
With significant advantages of conversion gain and port-to-port isolation, commutation-based mixers are preferred in RFIC. In term of conversion gain, mixers can be categorized into passive and passive mixers. The passive mixers can be implemented using diodes or transistors [17]. They have simple structures, high linearity, high working frequency and easiness of design, e.g. no stability issue, but have

no conversion gain. On the other hand, the active mixers can provide the gain, hence reducing the noise contribution of subsequent stages. The active single and double-balanced mixers are the most common types of active mixers used in the RFIC design.

2.3 Active Mixer Analysis

2.3.1 Conversion Gain

Fig 2.4 shows the schematic of a single-balanced active mixer. It consists of a gain stage (Q_1, Z_e), switching stage (Q_2 and Q_3) and load R_L. The LC tank load can be used to increase the voltage headroom for the transistors and gain for the mixer. Z_e, which can be an inductance or resistance, is the degenerative impedance used to increase the linearity for the mixer. The gain stage is a transconductance amplifier used to amplify the IF signal, V_{IF}, to compensate the loss due to the switching operation and determine the gain for the mixer. Transistors in the switching stage are turned on and off by the LO signal to perform the mixing operation. The LO signal has to be large enough to fully switch on and off transistors in the switching stage to minimize the noise contribution from the switching stage. The transistor Q_1, Q_2 and Q_3 are biased at the DC currents of I_0, $I_0/2$ and $I_0/2$ respectively.



(a) (b)

Fig. 2.4. Active single-balanced mixer (a) and equivalent circuit of the gain stage with base resistance r_b, base-collector capacitance c_π and transconductance g_m (b).

The gain stage converts the IF voltage to IF current, $I_{1,IF}$, which is then commutated by two transistors in the switching stage at the frequency of ω_{LO}. From Fig. 2.4(b),

$$V_{IF} = \left(r_b + \frac{1}{sC_\pi} \right) V_\pi sC_\pi + Z_e \left(V_\pi sC_\pi + g_m V_\pi \right) \tag{2.3}$$

$$V_\pi = \frac{V_{IF}}{sC_\pi \left(r_b + \frac{1}{sC_\pi} + Z_e(1 + \frac{g_m}{sC_\pi}) \right)} \tag{2.4}$$

Making use (2.4), the IF current at the collector of Q_1 is calculated as

$$I_{1,IF} = g_m V_\pi = \frac{g_m V_{IF}}{sC_\pi \left(r_b + \frac{1}{sC_\pi} + Z_e(1 + \frac{g_m}{sC_\pi}) \right)} = G_m . V_{IF} \tag{2.5}$$

where $$G_m = \frac{g_m}{sc_\pi\left(r_b + \frac{1}{sc_\pi} + Z_e(1+\frac{g_m}{sc_\pi})\right)} \quad (2.6)$$

G_m in (2.6) is the total transconductance of the gain stage.

The current at the collector of Q_1 consists of two components, DC and IF currents as

$$I_1 = I_0 + I_{1,IF} = I_0 + G_m.V_{IF} \quad (2.7)$$

The mixing operation of the mixer is performed by turning on and off two transistors Q_2 and Q_3 in the switching stage using the large LO signal, V_{LO}. The LO signal can be a square wave or sinusoidal signal. As $V_{LO} > 0$, transistor Q_2 is on and transistor Q_3 is off. In this case, the output RF signal, V_{RF}, is calculated as

$$V_{RF} = -R_L(I_0 + G_m V_{IF}) \quad , V_{LO} > 0 \quad (2.8)$$

As $V_{LO} < 0$, transistor Q_2 is off and transistor Q_3 is on. In this case, the output RF signal, V_{RF}, is calculated as

$$V_{RF} = R_L(I_0 + G_m V_{IF}) \quad , V_{LO} < 0 \quad (2.9)$$

It is observed from (2.8) and (2.9) that the RF signal is obtained from toggling the signal term $R_L(I_0+G_mV_{IF})$ between positive and negative values. This is equivalent to multiplying the term $R_L(I_0+G_mV_{IF})$ with a bipolar square wave S(t) having the amplitude of 1 and frequency of ω_{LO} as shown in Fig. 2.5.

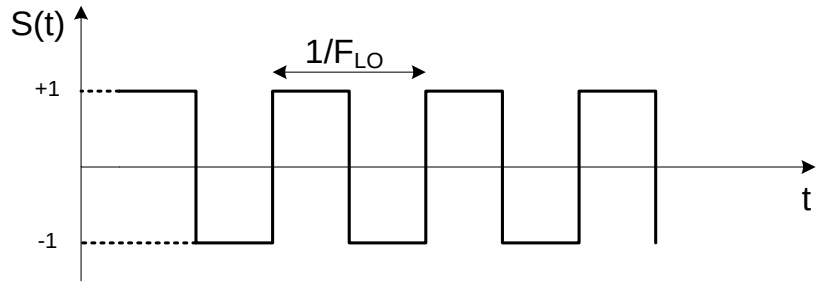


Fig. 2.5. Bipolar square-wave signal representing for the switching operation.

The RF output signal is then expressed as

$$V_{RF}(t) = R_L(I_0 + G_m V_{IF})S(t) \tag{2.10}$$

In form of Fourier series, S(t) is expressed as

$$S(t) = \frac{4}{\pi}\mathrm{Cos}(\omega_{LO}t) - \frac{4}{3\pi}\mathrm{Cos}(3\omega_{LO}t) + \frac{4}{5\pi}\mathrm{Cos}(5\omega_{LO}t) \ . \ . \ . \tag{2.11}$$

Making use of (2.11), $V_{RF}(t)$ in (2.10) is expressed as

$$V_{RF}(t) = R_L(I_0 + G_m V_{IF})\left(\frac{4}{\pi}\mathrm{Cos}(\omega_{LO}t) - \frac{4}{3\pi}\mathrm{Cos}(3\omega_{LO}t) + \frac{4}{5\pi}\mathrm{Cos}(5\omega_{LO}t) \ . \ . \ .\right) \tag{2.12}$$

With the first harmonic LO mixing, the fundamental component of S(t) is considered. Making use $V_{IF}(t) = A_{IF}\mathrm{Cos}(\omega_{IF}t)$, $V_{RF}(t)$ in (2.12) becomes

$$V_{RF}(t) = R_L\frac{4}{\pi}\left(I_0 + G_m A_{IF}\mathrm{Cos}(\omega_{IF}t)\right)\mathrm{Cos}(\omega_{LO}t) \tag{2.13}$$

$$V_{RF}(t) = I_0 R_L\frac{4}{\pi}\mathrm{Cos}(\omega_{LO}t) + \frac{2G_m R_L A_{IF}}{\pi}\mathrm{Cos}(\omega_{LO} + \omega_{IF}t) + \frac{2G_m R_L A_{IF}}{\pi}\mathrm{Cos}(\omega_{LO} - \omega_{IF}t) \tag{2.14}$$

The first term in (2.14) represents the LO feed-through and other terms are the sum and difference frequency components resulting from the mixing operation. The

voltage conversion gain, A_v, is defined as the ratio of the desired RF output amplitude to IF input amplitude. Note that two RF and IF signals are located at different frequencies.

$$A_v = \frac{2G_m R_L}{\pi} \tag{2.15}$$

The LO feed-through is the main disadvantage of the single-balanced mixer. Fig. 2.6 shows the circuit topology of the active double-balanced (Gilbert) mixer which eliminates the LO feed-through problem in the single-balance counterpart. The mixer comprises a differential pair gain stage (Q_1 and Q_2) with degenerative impedance Z_e and a differential switching stage (Q_3, Q_4, Q_5 and Q_6). The gain stage amplifies the IF signal while the switching stage performs the multiplying operation which up-converts the signal from IF frequency to RF frequency.

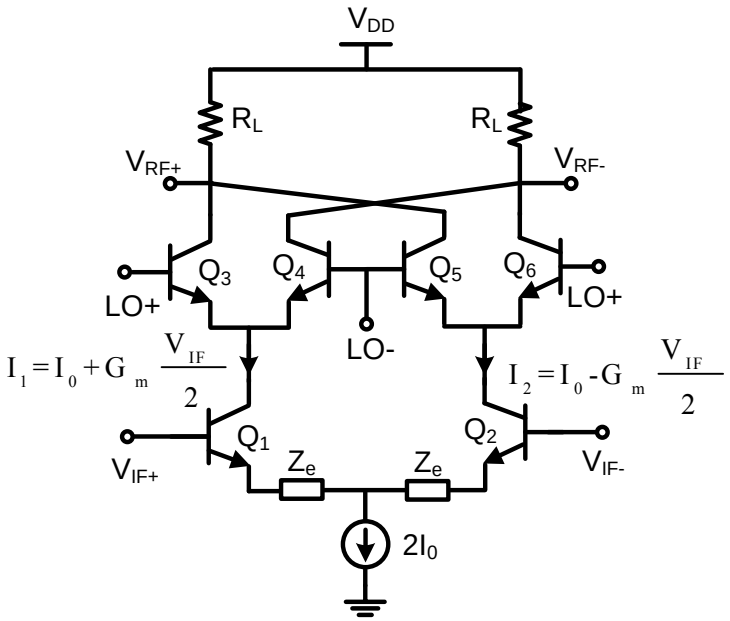


Fig. 2.6. Double-balanced Gilbert mixer schematic.

The gain stage converts the IF voltage to IF currents $I_{1,IF}$ and $I_{2,IF}$ which are then commutated by transistors in the switching stage at the frequency of ω_{LO}. From Fig. 2.6, the currents at the collector of Q_1 and Q_2 are calculated as

$$I_1=I_0+G_m\frac{V_{IF}}{2} \tag{2.16}$$

$$I_2=I_0-G_m\frac{V_{IF}}{2} \tag{2.17}$$

where G_m is the total tranconductance of the gain stage and is calculated in (2.6).

The multiplying operation of the double-balanced mixer is performed by switching transistors in the switching stage. As $V_{LO} > 0$, transistor Q_3 and Q_6 are on and Q_4 and Q_5 are off. In this case, making use (2.16) and (2.17), the RF output voltage $V_{RF}(t)$ is calculated as

$$V_{RF} = R_L(I_2\text{-}I_1) = -G_mR_LV_{IF},\ V_{LO} > 0 \tag{2.18}$$

As $V_{LO} < 0$, transistor Q_3 and Q_6 are off and Q_4 and Q_5 are on. In this case, the RF output voltage $V_{RF}(t)$ is calculated as

$$V_{RF} = R_L(I_1\text{-}I_2) = G_mR_LV_{IF},\ V_{LO} < 0 \tag{2.19}$$

It is also observed from (2.18) and (2.19) that the RF signal is obtained from toggling the signal term $G_mR_LV_{IF}$ between positive and negative values at the frequency of ω_{LO}. This is equivalent to multiplying the term $G_mR_LV_{IF}$ with a bipolar square wave S(t) having the amplitude of 1 and frequency of ω_{LO} as shown in Fig. 2.5.

$$V_{RF}(t) = G_mR_LV_{IF}(t)S(t) \tag{2.20}$$

Making use (2.11) and assume that we just consider the fundamental component of S(t), $V_{RF}(t)$ in (2.20) becomes

$$V_{RF}(t) = \frac{4}{\pi} G_m R_L A_{IF} \mathrm{Cos}(\omega_{IF} t) \mathrm{Cos}(\omega_{LO} t) \tag{2.21}$$

$$V_{RF}(t) = \frac{2G_m R_L A_{IF}}{\pi} \mathrm{Cos}(\omega_{LO} + \omega_{IF} t) + \frac{2G_m R_L A_{IF}}{\pi} \mathrm{Cos}(\omega_{LO} - \omega_{IF} t) \tag{2.22}$$

Equation (2.22) shows that the RF output voltage contains the sum and difference frequency components and no LO feedthrough.

From (2.22), the conversion gain of the double-balanced mixer is calculated as

$$A_V = \frac{2G_m R_L}{\pi} \tag{2.23}$$

Equations of (2.15) and (2.23) show that the conversion gains of single-balanced and double-balanced mixers are equal. High gain in mixers is desired for providing enough IF signal power to the next stage in transceiver systems. Equation (2.23) shows that increasing the total tranconductance and load resistance improves the conversion gain of the mixers.

2.3.2 Noise Figure

Noise figure of up-conversion mixers is defined as a ratio of signal to noise ratio at the IF port to the signal to noise ratio at the RF port of the mixer. Generally, active mixers have three important sources of noise as

Noise already present at the RF: The transistors and resistors in the circuit will generate the thermal noise at the RF frequency. Some of this noise will be at the

output and corrupt the signal. For example, the collector resistors of the switching stage will add noise directly to the signal at the output RF.

Noise at the IF and image frequency: Any noise present at the IF and image frequency will also be mixed up to the RF. For instance, the collector shot noise of transistors in the gain stage at the IF and at the image frequency will both appear at the RF at the output.

Noise at multiples of the LO harmonic frequencies: Any noise that is near a multiple of the LO frequency can also be mixed up to the RF, just like the noise at the IF.

There are two ways to calculate the noise figure of the mixer based on the type of frequency translation modes: double-sideband and single-sideband. The single-sideband noise figure is used in the heterodyne architecture where the single-sideband signal is down or up converted and the image signal is rejected. However, the noise from the image band is converted to the IF band along with the noise from the desired band, making the mixer suffer more noise as compared to the double sideband conversion systems such as direct conversion system.

In the balanced active mixer, the noise comes from the gain stage, switching stage and the load. In the gain stage, the thermal noise due to the base resistance and degenerative resistors and the collector shot noise contribute main components of noise. The transistors in the gain stage need to have large sizes and high currents to reduce the noise figure for the mixer. However, this results in increased DC power consumption.

The noise contribution from transistors in the switching stage is due to the parasitic capacitors at the common node and the on-off transitions of the switching transistors [18]. With the large LO power, the switching transistors are alternately switched between completely off and fully on. When off, the transistors contribute no noise, and when fully on, the switching transistors behave as cascode transistors, which do not contribute the noise significantly. If the switching transistors are not turned on or off abruptly, both transistors in the differential pair are on at the same time, leading to pumping noise to the load; since in this case, they work as a differential amplifier. To reduce the noise contribution from the switching stage, the parasitic capacitors at the common node are minimized and the LO signal is better in the square wave and large amplitude. Using small-size transistors in the switching stage reduces the parasitic capacitance and required LO power as well [19].

2.3.3 Port-to-Port Isolation

Port-to-port isolations are performance metrics characterizing the leakage of signals from one port of the mixer to another. A port-to-port isolation is defined as the ratio of the signal power available at one port to the measured power of that signal at another port of the mixer. In the up-conversion mixer, two types of important leakages are the LO - RF and LO - IF leakages as shown in Fig. 2.7. Since the LO signal is usually high in power, it can easily leak to the RF and IF ports through the substrate and parasitic capacitances of mixers. The large LO leakage signal at RF port can saturates the subsequent circuits such as drive and power amplifiers. In addition, the leakage LO

can be transmitted through the antenna and affects the receiver or pollutes the wireless environment. The LO leakage at the IF port causes self-mixing and generates the DC offsets.

The double-balanced Gilbert mixer exhibits much better port isolation as compared to the single-balanced counterpart. A series resonant L-C network can be used across the outputs of the mixer in Fig. 2.4 and 2.6 to further suppress the LO leakage or get rid of the unwanted sidebands.

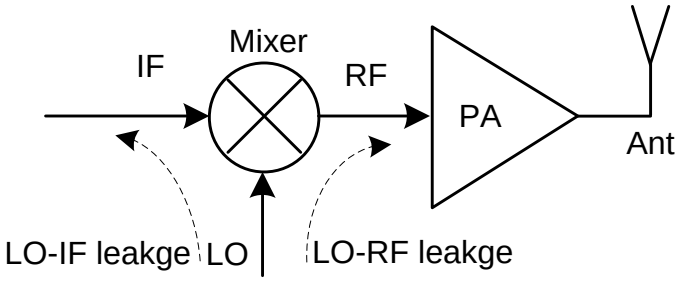


Fig. 2.7. Port-to-port leakage in up-conversion mixer.

2.3.4 Linearity

The linearity of the mixer mainly depends on the linearity of the gain stage. Degenerative inductors or resistors are used to increase the linearity [20]. The linearity is improved by increasing the degenerative impedance or increasing the bias current, hence the tranconductance. Increasing the supply voltage and using the tuned loads instead of resistance loads will increase the gain and linearity for the mixer. The bias voltage at the base of the transistors in the switching stage can be increased to increase the headroom voltage for the transistors in the gain stage, hence increasing the linearity.

2.4 24.5-GHz Mixer Design

The 24.5-GHz mixer designed to generate the 24.5-GHz signal from 21-GHz IF and 3.5-GHz LO signals. The LO leakage is an important issue in the mixer design. The intentional choice of 3.5-GHz LO signal whose frequency is quite far away from the output frequency of 24.5 GHz improves the purity of the output signal in the sense that the possible 3.5-GHz LO leakage signal can be easily removed using a low-Q band-pass filter.

As shown in Fig. 2.8, the 24.5-GHz mixer consists of a single-ended to differential active balun, double-balanced Gilbert mixer cell, differential amplifier and band pass filter (BPF). The input active balun is used to facilitate the wafer characterization in which a single-ended IF signal can be used. The double-balanced Gilbert mixer cell is chosen instead of the single-balanced counterpart to enhance the IF-to-RF and LO-to-RF isolation and even-order suppression. The LC tanks at the outputs of the Gilbert cell are used to boost the gain and form the bandpass responses for the mixer. A differential amplifier, functioning as differential-to-single active balun, is used to convert the differential signal at the output of Gilbert cell to single-ended RF signal for the following stages in the transmitter which are in the single-ended architectures. This amplifier increases the gain and output power for the mixer. The BPF at the output of the mixer passes the 24.5-GHz signal, suppresses the LO, low sideband at 17.5 GHz and mixing product at 35 GHz ($2F_{IF}$-$2F_{LO}$); this 35-GHz signal is an unwanted interference to the other band of the transmitter. In the whole transmitter, the mixer should be preceded with a band-stop filter to reject the image signal at 28 GHz.

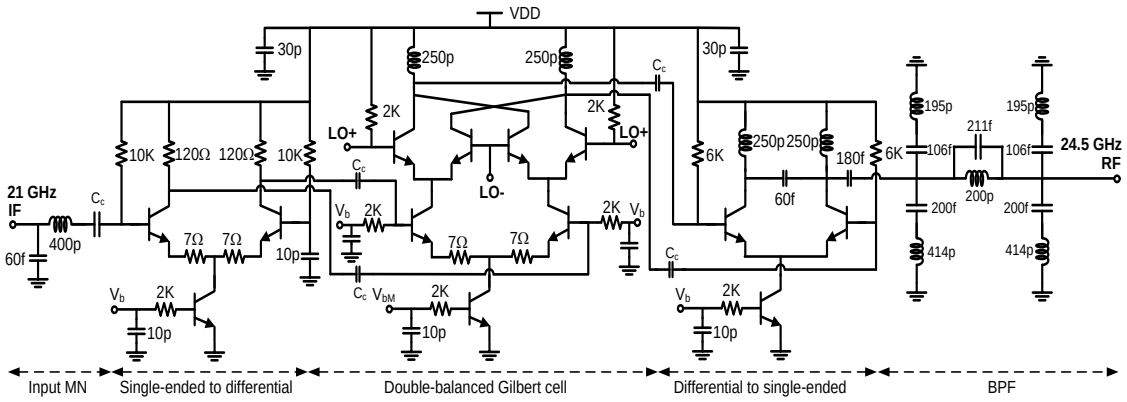


Fig. 2.8. 24.5-GHz mixer schematic.

The design specifications of mixers are different from their applications. In this design, the mixer is used as a source generator; therefore it is designed to have high linearity, high harmonic and spur rejection, and reasonable noise figure using a DC supply voltage of 1.8V. Table 2.1 shows design specifications for the 24.5-GHz mixer.

Table 2.1 24.5-GHz mixer design parameters.

IF frequency (GHz)	21	Noise figure (dB)	9
LO frequency (GHz)	3.5	$P_{out,1dB}$ (dBm)	-5
RF frequency (GHz)	24.5	LO power (dBm)	0
Power conversion gain (dB)	20	LO-RF Isolation (dB)	30
Side-band suppression (dB)	30	IF-RF Isolation (dB)	-

The 24.5-GHz mixer is designed using the Jazz 0.18-μm BiCMOS process [21] which has 6 metal layers and the substrate resistivity of 10 Ω.cm. The SiGe HBT transistors used for the mixer have the cut-off frequency of 200 GHz which is well suited

for 24.5 GHz design. All the on-chip inductors, vias and interconnecting lines are designed using the topmost metal layer and simulated using the EM simulator IE3D [22]. The mixer is simulated, optimized and laid-out using Cadence [23].

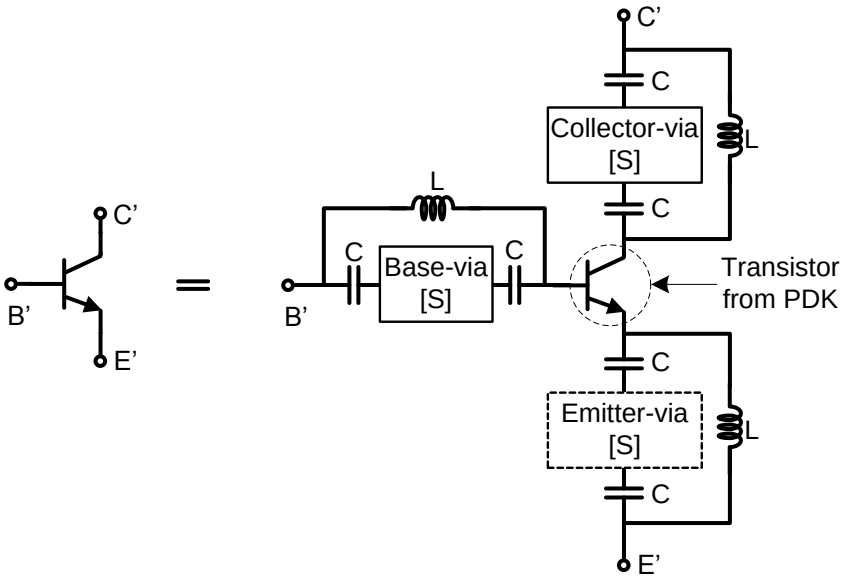


Fig. 2.9. Transistor model including vias S-parameters. C's and L's are very large capacitors and inductors used to block the DC and AC signals.

At high frequencies, the effects of short vias connecting the transistor terminals from metal 1 or 2 to metal 6 are significant. It is important to do the EM simulation for those vias and include their S-parameters into the active device for use to take the account of vias effects. It is noted that the parasitic components from vias cannot be extracted from cadence RCX extraction. Fig. 2.9 shows the transistor model including S-parameters of the vias connecting to the base, collector and emitter terminals of the original transistor from the package design kit (PDK). Large capacitors, C, and inductors, L, are used as DC and AC blocking components, respectively. The post-layout

simulation results for the circuits with the use of this model and S-parameters of other passive components, including interconnects, are more reliable than those with the use of Cadence RCX extraction.

2.4.1 Single-ended to Differential Active Balun

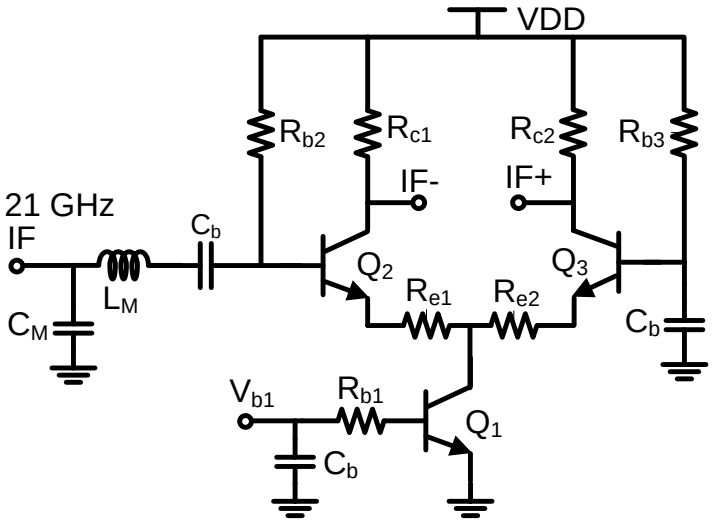


Fig. 2.10 Single-ended to differential active balun.

The active balun shown in Fig. 2.10 is designed to convert the 21-GHz IF single-ended signal to differential one. It consists of a differential pair (Q_2 and Q_3) and a current source (Q_1). One input of the differential pair is single-ended and another is grounded through a bypass capacitor. Resistor loads R_{c1} and R_{c2} are used instead of inductors to save the area. The amplitude and phase balance of the active balun is strongly affected by the parasitic capacitors existing at the common node, hence the size of transistor Q_1 of the current source. Therefore, there is a trade-off between the balance, which requires

the small size for Q_1, and the gain, which requires the large size for Q_1, of the active balun. The small size of transistor Q_1 is chosen to give low parasitic capacitance while providing a DC current of 6 mA to the differential pair. The values of Rc's are chosen so that the DC voltages dropped on Rc's are 0.6 V; hence providing enough headroom voltages for transistors Q_1, Q_2 and Q_3. Transistors Q2 and Q3 are biased to work at highest f_T at the DC currents of 3 mA. Their sizes are chosen to be 3 um. The degenerative resistors R_{e1} and R_{e2} are used to increase the linearity for the active balun [24]. The input matching network consisting of L_M and C_M is design to match the input of the active balun with 50 Ω at 21 GHz. The table 2.2 shows the circuit element values for the active balun.

Table 2.2 Circuit element values of the active balun

Circuit Element	**Value**	**Element**	**Value**	**Element**	**Emitter Area**
R_{c1}, R_{c2}	200 Ω	C_b	5 pF	Q_1	0.15x6 μm^2
R_{b1}	2 KΩ	VDD	1.8 V	Q_2, Q_3	0.15x3 μm^2
R_{b2}, R_{b3}	12 KΩ	Vb	1.3 V		
L_M	400 pH	C_M	60 pF		

2.4.2 Double-balanced Gilbert Mixer Cell

The double-balanced Gilbert mixer cell shown in Fig. 2.11 is designed for high gain and high linearity while achieving a reasonable noise figure. It consists of an IF gain stage (Q_5 and Q_6), LO switching stage (Q_7, Q_8, Q_9 and Q_{10}) and current source (Q_4).

The inductors L_{c1} and L_{c2} are used to resonate all parasitic capacitors at the outputs of the mixer and form the tuned loads. Using the tuned loads instead of resistor loads boosts the gain, increases the headroom for transistors; hence increasing the linearity for the mixer and partly rejecting the unwanted output frequency components through their band pass frequency responses.

The voltage gain of the mixer is proportional to the transconductance of the transistors in the IF gain stage and the equivalent parallel resistances, R_L's, of the loading inductors L_{c1} and L_{c2} as shown in the equation (2.23)

$$Av = \frac{\pi}{2} g_m R_L$$

Where $R_L = R_{L1} = R_{L2} = Q_L \omega L_{c1} = Q_L \omega L_{c2}$, and Q_L is the quality factor of inductors.

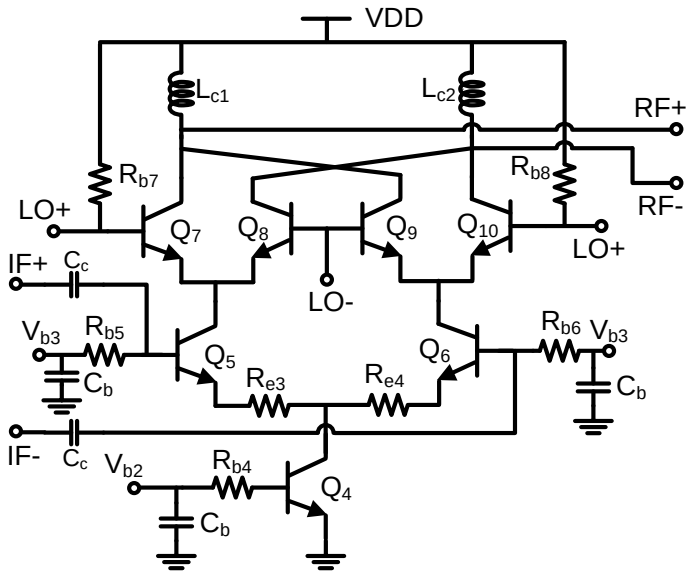


Fig. 2.11. Double-balanced Gilbert mixer celll.

The inductors L_{c1} and L_{c2} are designed using the thickest topmost metal layer and optimized using the EM simulator IE3D to get high quality factors, resulting in high gain for the mixer. The inductor quality factors of 16 are obtained.

The large sizes and large bias currents of transistors Q_5 and Q_6 in the IF gain stage are desired to achieve the high gain, high linearity and low noise figure for the mixer. As there is always a trade-off between the gain and the power consumption in the IF gain-stage design, the iterative optimization is performed to choose the sizes, bias currents for transistors. Transistors having the configuration of one emitter, two base and two collector contacts (CBEBC) with emitter area of 0.15x8 μm^2 are chosen for Q_5 and Q_6. They are biased at the currents of 6.4 mA for maximum f_T. Degenerative resistors R_{e3} and R_{e4} of 10 Ω are used to further improve the linearity of the IF stage. As the noise of the mixer is mainly contributed from the IF stage as long as the transistors in the LO stage are switched abruptly [19], large sizes of Q_5 and Q_6 with configuration of two base contacts lower the thermal noise contribution due to small base resistances.

Transistor Q_4 has the size of 0.15x10 μm^2 and is biased at the current of 12.8 mA to sufficiently provide the current for the whole mixer cell. The small size of Q_4 results in small parasitic capacitance hence increasing the common mode rejection for the mixer.

The sizes of transistors in the LO switching stage (Q_7, Q_8, Q_9 and Q_{10}) are chosen to be small with multi base and collector configuration for fast switching [17]. Smaller sizes of switching transistors result in lower needed LO power but degrease the linearity as well due to lower current handling. Fast switching for LO switching stage results in

improving the linearity and reducing the noise contribution from LO switching stage transistors. The simulation shows that the sizes of 0.15x4 μm^2 for transistors in the switching stage give lowest noise figure with a low LO power of -4 dBm. All bypass capacitors C_b's have values of 5pF. The coupling capacitors C_c's in the IF stage are 200 fF. The mixer core consumes a 12.8-mA DC current from a supply voltage of 1.8V. Table 2.3 shows the designed component values.

Table 2.3 Circuit element values of Gilbert mixer cell

Element	**Value**	**Element**	**Value**	**Transistor**	**Emitter Area**
L_{c1}	250 Ω	C_c	200 fF	Q_4	0.15x10 μm^2
R_{b3}, R_{b4}	2 KΩ	VDD	1.8 V	Q_5, Q_6	0.15x8 μm^2
R_{b5}	1 KΩ	R_{e2}	10 Ω	Q_7, Q_8, Q_9, Q_{10}	0.15x4 μm^2

2.4.3 Differential Amplifier

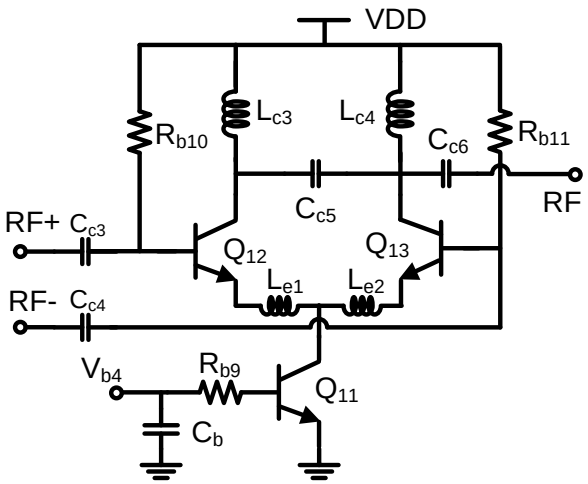


Fig. 2.12. Differential amplifier schematic.

A differential amplifier, as shown in Fig. 2.12, integrated with a passive balun is cascaded with the Gilbert mixer core to increase the gain and output power, and convert the differential signal at outputs of the mixer cell to single-ended signal. Transistors Q_{12} and Q_{13} are designed with the large emitter areas of 0.15x8 μm^2 and biased at DC currents of 7 mA for high gain and high linearity. Transistor Q_{11} biased at 14 mA functions as a DC current source for the differential amplifier. Loading inductors L_{c3} and L_{c4} are optimized to tune all the parasitic capacitors at the collectors of Q_{12} and Q_{13}, and form LC tanks which are for signal selectivity, and sideband and LO suppression. L_{c3}, L_{c4} are also used with C_{c3} to make a current combiner functioning as a passive balun to convert the differential to single-ended signal [17]. The capacitors C_{c3}, C_{c4} and C_{c6} are used to provide the matching at the input and output of the differential amplifier, respectively. Degenerative inductors L_{e1} and L_{e2} are used to increase the linearity for the amplifier. There is the trade-off between the gain and the linearity due to the values of degenerative inductors. The value of L_{e1} and L_{e2} are chosen as 25 pH after several iterations. L_{e1} and L_{e2} are implemented using line inductors. Values of elements used in the differential amplifier are shown in the Table 2.4.

Table 2.4 Circuit element values of the differential amplifier

Element	**Value**	**Element**	**Value**	**Transistor**	**Emitter Area**
$L_{c3,}$ L_{c4}	250 Ω	C_{c3}, C_{c4}	200 fF	Q_{11}	0.15x10 μm^2
$R_{b10,}$ R_{b11}	6 KΩ	C_5	60 fF	Q_{12}, Q_{13}	0.15x8 μm^2
R_{b9}	2 KΩ	L_{e1}, L_{e2}	25 pH	VDD	1.8 V

2.4.4 24.5-GHz Band Pass Filter

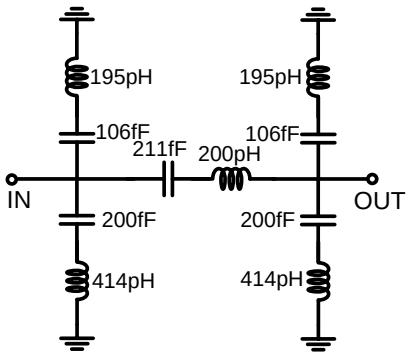


Fig. 2.13. 24.5-GHz band-pass filter.

A band-pass filter at the output of the differential amplifier is needed to select 24.5-GHz RF signal, and suppress low sideband at 17.5 GHz and mixing product at 35 GHz. The simulation results show that the PBF exhibits the insertion loss of 1.8 dB at 24.5 GHz and rejection of 34 and 37 dB at 17.5 and 35 GHz respectively.

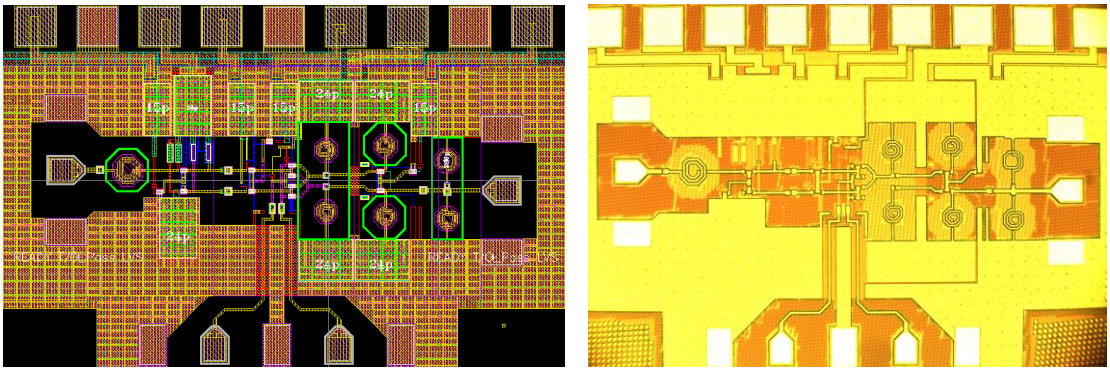
2.4.5 Mixer Optimization, Layout and Fabrication

The design of mixers at high frequencies is not a straight forward procedure as there are many trade-off parameters. At the first step, the ideal components including PDK transistors, resistors, capacitors and inductors can be used to design and optimize the mixer to meet the required specifications. The optimization of the mixer requires the understanding of the trade-off among mixer parameters including gain, linearity, noise figure, power consumption and LO power level. The real implementations of passive components which determine the mixer performance and chip area are considered as

well.

After the optimization using ideal components, the real components need to be used. Namely, the transistors should be replaced by the models in Fig. 2.9, the ideal capacitors are replaced with the real capacitors from the PDK, and the ideal inductors are replaced by their S-parameters obtained from EM-simulation based design. At this step, the circuit performance is normally changed and another optimization process is carried out.

The layout of the mixer produces additional interconnections which need to be modeled using EM simulators and included into the circuit simulation. The layout process may modify the designed inductors as well. The completion of the mixer design requires the interaction and several iterations of going back and forth among of layout, EM and circuit simulations. During this process, the layout also needs to be optimized to reduce parasitics as well as improve performance due to better electrical or physical (e.g., layout symmetry) characteristics



(a) (b)

Fig. 2.14 24.5-GHz mixer layout (a) and microphotograph (b).

The layout of the mixer is done in Cadence Virtuoso using Jazz 0.18-μm BiCMOS process. Figure 2.14 (a) shows the layouts of the complete 24.5-GHz mixer. The layout is done as symmetrical as possible in order to preserve the symmetry needed for the Gilbert mixer core to work properly. The size of the complete mixer is around 1.2mm x 0.9mm while that of the Gilbert mixer core is just 600μm x 350μm. As can been seen, most of the chip area is occupied by the passive components (inductors and interconnects). Metal 6 (top metal layer) is used for the IF, LO and RF signals. A strong ground consisting of six stacked metal layers is around the mixer. Metal 5 and metal 6 are used for interconnects of at LO and RF ports. Poly blocking layers are inserted underneath all inductors to prevent the poly dummies added during the fabrication process which affect the inductor performance. The microphotograph of the 24.5-GHz mixer is shown in Fig. 2.14(b).

2.4.6 24.5-GHz Mixer Performance

The 24.5-GHz designed mixer was measured on-wafer using Rhode & Schwarz vector network analyzer and Cascade probe station. The short-open-load-thru calibration method along with Microtech's impedance standard substrate standards was used. The 24.5-GHz mixer consumes a current of 40 mA from a power supply of 1.8 V.

Input, Output Return Losses and Stability

Stability is an important issue and should be the first check in the mixer design. Stability is confirmed using S-parameter (SP) simulation and measurement in which the

mixer's LO port is terminated with 50-Ω. In this case, the mixer is considered as a two-port amplifier. The IF and RF ports are the input and output ports, respectively. The S-parameter simulation and measurement is setup with small input power of -40 dBm. Simulated and measured results show that the mixer is unconditional stable from DC to 80 GHz with the mixer's stability K and B_1 factors larger than 1 and 0, respectively.

Fig. 2.15 shows the simulated and measured input and output return losses versus the frequencies. The measured input return loss is 13 dB at the IF frequency of 21 GHz and the measured ouput return loss is 9 dB at the RF frequency of 24.5 GHz. The mesured and simulated results are in good agrement.

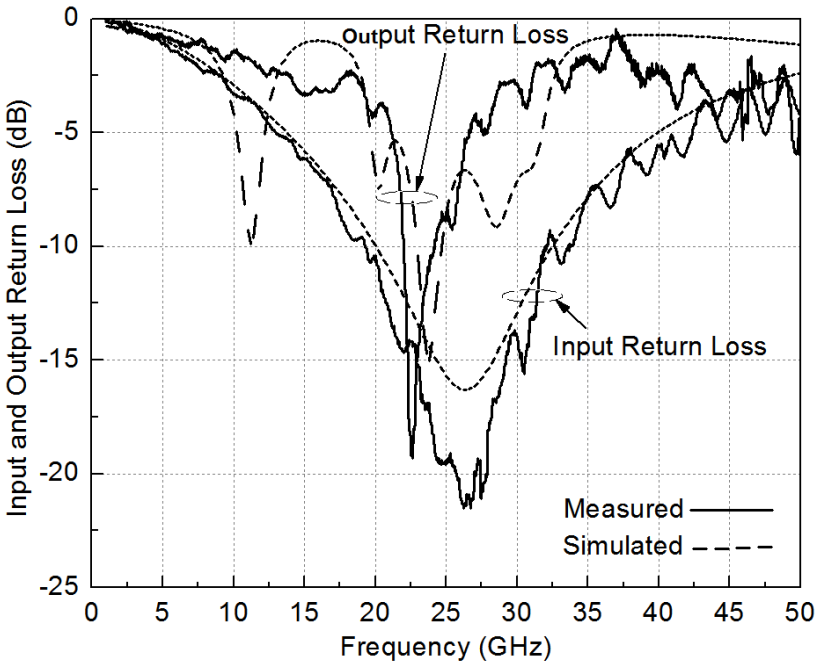


Fig. 2.15 24.5-GHz mixer input and output return losses.

Conversion gain versus the LO power and RF frequency

The simulation and measurement for the conversion gain versus the LO power is performed to determine the optimum LO power which maximizes the conversion gain of the mixer. The frequency and power of IF signal are set to 21 GHz and -40 dBm, respectively. The LO frequency is fixed at 3.5 GHz. The LO power is swept from -20 to 5 dBm with the step of +1 dBm. The conversion gain is calculated as the ratio of the 24.5-GHz RF output power and 21-GHz IF input power. The simulated and measured conversion gains versus LO power are in good agreement as shown in Fig. 2.16. The simulated result shows that the maximum conversion gain of 25.2 dB is obtained with the LO power of -4 dBm while the measured result shows that the maximum conversion gain of 25.7 dB is obtained with the LO power of -2 dBm. This measured optimum LO power of -2 dBm is used for subsequent measurements. The low measured LO power is achieved due to the selection of small sizes of transistors in the LO switching stage.

The simulation and measurement for the conversion gain versus the RF frequency are carried out to characterize the frequency response of the mixer. The LO frequency and power are fixed at 3.5 GHz and -2 dBm respectively. The IF power is set to -40 dBm and the IF frequency is swept from 14.5 to 29.5 GHz; therefore the resultant RF frequency is from 18 to 33 GHz. The conversion gain is calculated as the ratio of the RF output power and IF input power. Fig. 2.17 shows the conversion gain versus the RF frequency. The measured results show that the mixer exhibits the conversion gain of 25.7 dB at the RF frequency of 24.5 GHz, and the maximum conversion gain of 29.5 dB is located at 22.5 GHz. The peak of the measured frequency response is 2 GHz shifted

down as compared to simulated one. This may be due to the shifted frequency response of the BPF.

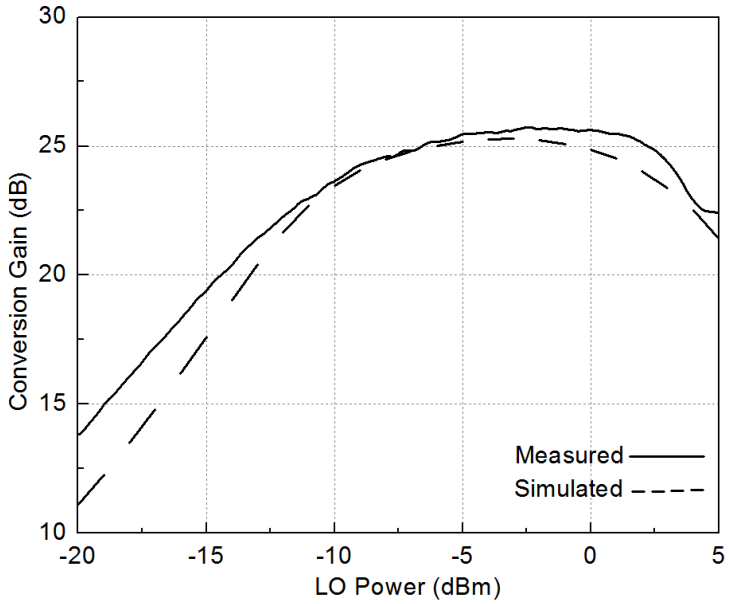


Fig. 2.16. Measured and simulated conversion gain 24.5-GHz mixer versus LO power.

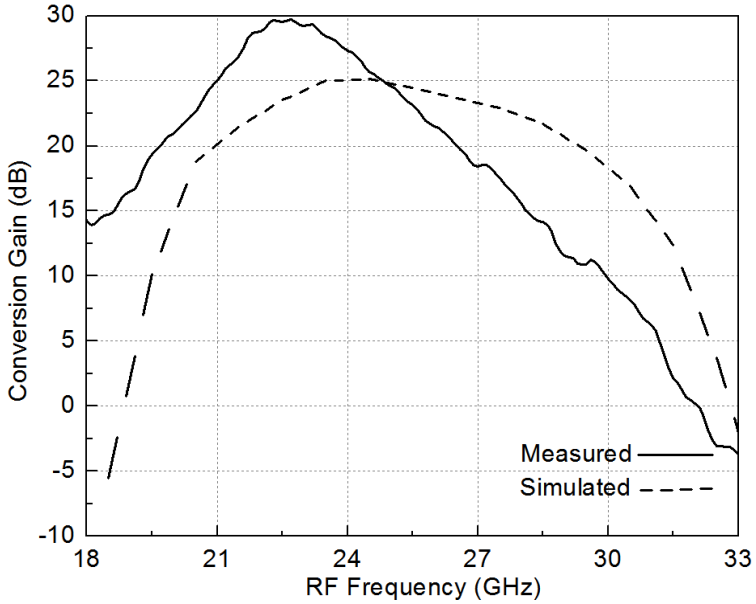


Fig. 2.17. Measured and simulated conversion gain of 24.5-GHz mixer versus RF frequency.

Noise Figure

The noise figure simulation for the complete mixer is performed using harmonic balance. The LO frequency and power are fixed at 3.5 GHz and -2 dBm respectively. The IF power is set to -40 dBm and the IF frequency is swept from 15 to 30 GHz. Fig. 2.18 shows the simulated noise figure of the mixer versus the IF input frequency. At 21 GHz, the noise figure is 8.7 dB which is a reasonable value for the up-conversion mixer and meets the design requirement.

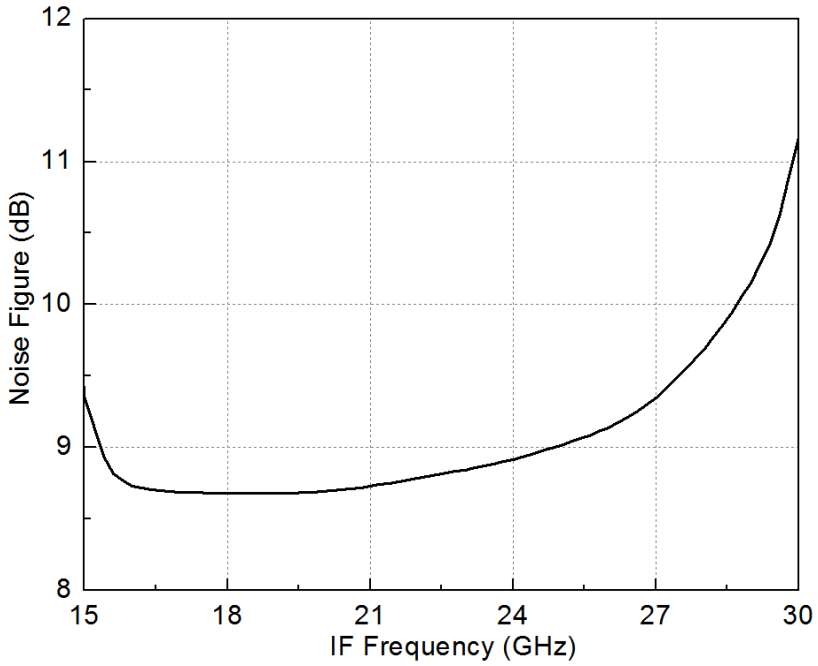


Fig. 2.18. Simulated noise figure of 24.5-GHz mixer versus IF frequency.

Mixer performance versus the IF input power

Fig. 2.19 shows the simulated and measured results of the gain and output power versus the IF input power. In the simulation and measurement, the LO frequency and

power are fixed at 3.5 GHz and -2 dBm, respectively, the IF frequency is set to 21 GHz and the IF power is swept from -40 to -10 dBm. The simulated and measured results are in very good agreement. The simulated results show that 24.5-GHz mixer exhibits the maximum gain of 25.7 dB, 1-dB input power, $P_{in,1dB}$, of -23 dBm, 1-dB output power, $P_{out,1dB}$, of 1.36 dBm, and maximum output power of 2.7 dBm.

Fig. 2.20 shows the isolations and low-sideband suppression versus the IF input power. The measured results shows that the LO-IF and LO-RF isolations are higher than 30 dB. The IF-RF isolation higher than 0 dB when the IF input power is larger than 20 dBm. The low-sideband suppression is defined as the power ratio of the low-sideband at 17.5 GHz and the high sideband at 24.5 GHz. The measured low-sideband suppression is higher than 10 dB over the full range of IF input power. Due to the discrepancy of the fabricated BPF compared to the designed one, the sideband suppression is not very high as designed.

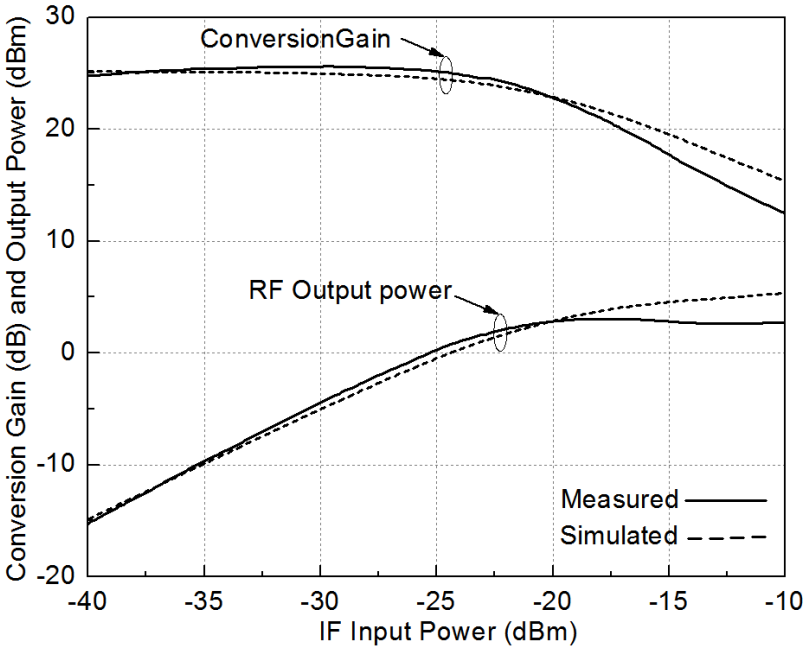


Fig. 2.19. Gain and RF output power of 24.5-GHz mixer versus IF input power.

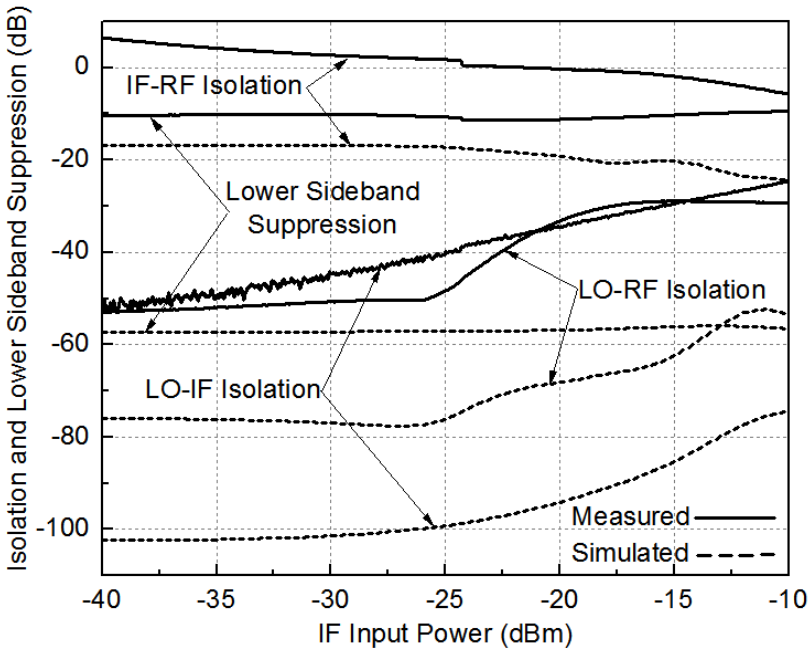


Fig. 2.20. Isolation and lower sideband suppression of 24.5-GHz mixer versus IF input power.

Fig. 2.21 shows the measured output signal spectrum of 24.5-GHz mixer with 21-GHz IF input power of -20 dBm, LO frequency of 3.5 GHz and LO power of -2 dBm. It can be seen that the output spectrum contains a 24.5-GHz signal with the power of 0 dBm, 17.5-GHz low-sideband signal with the power of -13 dBm, the 21-GHz IF leakage with the power of -25 dBm and other harmonics and mixing products with the powers of 30 dB lower than that of 24.5-GHz RF signal. The output PBF needs to be optimized to further suppress the low-sideband component.

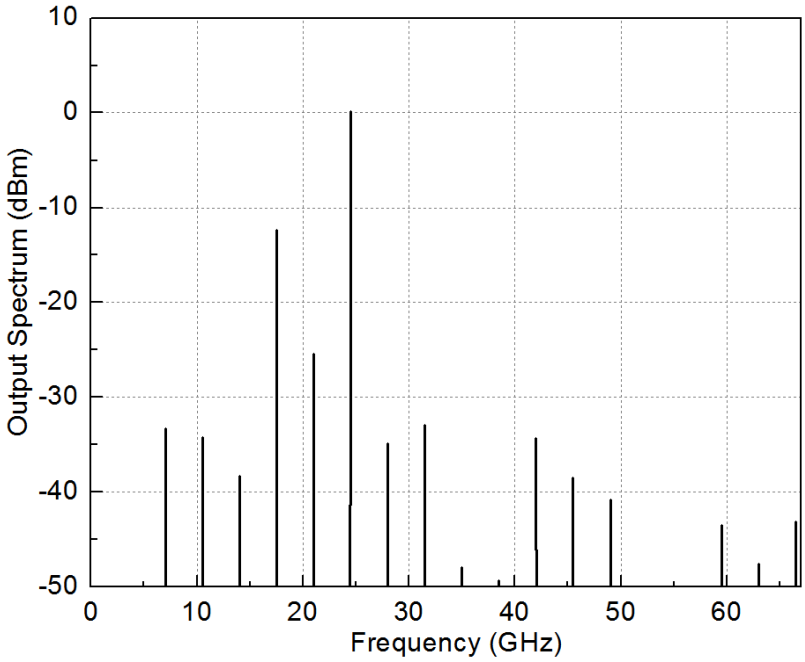


Fig. 2.21 Output spectrum of 24.5-GHz mixer with the IF input power of -20 dBm.

The measurement shows that by changing the bias voltage V_{b2} of the Gilbert cell, as shown in Fig. 2.11, from 0.8 V to 1.5 V, the conversion gain of the mixer changes from -10 dB to +25.7 dB. All performances of 24.5-GHz mixer are summarized in Table

2.5. The measured results show that the designed mixer performances meet the required specifications except the sideband suppression. The output PBF needs to be re-optimized to further reject the sideband signal.

Table 2.5 24.5-GHz mixer specification summary

	Design specification	Simulated results	Measured results
IF frequency (GHz)	21	21	21
LO frequency (GHz)	3.5	3.5	3.5
RF frequency (GHz)	24.5	24.5	24.5
Power conversion gain (dB)	20	25.3	25.7
Side-band suppression (dB)	30	56	13
Noise figure (dB)	9	8.7	NA
$P_{out,1dB}$ (dBm)	> 0	1.28	1.36
$P_{out,max}$ (dBm)	> 2	5	2.7
LO power (dBm)	< 0	-4	-2
LO-RF Isolation (dB)	30	60	30
IF-RF Isolation (dB)	-	17	0

2.5 35-GHz Mixer Design

The 35-GHz mixer is designed to generate the 35-GHz signal from 21-GHz IF and 14-GHz LO signals. Like the 24.5-GHz mixer, it consists of an input matching network, single-ended to differential balun, double-balanced Gilbert mixer cell, differential amplifier and band pass filter. The designs of constitute circuits of 35-GHz mixer are the same as those of 24.5-GHz mixer except that the circuit performances are

optimized at 35 GHz instead of 24.5 GHz. The loading inductors L_{c1}, L_{c2}, L_{c3} and L_{c4}, having values of 140 pH, are optimized to tune the output capacitors of the Gilbert mixer cell and the differential amplifier at 35 GHz. The BPF at the output of the mixer passes the 35-GHz signal, suppresses the LO and low sideband at 7 GHz. In the whole system, the 35-GHz mixer should be preceded with a band-stop filter at its input to reject the image signal at 49 GHz. The whole mixer is optimized to have high gain and linearity. Table 2.6 shows the design parameters of 35-GHz mixer.

Table 2.6. 35-GHz mixer design parameters

IF frequency (GHz)	21	Noise figure (dB)	9
LO frequency (GHz)	14	$P_{out,1dB}$ (dBm)	-5
RF frequency (GHz)	35	LO power (dBm)	0
Power conversion gain (dB)	20	LO-RF Isolation (dB)	30
Side-band suppression (dB)	30	IF-RF Isolation (dB)	-

Fig. 2.22 shows the complete schematic of 35-GHz mixer with values of the components. The layout and microphotograph of the mixer are shown in Fig. 2.23 (a) and (b), respectively. The 35-GHz mixer has the chip area of 1.3x0.9 μm^2.

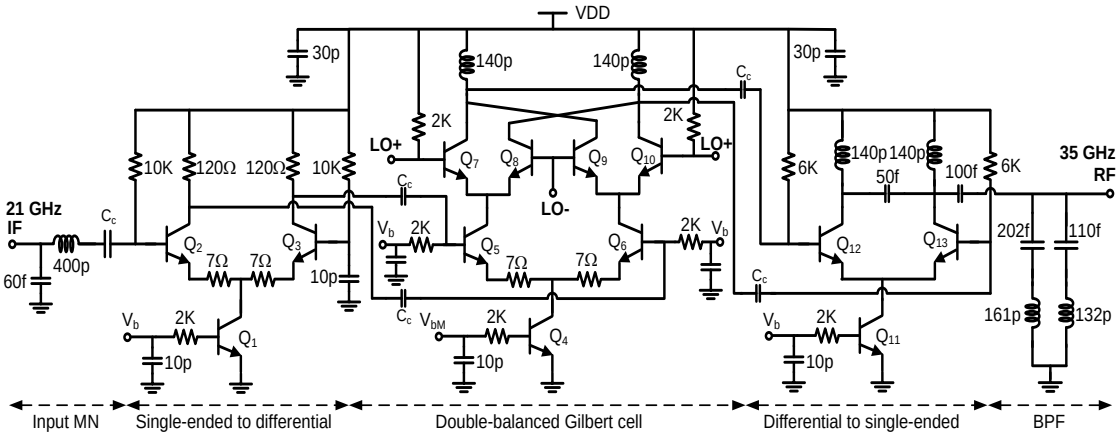
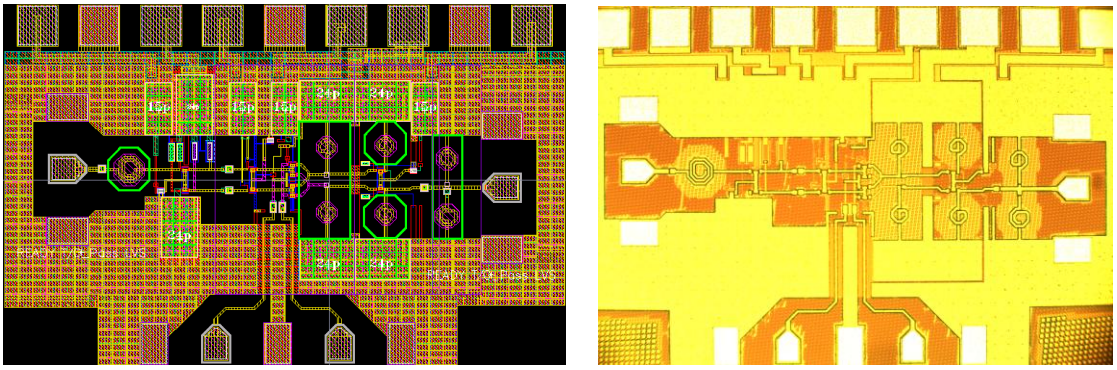


Fig. 2.22. 35-GHz mixer schematic.



(a) (b)

Fig. 2.23. 35-GHz mixer layout (a) and microphotograph (b).

2.5.1 35-GHz Mixer Performance

The designed mixer was measured on-wafer using Rhode & Schwarz vector network analyzer and Cascade probe station. The short-open-load-thru calibration method along with Microtech's impedance standard substrate standards was used. The 35-GHz mixer consumes a current of 40 mA from a power supply of 1.8 V.

Input, Output Return Losses and Stability

Stability is an important issue and should be the first check in the mixer design. Stability is confirmed using S-parameter (SP) simulation and measurement in which the mixer's LO port is terminated with 50-Ω. In this case, the mixer is considered as a two-port amplifier. The IF and RF ports are the input and output ports respectively. The S-parameter simulation and measurement is setup with small input power of -40 dBm. Simulated and measured results show that the mixer is unconditional stable from DC to 80 GHz with the mixer's stability K and B_1 factors larger than 1 and 0, respectively.

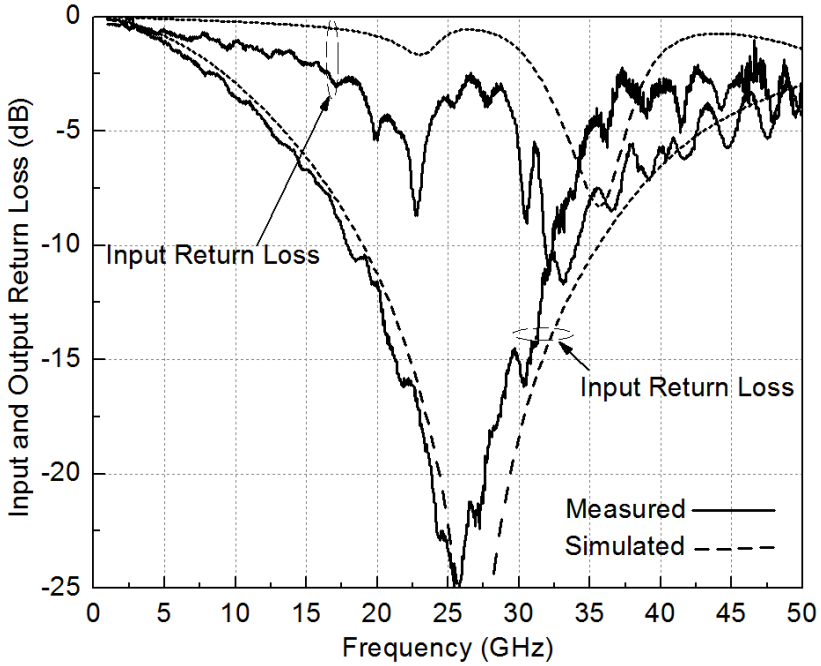


Fig. 2.24. 35-GHz mixer input and output return losses.

Fig. 2.24 shows the simulated and measured input and output return losses. The measured input return loss is 15 dB at the IF frequency of 21 GHz and the measured

ouput return loss is 5 dB at the RF frequency of 35 GHz.

Conversion gain versus the LO power and RF frequency

The simulation and measurement for the conversion gain versus the LO power is performed to determine the optimum LO power which maximizes the conversion gain of the mixer. The frequency and power of IF signal are set to 21 GHz and -40 dBm, respectively. The LO frequency is fixed at 14 GHz. The LO power is swept from -20 to 5 dBm with the step of +1 dBm. The conversion gain is measured as the ratio of the 35-GHz RF output power and 21-GHz IF input power. The simulated and measured conversion gains versus LO power are shown in Fig. 2.25. The simulated result shows that the maximum conversion gain of 23.4 dB is achieved with the LO power of 0 dBm while the measured result shows that the maximum conversion gain of 22.5 dB is obtained with the LO power of 0.6 dBm. This measured optimum LO power of 0.6 dBm is used for subsequent measurements. The low measured LO power is achieved due to the selection of small sizes of transistors in the LO switching stage.

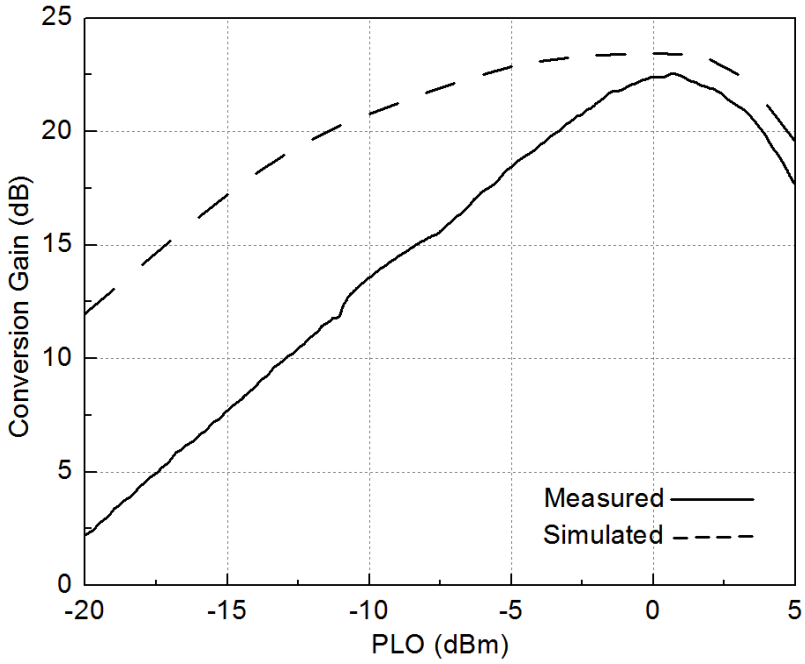


Fig. 2.25. Measured and simulated conversion gains of 35-GHz mixer versus LO power.

The simulation and measurement for the conversion gain versus the RF frequency are carried out to characterize the frequency response of the mixer. The LO frequency and power are fixed at 3.5 GHz and 0.6 dBm, respectively. The IF power is set to -40 dBm and the IF frequency is swept from 14 to 30 GHz; therefore the resultant RF frequency is from 28 to 44 GHz. The conversion gain is measured as the power ratio of the RF output and IF input signals. Fig. 2.26 shows the conversion gain versus the RF frequency. The measured results show that the mixer exhibits the conversion gain of 22 dB at the RF frequency of 35 GHz, and the maximum conversion gain of 27 dB is located at 32.5 GHz.

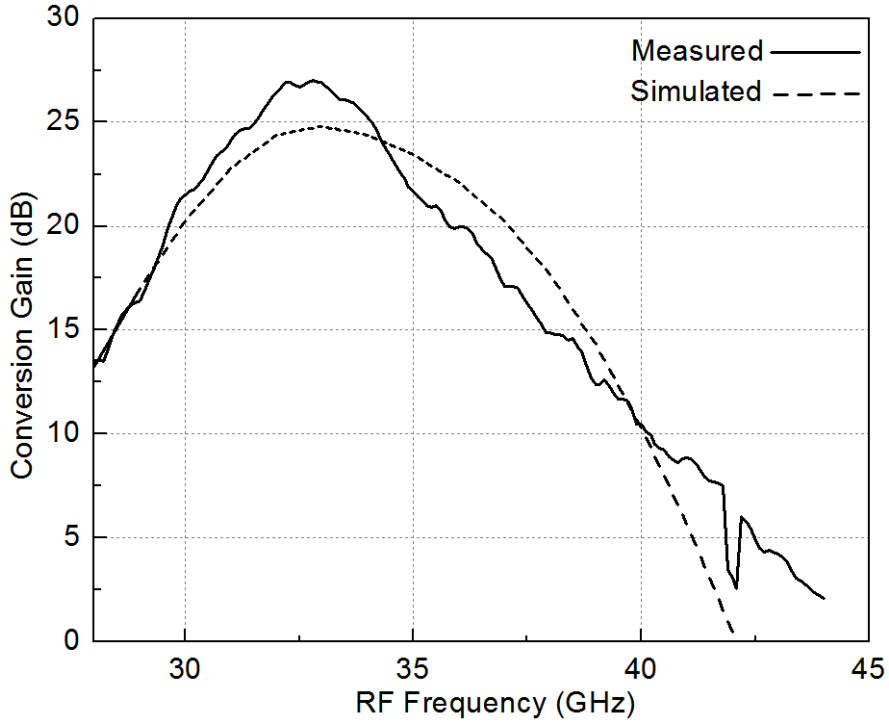


Fig. 2.26. Measured and simulated conversion gains of 35-GHz mixer versus RF frequency.

Noise Figure

The noise figure simulation for the complete mixer is performed using harmonic balance. The LO frequency and power are fixed at 14 GHz and 0.6 dBm, respectively. The IF power is set to -40 dBm and the IF frequency is swept from 15 to 30 GHz. Fig. 2.27 shows the simulated noise figure of the mixer versus the IF input frequency. At 21 GHz, the noise figure is 8 dB which is a reasonable value for the up-conversion mixer and meets the design requirement.

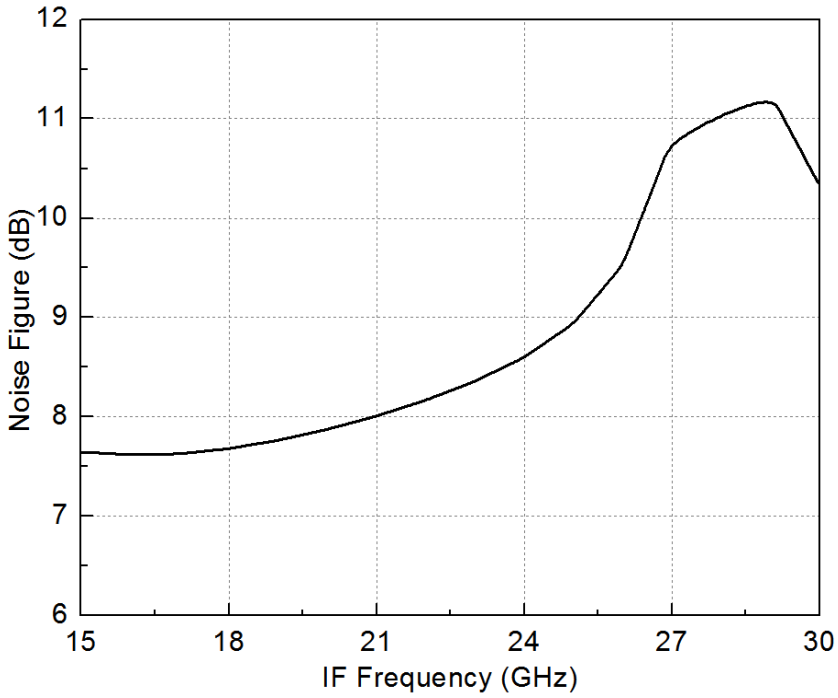


Fig. 2.27. Simulated noise figure of 35-GHz mixer versus IF frequency.

Mixer performance versus the IF input power

Fig. 2.28 shows the simulated and measured results of the gain and output power versus the IF input power. In the simulation and measurement, the LO frequency and power are fixed at 14 GHz and 0.6 dBm, respectively, the IF frequency is set to 21 GHz and the IF power is swept from -40 to -10 dBm. The measured results show that 35-GHz mixer exhibits the maximum gain of 22.4 dB, 1-dB input power, $P_{in,1dB}$, of -23 dBm, 1-dB output power, $P_{out,1dB}$, of -2.4 dBm, and maximum output power of 1 dBm.

Fig. 2.29 shows the isolations and low-sideband suppression versus the IF input power. The measured results shows that the LO-IF and LO-RF isolations are higher than 35 dB with the input power smaller than the 1-dB compression point of -23 dBm. The

IF-RF isolation is higher than 12 dB. The low-sideband suppression is defined as the power ratio of the low-sideband at 7 GHz and the high sideband at 35 GHz. The measured low-sideband suppression is higher than 35 dB over the full range of IF input power.

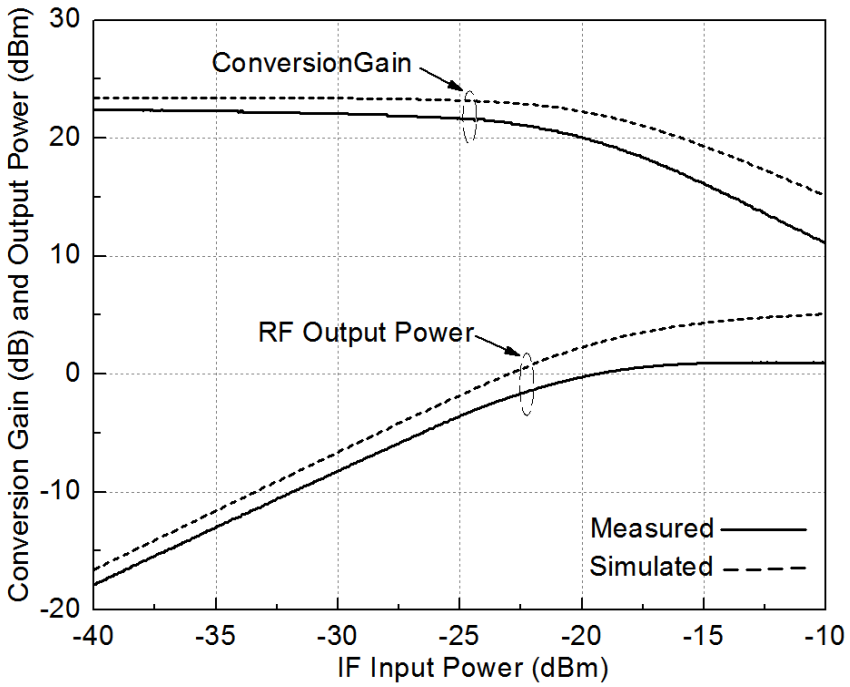


Fig. 2.28. Gain and RF output power of 35-GHz mixer versus IF input power.

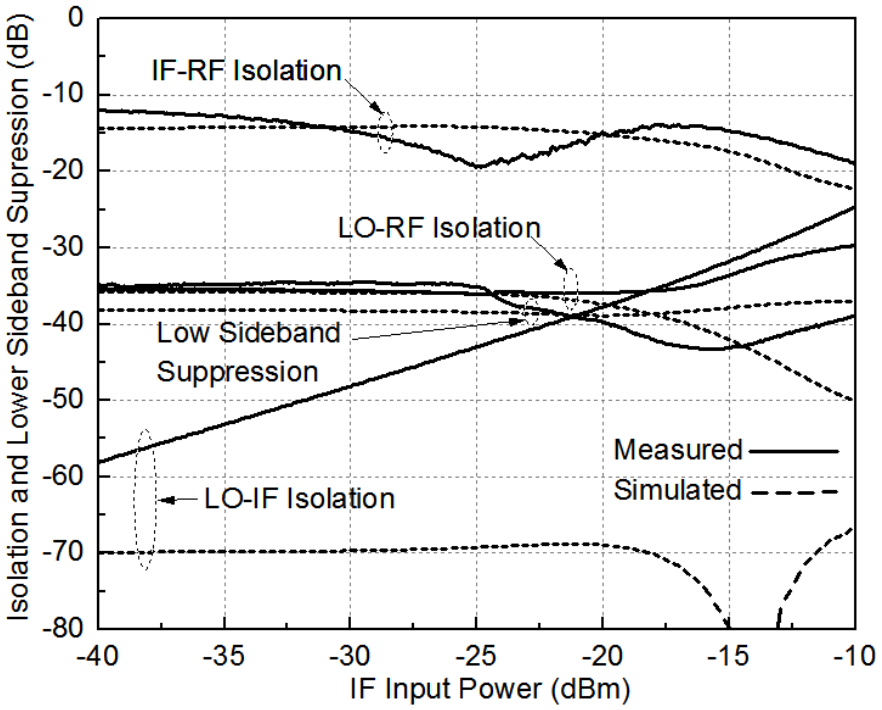


Fig. 2.29 Isolation and lower sideband suppression of 35-GHz mixer versus IF input power.

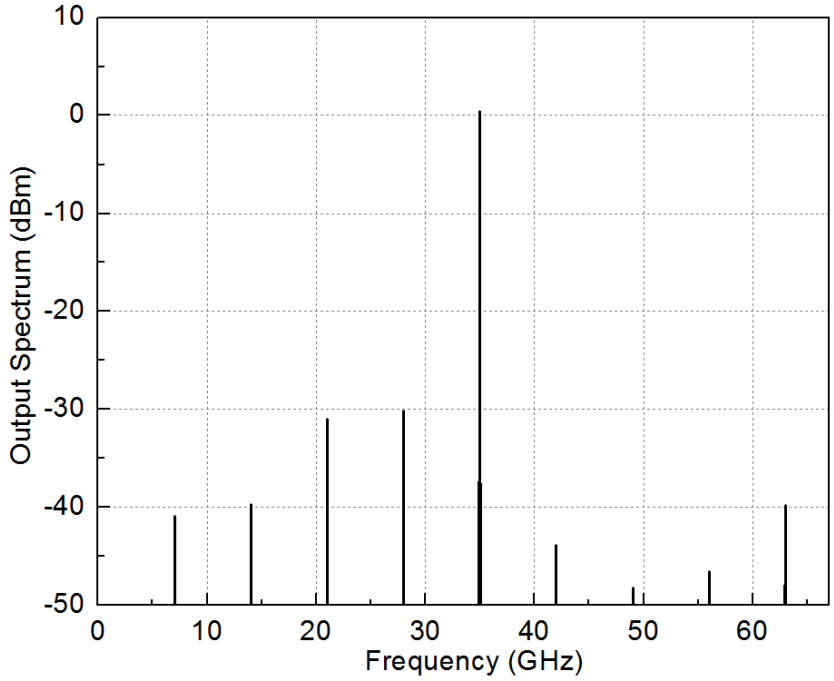


Fig. 2.30. Output spectrum of 35-mixer with the IF input power of -20 dBm.

Fig. 2.30 shows the measured output spectrum of the 35-GHz mixer with the 21-GHz IF input power of -20 dBm, LO frequency of 14 GHz and LO power of 0.6 dBm. It can be seen that the output spectrum contains a 35-GHz signal with the power of 0 dBm and other harmonics and mixing products with the powers of 30 dB lower than that of 35-GHz RF signal.

The measurement shows that by changing the bias voltage V_{b2} of the Gilbert cell, as shown in Fig. 2.11, from 0.75 V to 1.55 V, the conversion gain of the mixer changes from -13 dB to +22.4 dB. All performances of the 35-GHz mixer are summarized in Table 2.7. The measured results show that the designed 35-GHz mixer performances meet the required specifications.

Table 2.7 35-GHz mixer specification summary

	Design specification	Simulated results	Measured results
IF frequency (GHz)	21	21	21
LO frequency (GHz)	14	14	14
RF frequency (GHz)	35	35	35
Power conversion gain (dB)	20	23.5	22.4
Side-band suppression (dB)	30	38	35
Noise figure (dB)	9	8	NA
$P_{out,1dB}$ (dBm)	> -3	2	-2.4
$P_{out,max}$ (dBm)	> 2	5	1
LO power (dBm)	< 0	0	0.6
LO-RF Isolation (dB)	>30	35	35
IF-RF Isolation (dB)	-	15	12

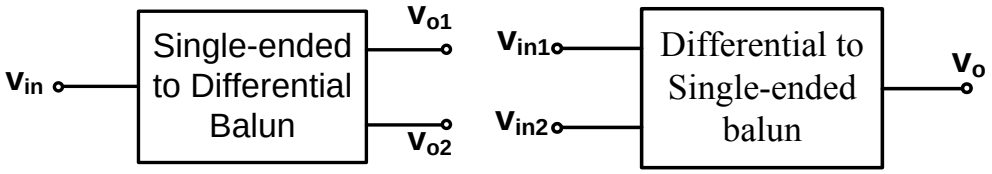
CHAPTER III

ULTRA-WIDEBAND ACTIVE BALUN*

In this chapter, novel circuit architectures for ultra-wideband active baluns are proposed and implemented. The techniques for parasitic neutralization and compensation used to keep the active baluns well-balanced over a wide frequency range from DC up to millimeter-wave frequencies are analyzed in detail.

3.1 Introduction

Baluns are important RF components used for converting single-ended to differential signals or differential to single-ended signals, and find many applications in RF wireless transceivers. Particularly, on-chip baluns are inevitable in differential RFICs, such as balanced mixers, that provide numerous advantages as compared to their single-ended counterparts for even-order distortion suppression, inter-component interference cancellation and port-to-port isolations. In measurements, on-chip baluns



(a) (b)

Fig. 3.1. Single-ended to differential (a) and differential to single-ended (b) balun models.

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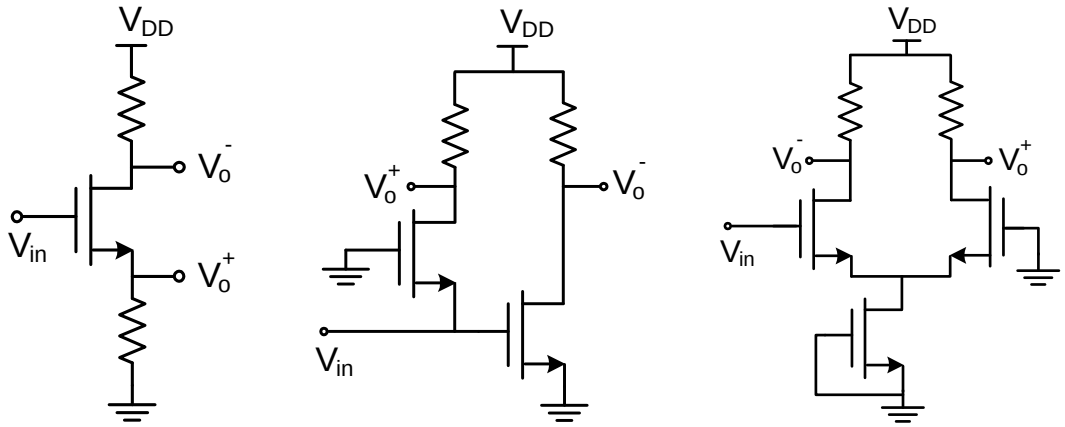
help simplify the measurement setup for on-wafer characterization of differential circuits as they enable external single-ended signals to be conveniently used.

Figure 3.1 shows two types of baluns, single-ended to differential and differential to single-ended baluns. The baluns are characterized by their balances. The single-ended to differential balun is balanced if two differential output voltages are equal in amplitude and 180-degree out of phase. The differential to single-ended balun is balanced if the output signal is zero when the two input signals have the same amplitude and 180-degree out of phase.

Baluns can be implemented using passive or active devices. Several passive and active baluns have been developed for MICs, GaAs MMICs, and Si RFICs [25]-[36]. The most crucial requirements for baluns are well-balanced amplitude and phase which are challenging for the design of baluns operating over wide bandwidths, particularly those extending to the millimeter-wave frequencies.



(a) (b) (c)

Fig. 3.2. Typical active balun circuits.

The Marchand balun in [25] was designed on a multilayered structure and exhibits amplitude and phase imbalances of less than 0.5 dB and 5^{o}, respectively, over a wide bandwidth from 4 to 20 GHz. In [26], a passive balun based on the Wilkinson power divider employs both lumped and distributed elements and achieves good amplitude and phase imbalances within 0.27 dB and 2° from 70 to 84 GHz, respectively. The broadband monolithic passive balun using planar-spiral transformer structure presented in [27] exhibits the amplitude and phase unbalance less than 0.5 dB and 5^{o}, respectively, over 16-30 GHz frequency band.

For RFICs, active balun are typically preferred than passive baluns due to their miniaturization and possible gain. Fig. 3.2 (a), (b) and (c) show typical active balun circuits which respectively generate differential signals by slitting an input signal using a single transistor [28], combining common gate (CG) and common source (CS) amplifiers [29], and using a differential amplifier with one input [30]. Those active baluns work well at low frequencies or in a narrow band, but their amplitude and phase balances become poor at high frequencies due to the inherent parasitic elements. Various techniques have been used to improve the amplitude and phase balances of the active baluns [31]-[36]. In [31] and [32], techniques for correcting the phase are implemented using differential amplifiers, resulting in well balance from 2 to 40 and 50 to 67 GHz, respectively. Good amplitude and phase balances from 0.2 to 22 GHz are obtained by increasing the common-mode rejection ratio [33]. The active balun in [34] employs the Darlington cells with base peaking inductors and feedback capacitor, and achieves good amplitude and phase balances across DC to 21 GHz. The active balun in [35]

implements the distributed technique and demonstrates an amplitude imbalance smaller than 2 dB and phase imbalance lower than 20 degrees from 4 to 40 GHz. The active balun in [36] employing a combined cascode–cascade configuration exhibits good balance of less than 1.8 dB in amplitude and 10 degrees in phase from DC up to 17 GHz.

The differential to single-ended active balun is used in integrated circuits to convert the differential signal to single-ended signal and suppress the common-mode signals as well. So, in addition to a high differential-mode gain, a very low common-mode gain is desirable. Several types of this active balun have been used, such as the differential amplifier type balun [37], multi-tanh doublet type balun and the push-pull type balun [38]. Two first active baluns, however, have poor balance when the frequency goes up as the output impedance of the non-ideal current source is not as high as required. The push-pull type balun consisting of two transistors and two resistors provides higher linearity than others but due to parasitic components of the active devices, it just keeps the balance at low frequency and does not at high frequency; hence, increasing the common-mode gain and reducing the common-mode signal suppression.

This chapter first presents a new type of active balun for single-ended to differential conversion capable of producing well amplitude and phase balances over extremely wide bandwidths extending from DC to millimeter-wave frequencies. It combines common-emitter (CE) with a degenerative inductor and common-collector (CC) amplifiers, and implements techniques for parasitic neutralization and compensation using external base and emitter inductors. The designed active balun on a 0.18-μm SiGe BiCMOS process exhibits an amplitude imbalance smaller than 1 dB and

phase imbalance better than 10^0 from DC to 50 GHz. It has a chip size of 0.55x0.58 mm^2 and consumes a current of 8 mA from a DC voltage of 1.8 V. In addition, a new differential to single-ended active balun exhibiting very good balance over an ultra-wide bandwidth at millimeter-wave frequencies and extremely high common-mode signal suppression in addition to high differential-mode gain is analyzed and simulated using a 0.18-μm BiCMOS process.

3.2 Single-ended to Differential Active Balun Design

3.2.1 Circuit and Analysis

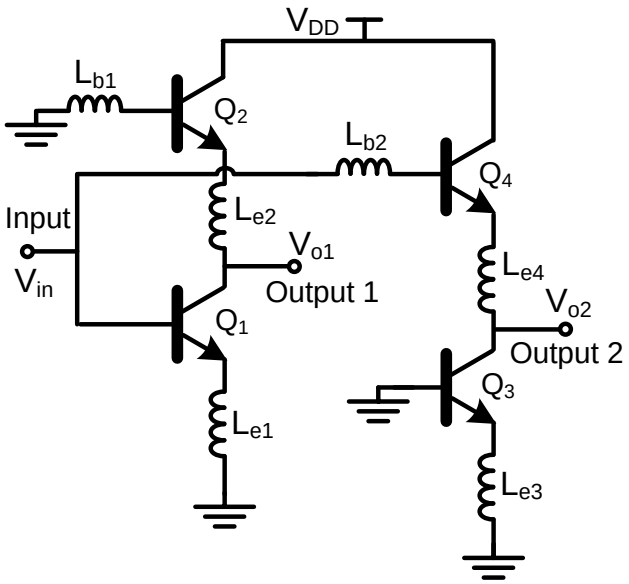


Fig. 3.3. Simplified schematic of proposed single-ended to differential active balun. Input matching and bias circuits are not shown.

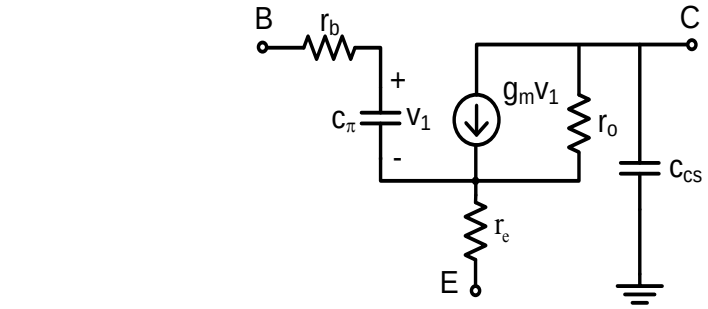
Figure 3.3 shows a simplified schematic of the proposed active balun that converts a single-ended signal (V_{in}) to two differential signals (V_{o1} and V_{o2}). It consists of a common-emitter amplifier with a degenerative inductor (Q_1, Q_2, L_{e1}, L_{e2} and L_{b1})

and a common-collector amplifier (Q_3, Q_4, L_{e3}, L_{e4} and L_{b2}). Q_2, L_{e2} and L_{b1} function as the load of the common-emitter amplifier, and Q_3 and L_{e3} work as the current source for the common-collector amplifier. The four HBT transistors are identical. Same emitter inductors ($L_{e1} = L_{e2} = L_{e3} = L_{e4}$) and base inductors ($L_{b1} = L_{b2}$) are used. The magnitude and phase balance of V_{o1} and V_{o2} are controlled by inductors L_e's and L_b's. These inductors particularly neutralize and compensate for the parasitic components of the transistors that have significant effects to the balun's performance at high frequencies, hence enabling well amplitude and phase balances for the balun up to a very high frequency and across a frequency range broader than those of the other reported baluns. In addition, L_{e1}, functioning as a degenerative inductor, helps improve the linearity of the balun.

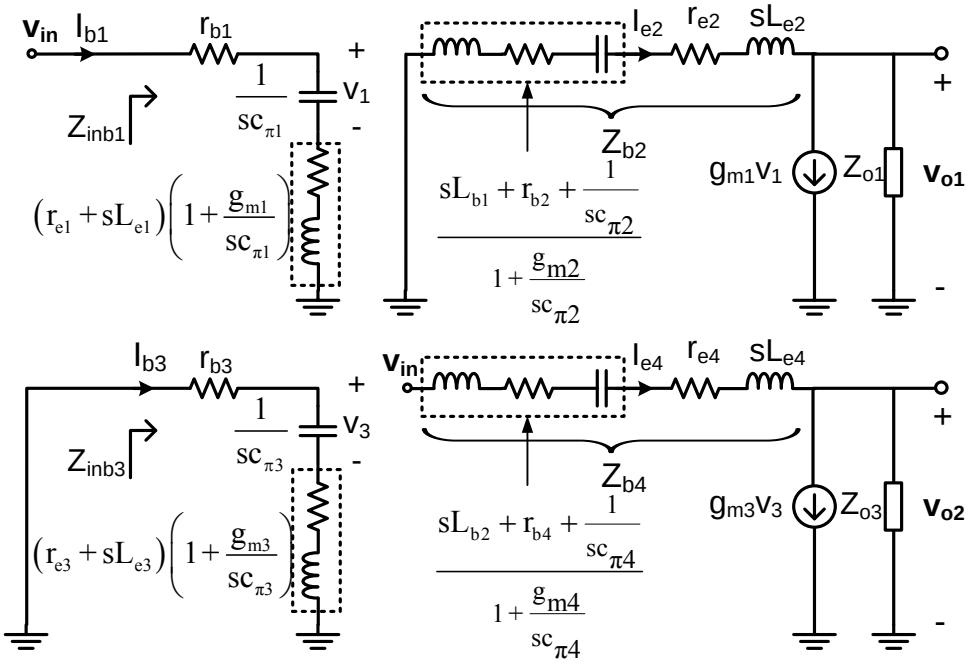
Figure 3.4(a) shows a simplified small-signal model of the HBT used in the active balun analysis and Fig. 3.4(b) shows the small-signal equivalent circuit of the active balun derived from Fig. 3.3 and Fig. 3.4(a) after several manipulations. The four transistors are biased at the same conditions and hence their small-signal parameters are equal. The transistor's output resistance r_o is normally large, around several KΩ, and is thus omitted for transistor Q_2 and Q_4. Z_{o1} and Z_{o3} are the output impedance looking into transistor Q_1 and Q_3 from its collector and can be derived as

$$Z_{oi} = \frac{1}{sc_{cs}} \left\| \left\{ r_o + \left[\left(r_b + \frac{1}{sc_\pi} \right) \| (r_e + sL_e) \right] \left(1 + \frac{r_o g_m}{1 + sc_\pi r_b} \right) \right\} \right. \quad (i=1,3) \tag{3.1}$$

where ‖ denotes parallel operation and $s = j\omega$.



(a)



(b)

Fig. 3.4. (a) Small-signal HBT model with base resistance r_b, emitter resistance r_e, output resistance r_o, base-collector capacitance c_π, transconductance g_m and collector-substrate capacitance c_{cs}. (b) Equivalent circuit of the active balun. Corresponding small-signal parameters of the transistors are equal. $Z_{inb1} = Z_{inb3}$, $Z_{b2} = Z_{b4}$. $L_{e1} = L_{e2} = L_{e3} = L_{e4} = L_e$, $L_{b1} = L_{b2} = L_b$.

The voltage gains between the input port and two differential ports are derived from Fig. 3.4(b) as

$$A_{v1} = \frac{v_{o1}}{v_{in}} = -\frac{g_{m1}}{Z_{inb1} sc_{\pi 1}} Z_{b2} \| Z_{o1} \tag{3.2}$$

$$A_{v2} = \frac{v_{o2}}{v_{in}} = \frac{1}{Z_{b4}} Z_{b4} \| Z_{o3} \tag{3.3}$$

where Z_{inb1}, Z_{b2}, and Z_{b4} are defined as in Fig. 3.4(b) and derived as

$$Z_{inb1} = r_{b1} + r_{e1} + \frac{L_{e1} g_{m1}}{c_{\pi 1}} + sL_{e1} + \frac{1 + r_{e1} g_{m1}}{sc_{\pi 1}} \tag{3.4}$$

$$Z_{b2} = \frac{sL_{b1} + r_{b2} + r_{e2} + \frac{L_{e2} g_{m2}}{c_{\pi 2}} + sL_{e2} + \frac{1 + r_{e2} g_{m2}}{sc_{\pi 2}}}{1 + \frac{g_{m2}}{sc_{\pi 2}}} \tag{3.5}$$

$$Z_{b4} = \frac{sL_{b2} + r_{b4} + r_{e4} + \frac{L_{e4} g_{m4}}{c_{\pi 4}} + sL_{e4} + \frac{1 + r_{e4} g_{m4}}{sc_{\pi 4}}}{1 + \frac{g_{m4}}{sc_{\pi 4}}} \tag{3.6}$$

In Fig. 3.4(b), $V_3 = 0$, due to the grounded base of Q_3, therefore the current source $g_{m3}V_3 = 0$. The balance of the balun is characterized by the ratio between the two voltage gains in (2) and (3), which is also the balance between the two output voltages V_{o1} and V_{o2}. This balance can be derived, making use $Z_{b2} = Z_{b4}$ and $Z_{o1} = Z_{o3}$, as

$$\frac{A_{v1}}{A_{v2}} = \frac{v_{o1}}{v_{o2}} = -\frac{Z_{b4}}{Z_{inb1}} \frac{g_{m1}}{sc_{\pi 1}} = -K \tag{3.7}$$

where

$$K = \frac{Z_{b4}}{Z_{inb1}} \frac{g_{m1}}{sc_{\pi 1}} = \frac{\frac{g_{m1}}{c_{\pi 1}}}{s + \frac{g_{m4}}{c_{\pi 4}}} \frac{s + \frac{r_{b4} + r_{e4} + \frac{L_{e4} g_{m4}}{c_{\pi 4}}}{L_{b2}} + \frac{sL_{e4} + \frac{1 + r_{e4} g_{m}}{sc_{\pi 4}}}{L_{b2}}}{\frac{r_{b1} + r_{e1} + \frac{L_{e1} g_{m1}}{c_{\pi 1}}}{L_{b2}} + \frac{sL_{e1} + \frac{1 + r_{e1} g_{m1}}{sc_{\pi 1}}}{L_{b2}}} \tag{3.8}$$

which is referred to as the balance factor of the active balun. The balun is perfectly

balanced when the two output signals V_{o1} and V_{o2} are equal in amplitude and 180-degree out of phase, which, from (3.8), leads to

$$K = 1 \tag{3.9}$$

Equations (3.8) and (3.99) show that the condition required to make the balun balanced is independent of the external loads of the balun and the transistor's output impedances Z_{o1} and Z_{o3}. Using the balance condition in (3.9) and making use of (3.8), we get

$$sL_{e1} + \frac{1 + r_{e1}g_{m1}}{sc_{\pi 1}} = sL_{e4} + \frac{1 + r_{e4}g_{m}}{sc_{\pi 4}} = 0 \tag{3.10}$$

and

$$\frac{g_{m1}}{c_{\pi 1}} = \frac{r_{b1} + r_{e1} + \dfrac{L_{e1}g_{m1}}{c_{\pi 1}}}{L_{b2}} = \frac{g_{m4}}{c_{\pi 4}} = \frac{r_{b4} + r_{e4} + \dfrac{L_{e4}g_{m4}}{c_{\pi 4}}}{L_{b2}} \tag{3.11}$$

from which, L_{e1}, L_{e2}, L_{e3}, L_{e4}, L_{b1} and L_{b2} are obtained at the design frequency, ω_o, as

$$L_{e1} = L_{e2} = L_{e3} = L_{e4} = \frac{1 + r_e g_m}{\omega_0^2 c_\pi} \tag{3.12}$$

and

$$L_{b1} = L_{b2} = L_e + \frac{c_\pi (r_b + r_e)}{g_m} = \frac{1 + r_e g_m}{\omega_0^2 c_\pi} + \frac{c_\pi (r_b + r_e)}{g_m} \tag{3.13}$$

Applying equations (3.10) and (3.11) to (3.8) clearly shows that the introduction of the emitter inductors L_e's and base inductors L_b's into the active balun produces means to neutralize and compensate for the effects of the transistor's parasitic components at high frequencies. Equations (3.10) and (3.12) show that the emitter inductors L_e's neutralize the parasitic capacitances while equations (3.11) and (3.13) demonstrate that the base inductors L_b's compensate for the effects of transistor's parasitic components.

As a result, the two common-emitter (Q_1 and Q_2) and collector (Q_2 and Q_4) amplifiers with neutralized and compensated parasitic elements can produce two output signals having the same amplitude and 180-deg out of phase from a single input signal.

Equations (3.12) and (3.13) represent the required inductances for the balun in terms of the transistor's parameters that make it perfectly balanced at the design frequency. Making use (3.12) and (3.13), K in (3.8) becomes

$$K = \frac{\omega_T}{s+\omega_T} \frac{s+\omega_T + \dfrac{(s^2+\omega_0^2)}{s\omega_0^2} \dfrac{(1+r_e g_m)}{\left(\dfrac{1+r_e g_m}{\omega_0^2 c_\pi} + \dfrac{c_\pi (r_b + r_e)}{g_m}\right) c_\pi}}{\omega_T + \dfrac{(s^2+\omega_0^2)}{s\omega_0^2} \dfrac{(1+r_e g_m)}{\left(\dfrac{1+r_e g_m}{\omega_0^2 c_\pi} + \dfrac{c_\pi (r_b + r_e)}{g_m}\right) c_\pi}} \tag{3.14}$$

where $\omega_T = \dfrac{g_m}{c_\pi}$. Equation (3.14) shows that the balance factor K of the balun is fully dependent on the transistor parameters and always equal to 1 at design frequency $\omega = \omega_0$.

Figure 3.5, plotted from (3.14), shows the magnitude and phase of K versus frequency for the active balun employing identical transistors Q_1, Q_2, Q_3 and Q_4 under the same bias conditions, whose parameters are r_b = 34 Ω, r_e = 1.6 Ω, g_m = 276 mA/V, c_π = 177 fF. The design frequency at which K=1 is 35 GHz. However, as can be seen, the magnitude and phase of K vary only slightly over extremely wide frequency ranges. For instance, across DC to 100 GHz, the magnitude of K only changes from 0.98 to 1.09 while its phase just varies from 0.02 to -3.7 degrees. This shows that the active balun is not only perfectly balanced at the design frequency, but also maintains very good balance from DC to frequencies far beyond the design frequency. It is interesting to note

that the magnitude and phase of K in (3.14) exhibit little changes when the transistor sizes or bias conditions, hence the transistor's small-signal parameters, are varied. It is also observed that the smaller the sizes of the transistors, hence the smaller the parasitic components, the wider the bandwidth of the active balun that can be kept well-balanced. These unique characteristics of the proposed active balun make it attractive for a variety of applications over a wide range of frequencies and operating conditions.

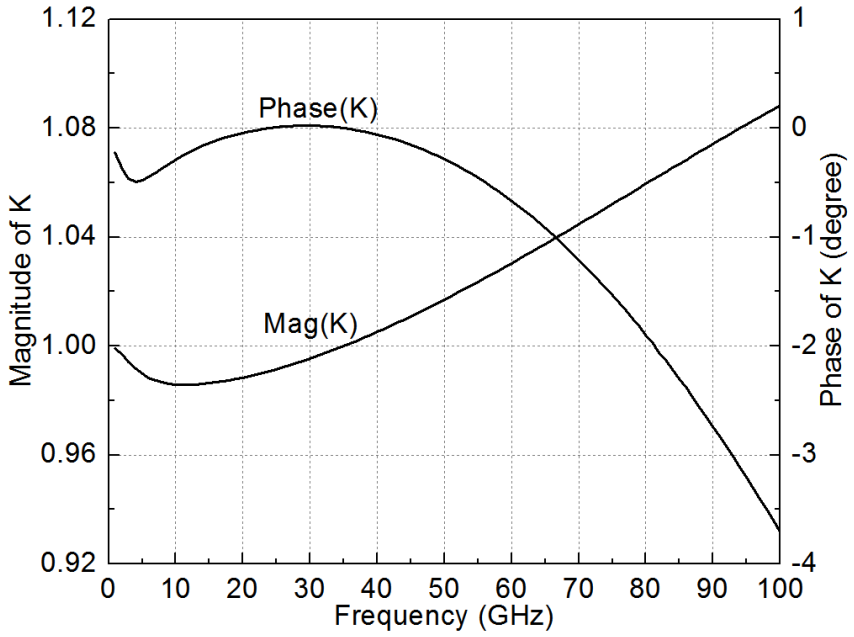


Fig. 3.5. Magnitude and phase of the balance factor K.

When the active balun is designed using (3.12) and (3.13), it always maintains the balance regardless of the loads or the output impedances of the circuits preceding and following the active balun, which is in contrast with other typical circuits whose performance is affected by external circuits. This property is desirable for the design of integrated circuits since any additional circuits added to the balun at its single-ended

input and/or differential outputs do not affect the balance of the balun, making the balun especially attractive for system integration. For instance, cascading a single-ended low noise amplifier (LNA) with the proposed active balun can form a differential LNA with good amplitude and phase balances, or integrating a LNA and mixer with the balun at its input and output ports, respectively, can form a good receiver front-end, without the need of optimization for the entire integrated differential LNA or receiver front-end.

A straightforward procedure to design the proposed active balun can be implemented using the foregoing analysis. First, a design frequency within the interested operating frequency range is chosen. Second, four transistors are selected and biased at the same conditions from which their small-signal parameters are extracted. It is noted that the size and bias current for these transistors should be small to achieve good balance across a wide bandwidth. Finally, the inductors L_e's and L_b's are calculated using (3.12) and (3.13).

3.2.2 Design and Fabrication

The proposed active balun was designed and fabricated using Jazz 0.18-μm SiGe BiCMOS process [21]. The topmost metal layer is used for the inductors, AC ground, and interconnects. All the on-chip inductors, interconnects, vias and AC ground were designed and simulated using the EM simulator IE3D [22]. The active balun was simulated, optimized and laid-out using Cadence [23].

The active balun was designed to have good amplitude and phase balance up to 50 GHz while consuming a low DC power. The design frequency, where K is equal to 1,

is 35 GHz. The four HBT Q_1, Q_2, Q_3 and Q_4 in the active balun have the same size with an emitter area of 0.15 x 10 μm^2 and are initially biased at a DC current of 8 mA. The bases of Q_1 and Q_3 are biased at 0.95 V and the bases of Q_2 and Q_4 are biased at 1.8 V through large resistors which do not affect the balun's RF operation. The collector of Q_2 and Q_4 are connected to V_{DD} of 1.8 V. The values of inductors L_e and L_b are first estimated using Eqs. (3.12) and (3.13) and then optimized in Cadence simulation at 35 GHz. Their final values are 168 pH and 120 pH, respectively.

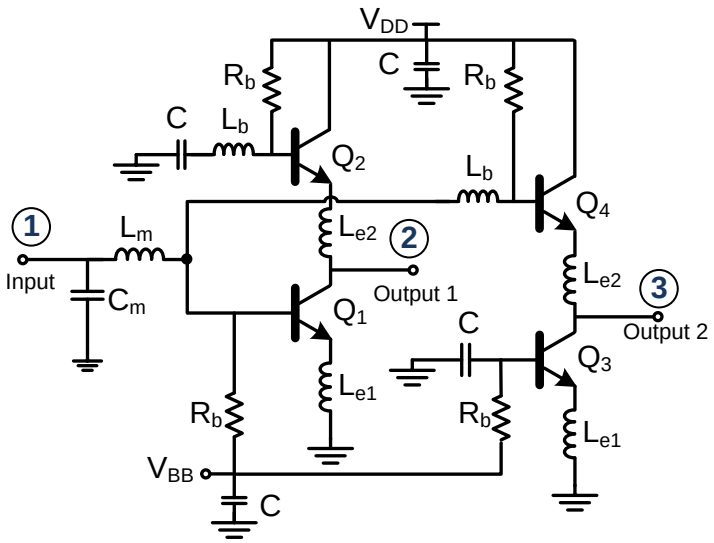


Fig. 3.6. Complete schematic of the designed active balun.

An L-type matching network consisting of a shunt capacitor of 70 fF and a series inductor of 200 pH is designed and used at the input of the balun. There is no output matching network in the designed balun. The complete active balun schematic is shown in Fig. 3.6 and the microphotograph of the active balun is shown in Fig. 3.7 with a chip

area (without pads) of 550 x 580 μm^2. The layout is made as symmetric as possible to enhance the balance of the active balun.

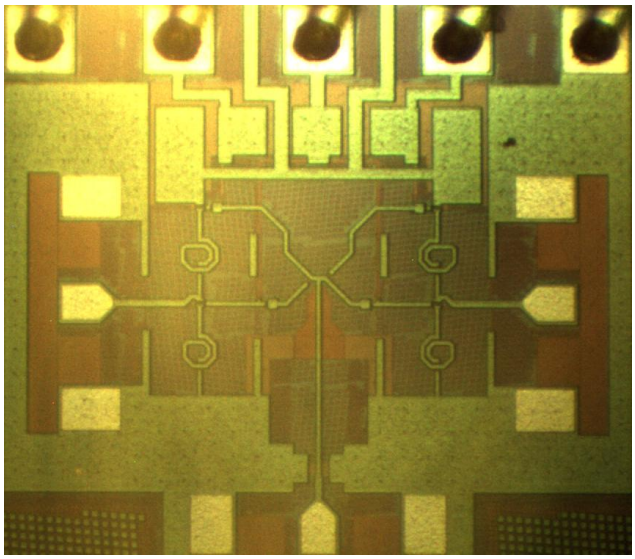


Fig. 3.7. Microphotograph of the designed active balun.

3.2.3 Active Balun Performance

The designed active balun was measured on-wafer using Rhode & Schwarz vector network analyzer and Cascade probe station. The short-open-load-thru calibration method along with Microtech's impedance standard substrate standards was used.

Figure 3.8 shows the simulated and measured insertion loss and phase between the input port and output ports (S_{21} and S_{31}), and amplitude and phase difference of the active balun under small-signal conditions at a bias current of 8 mA. The measured and simulated results are in reasonably good agreement from DC to 67 GHz. The measured results show that the balun exhibits good amplitude and phase balances over an ultra-

wide bandwidth. The amplitude balance between the two output ports is lower than 1 and 2.4 dB from DC to 60 GHz and DC to 67 GHz, respectively, while the phase balance is within 180 ± 10 degrees from DC to 50 GHz. At the design frequency of 35 GHz, the amplitude difference is only 0.03 dB while the phase difference is 180.07 degree, which shows extremely well balance. In the particular frequency range from 21 to 40.5 GHz, the amplitude and phase imbalance are lower 0.5 dB and 2^{o} (with respect to 180 deg.), respectively.

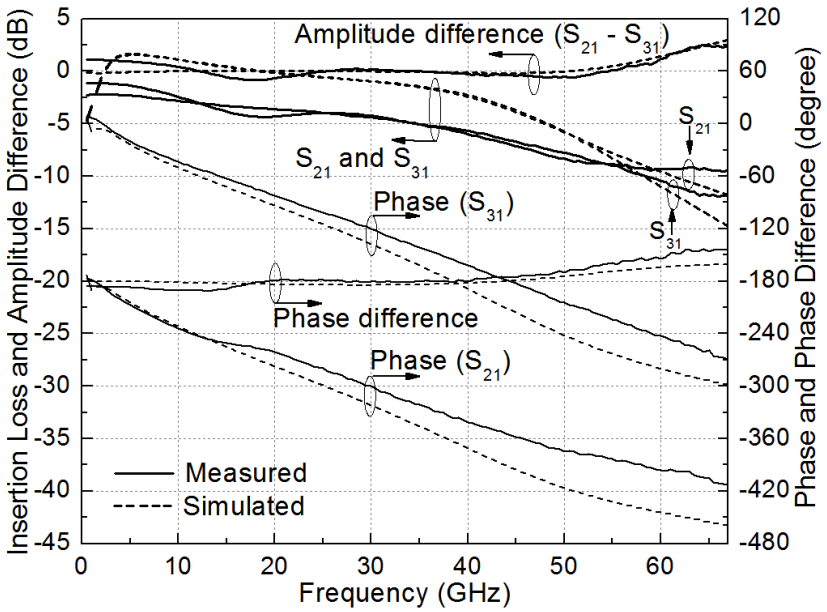


Fig. 3.8. Simulated and measured insertion loss, amplitude difference, phase and, phase difference of the active balun.

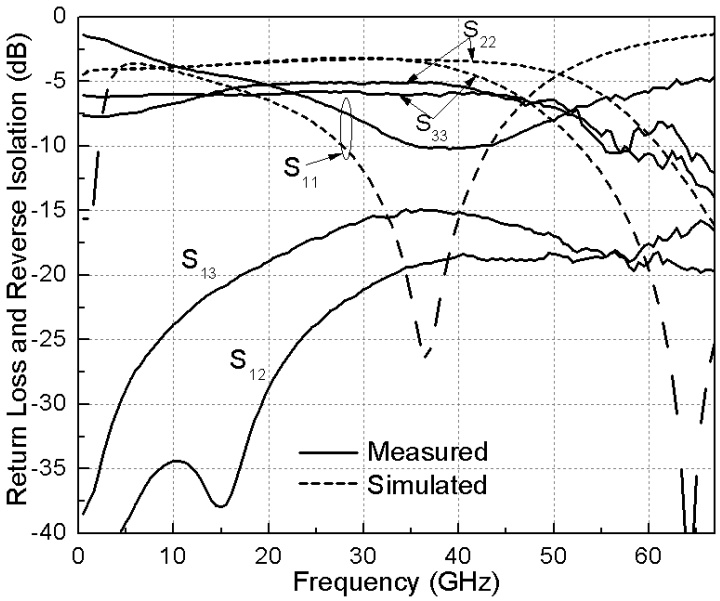


Fig. 3.9. Measured and simulated return losses and measured reverse isolations.

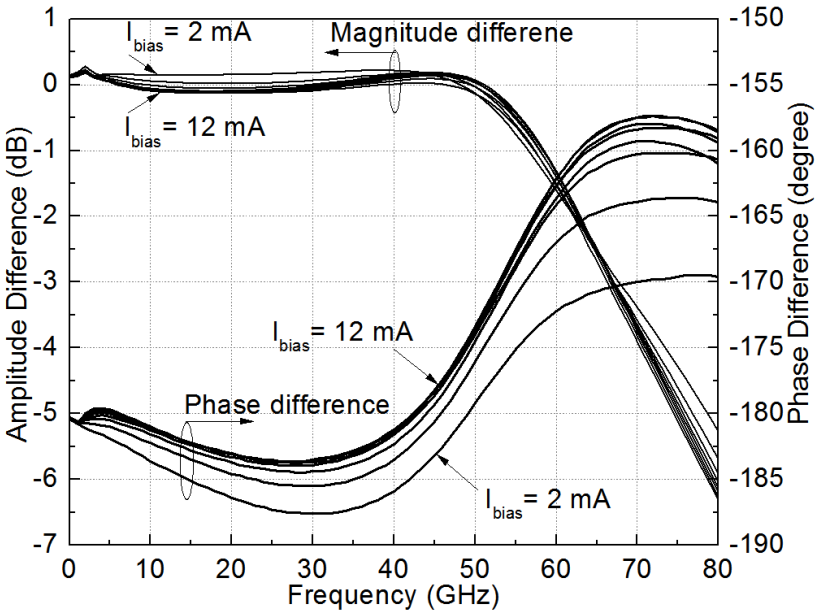


Fig. 3.10 Simulated amplitude and phase difference with different bias currents.

Fig. 3.9 shows the measured and simulated return losses and measured reverse isolations. The active balun exhibits a measured input return loss (S_{11}) of 10 dB and

output return losses (S_{22} and S_{33}) of around 5 dB at 35 GHz. It is noted, as mentioned earlier, that the balun does not have an output matching network. The two output return losses are almost identical from DC to 67 GHz. As seen from Fig. 3.3(b) the output impedances of the active balun are $Z_{b2} \| Z_{o1}$ and $Z_{b4} \| Z_{o3}$ at the output ports, respectively. These output impedances are equal (assuming that V_{in} has zero internal output impedance). The measured reverse isolations S_{12} and S_{13} are higher than 15 dB from DC to 67 GHz.

Table 3.1 Performance comparison

	[28]	[29]	[30]	[32]	This work
Frequency range (GHz)	60-67	2-40	0.5-22	4-40	DC-50
Amplitude imbalance (dB)	1.7	0.5	0.5	2	1
Phase imbalance (deg)	6.8	10	4	20	10
$P_{in,1dB}$ (dBm)	N/A	-5	-5	N/A	-0.4
P_{DC} (mW)	19	40	166	20	7.2
Topology	Diff. Amp.	Diff. Amp.	Diff. Amp.	Matrix	CE/CC
Process	90nm CMOS	0.13μm CMOS	0.25μm SiGe	0.15μm MESFET	0.18μm BiCMOS
Chip size (mm^2)	0.275	0.56	0.7	0.63	0.319

It is noticed that the active balun is capable of maintaining well amplitude and phase balance over a wide range of bias currents. The simulated results in Fig. 3.10 show that the amplitude difference is within 2 dB from DC to 63 GHz and the phase difference is within 180 ± 10 degrees from DC to 53 GHz when the bias current changes over a large range from 2 mA to 12 mA. The measured results (not shown) also show that the

amplitude imbalance is lower than 2 dB from DC to 60 GHz and the phase imbalance is within 10 degrees from DC to 50 GHz when the bias current changes from 2 mA to 7 mA. The measured input 1-dB compression points, $P_{in,1dB}$, at 35 GHz is -0.4 dBm. The use of CE amplifier with degenerative inductor and CC amplifier results in higher linearity as compared to CE/CB or CS/CG active baluns. The comparison of this new active balun with other previously reported active baluns in Table 3.1 shows that the proposed active balun exhibits the widest balance bandwidth and highest linearity, while having the lowest DC power consumption.

3.3 Differential to Single-ended Active Balun Design

3.3.1 Circuit and Analysis

A half of the circuit of the single-ended to differential active balun in Fig. 3.3 with modified input and output ports can be used as a differential to single-ended active balun. As shown in Fig. 3.11(a), the differential to single-ended active balun consists of two identical HBT transistors and three inductors L_{e1}, L_{e2} and L_b which control the balance of the balun. It differs from the other reported active balun [38], in that inductors L_{e1} and L_{e2} are used instead of resistors and an additional inductor (L_b) is employed. These three inductors enable the balance of the new balun to work up to a much higher frequency, and hence across a much wider frequency range, than that of the other balun. In addition, L_{e1}, as a degenerative inductor, helps improve the linearity of the balun. The use of L_{e1} and L_{e2} also helps reduce the DC power consumption. Fig. 3.11(b) shows the small-signal equivalent circuit of the active balun after several manipulations. The

transistor's output resistance r_o is normally large, around several KΩ, and is omitted for transistor Q_2. Z_{o1} is the output impedance looking into transistor Q_1 from its collector and is calculated as (3.1).

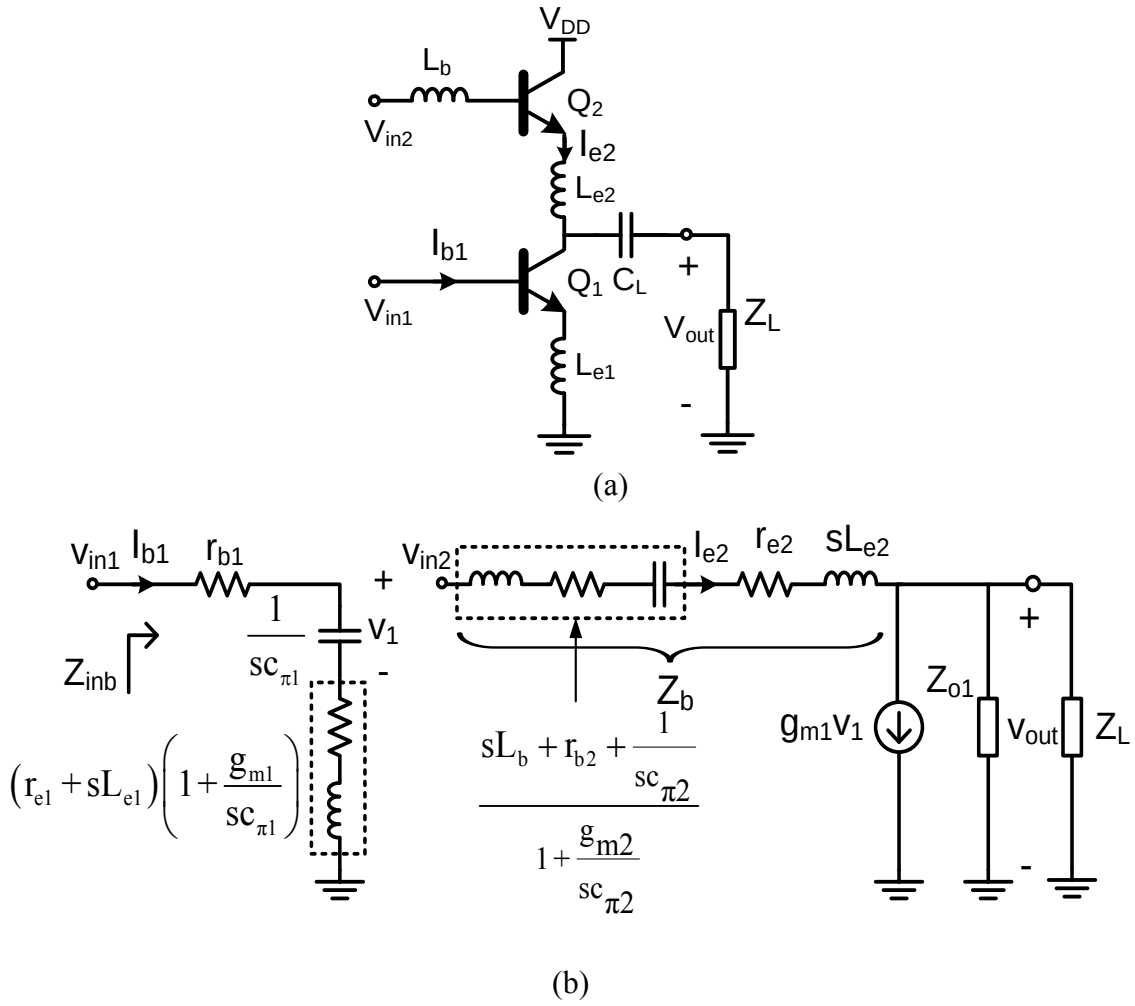


Fig. 3.11. Schematic (a) and equivalent circuit (b) of the differential to single-ended active balun.

The output voltage of the balun V_{out} is a function of two inputs V_{in1} and V_{in2} and, from Fig. 3.11(b), we can derive

$$v_{out} = Z_L \| Z_{o1} \left(i_{e2} - g_{m1} v_1 \right) \tag{3.15}$$

where

$$i_{e2} = \frac{v_{in2} - v_{out}}{Z_b} \tag{3.16}$$

$$v_1 = \frac{1}{sc_{\pi 1}} \frac{v_{in1}}{Z_{inb}} \tag{3.17}$$

with

$$Z_b = \frac{sL_b + r_{b2} + r_{e2} + \frac{L_{e2} g_{m2}}{c_{\pi 2}} + sL_{e2} + \frac{1 + r_{e2} g_{m2}}{sc_{\pi 2}}}{1 + \frac{g_{m2}}{sc_{\pi 2}}} \tag{3.18}$$

$$Z_{inb} = r_{b1} + r_{e1} + \frac{L_{e1} g_{m1}}{c_{\pi 1}} + sL_{e1} + \frac{1 + r_{e1} g_{m1}}{sc_{\pi 1}} \tag{3.19}$$

Z_{inb} is the input impedance of the balun at the input port corresponding to V_{in1}.

Substituting (3.16) and (3.17) into (3.15) and making use of (3.18) and (3.19), we obtain

$$v_{out} = \frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b} \left(v_{in2} - K v_{in1} \right) \tag{3.20}$$

where

$$K = \frac{Z_b}{Z_{inb}} \frac{g_{m1}}{sc_{\pi 1}} = \frac{\frac{g_{m1}}{c_{\pi 1}}}{s + \frac{g_{m2}}{c_{\pi 2}}} \frac{s + \frac{r_{b2} + r_{e2} + \frac{L_{e2} g_{m2}}{c_{\pi 2}}}{L_b} + \frac{sL_{e2} + \frac{1 + r_{e2} g_{m2}}{sc_{\pi 2}}}{L_b}}{\frac{r_{b1} + r_{e1} + \frac{L_{e1} g_{m1}}{c_{\pi 1}}}{L_b} + \frac{sL_{e1} + \frac{1 + r_{e1} g_{m1}}{sc_{\pi 1}}}{L_b}} \tag{3.21}$$

K is referred to as the balance factor. It is noted that the balance factor K in (3.21) is the same as the balance factor in (3.8) and it has all characteristics previously presented.

Similar to analysis of the single-ended to differential balun, L_{e1}, L_{e2} and L_b are obtained at the design frequency, ω_o, from the balance condition as

$$L_{e1} = L_{e2} = \frac{1 + r_{e1} g_{m1}}{\omega_0^2 c_{\pi 1}} = \frac{1 + r_{e2} g_{m2}}{\omega_0^2 c_{\pi 2}} \tag{3.22}$$

and

$$L_b = L_{e1} + \frac{c_{\pi 1}\left(r_{b1} + r_{e1}\right)}{g_{m1}} = L_{e2} + \frac{c_{\pi 2}\left(r_{b2} + r_{e2}\right)}{g_{m2}} \tag{3.23}$$

Now we consider two operation modes of the active balun.

Common mode: Under this mode, $V_{in1}=V_{in2}$, the active balun suppresses the common-mode input signals and its common-mode gain A_{vc} can be derived from (3.20) as

$$A_{vc} = \frac{v_{out}}{v_{in2}} = \frac{v_{out}}{v_{in1}} = \frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b}\left(1 - K\right) \tag{3.24}$$

This common-mode gain is contributed by the factors (1-K) and $\frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b}$. The first represents the main suppression provided by the active balun. The latter, on the other hand, represents the differential gain of the active balun as seen in Eq. (3.25); this gain degrades slightly the overall signal suppression of the active balun.

The magnitudes of (1-K), representing the active balun's primary common-mode signal suppression, and A_{vc}, characterizing the overall suppression of the active balun with and without output matching are shown in Fig. 4.12. As can be seen, the common-mode signal suppression provided by the active balun is significant, particularly around the design frequency. Without the output matching, the active balun provides more than

32-dB suppression up to 40 GHz and infinite suppression at the design frequency of 35 GHz. When the output is matched, the active balun provides the suppression higher than 31 dB up to 40 GHz and also theoretically infinite isolation at 35 GHz. Good common-mode signal suppression up to 80 GHz can also be observed from the plots.

Differential mode: Under this mode, $V_{in1} = -V_{in2} = \frac{V_d}{2}$, with $V_d = V_{in1} - V_{in2}$. This condition, together with the fact that K is almost 1 over a wide frequency range as seen in Fig. 3.5, enables $(1+K) \approx 2$. The active balun now works as an differential amplifier with its gain, A_{vd}, given from (3.20) as

$$A_{vd} = \frac{v_{out}}{v_d} = -\frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b} \tag{3.25}$$

The magnitude of A_{vd} is shown in Fig. 3.12. As can be seen, the active balun provides the differential-mode gain up to 50 GHz for both unmatched and matched output. At the design frequency of 35 GHz, it provides 1.3- and 10-dB gain with and without output matching, respectively.

At the design frequency $f = f_0$, K = 1, and we can obtain from (3.18) and (3.19):

$$Z_b = j\omega_0 L_b \tag{3.26}$$

$$Z_{inb} = R_{in} = r_{b1} + r_{e1} + \frac{L_{e1} g_{m1}}{c_{\pi 1}} = \frac{L_b g_{m1}}{c_{\pi 1}} \tag{3.27}$$

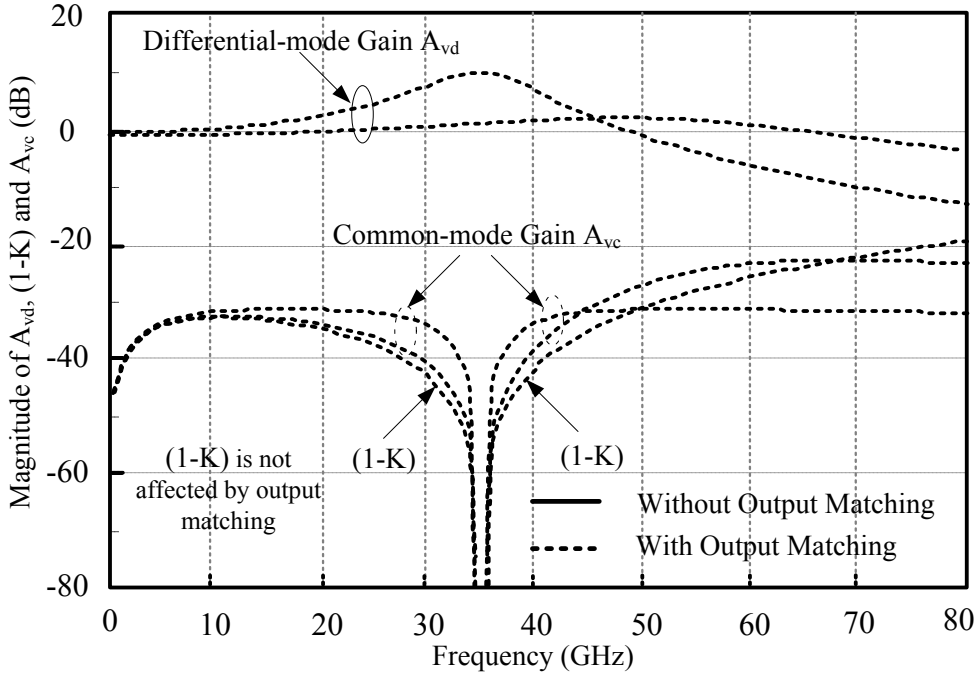


Fig. 3.12. Magnitudes of A_{vd}, (1-K) and A_{vc}. (1-K) is not affected by the output matching.

The matching at the input can be obtained by setting R_{in} in (3.27) equal to 50 Ω, while the output is matched by letting

$$Z_L = \left(Z_b \| Z_{o1}\right)^* \tag{3.28}$$

where * indicates conjugate match. The gain of the balun with output matching at ω_o can be obtained from (4.1), (4.25) and (4.26) as

$$A_{vd} = -\frac{1}{2}\frac{R_{o1}}{\omega_0 L_b} \tag{3.29}$$

or

$$|A_{vd}| = \frac{1}{2} \frac{R_{o1}}{\omega_0 \left(L_{e2} + \frac{c_{\pi 2}\left(r_{b2}+r_{e2}\right)}{g_{m2}} \right)}$$

$$= \frac{1}{2} \frac{R_{o1}}{\left(\frac{1+r_{e2}g_{m2}}{\omega_0 c_{\pi 2}} + \frac{\omega_0 c_{\pi 2}\left(r_{b2}+r_{e2}\right)}{g_{m2}} \right)} \tag{3.30}$$

upon using (3.12) and (3.13).

In this analysis, it is assumed that V_{in1} and V_{in2} are idea sources without internal impedances. In reality, these impedances would modify the derived equations (3.12) and (3.13) for the active balun's balanced conditions. This, however, will not cause loss of our analysis' generality. The foregoing formulation process still remains the same, except that the real and imaginary parts of these impedances, appearing at the input ports of the balun's equivalent circuit in Fig. 3.11(b), will be absorbed into the impedances described in (3.18) and (3.19).

3.3.2 Design and Simulated Result

The proposed differentia to single-ended active balun was designed and simulated using Jazz 0.18-μm BiCMOS process [21]. Two HBT transistors Q_1 and Q_2 in the active balun have the same size with an emitter area of 0.15 x 8.28 μm^2 and are biased at a DC current of 8.2 mA to get the highest f_T. The bases of Q_1 and Q_2 are biased at 0.92 V and 1.8 V, respectively, through large resistors which do not affect the balun's RF operation. The collector of Q_2 is connected to V_{DD} of 1.8 V. The values of inductors L_{e1}, L_{e2} and L_b are first estimated from Eqs. (3.12) and (3.13) and then optimized in

Cadence simulation at 35 GHz to have their final values of 130, 130 and 145 pH, respectively. These inductors have been designed and simulated using the full-wave electromagnetic simulator IE3D [22], having the quality factors around 18.

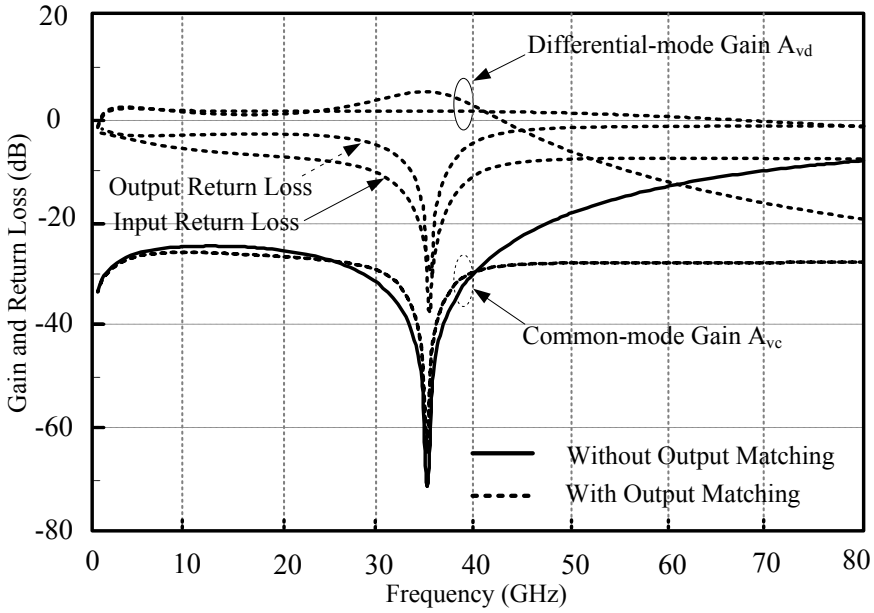


Fig. 3.13. Simulated differential- and common-mode gain and return losses.

Figure 3.13 shows the simulated differential- and common-mode gain and input (port with V_{in1}) and output return losses of the differential to single-ended active balun with and without output matching network under small signal condition. The simulated results show that the balun exhibits an ultra-wideband, ultra-high-common-signal suppression performance while consuming a DC current of 8.2 mA from a 1.8 V source. From 2 to 40 GHz, without output matching, the differential-mode gain is from 1.5 to 2.4 dB and the common-mode gain is from -25 to -70 dB, while with output matching,

the differential-mode gain is from 1 to 5.2 dB and the common-mode gain is from -25.7 to -65 dB. From 29.3 to 41 GHz, the input return loss is from 10 to 35 dB and from 32.7 to 37.1 GHz, the output return loss is from 10 to 38 dB. The best matching of input and output occur at 35 GHz as designed. At the design frequency of 35 GHz, the differential-mode gain is 1.8 dB and 5.2 dB while the common-mode gain is -71 dB and -65 dB corresponding with unmatched and matched output. The common-mode gain results show that the active balun provides extremely high common-mode signal suppression of 65 dB or 71 dB at 35 GHz and higher than 25 dB suppression over ultra-wide bandwidth from 2 to 40 GHz.

Simulation results also show that in the differential-mode, the active balun has an input 1-dB compression and input IP3 power of 0 dBm and 5.9 dBm, respectively, with unmatched output and of -8 dBm and 0.1 dBm, respectively, with matched output.

CHAPTER IV

ULTRA-HIGH ISOLATION RF SWITCH*

RF switches are one of the important building blocks in RF, microwave and millimeter-wave communication and radar systems. Single-pole single-throw (SPST), single-pole double-throw (SPDT) and multiple-pole multiple-throw switches (MPMT) can be used for various applications such as variable attenuators and phase shifters, transmit/receive modules, RF-pulse formers, and multi-standard multimode communication systems. Particularly, SPST switches can be used as a stand-alone component or as an integral element in subsystems and/or systems – for instance, in RF pulse transmitters [39]. For high-data-rate, short-range communication and some high-resolution radar systems, the SPST switches used for the transmitters' pulse-formation should have fast switching time and high isolation, in addition to low insertion loss. In this chapter, a new RF switch architecture possessing ultra-high isolation and possible gain is introduced.

4.1 CMOS SPST Switch Architectures and Performance

Fig 4.1 shows the RF SPST switch model in a 50-Ω network. The RF switch is turned on and off by a control voltage V_{ctr}. Insertion loss, isolation, linearity, switching time, and input and output return losses are the key metrics characterizing the performance of RF switches. When the switch is in the on state, the RF signal from the source passes through the switch to the load. Due to the imperfections, the RF signal experiences the power loss and possible distortion in the switch. The switch insertion loss characterizes the power loss in the switch and the switch linearity, specified by the 1-dB compression point, characterizes the signal handling capability without distortion of the switch. On the other hand, in the off state, the RF switch blocks the RF signal from passing to the load. The signal attenuation of the switch in the off state is characterized by its isolation. The switching time between the on and off states is an importance parameter characterizing the switch performance in high speed systems as well. In addition, like other blocks in RF systems, the RF switch is required to have good input and output matching over the operating frequency range. The input and output matches of the RF switch are characterized by the input and output return losses.

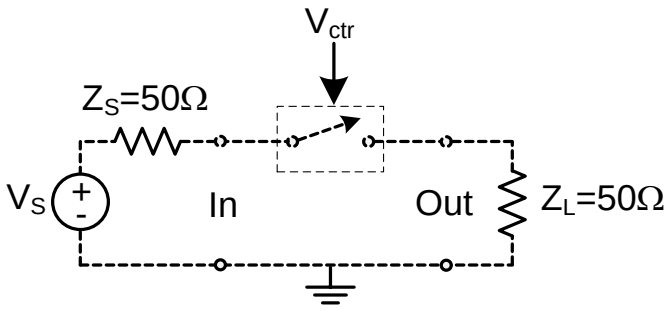


Fig. 4.1. RF switch model in a 50-Ω network.

In the simplest implementation, the SPST switch consists of a series or shunt MOSFET transistor as shown in the Fig. 4.2 (a) and (b). In the normal operation, the Sub terminal is connected to the Source. The large gate resistors, R_g, are used to prevent RF signals leaking to ground, hence improving the insertion loss. Using large gate resistors, however, results in the large switching time which is proportional to the product of the gate resistor and total capacitors at the gate.

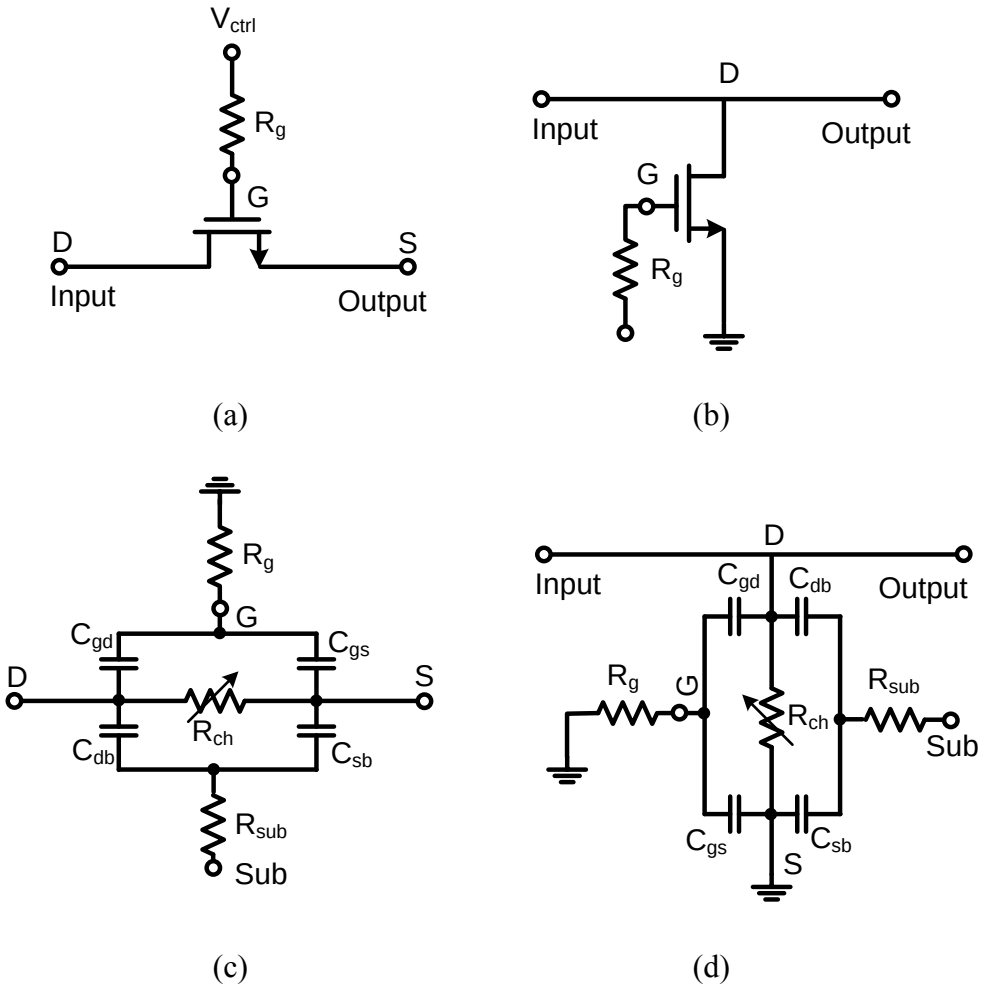


Fig. 4.2. Series SPST switch (a), shunt SPST switch (b), equivalent circuit of series SPST switch (c) and equivalent circuit of shunt SPST switch (d).

Fig. 4.2 (c) and (d) show the equivalent circuits of the corresponding series and shunt SPST switches. The substrate resistances, R_{sub}, representing for the loss in the silicon substrate have small values. The channel resistors, R_{ch}'s, are small when the transistors are in the on-state and large when the transistors are in the off-state. At low frequencies, the switch insertion loss and isolation are mainly determined by the channel resistors. However, at high frequencies the switch performances are dependent on the parasitic capacitors including C_{gs}, C_{gd}, C_{db} and C_{sb} as well. As shown in the Fig. 4.2(a) and (c), when the series SPST switch is in the off-state, the parasitic capacitors C_{gs} and C_{gd} allow the RF signal to leak from the input to output; hence decreasing the isolation. On the other hand, as shown in the Fig. 4.2(b) and (d), when the shunt SPST switch is in the on-state, the parasitic capacitors C_{db} and C_{sb} conduct the RF signals from the drain to the ground; hence increasing the insertion loss.

Increasing the size of the transistor in the series SPST switch improves its insertion loss as the channel resistor is smaller, but reduces its isolation as the parasitic capacitors become larger, resulting in more RF leakage from input to output. On the other hand, increasing the size of the transistor in the shunt SPST switch improves its isolation, but reduces its insertion loss as the parasitic capacitors of the transistor become larger; hence allowing more RF leakage from the input to the ground.

The series-shunt switch configuration as shown in Fig. 4.3 is commonly used to improve the insertion loss and isolation for the SPST switch. At low frequencies, the series transistor mainly determines the insertion loss while the shunt transistor mainly determines the isolation for the SPST switch. However, at high frequency ranges the

insertion loss and isolation are affected by both transistors. A procedure to select the optimum sizes for the series and shunt transistors for a given insertion loss or/and isolation is presented in the following section.

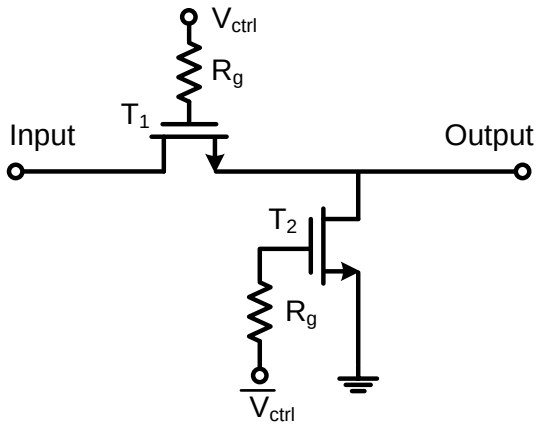
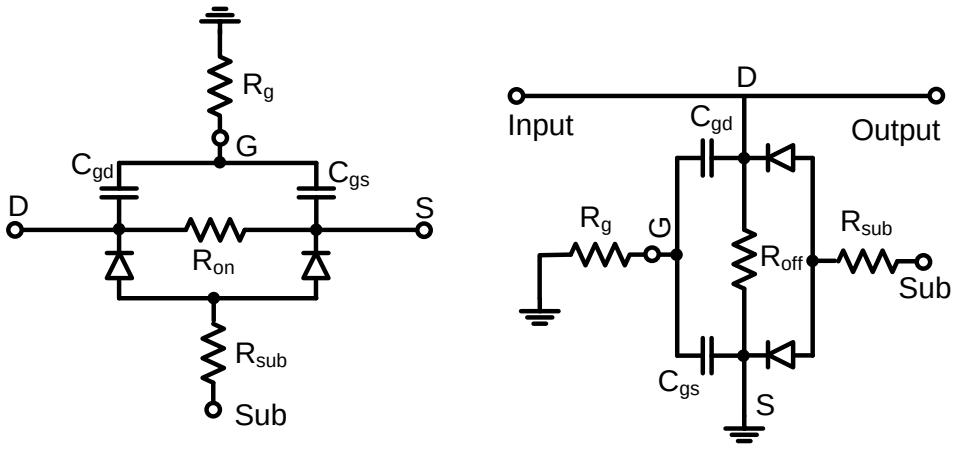


Fig. 4.3. Series-shunt SPST switch.

The linearity of the SPST switch in the on-state is limited by the parasitic diodes at the drain and source. When the RF input power is larger than a certain level, the parasitic diodes, which are off in the small signal conditions, are on and cause the distortion to the RF signal. Fig. 4.4(a) and (b) show the series and shunt SPST switch equivalent circuits in their on-states. They are modified from Fig. 4.2(c) and (d) in that the parasitic capacitors C_{db} and C_{sb} are replaced by two diodes representing for two PN junctions at the drain and source. It is noted that in the normal implementation, the Sub is connected to the source. In Fig. 4.4 (a), when the input power increases, the negative drain-to-source voltage swing reaching $-V_T$ turns on the diode between drain and body, resulting in clipped RF signals, where V_T is the threshold voltage to bias forward the

diode. Similarly, in Fig. 4.4 (b) a voltage swing reaching $-V_T$ at the drain would push the drain parasitic diode to forward bias condition, resulting in distorted RF signals. Making the substrate floating and biasing the substrate with negative voltages are effective approaches to increase the linearity for the MOSFET-based RF switch [40]-[42].



(a) (b)

Fig. 4.4. Series SPST switch in on-state (a) and shunt SPST switch in on-state (b).

4.2 Deep n-well CMOS Transistor with Floating Body

The main limitation of the CMOS transistors when used in switches is their parasitic capacitors, C_{gd}, C_{gs}, C_{sb} and C_{db}. The effects of C_{sb} and C_{db} are more remarkable than those of C_{gs} and C_{gd} at millimeter-wave frequencies due to their larger values and the conductive substrate. To reduce the effects of these capacitors, the floating-body technique with deep n-well transistors is used.

Figure 4.5 shows the cross sectional view of a deep n-well nMOS transistor and its schematic and model. R_{sub} represents the conductive substrate and substrate-ground

connection losses which are normally small for good substrate and substrate-ground connection. An investigation of substrate effects has been reported in [43]. The effects of the substrate, however, have not been included in the transistor models and depend strongly on the layout of circuits. The deep n-well structure is used to isolate the bulk of the transistor from the substrate connecting to the ground, hence preventing the leakage of RF signals from the transistor conducting channel to the ground. However, the deep n-well layer also inadvertently creates a pair of parasitic junction diodes, effectively equivalent to a parasitic capacitor C_{dnw}, as shown in Fig. 4.5. The value of this capacitor is proportional to the size of the deep n-well layers needed to enclose the transistors. As the operating frequency increases, or the transistor size is larger, the impedance of this capacitor becomes smaller, degrading the isolation provided by the deep n-well structure.

To maximize the isolation provided by the deep n-well layer, the isolated bulk of the transistor is biased at 0 V with a large resistor of 10 KΩ to make the transistor body floating and the deep n-well is biased at 1.8 V through a large resistor to establish a reverse-bias for the two p-n deep n-well junctions to reduce the value of C_{dnw}. The floating body helps increase the linearity for the transistor.

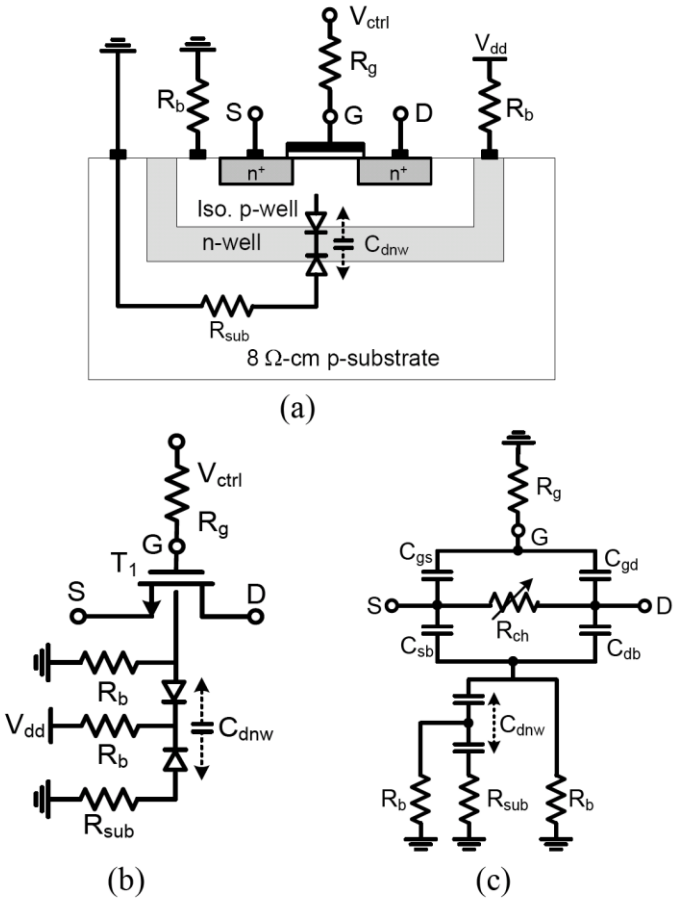


Fig. 4.5. Cross sectional view of a deep n-well transistor (a) and its schematic (b) and model (c).

4.3 Design of Series-Shunt SPST Switch Using Contour Graph

At high frequency ranges, especially millimeter-wave frequency, the insertion loss and isolation of the series-shunt SPST switch using the deep-n-well transistors, shown in Fig. 4.3, are mainly limited by the transistor parasitic capacitors and deep-n-well parasitic capacitors; all of which are complicatedly related to the transistor and deep-n-well layer sizes. This requires an analysis to find the optimum sizes for both the series and shunt transistors for a given design target of insertion loss and/or isolation. To

facilitate the device selection, contours corresponding to fixed insertion loss and isolation are plotted as the sizes of the series and shunt transistors are simultaneously swept at an interested frequency. The sizes of the deep n-well layers, hence the deep n-well parasitic capacitors, are also changed according to the transistor sizes. Fig. 4.6 shows the insertion and isolation contours for a pair of series and shunt 0.18-μm MOSFETs with a 400-Ω gate resistor at 35 GHz versus the finger numbers of the series and shunt transistors. The finger-width for both transistors is 4 μm.

It is found that the insertion loss contours have nearly parabolic form, while those for the isolation behave almost linearly. The insertion loss and isolation trade-off can be clearly seen in Fig. 4.6. The graph of the insertion loss and isolation contour provides a clear visual aid for the switch design. For a given insertion loss or isolation, the optimum transistor sizes are selected at the optimum point where an insertion loss contour and an isolation curve are tangential to each other. The plus (+) marks in the graph show some of the optimum points. For a given insertion loss, the optimum point provides the highest isolation while, for a given isolation, it provides the lowest insertion loss. The sizes of transistors corresponding to these optimum points should be chosen for the switch design. This analysis provides a method to determine the optimized transistor sizes for the series-shunt SPST switches.

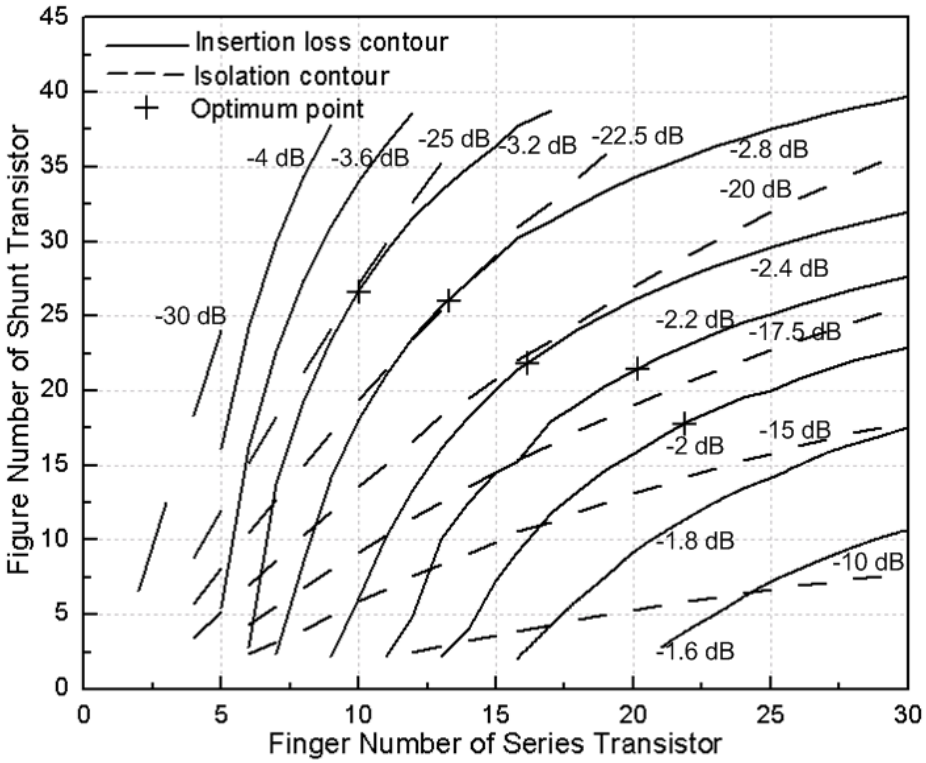


Fig. 4.6. Insertion loss and isolation contours.

4.4 Wide-band SPST Switch with Synthetic Transmission Line

Figure 4.7 shows the schematic of an SPST switch based on a series-shunt switch topology with deep n-well transistors implemented using a synthetic transmission-line technique for wide-band operation. The insertion loss and isolation of the SPST switch simultaneously depend on the size of the series and shunt transistors. Increasing the size of the series transistor reduces the on-state resistance, hence reducing the insertion loss at low frequencies, but, at the same time, also increases the parasitic capacitances including the deep n-well capacitance C_{dnw}, resulting in increase in insertion loss and

reduction of isolation at high frequencies. On the other hand, increasing the size of the shunt transistor increases the isolation, but also increases the insertion loss.

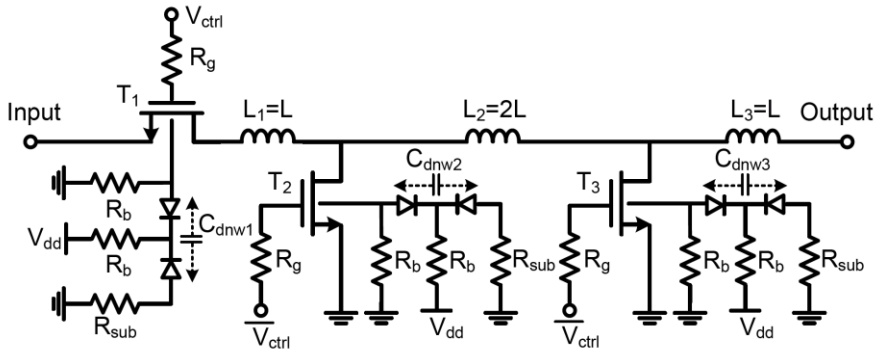


Fig. 4.7. Schematic of the SPST switch using synthetic transmission line.

At high frequencies, the drain-to-ground off-capacitances of the two (identical) shunt transistors T_2 and T_3 are the main factor in increasing the insertion loss and limiting the bandwidth of the switch. The synthetic transmission-line technique absorbs the effect of these capacitances into a transmission line, hence increasing the switch's bandwidth.

The series inductors are optimized by considering the drain- ground off-capacitors C_{off} of T_2 and T_3 in order to meet certain characteristic impedance Z_o and finite cutoff frequency f_c given by

$$Z_o = \sqrt{\frac{L}{C_{off}}} \tag{4.1}$$

and

$$f_c = \frac{1}{\pi\sqrt{LC_{off}}} \tag{4.2}$$

assuming lossless components. Ideally, synthetic transmission lines consist of many identical LC sections. A practical synthetic transmission line, however, has a limited number of sections - for example, two in our design - so its operating frequency range, within which the insertion loss is reasonably low and return loss is sufficiently large, is much lower than the cutoff frequency given in (4.2). Our analysis based on various transistors shows that the cutoff frequency should be approximately at least 3 times the highest operating frequency so that a synthetic transmission line of limited number of sections will demonstrate low insertion loss and high return loss. The value of L and the size for T_2 and T_3 can be determined by first assuming a cutoff frequency equal to at least 3 times of the highest operating frequency. L and C_{off} can then be determined by solving (4.1) and (4.2), and, from C_{off}, the size of T_2 and T_3 can be selected. It is noted that, if very high cutoff frequency is chosen, L may be too small to be realized and C_{off}, hence T_2 and T_3 size, may be so small that gives poor isolation for the SPST switch. The size of T_1 is finally selected to produce an insertion loss as low as possible while not affecting the isolation significantly.

4.5 Ultra-High-Isolation RF Switch Architecture

4.5.1 Motivation

For high-data-rate, short-range communication and some high-resolution radar systems, the SPST switches used for the transmitters' pulse-formation should have fast switching time and high isolation, in addition to low insertion loss. Among those, high isolation is especially crucial in order to reduce or prevent RF leakage. Undesired RF

leakage not only causes external effects, such as harm to other coexisting systems, but also internal effects such as reduced dynamic range.

Most of the reported high-performance switches were designed using III-V semiconductor based processes. However, as CMOS and BiCMOS technologies have scaled down and used in many RF integrated systems due to their low cost and for high integration capability, they have become great candidates for high-speed, low-loss and high-isolation switches at high frequencies.

Various CMOS RFIC switches have been reported from 2.4 GHz to 40 GHz, e.g. [43]-[48]. However, designing CMOS switches with low loss and high isolation over ultra-wide bandwidths at high frequencies crossing the millimeter-wave boundary is still challenging due to various issues such as effects of the parasitic capacitors at the PN junctions and the conductive substrate of MOSFETs at these frequencies. A high-isolation switch topology based on signal cancellation was described in [49]. This switch implements differential ports and requires differential input signal for RF leakage signal cancellation. The signal cancellation, and hence isolation improvement, is primarily dependent on the amplitude and phase balance of the input differential RF signal provided by a preceding circuit.

The CMOS T/R switch reported in [44] exhibits an insertion loss of 0.8 dB and an isolation of 29 dB at 5.8 GHz by optimizing the transistor widths and bias voltages, and minimizing the substrate resistances. Floating transistor body implemented by LC tanks [45] or deep n-well transistors [46]-[48] has been used to improve the insertion loss, isolation and linearity. For instance, 1.5-dB insertion loss and 30-dB isolation at 5.2

GHz for a T/R switch [45], and 1.1-dB insertion loss along with 27-dB isolation at 5.8 GHz for another T/R switch [46] have been achieved. The CMOS T/R switch implementing synthetic transmission line in [48] employs large-size transistors to achieve insertion loss of less than 2.5 dB and isolation of more than 25 dB over a wide bandwidth up to 20 GHz. Using parallel resonators between the drain and source of transistors and a high substrate resistance network results in higher than 32-dB isolation and lower than 2.2-dB insertion loss at 35 GHz for a SPDT switch [43]. A SiGe differential SPST switch with current steering producing less than 3-dB insertion loss between 20-26 GHz and higher than 42-dB isolation from 10-30 GHz was also reported [50].

While the LC tank technique in [45] leads to more complexity and large chip area [47], using deep n-well transistors with large bulk bias resistors results in a more compact chip but with possibly limited performance at high frequencies, especially in the millimeter-wave region. As the operating frequency increases, the impedances of the parasitic capacitors coexisting with the deep n-well layer become smaller; hence lessening the isolation function of the deep n-well layer. As a result, for a given device technology, up to some certain frequency extent, the deep n-well layer becomes less effective in improving insertion loss and isolation. To reduce insertion loss and enhance isolation further, other techniques should be employed.

This section presents a new RF switch architecture that not only can increase the isolation significantly, but can also lower the insertion loss or potentially produce gain. The development of a new ultra-wideband RF switch operating from 10 to 38 GHz with

very high isolation and low loss/gain is also demonstrated. The enhanced isolation is obtained by implementing a RF leakage cancellation technique, in which the leaking RF signal when the switch is off is significantly reduced or removed by combining two identical off-switches through an active balun presented in Chapter III. The active balun not only helps increase the isolation of the switch when it is off, but also provides some possible gain during its on-state operation. The designed RF switch exhibits an unprecedented performance from 10 to 38 GHz under small signal stimulus: -2.6 dB (loss) to 0.4 dB (gain), 40 to about 70-dB isolation, and 8 to 20-dB input return loss. Within the narrow band around 35.5-38.5 GHz, the switch achieves extremely high isolation approaching the limit measurable by the vector network analyzer with the highest isolation of around 70 dB at 36 GHz. It has a chip size of 440 x 520 μm^2 and consumes a DC current of only 8 mA from a 1.8V source.

4.5.2 Architecture and Operation

Figure 4.8 shows the new RF switch architecture. It consists of two identical SPST switches and an active balun. The active balun can also be replaced with a passive balun. The two identical switches are named “Off-SPST” switch (always operating in the off-mode) and “Core-SPST” switch operating as a normal switch (on/off). The Off-SPST and Core-SPST switches can be implemented using any topology such as a simple conventional switch employing series and/or shunt transistors.

The RF switch is off or on according to the off-state or on-state of the Core-SPST switch, respectively. When the Core-SPST switch is off, an RF signal (V_{in1}) leaking

through this switch, due to its limited isolation, appears at the input port 1 of the balun. At the same time, another RF leakage signal (V_{in2}) from the Off-SPST switch also appears at the balun's input port 2. These signals are theoretically equal since both switches are identical, and are cancelled in the balun, resulting in no RF signal at the output of the RF switch, and hence (theoretically) infinite isolation at the design frequency of the balun.

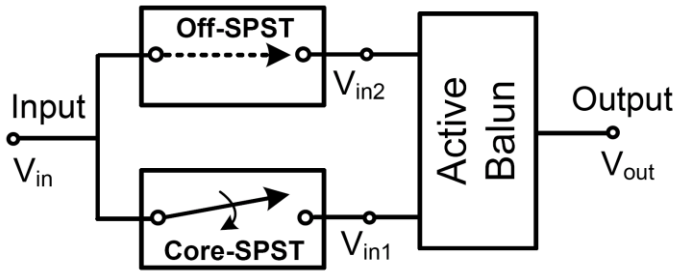


Fig. 4.8. High-isolation RF switch architecture.

It is noted that when the Core-SPST switch, and hence the RF switch, is on, there are still two RF signals passing through the balun, the main V_{in1} signal from the "on" Core-SPST switch and the leaking V_{in2} signal from the Off-SPST switch. However, as the balun's output signal (V_{out}) is a function of the difference between V_{in1} and V_{in2}, and V_{in1} is much larger than V_{in2}, V_{out} is not altered significantly. In fact, the active balun can also be designed to function as an amplifier to provide amplification for V_{in1} to compensate for the loss it suffers as going through the Core-SPST switch. This, in turn, results in an overall gain for the RF switch.

4.5.3 Switch Analysis

The active balun shown in Fig. 3.11(a) in chapter III is used. The active balun is characterized by its transfer function in (3.20) and balance factor K in (3.21). For convenience, the transfer function of the active balun is rewritten as

$$v_{out} = \frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b}\left(v_{in2} - K v_{in1}\right) \tag{4.3}$$

Now we consider two cases corresponding to the on and off states of the RF switch which are obtained when the Core-SPST switch is turned on and off, respectively.

Case 1 (RF Switch Off): Under this condition, V_{in1} and V_{in2} are equal and represent two identical leaking RF signals feeding the balun. The gain of the active balun when the switch is off can be derived from (4.3) as

$$A_{voff} = \frac{v_{out}}{v_{in2}} = \frac{v_{out}}{v_{in1}} = \frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b}\left(1 - K\right) \tag{4.4}$$

A_{voff} measures the suppression of the leaking RF signal V_{in1} as it traverses the active balun to the RF switch's output. It represents the additional isolation provided by the active balun to the RF switch besides the isolation obtained from the Core- SPST switch. This extra isolation is contributed by the factors (1-K) and $\frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b}$. The first represents the main isolation provided by the balun. The latter, on the other hand, represents the gain of the active balun when the RF switch is on; this gain degrades slightly the overall isolation of the RF switch.

The magnitudes of (1-K), representing the active balun's primary isolation contribution, and A_{voff}, characterizing the overall isolation contribution of the active

balun to the RF switch, with and without output matching are shown in Fig. 3.12. It is noted that the gain of the active balun when the switch is off, A_{voff}, is the common-mode gain in Fig 3.12. As can be seen, the extra isolation provided by the active balun to the proposed RF switch is significant, particularly around the design frequency, as compared to the conventional implementation of a single switch (i.e., Core-SPST switch alone). This effective isolation-enhancement technique is very useful for extending the isolation bandwidth of RF switches into the millimeter-wave range. Without the output matching, the active balun provides more than 32-dB isolation up to 40 GHz and infinite isolation at the design frequency of 35 GHz. When the output is matched, the active balun provides an isolation higher than 31 dB up to 40 GHz and also theoretically infinite isolation at 35 GHz. Good isolation improvement up to 80 GHz can also be observed from the plots 3.12.

Case 2 (RF Switch On): When the Core-SPST switch is on, the main RF signal V_{in1} from the Core-SPST switch is much larger than the leaking RF signal V_{in2} from the Off-SPST switch. This, together with the fact that K is almost 1 over a wide frequency range as seen in Fig. 3.5, enables V_{in2} to be ignored in Eq. (4.3). The active balun now works as an amplifier with its gain given from (4.3) as

$$A_{von} = \frac{v_{out}}{v_{in1}} = -\frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b} K \approx -\frac{Z_L \| Z_{o1}}{Z_L \| Z_{o1} + Z_b} \tag{4.5}$$

The magnitude of A_{von}, basically the different-mode gain of the active balun, is shown in Fig. 3.12, demonstrating possible gain contribution to the RF switch. As can be seen, the active balun provides gain for the RF switch up to 50 GHz for both unmatched

and matched output. At the design frequency of 35 GHz, it provides 1.3- and 10-dB gain with and without output matching, respectively. Of particular note is that, over a narrow frequency range, the proposed RF switch can achieve both high gain and extremely high isolation at microwave and millimeter-wave frequencies with proper device technologies.

4.6 10-38-GHz Ultra-high Isolation SPST Switch Design

The ultra-high isolation SPST switch was designed and fabricated using Jazz 0.18-μm BiCMOS process [21]. All the on-chip inductors and interconnecting lines were designed and simulated using the full-wave electromagnetic simulator IE3D [22].

4.6.1 Core-SPST and Off-SPST Switch Design

The Core-SPST and Off-SPST switches are identical and their schematics are given in Fig. 4.7. A small gate-bias resistor (R_g) of 200 Ω is chosen for possible high-speed switching [39]. All other bias resistors (R_b) have the same value of 10 KΩ. R_{sub} is assumed to be very small, around 0.1 Ω, which is reasonable with a very good ground-to-substrate contact implemented in the layout.

The design procedure presented in Part 4.4 is used to determine inductors L_1, L_2 and L_3 and the transistor sizes. Since the Core- and Off-SPST switches are designed to have a wide bandwidth up to 40 GHz, the cutoff frequency of the synthetic transmission line, f_c, is chosen to be 150 GHz. Solving Eqs. (4.1) and (4.2) with Z_o=50 Ω and f_c=150 GHz, we obtain L = 106 pH and C_{off}=42.2 fF. From C_{off}, the size of transistors T_2 and T_3

is found to be 75 μm, consisting of 15 fingers of 5-μm width. Using the isolation and insertion loss contour graph developed in Part 4.3, the size of transistor T_1 is chosen as 40 μm for low insertion loss. The small size selected for T_1 also leads to a large input impedance for the Off-SPST switch to facilitate a good matching at the input of the proposed RF switch. Fig. 4.9 shows the simulated insertion loss, return loss and isolation of the designed SPST switch. The simulated results show that the SPST has an insertion loss less than 3.9 dB, isolation higher 35 dB, and return losses more than 16 dB from DC up to 40 GHz.

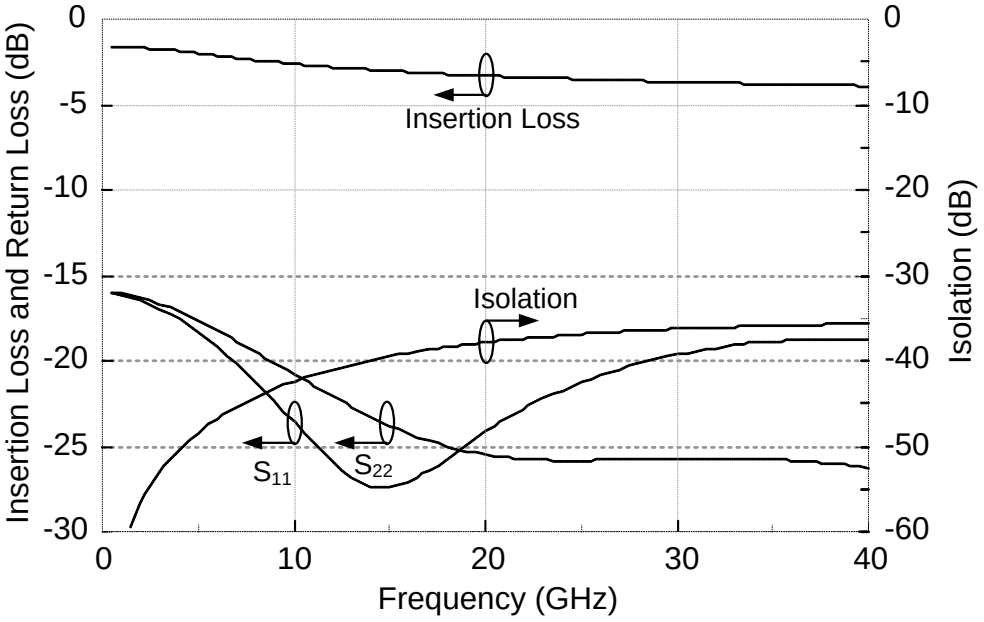


Fig. 4.9. Simulated insertion loss, return loss and isolation of the SPST switch.

4.6.2 RF Switch Design

Figure 4.10 shows the complete schematic of the proposed RF switch. It consists of two identical SPST switches and an active balun. The Off-SPST switch is always in off-state while the Core-SPST switch functions as a normal on-off switch controlled by V_{ctrl} and $\overline{V}_{ctrl}$. The two HBT transistors Q_1 and Q_2 in the active balun have the same size with an emitter area of 0.2x 8.28 μm^2 and are biased at a DC current of 8 mA. The bases of Q_1 and Q_2 are biased at 0.92 V and 1.8 V, respectively, through large resistors which do not affect the balun's RF operation. The collector of Q_2 is connected to V_{DD} of 1.8 V. The values of inductors L_{e1}, L_{e2} and L_b are first estimated from design Eqs. (3.12) and (3.13) and then optimized in Cadence simulation [23] at 35 GHz. Their final values are 130 pH, 130 pH and 145 pH, respectively.

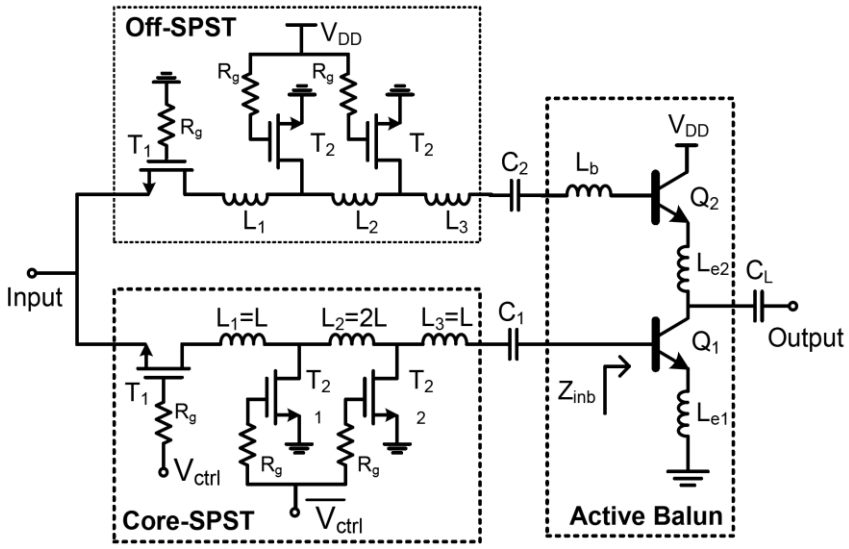


Fig. 4.10. Complete schematic of the proposed RF switch.

The input impedance of the Off-SPST switch in Fig. 4.10 has to be much larger than that of the Core-SPST switch in its on-state, so when the proposed RF switch is on, the Off-SPST switch will not degrade the overall RF switch's input matching and hence its loss or gain. This requires a small size for the two series transistors T_1. The designed gate width of 40 μm for T_1 meets this requirement.

Table 4.1 RF switch's parameters

Circuit Elements and Value			
T_1		40 μm gate width	
T_2, T_3		70 μm gate width	
Q_1, Q_2		0.2 x 8.28 μm^2 emitter area	
L_1, L_3	140 pH	L_b	145 pH
L_2	280 pH	R_g	200 Ω
L_{e1}, L_{e2}	130 pH	R_b	10 KΩ
C_1, C_2, C_L	2 pF	V_{DD}	1.8 V

The active balun acts as a load to the Core-SPST switch and hence its input impedance Z_{inb}, as given in Eq. (3.19), directly affects the RF switch's input matching. Since the Core-SPST switch is designed as a 50-Ω synthetic transmission line and the frequency-dependent Z_{inb} can only be real at a single design frequency, as can be seen from Eq. (3.28), a perfect match can only be possible at a single frequency. In order to obtain a good input matching for the RF switch across a wide bandwidth up to 40 GHz, the value of L, and hence L_1, L_2 and L_3, is optimized to get the best input matching at 25

GHz, instead of at the design frequency of 35 GHz. L = 140 pH is finally chosen. Table 4.1 lists the parameters of the designed RF switch.

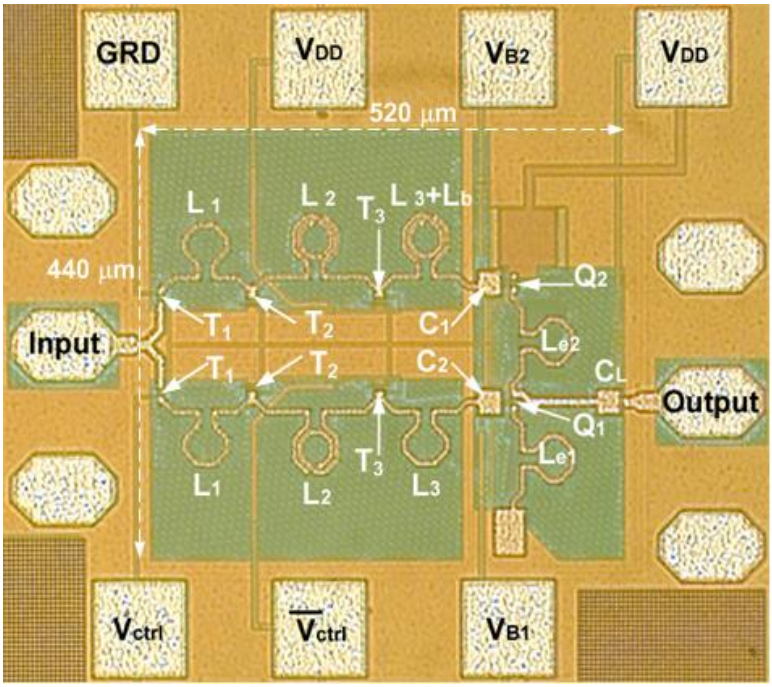


Fig. 4.11. Microphotograph of the proposed RF switch.

The microphotograph of the RF switch is shown in Fig. 4.11 with a chip area of 440 x 520 μm^2. The layout is made as symmetric as possible to enhance the balance of the active balun which helps suppression of the leaking RF signal as much as possible.

4.6.3 RF Switch Performance and Discussion

The proposed RF switch was measured on-chip using an Agilent PNA E8361C vector network analyzer (VNA). The Short-Open-Load-Thru calibration method along

with Microtech's impedance standard substrate standards was used.

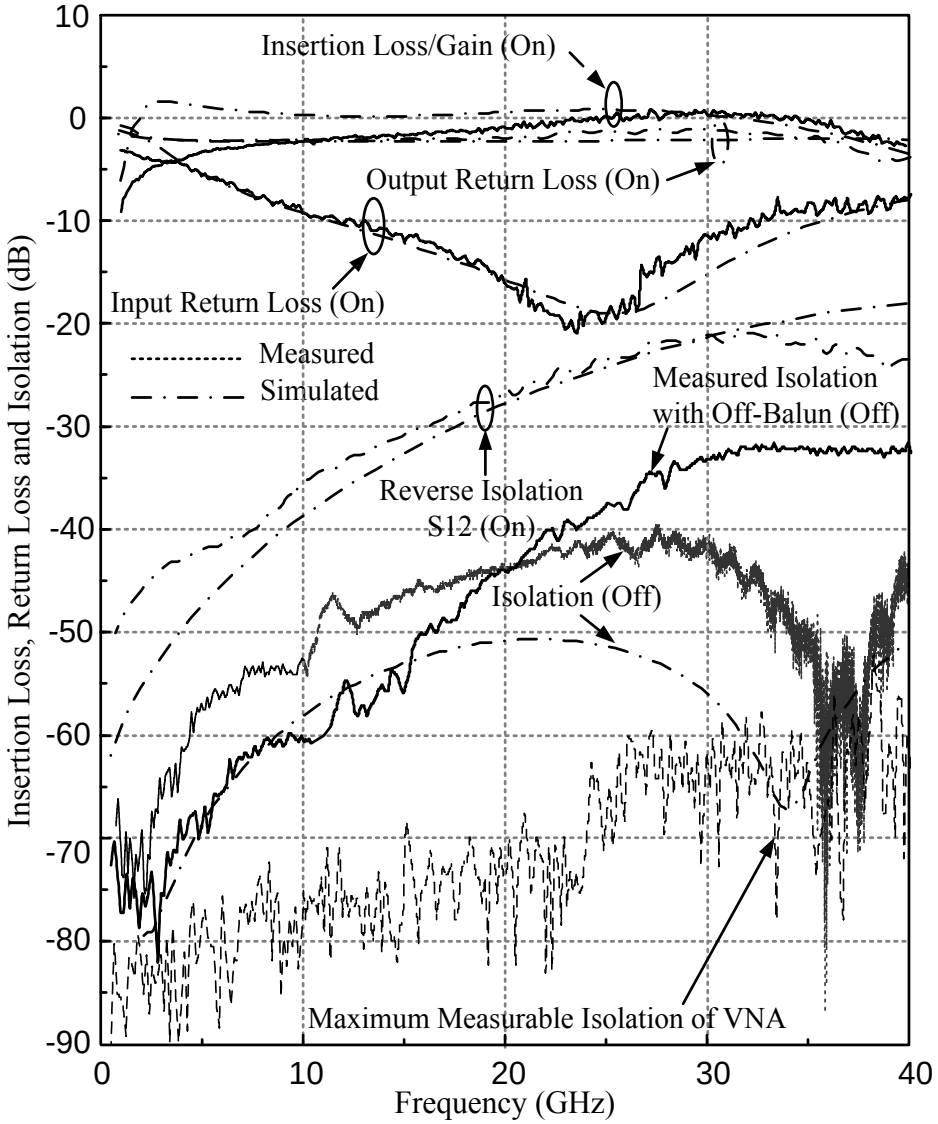


Fig. 4.12. Simulated and measured insertion loss/gain, return losses and isolation.

The unconditional stability of the switch is confirmed through simulations. Over 1-50 GHz, the switch's stability K and $|\Delta|$ factors are larger than 1.5 and smaller than

0.83, respectively. Fig. 4.12 shows the simulated and measured insertion loss/gain, reverse isolation (S12), input and output return loss, and isolation of the proposed RF switch under small signal conditions. The measured results show that the RF switch exhibits an ultra-wideband, ultra-high-isolation performance while consuming a DC current of only 8 mA from a 1.8 V source. From 10 to 38 GHz, the loss/gain is from -2.6 dB (loss) to 0.4 dB (gain), the input return loss is from 8 to 20 dB, the output return loss is from 1 to 5 dB, the reverse isolation under on operation is from 21 to 35 dB, and the isolation goes from 40 to about 70 dB. The isolation approaches 75 dB as the frequency is reduced to below 3 GHz. The RF switch provides the highest gain of 0.4 dB at 30 GHz, maximum input return loss of 20 dB at 23.5 GHz and, especially, an extremely high isolation around 70 dB at 36 GHz. It is noted that the RF switch was designed without an output matching network, which results in a very poor output return loss. This, however, does not affect the balun performance. As noted in the balun analysis, the active balun can achieve its balance, hence RF leakage suppression leading to very high switching isolation, regardless of its load. Nevertheless, an output matching network should be included to improve the output return loss and gain for the switch.

Within the narrow band around 35.5-38.5 GHz, the isolation of the RF switch, reaching ultra-high values with the highest value of about 70 dB at 36 GHz, is found to be limited by the measured isolation limitation of the VNA as shown in Fig. 4.12. The VNA's highest isolation level was measured by lifting the two RF probes into air and far away from each other. The RF switch may provide higher than 70 dB isolation at 36 GHz if measured with a VNA having higher isolation capability.

The calculated isolation of the proposed RF switch, as seen in Fig. 4.12, is substantially higher than that of a conventional switch topology without the RF-leakage cancellation as shown in Fig. 4.9, particularly at the design center frequency, demonstrating the superior isolation characteristic of the proposed RF switch. At 34 GHz, it shows a calculated isolation of 67 dB as compared to 36 dB obtained from a conventional switch. It is noted that, the isolation of a conventional switch usually keeps decreasing as the frequency is increased, but the isolation of the proposed RF switch, while also following a similar trend, has a particular window within which the isolation is increased substantially, reflecting the RF leakage suppression characteristic provided by the active balun.

Figure 4.12 also shows the measured isolation of the switch when the active balun is turned off by setting all of its dc-bias voltages to 0 V. It is observed that, from 25 to 40 GHz, the isolation of the RF switch with the active balun off is reduced to below 32 dB, while that with the active balun on is increased and, within the frequency band around the design frequency, reaches extremely high values, approaching more than 70 dB at 36 GHz. This clearly reveals the working function of the active balun in suppressing the RF leaking signal. When the active balun is off, both the leaking RF signals through the Off-SPST and Core-SPST switches go to the RF switch's output through the parasitic capacitors of the HBTs instead of being cancelled. At 36 GHz, the proposed RF switch in its normal operation improves more than 38 dB of isolation than in the off-active-balun condition, which can be effectively considered as the minimum isolation improvement with respect to using just the (conventional) Core-SPST switch.

While the measured and simulation results of the insertion loss/gain, reverse isolation (S12), and input and output return losses are in good agreement from 10 to 40 GHz, the simulated isolation result shows more than 5-dB difference with the measured one, except in the narrow frequency range of 35.5-40 GHz. The difference in isolation is mainly due to the imbalance of the fabricated active balun, the control-signal bonding wires for the Core-SPST and Off-SPST switches, and the inaccuracy of the models for the passive elements and active devices. The imbalance of the active balun is primarily due to the circuit layout as well as the layout and fabrication of the HBTs and inductors. This imbalance makes the conditions in (3.12) and (3.13) not very well satisfied. Moreover, although the constituent switches are laid-out symmetrically on-chip, the bonding wires at their control pins connected to the gates of the CMOS transistors through small resistors of 200 Ω affect their symmetry. As the RF switch is off, the unsymmetry leads to two unequal leaking RF signals produced by the Core-SPST and Off-SPST switches. These unequal signals cannot be cancelled completely by the balun, hence reducing the isolation.

Fig. 4.13 shows the measured and calculated insertion loss and isolation of the proposed RF switch versus input power at 35 GHz using a spectrum analyzer. The measured results show that, in the on-state, the RF switch has an insertion loss from 1-2 dB and an input 1-dB compression power of -2.5 dBm. This low power compression is due to the fact that the linearity of the RF switch is primarily determined by the active balun's linearity. Either a higher-linearity active balun or a passive balun is needed to improve the switch’s linearity. On the other hand, the linearity of the RF switch in its

off-state is relatively high. The measured results show that the isolation of the RF switch varies from 51.3 to 51.85 dB for the input power from -20 to 6.5 dBm which is the maximum power available to the chip from our synthesizer. Within this input power range, the off-state 1-dB power compression does not occur. The simulated isolation does not compress until 22-dBm input power. This high power compression results since, up to 22 dBm, the balun is still operating in its linear region due to the small input power caused by the SPST switch's isolation. The measured large-signal results are consistent with those measured under small-signal conditions.

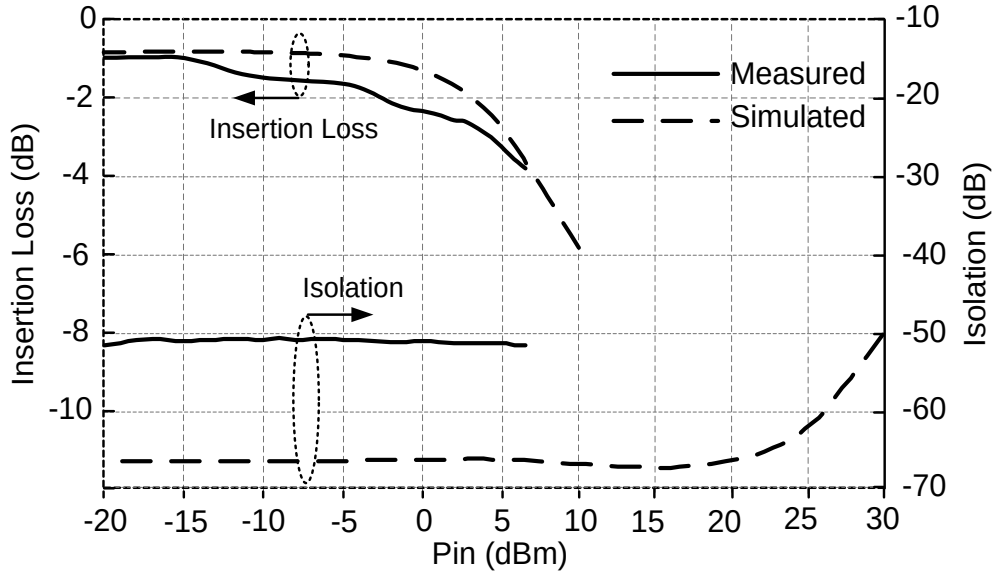


Fig. 4.13. Measured and simulated insertion loss and isolation versus input power at 35 GHz.

CHAPTER V

MILLIMETER-WAVE CONCURRENT DUAL-BAND POWER AMPLIFIER

In this chapter, a new class of concurrent dual-band impedance matching networks along with the technique for synthesizing them and a new 0.18-μm SiGe BiCMOS concurrent dual-band PA are presented. These matching networks enable simultaneous matching of two arbitrary loads to two arbitrary sources at two different frequencies, utilizing the impedance-equivalence properties of LC networks that any LC network can be equivalent to an inductor, capacitor, open or short at different frequencies. These concurrent dual-band matching networks also produce dual-bandpass filtering response with high out-of-band rejection, helping suppress the harmonics and inter-modulation products in nonlinear circuits such as power amplifiers (PAs). A new 0.18-μm SiGe BiCMOS concurrent dual-band PA was designed based on the developed dual-band matching networks around 25.5 and 37 GHz which works in the single-band mode (25.5 or 37 GHz) and dual-band mode (concurrent 25.5 and 37 GHz). This chapter begins with an overview of the power amplifier fundamentals.

5.1 Power Amplifier Fundamentals

Power amplifiers (PAs) are critical components in the transmitter front-end and are used to amplify the transmitting signal to a required power level so that the signal can be detectable at the receiver. The design of PAs involves to a multi-step process from selections of device, circuit topology, operation mode, power supply, biasing and

matching networks to circuit simulation, EM simulation, optimization, layout and measurement. Therefore, the design of PAs is very challenging and involves to a number of trials and errors. In order to provide a high power to the load, PAs typically work in the large signal conditions and consume a large DC power as well, making it the most power-hungry building block in RF transceivers. PAs are mainly characterized by maximum output power, power gain, efficiency and linearity.

5.1.1 Output Power

Fig. 5.1 shows a typical power amplifier consisting of a transistor biased using radio frequency chokes (RFC) at the collector and input, and output matching networks. The PAs will not only generate power at the frequency of interest, but also at integer multiples of the fundamental frequency. In most cases, only the power at the fundamental frequency is wanted and the harmonic power has to be filtered out or suppressed at the output. The fundamental output power on the load R_L is calculated as

$$P_{out} = \frac{1}{2}\frac{V_o^2}{R_L} \tag{5.1}$$

where V_o is the fundamental voltage delivered to the load.

The maximum output power of the PAs depends on the DC power supply voltage V_{CC} and the optimum output impedance of the transistor. The output matching network is needed to match the load with the transistor's optimum output impedance for the maximum output power on the load.

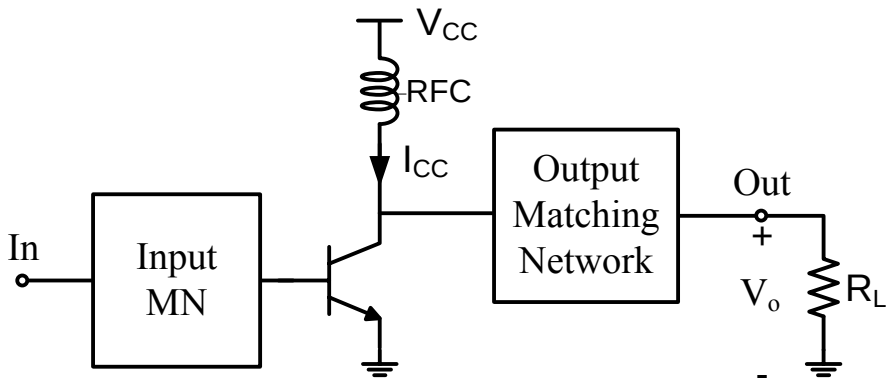


Fig. 5.1 Typical power amplifier.

5.1.2 Efficiency

There are two types of efficiencies used to characterize PAs in term of the capability of converting DC power to RF power. Efficiency, η, sometimes also called dc-to-RF efficiency, is used to measure how effectively the power from a DC supply is converted into the RF output power and is given by

$$\eta = \frac{P_{out}}{P_{DC}} \tag{5.2}$$

where P_{out} is the RF output power calculated in (5.1) and P_{DC} is the DC power of the power supply and is calculated as

$$P_{DC} = V_{CC} I_{CC} \tag{5.3}$$

where I_{CC} is the DC current component of the supply voltage. Power-added efficiency (PAE) is the efficiency of the PAs when the gain of the PA is taken into account. PAE is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} - P_{out}/G}{P_{DC}} = \eta\left(1 - \frac{1}{G}\right) \tag{5.4}$$

where P_{in} is the input power of the PA and $G = \frac{P_{out}}{P_{in}}$ is the power gain of the PA. It can be seen from (5.4) that the power gain of PAs needs to be high for maximizing PAE. High-PAE PAs are desired for battery-based applications.

5.1.3 Linearity

Linearity of the PAs is characterized by the 1-dB gain compression point and adjacent channel power ratio (ACPR). The 1-dB gain compression point indicates the power-handling capability of the PAs and is defined as the input/output power point where the nonlinearities of the PAs reduce the gain by 1 dB [51]. In addition, nonlinearity of the PAs causes the spectral regrowth or adjacent channel power problem for the modulated signal such as quadrature phase shift keying (QPSK), due to the high order inter-modulation (IMD) [52].

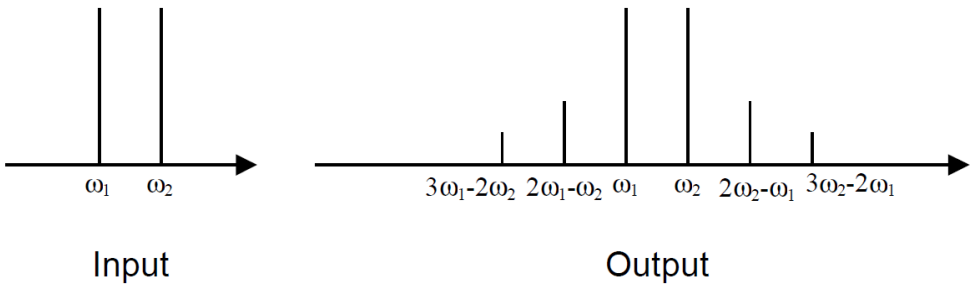


Fig. 5.2. Two tone inter-modulation product spectrum.

Fig. 5.2 shows the spectrum of the two-tone input signal and output signal of PA. Due to the nonlinearity, the IMD products appear as sidebands to the two input tones at the same frequency spacing of the two tones. Only the third and fifth order IMD products are shown in the figure. However, higher order IMD products such as the seventh or ninth order, can also be significant and appear in the spectrum for the strongly nonlinear PAs. The high order IMD products fall into the adjacent channel bandwidth and cause an unwanted spectrum as shown in Fig. 5.3. The adjacent channel power ratio (ACPR) is defined as the ratio of the measured power in an adjacent communications channel of a specified bandwidth and the power in the main channel of the same specified bandwidth, as shown in Fig.5.3. ACPR has become one of the dominant specifications for modern PAs due to the increasing use of multicarrier systems, digital modulation, as well as more densely packed communications channels [53].

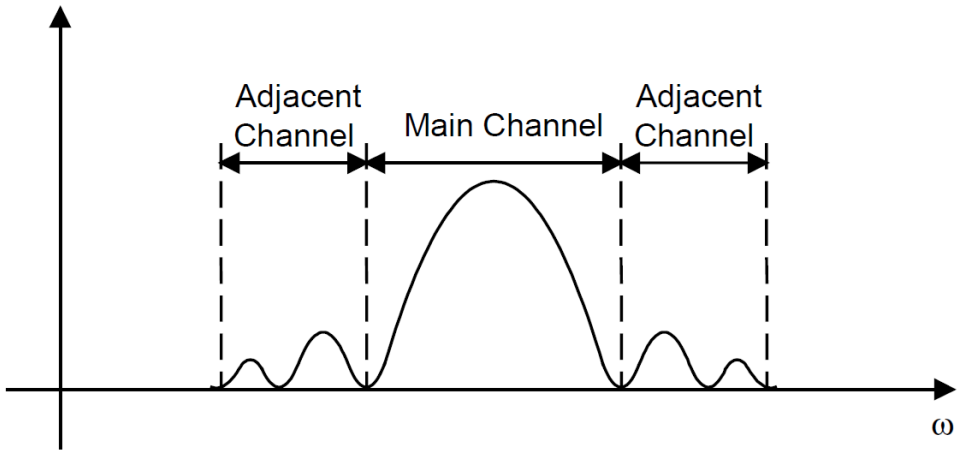


Fig. 5.3. Adjacent channel power.

In the weakly nonlinear amplifier such as the low noise amplifier, linearity is often checked using a two-tone test and characterized by the third-order intercept point IP3. However, this may not be applied for the PAs as previously discussed, the higher order in the PAs are significant. In such cases, it is needed to apply a modulated waveform and measure the spectral regrowth. In addition to gain compression and spectral regrowth, nonlinearity of the PAs may lead to AM-PM conversion corrupting the phase of the carrier.

5.1.4 Class A, B, AB and C Power Amplifiers

Power amplifiers are traditionally categorized under many classes: A, B, C, AB, D, E, F, and etc. [52]. Power amplifiers can be classified based on either the conducting angle of the transistor current, such as classes A, B, AB, and C, or the shapes of the collector/drain voltage and current controlled by the output matching network, provided that the transistor in this case operates as a switch such as classes D, E and F. In this section, the Class A, B, AB and C power amplifier are briefly reviewed**.**

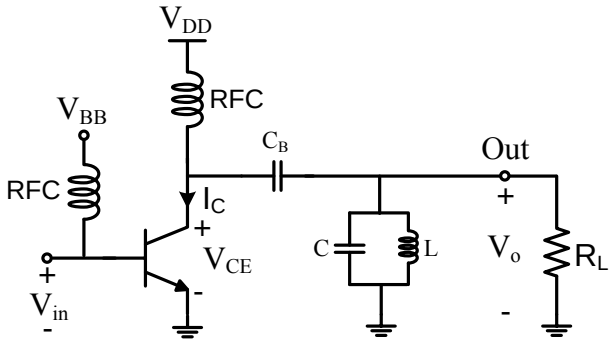
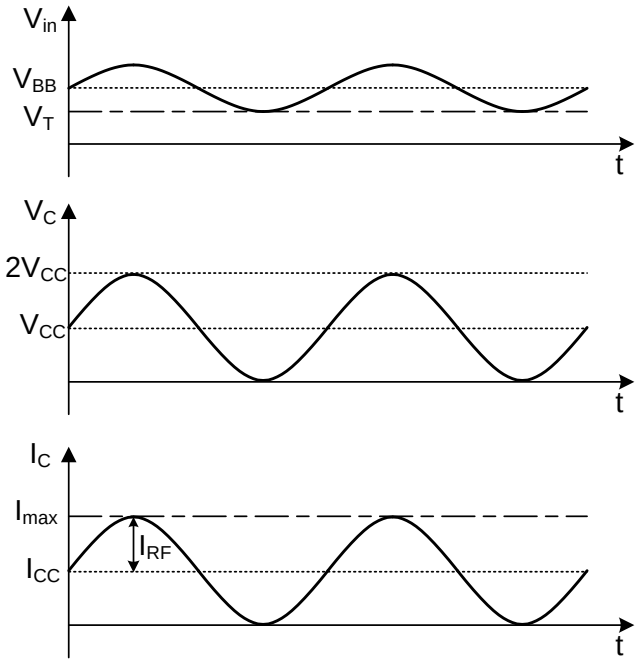
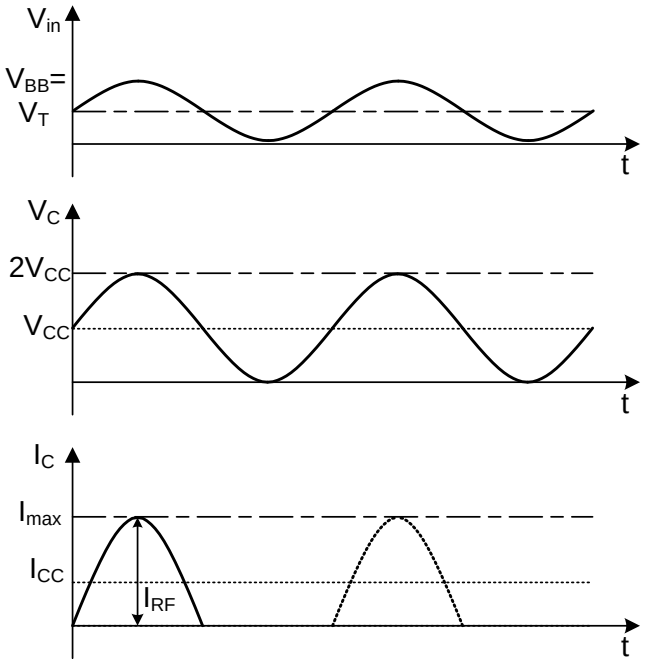


Fig. 5.4. Typical class A, B, AB and C power amplifier.

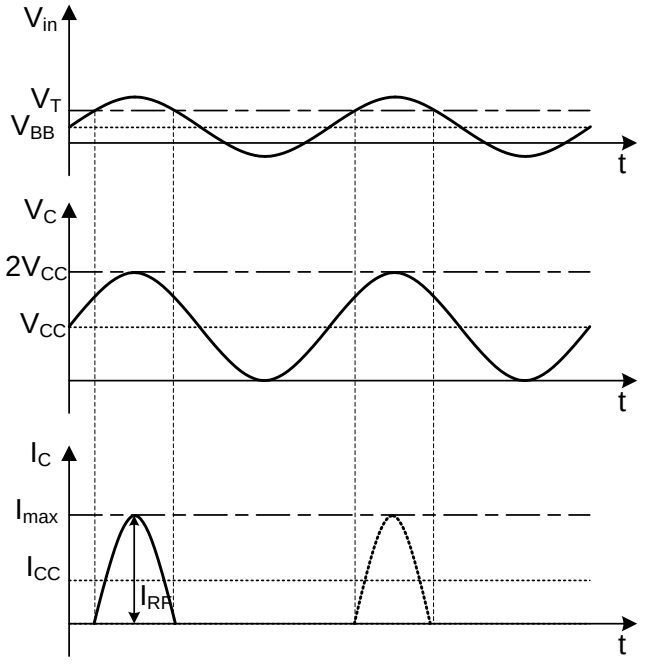
Figure 5.4 shows a typical single-ended power amplifier which can be used in class A, B, AB and C. R_L is the load which the PA delivers the output power to. Radio frequency chokes are used at the collector and base of the transistor for biasing. The large capacitor C_B is used to block the DC current to the load. The LC tank is used to keep the sinusoidal RF voltage on the load. By setting the bias voltage at the base, V_{BB}, the PA is configured to work at class A, B, AB or C.



(a)



(b)



(c)

Fig. 5.5. Waveforms of the collector current and voltage in class A (a), class B (b) and class C (c).

For the class-A power amplifiers, the operation point and input signal level are chosen so that the collector (or drain) current flows at all times. Class-A PAs, therefore, work in the linear region and minimize the signal distortion. The conduction angle of the collector current in the class-A power amplifier is 360^o. To maximum RF signal swing, the operation point of the transistor is set at the middle of the AC load line. In class-B operation, the base of the transistor is biased at the threshold voltage with $V_{BB} = V_T$, where V_T is the conduction threshold voltage of the transistor, so that the collector current flows in a half of every cycle. The conduction angle of the class-B PA is 180^o. In the class-AB, the bias point and input signal level are chosen to make the transistor to conduct the current in more than a half of every cycle. The conduction angle in the class-AB power amplifier is larger the 180^o and smaller than 360^o. In class-C PAs, the base of the transistor is biased at the voltage smaller than threshold voltage or even at a negative voltage to make the transistor to conduct the current less than a half of cycle. The conduction angle in the class-C PAs is smaller than 180^o. Fig. 5.5 shows the waveforms of the collector currents and voltages in class A, B and C.

To obtain high efficiency for the PAs, the power loss in the transistor needs to be minimized. That is, the collector current should be minimized while the voltage is high, and the voltage should be minimized while the current is high. It can be seen from Fig. 5.5 that for all waveforms, the maximum voltage is aligned with the minimum current, and the maximum current is also aligned with the minimum voltage. For class B and class C PAs, the current is zero for part of the cycle where the voltage is high, which leads to increased efficiency as compared to the class A PAs.

The analysis for class A, B and C PAs can be conducted together using the current waveform in Fig. 5.6. In this representation, the currents in class A, B and C PAs are different in the conduction angles of 2θ.

From the current wave form in Fig. 5.6, the total collector current can be expressed as

$$I_C = I_{CQ} + I_{RF}\cos\omega_0 t, \quad I_C > 0 \tag{5.5}$$

The bias current I_{CQ} is calculated from Fig. 5.6 as

$$I_{CQ} = -I_{RF}\cos\theta \tag{5.6}$$

where 2θ is the conduction angle.

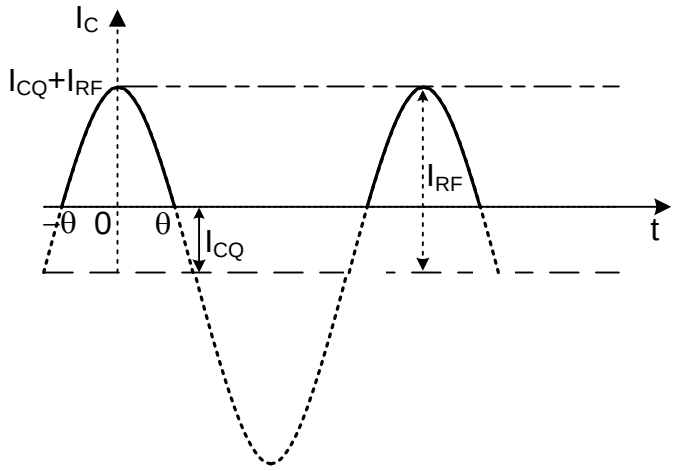


Fig. 5.6. Current waveform in the analysis of class A, B, and C PAs.

The average collector current is calculated as

$$I_{CC} = \frac{1}{2\pi}\int_{-\theta}^{\theta}(I_{CQ} + I_{RF}\cos\theta)d\theta = \frac{I_{RF}}{\pi}\left[\sin\theta - \theta\cos\theta\right] \tag{5.7}$$

The fundamental component of collector current is calculated as

$$I_{CM} = \frac{2}{T}\int_{0}^{T} I_C \cos\omega_0 t \, dt = \frac{2}{T}\int_{0}^{T}(I_{CQ} + I_{RF}\cos\omega_0 t)\cos\omega_0 t \, dt$$

$$I_{CM} = \frac{1}{2\pi}\left(4I_{CQ}\sin\theta + 2I_{RF}\theta + I_{RF}\sin 2\theta\right) \tag{5.8}$$

Making use of (5.6), the fundamental component of collector current becomes

$$I_{CM} = \frac{I_{RF}}{2\pi}\left(2\theta - \sin 2\theta\right) \tag{5.9}$$

Since the maximum voltage of the fundamental component on the load equals to V_{CC}, we have

$$V_{CC} = R_L I_{CM} = R_L \frac{I_{RF}}{2\pi}\left(2\theta - \sin 2\theta\right) \tag{5.10}$$

The I_{RF} is then calculated in term of V_{CC} as

$$I_{RF} = \frac{2\pi V_{CC}}{R_L\left(2\theta - \sin 2\theta\right)} \tag{5.11}$$

The maximum collector current, I_{Cmax} is the sum of the bias current I_{CQ} and I_{RF} as

$$I_{Cmax} = \frac{I_{RF}}{\pi}\left[\sin\theta - \theta\cos\theta\right] + \frac{2\pi V_{CC}}{R_L\left(2\theta - \sin 2\theta\right)}$$

$$I_{Cmax} = \frac{2\pi V_{CC}}{R_L\left(2\theta - \sin 2\theta\right)}\left[1 + \frac{\sin\theta - \theta\cos\theta}{\pi}\right] \tag{5.12}$$

The maximum output power is calculated as

$$P_{L\max} = \frac{1}{2}\frac{V_{CC}^2}{R_L} \tag{5.13}$$

Making use (5.7) and (5.11), the maximum average current is obtained as

$$I_{CC\max} = \frac{2V_{CC}\left[\sin\theta - \theta\cos\theta\right]}{R_L\left(2\theta - \sin 2\theta\right)} \tag{5.14}$$

Making use (6.13) and (6.14), the maximum efficiency is calculated as

$$\eta_{\max} = \frac{P_{L\max}}{V_{CC}I_{CC\max}} = \frac{2\theta - \sin 2\theta}{4\left(\sin\theta - \theta\cos\theta\right)} \tag{5.15}$$

Fig. 5.7 shows the maximum efficiency versus conduction angle plotted form (5.15).

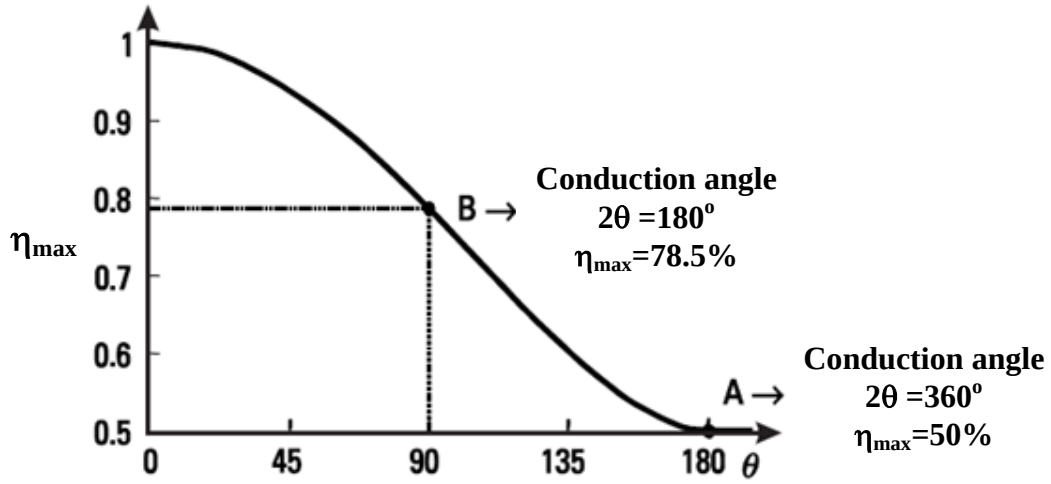


Fig. 5.7. Maximum efficiency versus conduction angle.

Applying values of conduction angles for each class of PAs, the maximum efficiency performance of PAs are characterized. The maximum efficiency of class A and B are 50% and 78.5% respectively. It can be inferred that the class AB PAs provide

the maximum efficiency between 50% and 78.5%. The efficiency of class C PAs can be higher than 78.5% and reaches 100%.

The main advantage of the class A PA is its high linearity due to the current conduction of 100% of the time, but good linearity can also be achieved with class AB and B or if the power is backed off; hence sacrificing the efficiency. The class A, B, and AB PAs are used for low-power applications, where the efficiency is less important, or in applications requiring high linearity, for example, in CDMA systems, where the modulated signals have variable amplitudes. With the same power supply voltage conditions, the maximum fundamental RF output powers of PAs are approximately equal in classes A, AB, and B. However, class B has a theoretical maximum efficiency of 78.5%, while class A has a theoretical maximum efficiency of 50%. It should be noted that practical efficiencies are much lower in fully integrated power amplifiers due to a number of non-idealities such as finite inductor quality factor, substrate loss, and saturation voltage in the transistors. Efficiencies of half of the theoretical maximum values can be considered very well, especially in a low-voltage process and high frequencies [54].

Class C PAs have theoretical maximum efficiencies higher than the class B, approaching 100% as the conduction angle decreases. However, this increase in efficiency results in a decrease in the output power. The output power approaches zero as the efficiency approaches 100%. Because of the difficulty of obtaining low conduction angles on an integrated circuit while sustaining the required power level, completely integrated class C power amplifiers are not very widely used [18].

5.2 Motivation

Advanced communication and radar systems working "concurrently" over multiple bands provide numerous advantages and have more capabilities as compared to their single-band counterparts for communications and sensing - a fact that is simple to understand since the communication and sensing are performed at multiple frequencies simultaneously. The ability of operating multiple bands simultaneously increases the diversity of transmitters and receivers and hence systems for simultaneous communications or sensing at multiple frequencies – especially needed when operating in environments with severe multi-path fading, such as indoors, urban settings or mountainous terrains, or when signal attenuation at some frequencies are excessively high, which hinder the communication and sensing capabilities. Achieving concurrent functions over multiband enables one single system to be used at multi-band simultaneously, leading to optimum size, cost and power consumption, and ease in realization for the system. True concurrent multiband systems require many components to work concurrently in multiple bands. Concurrent multiband power amplifiers (PAs) are one of them. It is noted that both single- and multi-mode operation occur in concurrent multiband components. Single-mode operation occurs when there exists only signals in one band, while multimode operation happens when signals in multiple bands occur at the same time. Multi-mode operation is especially important for concurrent multiband components since it characterizes truly the performance of these components.

Concurrent multiband PAs can be implemented using wideband PAs covering both desired and undesired frequency ranges in the multiband (i.e., all-pass). This

approach, however, does not produce optimum performance for the PAs in multiband concurrently since the optimum load of the PAs is inherently frequency-dependent. Moreover, wideband PAs generate more harmonics and inter-modulation products (IMP), hence reducing the PAs' performance and increasing interference with other RF systems. Furthermore, wideband PAs produce (unwanted) RF radiation in non-interested bands, leading to RF environment pollution and less stealthy operations. Therefore, using wideband PAs for concurrent multiband applications is generally undesirable.

Concurrent multiband PAs, that work "only" within the desired bandwidths in multiband (i.e., in multiple band-pass windows) is attractive. One of the important design criteria for such concurrent multiband PAs, like other concurrent multiband components, is their ability to exhibit concurrent multiband matching. Concurrent multiband matching may be achieved by implementing a filter function separately or internally within a matching network. Combing matching and filtering in a single matching network is attractive as it would result in a simple architecture, yet is also very challenging. In the following, we will provide a brief review of multiband PAs and corresponding multiband matching.

Various approaches have been implemented for multiband PAs operating up to 8 GHz [55]-[59]. In [55] and [56], a quad- and dual-band PA module is formed by combining four and two individual single-band PAs in parallel, respectively. Each individual PA is optimized for a narrow band and, in operation, is selected by switching on the corresponding power supply. This approach, although giving optimum performance in each band, results in large circuit size and hence increased cost whereas,

more importantly, can only produce operation in one band at each time (i.e., essentially, single-mode), and is thus not suitable for concurrent multiband operation (i.e., multimode). In [57]-[59], multiband PAs are implemented through reconfiguration of the components in the matching networks. In this approach, the same active devices are used for all bands, while the matching networks are adaptive with the operating bands by reconfiguring the passive components using RF switches or varactors. This approach significantly reduces the number of active devices, hence the amplifier area and cost, while maintaining optimum performance at all bands. It, however, results in increased circuit complexity due to the use of additional control circuits. Additionally, these multiband PAs can only be operated in a single band at each time instead of in a concurrent multiband.

Several PAs working to 5.2 GHz using concurrent multiband matching networks were reported in [60]-[63]. The performance of these multiband PAs is very much related to the technique used in the design of the matching networks. The dual-band PA in [60] uses a dual-band matching network consisting of two parallel lumped-element resonators on two parallel paths, each blocking the signal at one frequency. L-type dual-band matching networks consisting of series- and shunt-LC circuits are used in [61]. Dual-band PAs with dual-band matching networks, including harmonic-tuning circuits, using both lump elements and transmission lines are presented in [62], [63]. The concept of the impedance buffer developed in [62] allows implementation of the multiband harmonic termination by matching the device output with purely imaginary impedances, resulting in improved performance.

Dual-band matching techniques using transmission lines were reported in [64], [65]. These impedance-matching approaches, although are interesting for the design of dual-band components, may not be very suitable for CMOS/BiCMOS implementations since they result in large circuit size and hence cost.

Advanced SiGe HBTs possess RF performance comparable to III-V compound based HBTs, while having the advantage of compatibility with standard CMOS technologies which results in increased integration capability and low cost [66]. Many SiGe HBT PAs have been designed at K and Ka bands [67]-[70]. All of them, however, are single- or broad-band PAs. There has been no concurrent dual-band PA at K/Ka band using SiGe HBT reported.

The main objective of this chapter is two-fold. First, it presents a new class of concurrent dual-band impedance-matching networks and their design equations and methodology. These dual-band matching networks, while suitable for both lumped elements and transmission lines, are specifically formulated using lumped elements for possible on-chip implementations for miniature RFICs, particularly on CMOS/BiCMOS processes. They are synthesized from two single-band matching networks, enabling the matching of two arbitrary loads to two arbitrary source impedances at two arbitrary frequencies concurrently. Specifically, the dual-band matching networks are synthesized utilizing LC networks, each behaving as an inductor, capacitor, open, or short at different frequencies, to create proper matching and filtering functions, and hence are named “synthetic concurrent dual-band matching networks.”

Second, the chapter reports a new dual-band PA working concurrently at 25.5 and 37 GHz designed using the developed concurrent dual-band matching technique. Important design issues for concurrent dual-band PAs and detailed design of the 25.5/37 GHz PA are presented. The designed dual-band PA exhibits measured gains of 21.4 and 17 dB at 25.5 and 37 GHz, respectively, in both single- and concurrent dual-band modes. It also has maximum measured output powers of 16/13 dBm and 13/9.5 dBm at 25.5/37 GHz in the single- and concurrent dual-band mode, respectively. The PA has a chip size of 1.3×0.68 mm^2 and consumes a dc current of 120 mA from a 3-V source.

5.3 Challenges of Concurrent Dual-band PA Design at MMW

The design of power amplifiers at microwave/millimeter-wave frequencies presents significant challenges. Firstly, the low unity power gain frequency, f_{max}, and low breakdown voltage of the transistors make it difficult to achieve PAs with high gain, high efficiency and high output power. The cascode topology has been preferred than single transistor due to good input-output isolation and increase of power supply voltage used; hence the output power [71]. Recently, distributed active transformer has been used as a power combiner to increase the output power [72]-[73], but the efficiency is quite low.

The second issue is the loss of on-chip passive components, such as inductors and transmission lines, required for impedance matching, and low resistivity substrate which presents another barrier to full integration of a high-frequency power amplifier. Skin effect results in larger losses in inductors and transmission lines at high

frequencies. For instance, at 24GHz, the skin depth in aluminum is 0.5μm, which negates some of the advantages of a thick top metal layer. Some techniques, such as shields for inductors and transmission lines, and using shielded coplanar waveguides rather than micro strip lines, have been used to reduce these kinds of losses [73]-[75].

Another issue hampering advances in circuit design at mm-wave range, especially in silicon technologies, is the lack of accurate device modeling at such frequencies. Compared to lower frequencies where many parasitic elements and transmission line effects do not play a significant role, at millimeter-wave frequencies such effects become more dominant, and then accurate modeling becomes crucial. To address this issue, some works have been done to improve mm-wave frequency device models [76].

Design of high power amplifier at MMW using low breakdown voltage devices may require the passive power combiner and high transformation ratio impedance matching. The passive power combiner using the wide metal to comply the current density of the used technology reduces the performance of the PA due to the introduction of more parasitic capacitor and loss. Since the inherent output device impedance in high power amplifier is very low, impedance matching becomes very difficult, requiring higher impedance transformation ratios; hence lower the power transform efficiency.

The design of a concurrent dual-band PA introduces additional challenges as compared to that of a single-band PA. Fig. 5.8 shows the building blocks with their essential functions of a concurrent dual-band PA. Dual-band inter-stage matching

networks are also needed for multi-stage dual-band PAs. The active-device block may consist of one or several transistors.

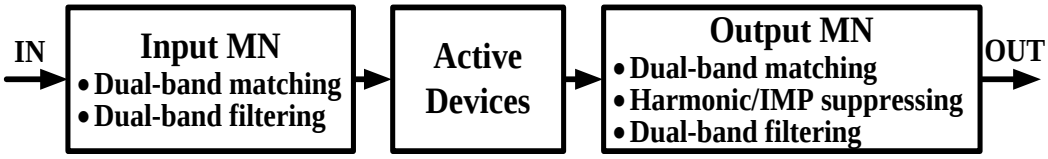


Fig. 5.8. Main blocks of a concurrent dual-band PA.

The design of the input and output matching networks of a concurrent dual-band PA is much more challenging than that of a single-band PA. In a single-band PA, the input and output matching networks provide matching only at one fundamental frequency to attain highest possible performance such as maximum output power or power-added efficiency. In addition, the single-band output matching network also needs to include harmonic control circuits to improve the PA performance [77]. In a concurrent dual-band PA, the PA is operated under dual-mode and is subjected to two-tone large-signal conditions. The active devices thus generate many more unwanted harmonics and IMPs than a single-band PA, which need to be suppressed for achieving good PA performance and avoiding harm to other components and systems. To illustrate this possible complex spectrum, Fig. 5.9 shows the output spectrum of a wideband PA simultaneously fed with two tones at 25.5 and 37 GHz. It is observed that, besides the two fundamental tones, there are many harmonics and IMPs generated due to the inherent nonlinearity of the active devices. While the harmonics of the two tones are

located at their upper side, the IMPs are distributed below, between and above the two fundamental frequencies. To achieve the best possible performance for a concurrent dual-band PA, the output matching network is required to not only match the 50-Ω load to optimum output impedances at two different fundamental frequencies, but also suppresses the harmonics and IMPs. It is apparent that suppressing the IMPs located very close to the two main tones is rather challenging, as this requires very high-Q networks which are difficult to achieve at millimeter-wave frequencies. Like the output matching network, the input matching network is required to simultaneously match the source with optimum input impedances at two different frequencies. The inter-stage matching networks, needed in multi-stage PAs, are required to match two different input impedances of the next stage to two different optimum output impedances of the previous stage at two different frequencies as well as suppress unwanted harmonics and/or IMPs generated from the previous stage. In addition to concurrently matching in dual-band, all the input, inter-stage and output matching networks should have dual-band filtering response to reduce the interferences generated by the PA to the existing components and systems, and reject the out-of-band signals possibly injecting into the PA and desensitizing the two main tones.

Techniques for impedance matching at one frequency, such as that described in [51], is relatively straightforward and widely used. However, simultaneously matching two arbitrary loads to two arbitrary source impedances at two different frequencies using lumped components required for concurrent dual-band matching networks, along with

the suppression of harmonics and IMPs needed for nonlinear components such as dual-band PAs, is still a challenging issue. This is addressed in the subsequent parts.

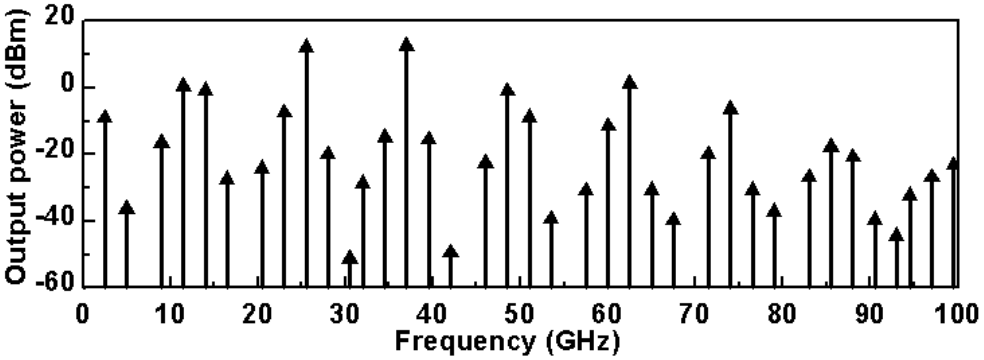


Fig. 5.9. Output spectrum of a wideband PA with two input tones at 25.5 and 37 GHz.

5.4 Synthetic Concurrent Dual-band Impedance-Matching Networks

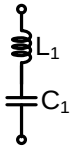
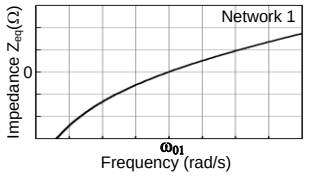
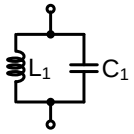
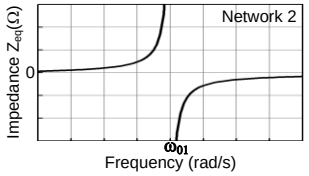
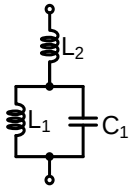
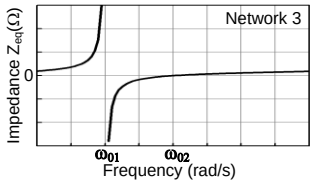
Concurrent dual-band impedance-matching networks are required to match two different impedances (herein referred to as load impedances) to two other different impedances (referred to as source impedances) at two different frequencies. A matching network is typically used to provide matching at a single band which is implemented in conventional single-band designs. We can infer that, in theory, in order to provide concurrent matching over dual-band (or in general multi-band), two single-band (or multiple single-band) matching networks would be needed. Using two separate matching networks to achieve dual-band matching, however, is not effective. A logical question is then: can a single network be synthesized from two different single-band matching networks to achieve concurrent matching at two different bands? To answer this question, we first consider general single-band lumped-element matching networks

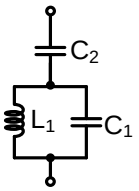
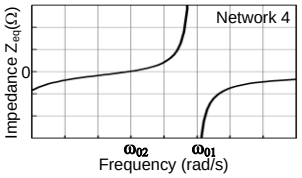
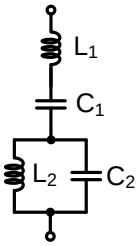
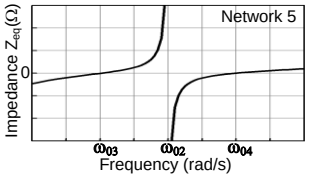
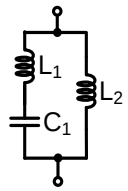
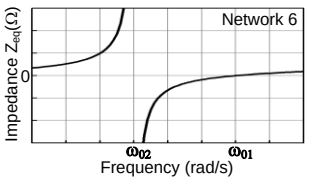
consisting of inductors and capacitors. Second, we recognize that any LC network can be equivalent to an inductor, capacitor, open, or short at different frequencies. This leads to the possibility that a LC network can be used to realize inductor, capacitor, open or short at different frequencies simultaneously. We can then conclude that it is possible to combine two separate single-band matching networks at two different frequencies into a single network that provides concurrent matching at these frequencies. Our proposed dual-band matching networks are derived based on this basic idea. It is particularly noted that the short- and open-circuited characteristics at certain frequencies of the LC networks used in the dual-band matching also result in the suppression of harmonics and/or IMPs, which are useful for the design of nonlinear components such as PA.

The key of our proposed concurrent dual-band matching design is based on LC networks that can function as an inductor, capacitor, open or short at different frequencies simultaneously. Table 5.1 shows the derived LC networks together with their impedance/admittance expressions, characteristics, and impedance plots, where L_{eq}, C_{eq}, Z_{eq}, and Y_{eq} are the equivalent inductance, capacitance, impedance, and admittance of the networks, respectively, and ω_{0i} (i=1, 2, …, 4) are the frequencies at which the networks become a short or open. More complicated networks and their characteristics can easily be developed from those in Table 5.1. Network 1 and 2 are the same as those used in [61]. Any network in Table 5.1 can be used to exhibit not only its equivalent inductance or capacitance at certain frequencies for the design of concurrent dual-band matching networks, but also open and/or short at other frequencies for signal suppression. For instance, Network 6 behaves as an inductor at $\omega < \omega_{02}$ or $\omega > \omega_{01}$, a

capacitor at $\omega_{02} < \omega < \omega_{01}$, open at $\omega = \omega_{02}$, and short at $\omega = \omega_{01}$. When used in shunt, Network 6 suppresses signals at $\omega = \omega_{01}$, whereas it blocks signals at $\omega = \omega_{02}$ when connected in series.

Table 5.1 LC networks and their impedances/admittances, characteristics and impedance plots

LC Network	Impedance/ Admittance	Characteristic	Impedance plot
Network 1 	$Z_{eq}=j(\omega L_1-\frac{1}{\omega C_1})$ $=\frac{j(\omega^2-\omega_{01}^2)}{\omega\omega_{01}^2 C_1}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$	$Z_{eq}=0$ at $\omega=\omega_{01}$ $L_{eq}=\frac{\omega^2-\omega_{01}^2}{\omega^2\omega_{01}^2 C_1}$ at $\omega>\omega_{01}$ $C_{eq}=\frac{\omega_{01}^2 C_1}{\omega_{01}^2-\omega^2}$ at $\omega<\omega_{01}$	
Network 2 	$Z_{eq}=\frac{j\omega\omega_{01}^2 L_1}{(\omega_{01}^2-\omega^2)}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$	$Z_{eq}=\infty$ at $\omega=\omega_{01}$ $L_{eq}=\frac{\omega_{01}^2 L_1}{\omega_{01}^2-\omega^2}$ at $\omega<\omega_{01}$ $C_{eq}=\frac{\omega^2-\omega_{01}^2}{\omega^2\omega_{01}^2 L_1}$ at $\omega>\omega_{01}$	
Network 3 	$Z_{eq}=j\omega L_2+\frac{j\omega\omega_{01}^2 L_1}{(\omega_{01}^2-\omega^2)}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$ $\omega_{02}=\omega_{01}\sqrt{\frac{L_1+L_2}{L_2}}$	$Z_{eq}=\infty$ at $\omega=\omega_{01}$ $Z_{eq}=0$ at $\omega=\omega_{02}$ $L_{eq}=L_2+\frac{\omega_{01}^2 L_1}{\omega_{01}^2-\omega^2}$ at $\omega<\omega_{01}$ or $\omega>\omega_{02}$ $C_{eq}=\left(-\omega^2 L_2+\frac{\omega^2\omega_{01}^2 L_1}{\omega^2-\omega_{01}^2}\right)^{-1}$ at $\omega_{01}<\omega<\omega_{02}$	

Network 4 	$Z_{eq}=\frac{1}{j\omega C_2}+\frac{j\omega\omega_{01}^2 L_1}{\omega_{01}^2-\omega^2}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$ $\omega_{02}=\omega_{01}\sqrt{\frac{C_2}{C_1+C_2}}$	$Z_{eq}=\infty$ at $\omega=\omega_{01}$ $Z_{eq}=0$ at $\omega=\omega_{02}$ $L_{eq}=\frac{-1}{\omega^2 C_2}+\frac{\omega_{01}^2 L_1}{\omega_{01}^2-\omega^2}$ at $\omega_{02}<\omega<\omega_{01}$ $C_{eq}=\left(\frac{1}{C_2}+\frac{\omega^2\omega_{01}^2 L_1}{\omega^2-\omega_{01}^2}\right)^{-1}$ at $\omega<\omega_{02}$ or $\omega>\omega_{01}$	
Network 5 	$Z_{eq}=\frac{j(\omega^2-\omega_{01}^2)}{\omega\omega_{01}^2 C_1}+\frac{j\omega\omega_{02}^2 L_2}{\omega_{02}^2-\omega^2}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$, $\omega_{02}=\frac{1}{\sqrt{L_2C_2}}$ $\omega_{03}=\sqrt{B-\frac{\sqrt{B^2-4C}}{2}}$ $\omega_{04}=\sqrt{B+\frac{\sqrt{B^2-4C}}{2}}$ $B=\omega_{01}^2+\omega_{02}^2+\omega_{01}^2\omega_{02}^2 L_2C_1$ $C=\omega_{01}^2\omega_{02}^2$	$Z_{eq}=\infty$ at $\omega=\omega_{02}$ $Z_{eq}=0$ at $\omega=\omega_{03}, \omega_{04}$ $L_{eq}=\frac{\omega^2-\omega_{01}^2}{\omega^2\omega_{01}^2 C_1}+\frac{\omega_{02}^2 L_2}{\omega_{02}^2-\omega^2}$ at $\omega_{03}<\omega<\omega_{02}$ or $\omega>\omega_{04}$ $C_{eq}=\left(\frac{\omega_{01}^2-\omega^2}{\omega_{01}^2 C_1}+\frac{\omega^2\omega_{02}^2 L_2}{\omega^2-\omega_{02}^2}\right)^{-1}$ at $\omega<\omega_{03}$ or $\omega_{02}<\omega<\omega_{04}$	
Network 6 	$Y_{eq}=\frac{j\omega\omega_{01}^2 C_1}{\omega_{01}^2-\omega^2}+\frac{1}{j\omega L_2}$ $Z_{eq}=\left(Y_{eq}\right)^{-1}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$ $\omega_{02}=\omega_{01}\sqrt{\frac{L_1}{L_1+L_2}}$	$Z_{eq}=0$ at $\omega=\omega_{01}$ $Z_{eq}=\infty$ at $\omega=\omega_{02}$ $L_{eq}=\left(\frac{\omega^2\omega_{01}^2 C_1}{\omega^2-\omega_{01}^2}+\frac{1}{L_2}\right)^{-1}$ at $\omega<\omega_{02}$ or $\omega>\omega_{01}$ $C_{eq}=\frac{\omega_{01}^2 C_1}{\omega_{01}^2-\omega^2}-\frac{1}{\omega^2 L_2}$ at $\omega_{02}<\omega<\omega_{01}$	

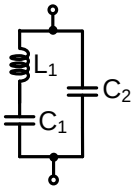
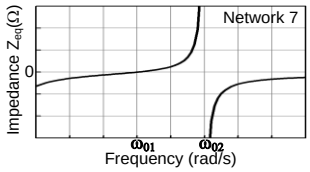
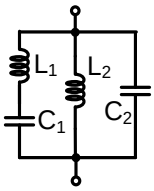
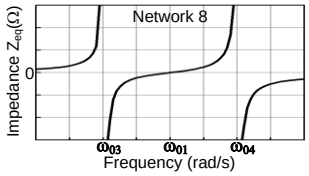
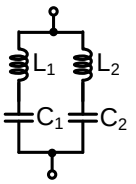
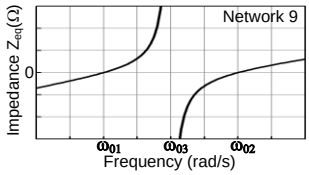
Network 7 	$Y_{eq}=\frac{j\omega\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+j\omega C_2$ $Z_{eq}=\left(Y_{eq}\right)^{-1}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$ $\omega_{02}=\omega_{01}\sqrt{\frac{C_1+C_2}{C_2}}$	$Z_{eq}=0$ at $\omega=\omega_{01}$ $Z_{eq}=\infty$ at $\omega=\omega_{02}$ $L_{eq}=\left(\frac{\omega^2\omega_{01}^2C_1}{\omega^2-\omega_{01}^2}-\omega^2C_2\right)^{-1}$ at $\omega_{01}<\omega<\omega_{02}$ $C_{eq}=\frac{\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+C_2$ at $\omega<\omega_{01}$ or $\omega>\omega_{02}$	
Network 8 	$Y_{eq}=\frac{j\omega\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+\frac{\omega_{02}^2-\omega^2}{j\omega\omega_{02}^2L_2}$ $Z_{eq}=\left(Y_{eq}\right)^{-1}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$, $\omega_{02}=\frac{1}{\sqrt{L_2C_2}}$ $\omega_{03}=\sqrt{B-\frac{\sqrt{B^2-4C}}{2}}$ $\omega_{04}=\sqrt{B+\frac{\sqrt{B^2-4C}}{2}}$ $B=\omega_{01}^2+\omega_{02}^2+\omega_{01}^2\omega_{02}^2L_2C_1$ $C=\omega_{01}^2\omega_{02}^2$	$Z_{eq}=0$ at $\omega=\omega_{01}$ $Z_{eq}=\infty$ at $\omega=\omega_{03}$, ω_{04} $L_{eq}=\left(\frac{\omega^2\omega_{01}^2C_1}{\omega^2-\omega_{01}^2}+\frac{\omega^2-\omega_{02}^2}{\omega_{02}^2L_2}\right)^{-1}$ at $\omega<\omega_{03}$ or $\omega_{01}<\omega<\omega_{04}$ $C_{eq}=\frac{\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+\frac{\omega^2-\omega_{02}^2}{\omega^2\omega_{02}^2L_2}$ at $\omega_{03}<\omega<\omega_{01}$ or $\omega>\omega_{04}$	
Network 9 	$Y_{eq}=\frac{j\omega\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+\frac{j\omega\omega_{02}^2C_2}{\omega_{02}^2-\omega^2}$ $Z_{eq}=\left(Y_{eq}\right)^{-1}$ $\omega_{01}=\frac{1}{\sqrt{L_1C_1}}$, $\omega_{02}=\frac{1}{\sqrt{L_2C_2}}$ $\omega_{03}=\omega_{01}\omega_{02}\sqrt{\frac{C_1+C_2}{\omega_{01}^2C_1+\omega_{02}^2C_2}}$	$Z_{eq}=0$ at $\omega=\omega_{01}$, ω_{02} $Z_{eq}=\infty$ at $\omega=\omega_{03}$ $L_{eq}=\left(\frac{\omega^2\omega_{01}^2C_1}{\omega^2-\omega_{01}^2}+\frac{\omega^2\omega_{02}^2C_2}{\omega^2-\omega_{02}^2}\right)^{-1}$ at $\omega_{01}<\omega<\omega_{03}$ or $\omega>\omega_{02}$ $C_{eq}=\frac{\omega_{01}^2C_1}{\omega_{01}^2-\omega^2}+\frac{\omega_{02}^2C_2}{\omega_{02}^2-\omega^2}$ at $\omega<\omega_{01}$ or $\omega_{03}<\omega<\omega_{02}$	

Fig. 5.10 illustrates the design process for a concurrent dual-band matching network to simultaneously transfer Z_{L1} to Z_{S1} and Z_{L2} to Z_{S2} at f_1 and f_2 ($f_1 < f_2$),

respectively. It consists of three steps. First, two separate single-band lumped-element matching networks transforming Z_{L1} to Z_{S1} at f_1 and Z_{L2} to Z_{S2} at f_2 are designed using a suitable matching technique (e.g., [51]) as shown in Figs. 5.10(a) and (b). In each branch of the single-band matching networks, there is at most one inductor or one capacitor having impedance/admittance of Z_{i1}/Y_{i1} at f_1 and Z_{i2}/Y_{i2} at f_2, (i=1, 2, 3). The two single-band matching networks can be of any type, such as L-type or Pi-type, and the number of elements in each matching network does not need to be the same.

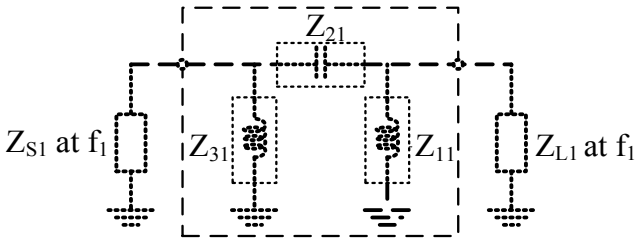
Second, a dual-band matching network is synthesized from the two designed single-band matching networks. This is done by replacing every two corresponding branches of the two single-band matching networks with an appropriate LC network from Table 5.1 having its equivalent impedance of $Z_{eq,i}$ satisfying

$$Z_{eq,i} = Z_{i1} \qquad \text{at } f = f_1 \tag{5.16}$$

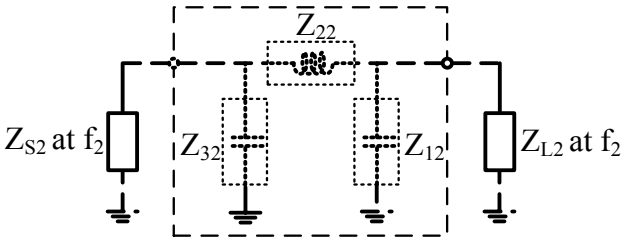
$$Z_{eq,i} = Z_{i2} \qquad \text{at } f = f_2 \tag{5.17}$$

as shown in Fig. 5.10(c). The dual-band matching network is electrically equivalent to the two single-band matching networks working simultaneously at two frequencies f_1 and f_2. It is noted that admittances $Y_{eq,i}$, Y_{i1} and Y_{i2} can also be used in lieu of impedances.

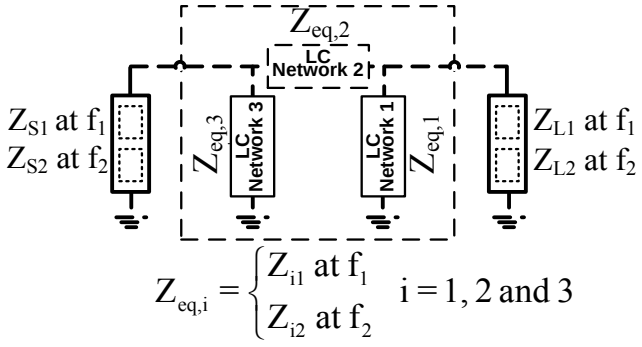
Third, the two equations resulting from conditions (5.16) and (5.17) are solved for each LC network to determine L's and C's. It is noted that the two conditions in (5.16) and (5.17) are only sufficient for two-element LC networks such as Network 1 and 2 used in Fig. 5.10(c).



(a)



(b)



(c)

Fig. 5.10. Single-band matching network at f_1 (a) and f_2 (b), and synthetic dual-band matching network (c).

For LC networks having more than two elements such as Network 3, other conditions need to be used – for instance, the harmonic/IMP suppression condition, in which the LC network becomes an open or short at the harmonic/IMP frequency, that is used for the design of the dual-band PA in Section 5.5. It is noted that Network 3 having three elements is used here to signify the versatility and generality of the proposed dual-

band matching technique. Conditions (5.16) and (5.17), and other possible conditions, produce a simple set of two-variable linear equations which are easy to be solved. It is noted that, for certain cases, real values for L and C may not be obtained and, in these cases, other conditions or even other LC networks need to be used instead. By properly choosing LC networks, a resultant synthetic concurrent dual-band matching network can exhibit not only perfect dual-band matching, but also dual-band filtering and harmonic/IMP suppression. It is noted a similar formulation can be used to derive dual-band matching networks consisting of only transmission lines or combined lumped elements and transmission lines. Detailed implementation of the proposed dual-band matching technique for the design of the output, inter-stage and input dual-band matching networks of the 25.5/37-GHz dual-band PA is described in Section 5.5.

5.5 K/Ka-band Concurrent Dual-band Power Amplifier Design

The 25.5/37-GHz concurrent dual-band PA was designed and fabricated using Jazz 0.18-μm SiGe BiCMOS process [21]. The SiGe HBT transistors used for the PA have break-down voltages BV_{CEO} = 1.9 V and BV_{CBO} = 5.8 V. The topmost metal layer is used for the inductors, AC ground, and interconnects. All the on-chip inductors, interconnects, vias and AC ground were designed and simulated using the EM simulator IE3D [22]. The PA was simulated, optimized and laid-out using Cadence [23]. All combining networks connecting HTBs' base, emitter and collector terminals were carefully simulated using IE3D before running the load-pull simulation.

5.5.1 PA Circuit, Device and Bias

Fig. 5.11 shows the schematic of the designed 25.5/37-GHz concurrent dual-band PA that consists of two cascode stages and three dual-band matching networks including input, inter-stage and output matching networks. The dual-band PA is biased to work in the class-AB mode. The cascode PA topology allows the transistor to operate at a voltage higher than the breakout voltage and provides maximizing gain and output power simultaneously [70], [78]. In the cascode pairs, the common-emitter transistors determine the gain for the PA while the common-base transistors with possibly high power supply voltage enable high RF output power [78]. In addition, the cascode structure provides high reverse isolation between the input and output, hence increasing the stability for the PA at high frequencies.

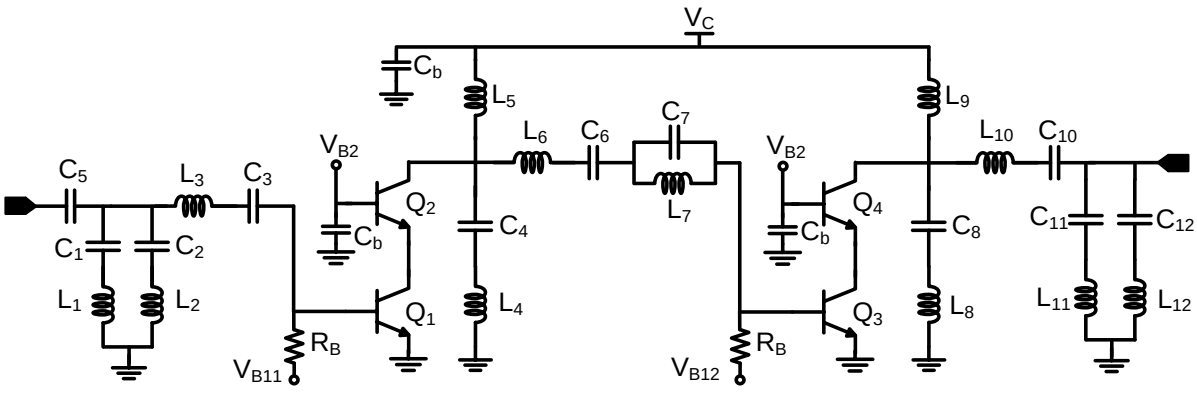


Fig. 5.11. Schematic of the 25.5/37-GHz concurrent dual-band power amplifier.

High-performance SiGe transistors used in this design suffer problem of low breakdown voltage of B_{VCEO} = 1.9V. It has been shown that the common-emitter

transistor with small base resistor can work at the collector-emitter voltage much higher than the base-open breakdown voltage BV_{CEO} [78], [79]. So the bases of transistors Q_1 and Q_3 are biased through resistors of 300 Ω to allow them to work at increased voltage swing. The base voltage of Q_2 and Q_4 are set at 1.8 V to keep transistors Q_1 and Q_3 working in the forward-active region and minimize the knee voltage for the cascode pair, hence maximizing the dynamic output voltage swing [79]. The bias voltage at the collectors of transistors Q_2 and Q_4 is of more concern for high-power cascode PAs. It needs to be high for high RF output power, but must be within a constraint to keep these transistors away from breakdown. The experimental study in [79] recommends that the maximum collector bias voltage V_C for maximizing the power performance and dynamic safe-operation area for cascode PAs to be lower than $1/2(BV_{CBO} + V_{B\_Q2} + V_{knee})$, which is 4.3 V for the SiGe HBT used in the designed dual-band PA, where V_{knee} is around 1V obtained from the simulated DC characteristic of the cascode pair. This ensures that the PA will undergo a gain compression before breakdown. The designed dual-band PA is biased at collector voltage V_C of 3 V.

Increased RF output power can be achieved by connecting many SiGe HBTs in parallel, necessitating the use of wide metal trips for interconnects and inductors to meet the required current density. However, using wide metal traces for inductors introduces more parasitic capacitances which affect the PA performance, especially at high frequencies. The number of parallel transistors used in a cascode stage is hence limited. In the designed dual-band PA, the common-emitter transistor Q_3 and common-base transistor Q_4 in the last cascode stage is each constituted from four parallel transistors,

while the common-emitter transistor Q_1 and common-base transistor Q_2 in the first stage each consists of two transistors. Each transistor has an emitter area of 0.15x20.32 μm^2 with two emitter, three base and two collector contacts. All transistors are biased at a current density of 10 mA/μm^2 for maximum f_{max} of 180 GHz.

The last stage is designed to give highest power efficiency while the first stage is designed to provide maximum output power. Load pull simulations are used to find the optimum loads at two different frequencies for each stage.

5.5.2 Concurrent Dual-band Output Matching Network Design

The dual-band output matching network is designed to concurrently transfer a 50-Ω load to two optimum impedances Z_{op1} = 14.5+7i Ω and Z_{op2}= 12+2i Ω at f_1 = 25.5 and f_2 = 37 GHz, respectively for maximum efficiency, and suppress the harmonics and IMPs. Following the dual-band matching methodology outlined in Section 5.4, two single-band output matching networks are first designed to transfer the 50-Ω load to Z_{op1} and Z_{op2} at 25.5 and 37 GHz, respectively. The 25.5-GHz matching network as shown in Fig. 5.12(a) consists of L_{o1}, C_{o2} and L_{o3}, and the 37-GHz matching network as shown in Fig. 5.12(b) consists of C_{o1} and L_{o2}. The concurrent dual-band output matching network as shown in Fig. 5.12(c) is synthesized from the 25.5- and 37-GHz matching networks to provide simultaneous output matching at 25.5 and 37-GHz. It consists of Network 6 (C_8, L_8 and L_9), Network 1 (L_{10} and C_{10}), and Network 9 (L_{11}, C_{11}, L_{12} and C_{12}) chosen from Table 5.1. These LC network types are chosen to not only synthesize the corresponding

inductor and capacitor at different frequencies, but also provide short or open at some particular frequencies to suppress the harmonics and IMPs.

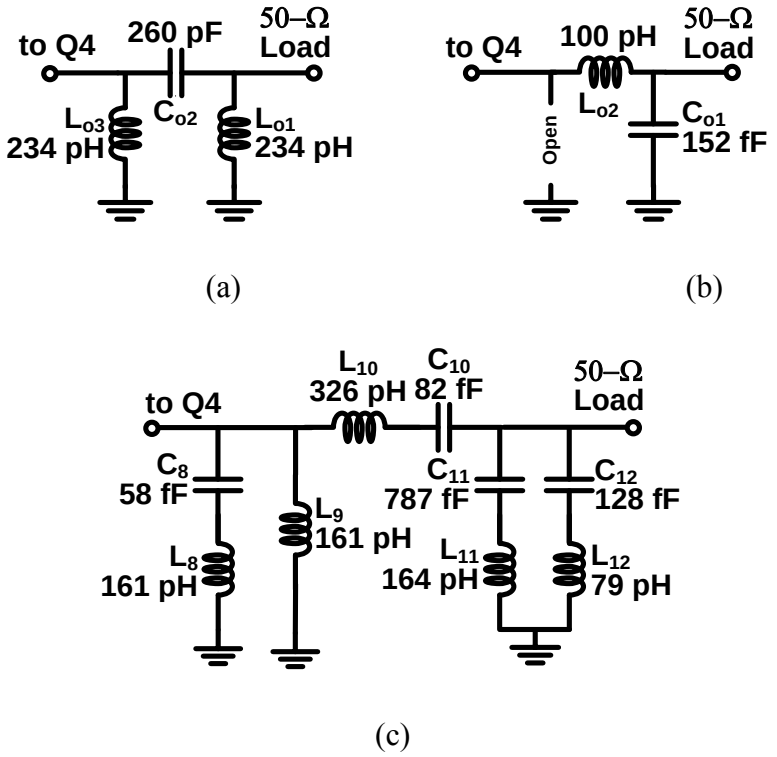


Fig. 5.12. 25.5-GHz (a) and 37-GHz (b) single-band output matching networks, and 25.5/37-GHz dual-band output matching network (c). An open is included in (b) to make the topologies in (a) and (b) compatible.

C_8, L_8 and L_9 (Network 6)

Network 6 consisting of C_8, L_8 and L_9 is used to simultaneously synthesize the inductor L_{o3} in Fig. 5.12(a) at $f_1 = 25.5$ GHz and the corresponding open circuit at $f_2 = 37$ GHz in Fig. 5.12(b). In addition, this network becomes a short circuit at 52.3 GHz to suppress the harmonic and IMP shown in Fig. 5.9. The short-circuit frequency of 52.3 GHz is chosen based on the distribution of the harmonics/IMPs in Fig. 5.9 and to

minimize the values of inductors L_8 and L_9, hence reducing the loss of the output matching network. Moreover, as shown in Fig. 5.11 the inductor L_9 conducts DC current to bias the cascade pair Q3 and Q4, thus avoiding the use of a bulky RF choke inductor. Making use of the Network-6 admittance expression listed in Table 5.1, (5.16) and (5.17) become

$$\frac{\omega_1\omega_{01}^2 C_8}{\omega_{01}^2-\omega_1^2}-\frac{1}{\omega_1 L_9}=-\frac{1}{\omega_1 L_{o3}} \tag{5.18}$$

$$\frac{\omega_2\omega_{01}^2 C_8}{\omega_{01}^2-\omega_2^2}-\frac{1}{\omega_2 L_9}=0 \tag{5.19}$$

where $\omega_1 = 2\pi f_1$ and $\omega_2 = 2\pi f_2$. The short-circuit condition is used at

$$\omega_{01}=\frac{1}{\sqrt{L_8 C_8}}=2\pi\times 52.3\times 10^9 \tag{5.20}$$

Equations (5.18)-(5.20) can be expressed in a simple set of two-variable linear equations:

$$\mathbf{A}C_8+\mathbf{B}\frac{1}{L_9}=\mathbf{M} \tag{5.21}$$

$$\mathbf{C}C_8+\mathbf{D}\frac{1}{L_9}=\mathbf{N} \tag{5.22}$$

where

$$\mathbf{A}=\frac{\omega_1\omega_{01}^2}{\omega_{01}^2-\omega_1^2},\ \mathbf{B}=\frac{1}{\omega_1},\ \mathbf{C}=\frac{\omega_2\omega_{01}^2}{\omega_{01}^2-\omega_2^2},\ \mathbf{D}=\frac{1}{\omega_2}$$

$$\mathbf{M}=-\frac{1}{\omega_1 L_{o3}}\ \text{and}\ \mathbf{N}=0$$

which are then solved to give the values for L_9, C_8, and L_8 as

$$L_9 = \frac{(\mathbf{AD\text{-}BC})}{(\mathbf{AN\text{-}CM})},\ C_8 = \frac{(\mathbf{DM\text{-}BN})}{(\mathbf{AD\text{-}BC})} \text{ and } L_8 = \frac{1}{C_8\omega_{01}^2}$$

or $C_8 = 58$ fF, and $L_8 = L_9 = 161$ pH.

L_{10} and C_{10} (Network 1)

Network 1 consisting of L_{10} and C_{10} is used to synthesize the capacitor C_{o2} in Fig. 5.12(a) at $f_1 = 25.5$ GHz and inductor L_{o2} in Fig. 5.12(b) at $f_2 = 37$ GHz. The capacitor C_{10} also functions as a DC block capacitor to prevent DC current from V_{CC} going to the 50-Ω load. Network 1 has less components than other networks, hence reducing the loss for the output matching network. Using the impedance expression for Network 1 shown in Table 5.1, we can write from (5.16) and (5.17):

$$\omega_1 L_{10} - \frac{1}{\omega_1 C_{10}} = -\frac{1}{\omega_1 C_{o2}} \tag{5.23}$$

$$\omega_2 L_{10} - \frac{1}{\omega_2 C_{10}} = \omega_2 L_{o2} \tag{5.24}$$

Solving (5.23) and (5.24) results in

$$L_{10} = \frac{(\mathbf{DM\text{-}BN})}{(\mathbf{AD\text{-}BC})} \text{ and } C_{10} = \frac{(\mathbf{AD\text{-}BC})}{(\mathbf{AN\text{-}CM})},$$

where

$$\mathbf{A}=\omega_1,\ \mathbf{B}=-\frac{1}{\omega_1},\ \mathbf{C}=\omega_2,\ \mathbf{D}=-\frac{1}{\omega_2},$$

$$\mathbf{M}=-\frac{1}{\omega_1 C_{o2}} \text{ and } \mathbf{N} = \omega_2 L_{o2}$$

or $L_{10} = 326$ pH and $C_{10} = 82$ fF.

L_{11}, C_{11}, L_{12} and C_{12} (Network 9)

Network 9 consisting of C_{11}, L_{11}, C_{12} and L_{12} is used to synthesize the inductor L_{o1} in Fig. 512(a) at f_1 = 25.5 GHz and C_{o1} in Fig. 5.12(b) at f_2 = 37 GHz. It also functions as short-circuit at 14 and 50 GHz to suppress the IMPs around 14 and 50 GHz, and the second harmonic of 25.5 GHz near 50 GHz. Equations (5.16) and (5.17) become, making use of Network 9's admittance expression:

$$\frac{\omega_1\omega_{01}^2 C_{11}}{\omega_{01}^2-\omega_1^2}+\frac{\omega_1\omega_{02}^2 C_{12}}{\omega_{02}^2-\omega_1^2}=-\frac{1}{\omega_1 L_{o1}} \tag{5.25}$$

$$\frac{\omega_2\omega_{01}^2 C_{11}}{\omega_{01}^2-\omega_2^2}+\frac{\omega_2\omega_{02}^2 C_{12}}{\omega_{02}^2-\omega_2^2}=\omega_2 C_{o1} \tag{5.26}$$

The harmonic and IMP suppression conditions are at

$$\begin{aligned}\omega_{01}&=\frac{1}{\sqrt{L_{11}C_{11}}}=2\pi 1410^9\\ \omega_{02}&=\frac{1}{\sqrt{L_{12}C_{12}}}=2\pi 5210^9\end{aligned} \tag{5.27}$$

Equations (5.25)-(5.27) can be rearranged into a set of two-variable linear equations from which C_{11}, L_{11}, C_{12} and L_{12} can be determined as

$$C_{11}=\frac{(\mathbf{DM}-\mathbf{BN})}{(\mathbf{AD}-\mathbf{BC})},\ L_{11}=\frac{1}{C_{11}\omega_{01}^2}$$
$$C_{12}=\frac{(\mathbf{AN}-\mathbf{CM})}{(\mathbf{AD}-\mathbf{BC})}\ \text{and}\ L_{12}=\frac{1}{C_{12}\omega_{02}^2}$$

where

$$\mathbf{A} = \frac{\omega_1\omega_{01}^2}{\omega_{01}^2 - \omega_1^2}, \mathbf{B} = \frac{\omega_1\omega_{02}^2}{\omega_{02}^2 - \omega_1^2}, \mathbf{C} = \frac{\omega_2\omega_{01}^2}{\omega_{01}^2 - \omega_2^2}, \mathbf{D} = \frac{\omega_2\omega_{02}^2}{\omega_{02}^2 - \omega_2^2},$$

$$\mathbf{M} = -\frac{1}{\omega_1 L_{o1}} \text{ and } \mathbf{N} = \omega_2 C_{o1}$$

or C_{11} = 787 fF, L_{11} = 164 pH, C_{12} = 128 fF, and L_{12} = 79 pH.

5.5.3 Concurrent Dual-band Inter-stage Matching Network Design

The dual-band inter-stage matching network is designed to concurrently match the second-stage's input impedances of 4–1.4i Ω and 4.5+1.8i Ω to the first-stage's output impedances of 30.8-24i Ω and 20.9-3.1i Ω at f_1 = 25.5 and f_2 = 37 GHz, respectively, to maximize the first-stage's output powers at these frequencies and suppress the IMPs existing at frequencies between the two fundamental tones. The 25.5-GHz single-band inter-stage matching network shown in Fig. 5.13(a) consists of L_{is1} and C_{is2}, and the 37-GHz single-band inter-stage matching network shown in Fig. 5.13(b) consists of C_{is1} and L_{is2}. The synthetic dual-band inter-stage matching network consists of Network 6 (C_4, L_4 and L_5) and Network 5 (L_6, C_6, L_7 and C_7). These networks are chosen to not only synthesize the corresponding inductor and capacitor at different frequencies, but also provide short and open at 30.2 and 31 GHz, respectively, hence suppressing the IMP components existing between the two main tones.

L_4, C_4 and L_5 (Network 6)

Network 6 consisting of L_4, C4, and L_5 is used to synthesize the capacitor C_{is2} at f_1=25.5 GHz and inductor L_{is2} at f_2=37 GHz. This network also produces a short at f_{01}=

30.2 GHz to suppress the IMP existing between f_1 and f_2 and create a dual-band response for the gain. Inductor L_5 conducts DC current to bias the cascade pair Q_1 and Q_2, hence eliminating the use of a bulky RF choke inductor. The values for C_4, L_4 and L_5 are obtained by solving (5.16) and (5.17) applying the admittance expression and short-circuit condition for Network 6, resulting in C_4 = 157 fF, $L_4 = L_5$ = 176 pH.

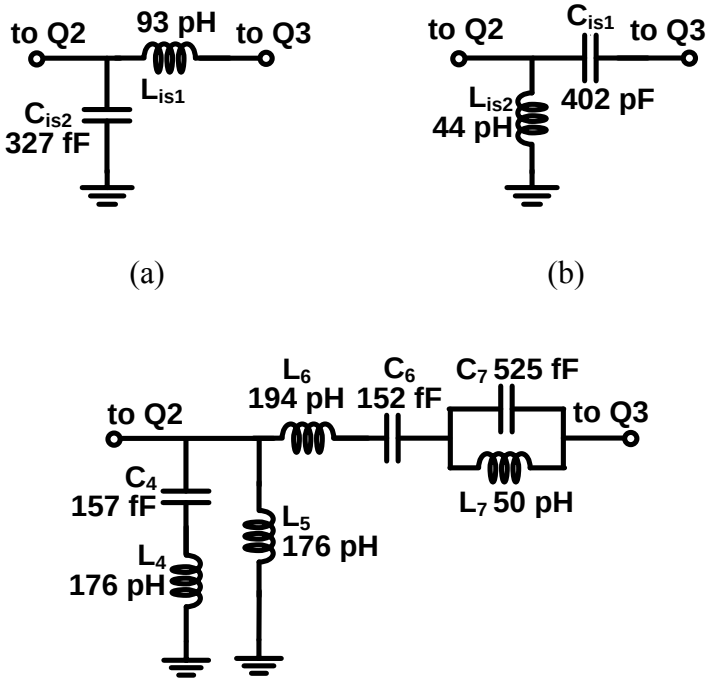


Fig. 5.13. 25.5-GHz (a) and 37-GHz (b) single-band inter-stage matching networks and 25.5/37-GHz dual-band inter-stage matching network (c).

L_6, C_6, L_7 and C_7 (Network 5)

Network 5 consisting of L_6, C_6, L_7 and C_7 is used to synthesize the inductor L_{is1} at f_1=25.5 GHz and the capacitor C_{is1} at f_2=37 GHz, while becoming an open circuit at

31 GHz to block the IMP existing between f_1 and f_2 and create a dual-band filtering response. Capacitor C_6 functions as an inter-stage DC blocking capacitor and the open-circuit frequency is determined by the parallel resonator of L_7 and C_7. Applying the impedance expression of Network 5 for (5.16) and (5.17), as well as Network 5's open-circuit condition shown in Table 5.1, we can obtain C_6 = 152 fF, L_6 = 194 pH, L_7 = 50 pH, and C_7 = 525 fF.

5.5.4 Concurrent Dual-band Input Matching Network Design

The dual-band input matching network is designed to concurrently match the first stage's input impedances of 7.4-4i Ω and 7.1-0.7i Ω to the 50-Ω source at 25.5 and 37 GHz, respectively, and reject the out-of-band signals.

Two single-band input matching networks at 25.5- and 37-GHz are shown in Figs. 5.14(a) and (b), respectively. The first one consists of L_{in1}, C_{in2}, and C_{in3} while the second one consists of C_{in1}, L_{in2}, and C_{in4}. Two capacitors C_{in3} and C_{in4} having the same value are used to reduce the gain at low frequencies and function as DC block capacitors. The dual-band input matching network consists of capacitor C_5 having the same value with C_{in3} and C_{in4}, Network 9 consisting of L_1, C_1, L_2 and C_2, and Network 1 consisting of L_3 and C_3.

L_1, C_1, L_2 and C_2 (Network 9)

Network 9 consisting of L_1, C_1, L_2 and C_2 is used to synthesize the inductor L_{in1} at f_1 = 25.5 GHz and C_{in1} at f_2 = 37 GHz, while acting as short-circuit at 18 and 51 GHz

to reject the out-of-band signals and shape the dual-band gain response. Values for C_{11}, L_{11}, C_{12} and L_{12} are obtained by solving (5.16) and (5.17) with the use of Network 9's impedance expression and short-circuit condition, resulting in C_1= 457 fF, L_1 = 171 pH, C_2 = 130 fF, and L_2 = 75 pH.

L_3 and C_3 (Network 1)

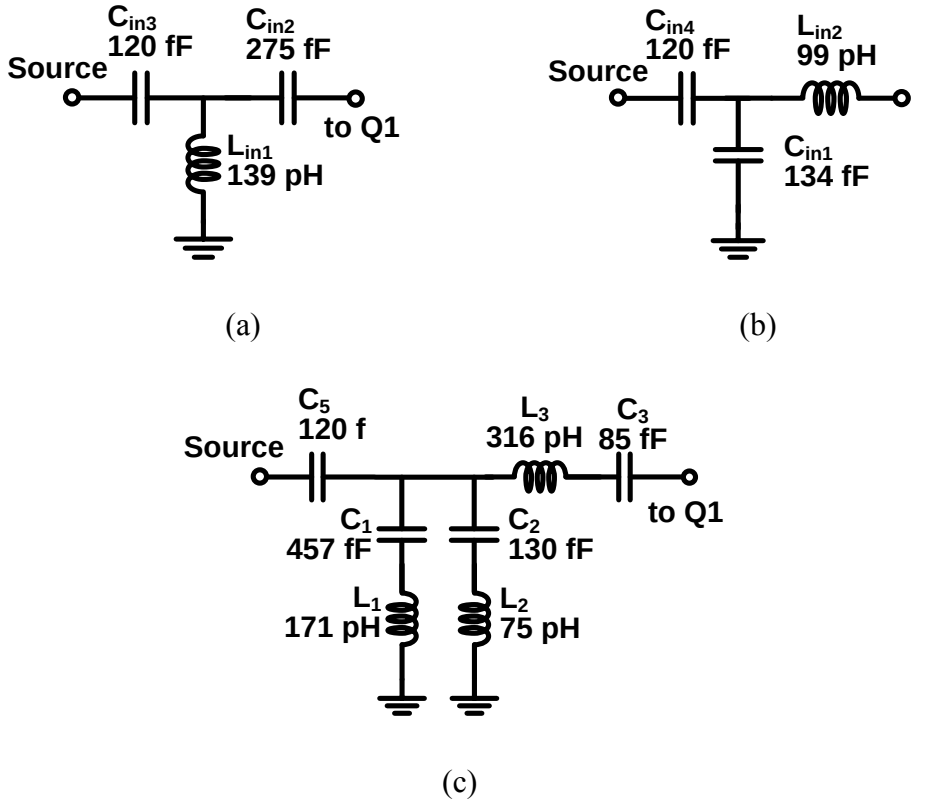


Fig. 5.14 25.5 GHz (a) and 37 GHz (b) single-band input matching networks, and 25.5/37-GHz dual-band input matching network (c).

Network 1 consisting of L_3 and C_3 is used to synthesize the capacitor C_{in2} at 25.5 GHz and inductor L_{in2} at 37 GHz. The capacitor C_3 also functions as a DC block

capacitor preventing DC current from the base of transistor Q1 feeding through the 50-Ω source. L_3 and C_3 are obtained from (5.16) and (5.17) as L_{10} = 316 pH and C_{10} =85 fF.

5.5.5 Power Amplifier Layout and Fabrication

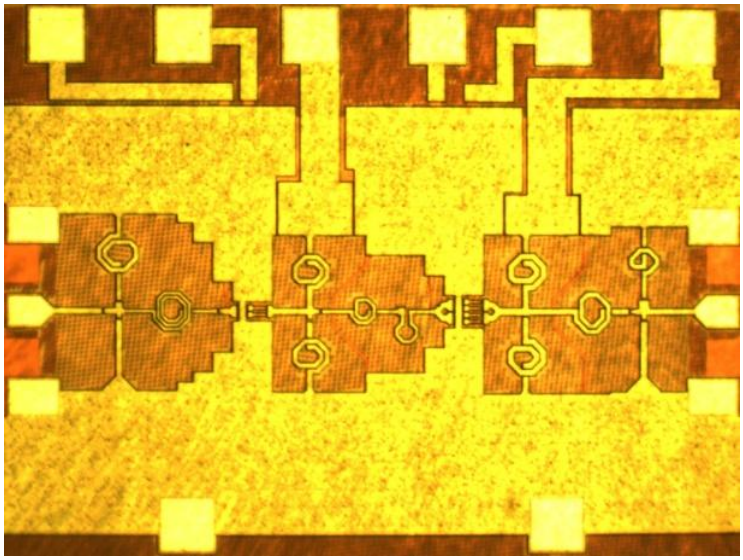


Fig. 5.15. Microphotograph of the 25.5/37-GHz dual-band power amplifier.

The 25.5/37-GHz concurrent dual-band PA was laid-out using Cadence. In the layout, the inductors are placed sufficiently far away from each other to reduce the inter-coupling while minimizing the chip area. All inductors in each dual-band matching network are simulated as a whole using IE3D to verify the performance after individual inductors have been laid-out. It is particularly noted that, at millimeter-wave frequencies, especially in large-area circuits, the AC ground has considerable effects to the circuit performance. It should therefore be considered as a distributed ground structure instead

of a simple ground point. To that end, it is crucial that complete EM simulation of the AC ground needs to be conducted and its EM-simulation result should be included in the circuit simulation and optimization. Fig. 5.15 shows a microphotograph of the dual-band PA. It has a chip area of 1.3×0.68 mm^2.

5.5.6 Dual-band Power Amplifier Performance

The designed concurrent dual-band PA was measured on-chip using Rhode & Schwarz vector network analyzer and Cascade probe station. The short-open-load-thru calibration method along with Microtech's impedance standard substrate standards was used. The unconditional stability of the PA was confirmed through simulated and measured results.

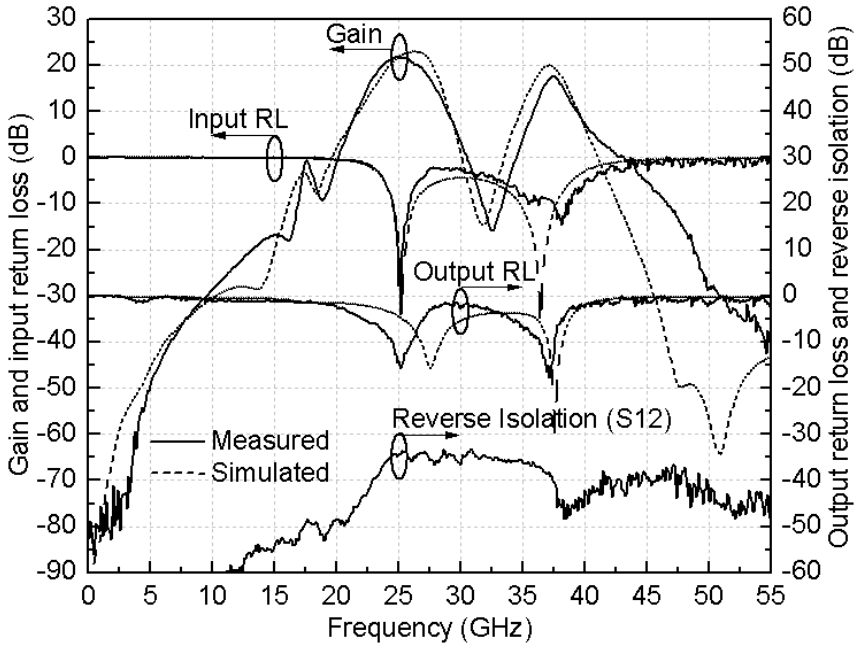


Fig. 5.16. Measured and simulated small-signal gain, return loss, and reverse isolation.

Fig. 5.16 shows the simulated and measured gain, input and output return loss, and reverse isolation of the concurrent dual-band PA under small-signal conditions. The dual-band PA exhibits gains of 21.4 dB and 17 dB, 3-dB bandwidths of 3.7 GHz and 1.8 GHz, input return losses of 14.8 and 9 dB, and output return losses of 12.5 and 15 dB at 25.5 GHz and 37 GHz, respectively. The reverse isolation is higher than 35 dB from DC to 55 GHz. The PA has a good dual-band gain response with out-of-band rejection below 0 dB from DC to 20, 30.5 to 34, and above 43 GHz. The rejection of signals at 32.5 GHz is 15 dB, while that at frequencies below 10 GHz and above 50 GHz is larger than 30 dB, resulting in good suppression of the harmonics, IMPs and out-of-band signals which are important for dual-band PA design. These characteristics are indeed achieved from the concurrent dual-band synthetic matching technique implemented for the input, inter-stage and output matching networks as expected. The PA consumes a current of 120 mA from a 3-V supply voltage.

The simulated and measured results are in good agreement from DC to 41 GHz. Particularly, the peak-gain differences between the measured and simulated results at 25.5 and 37 GHz are 0.6 and 2.6 dB, respectively. The series (L_4-C_4) and shunt (L_7-C_7) resonators help shape the dual-band gain through their resonant frequencies at 32.5 GHz. It is noted that most of the LC networks used in the dual-band PA change their equivalent impedance from inductance to capacitance, or vice versa, when the frequency crosses this notch point.

Fig. 5.17 shows the measured and simulated gain, output power and the power added efficiency (PAE) in the single-band mode at 25.5 and 37 GHz. The measured

results show that, in the single-band mode, the maximum output powers, $P_{out,max}$, reach 16 and 13 dBm, output 1-dB compression points, $P_{out,1dB}$, are 10.4 and 7.1 dBm, and maximum PAEs, PAE_{max}, are 10.6 and 4.9 % at 25.5 and 37 GHz, respectively.

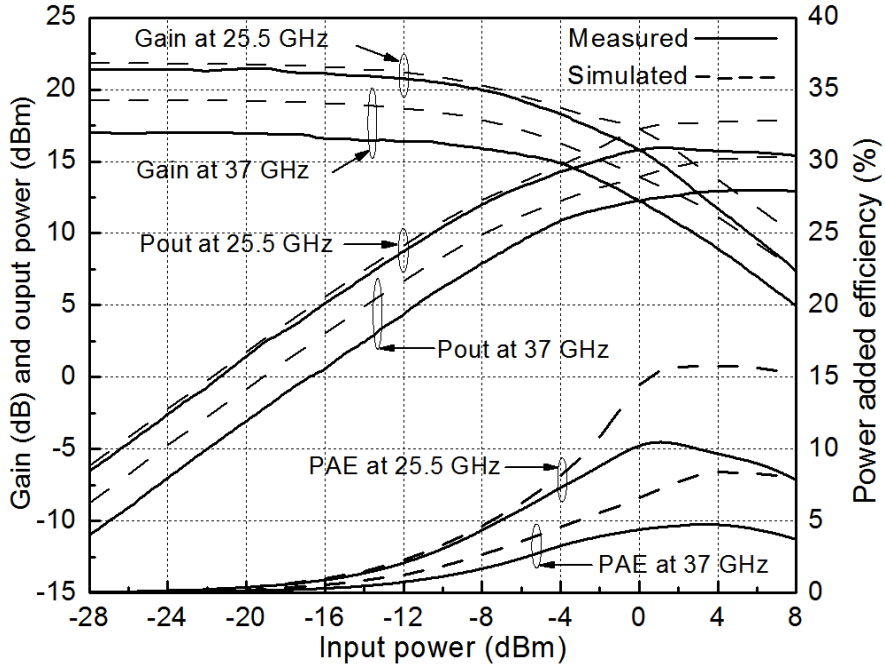


Fig. 5.17 Measured and simulated gain, output power and PAE at 25.5 and 37 GHz in single-band mode.

Since the PA gain at 25.5 GHz is higher than that at 37 GHz as seen in Fig. 10, the output power at 25.5 GHz is always higher than that at 37 GHz for the same input power. Therefore, in the dual-band mode and under equal input power, the 25.5-GHz signal would desensitize the 37-GHz signal, so that the PA reaches saturation state with much larger output power at 25.5 GHz than 37-GHz. In order to increase the 37-GHz saturation power, the input power at 25.5 GHz would need to be lower than that at 37 GHz.

Fig. 5.18 shows a simplified test bench for the PA measurement in the dual-band mode, in which two continuous-wave (CW) signals at 25.5 and 37 GHz are applied to the PA simultaneously. P_{in} is the initial (equal) input power of each tone, and $P_{in,f1} = P_{in}$ - 4.4 dBm and $P_{in,f2} = P_{in}$ are the input powers (in dBm) at 25.5 and 37 GHz, respectively. The input power of the 25.5-GHz tone is set to be 4.4 dB lower than that of the 37-GHz tone to ensure that the PA gives the same output power at both frequencies under small input-signal conditions, making use of the result that the difference of the two measured small-signal gains at 25.5 and 37 GHz is 4.4 dB as seen in Fig. 5.16. The same test bench is also used in the simulation using 2.4-dB difference between the input powers at 25.5 and 37 GHz, which is the difference of the two simulated gains at these frequencies as shown in Fig. 5.16.

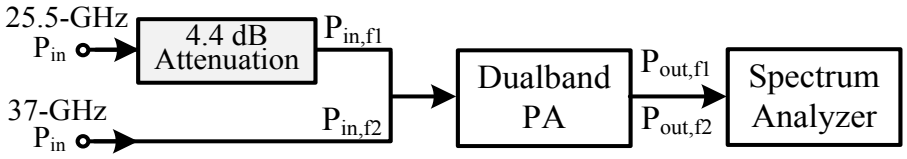


Fig. 5.18. Simplified test bench for the PA measurement in the dual-band mode.

Fig. 5.19 shows the measured and simulated gain, output power, and PAE in the dual-band mode. It is noted that the input power in the x-axis of Fig. 5.19 is P_{in} which is also equal to the input power of the 37-GHz tone ($P_{in,f2}$) in Fig. 5.18. As shown in Fig. 5.19, the measured output power of the 25.5- and 37-GHz signals are the same until their input power P_{in} reach -12.5 dBm. After that point, the 37-GHz output power is gradually

saturated while the 25.5-GHz output power keeps increasing for several dBm until it saturates. This shows different nonlinear behaviors of the active devices and the PA at large signal conditions, and the linearity of the PA at 25.5 GHz is higher than that at 37 GHz. The results in Fig. 5.19 signify that the nonlinearity of the PA is different for different frequencies as well as for dual- and single-mode. The measured results also show that, in the dual-band mode, the maximum output powers are 13 and 9.5 dBm, and the output 1-dB compression powers are 6.8 and 4.6 dBm at 25.5 and 37 GHz, respectively.

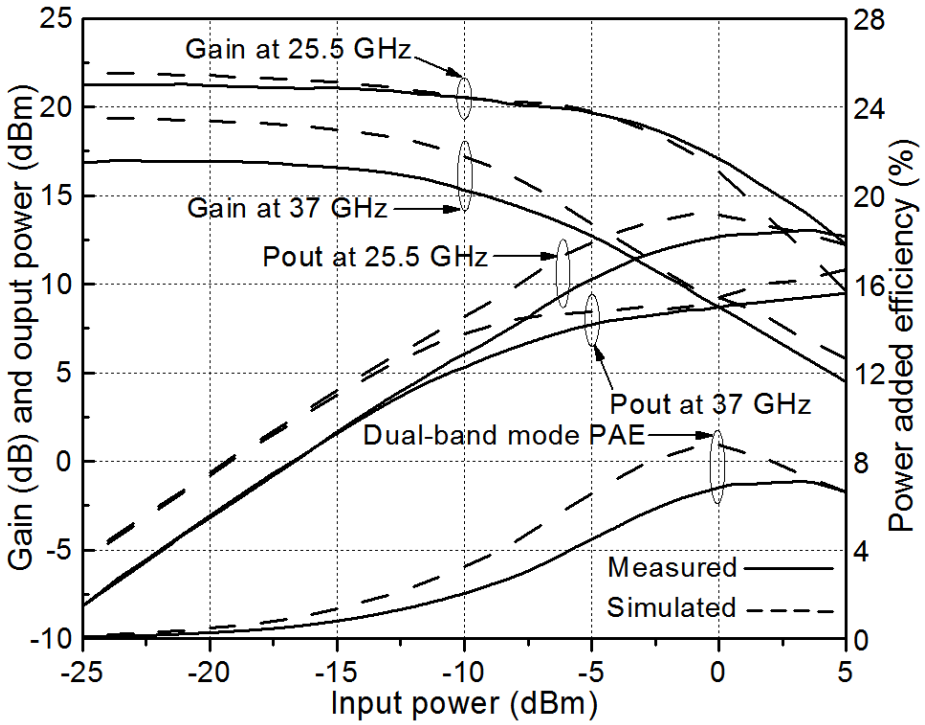


Fig. 5.19. Measured and simulated gain, output power and PAE in the 25.5/37-GHz dual-band mode.

It is noted that the PAE in the dual-band mode is expected to be different from that for the single-band mode. In order to take into account the effects of concurrent dual-band operation for PA, we define the PAE for the dual-band mode as

$$PAE=\frac{P_{out,f1}+P_{out,f2}-\left(P_{in,f1}+P_{in,f2}\right)}{P_{DC}} \tag{5.28}$$

where $P_{out,f1}$ and $P_{out,f2}$ are the output powers of the PA at 25.5 and 37 GHz, respectively, as indicated in Fig. 5.18. P_{DC} is the DC power. The measured results show that the maximum dual-band-mode PAE is 7.1%.

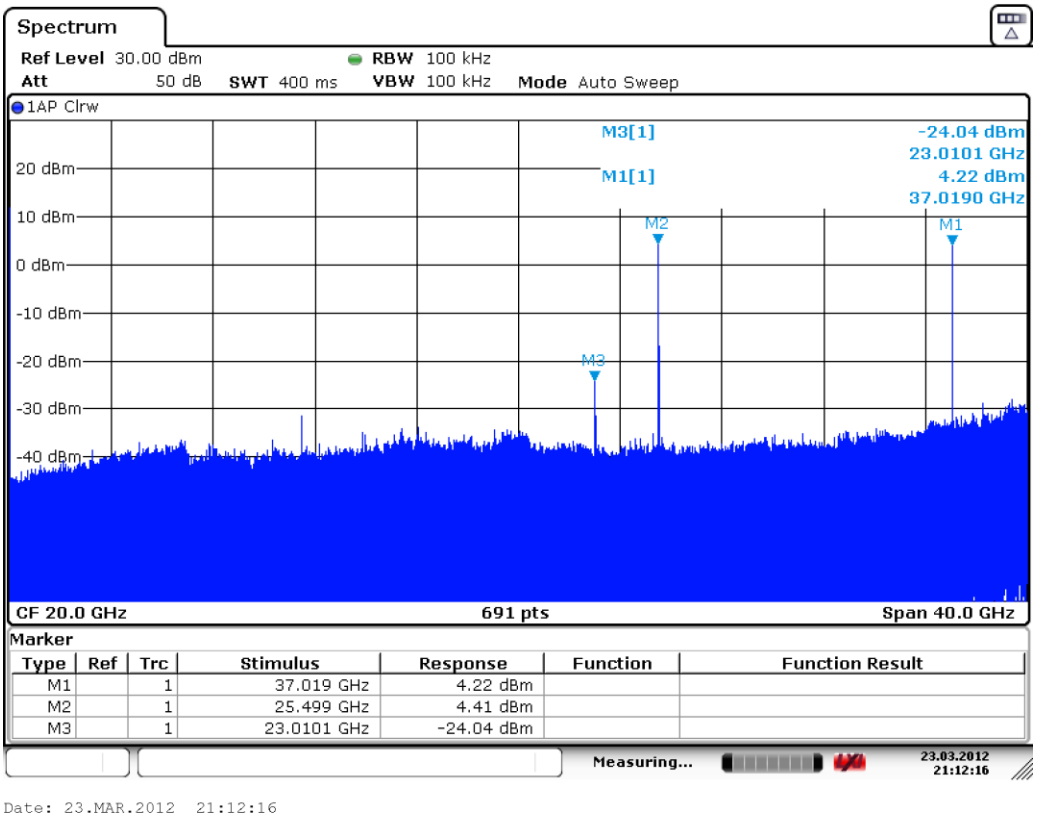


Fig. 5.20. Measured output spectrum of the dual-band PA in the dual-band mode.

It is observed that in the dual-band mode, the 25.5- and 37-GHz signals become compressed at input power several dBm lower than that in the single-band mode, and the maximum and 1-dB compression output power in the dual-band mode are lower than those in the single-band mode. Table 5.2 summarizes the performance of the designed concurrent dual-band PA in the single- and dual-band mode. The maximum difference between the simulated and measured results of gain, $P_{out,max}$, $P_{out,1dB}$, and PAE_{max} are 2.6 dB, 2.4 dBm, 1.7 dBm and 5.2 % in the single-band mode and 2.6 dB, 3.5 dBm, 2.2 dBm and 1.7% in the dual-band mode, respectively.

Fig. 5.20 displays the screen capture from a spectrum analyzer showing the output spectrum of the designed PA in the dual-band mode. In this measurement, the two fundamental tones at 25.5 and 37 GHz were used simultaneously as the input to the PA. The input power levels of the two tones were first increased to drive the PA into saturation, and then that of the 25.5-GHz tone was reduced so that the output powers of the two tones are roughly equal to 9 dBm. Note that 4.8 dB is added to the observed power level on the spectrum analyzer to compensate for the cable, connector and RF probe losses. It is observed that there is no IMP with power above the noise floor of -37 dBm existing between the two main tones, and there exists only one IMP at 23 GHz whose magnitude is 28 dB lower than the power of the two main tones. These results demonstrate good harmonic/IMP suppression of the developed dual-band matching technique.

Table 5.2 Summary of the PA performance in single- and dual-band mode

Parameter	**Single-band mode**				**Dual-band mode**			
	Simulated		**Measured**		**Simulated**		**Measured**	
Freq (GHz)	**25.5**	**37**	**25.5**	**37**	**25.5**	**37**	**25.5**	**37**
Gain (dB)	22	19.6	21.4	17	22	19.6	21.4	17
Input RL (dB)	21.3	17.1	14.8	9.1	21.3	17.1	14.8	9.1
Output RL (dB)	5.4	10.2	12.5	15	5.4	10.2	12.5	15
$\mathbf{P_{out,max}}$ (dBm)	17.8	15.4	16	13	14	11	13	9.5
$\mathbf{P_{out,1dB}}$ (dBm)	10.8	8.8	10.4	7.1	6.5	5.4	6.8	4.6
$\mathbf{PAE_{max}}$ (%)	15.8	8.4	10.6	4.9	8.8		7.1	

CHAPTER VI

DESIGN OF SiGe BICMOS CONCURRENT DUAL-BAND TRANSMITTER

6.1 Introduction

CMOS and related BiCMOS Radio-Frequency Integrated Circuits (RFICs) have advanced significantly during the past decades which, in turn, have pushed the performance and advancement of RF radar and communication systems that operate from several hundred MHz to millimeter-wave frequencies. Ultra-wideband and multi-band, multi-mode BiCMOS transmitters with high power, efficiency, linearity and dynamic range are important for modern high data-rate wireless communication and high resolution radar systems.

Various fully-integrated systems, based on different techniques including impulse, RF-pulse, phase-array and time correlation receiver using different technologies of III-V semiconductor, SiGe, CMOS and BiCMOS, have been reported [12], [80]-[86]. These systems use different transmit and receive antennae, with the transmitter (TX) and receiver (RX) located either on the same chip or different chips to maximize the system dynamic range. In order to reduce the system's cost and size, one antenna for both transmission and reception should be used along with a high-isolation T/R switch (or circulator). Particularly, in RF-pulse based systems using the correlation detection scheme such as [12], [85] and [86], RF pulse formers having ultra-high isolation are highly desired.

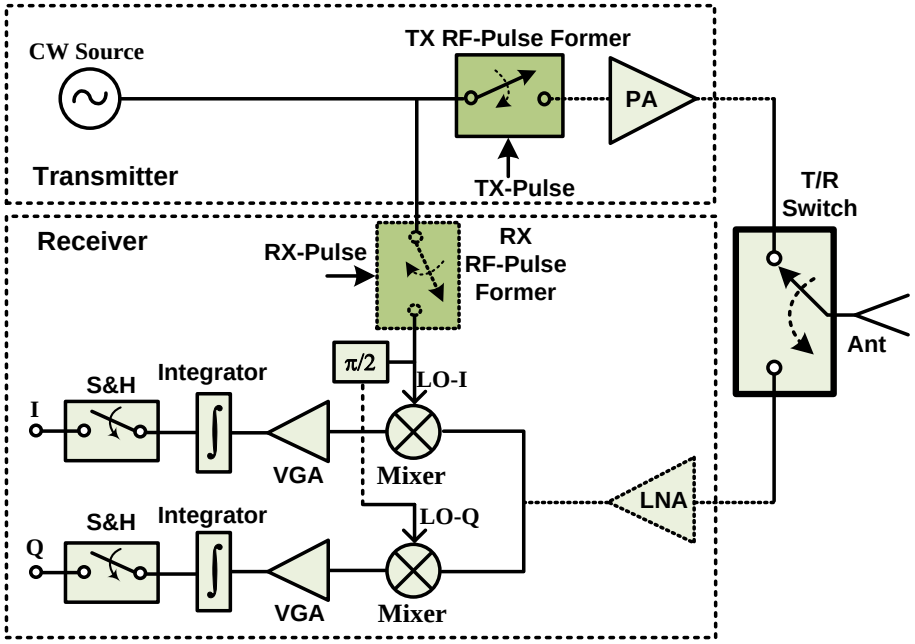


Fig. 6.1. Short-range RF-pulse radar transceiver using one antenna.

To illustrate the need of high-isolation RF pulse formers, we consider in Fig. 6.1 a time-gated correlation transceiver architecture using one antenna for short-range radar systems, which is modified from the architecture presented in [12]. The PA may be on all the time for short-range and high resolution applications. The operation of the transceiver is controlled by the TX-pulse and RX-pulse signals. In the transmission mode, a very narrow RF-pulse, setting the range resolution for the system, is produced from the TX RF-pulse former by gating the signal from the CW source, amplified by the PA, passes through the T/R switch, and transmitted by the antenna. In the reception mode, the reflected RF-pulse from the target, after captured by the antenna and amplified by the LNA, is correlated with the LO pulse, generated from the RX RF-pulse former by gating the signal from the CW source, on the basis of a particular/selective range gate. The signals at the I and Q mixer outputs are amplified by the respective VGA and then

integrated by the integrator. Based on the I and Q signals obtained by sampling the outputs of the integrators, the target is then characterized.

With the PA being on at all time, the transceiver in Fig. 6.1 needs an ultra-high-isolation RF-pulse former, considering possible RF leakage problems under the reception and transmission modes. Firstly, in the reception mode, as can be seen from Fig. 6.1, the leaking RF signal from the TX pulse-former, which is in the off state, is amplified by the PA and leaks to the receiver through the T/R switch. If the total isolation of the TX pulse-former and T/R switch is not high enough, this leakage signal is substantial and may be larger than the receiving signal, causing detrimental effects such as distorting the received signal, target undetectable, and reduced the detection range. To resolve this problem, the PA (and some other components) in the transmitting path may need to be turned off during the reception mode to improve the TX-RX isolation. This remedy however is not very suitable for short-range and high resolution radar systems as it slows down the system's operating speed due to the fact that, as the PA and/or other components are switched on and off frequently, they require some time in each state to completely settle before the transmission or reception process starts. Therefore, it is important to increase the isolation of the TX-pulse-former to enhance the system's dynamic range while keeping the PA on at all time. Secondly, during the transmission mode, the high-power transmitting signal from the TX port leaks to the RX port through the TR switch and mixes with the leakage LO signal from the RX-pulse former, resulting in I and Q offsets which affect the target's detection accuracy. The time needed to reset the I and Q offsets results in reduced radar update rate and increased

minimum detection range. In order to address the two aforementioned problems to make the performance of a one-antenna radar system similar to that of a two-antenna counterpart, the TX and RX RF-pulse formers need to have extremely high isolation.

In addition, dual-band systems provide numerous advantages as compared to single-band counterparts. In communication applications, it gives a larger capacity of information transfer and higher data rate. In radar applications, it offers higher ability of detecting, identifying, locating and tracking a wide range of targets, enhanced detection coverage, accurate target location, reduced survey time and cost, improved target information and improved reliability.

However, most of reported systems are single-band systems [82]-[87]. The transceiver for automotive radars reported in [86] works in dual bands at 22-29 GHz and 77-81 GHz but cannot operate in concurrent modes. This chapter presents the design of a concurrent dual-band transmitter working at 24.5 and 35 GHz for the short-range high-resolution radar and high-data-rate communication systems. The idea of dual-band operation in this transmitter is doubly significant and attractive when considering that all of the dual-band functions can be realized within only a single hardware system using the concurrent design technique, thus making the entire system no more complicated than a single-band counterpart.

6.2 Concurrent Dual-band Transmitter Architecture and Specifications

6.2.1 Transmitter Architecture and Operation

Fig. 6.2 shows the proposed concurrent dual-band RF-pulse transmitter for the short-range high-resolution radar and high-data-rate communication systems. The choice of RF-pulse based operation for the radar systems allows the transmitter to be used in the communication systems as well with appropriate modulation schemes, such as OOK. The designed transmitter is an advanced, low cost, compact and dual-band transmitter concurrently operating in K- and Ka-bands used for high-data-rate communication systems, and high accuracy and resolution radar systems for detection, identification, location, and tracking of multiple moving targets.

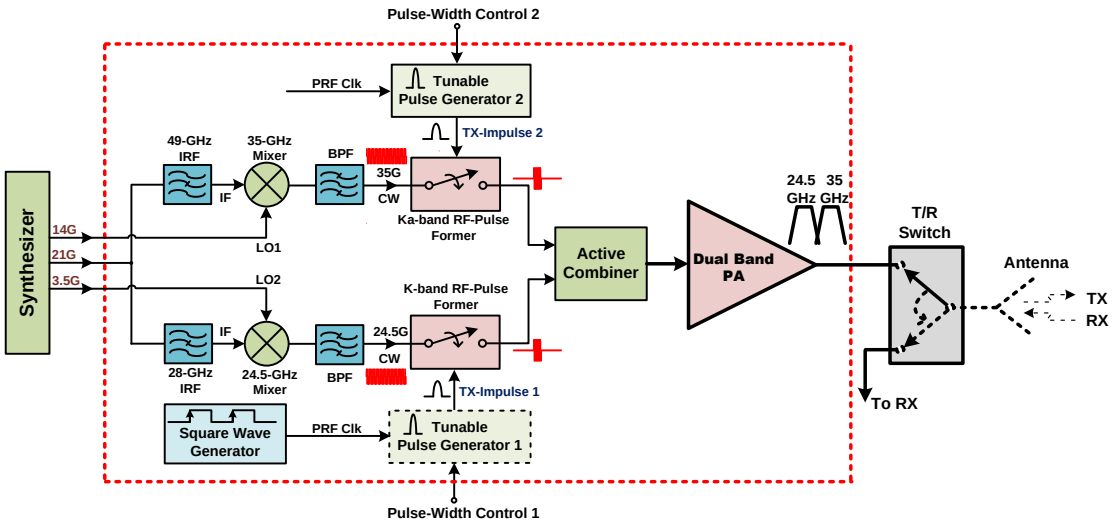


Fig. 6.2. Proposed concurrent dual-band transmitter architecture.

The transmitter is designed to transmit narrow RF-pulses at 24.5 and 35 GHz concurrently. The dual RF-pulses are incident to the target, reflected back and received at the receiver from which the presence of the targets are determined and other information such as location and velocity are extracted.

The proposed dual-band transmitter consists of two up-conversion mixers along with two image reject filters (IRFs), two RF-pulse formers, two tunable impulse generators (PGs), one square-wave clock generator, one active combiner and one concurrent dual-band power amplifier. The two mixers with variable gains are used as source generators to produce 24.5 and 35-GHz continuous wave (CW) signals from 21-GHz IF, and 3.5- and 14-GHz LO signals. The transmitting output powers are controlled by varying the gain of the mixers. Two K- and Ka-band RF-pulse formers, controlled by TX-impulses, are designed to generate very narrow RF pulses at 24.5 and 35-GHz, respectively, with extremely low RF leakage power when they are off. The width of the impulses; hence RF pulses at two frequency bands are independently tuned using two control voltages of pulse-width-control-1 and pulse-width-control-2. These RF-pulses are then combined in the active combiner, amplified by the concurrent dual-band power amplifier, and then transmitted to the air through a transmit/receive (T/R) switch and a dual-band antenna system. The transmitter is driven by a square wave clock for transmitting RF-pulses at the clock frequency of PRF. The pulse repetition frequency is very high for the transmitter use in the communication systems.

Capabilities of transmitting very narrow and tunable RF-pulse signals at high speed with extremely low RF leakage when the transmitter is off, and concurrently

operating at two carrier frequencies of 24.5 and 35 GHz characterize the unique features of this novel transmitter. The generation of tunable RF pulses allows the radar system to flexibly work at multiple range resolutions. The extremely low RF leakage, obtained with using the RF leakage cancellation technique, allows the transmitter to share one antenna system with the receiver, turn on the PA at all time, increase the system dynamic range, comply the transmitting spectrum requirement and avoid harming to other systems; hence improving system performance, size and cost. High data-rate in communication systems and high resolution in radar systems are achieved as the consequence of transmitting narrow RF pulses. In addition, the designed transmitter demonstrates a design approach for small size, low cost and low power consumption systems in which a single dual-band component is designed for use with two RF signals at two different bands.

6.2.2 Transmitter Specifications

A variety of parameters exist for the transmitter design, including the transmitted RF-pulse width (t_d), PRF, carrier frequencies (fc), maximum transmitted powers, RF leakage power and on/off isolation. The transmitter design can be started from the required range resolution. The proposed transmitter is required to provide the range resolution, ΔR, of 0.15 m. The RF-pulse width is then calculated from the range resolution as

$$t_d = \frac{2\Delta R}{c} = \frac{2 * 0.15}{3 * 10^8} = 1 \text{ ns} \tag{6.1}$$

where $c=3.10^8$m/s is the light velocity.

The bandwidth of the RF-pulse is then calculated from the RF-pulse width as

$$BW = \frac{1}{t_d} = 1\,\text{GHz} \tag{6.2}$$

The dual-band time-gated correlation receiver architecture, which is similar to the single-band counterpart shown in Fig. 6.1, is used for the objective of verifying the transmitter's design parameters. The minimum detectable signal power at the receiver front-end, S_{min}, is selected for two conditions. First, it must be higher than the RF leakage power from TX to RX in the reception mode, and second it allows the required signal-to-noise power ratio at the output of the receiver to be obtained for correct detection. Since the transmitter and receiver of the pulse radar system in this work share one antenna system using a T/R switch, the first condition sets the minimum detectable signal for the receiver. The RF leakage power from TX to RX in the reception mode, $P_{TX,\,leak}$, can be estimated from the maximum transmitting output power, P_{TX}, and the isolation of the RF-pulse former, I_{RFPM}, and T/R switch, I_{TR}, as

$$P_{TX,\,leak} = P_{TX} - I_{RFPM} - I_{TR} \tag{6.3}$$

The RF-pulse former isolation is 70 dB as presented in the following section and the T/R switch isolation is assumed as 25 dB. The maximum output powers for each band in the single-band and dual-band modes are determined from the maximum output powers of the concurrent dual-band power amplifier designed in Chapter V and listed in Table 5.2. The $P_{TX,\,leak}$ for each band in each mode is calculated using (6.3) and listed in Table 6.1. The sensitivity for each band is selected 5-dB higher than its $P_{TX,\,leak}$.

Table 6.1 Calculated specifications for transmitter

	Single-band		Dual-band	
Frequency (GHz)	24.5	35	24.5	35
P_{TX} (dBm)	16	13	9.5	9.5
$P_{TX,\ leak}$ at RX	-79	-82	-85.5	-85.5
RX's sensitivity	-74	-77	-80.5	-80.5
R_{max} (m)	14.7	12.4	14.7	12.4
$SNR_{out,min}$	0	-3	-6.5	-6.5
PRF_{max} (MHz)	10	12	10	12

The maximum detection range is then calculated from the receiver's sensitivity using radar equation [14]

$$R_{max} = \left[\frac{P_{TX} G_{TX} . G_{RX} . \lambda^2 . \sigma}{L . (4\pi)^3 . S_{min}} \right]^{1/4} \tag{6.4}$$

Where P_{TX} is the maximum transmitting power, G_{TX} and G_{RX} are transmit and receive antenna gains which are assume to be 10 dB, σ is the target cross-section which is assumed to be $10m^2$ [12], λ is the signal wavelength, and L is the insertion loss of the T/R switch which is assumed to be 2 dB.

The minimum signal to noise power ratio for each range gate, $SNR_{o,min}$, at the output of the integrators is calculated from the maximum range R_{max} using the radar equation [14] and listed in Table 6.1.

$$SNR_{o,min} = \frac{P_{TX} G_{TX} . G_{RX} . \lambda^2 . \sigma}{(4\pi)^3 . L^2 . K . T . BW . F . R_{max}^4} \tag{6.5}$$

where KT = -174 dBm is the thermal noise power density, BW is the bandwidth of the system which is 1 GHz, F is the receiver noise figure which is assumed to be 8 dB. It is noted that with the small $SNR_{o,min}$, it is required that the receiver take the integral of output signals of each range-gate for many RF pulses so that the required signal to noise power ratio at the output of the integrator is obtained [14].

The maximum PRF for the unambiguous range is calculated as

$$PRF_{max} = \frac{c}{2R_{max}} \tag{6.5}$$

The maximum PRF for different operation modes and frequencies are calculated and summarized in Table 6.1. For the objective of demonstration, the PRF of 3 MHz is used in this work.

Table 6.2 summarizes design specifications for the transmitter.

Table 6.2 Transmitter design specifications

Parameters	Specification
Operating frequency	24.5 GHz / 35 GHz
Sensing range	R_{min} = 0.15m, R_{max} = 12.4 - 14.7 m
RF-pulse duration (min)	T_0 = 1ns
Range resolution	ΔR =0.15m
Pulse repetition frequency	3 Mhz
Signal bandwidth (max)	1 GHz
Single-band mode output power	13/16 dBm at 24.5/35-GHz bands
Dual-band mode output power	9.5 dBm
On/Off isolation	> 70 dB

6.3 Concurrent Dual-band Transmitter Design

As shown in Fig. 6.2, the proposed dual-band transmitter consists of two up-conversion mixers going along with two image reject filters (IRFs), two RF-pulse formers, two tunable impulse generators (PGs), one square-wave clock generator, one active combiner and one concurrent dual-band power amplifier.

The design and measurement of two up-conversion mixers generating 24.5 and 35-GHz CW signals have been presented in Chapter II. The mixer measured results shown in Chapter II meet the design requirements for the transmitter. The concurrent dual-band power amplifier in Chapter V was redesigned and optimized to work at 24.5 and 35 GHz for the transmitter integration. Inductors used in the PA are designed with ground shields to improve their performance and reduce the coupling effects with other components. The redesigned PA is expected to have the same performance as presented in Chapter V.

Designs of other components constituting the dual-band transmitter including image reject filters, pulse generators, square-wave clock generator, RF pulse formers and power combiner will be presented in subsequent sections.

6.3.1 Image Rejection Filter Design

As shown in Fig. 6.2, the 24.5-GHz CW signal is generated by mixing 21-GHz IF and 3.5-GHz LO signal using the 24.5-GHz mixer, and the 35-GHz CW signal is generated by mixing 21-GHz IF and 14-GHz LO signals using the 35-GHz mixer. Therefore, image reject filters are needed to reject the 28- and 49-GHz image signals for

the 24.5- and 35-GHz mixers, respectively. The 28-GHz IRF, basically a band-stop filter, is designed to reject the 28-GHz image signal leaking from 35-GHz mixer and the 49-GHz IRF is designed to reject the 49-GHz image signal leaking from the 24.5-GHz mixer. Fig. 6.3 shows the schematics of the 28- and 49-GHz IRFs. The simulated insertion losses at 21 GHz and rejections at image frequencies are summarized in Table 6.3.

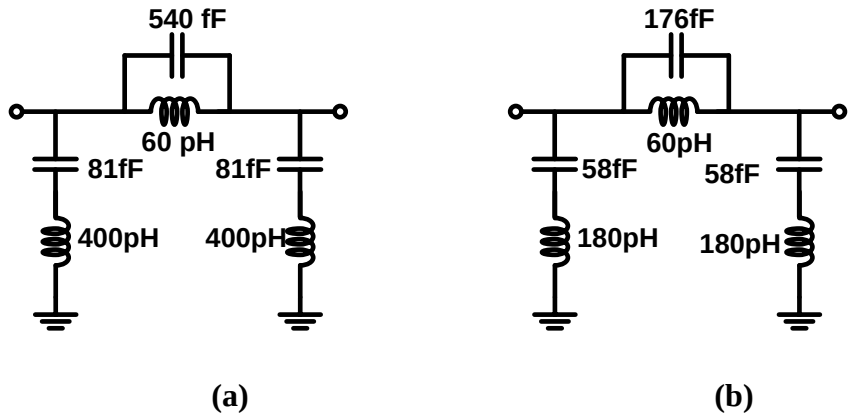


Fig. 6.3. 28-GHz (a) and 49-GHz (b) IRF schematic.

Table 6.3 28-GHz and 49-GHz IRF simulated performance

IRF	Insertion loss at 21 GHz (dB)	Rejection at image frequency (dB)
28-GHz	1.6	46
49-GHz	0.3	50

6.3.2 Impulse Generator Design and Measurement

The impulse generator produces an impulse signal to control the RF-pulse formers to gate 24.5 and 35-GHz CW signals to generate RF pulses. The widths of RF pulses are roughly equal to the widths of control impulses. It is desirable to have the

impulse duration, hence RF-pulse width, tunable so that the resolution of radar systems can be flexibly changed. The impulse generator is driven by a squared wave clock at the frequency of PRF. At every rising edge of the PRF clock, an impulse is generated.

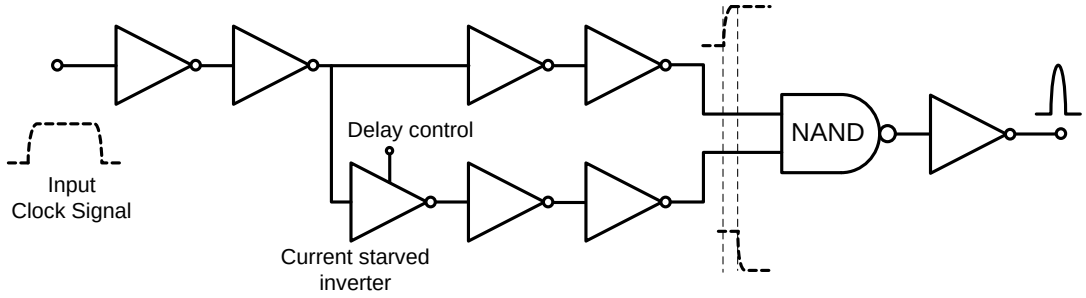


Fig. 6.4. Impulse generator schematic.

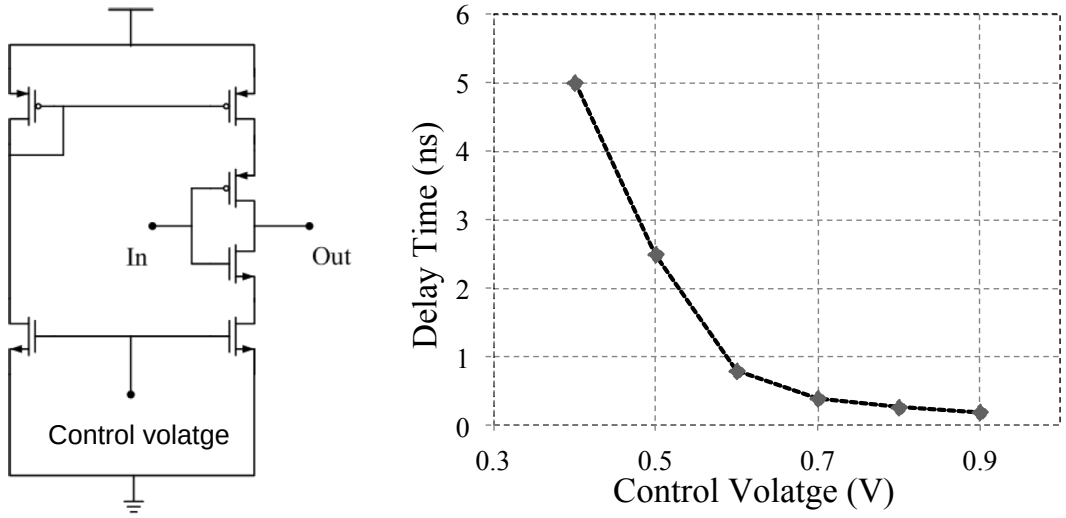


Fig. 6.5. Current starving inverter structure (a) and its delay tuning range (b).

The CMOS impulse generator, as shown in Fig. 6.4, is designed using digital logic gates presented in [3]. A chain of inverters is used to sharpen rising/falling edges

of the input clock signal, which is needed for the following generation of narrow impulse signals. The sharpened clock signal is then split into two branches. In one of the branch, the clock is delayed and inverted with respect to the other using chains of inverter and a current starved inverter. The following NAND gate then combines the rising and falling edges of these clocks to form an impulse as illustrated in Fig. 6.4.

The current starved inverter is used to invert the clock with a tunable delay. The delay of the clocks at the output and input of the current starved inverter is controlled using a control voltage. As shown in Fig. 6.5 (a), the control voltage changes the charging/discharging currents of the current starved inverter, hence tuning the delay time [3]. Fig. 6.5(b) shows the simulated delay time of the current starved inverter versus its control voltage. The simulation results show that the output impulse duration can be tuned from 200 ps to 5 ns when the control voltage changes from 0.9 to 0.4 V. Fig. 6.6 shows the several simulated impulses generated from the impulse generator and the 1-ns impulse is obtained with the control voltage of 0.56 V.

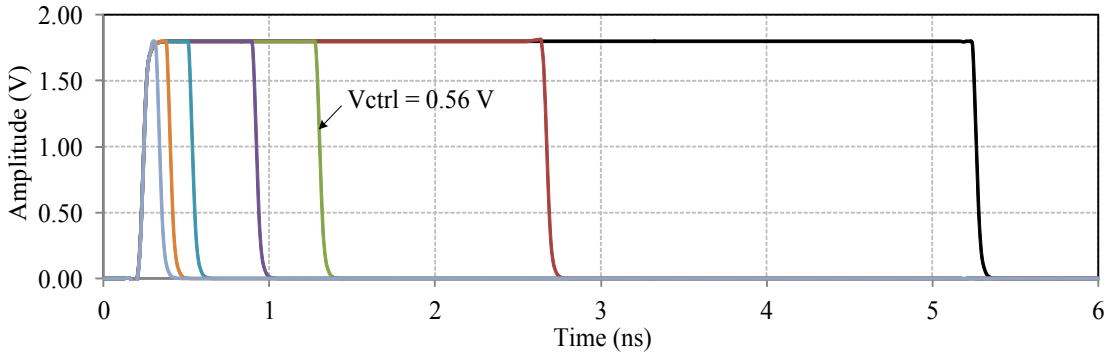


Fig. 6.6. Simulated tunable impulses.

Fig. 6.7 shows the measured results of the designed impulse generator. 1ns-impulse is obtained at control voltage of 0.9 V. Fig. 6.8 shows the measured inverted-impulses of 4-ns and 1-ns durations.

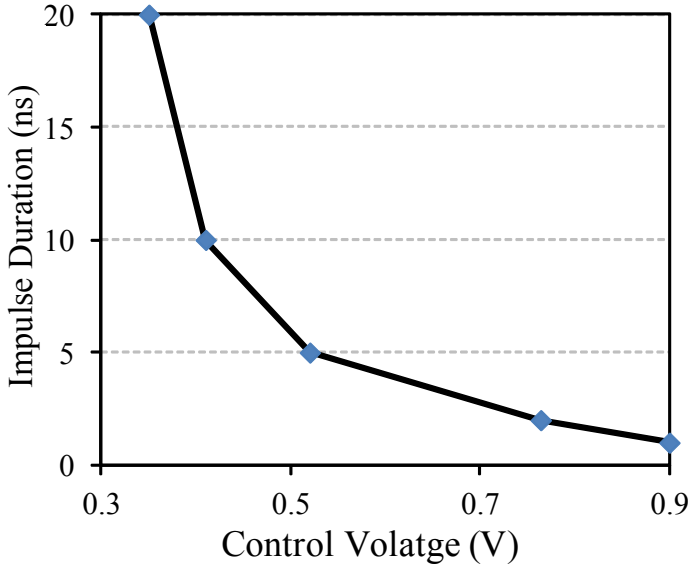
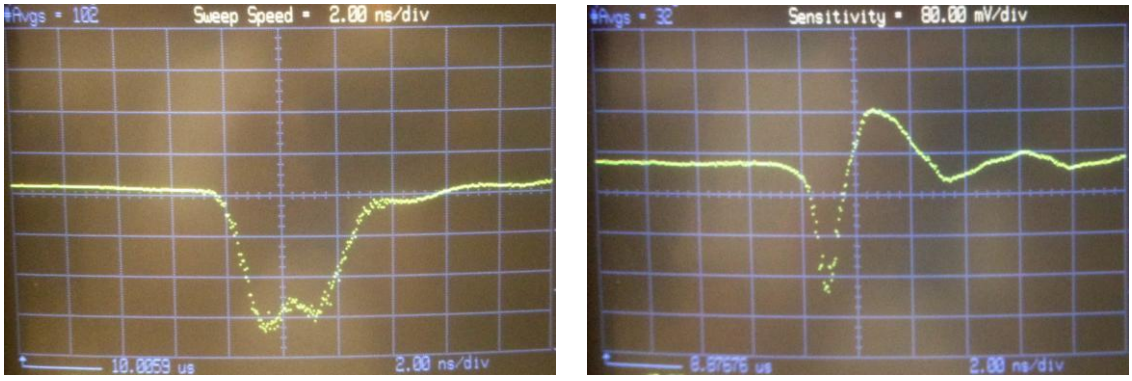


Fig. 6.7. Measured impulse duration versus control voltage.



(a) (b)

Fig. 6.8. Measured 4-ns (a) and 1-ns (b) inverted-impulses.

6.3.3 Square-Wave Clock Generator Design and Measurement

The square-wave clock generator in the transmitter generates the square-wave clock at the PRF of 3 MHz to drive the impulse generator, and hence the whole transmitter. As shown in Fig. 6.9, the square-wave clock generator consists of three inverters and a RC feedback network including R_1, R_2, and C, which provides a feedback loop for the oscillation [87].

The clock duty cycle is close to 50% and the clock frequency is given as

$$f = \frac{1}{2C(0.405R_{eq} + 0.693R_1)} \tag{6.6}$$

where

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} \tag{6.7}$$

With $R_1 = R_2$, the clock frequency becomes

$$f = \frac{0.559}{RC} \tag{6.8}$$

The square-wave clock generator is designed using Jazz 0.18 BiCMOS process with C = 12.4 pF, $R = R_1 = R_2 = 15$ KΩ and a power supply voltage of 1.8V.

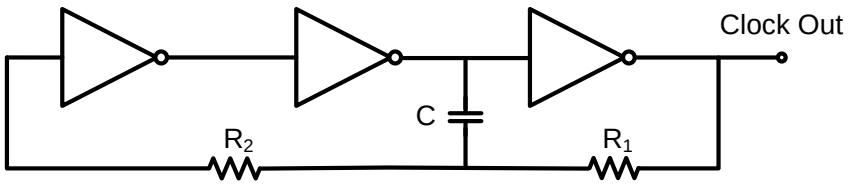


Fig. 6.9. PRF square-wave clock generator schematic.

Fig. 6.10 shows the measured square-wave clock with the peak-peak amplitude of 1.9 V. The spectrum of the measured clock, shown Fig. 6.11, shows that the PRF clock frequency is 2.92 MHz.

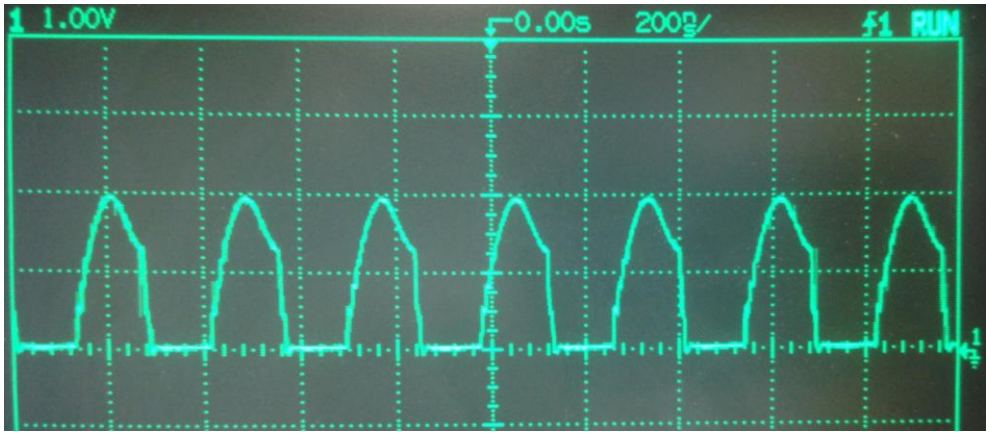


Fig. 6.10. Measured square-wave clock.

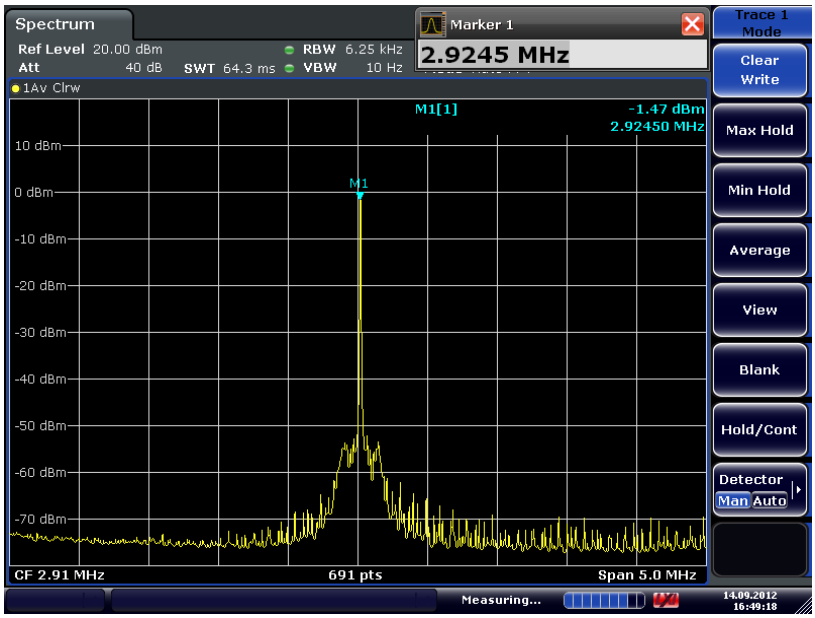


Fig. 6.11. Measured square-wave PRF clock spectrum.

6.3.4 K and Ka-band RF-pulse Former Design and Measurement

RF-pulse formers, based on time-gated STSP switches, are the most critical components in the short-range, high-resolution pulse radar and high-data-rate communication systems. RF-pulse formers with small switching time and high isolation are desirable for high range-resolution, accuracy, and receiver's dynamic range (hence detection range) in radar systems. The short-range high-resolution RF-pulse based radar system in this work is required to detect objects with range resolution of 15 cm. This leads to the need of RF-pulse formers capable of producing very narrow RF-pulses in the order of 1ns with small rising and falling time. For communication systems, narrow RF-pulses are needed to transmit and receive data at high rates. In addition, the RF-pulse formers in the transmitters are also required to have a very high isolation so that the transmitting signals can comply with the regulated spectrums and the RF leakage can be minimized, hence system's dynamic range can be enhanced. It is desirable to have low insertion loss or possible gain for the RF-pulse formers as well.

Ka-band RF-pulse Former

The Ka-band RF-pulse former is designed using the ultra-high high isolation SPST switch architecture presented in Chapter IV. As shown in Fig. 6.12, the Ka-band RF-pulse former consists of two identical SPST switches, an active balun, and input and output matching networks. The two identical switches are named "Off-SPST" switch, always operating in the off-mode, and "Core-SPST" switch operating as a normal switch (on/off). The Off-SPST and Core-SPST switches are implemented using a simple

conventional switch structure employing a series and a shunt deep-n-well transistor. Three inverters in the Off- and Core-SPST are used to produce complementary control impulses and sharpen the rising and falling edges of the control impulses. The active balun functioning as a differential amplifier is used to amplify the RF pulses and suppress the RF leakage as presented in Chapter III. The active balun is designed using the parasitic neutralization and compensation technique to have good balance at very high frequencies and over a wide bandwidth. The RF-pulse former exhibits gain when it is on and extremely high isolation when it is off. The input and output matching networks, formed by (L_{mi}, C_{mi}) and (L_{mo}, C_{mo}), respectively, provide good matching for the RF-pulse former.

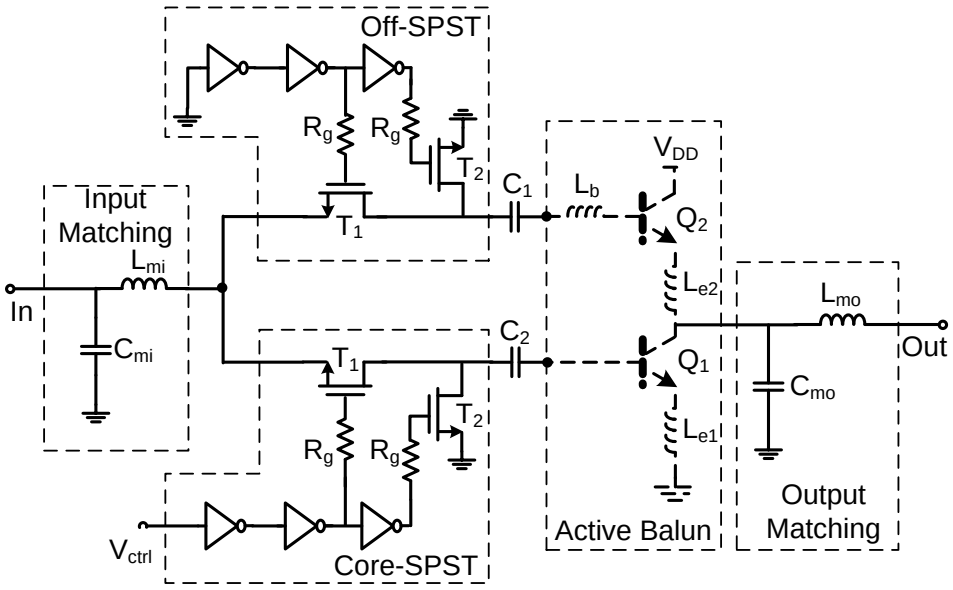


Fig. 6.12. Simplified schematic of the Ka-band RF-pulse former.

The RF pulses are formed by gating the 35-GHz CW signal passing through the

Core-SPST switch using the control impulses applying at the V_{ctrl} pin of the Core-SPST. In order to get a fast switching time in the order of 200 ps, the gate resistors for the transistors in the Core- and Off-SPST switches are chosen as 400 Ω. When the Core-SPST is off, the leakage RF signal from its output is combined with another RF leakage signal from the Off-SPST's output by the active balun and suppressed.

The Core- and Off-SPST are designed to have an isolation of 20 dB. From the insertion loss and isolation contour graph (Fig. 4.6), the series and shunt transistor sizes are chosen as 64 and 84 μm, respectively. The corresponding insertion loss is 2.4 dB.

The integrated inverters used to sharpen the rising and falling edges for the gating impulses are designed to have a very small delay between the their input and output, so that they cause less effects to the switching time of the RF-pulse former.

Active Balun Design

The two HBT transistors Q_1 and Q_2 in the active balun have the same size with an emitter area of 0.15 x 10.16 μm^2 and are biased at a DC current of 7.3 mA. The bases of Q_1 and Q_2 are biased at 1.1 V and 1.8 V, respectively, through large resistors which do not affect the balun's RF operation. The collector of Q_2 is connected to V_{DD} of 1.8 V. The values of inductors L_{e1}, L_{e2} and L_b are calculated from designed equations (3.12) and (3.13) presented in Chapter III, and then optimized in Cadence simulation [23]. Their final values are 95, 95 and 120 pH, respectively. All circuit elements and their values are summarized in Table 6.4.

Table 6.4 Ka-band RF-pulse former circuit elements and values

T_1		64 μm gate width	
T_2		80 μm gate width	
Q_1, Q_2		0.15 x 8.28 μm^2 emitter area	
L_{e1}, L_{e2}	95 pH	L_{mi}	178 pH
L_b	120 pH	C_{mi}	110 fF
R_g	400 Ω	L_{mo}	260 pH
V_{DD}	1.8 V	C_{mo}	122 fF

The Ka-band RF-pulse former was designed and fabricated using Jazz 0.18-μm BiCMOS process [21]. All the on-chip inductors and interconnecting lines were designed and simulated using the full-wave electromagnetic simulator IE3D [22]. The microphotograph of the RF-pulse former is shown in Fig. 6.13 with a chip area of 450 x 500 μm^2.

Measurement Results

The Ka-band RF-pulse former's S-parameters were measured on-chip using an Agilent PNA E8361C vector network analyzer. The Short-Open-Load-Thru calibration method along with Microtech's impedance standard substrate standards was used. The RF-pulse was measured in the time domain using the digital oscilloscope HP 54124T. The RF-pulse former is controlled on and off by the impulses generated from an external impulse generator Picosecond 10050A. The control impulses have tunable pulse widths from 100 ps to 10 ns with the rising and falling times of 45 ps and 110 ps, respectively.

The measurement of the RF-pulse former using the designed CMOS impulse generator is also carried out. The spectrums of the RF-pulses are measured using a Rohde & Schwarz FSV spectrum analyzer.

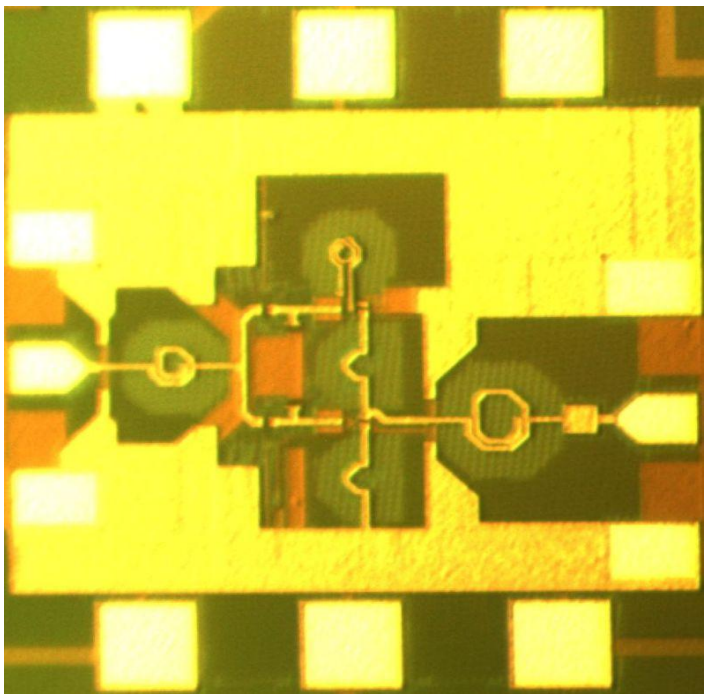


Fig. 6.13. Microphotograph of the Ka-band RF-pulse former.

Fig. 6.14 shows the simulated and measured insertion loss/gain, input and output return losses, and isolation of the ka-band RF-pulse former under small signal conditions. The measured results show that, around the design frequency of 35 GHz, the RF-pulse former exhibits an ultra-high-isolation performance, hence extremely low RF leakage, while consuming a DC current of only 7.3 mA from a 1.8-V source. From 31 to 37.1 GHz, the loss/gain is from -1.9 dB (loss) to 1.1 dB (gain), the input return loss is from 14.5 to 30 dB. The output return loss is higher than 10 dB from 33 to 35.9 GHz.

From 30 to 40 GHz the isolation is higher 40 dB and, especially at 34 GHz, the isolation reaches 70 dB along with the gain of 1.1 dB. At 35 GHz, the RF-pulse former exhibits a gain of 1.05 dB and a very high isolation of 57 dB.

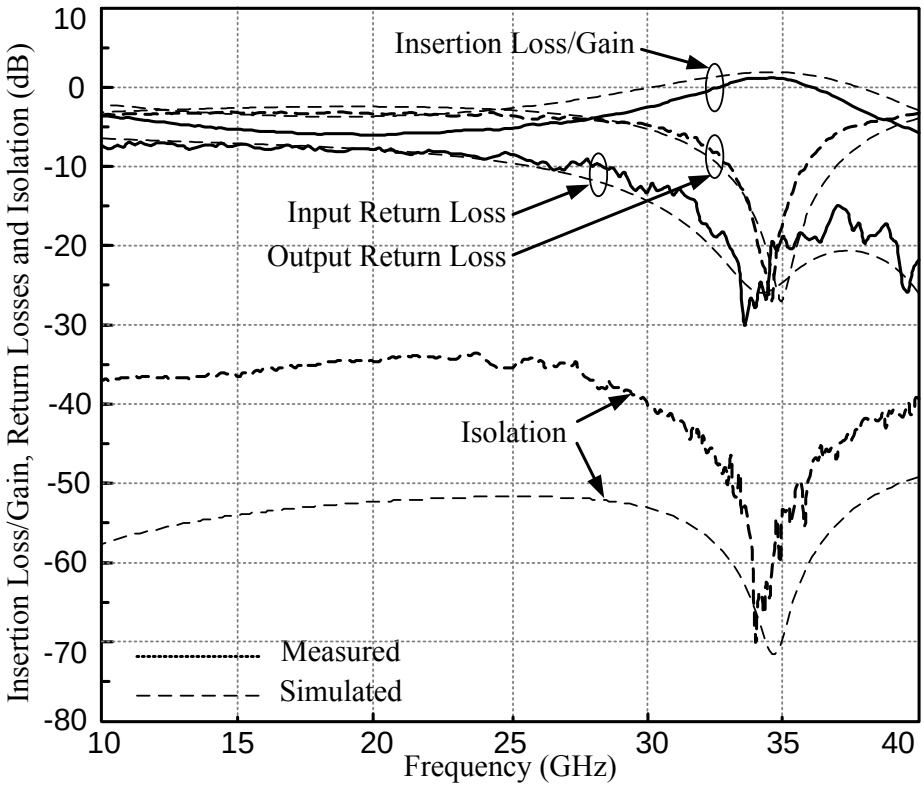


Fig. 6.14. Simulated and measured insertion loss/gain, return losses and isolation of the Ka-band RF-pulse former.

While the measured and simulated results of the insertion loss/gain, and input and output return losses are in good agreement from 10 to 40 GHz, the simulated isolation result shows more than 10-dB difference with the measured one, except in the narrow frequency range of 33-35 GHz. The difference in isolation is mainly due to the imbalance of the fabricated active balun and the inaccuracy of the models for the passive

elements and active devices. The measured input 1-dB compression point is -6 dBm. This power handling is enough for some applications with a following power amplifier used to amplify the RF-pulses.

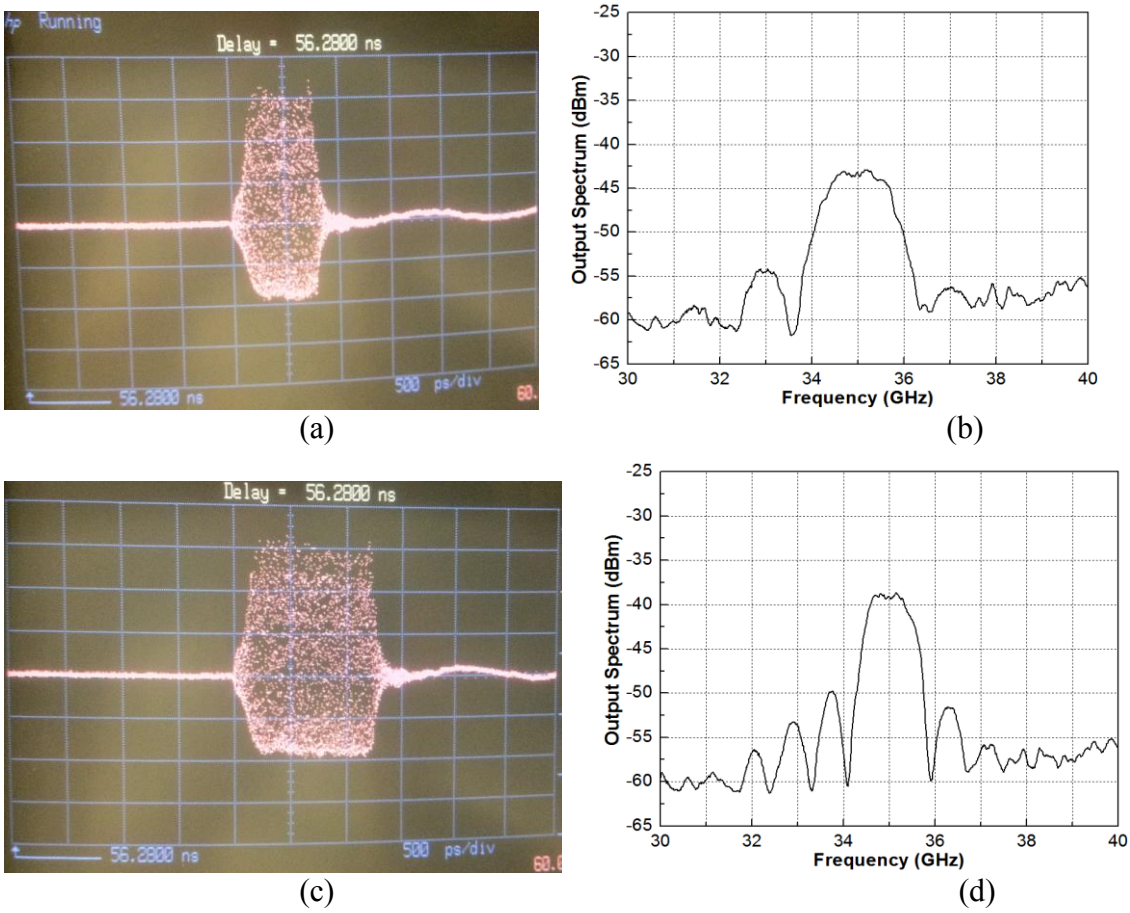


Fig. 6.15. Measured 35-GHz RF-pulses and their spectrums: 0.8-ns RF-pulse (a) and its spectrum (b), and 1.3-ns RF-pulse (c) and its spectrum (d).

The switching time of the RF-pulse former was measured based on the RF-pulse's envelope observed on the digital oscilloscope HP 54124T. The 35-GHz CW signal is gated by the control impulses generated from the impulse generator at the pulse

repetition frequency of 100 KHz. The inverters integrated in the RF-pulse former sharpen the rising and falling edges of control impulses, hence eliminating external effects, such as measurement cables and bonding wires, to the switching speed of the RF-pulse former which is mainly determined by the small gate resistor and gate-source capacitor of the MOSFET transistors. The envelope of the 35-GHz RF pulses at the output of the RF-pulse former can be clearly seen on the digital oscilloscope triggered by the trigger signal produced from the impulse generator.

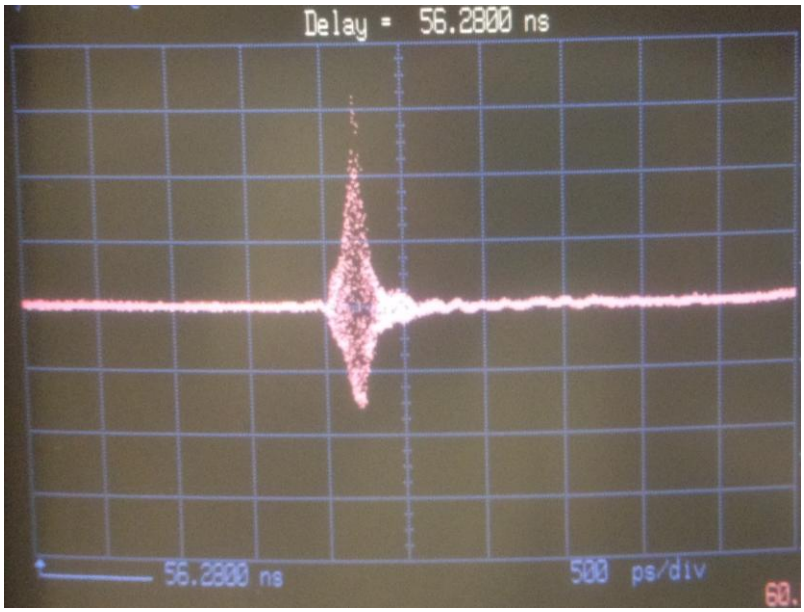


Fig. 6.16. Measured 200-ps RF pulse.

Fig. 6.15 shows the measured 0.8 and 1.3-ns RF-pulses and their spectrums. There is no RF leakage seen from the measured spectrums; the leakage, if any, is smaller than the magnitude of the actual RF-pulse, which demonstrates the ultra-high isolation of the RF-pulse former. From Figs. 6.15(a) and (b), the 10%-90% rising time and 90%-10%

falling time of the RF-pulse former are determined to be 136 ps and 70 ps, respectively. The total measured switching time of 206 ps is 26 ps larger than the simulated result due to the delay in the inverters. The small switching time of 206 ps allows the RF-pulse former to produce very narrow RF-pulses for high resolution radar and high-data-rate communication systems. Fig. 6.16 shows the measured 200-ps RF pulse, demonstrating the possibility of generating very narrow pulses.

Similar RF-pulse shapes and a minimum RF-pulse width of 300 ps are obtained from the measurement for the RF-pulse former using the control impulse produced from the designed CMOS impulse generator.

K-band RF-pulse Former

The design of K-band RF-pulse former is similar to that of Ka-band. The schematic of the 24.5-GHz switch is the same as one shown in Fig. 6.12. The active balun, and output and input matching networks are optimized at 24.5 GHz. Table 6.5 lists all designed circuit elements and their values for the K-band RF-pulse former. The microphotograph of the K-band RF-pulse former is shown in Fig. 6.17 with the chip area of 600 x 500 μm^2.

Fig. 6.18 shows the simulated and measured insertion loss/gain, input and output return losses, and isolation of the K-band RF-pulse former under small signal conditions. The measured results show that, around the design frequency of 24.5 GHz, the RF-pulse former exhibits an ultra-high-isolation performance, hence extremely low RF leakage, while consuming a DC current of only 7.3 mA from a 1.8-V source. From 18.5 to 27.6

GHz, the loss is from -3 dB to 0 dB, the input return loss is from 11.6 to 25.5 dB. The output return loss is higher than 10 dB from 23.2 to 26.3 GHz. From 10 to 40 GHz the isolation is higher 40 dB and, especially at 24.4 GHz, the isolation reaches 71 dB along with the insertion loss of 0 dB.

Table 6.5 K-band RF-pulse former circuit elements and values

T_1		64 μm gate width	
T_2		80 μm gate width	
Q_1, Q_2		0.15 x 8.28 μm^2 emitter area	
L_{e1}, L_{e2}	176.6 pH	L_{mi}	312 pH
L_b	215 pH	C_{mi}	140 fF
R_g	400 Ω	L_{mo}	400 pH
V_{DD}	1.8 V	C_{mo}	175 fF

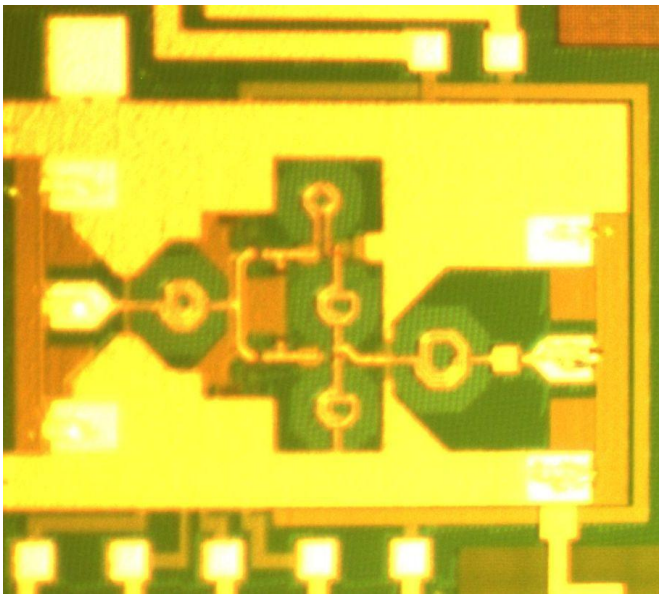
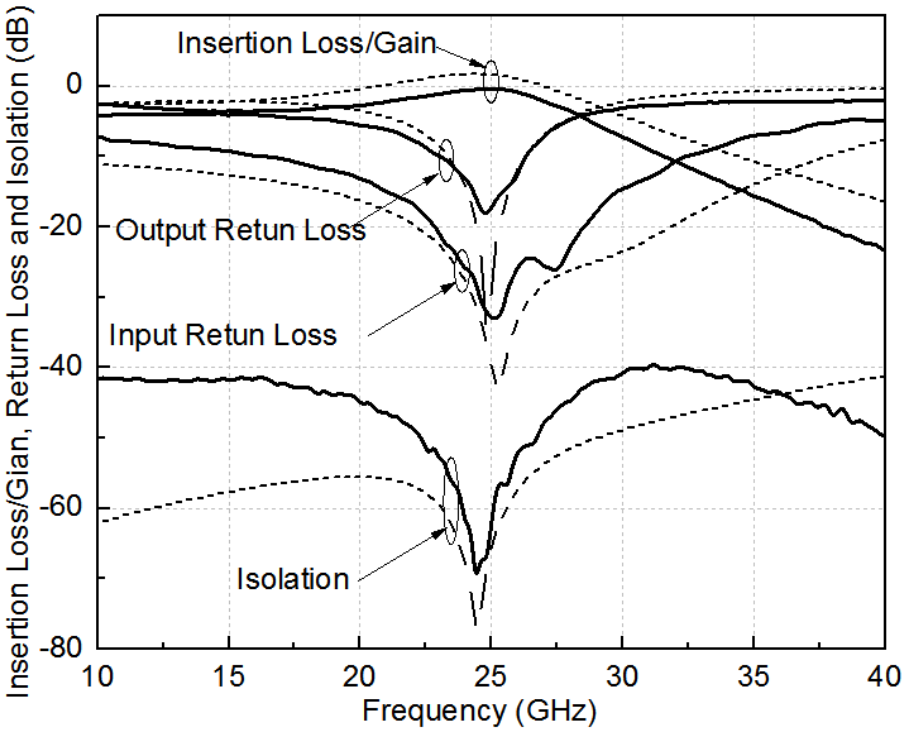


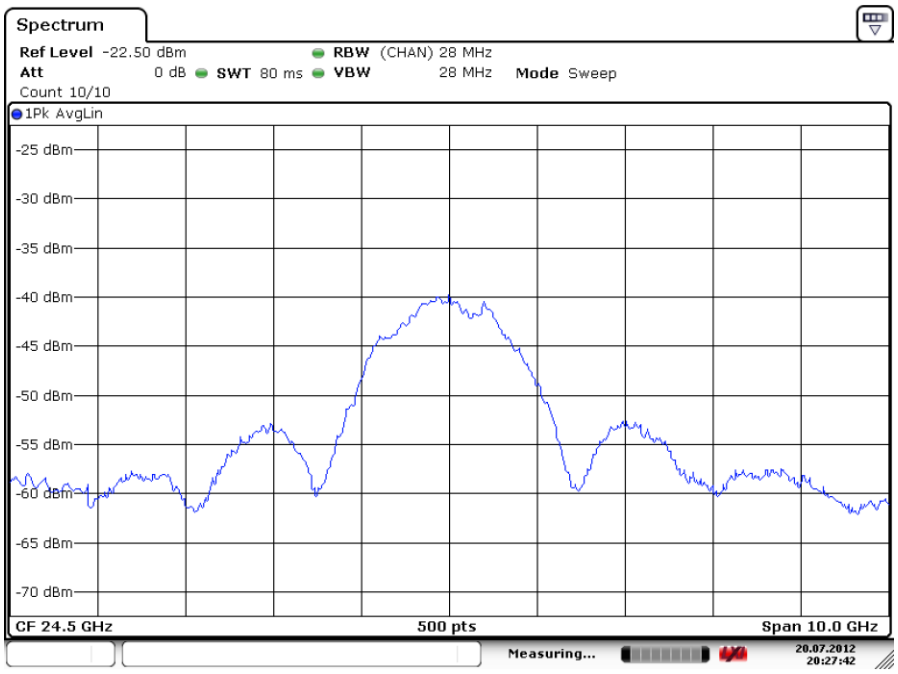
Fig. 6.17. Microphotograph of the K-band RF-pulse former.



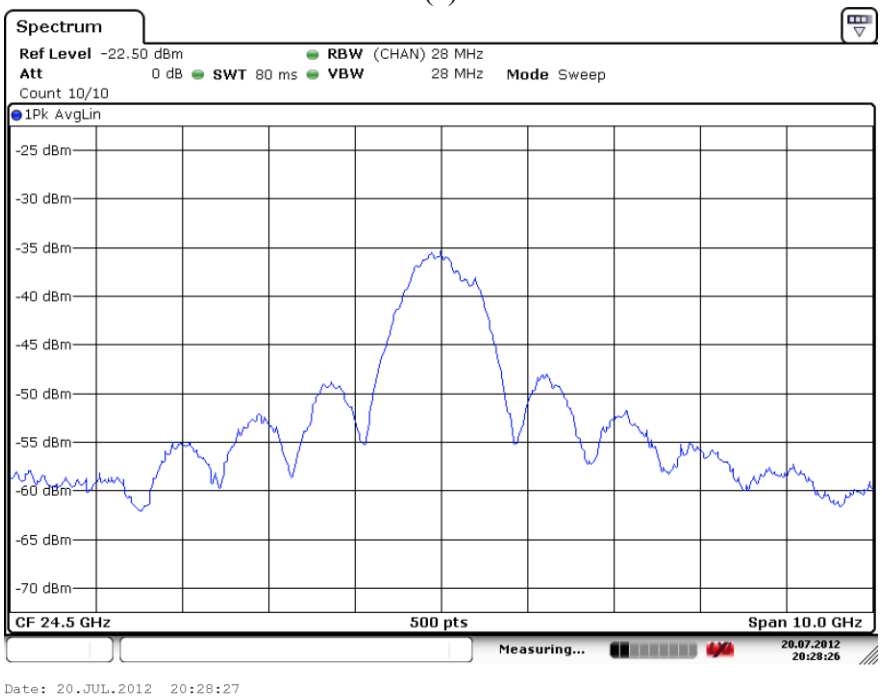
(a) (b)

Fig. 6.18. Simulated and measured insertion loss/gain, return losses and isolation of the K-band RF-pulse former.

While the measured and simulated results of the insertion loss, and input and output return losses are in good agreement from 10 to 40 GHz, the simulated isolation result shows more than 10-dB difference with the measured one in the frequency range below 20 GHz. The difference in isolation is mainly due to the imbalance of the fabricated active balun and the inaccuracy of the models for the passive elements and active devices. The measured input 1-dB compression point is -4 dBm. This power handling is enough for some applications with a following power amplifier used to amplify the RF-pulses.



(a)



(b)

Fig. 6.19. Measured spectrums of 0.8-ns (a) and 1.3-ns (b) RF-pulses at 24.5-GHz. The RF-pulse envelops are shown in Fig. 6.7 (a) and (c).

The RF-pulse, switching time and RF-pulse spectrums have been measured in the same way done with the Ka-band RF-pulse former. The measured envelops of 0.8- and 1.3-ns RF-pulses are as shown in Fig. 6.15 (a) and (c). The 10%-90% rising time of 136 ps and 90%-10% falling time of 70 ps are also obtained. As expected, the switching times of the RF-pulse formers do not depend on the RF signal frequency. Fig. 6.19 shows the measured spectrums of 0.8-ns and 1.3-ns RF-pulses at 24.5 GHz.

6.3.5 Active Combiner

As shown in Fig. 6.20, the active combiner is used to combine two RF-pulse chains at 24.5- and 35-GHz bands from K- and Ka-band RF-pulse formers and feed the composite signal into the concurrent dual-band power amplifier. The active combiner is used instead of passive combiner to provide gain to the composite signal, hence functioning as a dual-band drive amplifier for the dual-band power amplifier. The high port-to-port isolation of the active combiner minimizes the inter-band interference for the transmitter as well.

The active combiner, as shown in Fig. 6.20, consists of two common source amplifiers (Q_1 and Q_2) and a common base amplifier (Q_3). The input ports 1 and 2 are used for the 24.5- and 35-GHz RF-pulse chains, respectively. Two RF pulse chains are amplified by two common emitter amplifiers then combined in the common base amplifier. The dual-band output signal is at the port 3. L_{e1} and L_{e2} are used to increase the linearity for two common source amplifiers. Two input matching networks (L_{m1}, C_{m1}) and (L_{m2}, C_{m2}) are used to match the RF-pulse former outputs to the inputs of two

common source amplifiers at 24.5 and 35 GHz. The output loading network including L_c, R_c and C_o are optimized to provide good matching with 50 Ω which is the input impedance of the concurrent dual-band PA presented in Chapter V. The sizes of transistors and bias currents are optimized so that the active power combiner provides at least -3 dBm output power for each band to drive the dual-band PA into the saturated region. Table 6.6 shows the circuit elements and their values of the active combiner.

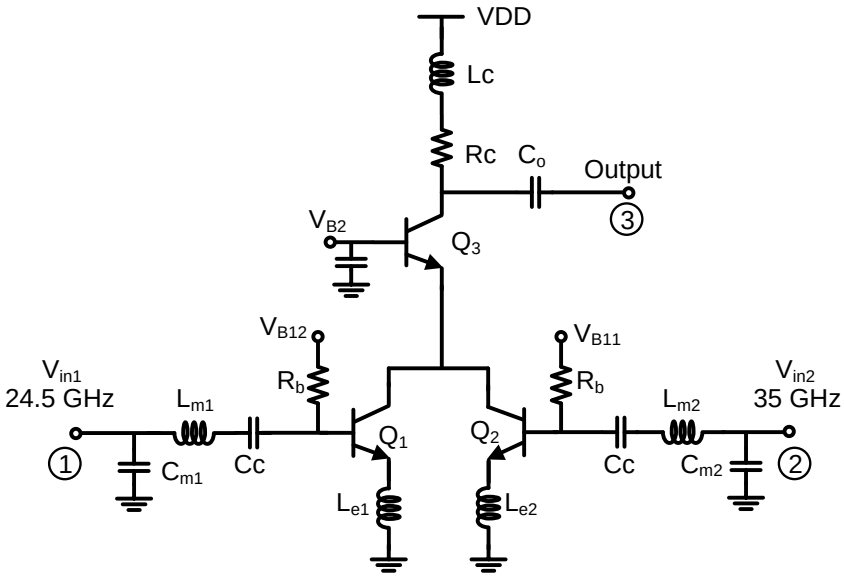


Fig. 6.20. The active combiner schematic.

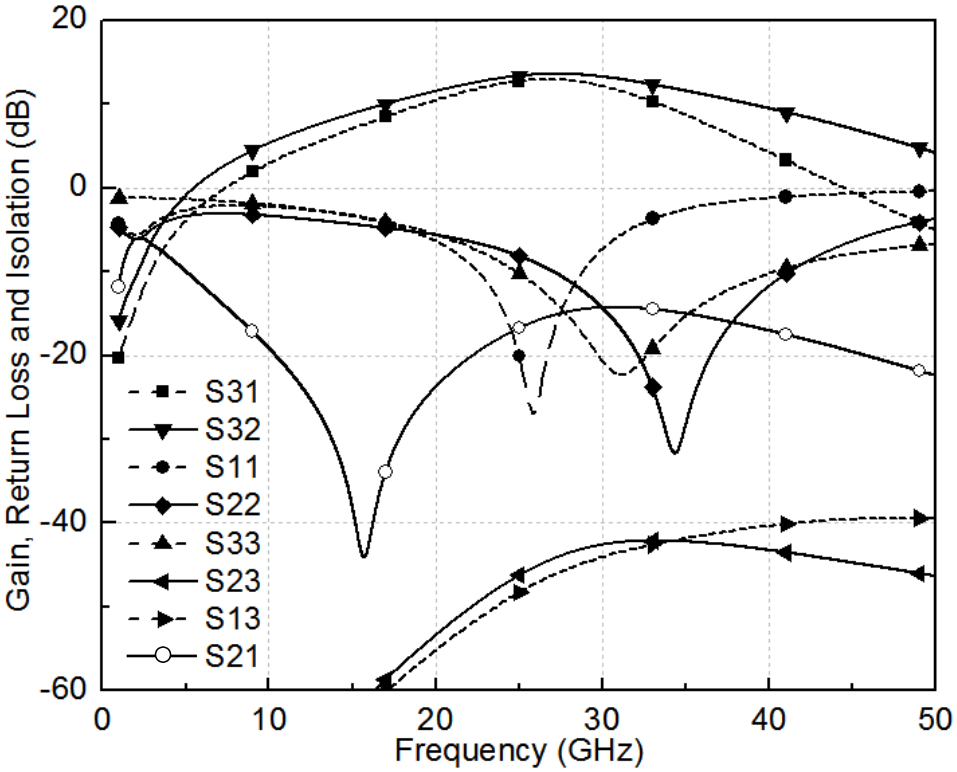


Fig. 6.21. Simulated gain, return loss and isolation of the active combiner.

Table 6.6 Active combiner circuit elements and values

Q_1, Q_2		0.15 x 10.16 μm^2 emitter area	
Q_3		0.15 x 20.32 μm^2 emitter area	
L_{e1}, L_{e2}	40 pH	C_{m2}	93 fF
R_b	2 KΩ	R_c	15 Ω
R_g	400 Ω	L_c	200 pH
Cc	1 pF	C_o	200 fF
L_{m1}	327 pH	V_{DD}	2.4 V
C_{m1}	140 fF	VB_2	1.8V
L_{m2}	141 pH	I_{bias}	18 mA

The simulated results shown in Fig. 6.21 show that the gains of the active combiner are 11.8 dB and 11.5 dB, the input return losses are 20 dB and 28 dB, and the output return losses are 10 and 15.2 dB at 24.5- and 35-GHz band, respectively. The port isolations are higher than 17 dB. The simulated results also show that the 1-dB output powers are -2 and -2.5 dBm at 24.5 and 35 GHz, respectively, which meet the requirement for driving the subsequent dual-band PA.

6.4 Concurrent Dual-band Transmitter Integration and Simulation

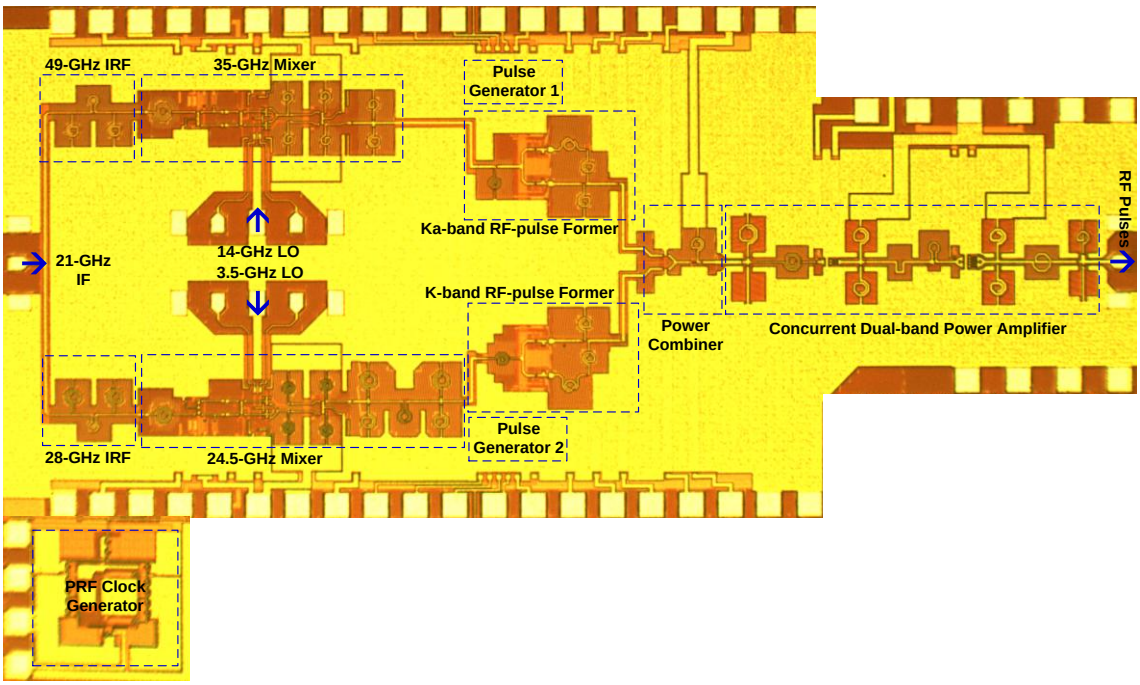


Fig. 6.22. Concurrent dual-band transmitter microphotograph. Total chip area is 7.9 mm^2 (including pads).

All constitute circuits for the transmitter shown in Fig. 6.2 have been designed and some of them have been individually measured. In this section, the complete concurrent dual-band transmitter that was integrated, simulated, optimized, laid out, fabricated and measured is described.

The whole transmitter is optimized to have high gain, high output powers and high harmonic/inter-modulation products suppression. The matching between building blocks are optimized to get high gain for the transmitter. The transmitter is laid-out as symmetric as possible. To facilitate on-wafer measurement, two differential LO signal pads are located inside the transmitter chip and all DC bias pins are around the chip.

Fig. 6.22 shows the microphotograph of the concurrent dual-band transmitter integrated from individual circuits presented in previous chapters and sections. The transmitter has a single-ended 21-GHz IF port, two differential LO ports at 3.5 and 14 GHz and one single-ended dual-band RF output port. In the dual-band mode measurement, four RF probes are used for one IF input, two LO and one RF output ports.

The harmonic balance simulation is used to simulate the whole transmitter gains and output powers for 24.5- and 35-GHz bands in single and dual band modes. The two 3.5- and 14-GHz LO signal powers are set to -2 and 0.6 dBm, respectively, based on the measured results of the mixers presented in Chapter II. Two RF-pulse formers for two bands are controlled to be on or off using two control signals generated from impulse generators. The 21-GHz IF input power is swept from -70 to -30 dBm during the simulation. Gains for 24.5 and 35-GHz bands are defined as

$$\text{24.5-GHz-band gain} = \frac{\text{24.5-GHz RF output power}}{\text{21-GHz IF input power}}$$

$$\text{35-GHz-band gain} = \frac{\text{35-GHz RF output power}}{\text{21-GHz IF input power}}$$

In the dual-band mode, two bands are on or off concurrently. Fig. 6.23 shows the simulated gains and output powers of the transmitter versus IF input power in the dual-band mode when two bands are on. Simulation results in Fig. 6.23 show that the transmitter exhibits the gains of 50 dB for both bands and the maximum output powers, P_{out_max}, of 13.2 and 11.3 dBm for 24.5- and 35-GHz bands, respectively. In order to maximize the output power for two bands, an input IF power of -32 dBm is used. Fig. 6.24 shows the simulated output spectrum of the transmitter in the dual-band mode when two bands are on and the 21-GHz IF input power is -32 dBm. It can be seen that the output spectrum contains two main tones at 24.5 and 35 GHz with the powers of 13.2 and 11.3 dBm, respectively, and other harmonics and inter-modulation products with powers of 35 dB lower than those of the two main tones. The maximum output powers of the transmitter in the dual-band mode meet the design specification. It is noted that the output powers of the transmitter for two bands are optimized concurrently through using the dual-band matching network technique for the dual-band power amplifier.

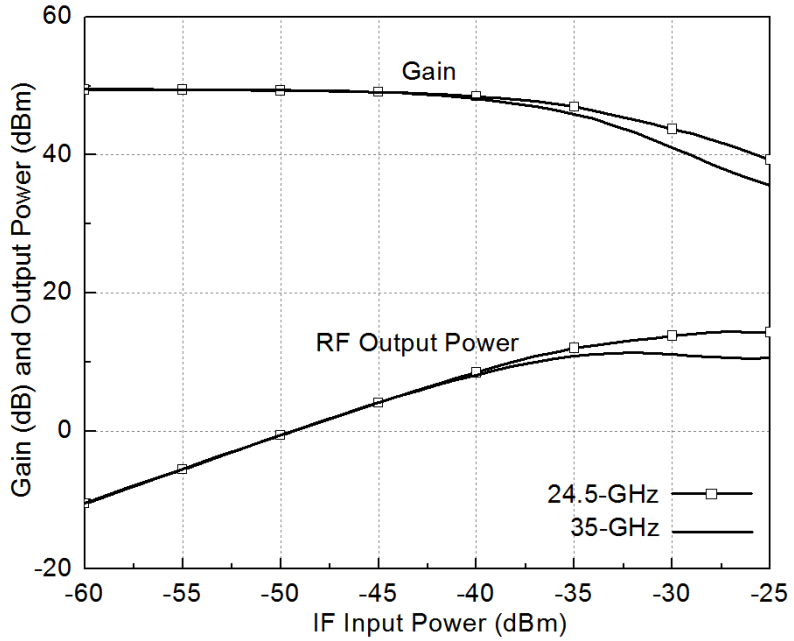


Fig. 6.23. Transmitter gain and output power in the dual-band mode. Two bands are on.

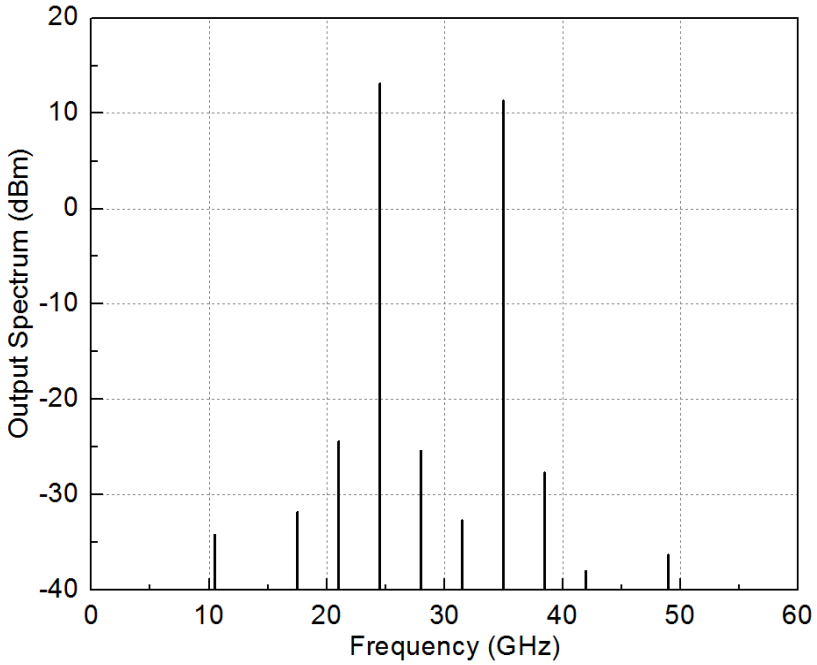


Fig. 6.24. Transmitter output spectrum in the dual-band mode. Two bands are on and IF input power is -32 dBm.

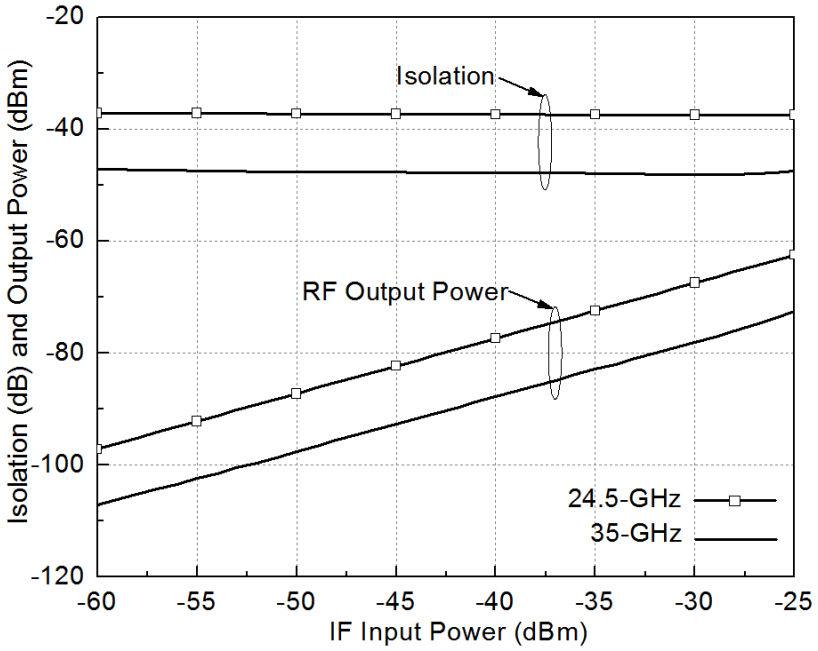


Fig. 6.25. Transmitter gain and output power in the dual-band mode. Two bands are off.

Fig. 6.25 shows the simulated isolations and RF leakage output powers of the transmitter in the dual-band mode when two bands are off versus the IF input power. Simulation results in Fig. 6.25 show that the transmitter exhibits isolations of 37 and 46 dB, and leakage output powers of -71 and -80 dBm for the 24.5- and 35-GHz bands, respectively, at an input IF power of -32 dBm. Fig. 6.26 shows the simulated leakage output spectrum of the transmitter in the dual-band mode when two bands are off and the 21-GHz IF input power is -32 dBm. It can be seen that the leakage output powers of the two main tones are -71 and -80 dBm, respectively, and the leakage powers of other frequency components are lower than -78 dBm. The low RF leakage powers demonstrate the RF leakage cancellation technique used in the RF-pulse formers. If the isolation of the T/R switch is assumed as 25 dB then the RF leakage power from the transmitter

available at the receiver front-end are -96 and -105 dBm at 24.5 and 35-GHz bands, respectively, which are all much smaller than the sensitivity of the receivers of -80.5 dB listed in Table 6.1. This demonstrates the possibility of using one antenna system for the transmitter and receiver.

In the single-band mode, one band is operating at one time. Fig. 6.27 shows the simulated gains and output powers of the transmitter versus the IF input power in the single-band modes when the bands are on. Simulation results in Fig. 6.27 show that the transmitter in the single-band modes exhibits the gains of 50 dB for both bands and the maximum output powers, P_{out_max}, of 16.5 and 17 dBm for the 24.5- and 35-GHz bands, respectively. In order for the transmitter to operate at the output powers of higher than 16 dBm in the single-band modes, the working input IF power of -28 dBm is selected. Fig. 6.28 (a) and (b) show the simulated output spectrums of the transmitter in the 24.5 and 35-GHz single-band modes with the bands on and the IF input power of -28 dBm. It can be seen that the output spectrum for each band contains the corresponding main tone at 24.5 or 35 GHz with the powers of 16.4 or 16.2 dBm, respectively, and other harmonics and inter-modulation products with the powers of 32 and 48 dB lower than that of the main tones. The simulated isolations and leakage output powers of the transmitter in the single-band modes with the bands off versus the IF input power are the same as those in the dual-band mode as shown in Fig. 6.25.

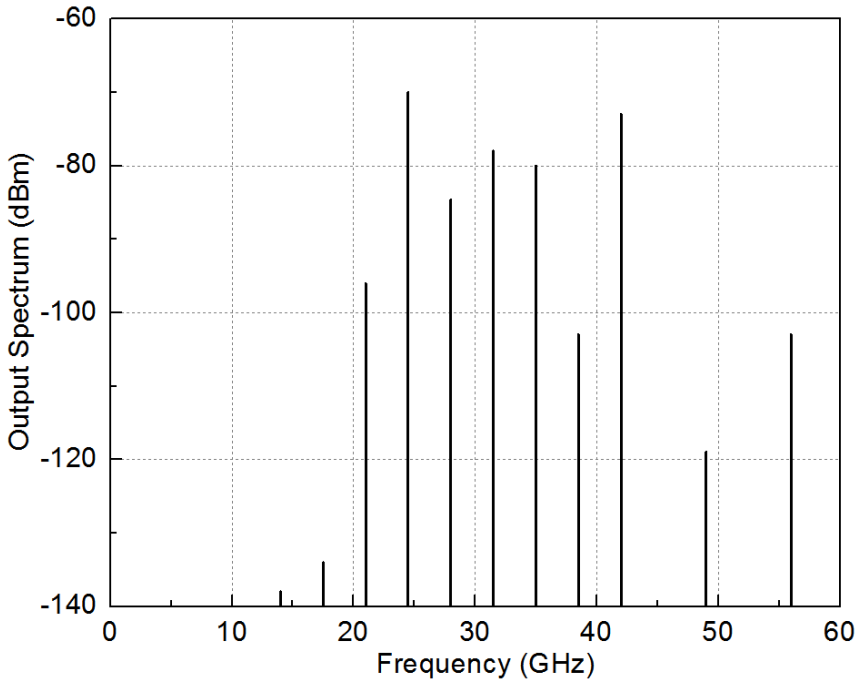


Fig. 6.26. Transmitter output spectrum in the dual-band mode. Two bands are off and the IF input power is -32 dBm.

Table 6.7 shows the simulated performance of the transmitter in the dual-band and single-band modes. It is interesting to calculate the on/off isolation of the transmitter in each band which is defined as the difference between the maximum transmitting output power when the transmitter is on and the RF leakage power when the transmitter is off at the same IF input power. High on/off isolations of transmitters are desirable for high dynamic range of radar and communication systems. The simulated results show that the on/off isolations of the designed transmitter are 84.2 and 91.3 dB for 24.5 and 35-GHz bands, respectively, in the dual-band mode, and 87.5 and 97 dB for 24.5 and 35-GHz bands, respectively, in the single-band mode. The ultra-high on/off isolation is

obtained due to the deployment of RF leakage cancellation technique for RF pulse formers.

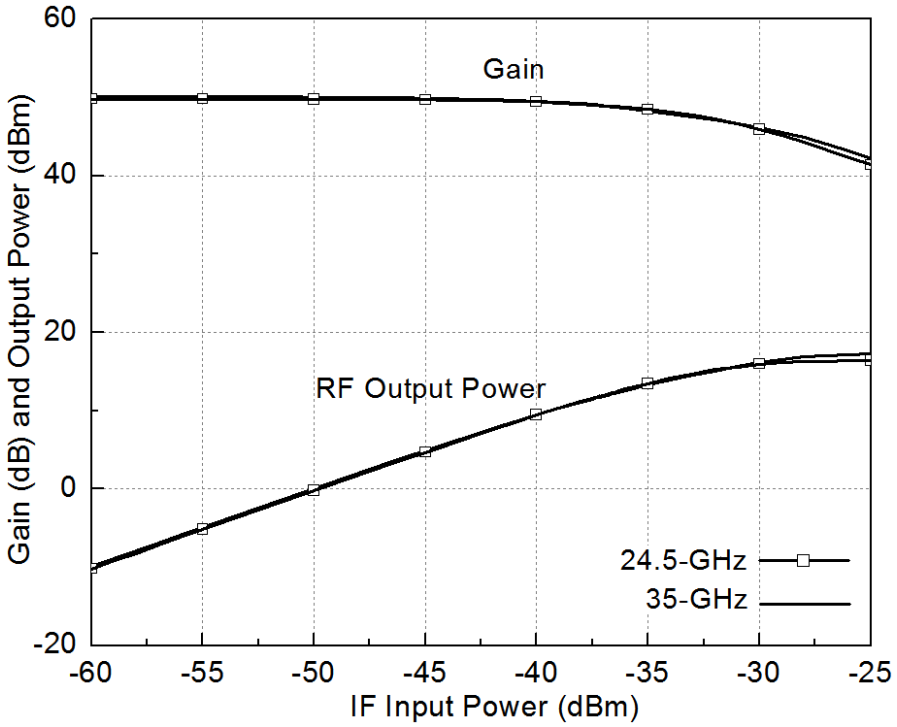
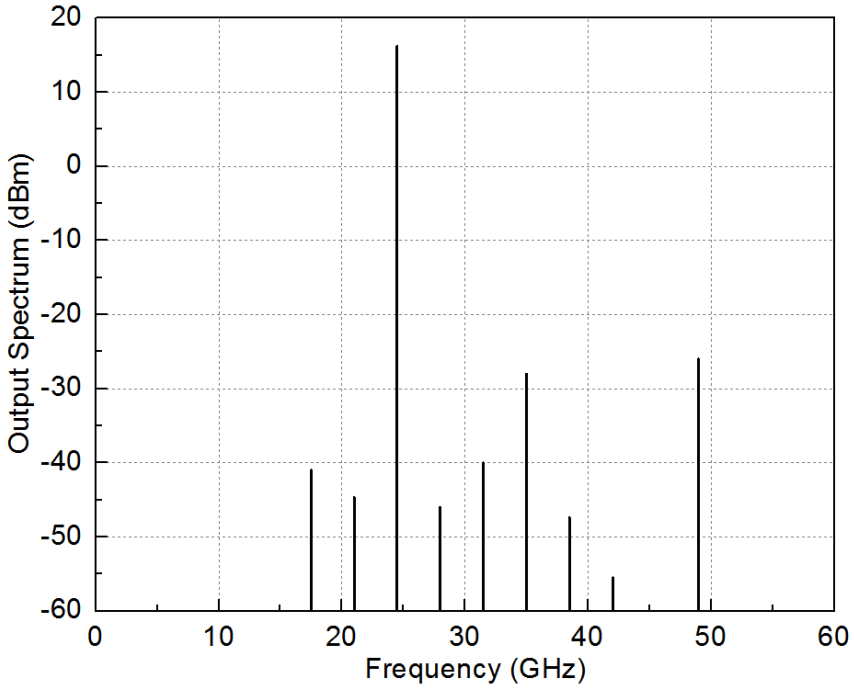
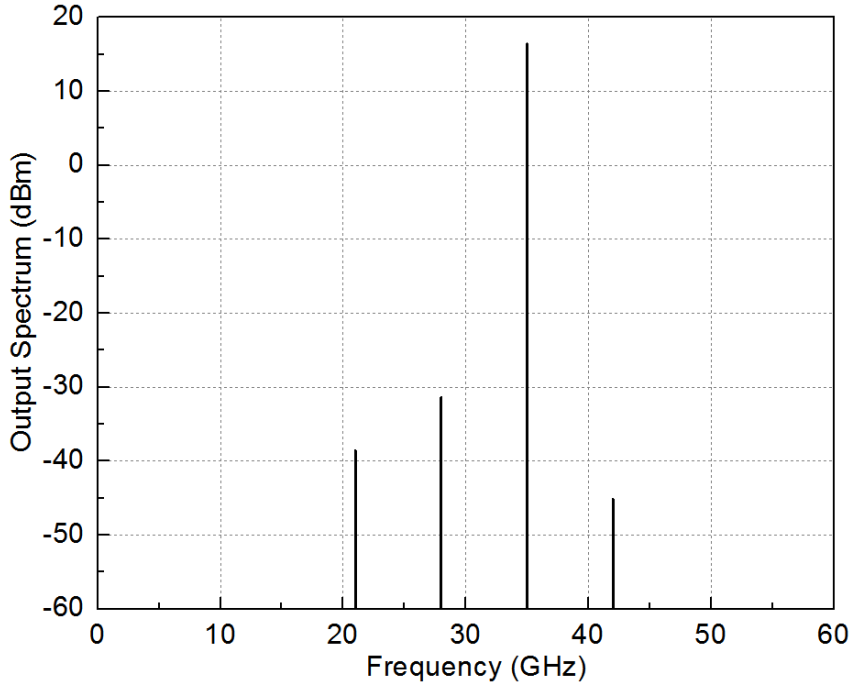


Fig. 6.27. Transmitter gain and output power in the 24.5 and 35-GHz single-band modes. Two bands are on.

Performance of the whole transmitter for all bands and operating modes summarized in the Table 6.7 and presented in previous sections such as achieved RF-pulse widths meet the design specifications listed in Table 6.2.



(a)



(b)

Fig. 6.28. Transmitter output spectrum in single-band mode with the IF input power of -28 dBm. 24.5-GHz band is on (a) and 35-GHz band is on (b).

Table 6.7 Simulated transmitter performance summary

			24.5-GHz band		35-GHz band	
Operation mode	24.5-GHz band	35-GHz band	Gain/ Isolation	P_{out_max}	Gain/ Isolation	P_{out_max}
Dual-band	On	On	50	13.2	50	11.3
	Off	Off	-37	-71	-46	-80
Single-band	On	Off	50	16.5	-46	-80
	Off	On	-37	-71	50	17

CHAPTER VII

CONCLUSION

7.1 Dissertation Summary

High demand for numerous wireless applications and advancement of technologies have pushed the operating frequencies of advanced radar and communication systems to MMW regime along with challenges in circuit designs for system performance enhancement. In this dissertation, several novel techniques and RFIC circuit architectures exhibiting unprecedented performance have been proposed and validated, demonstrating potentially significant improvement for MMW radar and communication systems. In addition, the design of an advanced, low-cost and miniature millimeter-wave concurrent dual-band transmitter for short-range, high-resolution radar and high-rate communication systems has been presented.

Novel active balun topologies have been proposed and analyzed, revealing their ultra-wideband balance characteristics. The active baluns combine the CE and CC amplifiers with neutralized and compensated parasitic components to maintain their balances across extremely wide bandwidths. The proposed baluns implemented on a 0.18-μm SiGe BiCMOS process exhibit good balance from DC to 50 GHz while consuming a very low DC power. Simple structure, ultra-wideband balance, independence of input and output loads, well-balance capability at high frequencies, high linearity, less amplitude- and phase-imbalance variation over bias currents, low power consumption, and straightforward design procedure are the remarkable characteristics of

the new active baluns, making them attractive for use in RF and millimeter wave transceiver systems.

A new RF switch architecture possessing ultra-high isolation and possible gain has been presented. The RF signal leakage cancellation technique implemented using the active balun has also been demonstrated, revealing useful characteristics of enhancing the switch isolation, besides providing some possible gain. A simple graphical technique for selecting optimum transistors for the series-shunt SPST switch was also described. The newly designed RF switch based on a 0.18-μm BiCMOS technology validates the new RF switch architecture with unprecedented performance across 10 to 38 GHz. Particularly, within the narrower band around 35.5-38.5 GHz, its isolation reaches ultra-high value of 70 dB. The new RF switch architecture, through its analysis and results, demonstrates that extremely high isolation is possible for RF switches such as SPST and T/R switches, etc. in the microwave and millimeter-wave regions and, hence, is very attractive for communication and radar systems as it alleviates the performance limitation of these systems hampered by the limited switching isolation.

New concurrent dual-band impedance-matching networks and their design methodology have been presented together with a 25.5/37-GHz concurrent dual-band PA. Each of the concurrent dual-band matching networks is synthesized from two single-band matching networks. They can be used to achieve not only concurrent matching between two arbitrary loads and two arbitrary sources at any dual-band frequencies, but also suppression of the harmonics and IMPs. The reported lumped-element dual-band matching networks are especially attractive for on-chip realization for

RFICs. Various other dual-band matching networks using lumped elements, transmission lines, or their combination can be developed based on those derived in this paper. The presented matching technique can also be implemented to derive concurrent multi-band matching networks having more than two bands. The designed concurrent dual-band PA produces good performance for both single mode and dual mode at 25.5 and 37 GHz with well dual-band shaped gain and capability of harmonic/IMP suppression resulting in improved linearity. The concurrent dual-band matching technique through its successful implementation for a concurrent dual-band PA design implicitly demonstrates that multi-band components, such as PA, low-noise amplifier, mixer, etc., can be designed relatively easy, facilitating the design of modern multiband/multimode communication and radar systems that have many benefits.

Development of low-power BiCMOS time-gated based RF-pulse formers has been presented. The K- and Ka-band RF-pulse formers exhibit capability of producing very narrow RF pulses in sub-nanosecond with extremely low RF leakage. Gain of 1.1 dB, high isolation up to 70 dB, rising time of 136 ps, falling time of 70 ps, and very narrow RF pulses of 200 ps have been measured. These unprecedented characteristics make the developed RF-pulse formers attractive for improving the cost and performance of microwave and millimeter-wave short-range high-data-rate communications and high-resolution radar systems.

The complete transmitter exhibiting unique characteristics obtained from capabilities of producing very narrow and tunable RF pulses with extremely RF leakage and working concurrently in dual bands at 24.5 and 35 GHz was designed. The

developed RF-pulse formers and concurrent dual-band power amplifier are used. The generation of narrow and tunable RF pulses using CMOS tunable sub-nanosecond impulse generators allows the radar system to flexibly work at high and multiple range resolutions. The extremely low RF leakage achieved with using the RF leakage cancellation technique allows the transmitter to share one antenna system with receiver, turn on the PA at all time, comply possible transmitting spectrum requirements, increase the system dynamic range, avoid harm to other systems; hence improving system size, cost and performance. High data-rate in communication systems and high resolution in radar systems are achieved as the consequence of transmitting very narrow RF pulses at high rates. In addition, the dissertation demonstrated a design approach for low chip-area, cost and power consumption systems in which a single dual-band component (power amplifier) is designed to operate with two RF signals simultaneously. The designed transmitter allows the radar system to detect targets from 0.15 to 12.4 and 14.7 m in range for 35-GHz and 24.5-GHz bands in the dual-band and single-band mode, respectively, with the range resolution of 15 cm. The developed concurrent dual-band transmitter can be used for numerous cost-effective and multi-functionality applications such as short-range high-data-rate communications, automotive radar, sensing, imaging, personnel and item tracking, and RFID.

REFERENCES

[1] Federal Communications Commission (FCC), "Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," First Report and Order, ET Docket 98-153, FCC 02-48; Adopted: February 2002; Released: April 2002.

[2] *High Rate Ultra Wideband PHY and MAC Standard*, Dec. 2005, ECMA standard 368.

[3] R. Xu, Y. Jin, and C. Nguyen, "Power-efficient switching-based CMOS UWB transmitters for UWB communications and radar systems," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3271–3277, Aug. 2006.

[4] L. Smaini, C. Tinella, C. Stoecklin, L. Chabert, C. Devaucelle, R. Cattenoz, and D. Belot, "Single-chip CMOS pulse generator for UWB systems," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1551–1561, Jul. 2006.

[5] D. Zito et al., "SoC CMOS UWB pulse radar sensor for contactless respiratory rate monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol.5, no. 6, pp. 503–510, 2011.

[6] B. Razavi, T. Aytur, C. Lam, F.-R. Yang, K.-Y. Li, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A UWB CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2555–2562, Dec. 2005.

[7] A. Ismail and A. Abidi, "A 3.1- to 8.2-GHz zero-IF receiver and direct frequency synthesizer in 0.18-μm SiGe BiCMOS for mode-2 MB-OFDM UWB

communication," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2573–2582, Dec. 2005.

[8] A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez, and E. Sanchez-Sinencio, "An 11-band 3–10 GHz receiver in SiGe BiCMOS for multiband OFDM UWB communication," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 935–948, Apr. 2007

[9] C. Shannon, "A Mathematical Theory of Communication," *The Bell System Technical Journal*, vol. 27, pp. 379-423, 623-656, July-October 1948.

[10] IEEE 802.15 Working Group for WPAN; http://www.ieee802.org/15/.

[11] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *IEEE Commun. Mag.*, vol. 40, pp. 140-147, Jan. 2002.

[12] I. Gresham *et al.*, "Ultra-wideband radar sensors for short-range vehicular applications," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 9, pp. 2105–2122, Sep. 2004.

[13] J. Wenger, "Automotive radar-status and perspectives," in *Proc. IEEE Compound Semiconductor Integrated Circuit Symp.*, Oct. 2005, pp. 21–25.

[14] M. Skolnik, Introduction to Radar Systems, McGraw-Hill, 3rd ed., New York, NY, 2002.

[15] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, Y. Wang, and A. Hajimiri, "A 77-GHz phased array transmitter with local LO-path phase shifting in silicon," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 182–183.

[16] Rui Xu, "CMOS Integrated Circuit Design For Ultra-Wideband Transmitters and Receivers", *PhD. Dissertation, Texas A&M Univ.,* August 2009.

[17] Razavi, *RF Microelectronics,* Prentice Hall, Upper Saddle River, NJ**,** 1998.

[18] John Roger, Calvin Plett, *Radio Frequency Integrated Circuit Design*, Artech House, Norwood, MA, 2003.

[19] K. Leong and R. G. Meyer, "Monolithic RF active mixer design," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 231–239, Mar. 1999.

[20] K. L. Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, pp. 548–555, Apr. 1998.

[21] Jazz Semiconductor, 4321 Jamboree Road, Newport Beach, CA 92660.

[22] IE3D. Zeland Softw. Inc., Fremont, CA, 2005.

[23] Cadence Design Systems, Inc., 2655, Seely Avenue, San Jose, CA 95134.

[24] C. Viallon, D. Venturin, J. Graffeuil, and T. Parra, "Design of an original K-band active balun with improved broadband balanced behavior,"*IEEE Microw. Wireless Compon. Lett*., vol. 15, no. 4, pp. 280–282, Apr. 2005.

[25] Andy C. Chen, Anh-Vu Pham, and Robert E. Leoni III, "Development of low-loss broad-band planar baluns using multilayered organic thin films,"*IEEE Trans. Microw. Theory Tech*., vol. 53, no. 11, pp. 3648–3655, Nov. 2005.

[26] Austin Ying-Kuang Chen, Yves Baeyens, Young-Kai Chen, and Jenshan Lin, "An 80 GHz High Gain Double-Balanced Active Up-Conversion Mixer Using

0.18 μm SiGe BiCMOS Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 6, pp. 326–328, Jun. 2011.

[27] J. Wang, W. J. Zhang, and Z. P. Yu, "The design of a planar-spiral transformers balun used in RF/MW based on 0.13 m CMOS process," in *Int. Microw. Millimeter Wave Technol. Conf.,* Apr. 2007, pp. 1–4.

[28] M. E. Goldfarb, J. B. Cole, and A. Platzker, "A novel MMIC biphase modulator with variable gain using enhancement-mode FET's suitable for 3 V wireless applications," in *IEEE Microw. Millimeter-Wave Monolithic Circuits Symp., Dig.*, May 1994, pp. 99–102.

[29] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[30] H. Ma, S. J. Fang, F. J. Lin, and H. Nakamura, "Novel Active Differential Phase Splitters in RFIC for Wireless Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2597-2603, Dec. 1998.

[31] Hsi-Han Chiang, Fu-Chien Huang, Chao-Shiun Wang and Chorng-Kuang Wang "A 90 nm CMOS V-Band Low-Noise Active Balun With Broadband Phase-Correction Technique", *IEEE J. Solid-State-Circuits*, vol. 46, no. 11, pp. 2583-2591, Nov. 2011.

[32] B. J. Huang, B. J. Huang, K. Y. Lin, and H. Wang, "A 2–40 GH active balun using 0.13 m CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 3, pp. 164–166, Mar. 2009.

[33] C. Viallon, D. Venturin, J. Graffeuil, and T. A. Parra, "Design of an original K-band active balun with improved broadband balanced behavior," *IEEE Microw. Wireless Compon. Lett*., vol. 15, no. 4, pp.280–282, Apr. 2005.

[34] Shou-Hsien Weng, Hong-Yeh Chang, and Chau-Ching Chiong, "A DC-21 GHz low imbalance active balun using darlington cell technique for high speed data communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 11, pp. 728–730, Nov. 2009.

[35] Mattias Ferndahl and Hans-Olof Vickes, "The matrix balun—A transistor-based module for broadband applications," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 1, pp. 53–60, Jan. 2009.

[36] Kooho Jung, William R. Eisenstadt, Robert M. Fox, Alvin W. Ogden, and Jangsup Yoon "Broadband active balun using combined cascode-cascade configuration," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1790–1796, Aug. 2008.

[37] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, Mc Graw Hill, New York, NY, 2001.

[38] D.-Y. Kim, S.-G. Lee, J.-H. Lee, "Up-Conversion Mixer for PCS Application using Si BJT," *IEEE 2nd International Conference on Microwave and Millimeter Wave Technology Proceedings*, Beijing, China, pp. 424-427, 2000.

[39] R. Xu, Y. Jin, and C. Nguyen, "Power-efficient switching-based CMOS UWB transmitters for UWB communications and radar systems," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3271–3277, Aug. 2006.

[40] N. Talwalkar, C. Yue, H. Guan, and S. Wong, "Integrated CMOS transmit-receive switch using *LC*-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 863–870, Jun. 2004.

[41] P. Piljae, S. Dong Hun, and C. P. Yue, "High-linearity CMOS T/R switch design above 20 GHz using asymmetrical topology and ACfloating bias," *IEEE Trans. Microwave Theory Tech*., vol. 57, pp. 948–956, Apr. 2009.

[42] Q. Li, Y. P. Zhang, K. S. Yeo, and W. M. Lim, "16.6- and 28-GHz fully integrated CMOS RF switches with improved body floating," *IEEE Trans. Microwave Theory Tech*., vol. 56, pp. 339–345, Feb. 2008.

[43] B. W. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 6, pp. 1364–1371, Jun. 2008.

[44] Z. Li, H. Yoon, F.-J. Huang, and K. K. O, "5.8-GHz CMOS T/R switches with high and low substrate resistances in a 0.18 μ-m CMOS process," *IEEE Microw. Wireless Compon. Lett*., vol. 13, no. 1, pp. 1–3, Jan. 2003.

[45] N. A. Talwalkar, C. P. Yue, H. Gan, and S. S.Wong, "Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz

applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 863–870, Jun. 2004.

[46] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Tech*., vol. 54, no. 1, pp. 31–39, Jan. 2006.

[47] Q. Li and Y.-P. Zhang, "CMOS T/R switch design: Towards ultrawideband and higher frequency," *IEEE J.Solid-State Circuits*, vol. 42, no. 3, pp. 563–570, Mar. 2007.

[48] Y. Jin and C. Nguyen, "Ultra-compact high-linearity high-power fully integrated DC-20-GHz 0.18-μm CMOS T/R switch," *IEEE Trans. Microw. Theory Tech*., vol. 55, no. 1, pp. 30–36, Jan. 2007.

[49] Nitin Jain, " High Isolation Switch In Balanced Lines," U.S. Patent 6 903 623, Jun. 7, 2005

[50] T. M. Hancock, I. Gresham, and G. M. Rebeiz, "A differential sub-nanosecond high-isolation absorptive active SiGe 24 GHz switch for UWB applications," in *Proc. IEEE RFIC Symp*., 2004, pp. 497–500.

[51] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, 2nd ed., Prentice Hall, Upper Saddle River, NJ, 1997.

[52] S. C. Cripps, *RF Power Amplifiers for Wireless Communication,* 1st ed., Artech House, Norwood, MA, 1999.

[53] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothercary, J.F. Sevic, and N.O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 814–826, Mar. 2002.

[54] Mona Hella and Mohammed Ismail, *RF CMOS Power Amplifiers: Theory, Design, and Implementation*, Kluwer Academic Publishers, Norwell, Boston, 2002.

[55] S. Zhang, J. Madic, P. Bretchko, J. Mokoro, R. Shumovich, and R. McMorrow, "A novel power-amplifier module for quad-band wireless handset applications," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no.11, pp. 2203–2210, Nov. 2003.

[56] K. Yamamoto, S. Suzuki, K. Mori, T. Asada, T. Okuda, A. Inoue, T. Miura, K. Chomei, R. Hattori, M. Yamanouchi, and T. Shimura, "A 3.2-V operation single-chip dual-band AlGaAs/GaAs HBT MMIC power amplifier with active feedback circuit technique," *IEEE Solid-State Circuits*, vol. 35, no. 8, pp. 1109–1120, Aug. 2000.

[57] H. Zhang, H. Gao, and G. P. Li, "Broad-band power amplifier with a novel tunable output matching network," *IEEE Trans. Microw. TheoryTech.*, vol. 53, no. 11, pp. 3606–3614, Nov. 2005.

[58] L. Yumin, D. Peroulis, S. Mohammadi, and L. P. B. Katehi, "A MEMS reconfigurable matching network for a class AB amplifier," *IEEE Microw. Wireless Compon. Lett*., vol. 13, no. 10, pp. 437–439, Oct. 2003.

[59] W. C. E. Neo, Y. Lin, X. D. Liu, L. C. N. De Vreede, L. E. Larson, M. Spirito, M. J. Pelk, K. Buisman, A. Akhnoukh, A. De Graauw, and L. K. Nanver, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," *IEEE Solid-State-Circuits*, vol. 41, no. 9, pp. 2166–2176, Sep. 2006.

[60] M.R. Ghajar and S. Boumaiza, "Concurrent dual band 2.4/3.5 GHz fully integrated power amplifier in 0.13μm CMOS technology," *Proceeding of EuMC,* Rome, Italy, September 2009, pp. 375–378.

[61] S.-F. R. Chang, W. L. Chen, S. C. Chang, C. K. Tu, C. L. Wei, C. H. Chien, C. H. Tsai, J. Chen, and A. Chen, "A dual-band RF transceiver for multistandard WLAN applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 1048–1055, Mar. 2005.

[62] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "A design technique for concurrent dual-band harmonic tuned power amplifier," *IEEE Trans. Microwave Theory and Tech*., vol. 56, no.11, pp. 2545–2555, Nov. 2008.

[63] Wenhua Chen, Seyed Aidin Bassam, Xiang Li, Yucheng Liu, Karun Rawat, Mohamed Helaoui, Fadhel M. Ghannouchi, Zhenghe Feng, "Design and Linearization of Concurrent Dual-Band Doherty Power Amplifier With Frequency-Dependent Power Ranges", *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2537–2545, Oct. 2011.

[64] Yongle Wu, Yuanan Liu, Shulan Li, Cuiping Yu, and Xin Liu, "A generalized dual-frequency transformer for two arbitrary complex frequency-dependent

impedances", *IEEE Microw. Wirel. Comp Lett*., vol. 19, no. 12, Dec. 2009, pp. 792–794

[65] Ming-Lin Chuang, "Dual-band impedance transformer using two section shunt stub", *IEEE Trans. Microw. Theory Tech*., vol. 58, no. 5, May 2010, pp. 1257–1263.

[66] Robert J. Trew," High-Frequency Solid-State Electronic Devices", *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 638-648, May 2005.

[67] T. S. D. Cheung and J. R. Long, "A 21–26-GHz SiGe bipolar power amplifier MMIC," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2583–2597, Dec. 2005

[68] Z. Ma, N. Jiang, G. Wang and S.A. Alterovitz, "An 18 GHz, 300 mW SiGe power HBT," *IEEE Electron Device Letters*, vol. 26, no. 6, pp. 381-383, June 2005.

[69] S. Chartier, E. Sonmez, H. Schumacher, "24 and 36 GHz SiGe HBT power Amplifiers," *Silicon Monolithic Integrated Circuits in RF Systems, Digest*, pp. 251-254, Sep. 2004.

[70] J.P. Comeau, J.M. Andrews, J.D. Cressler, "A Monolithic 24 GHz, 20 dBm, 14% PAE SiGe HBT Power Amplifier", *European Microwave Conference Proceedings*, pp. 419-422, Sep. 2006.

[71] Abbas Komijani, Arun Natarajan, and Ali Hajimiri, "A 24-GHz, +14.5-dBm Fully Integrated Power Amplifier in 0.18-um CMOS", *IEEE Journal Of Solid-State Circuits*, vol. 40, no. 9, September 2005.

[72] Ichiro Aoki, Scott D. Kee, David B. Rutledge, and Ali Hajimiri, ”Distributed Active Transformer—A New Power-Combining and Impedance-Transformation Technique”, *IEEE Trans. Microw. Theory Tech*., vol. 50, no. 1, January 2002.

[73] Ullrich R. Pfeiffer, and David Goren, ”A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology”, *IEEE Trans. Microw. Theory Tech*., vol. 55, no. 5, May 2007.

[74] M. Chang and G.M. Rebeiz, “A 26 to 40GHz Wideband SiGe Balanced Power Amplifier IC,” *IEEE RFIC Symposium Digest*, pp. 729–732, June 2007.

[75] Abbas Komijani, and Ali Hajimiri, ”A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon”, *IEEE Journal Of Solid-State Circuits*, vol. 41, no. 8, August 2006.

[76] C. Doan, S. Emami, A. Niknejad, R. Brodersen, “Millimeter-wave CMOS design,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 144—155, January 2005.

[77] A. N. Stameroff, A. Pham, and R. E. Leoni, “High Efficiency Push-Pull Inverse Class F Power Amplifier Using a Balun and Harmonic Trap Waveform Shaping Network,” *2010 IEEE MTT-S International Microwave Symposium Digest*, pp. 521- 525, May 2010.

[78] C. M. Grens, P. Cheng, and J. D. Cressler, “Reliability of SiGe HBTs for power amplifiers—Part I: Large-signal RF performance and operating limits,” *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 3, pp. 431–439, Sep. 2009.

[79] M. Rickelt, H.-M. Rein, E. Rose, "Influence of Impact-Ionization-Induced Instabilities on the Maximum Usable Output Voltage of Si-Bipolar Transistors," *IEEE Trans. Electron Devices*, pp. 774-783, April 2001.

[80] Domenico Zito, Domenico Pepe, Martina Mincica, Fabio Zito, Alessandro Tognetti, Antonio Lanatà, and Danilo De Rossi, "SoC CMOS UWB pulse radar sensor for contactless respiratory rate monitoring," *IEEE Trans. Biomed. Circuits Syst*., vol. 5, no. 6, pp. 503–510, 2011.

[81] A. Oncu, B. B. M. Wasanthamala Badalawa, and M. Fujishima, "22–29 GHz ultra-wideband CMOS pulse generator for short-range radar applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1464–1471, Jul. 2007.

[82] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-chip W-band SiGe HBT transceivers and receivers for doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2206–2217, Oct. 2008.

[83] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[84] Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip dipole antennas: Receiver and on-chip antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[85] E. Ragonese, A. Scuderi, V. Giammello, E. Messina, and G. Palmisano, "A fully integrated 24 GHz UWB radar sensor for automotive applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2009, pp. 306–307.

[86] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22-to-29GHz/77-to-81GHz BiCMOS transceiver for automotive radars," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech*. Papers, Feb. 2009, pp. 308–309.

[87] *CMOS Oscillators*, Fairchild Semiconductor Inc., Application Note 118, October 1974.