JITTER-TOLERANCE AND BLOCKER-TOLERANCE OF DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTERS FOR SAW-LESS MULTI-STANDARD RECEIVERS

A Dissertation

by

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ABSTRACT

The quest for multi-standard and software-defined radio (SDR) receivers calls for high flexibility in the receiver building-blocks so that to accommodate several wireless services using a single receiver chain in mobile handsets. A potential approach to achieve flexibility in the receiver is to move the analog-to-digital converter (ADC) closer to the antenna so that to exploit the enormous advances in digital signal processing, in terms of technology scaling, speed, and programmability. In this context, continuous-time (CT) delta-sigma (ΔΣ) ADCs show up as an attractive option. CT ΔΣ ADCs have gained significant attention in wideband receivers, owing to their amenability to operate at a higher-speed with lower power consumption compared to discrete-time (DT) implementations, inherent anti-aliasing, and robustness to sampling errors in the loop quantizer. However, as the ADC moves closer to the antenna, several blockers and interferers are present at the ADC input. Thus, it is important to investigate the sensitivities of CT ΔΣ ADCs to out-of-band (OOB) blockers and find the design considerations and solutions needed to maintain the performance of CT ΔΣ modulators in presence of OOB blockers. Also, CT ΔΣ modulators suffer from a critical limitation due to their high sensitivity to the clock-jitter in the feedback digital-to-analog converter (DAC) sampling-clock.

In this context, the research work presented in this thesis is divided into two main parts. First, the effects of OOB blockers on the performance of CT ΔΣ modulators are investigated and analyzed through a detailed study. A potential solution is proposed to

alleviate the effect of noise folding caused by intermodulation between OOB blockers and shaped quantization noise at the modulator input stage through current-mode integration. Second, a novel DAC solution that achieves tolerance to pulse-width jitter by spectrally shaping the jitter induced errors is presented. This jitter-tolerant DAC doesn't add extra requirements on the slew-rate or the gain-bandwidth product of the loop filter amplifiers. The proposed DAC was implemented in a 90nm CMOS prototype chip and provided a measured attenuation for in-band jitter induced noise by 26.7dB and in-band DAC noise by 5dB, compared to conventional current-steering DAC, and consumes 719μwatts from 1.3V supply.

DEDICATION

To my dear family, Dad and Rama

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1. INTRODUCTION

1.1 Background

1.1.1 Blocker-Tolerance in Future ADCs

Nowadays, there is an increasing interest in the wireless industry to reduce the complexity of the radio-frequency (RF) and analog baseband sections of the receiver chain and move the channel-select filtering into the digital-domain, as exemplified by Fig. 1.1. This entails moving the analog-to-digital converter (ADC) closer to the antenna. The main motivation is to exploit the enormous advances in digital signal processing (DSP), offered by new CMOS technologies, so that to enable the wide range of reconfigurability needed in multi-standard and future software-defined radio (SDR) receivers. Moreover, cost targets call aggressively for achieving full integration in a standard digital CMOS technology and remove expensive, bulky SAW filters from the RF section of the receiver.

In addition to the high flexibility needed in the interface between the analog and digital domains, the multi-standard/multi-band receiver outline shown in Fig. 1.1 requires the ADC to be robust to unwanted interferers. Without filtering in the receiver front-end, interferers can propagate through the receiver chain without adequate suppression and hence show up at the ADC input. In essence, strong out-of-band (OOB) blockers can saturate/overload the ADC building-blocks, cause instability in ADC structures whose operation is based on feedback loops, degrade the quality of the A/D

conversion due to distortion and insufficient anti-aliasing, and/or exhaust the ADC dynamic-range (DR) and block the wanted channel. The blocker tolerance challenge will be exacerbated further by realizing that the introduction of multi-standard wireless terminals and SDRs will motivate the expansion of the wireless market and services, making the wireless environment even more hostile.

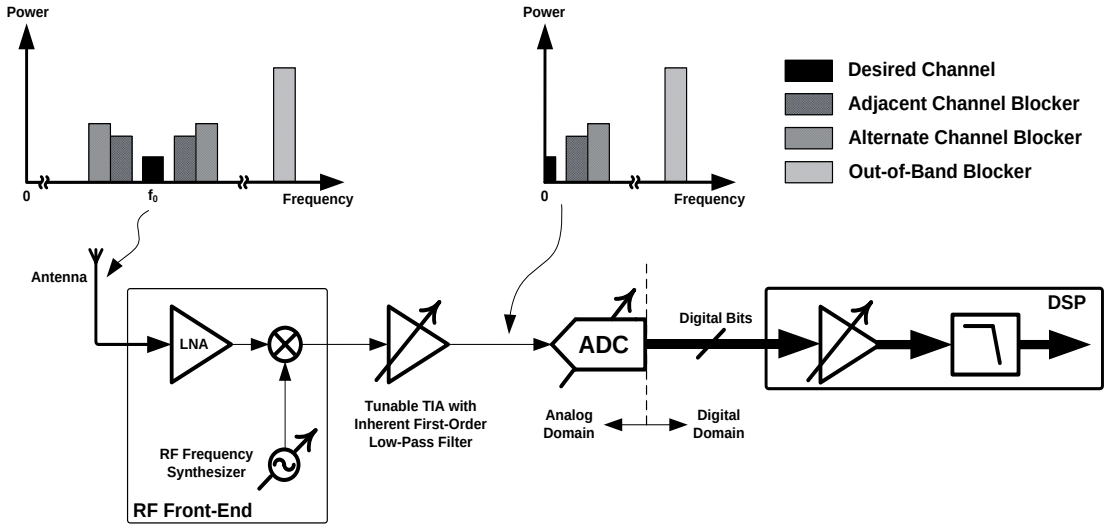


Fig. 1.1. Candidate architecture for SAW-less multi-standard/multi-band and software-defined radio receivers.

The foregoing premise implies that two new characteristics —reconfigurability and blocker-tolerance— need to be included in the ADC design specifications for future multi-standard wireless terminals and SDRs. Thus, the conventional ADC design triangle (Fig. 1.2(a)) should be upgraded to the design pentagon shown in Fig. 1.2(b). Every two parameters in the diagrams in Fig. 1.2 trade with each other and the true

severities of these tradeoffs are known only if relevant data have been obtained for the adopted technology and wireless profiles.

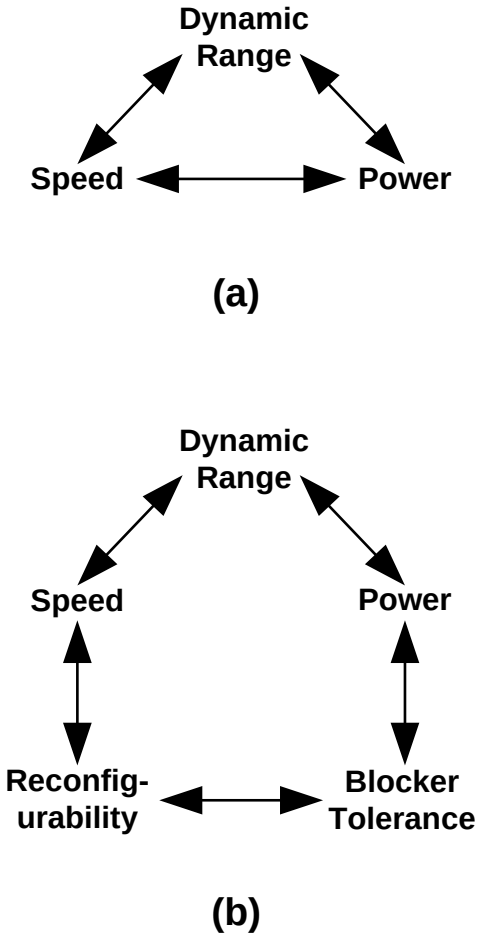


Fig. 1.2. (a) ADC design triangle in conventional receivers. (b) ADC design pentagon for multi-standard receivers and SDRs.

Combined with low power consumption needed for portable devices and mobile handsets, the foregoing abstract discussion leverages the basic criteria that should be considered in selecting ADC architecture for future multi-standard receivers and SDRs.

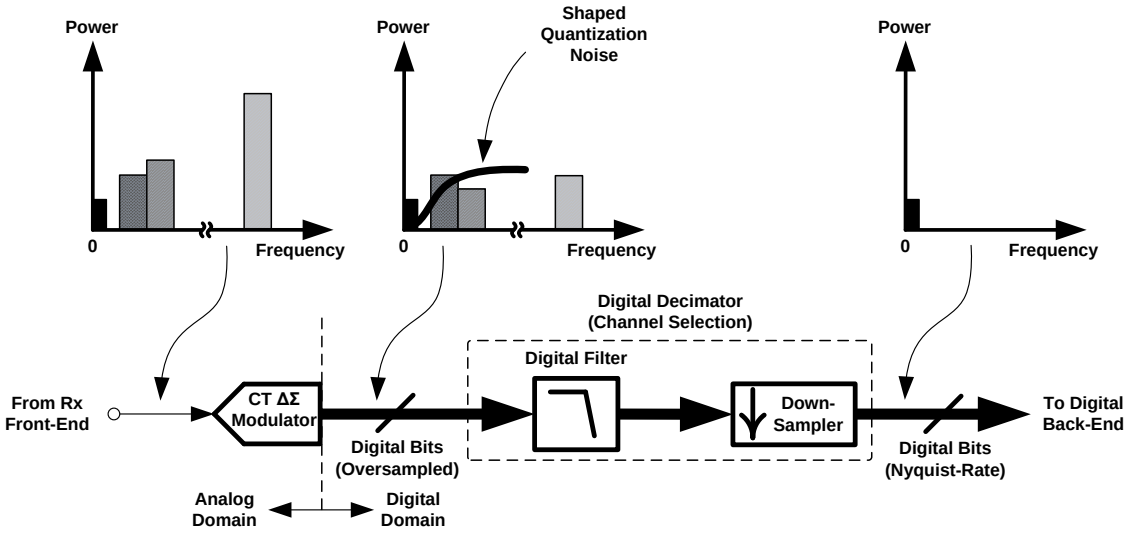


Fig. 1.3. Continuous-time ΔΣ ADC (ΔΣ pulse density modulation + digital decimation and filtering), with inherent blocker filtering.

Delta-sigma (ΔΣ) ADCs are the convenient choice in low power multi-standard receivers for three main reasons. First, they trade DSP for relaxed analog circuit complexity. Particularly, ΔΣ ADC implementations span analog and digital domains (ΔΣ pulse density modulation + digital decimation and filtering, as shown in Fig. 1.3) and hence exploit DSP to relax hardware requirements on analog blocks. Thus, the simplified analog part (ΔΣ modulator) and the digital filtering can be efficiently reconfigured to fulfill performance requirements of different standards at minimum power consumption. Second, ΔΣ modulators use oversampling and hence trade speed for resolution. Specifically, for a given ΔΣ modulator and channel bandwidth (BW), higher effective number of bits (ENOB) can be achieved by increasing the oversampling ratio (OSR). This qualifies ΔΣ ADCs to benefit from increasing speeds of operation offered by

advanced deep submicron CMOS technologies (maximum cutoff-frequency $f_T > 300\ GHz$ in 45nm [1]) to meet higher resolution requirements for modern and future wireless services at minimum power overhead. Third, digital filtering following the ΔΣ modulator can perform channel selection. As a result, ΔΣ ADC structures can save area and power by avoiding an explicit channel-select filter. Several multi-standard ΔΣ modulators have been reported in the literature [2]-[9][1].

Because multi-standard wireless terminals must handle several wireless services including both narrow-band (e.g. GSM, channel BW=200 KHz) and wide-band (e.g. WLAN802.11n, channel BW=40 MHz) channels, continuous-time (CT) ΔΣ modulators show up as an attractive option. ΔΣ modulators with CT loop-filters (see Fig. 1.4) have gained popularity in battery powered applications due to speed/power advantages over their discrete-time (DT) counterparts, enabling a higher clock rate or lower power consumption [10], [11]. In a CT modulator, the time discretization takes place at the quantizer input, as shown in Fig. 1.4, which is the point of maximum error suppression, providing inherent robustness to sampling errors. Also, CT modulators can provide inherent anti-alias filtering. Recent CMOS implementations show feasible input bandwidths up to a few tens of MHz [12]–[15]. However, CT ΔΣ modulators suffer from a critical limitation due to their high sensitivity to the clock-jitter in the feedback digital-to-analog converter (DAC) sampling clock [16]. The clock-jitter problems are considered in details in the next sub-section.

[1] These multi-standard ΔΣ modulators were not designed following the multi-standard receiver model in Fig. 1. In essence, such ADCs would process only the desired channel which is assumed to be appropriately selected and filtered by prior *reconfigurable* filtering in receiver front-end.

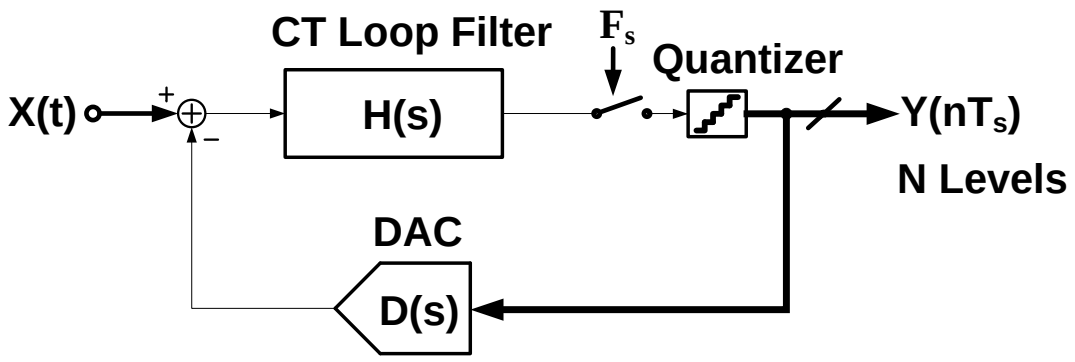


Fig. 1.4. Continuous-time ΔΣ modulator block-diagram.

1.1.2 Clock-Jitter Challenge

The quest for higher data rates in state-of-the-art wireless standards and services calls for wideband and high-resolution data-converters in wireless transceivers. While modern integrated circuits (IC) technologies provide high cut-off frequencies (f_T) for transistors and hence allow the operation at higher speeds, the main limitation against increasing speed of operation of data-converters is the problem of clock-jitter. Clock-jitter is a common problem associated with clock generators due to uncertainty in the timing of the clock edges caused by the finite phase-noise (PN) in the generated clock waveform. Particularly, noise components induced by several noise sources in the system providing the clock (e.g. phase-locked loop, PLL) add to the clock waveform and cause uncertainty in the timing of the zero-crossing instants from cycle to cycle. Figure 1.5 shows a survey chart of the analog-to-digital converter (ADC) implementations reported in the IEEE International solid-state circuits conference (ISSCC) and VLSI Symposium since 1997 [17]. The straight lines show the limitation on the achievable

signal-to-noise ratio (SNR) by clock-jitter for root-mean square (rms) jitter values of 1ps and 0.1ps. As can be seen from the chart, the performance of most ADCs falls below the line corresponding to 1ps rms jitter, few ADCs reside in the range between 1ps and 0.1ps, and almost all ADC implementations reported so far are beyond the 0.1ps rms jitter line. This means that the main limitation on increasing the ADC performance in terms of SNR and speed is the specification on the clock-jitter of 0.1ps.

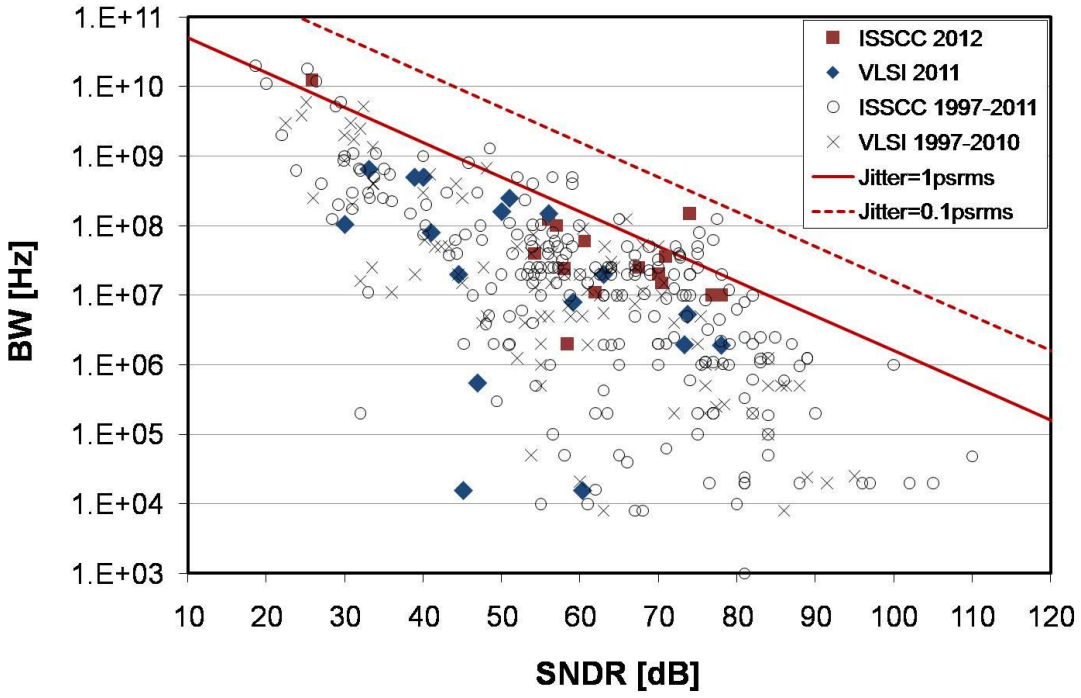


Fig. 1.5. ADC Performance Survey 1997-2012 [17].

In CT ΔΣ modulators, the random variations of the DAC sampling clock edge which cause uncertainty in the pulse-width of the feedback waveform and hence the integrated values at the outputs of the loop filter integrators. Called pulse-width jitter (PWJ), it is

equivalent to applying random phase modulation to the digital signal coming in the feedback, causing a part of the shaped noise outside the signal band to fall into the signal band. The noise induced by PWJ of the outermost DAC is the most critical one, as it appears directly at the output.

1.2 Thesis Organization

The main motivation for the research effort presented by this thesis is to investigate and provide innovative solutions to achieve jitter tolerance and immunity to OOB blockers in CT ΔΣ modulators at low power overhead in the context of multi-standard and SDR receivers. The thesis is organized as follows.

Section 2 provides a comprehensive background and study for the effects of clock-jitter in the sampling-clocks of ΔΣ modulators. Matlab/Simulink models for additive errors induced by clock-jitter in ΔΣ modulators are given and discussed. These models are in characterizing the sensitivities of various types of ΔΣ architectures to clock-jitter.

In Section 3, the sensitivity of the ΔΣ loop operation to the signal swing and settling speed limitations in presence of large OOB blocking signals will be analyzed. Also, the effects of OOB blocker components appearing at the output of the modulator on the ADC DR budgeting are discussed.

Section 4 investigates the sensitivity of single-bit CT ΔΣ ADCs to OOB blockers received in companion with desired signals. In essence, the residual interferer signal appearing at the output of the CT loop filter can flip the single-bit quantizer decision

near the zero crossings of the loop filter output signal. An intuitive analysis of this effect on the performance of single-bit ΔΣ modulators in presence of OOB interferes is provided.

Section 5 investigates the sensitivity of CT ΔΣ ADCs to feedback PWJ in presence of blockers received at the ADC input. The analyses cover several types of DAC waveforms as well as multi-bit and single-bit DACs. Also, a comparison between ΔΣ modulators with feedforward and feedback loop filter structures in terms of robustness to DAC PWJ, in presence of blockers, is performed. Discussions and conclusions developed in this section are verified by CT simulations in Matlab/Simulink and simulations results show good agreement with the theoretical expectations.

In section 6, a simple feedforward spectral shaping technique for the PWJ induced errors in oversampled DACs is presented. The proposed technique features a feedforward combination between the conventional rectangular-pulse current-steering (CS) DAC and a DT switched-capacitor-resistor (SCR) DAC to achieve spectral shaping for the jitter induced error. The benifit of this hybrid DAC solution using error specral shaping is illustrated in the context of feedback DACs used in CT ΔΣ modulators.

Section 7 presents detailed analysis for the performance sensitivity of CT ΔΣ modulators to loop filter nonlinearities in presence of large OOB blockers. The problem of noise folding caused by nonlinearities in presence of large OOB blockers is explained and analyzed. A new solution is presented to mitigate the noise folding problem and the potential of the proposed solution is verified by simulations.

Finally, summary and conclusions are given in Section 8.

2. CLOCK-JITTER EFFECTS IN DELTA-SIGMA MODULATORS: BACKGROUND AND ANALYSIS

2.1 Introduction

This section provides a comprehensive background and study for the effects of clock-jitter in the sampling-clocks of ΔΣ modulators. Matlab/Simulink models for additive errors induced by clock-jitter in ΔΣ modulators are given and discussed. These models are in characterizing the sensitivities of various types of ΔΣ architectures to clock-jitter. The material in this section is organized as follows. Section 2.2 gives a general background about the types of errors caused by clock-jitter in different classes of switched circuits and signal waveforms. The critical sources of jitter induced errors in a ΔΣ loop are identified for DT and CT ΔΣ modulators and a comparison between the two types, in terms of sensitivity to clock-jitter, is done in Section 2.3. Section 2.4 provides detailed sensitivity analysis for CT ΔΣ modulators to clock-jitter in the feedback DAC sampling-clock. In Section 2.5, Simulink models, based on the analysis of Section 2.4, for the additive errors generated by clock-jitter in CT ΔΣ modulators are shown and the robustness of these models is verified by CT simulations in Matlab/Simulink. Simulations results show good agreement with the theoretical expectations. Finally, conclusions are drawn in Section 2.6.

2.2 Jitter Problems: Background

Since digital data is always available in DT form, then any process of converting information from analog form to digital bit-stream or vice versa entails sampling. However, the clock signals driving sampling switches suffers clock-jitter due to the noise components that accompany the clock waveform. Figure 2.1 shows the PN density in a typical voltage-controlled oscillator (VCO)[2]. In the time-domain, the integrated effect of these noise components results in random variations in the phase of the generated clock signal. In data-converters, the problem of clock-jitter is a very critical issue and can significantly deteriorate the achievable SNR by several dBs. The problems resulting from clock-jitter are classified as follows:

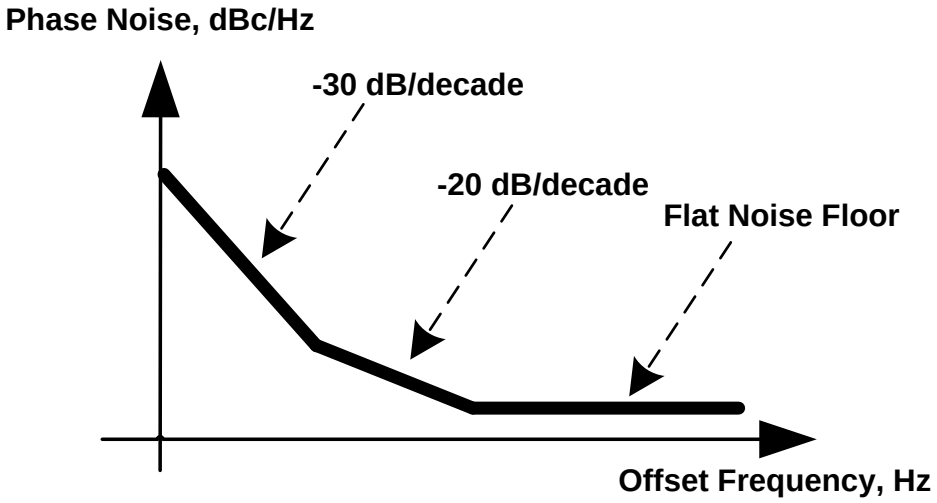


Fig. 2.1. Typical phase-noise profile in a VCO.

[2] **The design of clock generators and the mechanisms of PN generation in PLLs are not within the scope of the material given in this section.**

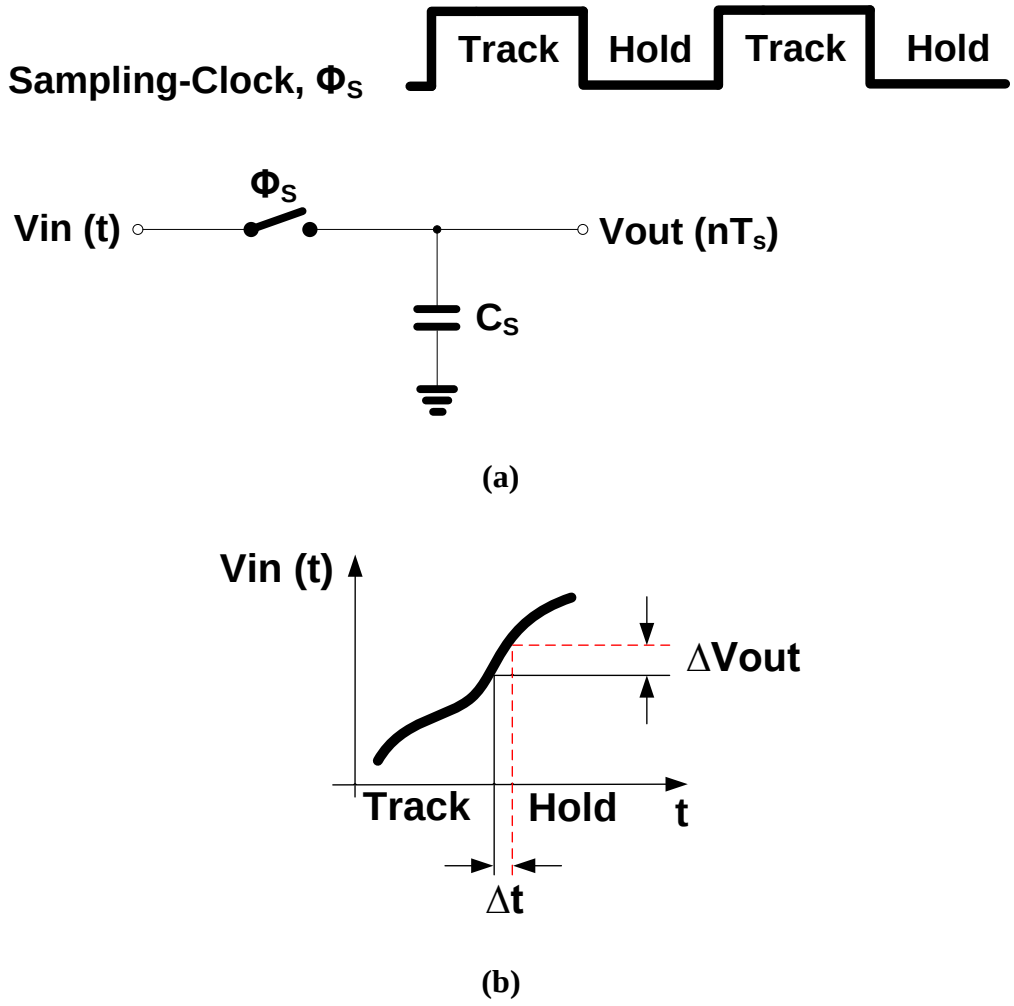


Fig. 2.2. T/H Circuit. (a) Schematic view and clock waveform. (b) Effect of aperture jitter on sampled values.

2.3 Aperture Jitter: Voltage Sampling Errors

In ADCs, it is desirable to convert CT voltage signals into DT form. Figure 2.2(a) shows a common track-and-hold (T/H) circuit based on a switch driven by a clock signal (sampling-clock) and a sampling capacitor C_S. Errors in the sampled voltage (during the tracking phase) value is one of the most common problems resulting from

timing uncertainty Δt (clock-jitter) in the sampling-clock. Particularly, on sampling an input voltage signal, random variations in the timing of the clock edges can result in an incorrect sampled signal, as illustrated in Fig. 2.2(b). This effect is called aperture jitter. The noise induced by aperture jitter can be illustrated as follows. Suppose that a sinusoidal signal $A\ sin(\omega t)$, where A is the amplitude and ω is the angular frequency, is to be sampled using a T/H circuit. Then, the error in the n^{th} sample of the sampled signal due to a timing error $\Delta t(n)$ is given by

$$e(n\,T_s) = A\,\{sin[\omega(n\,T_s + \Delta t(n))] - sin(\omega\ n\,T_s)\}$$

$$\approx A\ \omega\ \Delta t(n)\ cos(n\,T_s). \tag{2.1}$$

where T_s is the sampling-period. If σ_j^2 is the variance of the timing error Δt, then the error power is given by

$$\sigma_e^2 = E(e^2) = \frac{\left(A\ \omega\ \sigma_j\right)^2}{2}. \tag{2.2}$$

Since the signal power of the sinusoid is given by $A^2/_2$, the SNR due to aperture jitter is given by

$$SNR|_{Due\ to\ aperture\ jitter} = 10\ Log\ \left(\frac{1}{\omega^2\sigma_j^2}\right) = 10\ Log\ \left(\frac{1}{4\,\pi^2\,f^2\sigma_j^2}\right), \tag{2.3}$$

where $f = \omega/2\pi$ is the frequency. From (3) the SNR has the worst value at the edge of the signal band (largest value of frequency, f_{max}). The plots in Fig. 2.3 show the limitation on the achievable SNR vs. the signal frequency due to aperture jitter for different values of the rms jitter σ_j.

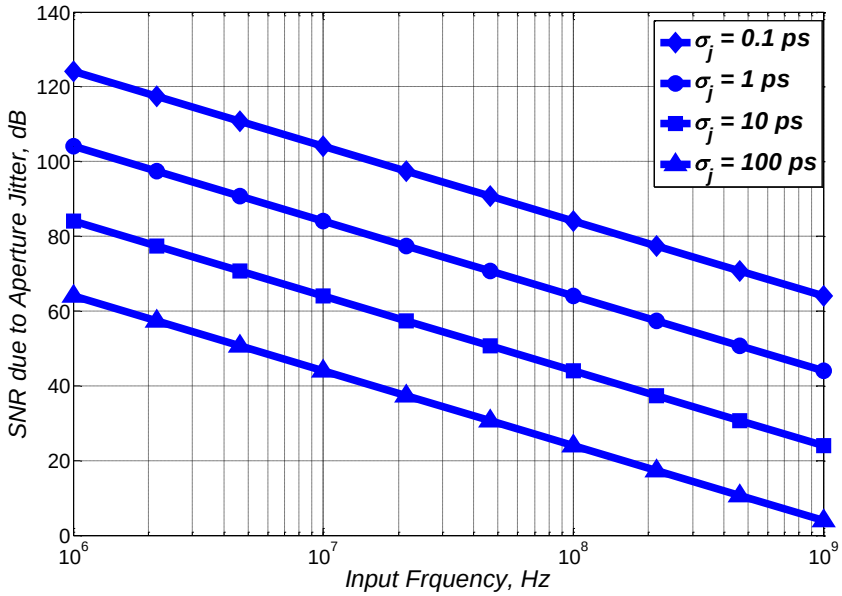
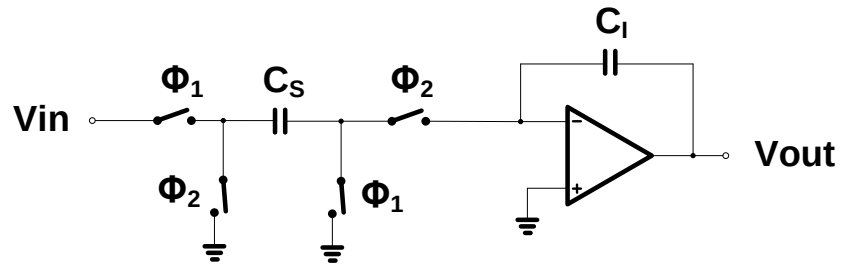


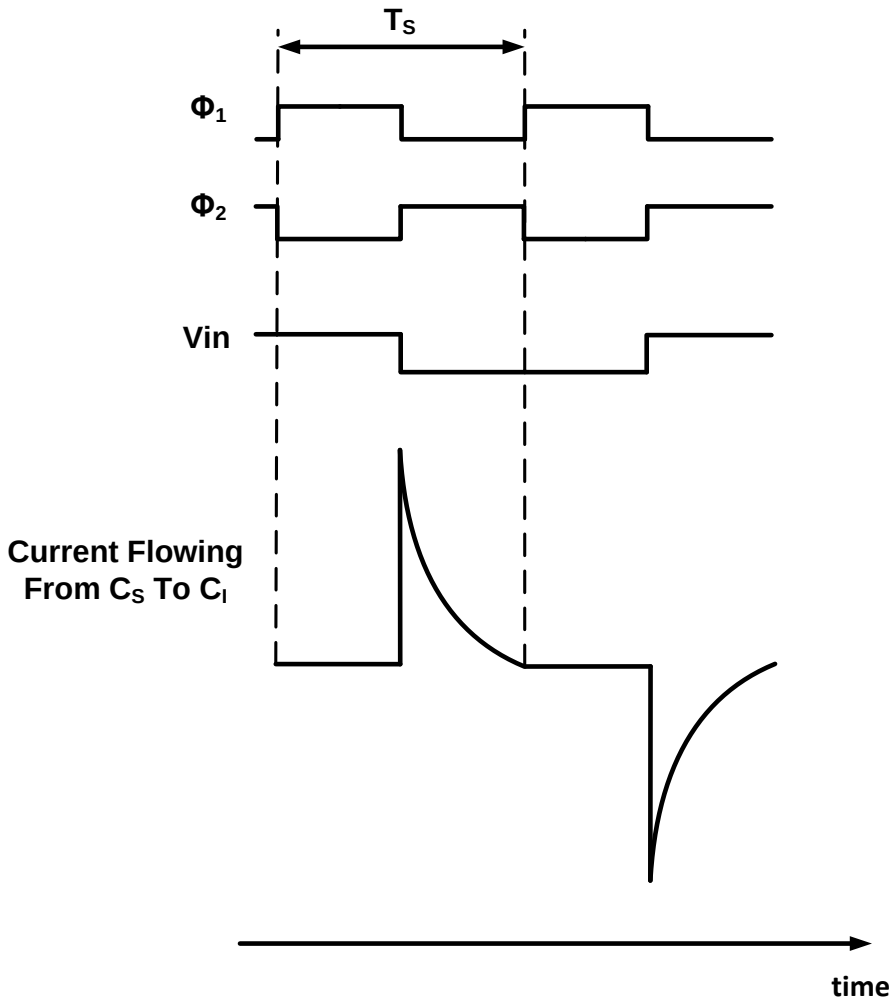
Fig. 2.3. SNR variation with the input frequency due to aperture jitter for different rms jitter values.

2.4 Charge Transfer Jitter

Another effect of clock-jitter, called charge transfer jitter, shows up in circuits whose operation is based on charge transfer by switching. In particular, switched-capacitor (SC) circuits commonly used in DT ADCs and DACs suffer from charge transfer errors due to clock-jitter in the sampling clocks. Consider the simple non-inverting SC integrator in Fig. 4(a). As shown by the time-domain waveforms in Fig. 2.4(b), during integrating phase $\emptyset_2$, the charge stored in a sampling capacitor C_S is transferred to an integrating capacitor C_I through the ON resistance (R_{ON}) of the switch. The discharging of C_S takes place in an exponentially-decaying rate.



(a)



(b)

Fig. 2.4. (a) Non-inverting switched-capacitor discrete-time integrator. (b) Time domain waveforms for clock phases, input signal, and charge flow from C_S to C_I.

For a given clock-cycle n, the instantaneous exponentially-decaying current $I_n(t)$ resulting from the charge transfer from C_S to C_I can be derived as follows:

$$I_n(t) = \begin{cases} I_P\, e^{\frac{-(t-\alpha)T_s}{\tau}} & , \quad \alpha T_s < t < \beta T_s, 0 \leq \alpha \leq \beta \leq 1 \\ 0 & , \quad otherwise \end{cases}, \tag{2.4}$$

where I_P is the value of the peak current at the beginning of the pulse, α and β are the start and end times of the exponentially-decaying pulse normalized to the sampling period T_s and τ is the discharging time-constant and is given by the product $R_{ON}C_S$. The values of α and β are determined by the duty-cycle of the clock. In typical SC circuits, $\alpha = 0.5$ and $\beta = 1$. Recall that the input voltage is sampled on C_S during the first clock half-cycle (when $\emptyset_1$ is high) and then the charge on C_S is transferred to C_I during the second clock half-cycle (when $\emptyset_2$ is high). For a total charge of Q_n to be transferred during $\emptyset_2$ of clock-cycle n,

$$Q_n = \int_{\alpha T_s}^{\beta T_s} I_n(t)\, dt = \int_{\alpha T_s}^{\beta T_s} I_P\, e^{\frac{-(t-\alpha)T_s}{\tau}}\, dt = -\tau\, A\, e^{\frac{-(t-\alpha)T_s}{\tau}}\Big|_{\alpha T_s}^{\beta T_s}$$

$$= \tau\, A \left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right) \tag{2.5}$$

Thus,

$$I_P = \frac{Q_n}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)}. \tag{2.6}$$

Substituting with (6) in (4) yields

$$I_n(t) = \begin{cases} \dfrac{Q_n}{\tau\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{\frac{-(t-\alpha)T_s}{\tau}} & , \quad \alpha T_s < t < \beta T_s, 0 \leq \alpha \leq \beta \leq 1. \\ 0 & , \quad otherwise. \end{cases} \tag{2.7}$$

However, in presence of timing error $\Delta t(n)$ in the pulse-width of the discharging phase $\emptyset_2$, the resulting error in the integrated charge in the $n^{\underline{th}}$ clock-cycle is given by

$$e_j(n) = \frac{Q_n}{\tau\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \int_{\beta T_s}^{\beta T_s + \Delta t(n)} e^{\frac{-(t-\alpha)T_s}{\tau}} dt$$

$$= \frac{-Q_n}{\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{\frac{-(t-\alpha)T_s}{\tau}} \Bigg|_{\beta T_s}^{\beta T_s + \Delta t(n)}$$

$$= \frac{Q_n}{\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \left[e^{\frac{-(\beta-\alpha)T_s}{\tau}} - e^{\frac{-(\beta-\alpha)T_s - \Delta t(n)}{\tau}} \right]$$

$$= \frac{Q_n}{\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{\frac{-(\beta-\alpha)T_s}{\tau}} \left[1 - e^{-\frac{\Delta t(n)}{\tau}}\right], \tag{2.8}$$

which for $\Delta t_n \ll \tau$ can be approximated by

$$e_j(n) \approx \frac{Q_n}{\tau\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{\frac{-(\beta-\alpha)T_s}{\tau}} \Delta t(n). \tag{2.9}$$

If σ_j^2 the variance of the timing error $\Delta t(n)$, then the error power is given by

$$\sigma_e^2 = E(e^2) = \left(\frac{Q_{rms}}{\tau\left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{\frac{-(\beta-\alpha)T_s}{\tau}} \right)^2 \sigma_j^2, \tag{2.10}$$

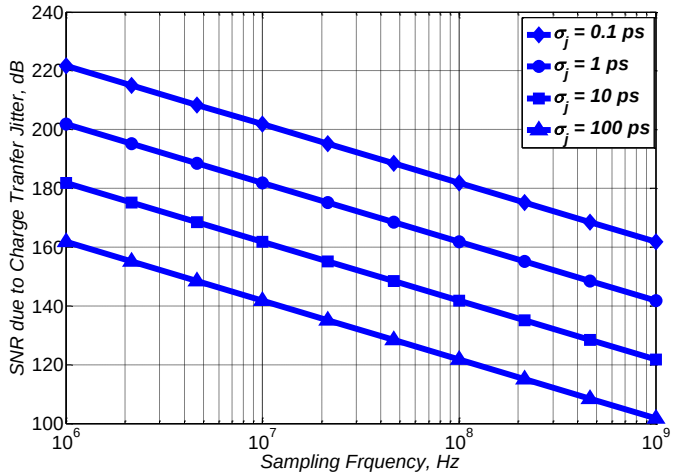
where Q_{rms} is the rms charge sampled on the sampling capacitor C_S. Thus, the SNR due to charge transfer jitter caused by charge transfer jitter is given by

$$SNR|_{Due\ to\ charge\ transfer\ jitter} = 10\ Log\left(\frac{{Q_{rms}}^2}{\left(\frac{Q_{rms}}{\tau\left(1-e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)}e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)^2\sigma_j^2}\right)$$

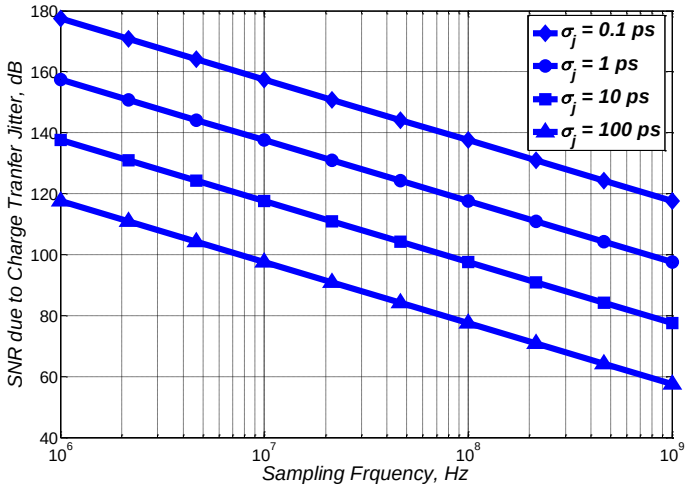
$$= 10\ Log\left(\frac{\tau^2\left(1-e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)^2}{\left(e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)^2}\frac{1}{\sigma_j^2}\right). \qquad (2.11)$$

The plots in Fig. 2.5 show the limitation on the achievable SNR vs. the signal frequency due to charge transfer jitter for different values of the rms jitter σ_j. Typical values of $\alpha = 0.5$ and $\beta = 1$ have been considered. The results are provided for $\tau = 0.05\ T_s$, $0.1\ T_s$, and $0.2\ T_s$. As can be seen from the plots in Fig. 2.5, for a given clock frequency, the SNR limitation due to charge transfer jitter is much more relaxed compared to the aperture jitter error (Fig. 2.3). This result was expected because from equation (2.11), the effect of the jitter induced noise is reduced by an exponential factor indicating that charge transfer error in SC circuits should be less critical. This also can also be explained intuitively by noting that for the exponentially-decaying waveform in Fig. 2.6, the amplitude of the pulse is rather low at the end of the clock-cycle and hence the amount of charge that varies over one clock period due to jitter is significantly reduced. However, for a given rms jitter and sampling frequency, the SNR limitation due

to charge transfer jitter degrades as the discharging time-constant τ increases. This is because the value of the charge transfer current at the end of the clock-cycle (discharge phase) is varying exponentially with τ, thus for a given timing error Δt, the error in the amount of charge transferred is higher.

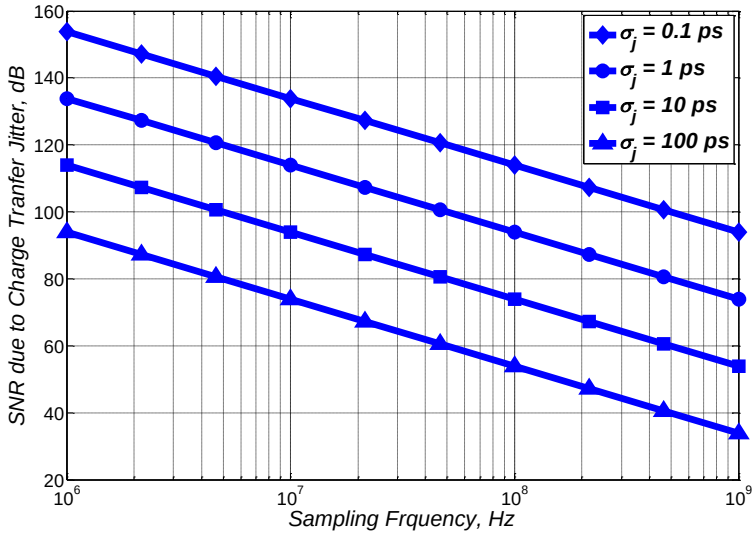


(a)



(b)

Fig. 2.5. SNR variation with the input frequency due to charge transfer jitter for different rms jitter values. (a) $\tau = 0.05\,T_s$. (b) $\tau = 0.1\,T_s$. (c) $\tau = 0.2\,T_s$.



(c)

Fig. 2.5 Continued.

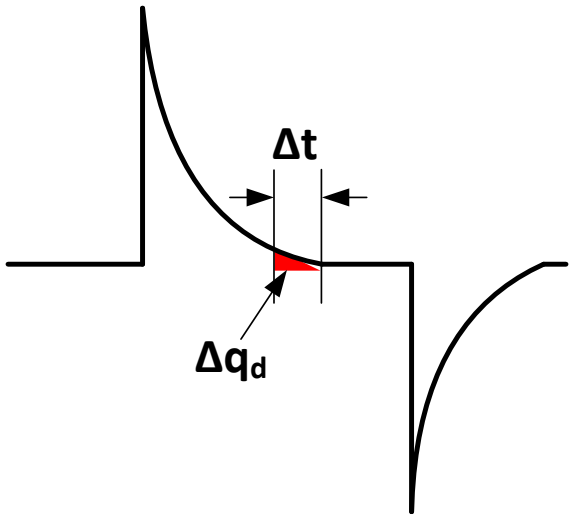


Fig. 2.6. Jitter-tolerant exponentially-decaying waveform.

2.5 Pulse-Width Jitter

Continuous-time CS DAC, shown in Fig. 2.7(a), is used to convert digital signals into CT analog pulses. Clock-jitter in the sampling-clock of a CT DAC modulates the pulse-width of the waveform at the DAC output. Called pulse-width jitter (PWJ), this problem generally shows up in circuits whose operation is based on current-switching, e.g. CS DACs, charge sampling circuits, and charge pumps. In systems using CT DACs (e.g. audio transmitters and CT ΔΣ modulators), the DAC is loaded by a CT filter stage that integrates the output current pulse from the DAC. The error in the amount of integrated charges is directly proportional to the timing error Δt in the pulse-width, as illustrated by the time-domain waveform in Fig. 2.7(b). If the clock-jitter causes timing errors Δt with variance σ_j^2 and the switched-current levels are $\pm I_S$, the variance of the charge transferred per clock-cycle T_s is

$$\sigma_e^2 = \sigma_j^2 \, {I_S}^2. \tag{2.12}$$

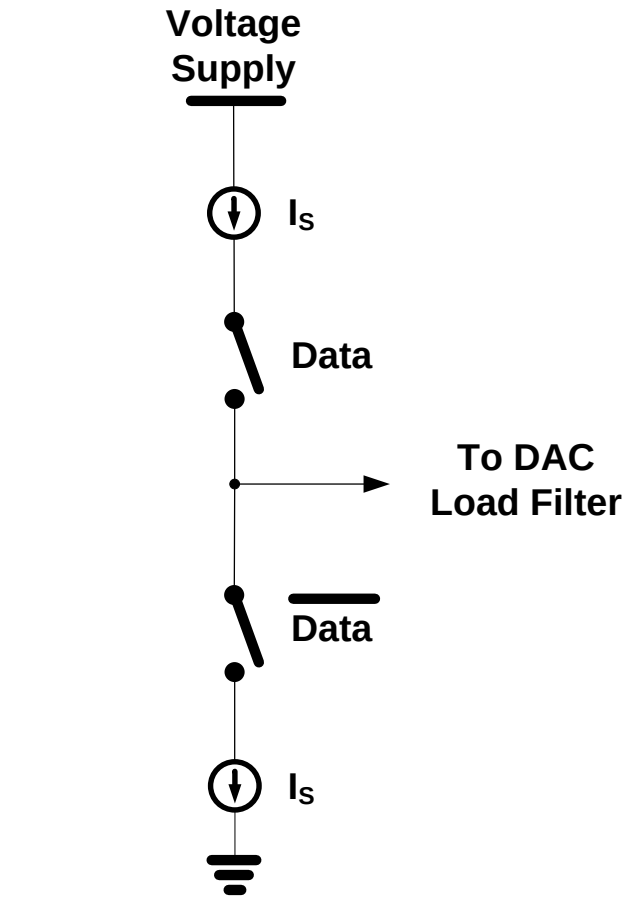
For a sinusoidal signal, the maximum signal power in terms of the integrated charge signal per clock-cycle is given by

$$\sigma_{signal}^2 = \frac{{I_S}^2 \, {T_s}^2}{2}. \tag{2.13}$$

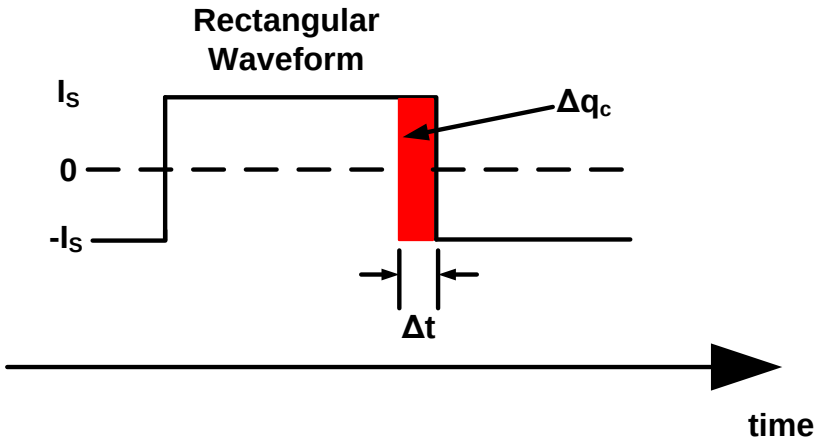
Thus, the maximum SNR against PWJ is given by

$$SNR|_{Due\ to\ pulse-width\ jitter} = 10\ Log\ \left(\frac{{T_s}^2}{2\ \sigma_j^2}\right), \tag{2.14}$$

Thus, the SNR degradation by PWJ is less than that of the aperture jitter by a factor of $2\pi^2$. The plots in Fig. 2.8 show the limitation on the achievable SNR vs. the signal frequency due to PWJ problem for different values of the rms jitter.



(a)



(b)

Fig. 2.7. Pulse-width jitter in switched-current circuits.

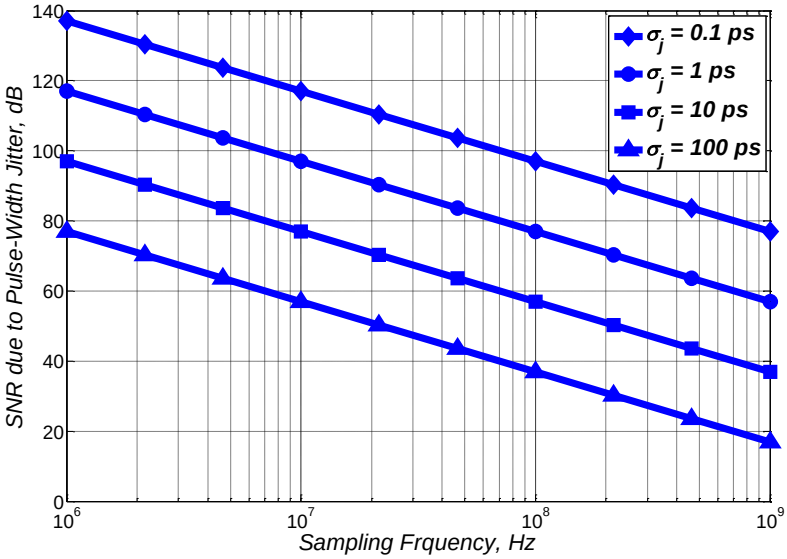


Fig. 2.8. SNR variation with the input frequency due to pulse-width jitter for different rms jitter values.

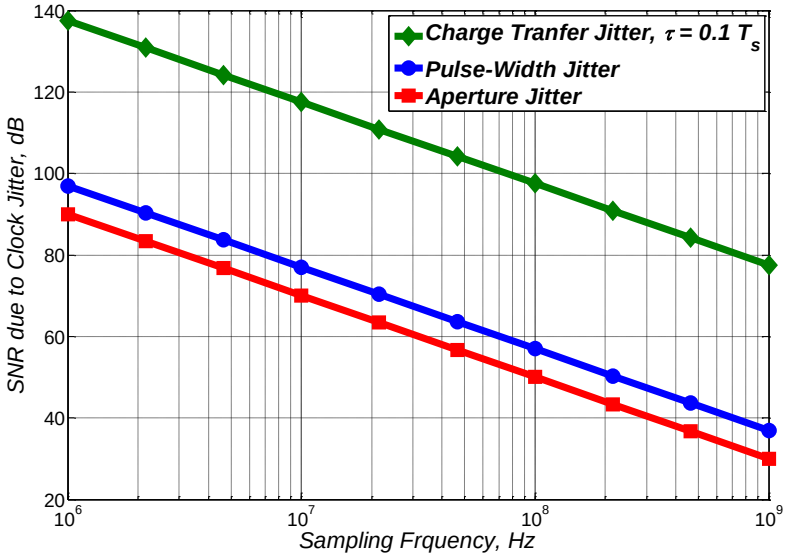


Fig. 2.9. SNR variation with the sampling frequency due to different types of jitter induced errors for a rms jitter of 10 ps.

Figure 2.9 provides a comparative insight about the SNR limitation imposed by each one of the clock-jitter induced problems discussed above. It is worth noting that these plots are for Nyquist-rate sampling; however the foregoing analysis and results can be easily extended to include the effect of oversampling in oversampled circuits. As can be observed from the plots in Fig. 2.9, for a given sampling frequency, the maximum limitation on the achievable SNR is caused by aperture jitter. However, the charge transfer jitter limits the SNR at very high frequencies; for example for an SNR of 80 dB, the charge transfer jitter starts to limit the achievable SNR at sampling frequency $F_s \geq 1\ GHz$ for $\tau = 0.1\ T_s$, and as mentioned before more robustness to charge transfer jitter at high frequencies can be obtained by reducing the discharging time-constant τ.

2.6 Sensitivity of ΔΣ Modulators to Clock-Jitter

The purpose of this section is to address the effects of clock-jitter in the two main classes of ΔΣ modulators, shown in Fig. 2.10, and provide a comparison between them in terms of sensitivity to clock-jitter. In order to determine the performance sensitivity to clock-jitter in DT and CT modulators, the critical sources of jitter induced errors in the loop should be identified in each one. The most critical clock-jitter errors in a ΔΣ modulator are those generated at the modulator input and in the feedback path through the outermost DAC feeding the first stage in the loop filter (recall that errors generated at inner nodes in the loop are suppressed by the previous stages of the loop filter). The feedback signal is carrying a digital data (coming from the loop quantizer) and hence it

is robust to aperture jitter[3]. However, depending on the type of the adopted feedback DAC, the feedback signal in a ΔΣ loop can suffer one of the other two kinds of jitter induced errors (namely, charge transfer jitter and PWJ). The effect of feedback jitter can be further discussed in the frequency domain with the aid of Fig. 2.11 as follows.

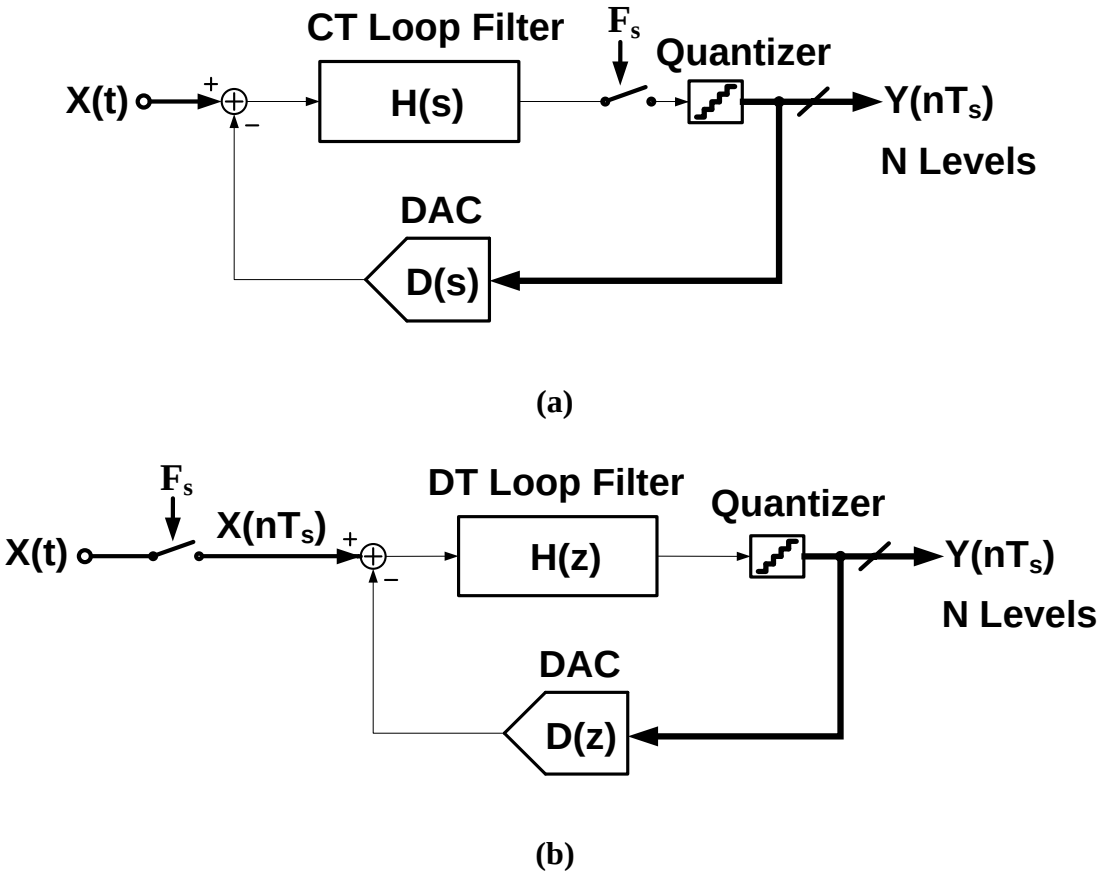


Fig. 2.10. ΔΣ Modulators. (a) Continuous-Time. (b) Discrete-Time.

[3] **Since the digital data coming in the feedback is usually sampled at the middle of the clock-cycle, sampled signal in the feedback can suffer aperture jitter only if the clock-jitter is ≥ $T_s/2$.**

Recall that the modulator feedback signal includes the in-band desired signal (input signal) and the high-pass shaped noise. Since the sampling process ideally is a multiplication in time, the spectra of the analog input signal and the clock signal convolve. Thus, the error generated by DAC clock PN has two main components, as illustrated by Fig. 2.11. First, the clock PN components close to the clock frequency modulates the in-band desired signal resulting in signal side-bands in the same manner like the PN of an upfront sampler [18]. Second, the wideband clock PN, modulates the high-pass shaped noise components and the modulation products fall over the desired band and hence elevate the in-band noise level.

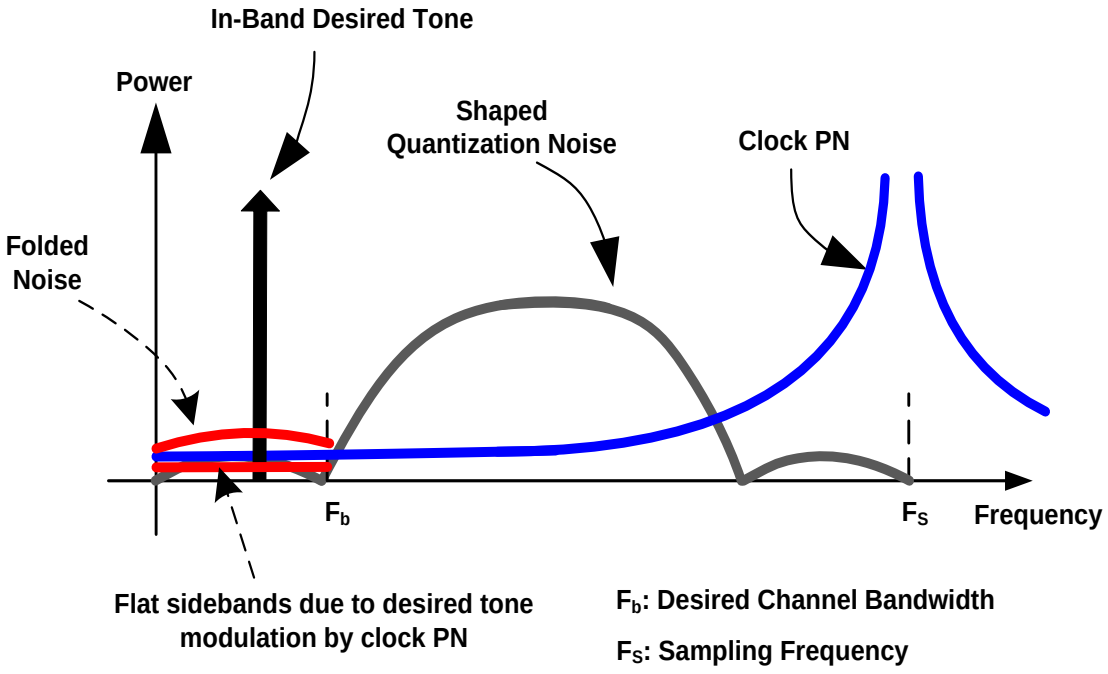


Fig. 2.11. Modulation of in-band desired signal and shaped quantization noise by phase-noise in the DAC sampling clock.

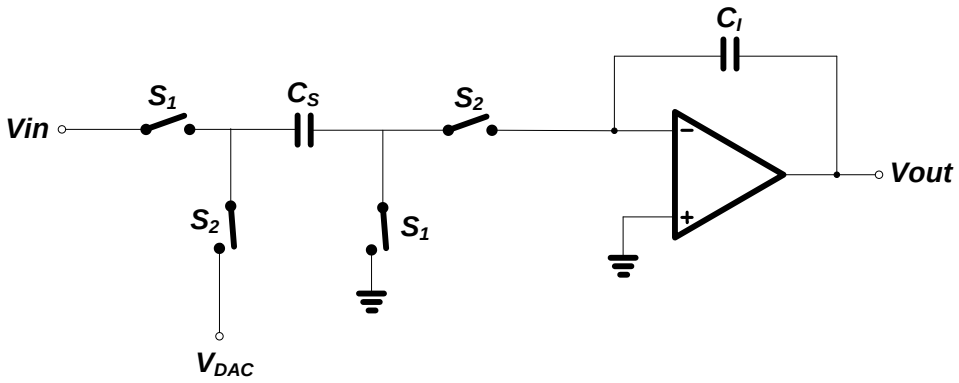


Fig. 2.12. Non-inverting switched-capacitor discrete-time integrator.

2.6.1 DT ΔΣ Modulators

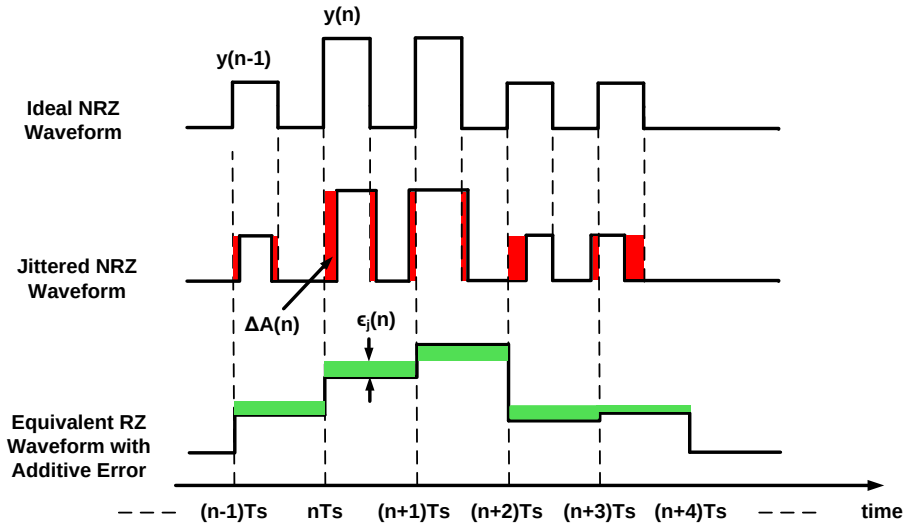
In DT ΔΣ modulators, the sampling takes place at the modulator input. The SC integrator in Fig. 2.12 is commonly used as an input stage for DT loop filters in ΔΣ modulators. The sampling aperture jitter errors due to the sampling switch (S_1) will be added to the signal at the input and hence will directly appear at the modulator output without any suppression. As mentioned earlier, the feedback signal (V_{DAC}) doesn't experience aperture jitter because the feedback signal is DT and also it has discrete amplitude levels. Thus, timing errors cannot result in a sampled value that is different from the original feedback one. Timing errors at switch S_2 cause charge transfer jitter errors being added at the input stage. However, the charge transfer jitter errors at S_2 are very small owing to the high robustness of the exponentially-decaying waveform to clock-jitter and moreover R_{ON} of the switches are usually very small resulting in a small time-constant τ which gives more jitter robustness to the waveform (recall the analysis given in the previous section).

According to the above discussion, the jitter induced noise in DT ΔΣ modulators is mainly dominated by the aperture error at S_1. At a given sampling speed, the only way to improve the performance of DT ΔΣ modulators is to improve the jitter performance of the clock generator which translates into significant increase in the total power consumption in case of ΔΣ ADCs targeting high resolution. On the other hand, for a given rms jitter, if the sampling frequency is reduced for the sake of improving tolerance to jitter errors, then to achieve high resolution at the resulting low OSR, the filter order and/or the quantizer levels need to be increased. This translates into significant power penalty too. Moreover, this approach wouldn't work for state-of-the-art wireless standards with continuously increasing channel bandwidths.

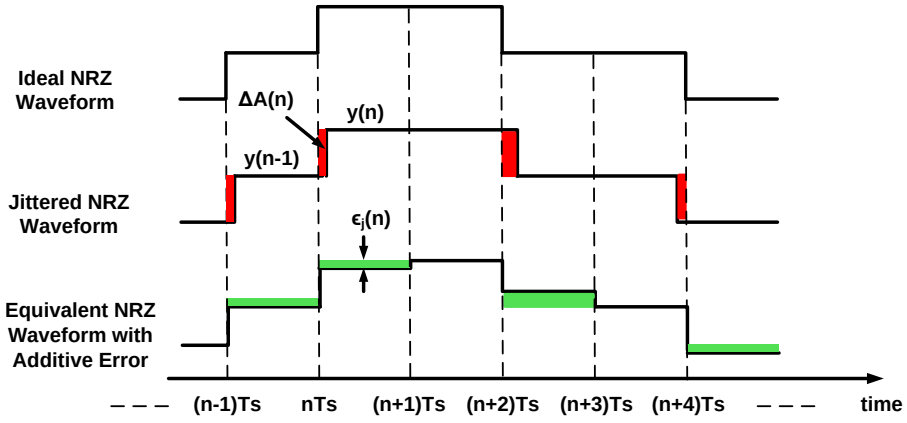
2.6.2 CT ΔΣ Modulators

In CT ΔΣ modulators, sampling occurs after the loop filter and hence sampling errors including aperture jitter are highly suppressed when they appear at the output because this is the point of maximum attenuation in the loop. However, CT ΔΣ implementations suffer from jitter errors added to the feedback signal. Particularly, in a CT ΔΣ modulator the DAC converts the quantizer output DT signal into CT pulses. The waveform coming from the CT DAC is fed to the loop filter to be integrated in the CT integrator stages. Thus, PWJ in the DAC waveform causes uncertainty in the integrated values at the outputs of the loop filter integrators. Rectangular waveform DACs are commonly used in CT ΔΣ structures due to their simple implementation and the relatively relaxed slew-rate (SR) requirement they offer for the loop filter amplifiers.

Return-to-zero (RZ) DACs are the most sensitive to feedback PWJ because the random variations are affecting the rising and falling edges of the waveform at every clock-cycle.



(a)



(b)

Fig. 2.13. Equivalent input referred error induced by pulse-width jitter [19]. (a) RZ DAC. (b) NRZ DAC.

The jitter sensitivity can be slightly reduced by using a NRZ DAC because in this case, the clock-jitter will be effective only during the clock edges at which data is changing. The equivalent input-referred errors induced by clock jitter in RZ and NRZ waveforms for a certain sequence of data are illustrated in Fig. 2.13.

As mentioned earlier, clock-jitter errors added in the feedback path are the most critical because they entail random phase modulation that folds back high-pass shaped noise components over the desired channel. For typical wideband CT ΔΣ modulators with NRZ current steering DACs in the feedback, the error induced by the PWJ in the DAC waveform can be up to 30% - 40% of the noise budget [10], [16], [20].

Convenience for low power implementations: CT ΔΣ modulators have gained significant attention in low power and high speed applications because they can operate at higher speed or lower power consumption compared to DT counterparts. Recall the relaxed gain bandwidth (GBW) product requirements they add on the loop filter amplifiers compared to DT implementations in which the loop filter is processing a DT signal and hence a GBW requirement on the amplifier is typically in the range of five times the sampling frequency. Moreover, sensitivity of CT ΔΣ modulators to DAC clock-jitter can be minimized by processing the DAC pulse or modifying its shape so as to alleviate the error caused by the DAC clock jitter [19]. That is, the achievable SNR of a CT ΔΣ modulator can be improved against clock-jitter without having to improve the jitter performance of the clock generator or to reduce the sampling speed and increase the order of the loop filter or the quantizer resolution. This definitely translates into

power savings because it avoids increasing the complexity of the clock generator or the ΔΣ modulator and hence avoiding extra power penalties[4].

2.7 Analysis of Jitter Effects in CT ΔΣ Modulators

This section provides detailed analysis for the effects of DAC clock-jitter on the performance of CT ΔΣ modulators for the most commonly used DAC types.

2.7.1 Return-To-Zero DAC Waveforms

Return-to-zero DAC waveforms are known to be robust to even-order nonlinearities resulting from mismatch between rise and fall times, as well as less sensitive to excess loop delay in the quantizer compared to NRZ waveforms [10]. However, as mentioned in previous section, they are the most sensitive to PWJ because the additive jitter induced errors are linearly proportional to the random timing errors at the rise and fall edges every clock-cycle, as illustrated in Fig. 2.13(a). The equivalent error induced by PWJ in a RZ DAC waveform is given by

$$\epsilon_j(n) = \frac{\Delta A(n)}{T_s} = y(n)\frac{T_s}{T_C}\frac{\left(\Delta t_r(n) + \Delta t_f(n)\right)}{T_s}, \tag{2.15}$$

where $\Delta A(n)$ is the area difference resulting from the error in the total integrated charge per one clock period T_s between the ideal and the jittered waveforms, $y(n)$ is the modulator output at the n^{th} clock cycle, T_C is the duty-cycle of the RZ pulse, and $\Delta t_r(n)$ and $\Delta t_f(n)$ are the random timing errors in the rise and fall edges, respectively, of the n^{th}

[4] This is provided that the solution adopted to improve the DAC tolerance to clock jitter errors is not adding high power overhead and thus not increasing the total power consumption.

DAC pulse. The amplitude of the DAC pulse varies inversely proportional with the pulse duty-cycle so that to supply a constant amount of charge (determined by Full-Scale (FS) voltage level of the quantizer) to the loop filter per clock-cycle. Following the procedure in [19], for a single tone $V_{sig} \cdot sin(\omega_{sig} t)$ at the input of the ΔΣ modulator, the integrated in-band jitter-induced noise power (IBJN) for a RZ DAC is given by

$$IBJN|_{RZ} = \frac{2}{OSR}\left(\frac{\sigma_j}{T_C}\right)^2 \left[\frac{{V_{sig}}^2}{2} + \frac{\Delta^2}{12} \cdot \frac{1}{2\pi}\int_{-\pi}^{\pi} \left|NTF\left(e^{j\omega}\right)\right|^2 d\omega\right]. \quad (2.16)$$

where σ_j is the rms jitter in the DAC sampling-clock, OSR is the oversampling ratio of the modulator, Δ is the quantization step of the loop quantizer, and NTF is the noise transfer-function of the modulator. From equation (2.16), the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

$$IBJN|_{RZ,due\ to\ input\ signal} = \frac{{V_{sig}}^2}{OSR}\left(\frac{\sigma_j}{T_C}\right)^2. \quad (2.17)$$

$$IBJN|_{RZ,due\ to\ shaped\ noise} = \frac{1}{OSR}\left(\frac{\sigma_j}{T_C}\right)^2 \frac{\Delta^2}{12\pi}\int_{-\pi}^{\pi} \left|NTF(e^{j\omega})\right|^2 d\omega. \quad (2.18)$$

From the expression in (2.16), it is evident that the IBJN decreases proportionally with the OSR and the duty cycle of the DAC pulse. Particularly, 1) as the OSR increases, the power spectral density (PSD) of the PWJ induced errors is reduced and hence the resulting integrated in-band noise is decreased accordingly, 2) the additive error in the amount of integrated charge in the loop filter varies linearly with the PWJ at the rise and fall edges by a factor roughly equal to the pulse amplitude (Fig. 2.13(a)), which is inversely proportional to T_C. The IBJN due to in-band signal component, given in (2.17), causes sidebands of the input signal to appear in the desired band. Also, from (2.18),

PWJ randomly modulating shaped noise results in noise folding back over the desired band and hence elevating the in-band noise level. In (2.16) and (2.18), the effect of the quantizer resolution is implicitly included in Δ^2.

2.7.2 Non-Return-To-Zero DAC Waveforms

Non-return-to-zero DACs are known to be highly sensitive to excess loop delay and also they result in even-order nonlinearities due to mismatch between rise and fall times, in contrast to RZ DAC waveforms. However, they are commonly used in CT ΔΣ modulators due to their simple implementation, relaxed SR requirement on the integrating amplifiers, and lower sensitivity to clock-jitter compared to RZ DACs. As illustrated by Fig. 2.13(b), in NRZ waveforms the clock-jitter will be effective only during the clock edges at which data is changing. Equivalent error induced by clock-jitter in a NRZ waveform is given by

$$\epsilon_j(n) = \frac{\Delta A(n)}{T_s} = (y(n) - y(n-1))\frac{\Delta t(n)}{T_s}, \tag{2.19}$$

where $\Delta t(n)$ is the random timing error in the clock edge of the $n^{\underline{th}}$ clock-cycle. From [19], for a single tone $V_{sig} \cdot sin(\omega_{sig} t)$ at the input of the ΔΣ modulator, the total IBJN for a NRZ DAC is given by

$$IBJN|_{NRZ} = 4 \cdot OSR \cdot BW^2 \cdot \sigma_j^2 \cdot \left[\frac{\pi^2}{2}\left(\frac{{V_{sig}}^2}{{OSR_{sig}}^2}\right) + \frac{\Delta^2 \cdot {\sigma_{NTF,RMS}}^2}{12}\right]$$

$$\leq 2\pi^2 \frac{{V_{sig}}^2 \cdot BW^2 \cdot \sigma_j^2}{OSR} + \frac{OSR \cdot BW^2 \cdot \Delta^2 \cdot {\sigma_{NTF,RMS}}^2 \cdot \sigma_j^2}{3}. \tag{2.20}$$

where BW is the input signal bandwidth, OSR_{sig} is the ratio of the sampling frequency to double the input signal frequency, and ${\sigma_{NTF,RMS}}^2 = \frac{1}{\pi}\int_{-\pi}^{\pi}\left[\left|NTF\left(e^{j\omega}\right)\right|^2 \cdot (1-\cos\omega)\right] d\omega$. Thus, the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

$$IBJN|_{NRZ,due\ to\ signal} \leq 2\pi^2 \frac{{V_{sig}}^2 \cdot BW^2 \cdot \sigma_j^2}{OSR}. \tag{2.21}$$

$$IBJN|_{NRZ,due\ to\ shaped\ noise} = \frac{OSR \cdot BW^2 \cdot \Delta^2 \cdot {\sigma_{NTF,RMS}}^2 \cdot \sigma_j^2}{3}. \tag{2.22}$$

From the expression in (2.21), the IBJN due to signal is inversely proportional with the OSR because, intuitively, as the OSR increases, less signal-related transitions will occur at the modulator output and hence less additive jitter noise will be generated. This note is applicable only to transitions at the modulator output in the frequency range of the input signal. For example, in case of DC inputs, the modulator output will exhibit limit cycles and yields discrete tones at the output spectrum [21]; however, these transitions at the output waveform are due to the shaped quantization noise and not the input signal. On the other hand, from (2.22), the IBJN due to shaped noise increases proportionally with the OSR because a higher OSR means more OOB shaped noise components will be modulated and fold back over the desired channel by the PN components at their respective frequencies. Therefore, the OSR needs to be optimized for better robustness to PWJ according to the contribution of each component (in-band signal and shaped noise). Also, the IBJN due to shaped noise is proportional to ${\sigma_{NTF,RMS}}^2$, and thus to minimize the PWJ, the aggressiveness of the NTF needs to be relaxed. This gives a

trade-off between quantization noise suppression and sensitivity to PWJ and hence a compromise is needed.

2.7.3 Switched-Capacitor-Resistor DACs with Exponentially-Decaying Waveforms

A commonly used solution to alleviate DAC sensitivity to PWJ is the SCR DAC with exponentially-decaying waveform, shown in Fig. 2.14. The exponentially-decaying waveform (Fig. 2.6) of the SCR DAC makes the amount of charge transferred to the loop per clock-cycle less dependent on the exact timing of the DAC clock-edges [16], [22].

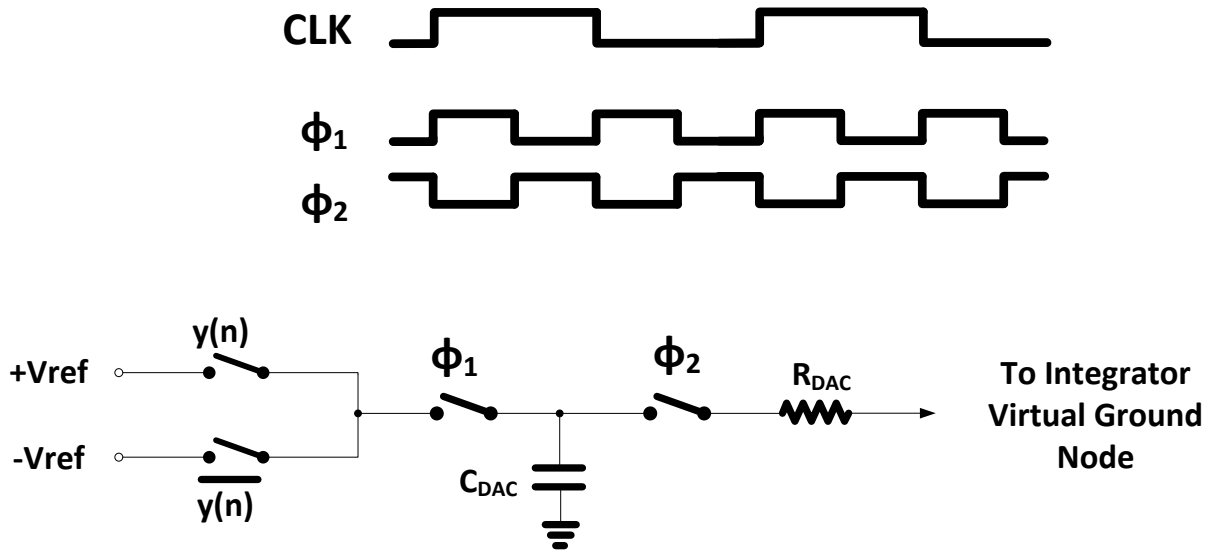


Fig. 2.14. SCR DAC.

For a given clock-cycle n, the instantaneous exponentially-decaying current $I_n(t)$ resulting from the charge transfer is given by equation (2.4). Recall that the

feedback value is sampled on C_{DAC} during the first clock half-cycle (when $\emptyset_1$ is high) and then the sampled voltage is transferred to loop filter during the second clock half-cycle (when $\emptyset_2$ is high). For a total integrated charge of $k_{DAC} \cdot y(n) \cdot T_S$ to be delivered by the SCR DAC during $\emptyset_1$ of clock-cycle n,

$$k_{DAC} \cdot y(n) \cdot T_S = \int_{\alpha T_s}^{\beta T_s} I_P \; e^{\frac{-(\beta-\alpha)T_s}{\tau}} dt = \tau \, I_P \left(1 - \; e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right). \tag{2.23}$$

where k_{DAC} is the feedback DAC gain coefficient. Therefore,

$$I_P = \frac{k_{DAC} \cdot y(n) \cdot T_S}{\tau \left(1 - \; e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)}. \tag{2.24}$$

However, in presence of timing error $\Delta t(n)$ in the pulse-width of the discharge phase $\emptyset_2$ in the $n^{\underline{th}}$ clock cycle, the equivalent input-referred additive error in the integrated charge is given by

$$\epsilon_j(n) = \frac{1}{T_S} \frac{k_{DAC} \cdot y(n) \cdot T_S}{\tau \left(1 - \; e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \int_{\beta T_s}^{\beta T_s + \Delta t(n)} e^{\frac{-(t-\alpha)T_s}{\tau}} dt$$

$$= \frac{k_{DAC} \cdot y(n)}{\left(1 - \; e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \, e^{\frac{-(\beta-\alpha)T_s}{\tau}} \left[1 - \; e^{-\frac{\Delta t(n)}{\tau}}\right], \tag{2.25}$$

which for $\Delta t(n) \ll \tau$ can be approximated by

$$\epsilon_j(n) \approx \frac{k_{DAC} \cdot y(n)}{\tau \left(1 - \; e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \, e^{\frac{-(\beta-\alpha)T_s}{\tau}} \Delta t(n). \tag{2.26}$$

If σ_j^2 is the variance of the timing error $\Delta t(n)$, then for a single tone $V_{sig} \cdot sin(\omega_{sig} t)$ at the input of the ΔΣ modulator, the power of the input-referred IBJN is given by

$$IBJN|_{SCR} = \frac{1}{OSR} \cdot \left[\frac{e^{\frac{-(\beta-\alpha)T_s}{\tau}}}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \right]^2 \cdot \sigma_j^2$$

$$\cdot \left[\frac{{V_{sig}}^2}{2} + \frac{\Delta^2}{12} \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} \left| NTF\left(e^{j\omega}\right) \right|^2 d\omega \right]. \quad (2.27)$$

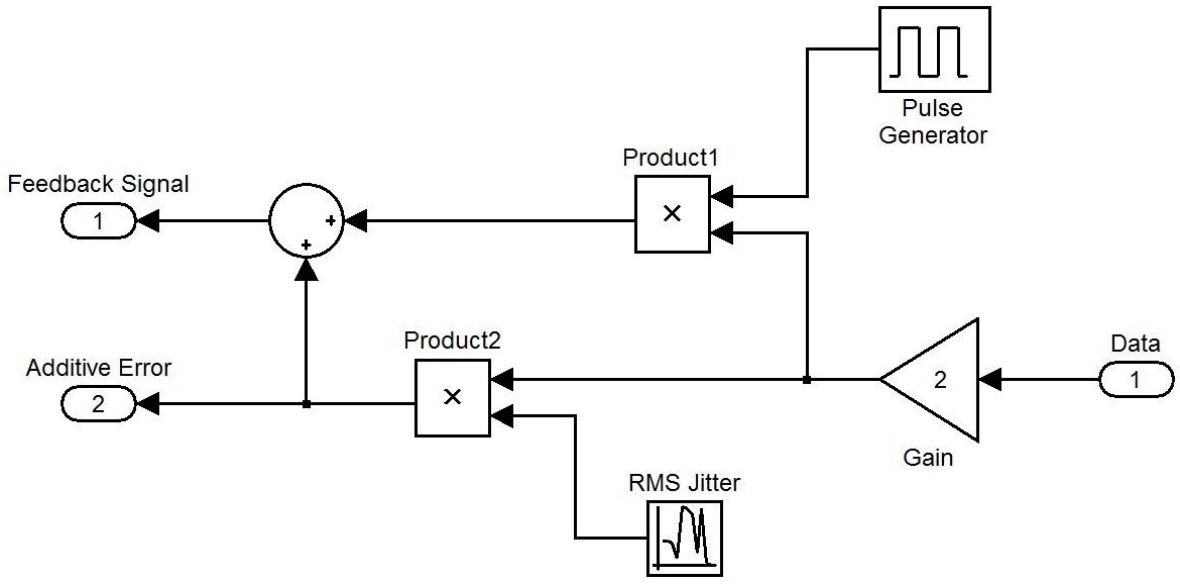
The expressions for the IBJN due to input signal and shaped quantization noise are given by

$$IBJN|_{SCR,due\ to\ input\ signal} = \frac{1}{OSR} \cdot \left[\frac{e^{\frac{-(\beta-\alpha)T_s}{\tau}}}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \right]^2 \cdot \sigma_j^2 \cdot \frac{{V_{sig}}^2}{2}. \quad (2.28)$$

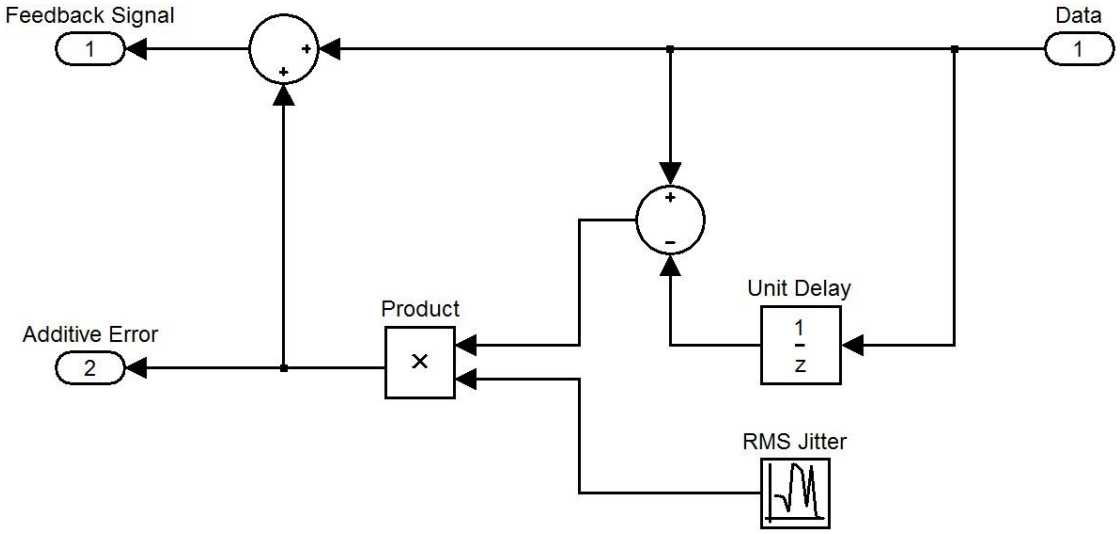
$$IBJN|_{SCR,due\ to\ shaped\ noise} = \frac{1}{OSR} \cdot \left[\frac{e^{\frac{-(\beta-\alpha)T_s}{\tau}}}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)} \right]^2 \cdot \sigma_j^2 \cdot \frac{\Delta^2}{12}$$

$$\cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} \left| NTF\left(e^{j\omega}\right) \right|^2 d\omega. \quad (2.29)$$

As expected, the sensitivity of SCR DACs to PWJ, given by (2.27)-(2.29) is the same as the RZ DAC case (2.16)-(2.18) but exponentially reduced. However, the increased peak current of the SCR DAC, given by (2.28), adds higher requirements on the SR and the GBW of the loop filter integrator [16, 23]. Moreover, CT ΔΣ modulators using SCR DACs have poor inherent anti-aliasing compared to those using CS DACs [24] due to the loading of the SCR DAC on the integrating amplifier input nodes. The hybrid SI-SCR DAC solution in [25] provides suppression to PWJ noise equivalent to that offered by SCR DACs without adding extra requirements on the SR or GBW of the integrating amplifier.

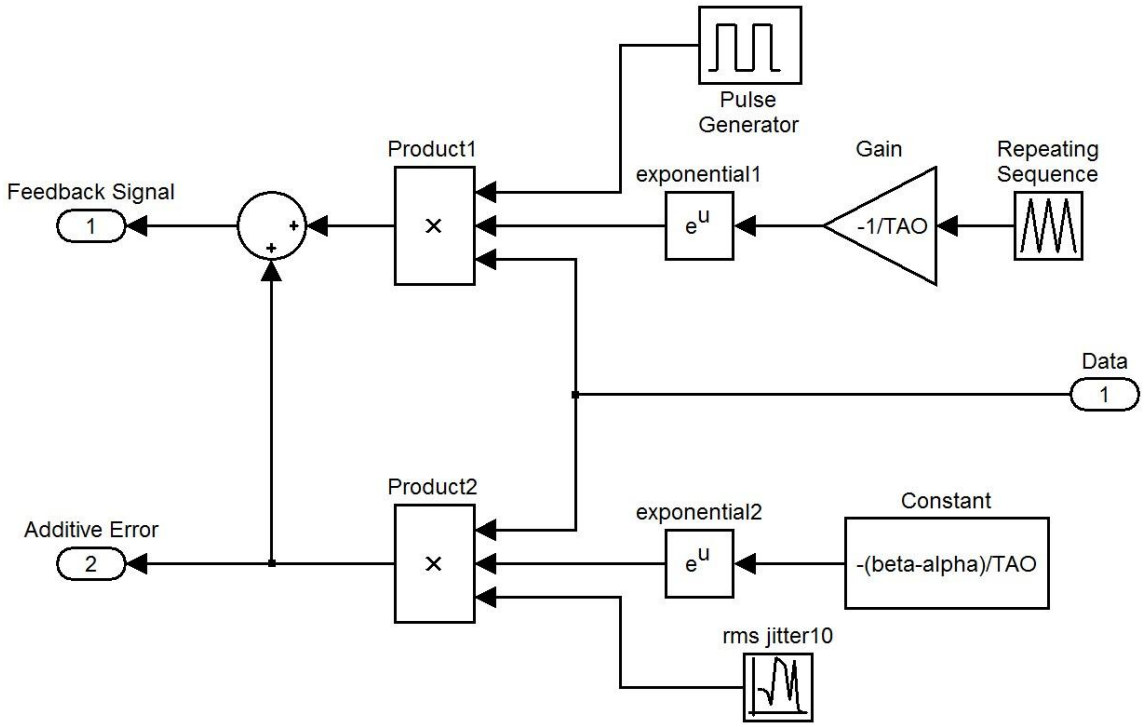


(a)



(b)

Fig. 2.15. Simulink Modeling for DACs and jitter induced additive errors in the feedback of a CT ΔΣ modulator. (a) RZ DAC. (b) NRZ DAC. (c) SCR DAC.



(c)

Fig. 2.15 Continued.

2.8 Modeling and Simulation of Jitter Effects in CT ΔΣ Modulators Using Matlab/Simulink

In this section, Matlab/Simulink models for the jitter induced errors in different DAC types are shown. The models are based on the expressions of the additive jitter errors developed in the previous section and will be verified by simulations. Fig. 2.15 shows the Simulink models for RZ, NRZ and SCR DACs, including the additive jitter errors based on the expressions in (2.15), (2.19), and (2.25), respectively. Note that these additive errors in the feedback should be multiplied by the gain coefficient of their respective feedback path. These models are examined through simulations in

Matlab/Simulink to verify their accuracy and compliance with the developed analysis. The feedforward third-order single-bit CT ΔΣ modulator in Fig. 2.16 is used as a test vehicle for the system-level simulations. The modulator operates at an OSR of 100 with a target ENOB of 13 bits over a baseband channel bandwidth of 1.92 MHz for the WCDMA standard. The noise budgeting for the ADC to achieve the required ENOB is given in Table 2.1. Table 2.2 lists the specifications and summary of the achievable performance of the modulator when an SCR DAC model is used with DAC time-constant $\tau = 0.1\,T_S$. Recall that an SCR DAC is a convenient option to provide robustness to clock-jitter and maintain the low percentage of the jitter induced noise in the noise budget. The DR and PSD plots of the modulator are given in Fig. 2.17 and Fig. 2.18. The maximum signal-to-noise-plus-distortion ratio (SNDR) is calculated as 80dB.

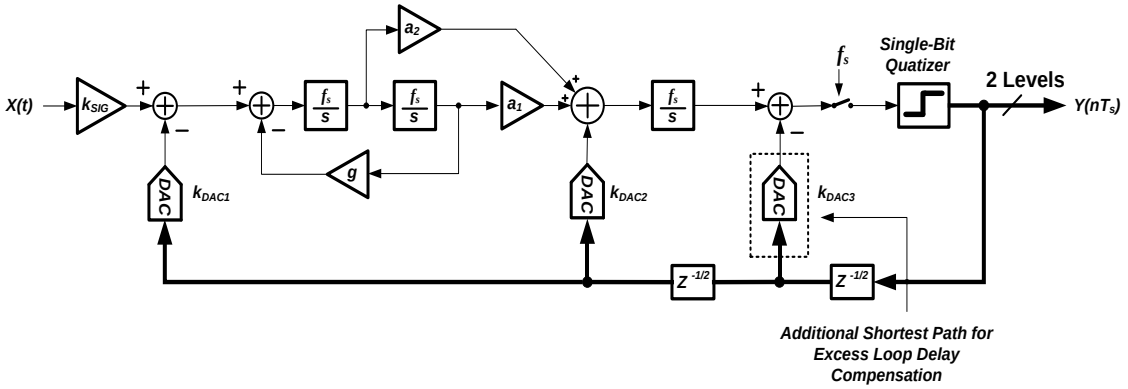


Fig. 2.16. Adopted modified feedforward CT single-bit ΔΣ modulator.

To examine the sensitivity of the modulator to clock-jitter for different DAC types by simulations, the appropriate model for the feedback DAC including the additive

jitter errors is chosen from the ones in Fig. 2.15, according to the adopted DAC type (RZ, NRZ, or SCR), and is added to the Simulink model of the complete modulator. The plots in Fig. 2.19 imply that for sufficiently large rms jitter in the DAC sampling-clock, the IBJN increases significantly and dominate the total in-band noise (IBN).

Table 2.1. Modulator noise budget

Noise/Distortion Source	Noise Budget	SNR
Quantization Noise	10%	90 dB
Thermal Noise	50%	83 dB
Jitter Induced Noise	10%	90 dB
Nonlinearity induced Distortion	20%	87 dB
Others	10%	90 dB

Table 2.2. Modulator specifications and performance summary

Property	Value
Sampling Frequency	384 MHz, RMS Jitter 10 ps
Signal Bandwidth	1.92 MHz
Oversampling Ratio (OSR)	100
ENOB	13
Peak SNDR	80 dB
Dynamic Range	84 dB
SFDR	83 dB

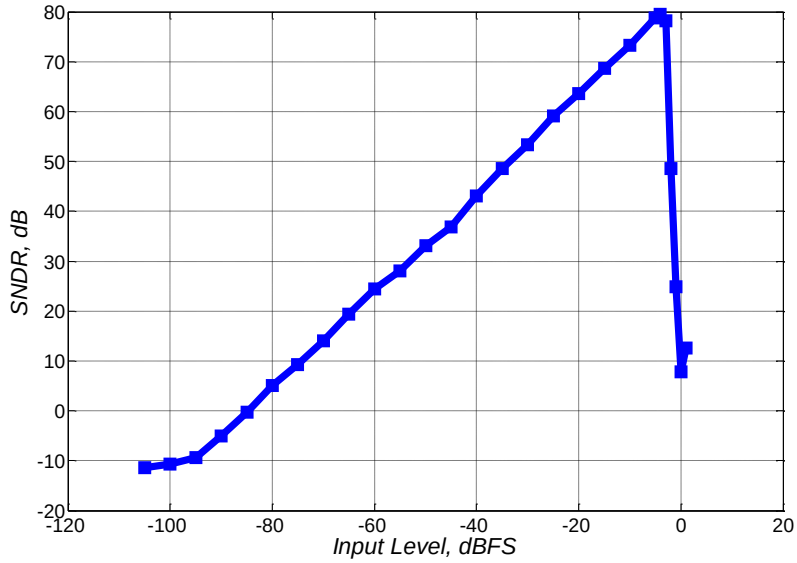


Fig. 2.17. Dynamic-range of the adopted ΔΣ modulator.

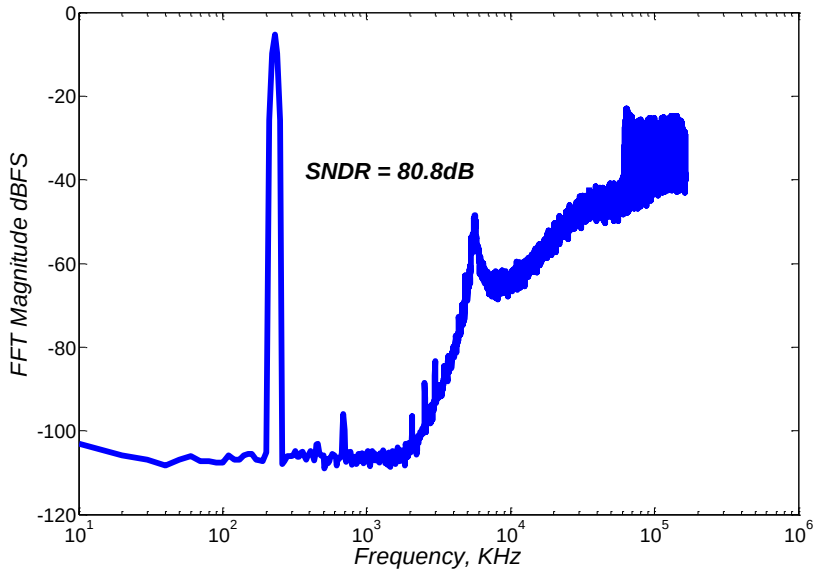
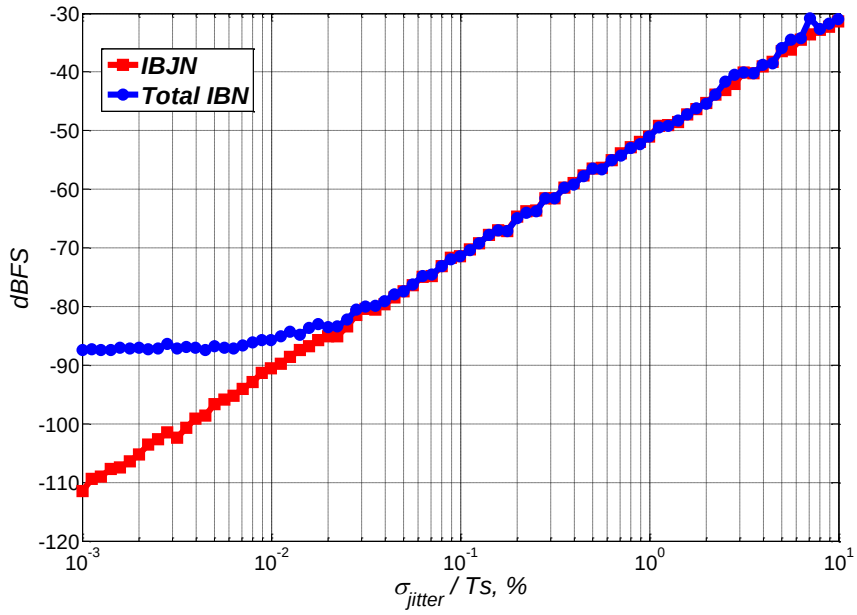


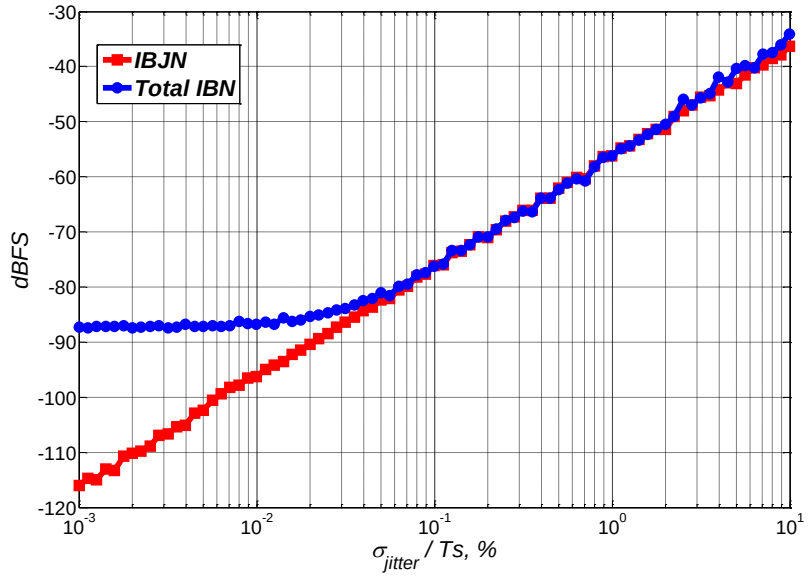
Fig. 2.18. PSD at the modulator output calculated using 32768 FFT points with 16 averages. $\boldsymbol{Signal\ Amplitude = -4\ dBFS, Signal\ Frequency = 270\ KHz.}$

For the SCR DAC, it can be seen from the plots in Fig. 2.19(c) that the robustness to clock-jitter degrades proportionally with the DAC time-constant τ, as discussed earlier in the analysis. To compare the robustness to clock-jitter in the three DAC types, IBJN plots are combined together in Fig. 2.20, and it is evident that the SCR DAC is the most tolerant to DAC jitter while RZ DAC is the most sensitive.

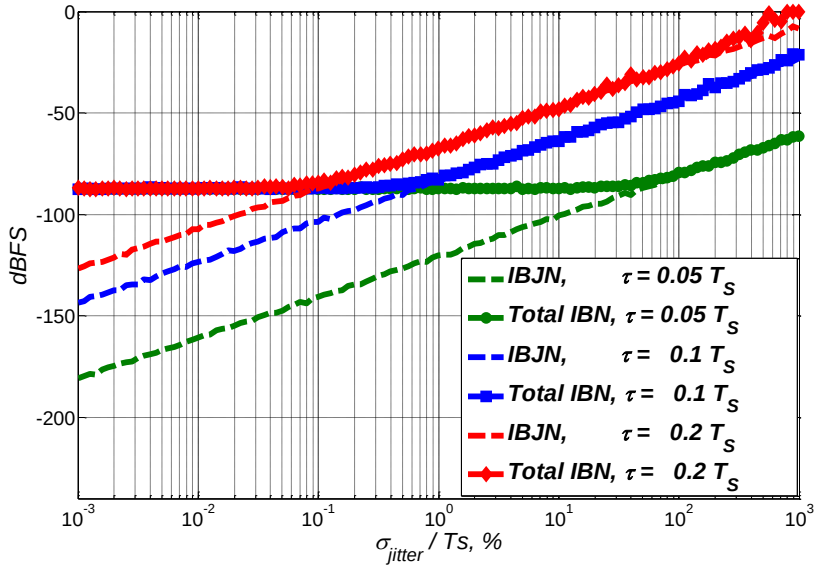


(a)

Fig. 2.19. Sensitivity plots of the ΔΣ modulator in Fig. 2.16 to clock-jitter in the DAC. $Signal\ Amplitude = -4\ dBFS$, $Signal\ Frequency = 1.9\ MHz$. (a) RZ DAC. (b) NRZ DAC. (c) SCR DAC.



(b)



(c)

Fig. 2.19 Continued.

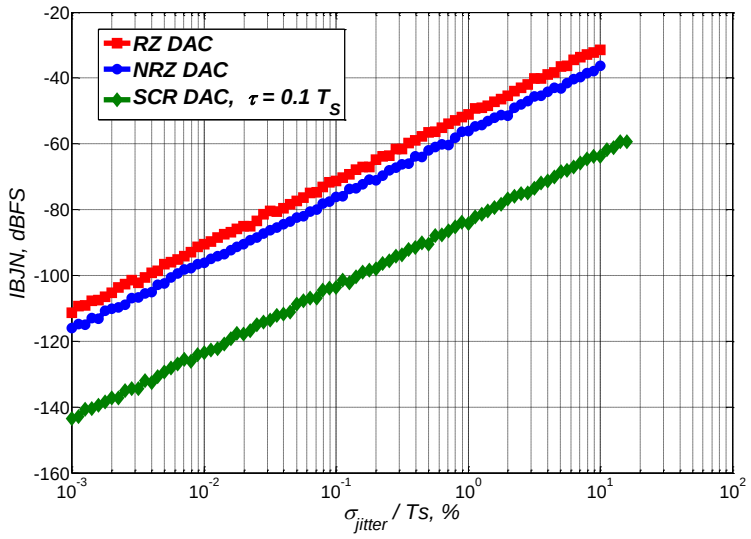


Fig. 2.20. IBJN plots for the ΔΣ modulator in Fig. 18 using different DAC types. $\boldsymbol{Signal\ Amplitude = -4\ dBFS, Signal\ Frequency = 1.9\ MHz.}$

3. EFFECTS OF BLOCKERS ON LOOP DYNAMICS AND DYNAMIC-RANGE BUDGETING OF CONTINUOUS-TIME DELTA-SIGMA MODULATORS[*]

3.1 Introduction

For a given wireless standard, the ADC used in the wireless receiver needs enough DR to satisfy two main requirements: a) proper signal flow: process the maximum power at the ADC input without being saturated or overloaded, and b) minimum signal detection: maintain the required bit-error-rate (BER) for the minimum detectable desired signal (sensitivity). For typical ΔΣ modulators, handling in-band, blocker-free signals, the requirements on the signal flow within the modulator and the signal detection at the modulator output set the design specifications on the modulator building-blocks based on the DR of the input desired signal. However, in presence of OOB blockers at the ADC input, the ΔΣ modulator can suffer signal flow and/or detection blocking.

In essence, to maintain proper operation of a ΔΣ modulator, it is necessary to keep the loop dynamics in terms of signal swing and speed within the appropriate ranges that can be provided by the adopted circuits at acceptable performance. Swing and settling speed limitations of the ΔΣ modulator building-blocks can block the signal propagation through the ΔΣ loop and thus yield output bit streams that do not reflect the actual input signal. Particularly, signal flow blocking effects cause the signal swings

[*] Part of this chapter is reprinted with permission from "Sensitivity Analysis of Continuous-Time ΔΣ ADCs to Out-of-Band Blockers in Future SAW-Less Multi-Standard Wireless Receivers," by Ramy Saad, Diego Luis Aristizabal-Ramirez, and Sebastian Hoyos, September 2012. *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 9, pp. 1894-1905.

within the loop (either at internal nodes or modulator output) to clip and/or vary at rates imposed by circuit speed limitations and not proportional to the input signal, hence resulting in substantial distortion and can potentially drive the loop unstable. Moreover, when the signal flow is blocked, the modulator output is no longer tracking the input, and hence the feedback function is lost and the loop is said to be virtually broken. To recover from loop blocking (e.g. by resetting), usually a finite recovery time is needed to restore the loop normal operation again, which translates into delays and unrecoverable data frames loss in wireless receivers.

In this section, the sensitivity of the loop operation/dynamics to the signal swing and settling speed limitations and the ADC DR budgeting in presence of large OOB blocking signals are analyzed. The section flow is organized as follows. Section 3.2 discusses the effects of OOB blockers on signal propagation in the ΔΣ modulator loop according to limited swing headroom of the adopted circuits. The performance sensitivity of CT ΔΣ modulators to slew-rate (SR) of loop filter amplifiers in presence of large OOB blockers is analyzed in section 3.3. Section 3.4 explains the link budget analysis to determine ADC DR requirements in presence of interferers. Finally, conclusions are drawn in section 3.5. Analysis and dicussions provided in the section are verified by CT simulations in Matlab/Simulink and simulations results show good agreement with theoritical discussions.

3.2 Limited Signal Swing and Saturation

3.2.1 Loop Filter Saturation

In ΔΣ modulators, signal clipping due to limited signal swing at the outputs of loop filter stages is caused by large inputs for which the feedback waveform coming from modulator output cannot cope with the incoming signal excursions. In essence, for sufficiently large input signals, high residual (error) signal is applied to the loop filter causing saturation at outputs of some or all filter stages. The sensitivity of the performance of ΔΣ modulators to signal clipping is twofold. First, if any of the feedforward paths in the loop filter gets saturated, the signal experiences a hard nonlinearity that yields substantial distortion at the modulator output as well as severely increasing baseband noise [26]-[28], especially if the signal clipping happens at an early stage in the loop filter. Second, if all the feedforward paths within the loop filter suffer signal clipping, the modulator output will be isolated from the input signal such that the resulting output bit stream does not carry the information in the modulator input signal. As a result, the feedback function is lost and the loop is virtually broken. This problem is the most critical consequence of signal clipping in ΔΣ modulators because it entails a non graceful degradation in the operation [29], [30] in which the modulator behavior is altered [31]. A finite recovery time is needed to restore the normal loop operation after recovery from saturation (e.g. by resetting), which translates into delays and unrecoverable data loss in wireless receivers.

Based on the foregoing discussion, the sensitivity of ΔΣ modulators to signal

clipping in the loop filter is mainly determined by the response of the loop filter to the input signal. Recall that saturation happens because the feedback cannot follow up with the input signal and at the most critical case in which all the feedforward paths of the loop filter are saturated, the feedback is virtually not functional. Therefore, to determine the severity of OOB blockers on the performance of CT ΔΣ modulators in terms of signal clipping, it is necessary to study the response of *loop filter feedforward paths* to OOB blocker signals.

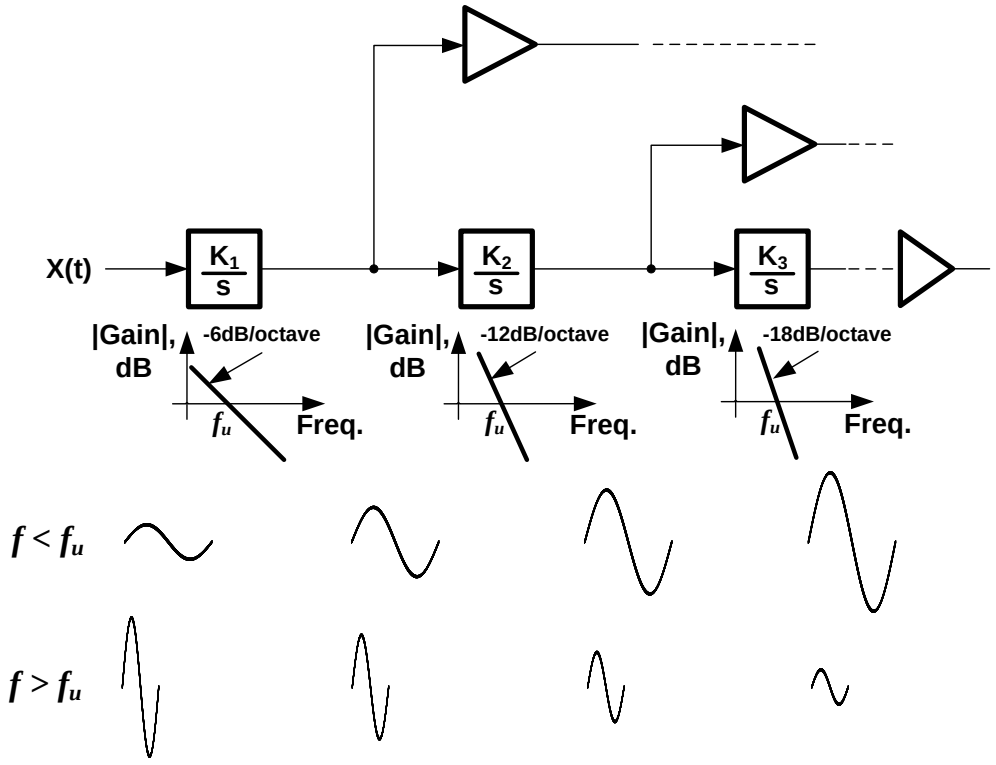


Fig. 3.1. Magnitude responses of feedforward paths of loop filter to input sinusoids.

In general, feedforward paths in a CT loop filter usually include a cascade of integrators, whose number varies from 1 to *n*, where *n* is the order of the loop filter. For

a chain of m integrators each with unity-gain frequency f_u, the gain at a given frequency f is proportional to $\left(f_u/f\right)^m$. Thus, for in-band desired signals, where f is always smaller than f_u, the signal level is amplified as it propagates through the chain, as illustrated in Fig. 3.1. Traditionally, scaling is applied to the loop coefficients, during system-level design of ΔΣ modulators, so that to optimize the signal swings at the integrators outputs for maximum input levels and avoid clipping [32].

When an OOB blocker is applied to the ΔΣ modulator, depending on the blocker frequency (f_{BLK}), whether it is higher or lower than f_u, the OOB signal will be either amplified or attenuated, respectively. For typical wireless standards and integrator gains in ΔΣ modulators, blockers with $f_{BLK} < f_u$ are those coming from signals belonging to the same wireless standard of the desired channel and therefore their values are controlled by the blocker profile and can be easily extracted from the standard documentations [33]-[35]. Thus, they can be considered in the ADC DR budgeting (explained in section 3.4) and also in the loop coefficient scaling to prevent signal clipping. However, interferers coming from frequencies > f_u can belong to other wireless standards/bands. Even if these blockers are weak, they can be many due to existence of several wireless applications serving various needs of consumers in a given area and hence they can sum up to a large OOB blocking power. Consequently, critical OOB blocking power is that coming from other wireless standards (frequencies > f_u). Thus, from now on the term OOB will be used to denote blocker signals with $f_{BLK} > f_u$. OOB signals are attenuated as they propagate through the integrators chain and hence

earlier integrating stages are more prone to clipping due to large OOB blockers than later ones, as illustrated by Fig. 3.1. This fact indicates that signal clipping due OOB blockers is very critical and can block loop operation for either type of CT ΔΣ modulator architectures given in Fig. 3.2 because the first stage is common for all feedforward paths in the loop filter.

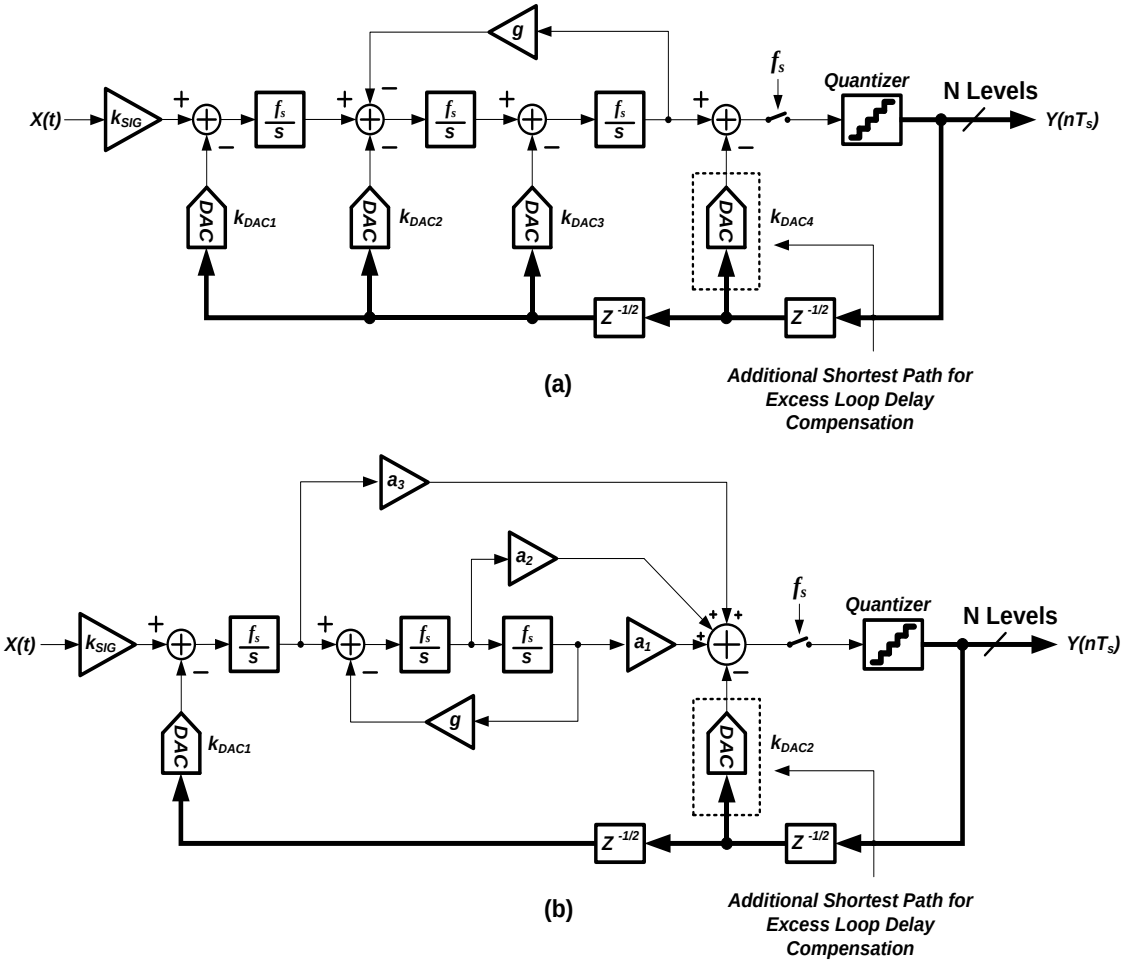


Fig. 3.2. CT ΔΣ modulators examples (third-order). (a) Feedback structure. (b) Feedforward structure.

To show the effect of OOB blockers on signal clipping in the loop filter stages, the feedback CT ΔΣ modulator in Fig. 3.2(a) is simulated with the following specifications: 6-levels quantizer, OSR=42, sampling frequency $f_s = 16.8\,MHz$, $f_u = 1.05\,MHZ$, integrator saturation limits $V_{SAT} = \pm 1.5\,FS$. A weak input desired tone, $A_{SIG} = -75\,dBFS$, at $f_{SIG} = 31\,KHz$ and an OOB blocker tone at $f_{BLK} = 3.96\,MHZ$ are applied to the input terminal of the modulator. The input desired signal has been chosen to be relatively very weak so that for large OOB blocker levels the signal swings at the outputs of the loop filter stages are dominated by the blocker and hence the effect of the blocker on the signal swing and the resulting clipping can be clearly observed.

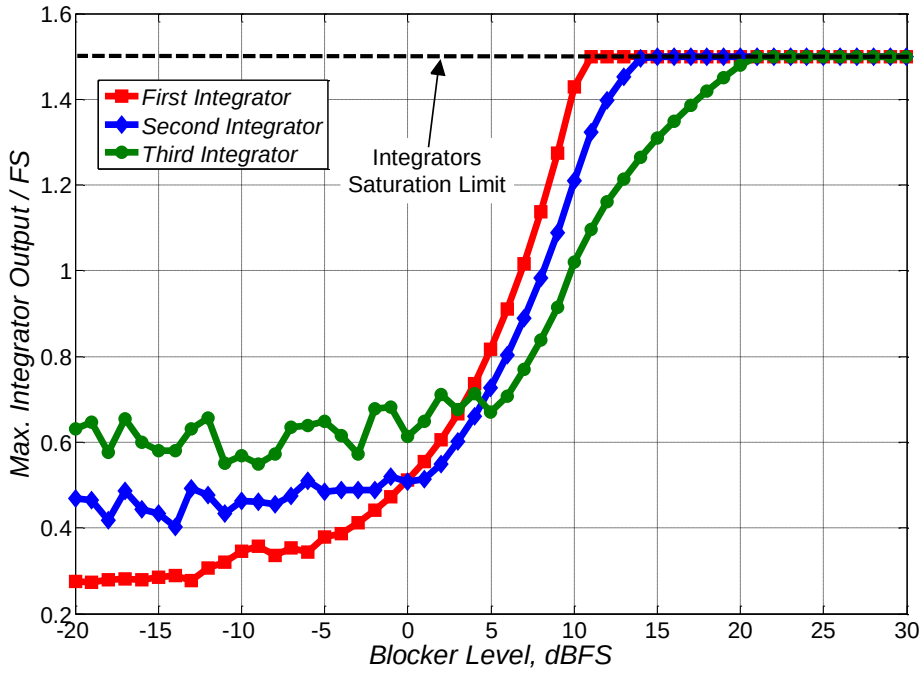


Fig. 3.3. Maximum integrator output swing variation with the OOB blocker level, $f_{BLK} > f_u$.

The results are obtained through CT simulations in Matlab/Simulink. The plots in Fig. 3.3 show the variations in the maximum signal swings at the outputs of the integrators with the OOB blocker level. As expected, earlier integrators in the chain saturate first. For OOB blocker levels $< 4\ FS$, the swing at each stage in the loop filter is higher than the preceding ones because the attenuated blocker component at the outputs of loop filter stages is very weak. In this case the analysis of the signal swing reduces to the typical case of any ΔΣ modulator where the signal swing, dominated by the amplified desired signal, increases as signal propagates deeper in the loop filter.

3.2.2 Quantizer Overloading

A quantizer is said to be overloaded if the quantization noise added at the quatizer output exceeds $\Delta/2$ [30], [31], [36], where Δ is the quantization step. Thus, to maintain a quantizer not overloaded, the input signal level to the quantizer shouldn't exceed $FS + \Delta/2$, where FS is the maximum full-scale output level of the quantizer. If the loop quantizer is overloaded by a certain value, the ΔΣ modulator will go unstable [31].

In typical ΔΣ modulators, this problem is avoided by controlling the input signal level so that not to exceed the maximum stable amplitude (MSA) [29] for which the loop quantizer get overloaded. However, in presence of OOB blockers, residual blocker components appearing at the loop filter output can overload the quantizer and drive the loop unstable. This problem is more critical in feedforward CT ΔΣ structures (Fig. 3.2b)

than feedback counterparts (Fig. 3.2a) because the OOB attenuation offered by the loop filter is inadequate due to low-order feedforward paths.

3.3 Finite Slew-Rate of Loop Filter Amplifiers

Slew-rate is a large signal, purely nonlinear effect that shows up in active integrators due to limited current capability of driving amplifiers [32]. In a ΔΣ modulator, the outermost integrator is the most critical one, whereas errors entering at later integrators are suppressed. Thus, in the following, only the SR of the first integrator is taken into account. The maximum SR at the first integrator output is given by:

$$SR|_{int1} = \left| {dV_{out1}}/{dt} \right|_{max} \geq f_s \cdot (k_{SIG} V_{SIG} + k_{DAC1} V_{FS}) \,, \tag{3.1}$$

where V_{out1} is the voltage at the output of the first integrator, k_{SIG} and k_{DAC1} are the scaling coefficients for the feedforward and feedback input signals to the first integrator, respectively, V_{SIG} is the input signal amplitude and V_{FS} is the full-scale feedback voltage. In typical ΔΣ modulators, V_{SIG} is always controlled to be less than the maximum stable amplitude (MSA) voltage level V_{MSA} which is $< V_{FS}$. For the first integrator stage in the loop filter, the value of k_{DAC} is $\geq k_{SIG}$, and the ratio between them is determined according to the feedback DAC waveform [33]. Thus, the SR is mainly limited by the feedback DAC peak current [33]. However, in presence of blockers, the input signal to the modulator can include OOB signals with amplitudes $> V_{FS}$. Thus, more stringent requirements are imposed on the SR of the first integrator, depending on the maximum amplitude of the OOB blockers.

If slewing happens at the integrator output, the combined waveform including the desired in-band signal and the OOB blockers will experience hard nonlinearity due to nonlinear settling. This will give rise to substantial distortion at the modulator output as well as dramatic increase in the noise floor due to noise leakage [34]. The problem of increased SR requirements caused by OOB blockers is remedied in later integrators for two main reasons. First, the errors coming from later stages are shaped by previous ones. Second, the OOB signals are attenuated as they propagate in the loop filter chain.

CT simulations in Matlab/Simulink have been carried out using different wanted signal and OOB blocker levels to illustrate the foregoing argument. The CT ΔΣ modulator in Fig. 3.2(a) has been simulated using the following specifications: 6-levels quantizer, oversampling ratio $OSR = 42$, and sampling frequency $f_s = 16.8\,MHz$. An input desired signal at frequency $f_{SIG} = 31\,KHz$ and OOB blocker tone with frequency $f_{BLK} = 3.96\,MHZ$ are applied to the ΔΣ modulator input. The integrator is modeled as an active-RC integrator using a conventional op-amp stage. The effects of the finite DC gain (A_{DC}) and gain-bandwidth product (GBW) of the op-amp are included by using the following first-order transfer function for the amplifier [32]

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_P}}, \quad GBW = A_{DC}\,\omega_P \;\; rad/sec, \tag{3.2}$$

where ω_P is its dominant pole of the op-amp circuit. Thus, for an integrator with multiple inputs coming from feedforward and feedback paths, the transfer function of the i^{th} input path of the integrator model is given by

$$H_i(s) = \frac{k_i f_s}{\frac{s^2}{GBW} + s\left[1 + \frac{1}{A_{DC}} + \frac{\sum_{l=1}^{n} k_l f_s}{GBW}\right] + \frac{\sum_{l=1}^{n} k_l f_s}{A_{DC}}}, \tag{3.3}$$

where k_i is the integrator gain coefficient seen by the $i^{\underline{th}}$ input path. The effect of SR is modeled by decomposing (3.3) into the product of two transfer functions as follows.

$$\begin{aligned} H_i(s) &= D_i(s) \times G_i(s) \\ &= \frac{s\, k_i f_s}{\frac{s^2}{GBW} + s\left[1 + \frac{1}{A_{DC}} + \frac{\sum_{l=1}^{n} k_l f_s}{GBW}\right] + \frac{\sum_{l=1}^{n} k_l f_s}{A_{DC}}} \times \frac{1}{s} \end{aligned} \tag{3.4}$$

In particular, the integrator transfer function is modeled as a cascade of a differentiated version of (3.3) $D_i(s)$ followed by a lossless integrator $G_i(s)$ to compensate for the differentiation. Thus, the output of the first product $D_i(s)$ gives the rate of change of the signal swing at the integrator output. Then, the SR effect can be included by applying the limitation on the rate of change at the output of $D_i(s)$ in the time-domain as follows. Let $x(t)$ denote the input of the integrator $H_i(s)$ in the time-domain and $d_i(t)$ is the time-domain equivalent representation of $D_i(s)$, then the output of $D_i(s)$ in the time- domain is given by

$$y(t) = x(t) * d_i(t), \tag{3.5}$$

where $*$ denotes convolution. The time-domain expression for the signal applied to $G_i(s)$ is given by

$$z(t) = \min\big(SR, y(t)\big), \tag{3.6}$$

where SR is the slew-rate value. Recall that $z(t)$ is the rate of change of the signal swing at the output of $h_i(t)$, where $h_i(t)$ denotes the time-domain equivalent of $H_i(s)$. The condition in (3.6) limits the maximum rate of change at the integrator output to the SR.

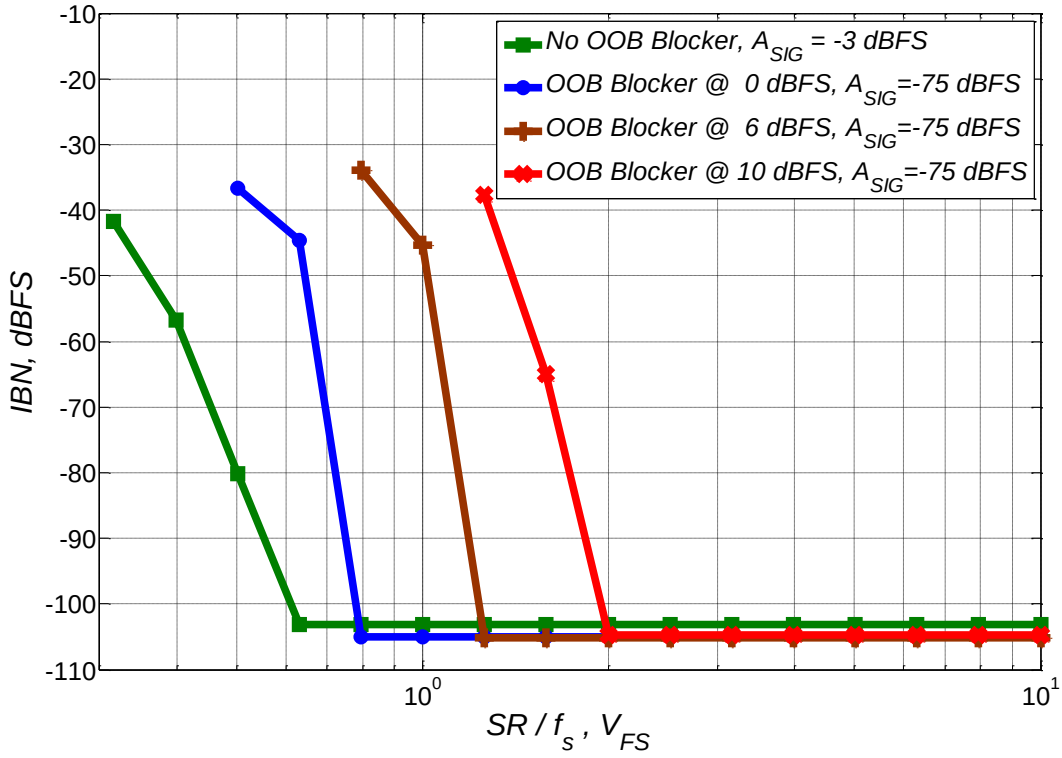


Fig. 3.4. IBN of a third-order CT modulator due to SR of the first integrator stage in presence of OOB blockers, $f_{SIG} = 31\ KHz$.

Then, the lossless integration in $G_i(s)$ compensates for the differentiation included in $D_i(s)$ to obtain eventually the actual integrator transfer function $H_i(s)$. The lossless integrator compensates the effect of differentiation and provides the actual signal seen at the output of the active-RC integrator. The SR limitation imposed by the wanted signals is obtained by simulating the modulator using an in-band input tone whose amplitude is equal to the MSA (-3 dBFS). In presence of an OOB blocker tone, a weak desired signal (-75 dBFS) is used so that the signal swing at the first integrator is dominated by the OOB blocker and hence the SR limitations added by the blocker signal can be observed.

Simulation results show that as the OOB blocker level increases so does the minimum required SR at the first integrator stage.

3.4 Dynamic-Range and Link Budgeting

Figure 3.5 shows the typical DR budgeting for an ADC in a wireless receiver. The detection signal-to-noise ratio (SNR) is the minimum SNR that achieves the BER specified by the standard according to the modulation scheme. However, in reality, noise in the receiver front-end sets the detection SNR, and to limit further SNR degradation by the ADC noise to about 0.1 dB, the ADC noise level should be (~ 15-20 dB) well below the noise level dictated by the detection SNR [37]. A 6-10 dB headroom margin is taken into account, below the full-scale (*FS*) level of the ADC, to cover DC offsets, baseband gain step error, fading, and transient signal/envelope variations. Some modulation schemes, like OFDM, have a typical peak-to-average ratio (PAR) in the range of 12-17 dB [30], [31], depending on the number of sub-channels. The ADC DR should account for this value to avoid signal compression or clipping.

Traditionally, owing to the baseband channel filtering and blocker rejection, the signal range is determined only by the input range of the wanted channel:

$$DR_{ch} = P_{ch,max} - P_{ch,min}\ , \tag{3.7}$$

where $P_{ch,min}$ and $P_{ch,max}$ are the minimum and maximum signal power in the wanted channel at the ADC input, respectively, according to the adopted standard and front-end gain. However, in presence of blockers (adjacent channels, alternate channels, or OOB), the residual dynamic-range DR_{res} [11] is added (see Fig. 3.8) to handle the interferer

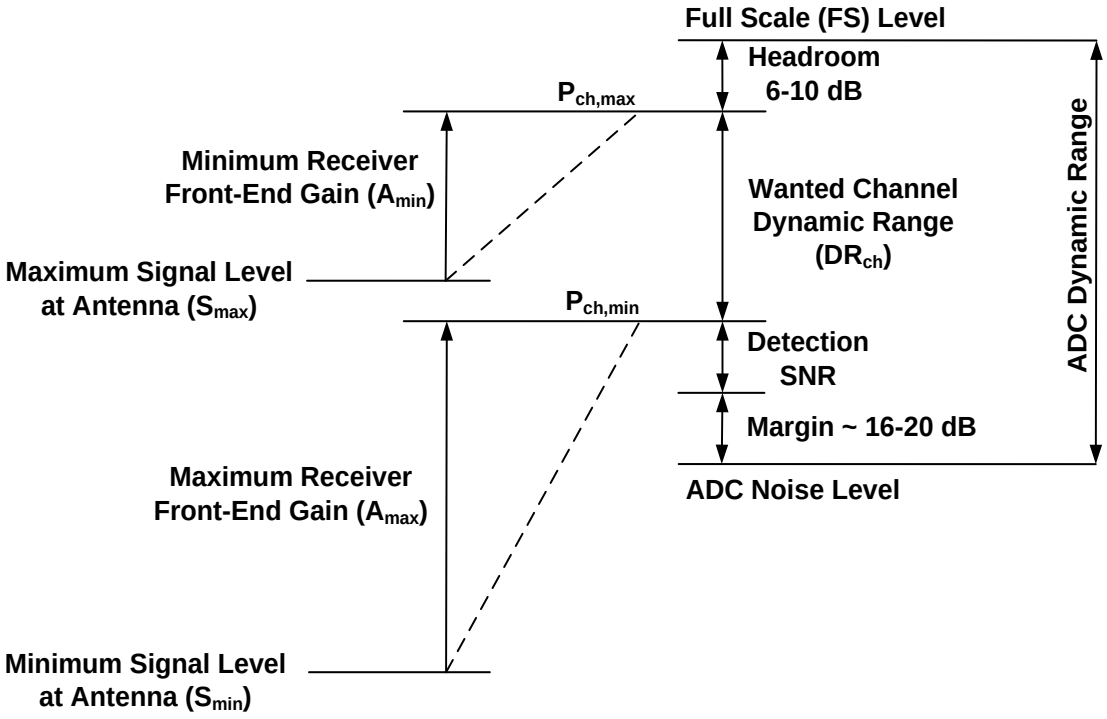


Fig. 3.5. Conventional ADC dynamic range budgeting.

components appearing at the ADC output, and is given by

$$DR_{res} = \int_{Entire\ Spectrum} P_{BLK}(j\omega) \cdot |STF(j\omega)|^2 \quad d\omega\,, \tag{3.8}$$

where $P_{BLK}(j\omega)$ is the blocker power at frequency ω at the ADC input and $STF(j\omega)$ is the magnitude of the modulator signal-transfer-function (STF) from the modulator input to the loop filter output at frequency ω. According to the receiver outline in Fig. 1.1, which is re-drawn in Fig. 3.6, where minimal filtering is offered in the front-end, large blocking power is expected to appear at the ADC input.

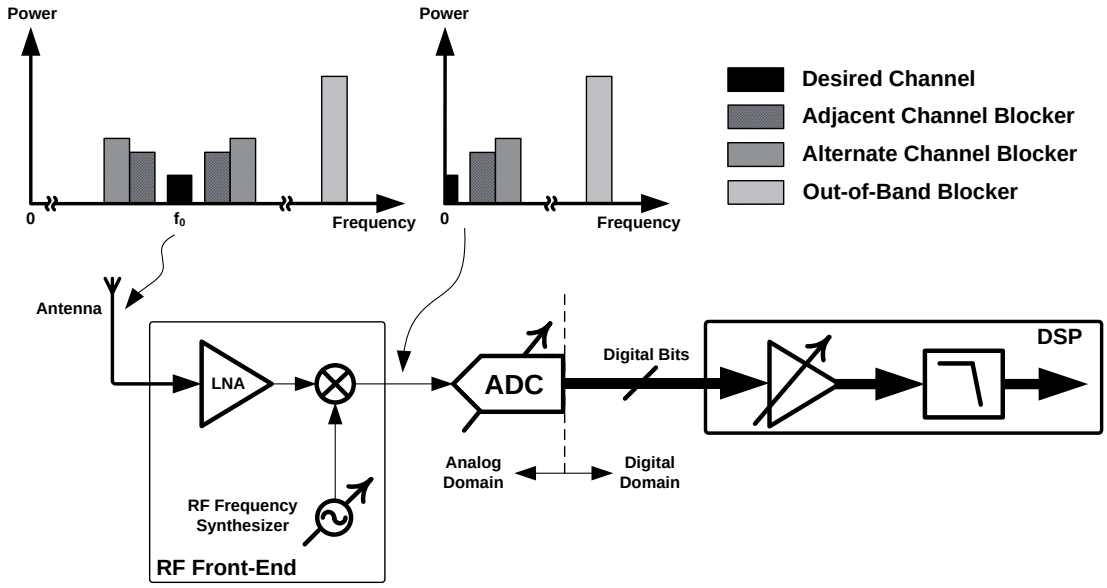


Fig. 3.6. Candidate architecture for SAW-less multi-standard/multi-band and software-defined radio receivers.

Figure 3.7 shows the magnitude responses of the STFs for the CT ΔΣ modulators in Fig. 3.2. The strength of OOB blocker suppression at a given blocker frequency varies according to the magnitude frequency response of the modulator STF. Owing to the higher OOB attenuation offered by CT feedback ΔΣ modulators, large OOB blocking power appearing at the ADC input can be adequately suppressed and become comparable to the maximum input of the desired channel or even much weaker when they appear at the output of the modulator. As a result, the estimation of DR_{res} should consider the effect of the blocker attenuation by the STF, as given in (3.8), to avoid overly pessimistic estimation of the ADC DR. Figure 3.8 illustrates the link budget analysis for calculating the required ADC DR according to the receiver outline given in Fig. 3.6. In presence of large OOB blockers at the ADC input, the sensitivity of the DR

to the modulator STF attenuation at the OOB blocker frequency suggests that feedback ΔΣ modulators are convenient choice to relax the DR requirement on the adopted ADC.

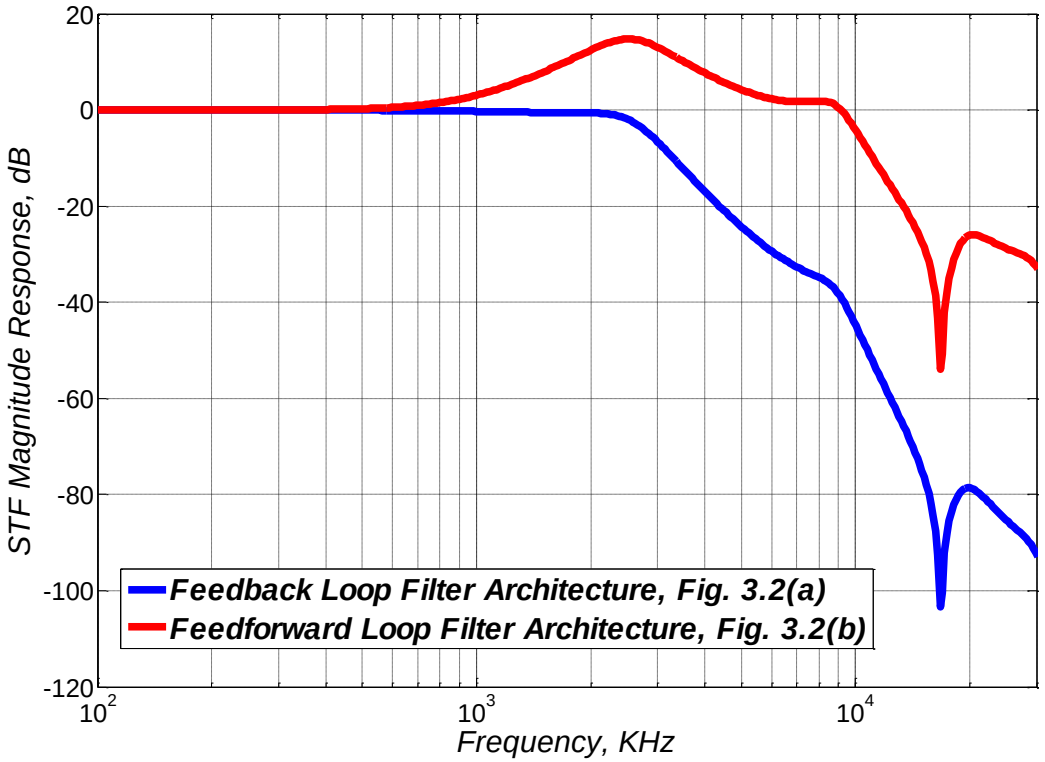


Fig. 3.7. STFs for the CT ΔΣ modulators in Fig. 3.2.

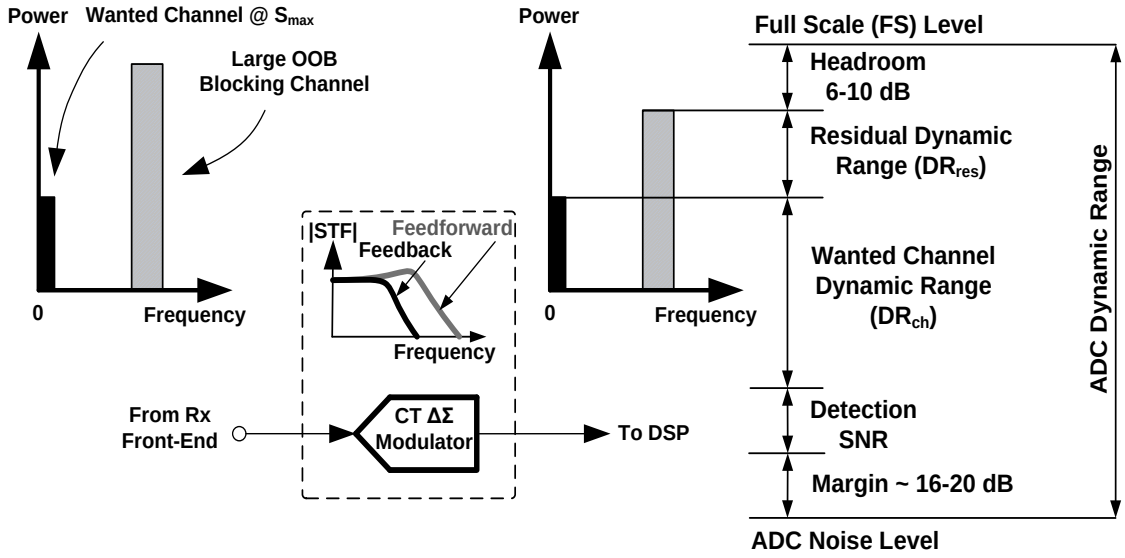


Fig. 3.8. ADC dynamic-range budgeting in presence of blockers.

4. ON THE SENSITIVITY OF SINGLE-BIT CONTINUOUS-TIME ΔΣ ANALOG-TO-DIGITAL CONVERTERS TO OUT-OF-BAND BLOCKERS[*]

4.1 Introduction

Although multi-bit ΔΣ modulators relax the noise shaping requirement on the loop filter and show better robustness to clock-jitter in the feedback DAC sampling clock [38], when compared to single-bit implementations, they suffer from limited linearity in the feedback multi-bit DAC due to inherent mismatch between DAC unit cells. Such DAC nonlinearity can compromise the performance of the ADC by folding high-pass-filtered (shaped) quantization noise into the band of interest, unless some kind of digital dynamic element matching (DEM) or shuffling blocks are added before the DAC, which comes at the expense of introducing a slight increase in the ADC noise floor as well as increasing the power budget and the loop excess delay. On the other hand, single-bit ΔΣ modulators do not suffer from DAC nonlinearity because single-bit DACs are inherently linear [2], [6], [9], [5]. This section investigates the sensitivity of single-bit CT ΔΣ ADCs to OOB blockers received in companion with desired signals. In essence, the residual interferer signal appearing at the output of the CT loop filter can flip the single-bit quantizer decision near the zero crossings of the loop filter output signal. An intuitive analysis of this effect on the performance of single-bit ΔΣ modulators in presence of OOB interferes is provided. System level simulations for a

[*] Reprinted with permission from "Sensitivity of single-bit continuous-time ΔΣ analogue-to-digital converters to out-of-band blockers," by Ramy Saad and Sebastian Hoyos, June 2010. *IET Electronics Letters*, vol. 46, no. 12, pp. 826-828.

single-bit fifth-order CT ΔΣ modulator at OSR of 40 have been carried out. A reduction in the achievable signal-to-noise-plus-distortion ratio (SNDR), that can be as large as 10 dB when applying a 0 dBFS OOB blocker tone along with a weak -75 dBFS desired tone, has been observed. The simulations results show good agreement with the adopted theoretical discussion.

4.2 Intuitive Discussion

The fifth-order single-bit CT cascade-of-resonators-feedback (CRFB) ΔΣ modulator in Fig. 4.1 will be used in the forecoming discussion. Figure 4.2 depicts the magnitude responses for the STF and the noise transfer functions (NTFs), NTF1[5] and NTF2[6], for the ΔΣ modulator in Fig. 4.1, designed for an OSR of 40. As shown in Fig. 2, the inherent LPF characteristic of the STF exhibits a flat response over the band of interest and drops by a slope of 100dB/decade after the corner frequency. On applying an input desired (in-band) signal $X_{signal}(s)$ and an OOB blocker signal $X_{OOB}(s)$ to the ΔΣ modulator, the quantizer input-referred sampled (DT) signal can be expressed as follows:

$$V_{Qin}(z) = \Big(X_{signal}(z) + X_{OOB}(z)\Big) STF(z) + Q(z)\, NTF2(z) \tag{4.1}$$

where $Q(z)$ is the quantization noise injected into the loop at the quantizer.

[5] NTF1 is the main noise-shaping transfer function of the modulator over the signal path from the quatizer to the modulator output.

[6] NTF2 is the noise transfer function from the quantizer output to the quantizer input through the loop. NTF2(z) = NTF1(z) - 1

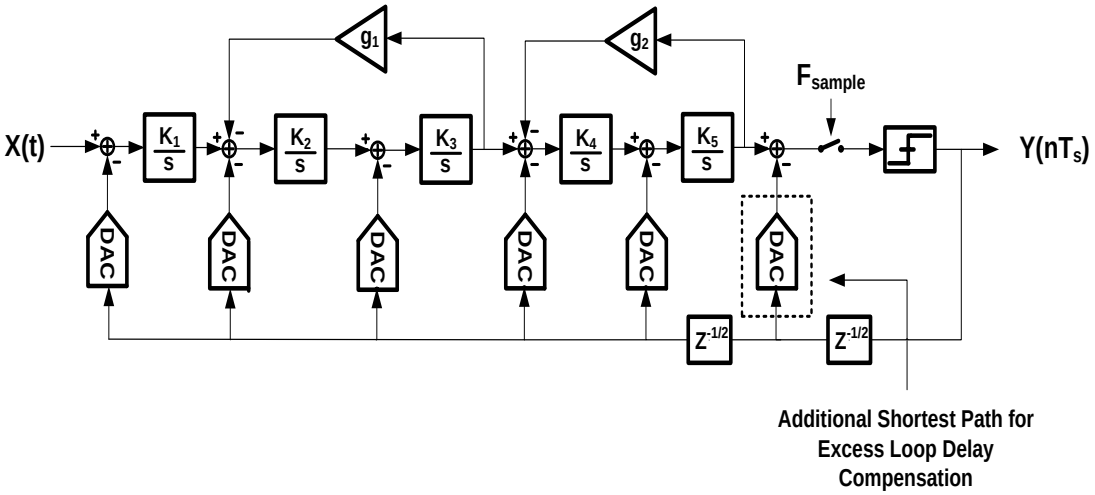


Fig. 4.1. Fifth-order continuous-time ΔΣ modulator in CRFB structure.

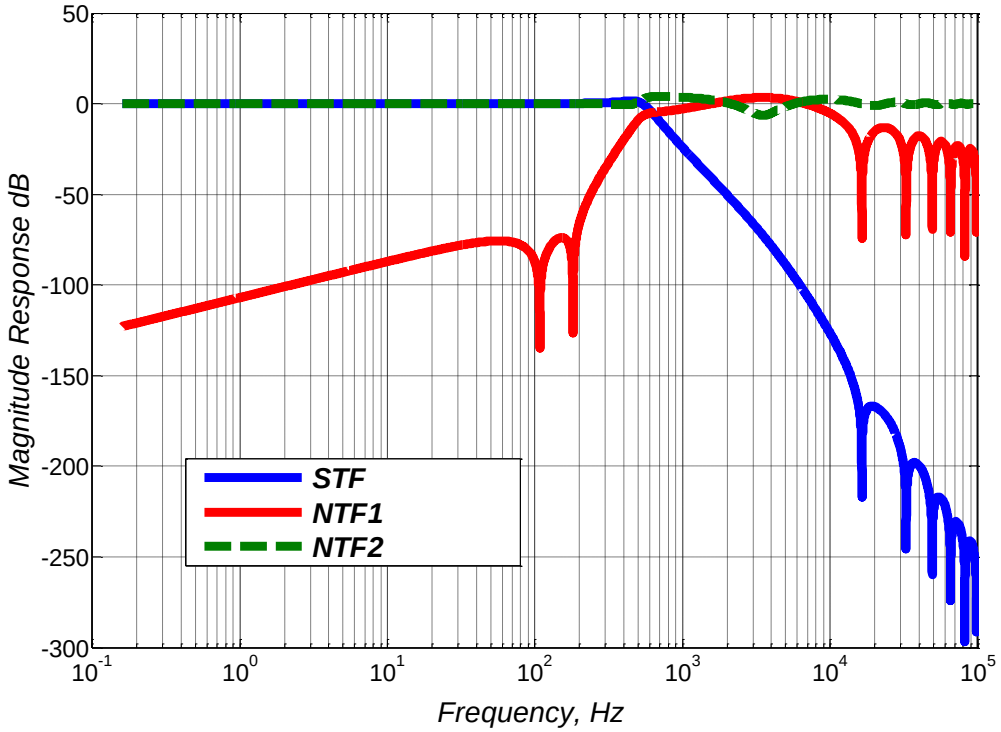


Fig. 4.2. Magnitude responses for signal and noise transfer functions at quantizer input and output terminals for the ΔΣ modulator in Fig. 4.1.

Although OOB blockers are attenuated by the STF, there are still remaining residual blocker components, superimposing on the quantizer input signal. Since this attenuated residual signal is usually small (for typical OOB signal power dictated by communication standards that can be tolerated at the receiver input), its effect is effective only near the zero-crossings of the main waveform composed of the desired signal and unshaped quantization noise given by

$$V_{Qin}(z) = X_{signal}(z)\, STF(z) + Q(z)\, NTF2(z). \quad (4.2)$$

In other words, the small residual blocker component at the loop filter output can flip the comparator decision in the proximity of the zero-crossing of the main blocker-free waveform in (4.2) because the comparator threshold in case of single-bit quantizers is nominally equal to zero. It is worth noting that the blocker $X_{OOB}(s)$ is located at a carrier-frequency and carries information different from those of the baseband desired in-band signal component $X_{signal}(s)$ and the unshaped noise component $Q(z)\, NTF2(z)$ is almost random. Thus, the residual blocker signal is uncorrelated with the quantizer input blocker-free signal in (4.2). As a result, the blocker-induced comparator decision error near the signal zero-crossings is neither correlated with itself nor with the stimulating residual blocker signal, as if these errors were generated by a random mechanism. This is equivalent to the effect of quantizer clock-jitter. Quantizer sampling jitter results from the random variations in the sampling clock-edge and can yield uncertainty in the comparator's decisions in the proximity of zero-crossings of the input waveform. For typical clock-jitter standard deviation values, jitter-induced error is usually shaped by $NTF1$ at the modulator output and no noticeable degradation in the

ADC arises. However, if the sampling jitter error power is high, the random phase modulation at the sampling edges, and the resulting increased uncertainty in the quantizer decision, can cause that some part of the shaped quantization noise outside the signal band falls into the signal band [10], degrading the achievable SNDR. Similar effect can be observed in the OOB blocker case. Particularly, as the residual blocker signal after the CT loop filter increases, due to increase in the amplitude of the input blocker signal applied to the ΔΣ modulator or inadequate attenuation by the STF, the induced uncertainty in the comparator decision will increase accordingly and hence folding more quantization noise over the band of interest at the quantizer[7]. The analysis and discussion leveraged in this section will be verified and demonstrated by system-level simulations given in the next section.

4.3 Simulation Results

System-level simulations using MATLAB/Simulink have been carried out to examine the effect of OOB on the performance of CT single-bit ΔΣ modulators. The fifth-order CT ΔΣ modulator structure in Fig. 4.1 has been adopted in the system-level simulations. The sampling frequency f_S is set to 16 MHz and OSR is 40. For simulation purposes, a weak in-band input sinusoid of amplitude -75 dBFS at 191KHz and a stronger OOB blocker at 5.7 MHz, which is one decade far from the STF 3-dB corner frequency, are applied to the modulator. The amplitude of the OOB blocker signal has been swept so that to examine the sensitivity of the achievable SNDR at a given desired

[7] **The quantization noise at the loop quantizer is measured as the difference between the quantizer input and output signals**

signal amplitude to the OOB blocker level. Figure 4.3 depicts the variation of the SNDR and the quantization noise added at the loop quantizer (over the band of interest) with the input blocker level so that to show the modulator response for different blocker values and illustrate the SNDR degradation due to the increase of the in-band quantization noise with the increase of the OOB blocker power.

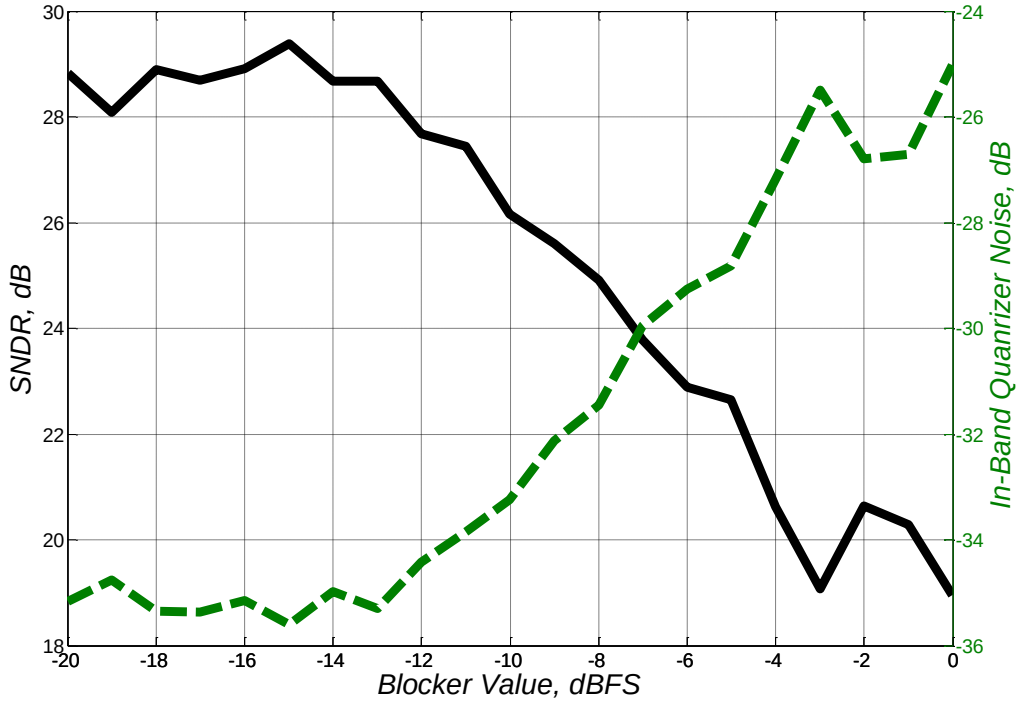


Fig. 4.3. Variation of the SNDR and the in-band quantizer noise power with the input blocker.

4.4 Conclusion

The sensitivity of single-bit CT ΔΣ modulators to OOB has been studied and shown to exhibit a quantizer sampling jitter-like effect especially in case of weak in-band signals. The adopted argument has been demonstrated through system-level simulations by examining the performance of a fifth-order single-bit ΔΣ modulator in a CRFB structure in presence of OOB blockers. A reduction in the achievable SNDR, that can be as large as 10 dB when applying a 0 dBFS OOB blocker tone along with a weak desired tone, has been observed. The premise adopted in the argument and verified by the simulation results suggests that the performance of single-bit CT ΔΣ modulator is sensitive to OOB and shows noticeable degradation in presence of sufficently high OOB signals.

5. EFFECTS OF OUT-OF-BAND BLOCKERS ON PULSE-WIDTH JITTER INDUCED ERRORS IN CONTINUOUS-TIME ΔΣ MODULATORS*

5.1 Introduction

This section investigates the sensitivity of CT ΔΣ ADCs to feedback PWJ in presence of blockers received at the ADC input. The analyses cover several types of DAC waveforms as well as multi-bit and single-bit DACs. Also, a comparison between ΔΣ modulators with feedforward and feedback loop filter structures in terms of robustness to DAC PWJ, in presence of blockers, is performed. Discussions and conclusions developed in the section are verified by CT simulations in Matlab/Simulink and simulations results show good agreement with the theoretical expectations. The section is organized as follows. In Section 5.2, the DAC PWJ analysis given in section 2 is extended such that the sensitivity of the integrated in-band noise (IBN) generated by PWJ in feedback DACs to blocker components at the modulator output is studied in details for different DAC types. In Section 5.3, the developed expressions and results are used to compare between different classes of CT ΔΣ architectures, including single-bit and multi-bit modulators with feedforward and feedback loop filters, in terms of robustness to DAC PWJ in presence of large out-of-band (OOB) blockers. Finally, conclusions are drawn in Section 5.4.

* Part of this chapter is reprinted with permission from "Sensitivity analysis of pulse-width jitter induced noise in continuous-time delta-sigma modulators to out-of-band blockers in wireless receivers," by Ramy Saad and Sebastian Hoyos, May 2011. *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1636-1639.

5.2 Pulse-Width Jitter in Presence of OOB Blockers

In this section, the jitter sensitivity analysis for commonly used DAC waveforms

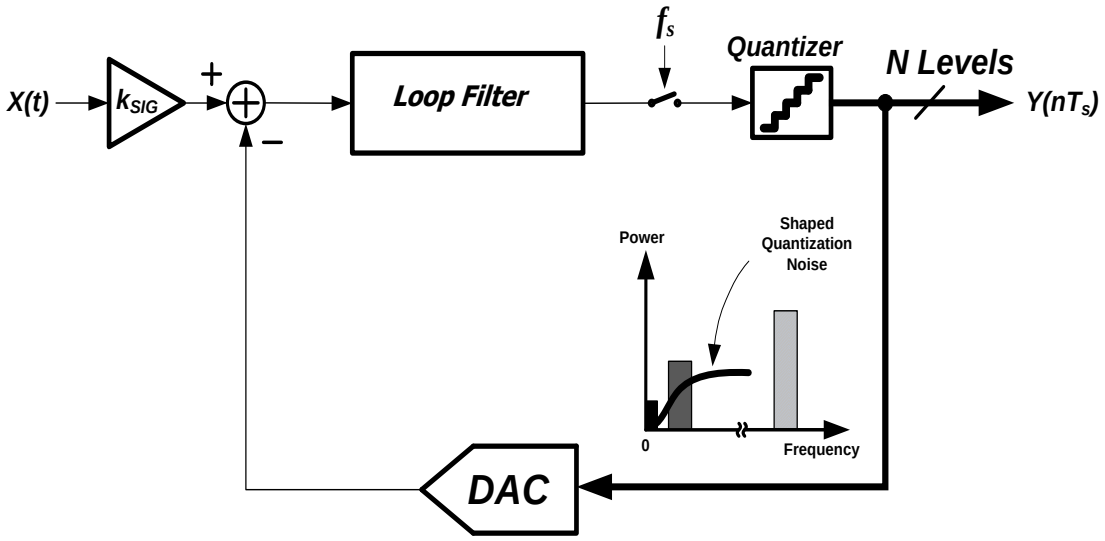


Fig. 5.1. Effect of blocker components in the feedback on PWJ errors.

in CT ΔΣ modulators will be extended so that to include the effects of OOB blockers appearing at the ADC input. In presence of a blocker signal $x_{BLK}(t)$ at the ADC input, the modulator output at the n^{th} clock cycle $y(n)$ is given by

$$y(n) = \left[\left(u(t) + x_{BLK}(t)\right) * stf(t)\right]\Big|_{t=nT_s} + q(n) * ntf(n) \tag{5.1}$$

To simplify the analysis, a single blocker tone, $x_{BLK}(t) = V_{BLK} \,.\, cos(\omega_{BLK} t)$, is assumed at the input of the ΔΣ modulator. The forecoming analysis can be easily extended to include multi-tone or modulated blocker signals. Now, the DT sampled blocker component at the quantizer input is given by

$$x_{BLK}(n) = V_{BLK} \cdot G_{\omega_{BLK}} \cdot cos\left(\omega_{BLK} nT_s + \varphi_{\omega_{BLK}}\right), \tag{5.2}$$

where $G_{\omega_{BLK}} = |STF(j\omega_{BLK})|$ and $\varphi_{\omega_{BLK}} = \angle\, STF(j\omega_{BLK})$ are the gain and excess

phase of the filter response $STF(j\omega)$ at the blocker frequency ω_{BLK}, respectively. For the RZ DAC waveform, the IBJN due to the blocker component can be obtained from (2.17) by replacing the signal power ${V_{sig}}^2/2$ with the power of blocker component in the feedback signal, determined by the product $V_{BLK}^2 \cdot G_{\omega_{BLK}}^2/2$ (Fig. 5.1).

$$IBJN|_{RZ,due\ to\ Blocker} = \frac{{V_{BLK}}^2 \cdot G_{\omega_{BLK}}^2}{OSR}\left(\frac{\sigma_t}{T_C}\right)^2. \tag{5.3}$$

Similarly, (2.28) is modified to yield the blocker-related contribution to the IBJN in an SCR DAC as follows

$$IBJN|_{SCR,due\ to\ Blocker} = \frac{1}{OSR}\cdot\left[\frac{e^{\frac{-(\beta-\alpha)T_s}{\tau}}}{\tau\left(1-e^{\frac{-(\beta-\alpha)T_s}{\tau}}\right)}\right]^2 \cdot \sigma_j^2 \cdot \frac{{V_{BLK}}^2 \cdot G_{\omega_{BLK}}^2}{2}. \tag{5.4}$$

However, for NRZ waveforms, it is required to extract the blocker contribution in $y(n)-y(n-1)$ in equation (2.19) so that to obtain the blocker induced IBJN [39], [40]. The difference between two consecutive blocker samples $dx_{BLK}(n)$ is expressed as

$$\begin{aligned} dx_{BLK}(n) &= x_{BLK}(n) - x_{BLK}(n-1) \\ &= 2\cdot V_{BLK}\cdot G_{\omega_{BLK}}\cdot sin\left(\omega_{BLK}\frac{(2n-1)T_s}{2}+\varphi_{\omega_{BLK}}\right)\cdot sin\left(\omega_{BLK}\frac{T_s}{2}\right). \end{aligned} \tag{5.5}$$

Note that in case of a blocker signal, the approximation $sin(x)\approx x$ cannot be applied here to the last sinusoidal term in (5.5) because the blockers are out of the signal band and hence can be at high frequencies that are not much less than the sampling frequency. Hence, the power of the blocker-related component of $dy(n)$ is given by

$$\sigma_{dx_{BLK}}^2 = 2\cdot V_{BLK}^2\cdot G_{\omega_{BLK}}^2\cdot sin^2\left(\omega_{BLK}\frac{T_s}{2}\right). \tag{5.6}$$

Substituting this expression for σ_{dy}^2 in (12), yields the IBJN due to the blocker component

$$IBJN|_{NRZ,due\ to\ blocker} = 4 \cdot OSR \cdot BW^2 \cdot \sigma_j^2 \cdot \sigma_{dx_{BLK}}^2$$

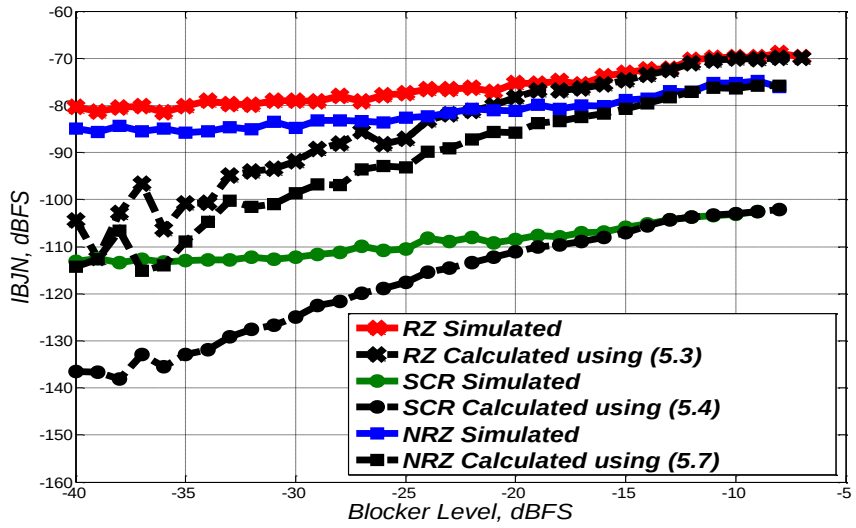
$$= 8 \cdot OSR \cdot BW^2 \cdot \sigma_j^2 \cdot V_{BLK}^2 \cdot G_{\omega_{BLK}}^2 \cdot sin^2\left(\omega_{BLK}\frac{T_s}{2}\right). \qquad (5.7)$$

For all aforementioned DAC waveforms, the blocker induced IBJN is directly proportional to the power of the blocker component in the feedback signal (Fig. 5.1), determined by $V_{BLK}^2 \cdot G_{\omega_{BLK}}^2/2$. In SI RZ and SCR DACs, the dependence of the blocker induced IBJN on the blocker frequency is such that for a given blocker level at the modulator input, the amplitude of the blocker component in the feedback depends on the value of the STF magnitude response at the blocker frequency, $G_{\omega_{BLK}}$. However, for NRZ DACs, from (5.7), it can be seen that in addition to the frequency dependence of $G_{\omega_{BLK}}$, the periodic term $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ depends also on the frequency of the blocker tone. This periodic dependence is resulting from the fact that the jitter induced error in NRZ waveforms is proportional to the first-order difference of the feedback signal $dy(n)$. For sufficiently small blocker frequencies (e.g. adjacent-channel blockers), such that $\left(\omega_{BLK}\frac{T_s}{2}\right) \ll 1$, the squared sinusoidal term can be approximated as $\left(\omega_{BLK}\frac{T_s}{2}\right)^2$, which is a very small value (much less than unity) [40]. In this case, the contributions by other factors (OSR, BW, σ_j, V_{BLK}, and $G_{\omega_{BLK}}$) are attenuated and the resulting IBJN is very small. Since the sinusoidal function is periodic, this case extends to include frequency ranges in which the product $\omega_{BLK}\frac{T_s}{2}$ is very close to 2π and its multiples:

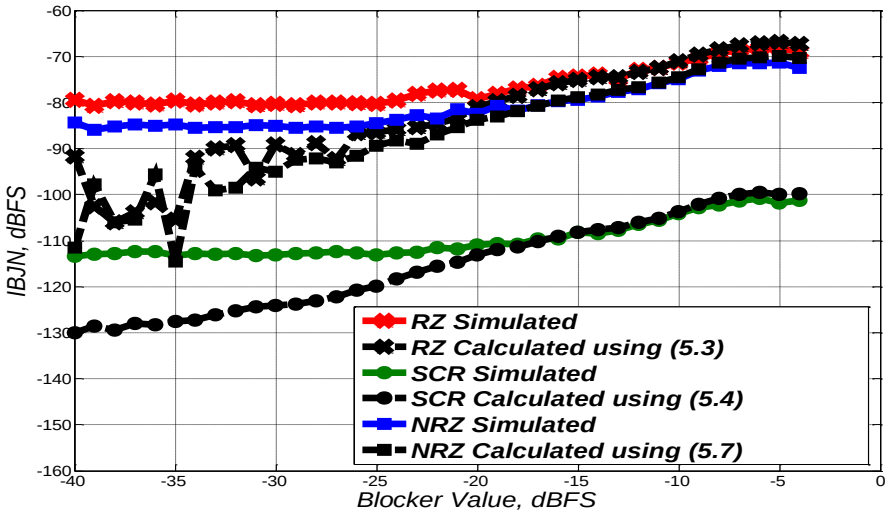
$$sin^2\left(\omega_{BLK}\frac{T_s}{2}-2k\pi\right)\approx\left(\omega_{BLK}\frac{T_s}{2}-2k\pi\right)^2,\qquad for\ 0<\left|\omega_{BLK}\frac{T_s}{2}-2k\pi\right|\ll 1\,, \tag{5.8}$$

where $k = 0, 1, 2, \dots, n$. Recall that the lack of filtering and the wideband receiver front-end allow a wide range of OOB blockers to appear at the ADC input. On the other hand, for blocker frequencies close to the Nyquist-rate bandwidth (πf_s) and its odd multiples, such that $\omega_{BLK} \sim (2k+1)\pi f_s$, the squared sinusoidal term is approximated by unity and thus the contributions by (OSR, BW, σ_j, V_{BLK}, and $G_{\omega_{BLK}}$) are not attenuated by the sin^2 term.

To illustrate the effect of blockers on the IBJN, the feedforward ΔΣ modulator in Fig. 3.2(b) is used as a test vehicle for system-level simulations with a sampling frequency $f_s = 16.8\,MHz$, OSR=42, and 6-levels quantization. As shown in Fig. 3.7, feedforward ΔΣ configurations have limited filtering for OOB blockers, and even have amplification over a certain range due to peaking in the magnitude response, in contrast to feedback structures. Thus, they offer a convenient environment to exemplify the sensitivity of the IBJN to OOB blockers. Comparison between ΔΣ modulators with feedback and feedforward loop filter architectures, in terms of their sensitivity to blocker induced PWJ, will be provided in the next section. The effect of PWJ in feedback DACs is modeled using (2.15), (2.19), and (2.26) for SI RZ, SI NRZ, and SCR DACs, respectively, with a RMS jitter standard-deviation of $0.1\,\%\,T_s$. CT simulations have been carried out using a weak in-band tone $V_{SIG} = -75\,dBFS$, $\omega_{SIG} = 2\pi \times 31KHz$, so that the effect of the OOB blocker tone dominates and can be observed.

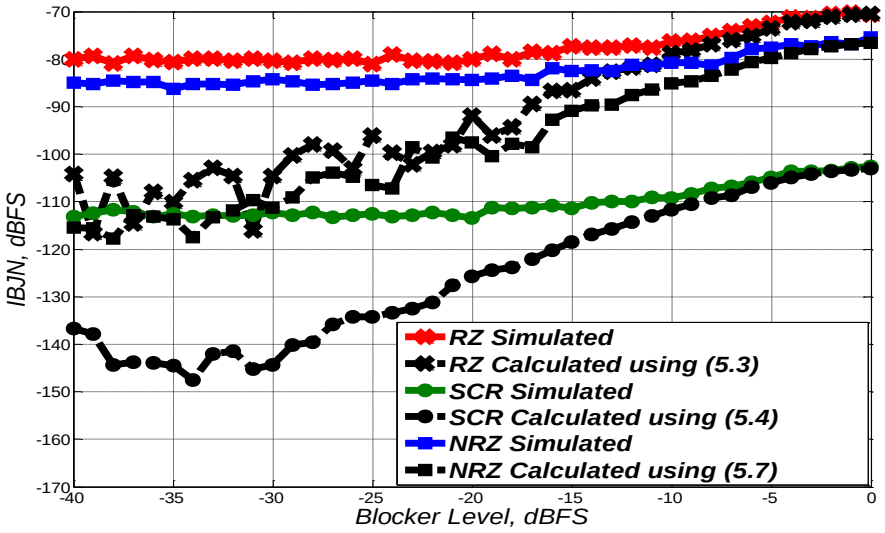


(a)



(b)

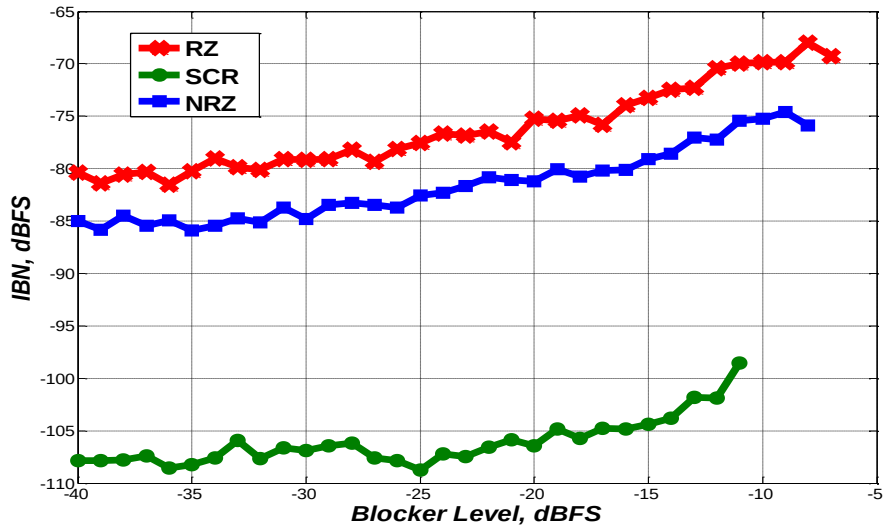
Fig. 5.2. Sensitivity of a feedforward 6-levels third-order CT ΔΣ modulator to OOB blocker levels at the modulator input, in terms of IBJN (a) $\omega_{BLK} = 2\pi \times 4.2MHz$. (b) $\omega_{BLK} = 2\pi \times 8.4MHz$. (c) $\omega_{BLK} = 2\pi \times 12.6MHz$. $V_{SIG} = -75\ dBFS$, $f_{SIG} = 31\ KHz$, $\sigma_j = 0.1\%\ T_S$.



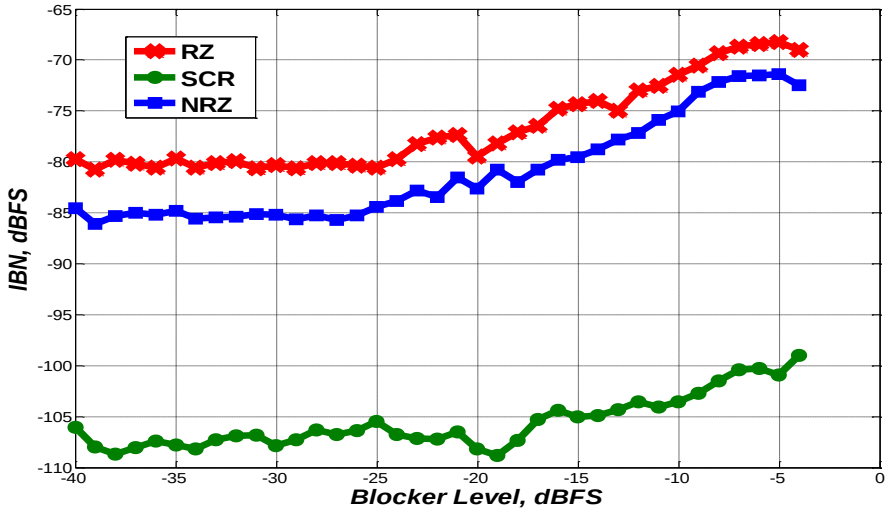
(c)

Fig. 5.2 Continued.

The plots in Fig. 5.2 and Fig. 5.3 show the increase in the IBJN with the blocker level and the resulting increase in the overall IBN for OOB blocker tones at different frequencies. The correlation between the simulations plots of Fig. 5.2 and Fig. 5.3 indicates that at certain range of OOB blocker levels, the blocker induced IBJN dominates the total IBN and hence effectively degrades the achievable SNDR (by up to 10 dB). The plots in Fig. 5.2 (and Fig. 5.3) are arranged such that the IBJN (and IBN) plots for a given blocker frequency are collected in one window so that to give a comparative view between the three DAC types (SI RZ, SI NRZ, and SCR). As expected, the SI RZ DAC has the worst performance towards PWJ (highest IBJN) while the SCR DAC is the most robust (lowest IBJN). It is observable that the three DAC types have the almost same sensitivity to blocker induced PWJ, since for a given blocker

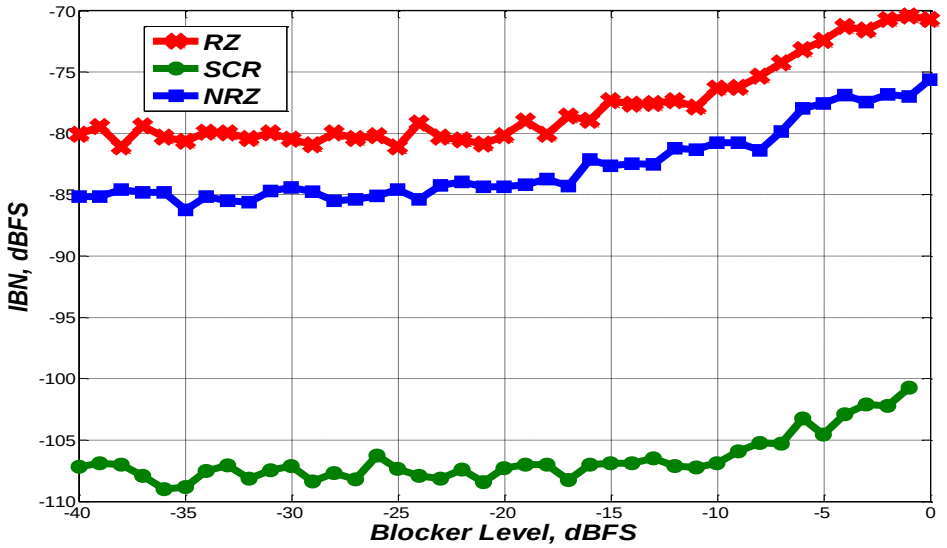


(a)



(b)

Fig. 5.3. Sensitivity of a feedforward 6-levels third-order CT ΔΣ modulator to OOB blocker levels at the modulator input, in terms of total IBN (a) $\omega_{BLK} = 2\pi \times 4.2MHz$. (b) $\omega_{BLK} = 2\pi \times 8.4MHz$. (c) $\omega_{BLK} = 2\pi \times 12.6MHz$. $V_{SIG} = -75\,dBFS$, $f_{SIG} = 31\,KHz$, $\sigma_j = 0.1\%\,T_S$.



(c)

Fig. 5.3 Continued.

frequency, the IBJN plots are roughly increasing at the same rate.

The following detailed discussion of the simulation results will help gaining more insight and link them with the preceding analysis. The special blocker frequencies: 4.8 MHz, 8.4 MHz, and 12.6 MHz, have been picked up so that the values of the frequency dependent factor $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ in (41) are 0.5, 1, and 0.5, respectively. The key point is to be able to examine the periodicity in the frequency response provided by the sin^2 term (see Fig. 5.4). It is worth noting that the plots in Fig. 5.2, Fig. 5.3, and Fig. 5.4 are depicted only up to the critical blocker levels, after which the modulator becomes unstable due to quantizer overloading, and hence no meaningful information

can be obtained about the IBJN or IBN. From the plots in Fig. 5.3, at critical blocker levels, the increase in the total IBN can be as large as 10 dB for the three DAC types. The critical blocker levels are proportional to the blocker frequencies because higher blocker frequencies experience less gain in the loop filter before they reach the quantizer (Fig. 3.7). At smaller blocker frequencies, the IBJN (and hence the IBN) starts to increase at lower blocker levels, indicating that the sensitivity of the PWJ to the blocker level is higher due to the frequency response of $G^2_{\omega_{BLK}}$.

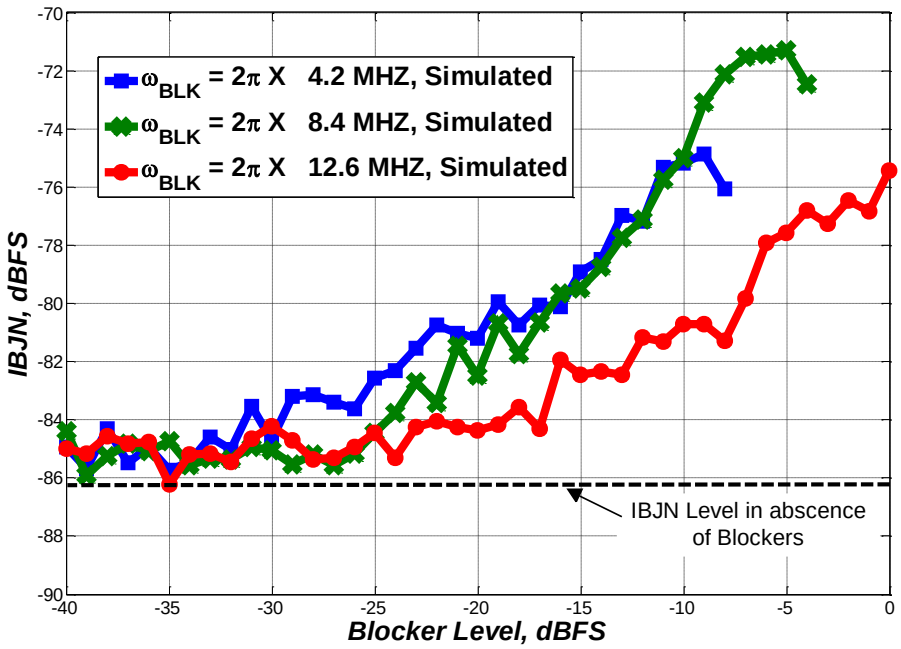


Fig. 5.4. Sensitivity of a feedforward 6-levels third-order CT ΔΣ modulator with NRZ DAC waveform to OOB blocker levels at the modulator input, in terms of total IBJN. $\omega_{BLK} = 2\pi \times 12.6MHz, V_{SIG} = -75\ dBFS, f_{SIG} = 31\ KHz, \sigma_j = 0.1\%\ T_S$.

The simulations plots in Fig. 5.2 depict the total IBJN resulting from random phase-modulation of signal, quantization noise, and OOB blocker components in the feedback signal, whereas the plots obtained by calculation from (5.3), (5.4), and (5.7) give only the IBJN due to blockers. Thus, the simulation and calculation plots coincide only at OOB blocker levels for which the IBJN induced by OOB blocker increase and dominate the total IBJN. Coincidence between simulated and calculated IBJN values at sufficiently large OOB blocker levels implies a very good matching between the developed analysis and the simulations results.

Now, it is time to look at the effect of the periodic $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ term in (5.7). The IBJN plots for NRZ DAC waveform given in Fig. 5.2 are rearranged together in Fig. 5.4. For a given in-band signal, at critical blocker levels, the blocker power appearing in the feedback path (determined by $V_{BLK}^2 \cdot G_{\omega_{BLK}}^2/2$) is almost the same because the quantizer overloading level (which determines the critical blocker level) is constant. Thus, for NRZ DAC waveform, the value of the maximum blocker induced IBJN (IBJN @ critical blocker level) vary according to the $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ term in (2.20). Owing to the periodicity of the $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ term, the maximum IBJN values for the two blocker tones at 4.8 MHz and 12.6 MHz are almost equal, as shown in Fig. 5.4. The maximum IBJN value for the 8.4 MHz tone is roughly 3 dB higher because the $sin^2\left(\omega_{BLK}\frac{T_s}{2}\right)$ term in this case is twice its value for the other blocker tones.

5.3 Comparison between Different Types of Modulators

5.3.1 Single-Bit vs. Multi-Bit Quantizers

The previous analysis applies well to ΔΣ modulators with multi-bit quantizers. Recall that the developed analysis and expressions match very well with the simulations results given in the previous section using a multi-bit ΔΣ modulator. However, for single-bit modulators, the case is different [41]. Before going into the comparison between the sensitivities of IBJN to blockers in modulators with single- and multi-bit quantizers, it is important to highlight a very important difference between the two architectures in terms of how the input data modulate their output waveforms. Particularly, in single-bit modulators, the signal at the modulator input is just modulating the density of the output bit stream (recall that a single-bit quantizer is just sensitive to the polarity of its input), while for multi-bit ΔΣ modulators, the input signal modulates the density of the output digital codes as well as their values (amplitudes) [36].

Thus, in ΔΣ modulators with multi-bit quantizers, the effect of an OOB blocker component at the output of the loop filter is reflected in both the frequency and swing of the output waveform. As a result, the amplitude of the blocker signal will appear in the feedback depending on how precisely the quantizer is digitizing the signal appearing at its input. On the other hand, for single-bit modulators, blocker components remaining at the loop filter output modulates only the switching rate of the feedback pulses. That is, for an output stream of single-bits, the amplitude of the blocker component at the

modulator output will show up only after the output bit stream is averaged and by that time it will be filtered and hence attenuated. Recall that the modulator output is fed back directly through the DAC every clock-cycle without being averaged.

The foregoing discussion implies that for single-bit modulators, the power of the blocker components at the loop filter output will not show up instantaneously in the feedback pulses, however, averaging over certain period of time ie needed to extract the information (power) about the blocker component. This observation combined with the fact that the PWJ expressions in (2.15), (2.19), and (2.26) are proportional to the instantaneous values of the feedback signal, $y(n)$, yield the result that single-bit modulators are robust to PWJ errors due to blockers. In contrast, multi-bit modulators are sensitive to PWJ errors caused by OOB blockers because the instantaneous values of $y(n)$ vary according to the blocker component showing up at the quantizer input. This result is surprising because single-bit modulators are known to be more sensitive to PWJ compared to multi-bit counterparts.

To examine the sensitivity of single-bit modulators to blocker induced IBJN by simulations, a single-bit ΔΣ modulator following the feedforward structure of Fig. 3.2(b) is designed. The single-bit ΔΣ modulator design parameters ($f_s = 33.6\,MHz$ and OSR=84) have been picked up so that to achieve equivalent performance (in terms of dynamic-range and SNDR) to the multi-bit counterpart used in the previous section. Since single-bit DACs are more sensitive to PWJ than multi-bit ones [16], a RMS jitter with standard-deviation of $0.06\,\%\,T_s = 18\,psec$ (compared to $0.1\,\%\,T_s = 59.5\,psec$ in the multi-bit case) is added to the DAC sampling clock in the single-bit modulator so

that to maintain the same IBJN as in the previously simulated multi-bit modulator. This equivalence is required for a fair comparison between the sensitivities of multi-bit and single-bit modulators to blocker induced PWJ errors, at a given performance.

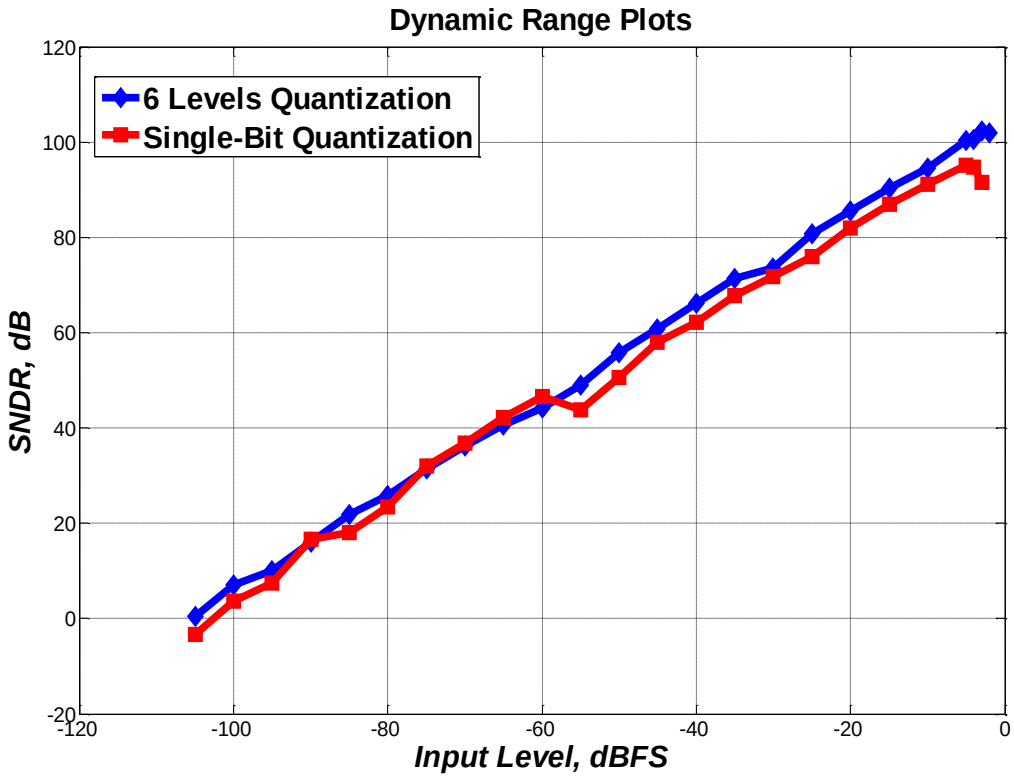


Fig. 5.5. Dynamic-range plots for two equivalent feedforward third-order CT ΔΣ modulators with 6-levels and single-bit quantization.

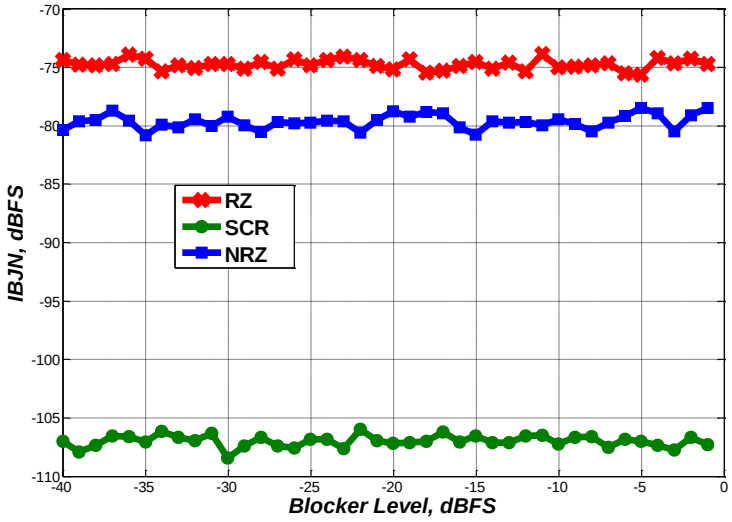
The dynamic-range plots in Fig. 5.5 show that the two modulators are achieving almost equal dynamic-ranges and maximum SNDR, and the most important is that the SNDR (and hence the IBN) at the input level used for testing ($V_{SIG} = -75\ dBFS$) is the same for both modulators so that to ensure that they have the same IBN.

For different DAC types, the plots in Fig. 5.6 show that the IBJN and IBN of the single-bit modulator are completely insensitive to the blocker levels. Again, these plots are depicted only up to the critical blocker levels, after which the modulator becomes unstable due to quantizer overloading, and hence no meaningful information can be obtained about the IBJN or IBN. Since a single-bit quantizer overloads at larger signal levels at its input compared to multi-bit quantziers, critical blocker levels in the single-bit modulator are higher than those in the multi-bit counterpart.

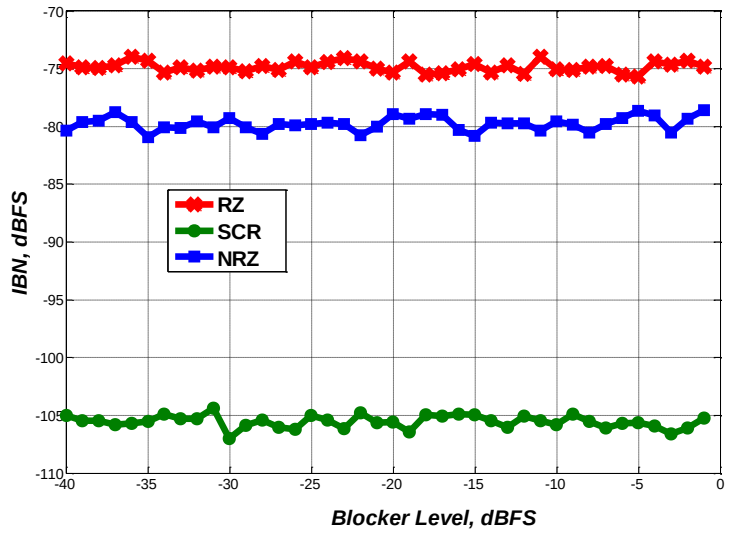
The discussion and simulations results given in this section provide evidently an interesting conclusion that the IBJN in single-bit modulators is completely insensitive to blocker components remaining at the loop filter output.

5.3.2 Feedforward vs. Feedback Loop Filter Architectures

Based on the conclusion developed in the previous section, in order to examine the differences between feedback and feedforwad modulator structures in terms of their IBJN sensitivities to blockers, it is convenient to use multi-bit quantizers. Owing to their relaxed requirements on the amplifier signal swing and distortion, feedforward $\Delta\Sigma$ modulators have been an attractive choice for several multi-standard and wideband low power ADCs reported in the literature [2]-[5].



(a)

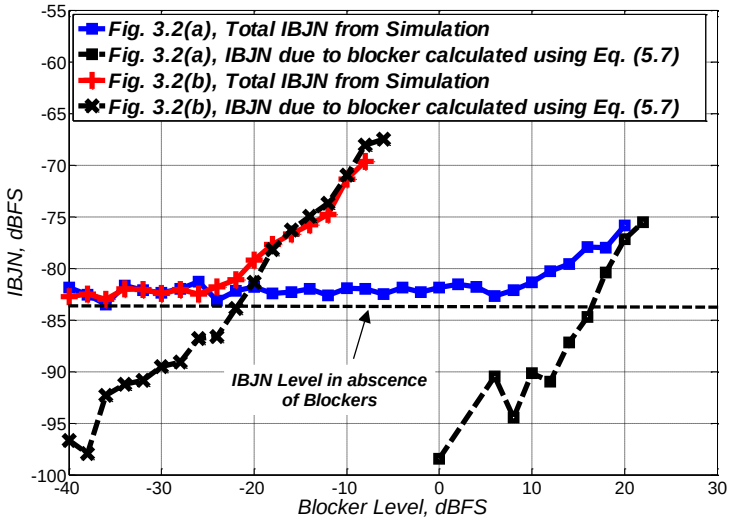


(b)

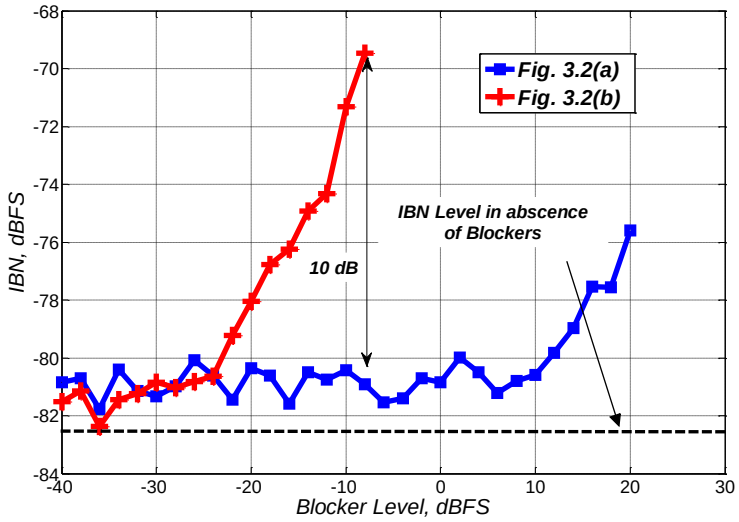
Fig. 5.6. Sensitivity of a feedforward single-bit third-order CT ΔΣ modulator to OOB blocker levels at the modulator input, in terms (a) IBJN. (b) Overall IBN. $\omega_{BLK} = 2\pi \times 8.4MHz. V_{SIG} = -75\ dBFS, f_{SIG} = 31\ KHz,\ \sigma_j = 0.06\% T_S.$

In presence of blockers, it can be seen from (5.3), (5.4), and 5.7) that the term $G_{\omega_{BLK}}^2$ implies an important difference between the responses of ΔΣ modulators using feedforward and feedback loop filters to DAC PWJ. Figure 3.7 shows the STF magnitude responses for the third-order CT ΔΣ modulators in Fig. 3.2. Due to feedforward paths in the loop filter, feedforward ΔΣ configurations have limited filtering to interferers, and even have amplification over a certain range in the STF magnitude response (caused by peaking). On the other hand, feedback structures show a stronger low-pass filtering STF and hence higher attenuation for OOB blockers. Therefore, for a given blocker amplitude and frequency at the ADC input, the value of $G_{\omega_{BLK}}^2$ for a feedforward loop filter will be higher and hence the expressions in (5.3), (5.4), and (5.7) will yield higher IBJN values. Thus, for sufficiently large OOB blockers, feedback ΔΣ modulator structures are expected to show more robustness to PWJ than feedforward structures and the difference in the performance is determined by the difference in the magnitude responses of their STFs at the blocker frequency.

The CT ΔΣ modulators in Fig. 3.2 are used for system-level simulations with $f_s = 16.8\,MHz$, OSR=42, and 6-levels quantization. NRZ DACs are used and the effect of PWJ is modeled by (2.19) with a RMS jitter standard-deviation of $0.1\,\%\,T_s = 59.5\,psec$ in the DAC clock. Again, the in-band signal is a weak tone, $V_{SIG} = -75\,dBFS$, $\omega_{SIG} = 2\pi \times 31KHz$, so that to observe the effect of the blocker signal. The OOB blocker frequency is $\omega_{BLK} = 2\pi \times 8.4\,MHz$. As can be seen from Fig. 5.7, the feedback modulator in Fig. 3.2(a) is showing more robustness to the IBJN generated by the OOB blocker tone than the feedforward architecture of Fig. 3.2(b).



(a)



(b)

Fig. 5.7. Sensitivity of a feedforward and feedback 6-levels third-order CT ΔΣ modulators with NRZ DACs to OOB blocker levels at the modulator input, in terms (a) IBJN. (b) Overall IBN. $\omega_{BLK} = 2\pi \times 8.4MHz, V_{SIG} = -75\ dBFS,$ $f_{SIG} = 31\ KHz,\ \sigma_j = 0.1\%\ T_S.$

For a given RMS jitter, the blocker induced IBJN and the resulting increase in the IBN for the feedforward case can be 10 dB higher than the noise levels in feedback modulator. Owing to the stronger filtering offered by the feedback modulator, it can tolerate higher blocker levels without being overloaded.

5.4 Conclusion

The sensitivity of ΔΣ modulators with CT loop filters to DAC PWJ in presence of blockers has been investigated in details. The developed analysis covered the commonly used DAC types including SI RZ, SI NRZ, and SCR with exponentially-decaying waveform. It has been shown that for all types of multi-bit DACs, the IBJN induced by a blocker signal increases proportionally with the power of the blocker component in the feedback path and also varies periodically with the blocker frequency through a squared sinusoidal factor for multi-bit NRZ DACs. In contrast, single-bit ΔΣ modulators are shown to be completely robust to blocker induced IBJN since the signal swing in their feedback waveforms is independent of the quantizer input signal and hence the blocker component power. In addition to difference in types of quantizers, comparison between different classes of ΔΣ modulators also covered different loop filter structures. According to results obtained by simulations, the IBJN due to blockers dominates the total IBN for feedforward multi-bit ΔΣ modulators and can increase the total IBN by 10 dB. However, for a given blocker power at the ADC input, multi-bit feedback ΔΣ modulators show more robustness to PWJ than their feedforward counterparts, owing to their stronger low-pass filtering characteristic.

6. HYBRID DAC WITH FEEDFORWARD SPECTRAL SHAPING TECHNIQUE FOR CLOCK-JITTER INDUCED ERRORS*

6.1 Introduction

A simple hybrid oversampled DAC based on feedforward spectral shaping technique for the PWJ induced errors is presented. The benifit of this hybrid DAC solution is illustrated in the context of feedback DACs used in CT ΔΣ modulators. Simulation results show that the jitter tolerance of the proposed DAC solution is equivalent to that of the commonly used jitter-tolerant exponentially-decaying waveform SCR DAC structure, but at much more relaxed SR requirement on the op-amp used in the DAC load circuit, which translates into significant power savings. A prototype chip for the proposed hybrid DAC is fabricated in a 90nm CMOS technology. The implemented hybrid jitter-tolerant DAC provides a measured attenuation for in-band jitter induced noise by 26.7dB, compared to conventional CS DAC. The DAC chip consumes only 719μwatts from 1.3V supply.

6.2 Switched-Capacitor-Resistor DAC

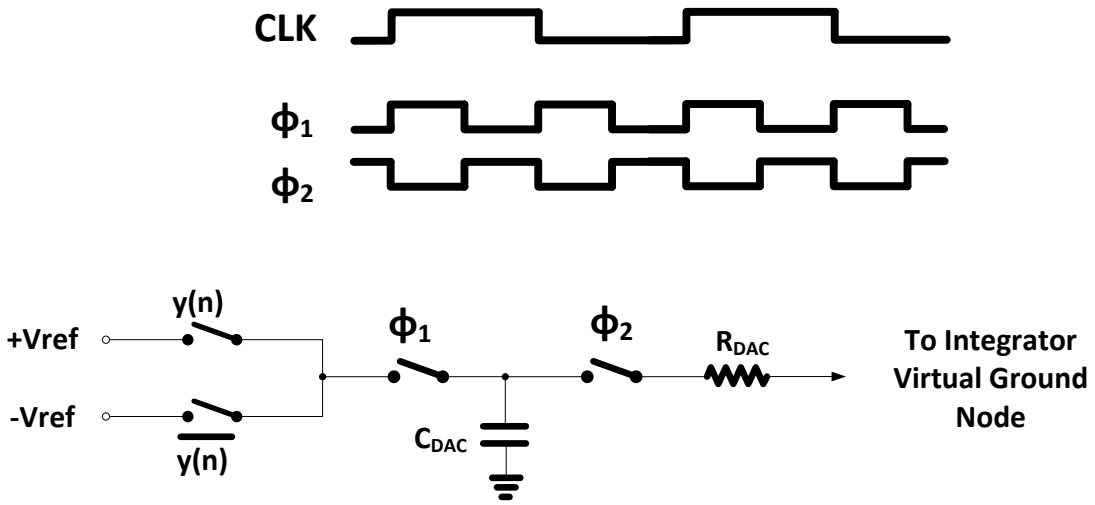
The large sensitivity to feedback pulse-width variations is due to the high amplitude of the traditionally used rectangular waveforms at the set and reset time instants, making the amount of charge fed back to the loop-filter strongly dependent on

* Part of this chapter is reprinted with permission from "Feedforward spectral shaping technique for clock-jitter induced errors in digital-to-analogue converters," by Ramy Saad and Sebastian Hoyos, February 2011. *IET Electronics Letters*, vol. 47, no. 3, pp. 171-172.

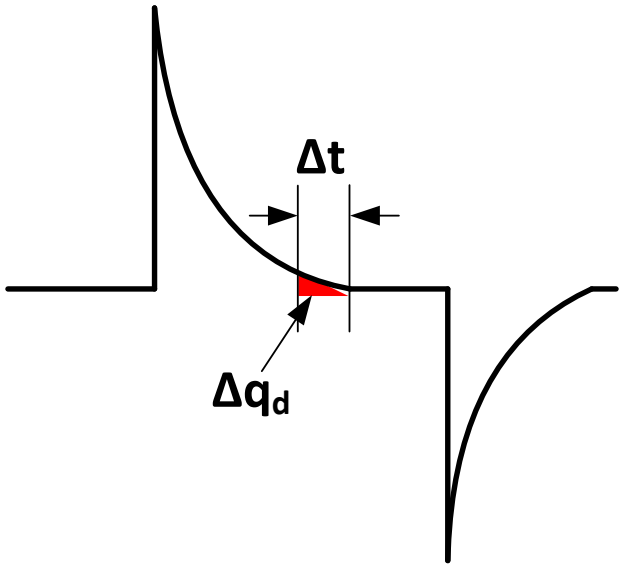
the pulse-width. As a consequence, there has been a considerable interest in the use of decaying feedback pulse shapes like, for example, sine-shaped feedback, exponentially-decaying feedback, and the triangular waveform feedback. Among these, the exponentially-decaying pulse shape is the one that has been most frequently implemented simply by using a switched-capacitor with a series resistor [16], [23], as shown in Fig. 6.1. Particularly, the feedback signal waveform is suppressed at the switching instant due to the decaying pulse form and hence the sensitivity of the amount of feedback charges provided by the DAC to timing jitter is very low.

However, this improvement in the robustness to clock-jitter comes at the expense of adding much higher requirements on the SR and GBW of the amplifiers used at the DAC load (e.g. in loop filters of CT ΔΣ modulators). A CT ΔΣ modulator with SCR feedback DAC needs approximately a factor of T_S/τ_{DAC} times higher SR in the corresponding integrator, where T_S is the sampling period and τ_{DAC} is the SCR DAC time-constant. This is mainly due to the increase of the DAC peak current caused by the abrupt transition of a large amount of charge at the beginning of the exponentially-decaying pulse, whose value is proportional to $1/\tau_{DAC}$. To achieve adequate tolerance to clock-jitter in wideband ΔΣ modulators, τ_{DAC} is typically in the range of $0.05\,T_S$ to $0.1\,T_S$ [16], resulting in an increased SR requirement on the integrators in the order of 10 times, compared to the case of NRZ DACs. This increase in the integrators SR requirement translates into higher power consumption. In [23], a modified feedback DAC technique using a switched-capacitor with a variable switched series resistor (SCSR) reduces the typically high SCR DAC output peak currents, providing some

reduction in the SR requirements of the integrators; however the SR requirement is still higher than the case of NRZ DAC.



(a)



(b)

Figure 6.1. SCR DAC. (a) Implementation. (b) Jitter-tolerant exponentially-decaying HRZ waveform.

Also, for an SCR DAC, the GBW requirement on the integrating amplifier increases by almost 2-5 times depending on the target ADC resolution [16]. Moreover, CT ΔΣ modulators using SCR DACs have poor inherent anti-aliasing compared to those using CS DACs [24] due to the loading of the SCR DAC on the integrating amplifier input nodes. In order to avoid the additional requirements on the GBW and maintain the inherent anti-aliasing, buffering is needed between the SCR DAC and the virtual ground nodes of the loop filter amplifier. However, buffering is not convenient in this case because the large signal swing of the feedback exponentially-decaying waveform makes it highly sensitive to the nonlinearities of the V-to-I conversion in a MOSFET transistor used as a buffer [42].

6.3 Proposed Hybrid CS-SCR DAC Solution

6.3.1 Basic System-Level Concept

The main goal is to provide tolerance to DAC PWJ equivalent to that offered by the SCR exponentially-decaying waveform DACs without adding extra requirements on the op-amp SR and GBW, as will be explained in the following discussion. Figure 6.2 shows a simplified block-diagram that describes the basic concept of the adopted hybrid CS-SCR DAC when used in CT ΔΣ modulators [25], [43]. The key point is to extract the PWJ induced error in the amount of charge supplied by the main CS DAC to loop filter in each clock-cycle, with the aid of a voltage sampling SC circuit that is not suffering PWJ, and inject this charge error with opposite polarity into the loop filter through an

SCR circuit in the next clock-cycle. Thus, the PWJ induced noise undergoes a first-order high-pass filtering ($1-Z^{-1}$), as illustrated by the diagram in Fig. 6.2.

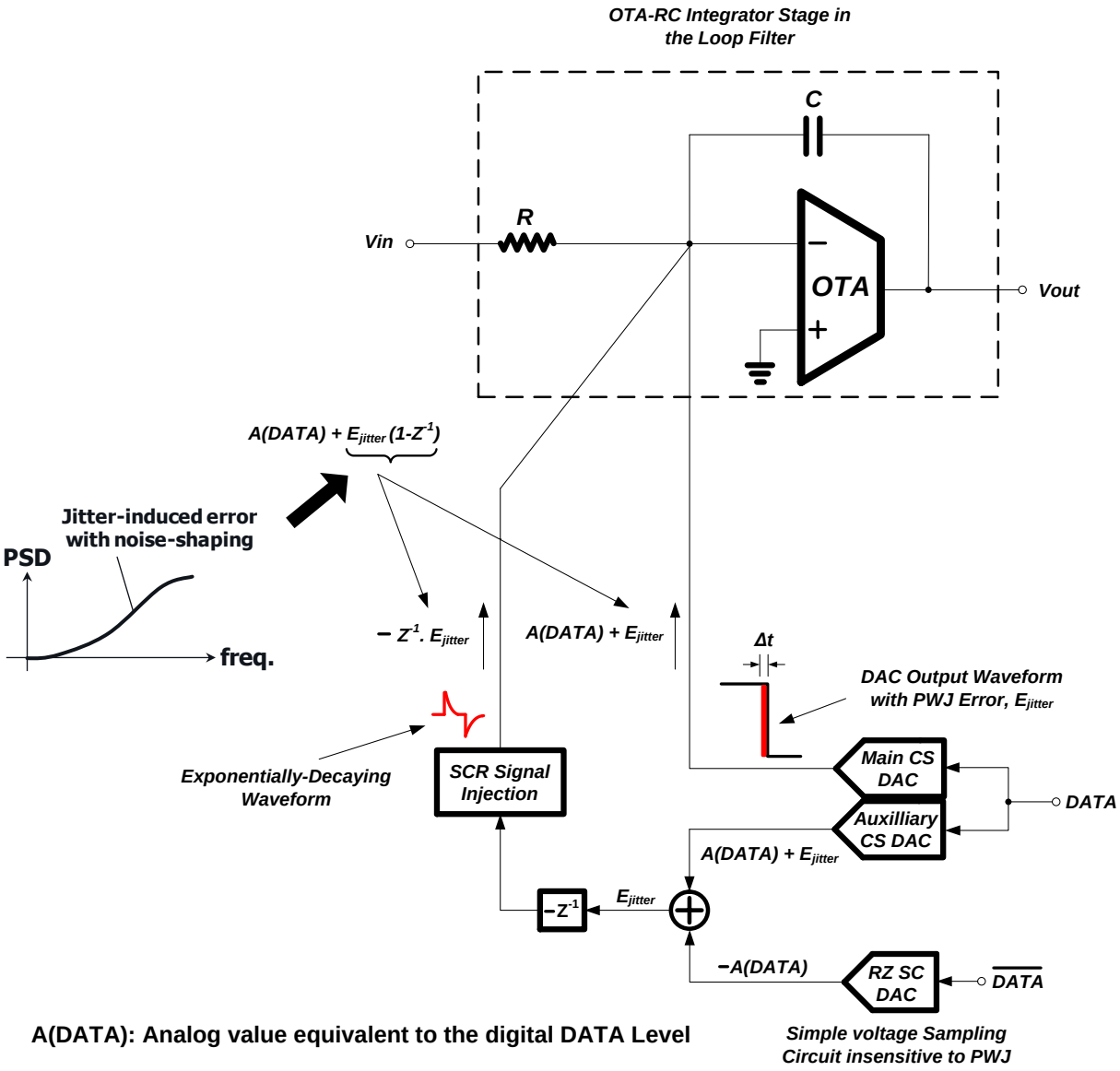


Fig. 6.2. Block-diagram for the proposed hybrid DAC solution based on spectral shaping of jitter induced errors.

The digital signal $\boldsymbol{DATA}$ is applied to two identical NRZ SI DACs and a RZ SC DAC. The RZ SC DAC is simply a voltage sampling circuit and hence it is not suffering from clock-jitter. The charge sampled by the SC DAC is a jitter-free reference that will be used later to extract the error in the integrated charge due to PWJ. The main CS DAC provides the main feedback path to the loop filter, whereas the error-free reference value sampled by the RZ SC DAC is subtracted from the output of the auxiliary CS DAC. The result of this subtraction is equal to the error in the integrated charge, $\boldsymbol{E_{jitter}}$, induced by PWJ. Then, this charge error is inverted and fed to the loop filter during the next clock cycle (i.e. delayed by one sample), thus achieving a first-order spectral shaping for the jitter induced error. Therefore, $\boldsymbol{E_{jitter}}$ is shaped and pushed to higher frequencies to be later removed by the decimation filter in the digital domain. High fidelity in this delayed jitter induced error signal is needed so that to achieve accurate shaping. Thus, the delayed error replica ($-\boldsymbol{E_{jitter}} \cdot \boldsymbol{Z^{-1}}$) is injected using an exponentially-decaying pulse to ensure adequate robustness of this particular signal to clock jitter, and hence achieve reliable shaping. The overhead in the signal swing added to the feedback signal waveform by this exponentially-decaying pulse is extremely small because it carries only the delayed error replica ($-\boldsymbol{E_{jitter}} \cdot \boldsymbol{Z^{-1}}$), whose dynamic-range is much smaller than that of the original feedback signal (data + shaped quantization noise) coming from the NRZ DAC. The key point is to combine the rectangular waveform and the exponentially-decaying waveform efficiently to achieve the required error spectral shaping without adding high requirements on the op-amp SR. Another advantage of the small signal swing of the exponentially-decaying waveform carrying the error signal is

that it lends itself to buffering without suffering nonlinearities, in contrast to the case of an SCR DAC in which the exponentially-decaying waveform is carrying the whole feedback signal. This point will be illustrated further in sub-section 6.3.3 discussing the proposed circuit implementation of the hybrid DAC. The proposed hybrid error shaping technique can be implemented with minimized additional hardware (a simple SC sampling circuit and additional CS DAC, as shown in Fig. 6.2). Also, the spectral shaping is acheived by a feedforward open loop approach and hence avoid the limitations and stability issues associated with closed loop implementations. Moreover, no blocks are added on the signal path and hence avoiding additional excess loop delay in the feedback path.

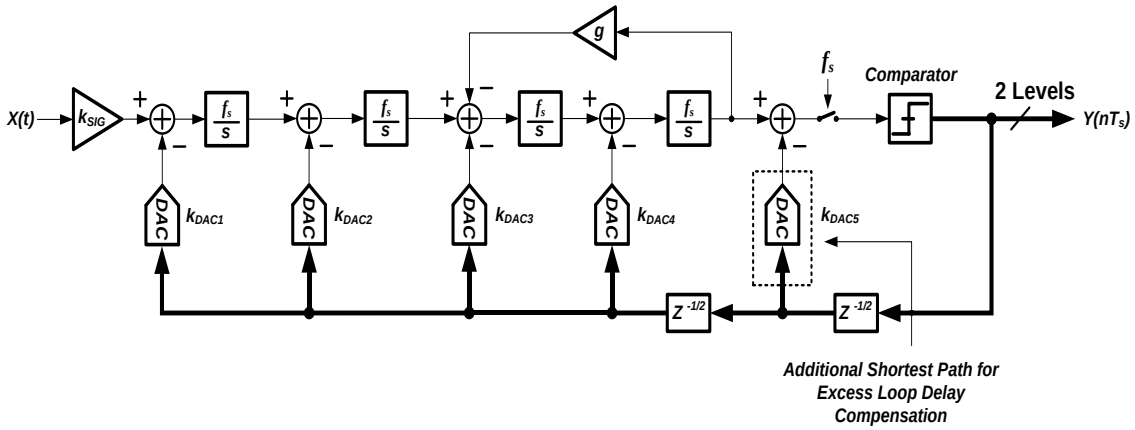
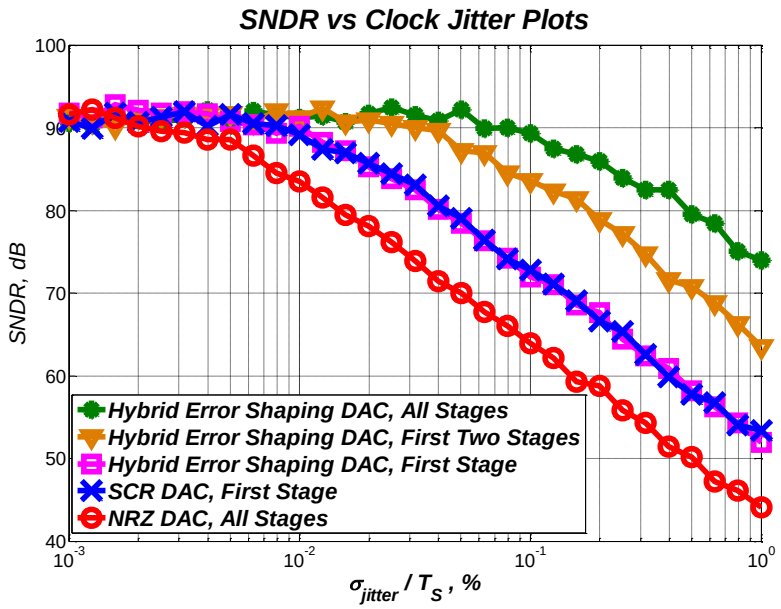


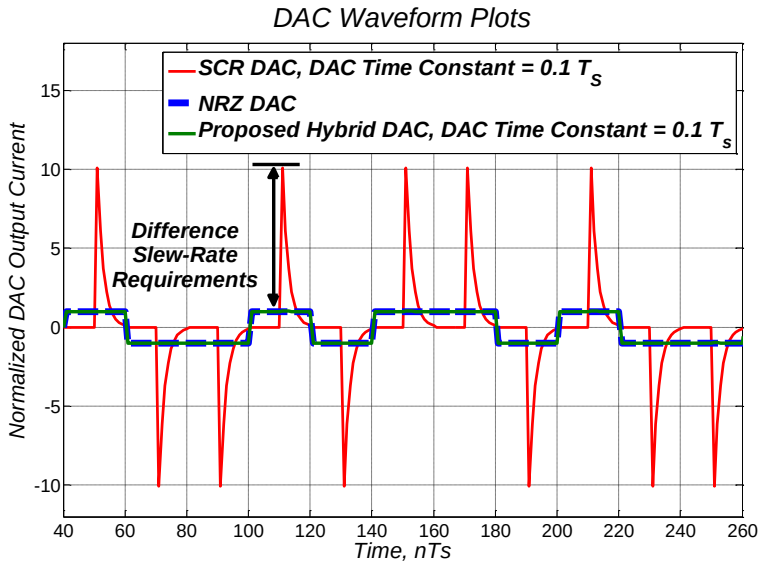
Fig. 6.3. Fourth-order single-bit continuous-time ΔΣ modulator in cascade-of-resonators-feedback (CRFB) structure.

6.3.2 System-Level Simulation Results

System-level simulations have been carried out using the CT ΔΣ modulator in Fig. 6.3 to demonstrate the performance of the proposed hybrid DAC error shaping scheme.



(a)



(b)

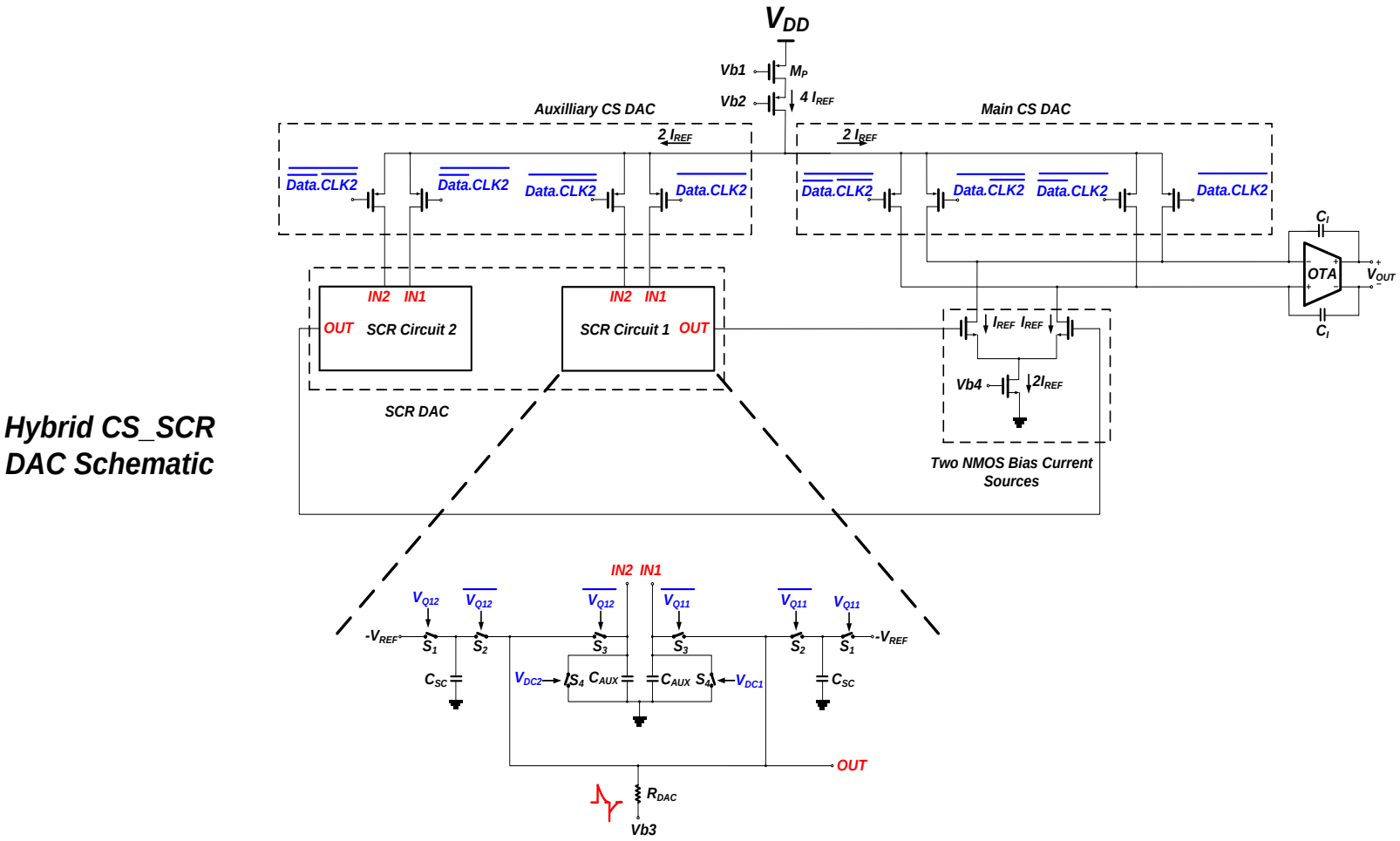
Fig. 6.4. (a) SNDR vs. clock-jitter standard deviation σ_{jitter} for different DAC implementations. (b) DAC output current waveforms.

This single-bit high-order feedback modulator is chosen because these architectures are known to be the most sensitive to PWJ due to multiple feedback DACs and also the sensitivity to PWJ is exacerbated by the presence of single-bit DACs. Thus, this modulator is a convenient test vehicle to demonstrate the potential of the proposed jitter-tolerant hybrid DAC solution. The sampling-frequency f_S is set to 20 MHz and the OSR is 50. The modulator is excited by a strong input tone at the edge of the Nyquist-rate bandwidth, such that $V_{SIG} = -6\,dBFS$, $\omega_{SIG} = 2\pi \times 191KHz$, so that to observe the effect of the blocker signal.

It can be seen that the exponentially-decaying waveform SCR DAC and the proposed error shaping scheme are providing the same jitter tolerance when applied to the feedback DAC feeding the first (outermost) integrator. As shown in Fig. 6.4(a), more robustness to feedback PWJ error can be acheived by using the proposed hybrid DAC to feed all the loop filter stages. The waveforms depicted in Fig. 6.4(b) show that the equivalent feedback current from the proposed hybrid DAC is very close to the conventional NRZ SI DAC and much smaller than the peak output current of the commonly used jitter-tolerant SCR DAC with exponentially-decaying waveform. This demonstrates that the proposed error shaping DAC solution is not adding extra requirements on the SR of the load integrator and hence saving power.

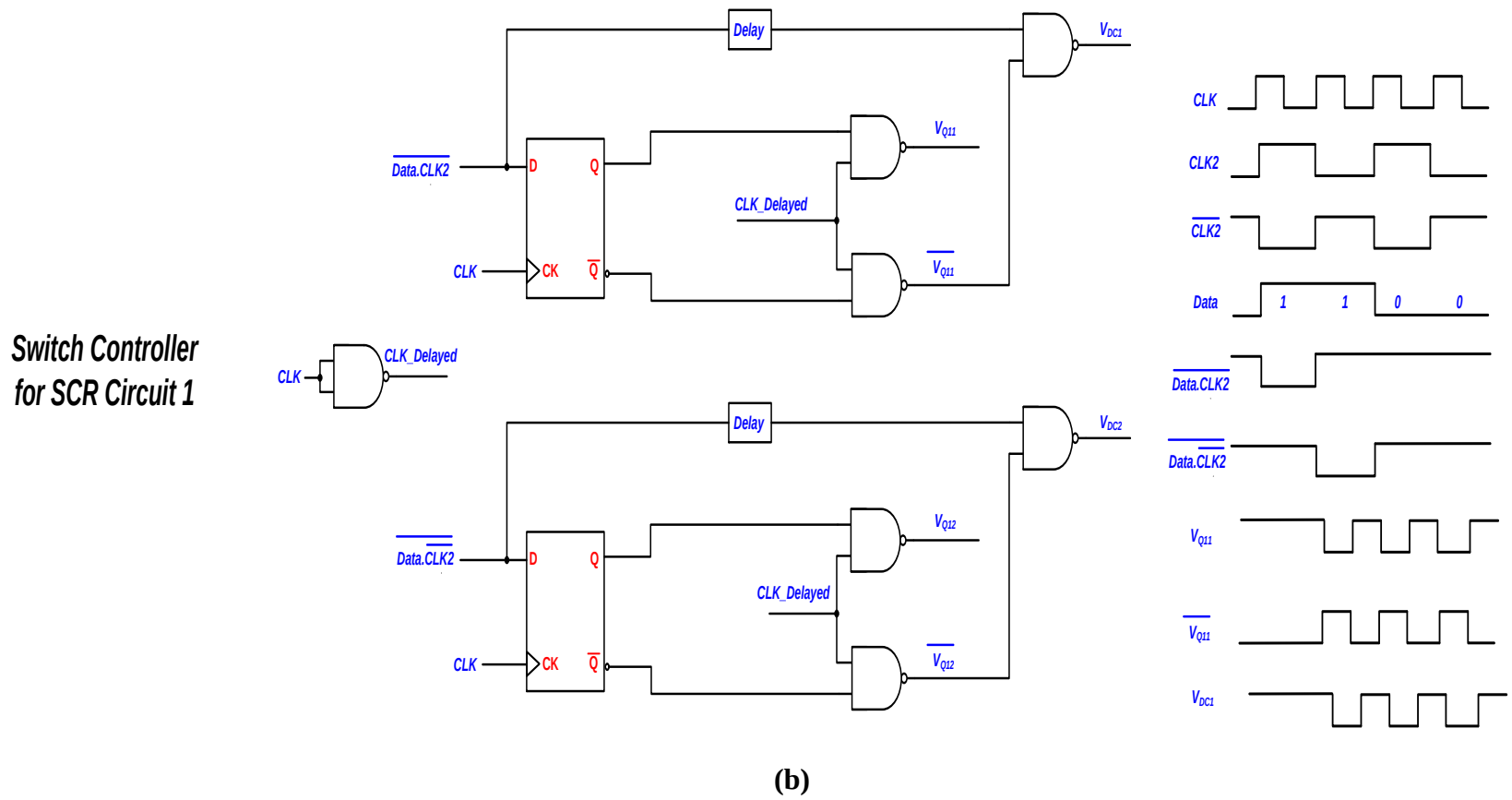
6.3.3 Circuit Level Realization of the Hybrid DAC Solution

Figure 6.5(a) shows the schematic of the hybrid CS-SCR DAC and an integrator is added at its load so that to observe the effect of PWJ on the integrated charges.



(a)

Fig. 6.5. (a) Schematic of the hybrid CS-SCR DAC. (b) Timing controller for SCR Circuit 1.



(b)

Fig. 6.5 Continued.

A single-bit DAC configuration is used to demonstrate the potential of the implemented jitter-tolerant DAC for single-bit waveforms, which are the most sensitive to PWJ. The hybrid DAC can be easily extended to multi-bit DACs; however, they suffer less from PWJ. The DAC is composed of four parts: 1- two NMOS bias current sources, 2- main PMOS CS DAC, 3- auxiliary PMOS CS DAC, and 4- SCR DAC circuit. The two bias current sources inject common-mode (CM) currents $\boldsymbol{I_{REF}}$ to prevent a CM offset from appearing at the OTA virtual ground nodes. The main DAC provides the main current waveform $2\boldsymbol{I_{REF}}$ fed to the load integrator and this waveform is suffering PWJ. During a given clock-cycle, one of the auxiliary DAC branches provides a replica of the main DAC current that is integrated on a capacitor $\boldsymbol{C_{AUX}}$, while the corresponding SC circuit samples an inverted version of the voltage value equivalent to the input digital level ($-\boldsymbol{V_{REF}}$) on a capacitor $\boldsymbol{C_{SC}}$ through switch $\boldsymbol{S_1}$. Also, $\boldsymbol{V_{REF}}$ equals the voltage resulting from charge integrated by $2\boldsymbol{I_{REF}}$ on $\boldsymbol{C_{AUX}}$ during one clock-period, without suffering PWJ. Note that $\boldsymbol{C_I = 2C_{AUX} = 2C_{SC}}$**.** In the next clock-cycle, switch $\boldsymbol{S_1}$ is opened and switches $\boldsymbol{S_2}$ and $\boldsymbol{S_3}$ are closed in the first half-cycle and $\boldsymbol{C_{AUX}}$ and $\boldsymbol{C_{SC}}$ are discharged through resistor $\boldsymbol{R_{DAC}}$. The net current flowing through the $\boldsymbol{R_{DAC}}$ is due to the PWJ induced charge error on $\boldsymbol{C_{AUX}}$ (which equals the PWJ induced charge error on $\boldsymbol{C_I}$) and has an exponentially-decaying waveform. The resulting exponentially-decaying voltage waveform across $\boldsymbol{R_{DAC}}$ drives the gate of an NMOS device in the appropriate branch of the bias current source so that to inject a negative replica of the PWJ induced error during the previous clock-cycle into the load integrator. Then, in the second half-cycle capacitor $\boldsymbol{C_{AUX}}$ is shortened through $\boldsymbol{S_4}$ to be discharged. Figure 6.5(b) shows the

controller of the switches in SCR circuit 1 and a timing diagram to illustrate the control signals of the DAC switches with a simple data sequence example (1, 1, 0, 0).

Reusing the NMOS current sources as buffers to inject the delayed inverted error replicas into the integrator avoids the need for increased GBW in the OTA and also maintains the inherent anti-aliasing when this hybrid DAC is used in a CT ΔΣ modulator. The V-to-I conversion at the buffer doesn't suffer nonlinearities because the exponentially-decaying voltage across $\boldsymbol{R_{DAC}}$ carries only the PWJ induced error and thus it is relatively very small compared to the full-scale level of the main signal. It is worth noting that to achieve efficient spectral shaping for PWJ errors, $\boldsymbol{R_{DAC}}$ needs to match $\boldsymbol{1/g_m}$ of the current source NMOS device as much as possible. Thus, the resistors $\boldsymbol{R_{DAC}}$ and the NMOS devices of the current sources need to be carefully designed and laid out. Also, the switches $\boldsymbol{S_1}$-$\boldsymbol{S_4}$ should be designed with dummy switches to minimize effects of charge injection and clock feed-through. Another advantage of the hybrid CS-SCR DAC implementation in Fig. 6.5(a) is that the noise of the upper PMOS current source transistor ($\boldsymbol{M_P}$) and the power supply noise from $\boldsymbol{V_{DD}}$, which are the main contributors to the DAC noise, experience high-pass filtering.

6.4 Chip Implementation and Experimental Results

To prove the concept of the proposed hybrid DAC solution on silicon, a test chip for the hybrid CS-SCR DAC circuit is fabricated in 90nm CMOS technology. The DAC is loaded by an active OTA-RC integrator stage, as shown in Fig. 6.6, so that to hunt the

PWJ errors at the integrator output and also to emulate the actual loading on the DAC in a CT ΔΣ modulator. The chip is powered by 1.3V supply.

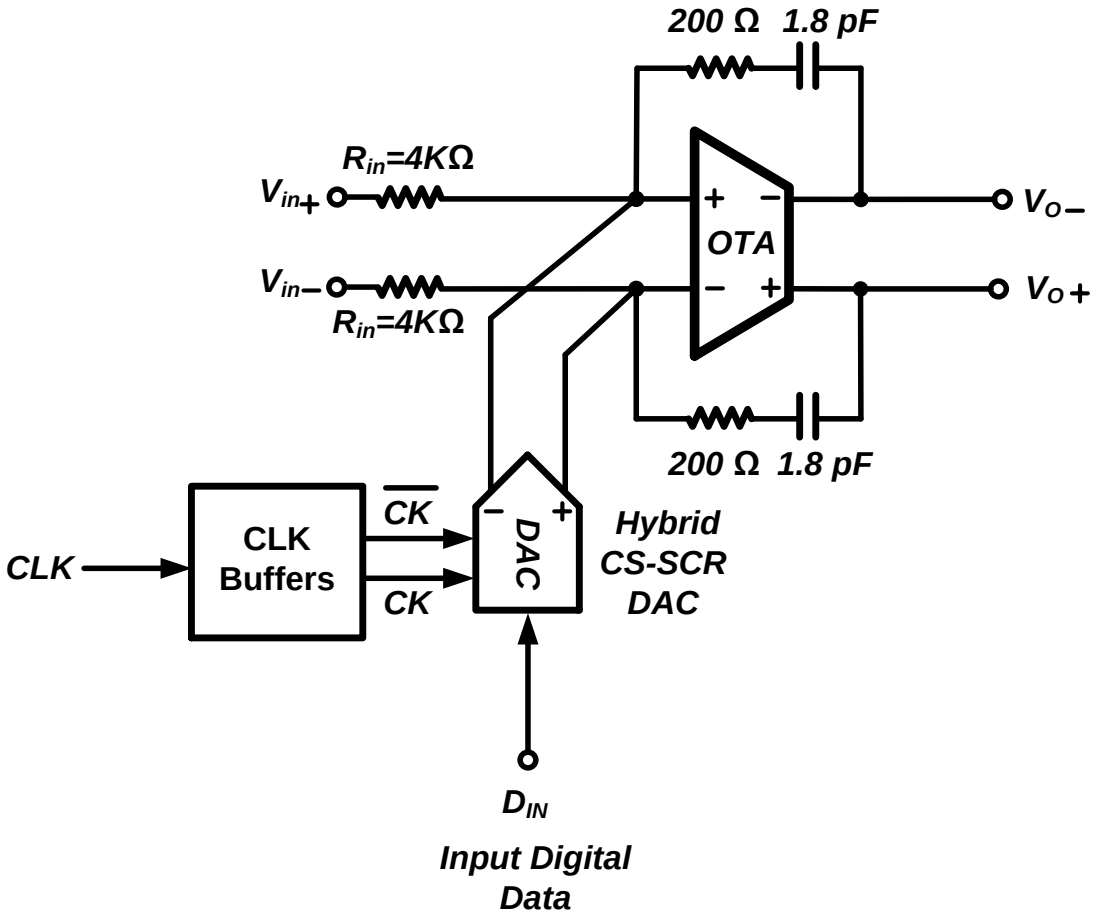


Fig. 6.6. Implemented circuit configuration.

The WCDMA baseband bandwidth of 1.92MHz is targeted. To achieve the target resolution of 11 bits, the DAC is clocked at 384MHz. The chip operates in two modes, such that the auxiliary CS DAC and SCR circuits are enabled in the hybrid CS-SCR

DAC mode and they are disabled in the conventional CS DAC mode, so that to measure the suppression of the PWJ products and in-band noise provided by the hybrid DAC.

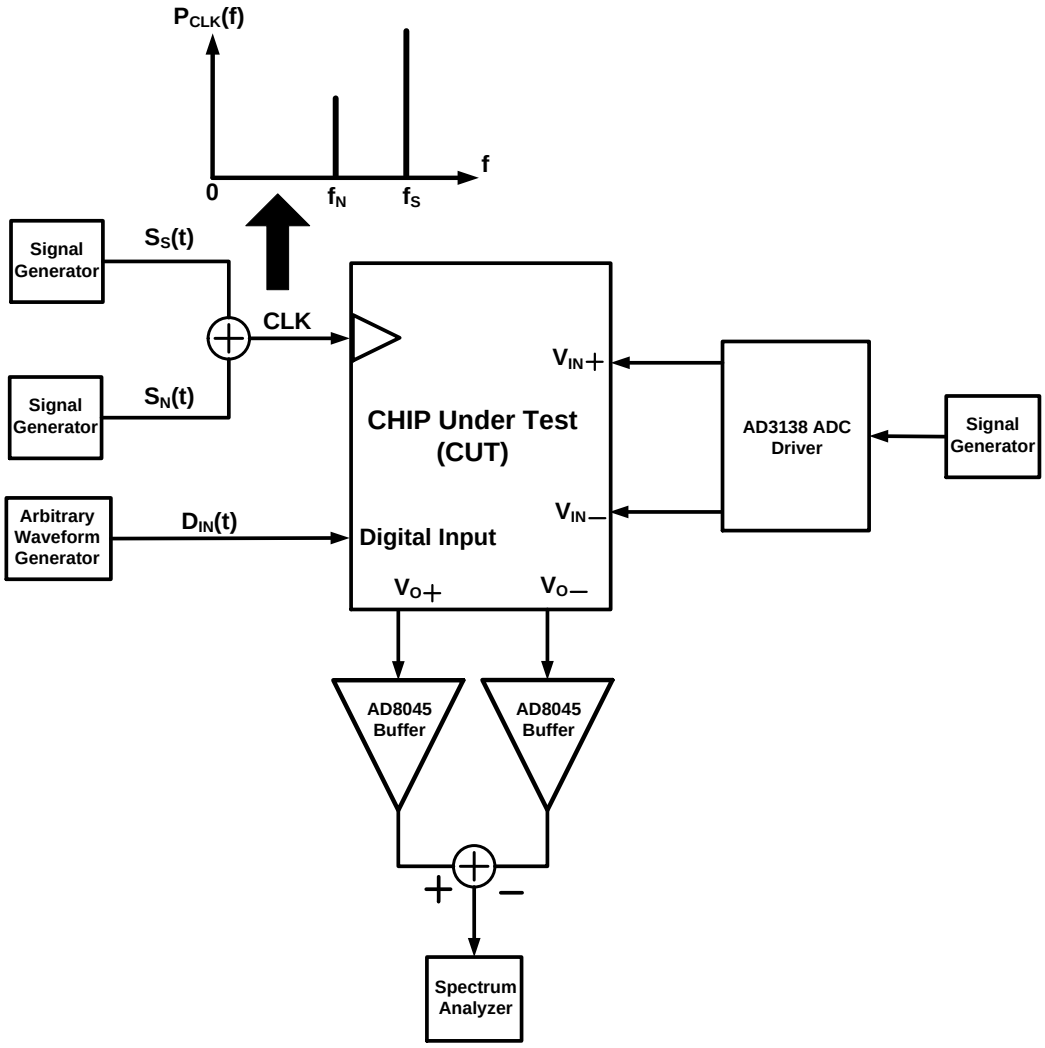


Fig. 6.7. Testing setup.

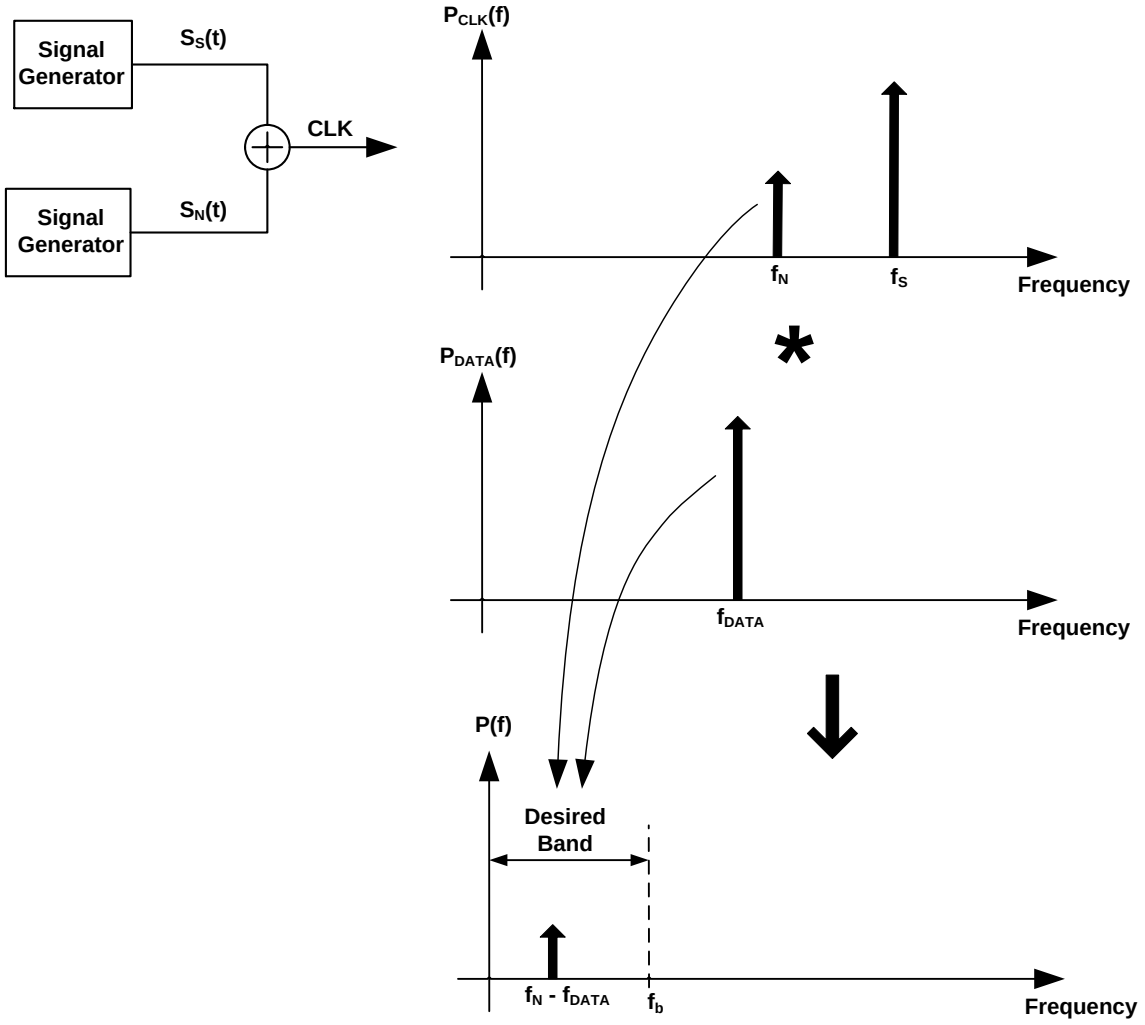
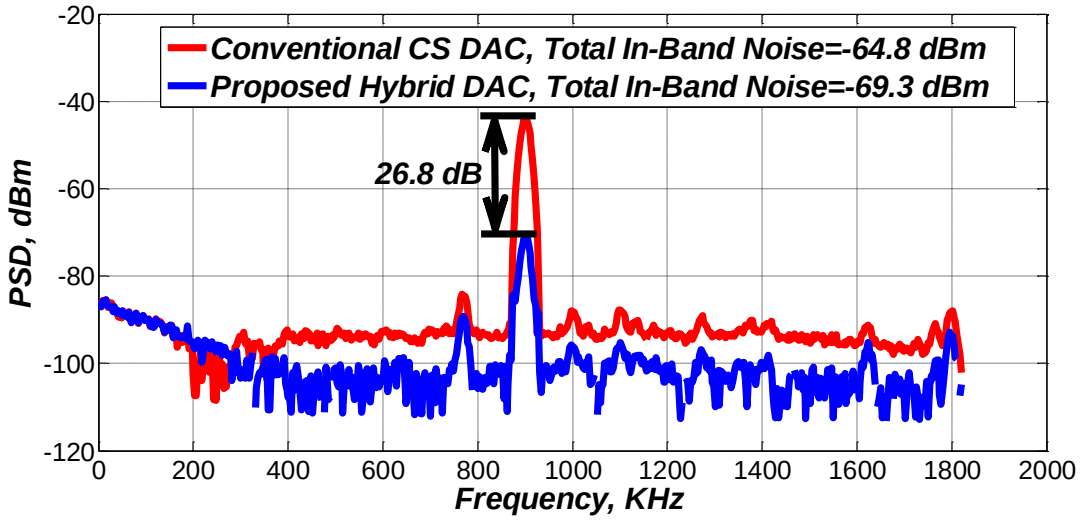
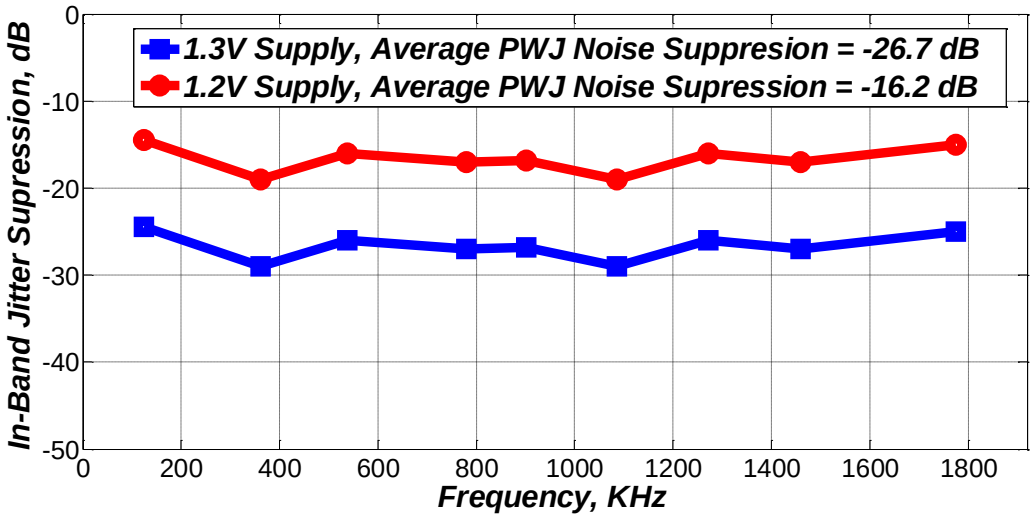


Fig. 6.8. Testing procedure based on noise tone folding due to periodic jitter in clock.

The chip was tested using the test setup in Fig. 6.7. The testing procedure, illustrated in Fig. 6.8, can be explained as follows. The sensitivity to PWJ is examined by applying a sinusoidal noise tone superimposed $\mathbf{f_N}$ on the main clock tone $\mathbf{f_S}$ to emulate the effect of periodic jitter and applying a digital single-bit tone $\mathbf{f_{DATA}}$, outside



(a)



(b)

Fig. 6.9. (a) PSD at DAC output. (b) Measured in-band folded tones suppression over the desired channel bandwidth of 1.92MHz.

the band of interest $\mathbf{f_b}$, at the DAC input. The resulting in-band convolution product represents the folding of out-of-band signals over the desired channel due to clock-jitter.

The transfer function from the DAC input to the integrator output is characterized. The PWJ induced components, referred to the DAC input, are obtained by measuring the output of the integrator using a spectrum analyzer and then the data is saved and taken on MATLAB to calculate the input-referred spectrum using the integrator transfer function characterized earlier.

Figure 6.9(a) shows the FFT at the DAC output when the DAC is tested using an 80MHz input digital tone and a sinusoidal jitter at 80.9 MHz added to the main clock tone. The jitter tone is -30dBc of the main clock tone. The hybrid DAC suppresses folded component (@ 900KHz) by 26.8dB. Also, in-band noise floor is reduced by 5dB due to DAC noise filtering offered by circuit realization of the hybrid DAC. Figure 6.9(b) shows the measured in-band suppression offered by the DAC to the folded tones over the desired channel bandwidth when the frequency of the clock noise is swept. Table 6.1 summarizes the measured performance of the chip and compares the hybrid CS-SCR DAC to the DAC reported in [23]. The die micrograph is shown in Fig. 6.10.

6.5 Conclusion

A hybrid CS-SCR DAC solution, based on feedforward spectral shaping for the jitter induced error using a NRZ rectangular waveform CS DAC and SC DAC combination, has been proposed. The new technique is shown to achieve high robustness to DAC PWJ without requiring faster settling or higher GBW in the op-amp used in the load circuit. Furthermore, this proposed hybrid CS-SCR DAC maintains the inherent anti-aliasing capability of CT $\Delta\Sigma$ modulators. The potential of the proposed hybrid DAC

solution is demonstrated on silicon through a 90nm CMOS prototype chip. The jitter-tolerant DAC chip provided attenuation for in-band jitter induced noise by 26.7dB and in-band DAC noise by 5dB, compared to conventional CS DAC. The hybrid DAC consumes 719µwatts from 1.3V supply.

Table 6.1. Summarized measured performance of the chip and comparison with the SCSR DAC reported in [23].

Property	**Value**	
	This work	**[23]**
Technique	Hybrid CS-SCR	SCSR
Technology	IBM 9LP 90nm CMOS	90nm RF-CMOS
Supply	1.3V	1.2V
Sampling Frequency	384 MHz	312 MHz
Target Signal Bandwidth	1.92 MHz	1.92 MHz
OSR	100	81
Peak SNR	68.2 dB	-
In-band Jitter Suppression	26.7 dB	30 dB
Average in-band DAC current sources Noise Suppression	**5 dB**	-
Maintains inherent anti-aliasing if used in CT ΔΣ modulator	**Yes**	**No**
Chip Power Consumption		
OTA	**1.07 mW**	**2.688 mW**
DAC Core	**719 µW**	**1.08 mW**
Dynamic Power (Controller + Clock Buffers + Drivers)	2.62 mW	-
Total	4.42 mW	-
Chip Area		
DAC	0.166 mm^2	-
OTA-RC Integrator	0.08625 mm^2	-
Total	0.252 mm^2	-

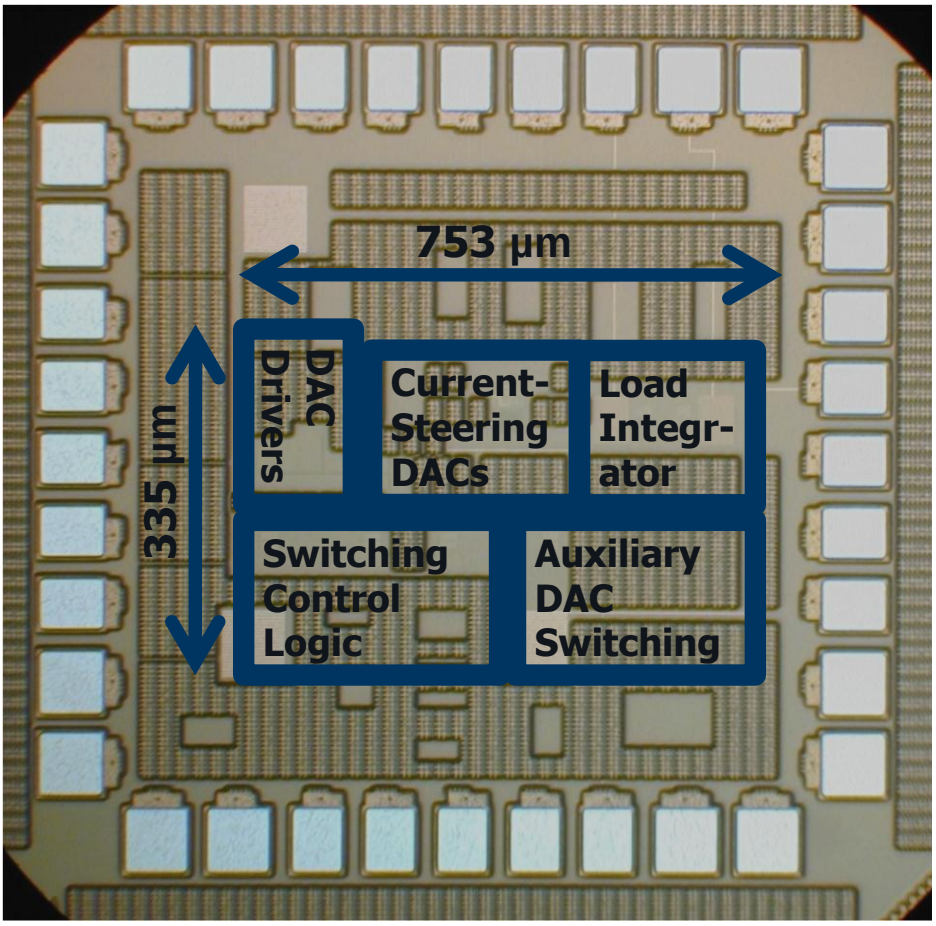


Fig. 6.10. Chip die photo.

7. SENSITIVITY TO LOOP FILTER NONLINEARITIES AND NOISE FOLDING IN PRESEONCE OF BLOCKERS[*]

7.1 Introduction

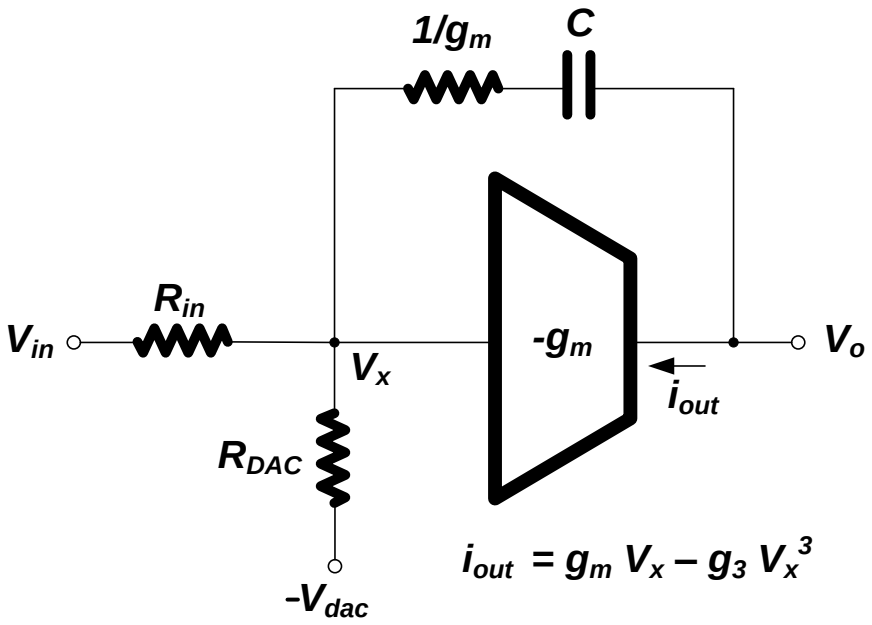
In a ΔΣ loop, critical nonlinearities come from the feedforward paths (loop filter) and the feedback paths (if multi-bit DAC is used). Particularly, in-band distortion errors generated by nonlinearities of the components used in the first stage of the loop filter or inherent mismatch between unit cells in the outermost DAC appear at the output without shaping. Recall that errors generated at inner stages in the loop filter or at the quantizer are suppressed by the preceding filter stages. In studying the sensitivity to nonlinearities in presence of large OOB blockers, we need to focus on the loop filter input-referred distortion rather than nonlinear behavior resulting from mismatch in DAC unit cells for two main reasons. First, according to previous sections, a blocker-tolerant ΔΣ ADC will need to show adequate attenuation for OOB blockers in the loop filter. Thus, the remaining residual blocker components appearing in the feedback path will be much weaker than blockers coming from the ADC input, making loop filter nonlinearity more critical. Second, there are several techniques that have been adopted throughout the literature to alleviate the effect of DAC nonlinearities (e.g. using single-bit DAC, dynamic element matching, data-weighted averaging, and shuffling). Thus, in the following analysis, only the sensitivity to loop filter nonlinearity will be considered.

[*] Part of this chapter is reprinted with permission from "Sensitivity Analysis of Continuous-Time ΔΣ ADCs to Out-of-Band Blockers in Future SAW-Less Multi-Standard Wireless Receivers," by Ramy Saad, Diego Luis Aristizabal-Ramirez, and Sebastian Hoyos, September 2012. *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 9, pp. 1894-1905.

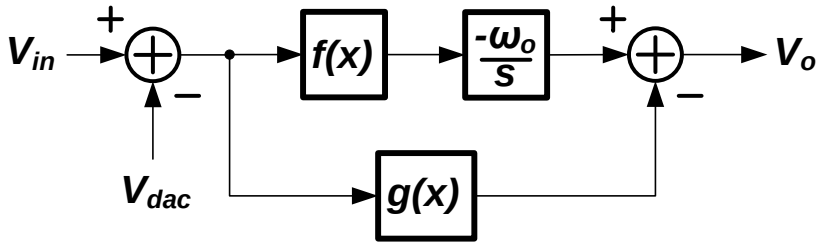
For conventional ΔΣ modulators, the requirement on loop filter nonlinearity, calculated according to the required spurious-free dynamic-range (SFDR), is specified for in-band signals only. In other words, distortion quantities are calculated using in-band tones (e.g. two-tone test using two in-band tones for intermodulation (IM) measurement) [9]. This is expected because the signal applied to the ADC is blocker-free, and hence the OOB signal power is negligible. However, in presence of large OOB blockers, specifications of loop filter nonlinearities need to be calculated with awareness of the expected OOB blocking power, especially when the desired signal is weak. This can be estimated using the blocker profile described in each standard as well as the maximum expected carrier/channel power from each one of the other standards supported by the wireless handset receiver. Thus, a blocker-tolerant ΔΣ modulator needs to feature sufficient linearity in the loop filter so that to maintain the target SFDR for in-band signals and achieve the required signal-to-noise-plus-distortion ratio (SNDR) in presence of large OOB blockers. Moreover, the modulator may need to fulfill additional blocker-related tests (e.g. IM test and amplitude-modulation (AM) suppression test) required by some wireless standards like GSM [33].

In this section, the performance sensitivity of CT ΔΣ modulators to loop filter nonlinearities in presence of large OOB blockers are analyzed in details. The section is organized as follows. Section 7.2 described the nonlinear model for the loop filter stages that will be used in the following nonlinearity analysis. The problem of noise folding caused by nonlinearities in presence of large OOB blockers is explained in section 7.3. In section 7.4, the proposed solution for the noise folding problem is presented and

verified by simulations. Conclusions are drawn in section 7.4.



(a)



(b)

Fig. 7.1. Zero-compensated OTA-based active-RC inverting integrator stage. (a) Circuit realization. (b) Equivalent model including nonlinearities.

7.2 Integrator Model Including Nonlinearities

It is instructive to analyze and model the nonlinearity of the loop filter stages so that to proceed with the discussion of its effects on the ΔΣ modulator operation in presence of OOB blockers thereafter. Since the first integrator is the dominant source of distortion, the rest of the loop filter will be considered linear for simplicity of the analysis. Detailed analysis covering various aspects of nonlinearities in ΔΣ modulators are given in [44], [45]. A commonly used integrator stage in CT ΔΣ modulators is the active-RC integrator. A zero-compensated active-RC integrator using an operational transconductance amplifier (OTA) is shown in Fig. 7.1(a). Following the analysis given in [46], without loss of generality, the feedback DAC signal is assumed to be a voltage V_{DAC} applied through a resistive branch whose resistance is equal to that of the input branch, $R_{in} = R_{DAC} = R$. It is worth noting that that loop filter integrators are usually implemented in a fully-differential scheme and hence the even-order distortion terms are extremely attenuated causing the distortion behavior to be mainly dominated by the third-order nonlinearity term. The transconductor is assumed to be weakly nonlinear with the output current being related to the input voltage as $i_O = g_m V_x - g_3 {V_x}^3$. The output voltage V_O can be expressed as

$$V_O(t) = \frac{-1}{C}\int_0^t \left(\frac{V_{in} - V_{DAC} - 2V_x}{R}\right) dt - \frac{1}{g_m}\left(\frac{V_{in} - V_{DAC} - 2V_x}{R}\right) + V_x \,. \qquad (7.1)$$

Applying KCL at the OTA input,

$$\frac{V_{in} - V_{DAC} - 2V_x}{R} = g_m V_x - g_3 {V_x}^3 \,. \tag{7.2}$$

Solving for V_x and keeping terms up to third-order,

$$V_x \approx \frac{V_{in} - V_{DAC}}{(2 + g_m R)} + g_3 R \frac{(V_{in} - V_{DAC})^3}{(2 + g_m R)^4} \,. \tag{7.3}$$

Substituting this in (7.1) (and again retaining terms up to third-order) yields

$$V_O(t) \approx \frac{-1}{C} \int_0^t \frac{g_m (V_{in} - V_{DAC})}{(2 + g_m R)} - \frac{2 g_3 (V_{in} - V_{DAC})^3}{(2 + g_m R)^4} dt + \frac{g_3}{g_m} \frac{(V_{in} - V_{DAC})^3}{(2 + g_m R)^3} \,. \tag{7.4}$$

From the expression in (7.4), the integrator nonlinearity can be modeled as shown in Fig. 7.1(b), where the integrator unity-gain frequency ω_o is given by

$$\omega_O = \frac{1}{RC} \frac{1}{\left(1 + \frac{2}{g_m R}\right)} \,, \tag{7.5}$$

and the characteristic functions for the input-referred distortion $f(x)$ and the output additive distortion $g(x)$ are expressed as

$$f(x) = x - \frac{2g_3}{g_m} \frac{x^3}{(2 + g_m R)^3} . \tag{7.6}$$

$$g(x) = \frac{g_3}{g_m} \frac{x^3}{(2 + g_m R)^3} . \tag{7.7}$$

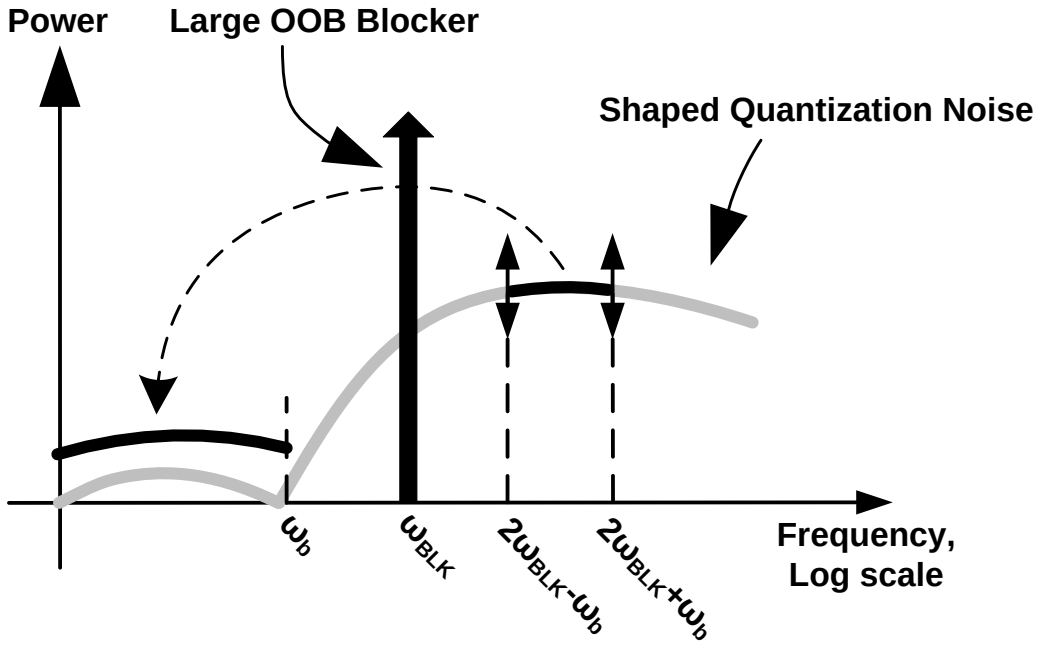


Fig. 7.2. Noise folding caused by intermodulation between OOB blocker and shaped quantization noise.

7.3 Noise Folding Problem

A critical performance degradation effect caused by loop filter nonlinearity, in presence of large OOB blocking power, is noise folding. As illustrated in Fig. 7.2, intermodulation between strong OOB blockers (coming from ADC input) and high-pass shaped noise (coming from feedback) causes noise folding over the desired channel. To

analyze this effect, consider a blocker tone $x_{BLK}(t) = A_{BLK}\cos\omega_{BLK}t$ and a quantization noise tone $x_{QN}(t) = A_{QN}\cos\omega_{QN}t$, which experience third-order nonlinearity with a coefficient α_3. The resulting IM products are given by [47]

$$\omega = 2\omega_{BLK} \mp \omega_{QN}: \frac{3\alpha_3 A_{QN}A_{BLK}^2}{4}\cos(2\omega_{BLK} - \omega_{QN})t + \frac{3\alpha_3 A_{QN}A_{BLK}^2}{4}\cos(2\omega_{BLK} + \omega_{QN})t\,. \tag{7.8}$$

$$\omega = 2\omega_{QN} \mp \omega_{BLK}: \frac{3\alpha_3 A_{BLK}A_{QN}^2}{4}\cos(2\omega_{QN} - \omega_{BLK})t + \frac{3\alpha_3 A_{BLK}A_{QN}^2}{4}\cos(2\omega_{QN} + \omega_{BLK})t\,. \tag{7.9}$$

Equations (7.8) and (7.9) can be used to draw some observations with the aid of Fig. 7.2 as follows. First, quantization noise power is shaped by the NTF over the whole band from 0 to $2\pi f_s$ and thus in reality, for a given OOB blocker frequency ω_{BLK}, intermodulation expressed in (7.8) and (7.9) will occur between the blocker and all the quantization noise components. Second, since OOB blockers are out of the wanted channel ($\omega_{BLK} > \omega_b$, where $\omega_b = 2\pi \times BW$) errors appearing over the desired band due to noise-blocker intermodulation will result from the first terms in (7.8) and (7.9). Although other terms entailing frequency addition can result in errors around f_s that can alias back over the desired channel after sampling, these errors will be attenuated by the inherent anti-aliasing in CT ΔΣ implementations. Third, because the in-band quantization noise is typically very weak (due to noise shaping) and recalling that OOB

blocker frequencies are $\gg \omega_b$, in-band intermodulation induced errors will result from out-of-channel shaped noise components and blockers. It is important to note that for near blockers (not OOB) and for far OOB blockers (ω_{BLK} close to $2\pi f_s$), noise folding is

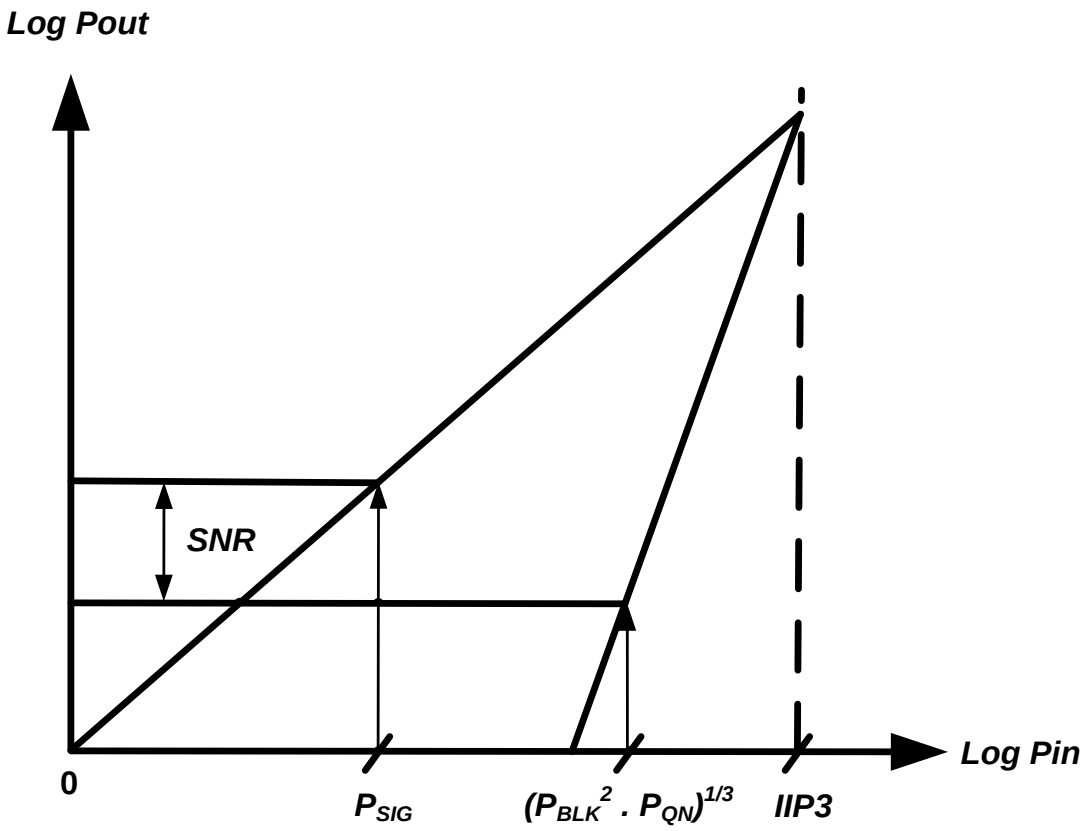


Fig. 7.3. Derivation of loop filter *IIP3* in presence of OOB blockers according to noise folding.

very weak because the blocker signal intermodulates with very low noise power to produce in-band errors. Fourth, in presence of strong OOB blockers ($\gg$ shaped noise components), the first term in (7.8) dominates the noise folding because it is a stronger

function of the blocker level A_{BLK} (A_{BLK} is squared). Recall that for typical ΔΣ modulators, magnitude levels of out-of-channel shaped noise components $A_{QN} < -30\,dBFS$. Particularly, effective folded noise components that fall in the wanted channel are those generated by the intermodulation between the OOB blocker and the shaped quantization noise over the frequency range $2\omega_{BLK} - \omega_b \rightarrow 2\omega_{BLK} + \omega_b$ (see Fig. 7.2). On the other hand, if the OOB blocker is not sufficiently strong (≤ out-of-channel shaped noise component at its respective frequency), the effect of noise folding is negligible and cannot yield effective additive error over the wanted channel.

The required IIP_3 for the loop filter, according to noise folding, can be calculated using the graphical representation of Fig. 7.3. P_{SIG}, P_{BLK}, and P_{QN} denote the signal power, blocker power, and integrated quantization noise power in the band $2\omega_{BLK} - \omega_B \rightarrow 2\omega_{BLK} + \omega_B$, respectively, at the loop filter input. The ratio of desired signal to intermodulation products should satisfy the required SNR to achieve a prescribed BER specification. According to Fig. 7.3, the IIP_3 requirement on the loop filter according to noise folding is determined by the following inequality:

$$IIP_3 - P_{SIG} + SNR \leq 3(IIP_3 - \frac{2P_{BLK}}{3} - \frac{P_{QN}}{3})$$

$$\xrightarrow{yields} IIP_3 \geq \frac{2P_{BLK} + P_{QN} - P_{SIG} + SNR}{2}\,. \tag{7.10}$$

CT simulations have been carried out using the ΔΣ modulator in Fig. 3.2(a) to verify the results and observations derived in this section about noise folding. The first stage in the loop filter is modeled using the nonlinear integrator model given in Fig. 7.1(b) with a nonlinearity factor corresponding to $IIP_3 = 23\,dBFS$. The power spectra

depicted in Fig. 7.4 are calculated by applying a Fast Fourier Transform (FFT) using a Blackman-Harris window on the digital output bit stream. Obviously, the in-band noise floor increases with the blocker amplitude due to noise folding and hence the achievable SNDR drops accordingly. The blocker components appearing in the FFT plots are lower than their original values due to attenuation in the loop filter. However, noise folding occurs at the first integrator with the OOB blocker tone at full amplitude before being attenuated. For sufficiently large OOB blocker levels, the SNDR drops below zero, as shown in Fig. 7.4, and weak in-band signals are no longer detectable. This effect limits the ADC sensitivity. Plots in Fig. 7.5 show the degradation in the ADC sensitivity and DR due to noise folding. Figure 7.6 shows the sensitivity of noise folding to OOB blocker level. As can be observed, for an OOB blocker tone at 5.6 MHz, noise folding, due to nonlinearity of the first integrator stage is effective for blocker amplitudes > $-10\ dBFS$, whereas for lower blocker levels, folded noise is negligible. The noise folding effect is mainly dominated by the nonlinearity of the first stage in the loop filter for two reasons. First, the frequency shaping offered by the first integrator attenuates the noise folded at the succeeding stage in the loop filter chain. Second, as the OOB blocker signal propagates in the loop filter, it gets attenuated and thus noise folding components are reduced. Recall that, as mentioned earlier, noise folding is weak for near blockers whereas critical blockers are those far from the channel and nearer to the Nyquist sampling rate and thus they get attenuated upon integration (ω_{BLK} > unity-gain frequency of the integrator ω_u). The simulations in Fig. 7.6 were performed with a non-

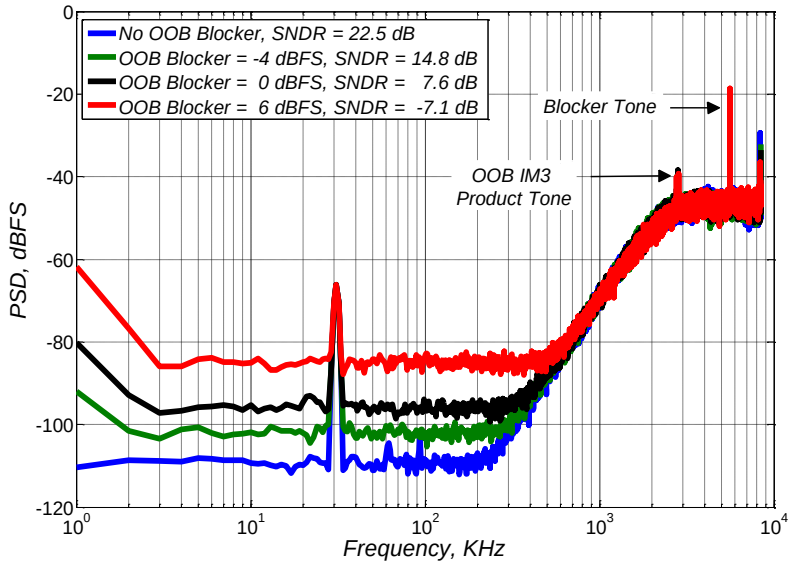


Fig. 7.4. Power spectra at the output of a third-order CT modulator in presence of an OOB blocker tone at $5.6\ MHz$, $A_{SIG} = -65\ dBFS$, $f_{SIG} = 31\ KHz$, first stage $IIP_3 = 23\ dBFS$.

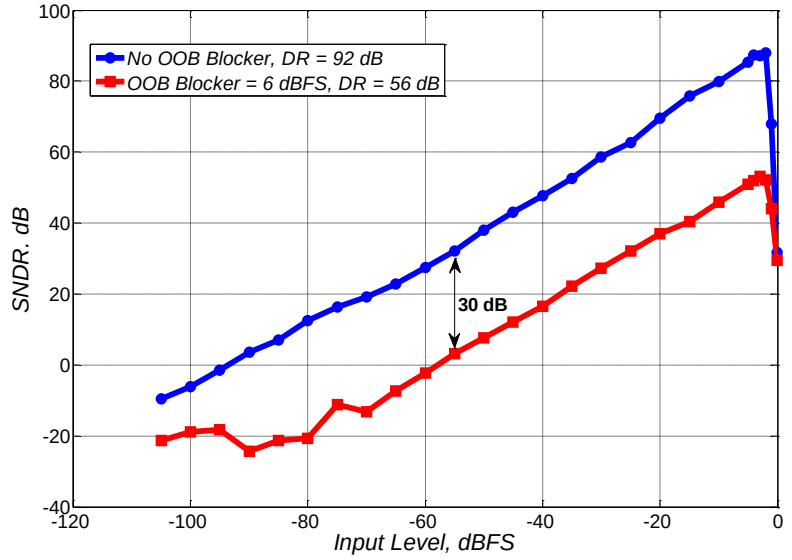


Fig. 7.5. DR degradation due to noise folding in presence of a $6\ dBFS$ OOB blocker tone at $5.6\ MHz$, $f_{SIG} = 31\ KHz$, first stage $IIP_3 = 23\ dBFS$.

linear integrator modeled in the first stage, second stage, and both. As can be seen, on introducing nonlinearities in the second integrator stage only, the IBN is not increasing with the blocker level; indicating that noise folding at the second stage is almost ineffective and causes very minute increase in the IBN. This is further illustrated by the distinct similarity when comparing the results of nonlinearity at the first stage only and nonlinearity at both stages. The increase in the IBN level in case of having nonlinearities in the second stage only compared to the ideal case in which all the filter stages are linear is coming from the in-band distortion due to intermodulation between OOB noise components and thus it is not sensitive to the blocker level. It is worth noting that the maximum tolerable OOB blocker level at the ADC input was in the range of $-10\ dBFS \rightarrow 0\ dBFS$ in the plots of Fig. 5.4, whereas in Fig. 7.6 the maximum tolerable blocker level is higher. Recall that, owing to their stronger low-pass filtering, compared to feedforward counterparts, feedback CT ΔΣ modulators can tolerate larger blocker levels while maintaining loop stability.

Although the foregoing analysis assumed a single blocker tone for simplicity, in reality the effective OOB blocking power can be distributed over several blockers and not necessarily concentrated in one blocker tone or channel. Recall that it is very likely for ADCs used in SAW-less multi-standard/multi-band wireless terminals (not using RF band-select or baseband channel-select filtering before the ADC) to receive multiple OOB blockers at different frequencies. Even if these blockers are weak, they can be many due to existence of several wireless applications serving various needs of consumers in a given area, and hence they can sum up to a large OOB blocking power.

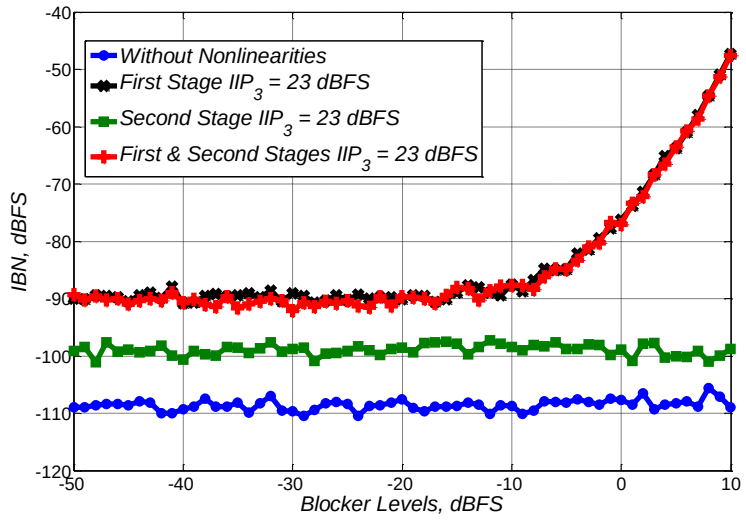


Fig. 7.6. IBN sensitivity to OOB blocker level due to noise folding, OOB blocker tone at $5.6\ MHz$, $A_{SIG} = -65\ dBFS$, $f_{SIG} = 31\ KHz$.

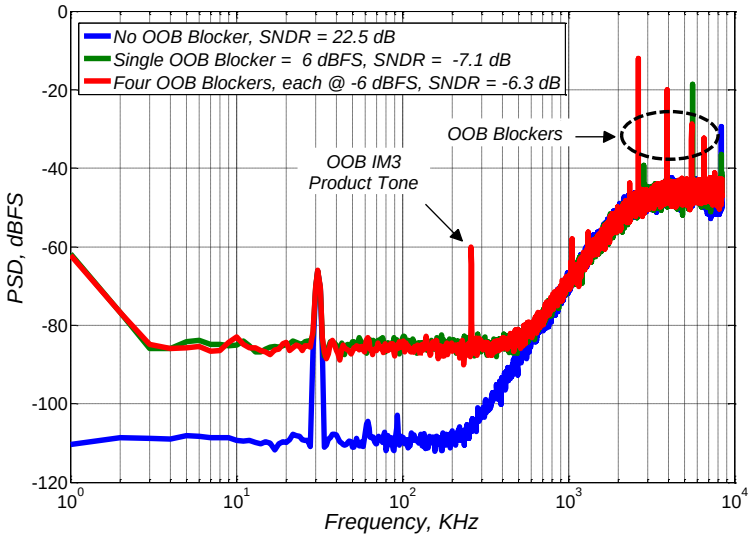


Fig. 7.7. Power spectra at the output of a third-order CT modulator in presence of single OOB blocker tone, $f_{BLK} = 5.8\ MHz$ and four OOB blocker tones, $f_{BLK1} = 2.63\ MHz$, $f_{BLK2} = 3.94\ MHZ$, $f_{BLK3} = 5.52\ MHZ$, $f_{BLK4} = 6.57\ MHZ$, $A_{SIG} = -65\ dBFS$, $f_{SIG} = 31\ KHz$, first stage $IIP_3 = 23\ dBFS$.

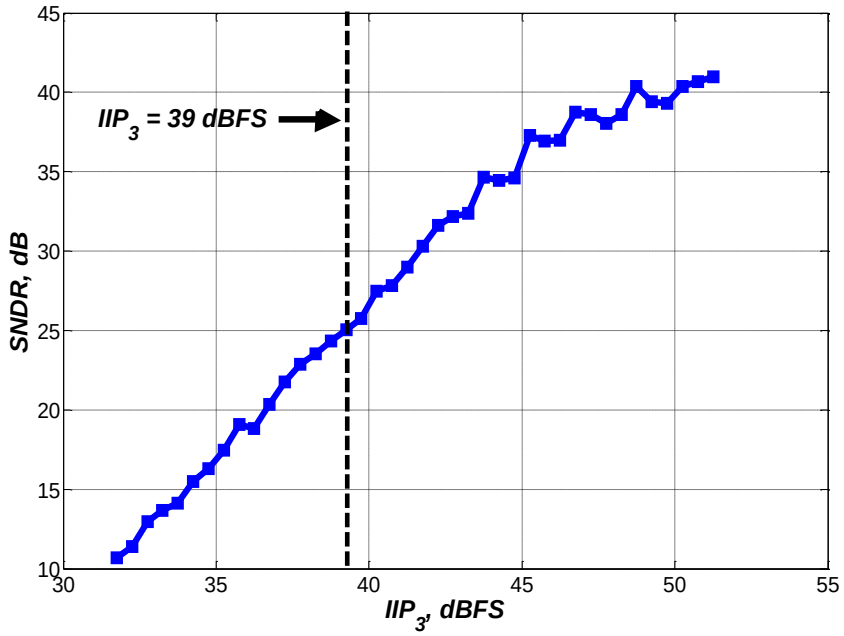


Fig. 7.8. IIP_3 requirement on the loop filter. 6 $dBFS$ OOB blocker tone at 5.6 MHz, $A_{SIG} = -65\ dBFS$, $f_{SIG} = 31\ KHz$.

Furthermore, the emerging technologies in wireless communications (e.g. LTE) are adopting OFDM system in which the channel information is distributed over several orthogonal carriers. Again this fact indicates that the OOB blocking power can be distributed over several blocking signals and not only around a certain carrier frequency. Therefore, it is instructive to examine the effect of noise folding in presence of multiple blocker tones. The FFT power spectra given in Fig. 7.7 show the equivalence between noise folding caused by a single OOB blocker tone whose amplitude level is 6 $dBFS$, and four equal OOB tones at different frequencies, each of which has an amplitude 12 dB lower than that of the single blocker. It is evident that for a given blocking power,

a combination of some lower power OOB blockers can yield noise folding equivalent to that caused by a single stronger blocker. Again, the difference in the blockers amplitudes appearing in the red plot is due to the amplitude response of the STF.

The plot in Fig. 7.8 shows the SNDR sensitivity to the IIP_3 of the input stage of the loop filter, due to noise folding, in presence of a $6\,dBFS$ $5.6\,MHz$ OOB blocker. From this plot we can infer that noise folding is the main limitation on the OOB nonlinearity of the loop filter input stage in presence of large OOB blockers. As can be seen from Fig. 7.8, to detect a weak signal of $-65\,dBFS$ at an SNR of $25\,dB$ in presence of a $6\,dBFS$ OOB blocker, an $IIP_3 \geq 39\,dBFS$ is required, which is an extremely tough requirement on the linearity of the first stage in the loop filter.

7.4 Proposed Approach to Relax Sensitivity to Noise Folding

The problem of noise folding can be remedied by making two observations. First, noise folding happens because the incoming blockers and feedback shaped noise experience nonlinearities after the two signals are combined together, as exemplified by equations (7.8) and (7.9). Second, noise folding effect is substantially suppressed after first integration stage. Thus, a potential approach to alleviate the problem of noise folding is to move the common nonlinearities seen by the blockers and shaped noise together (after being combined through an integrator stage) after the first integration operation. That is, if the blocker signal and the shaped noise get integrated and then combine and experience nonlinearities after the first integration, then the resulting noise

folding components will be much lower than the conventional case in which they combine and intermodulate together at the ADC input and before the integration.

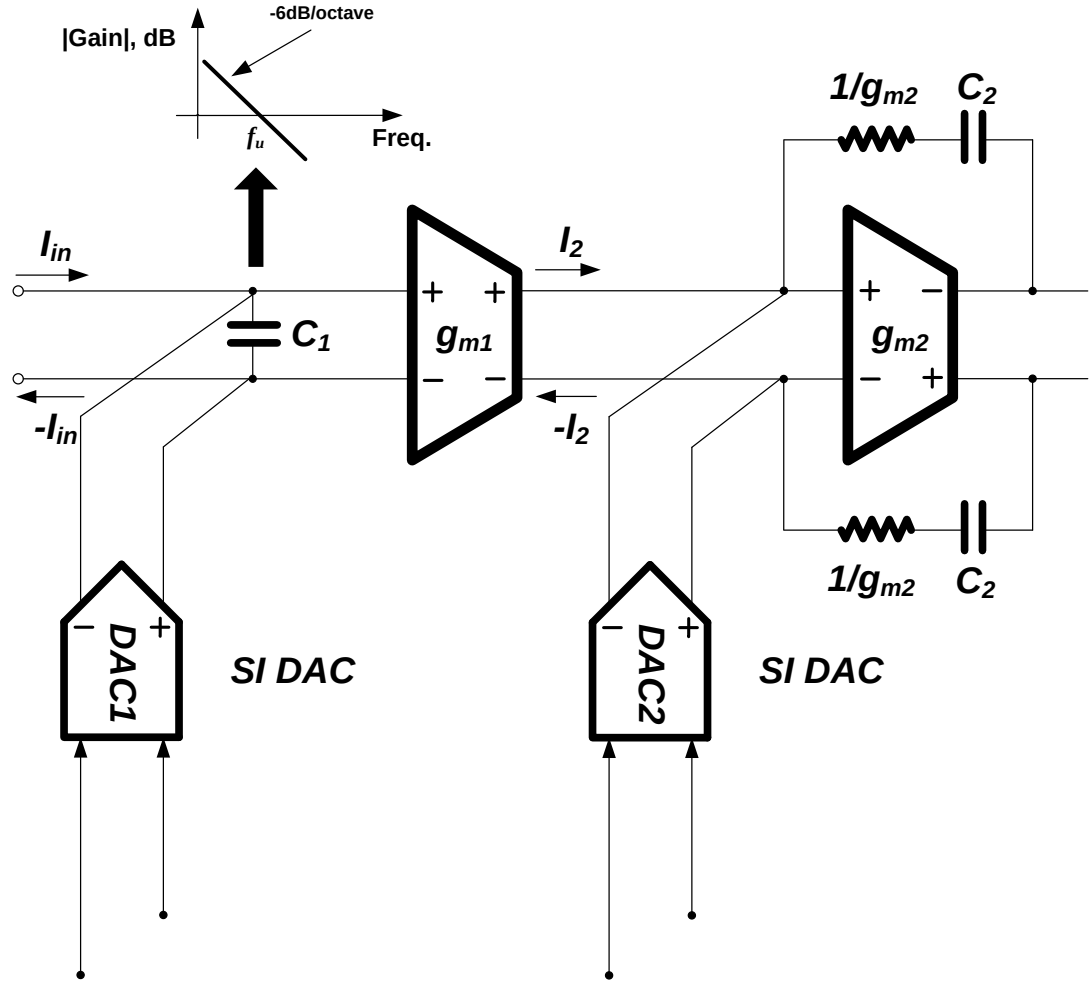


Fig. 7.9. First two integrator stages in a CT loop filter with a current-mode input integrator stage.

A possible solution is to use current-mode integrator at the input of the modulator, as illustrated in Fig. 7.9. The key point here is that the input and the feedback

are provided as currents integrated on the input capacitor and the integrated signal is applied to the next integrator stage through a transconductance amplifier that converts the integrated voltage into current.

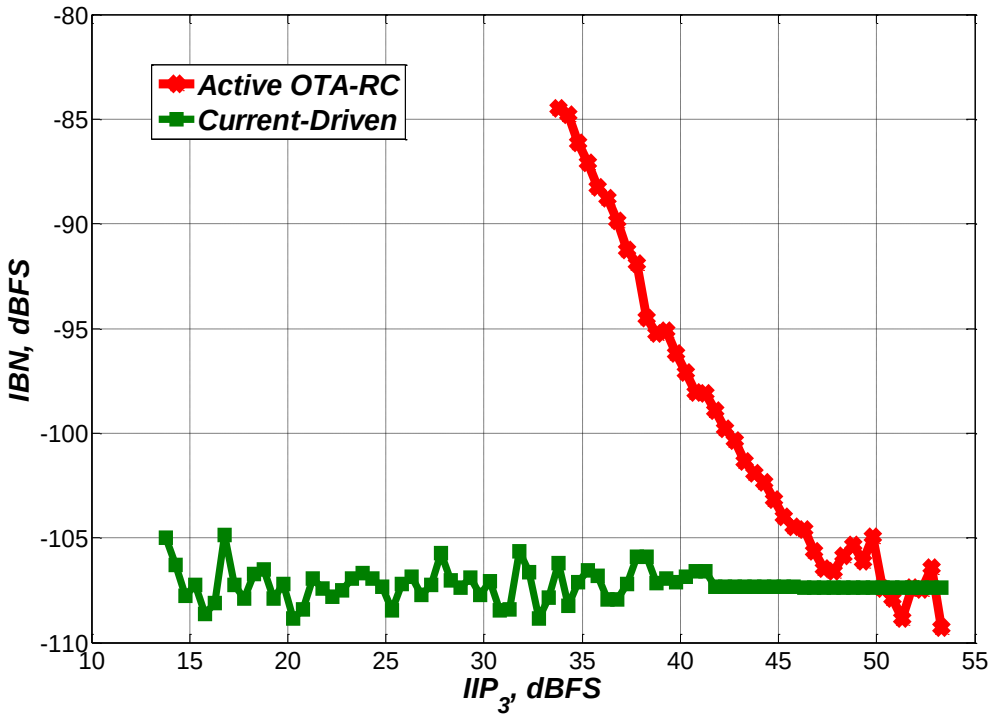


Fig. 7.10. Sensitivity of total IBN to IIP_3 of the first integrator stage in the loop filter for a current-mode integrator and an active-RC integrator. 6 $dBFS$ OOB blocker tone at 5.6 MHz, $A_{SIG} = -65\ dBFS$, $f_{SIG} = 31\ KHz$.

Thus, the blocker signal and the feedback shaped noise get integrated firstly in the input capacitor and then the integrated signal experience the input nonlinearity of the Gm-stage as well as the output nonlinearity of the stage preceding the ADC (possibly the variable-gain transconductance amplifier). That is, the combined signal (blocker +

shaped noise) experiences nonlinearities and intermodulation after the integration, resulting in a very weak sensitivity of the performance to noise folding. The plots in Fig. 7.10 indicate that the requirement on the IIP_3 of the Gm amplifier used in the first stage in the loop filter is not limited by noise folding when using a current-driven input stage, since the noise folding takes place after the first integration stage. On the other hand, for the conventional case in which an active-RC integrator is used at the input stage, the IBN is increasing significantly as the IIP_3 of the active-RC integrator goes down due to noise folding. That is, noise folding is the main limitation on nonlinearity if active-RC integrator stage is used at the input, whereas when using a current-mode input stage with a passive capacitor for integration the requirement on the nonlinearity of the following amplifier is no longer limited by noise folding.

7.5 Conclusion

The limitations on the achievable performance caused by loop filter nonlinearities in presence of large OOB blockers were discussed and it has been shown that, in presence of a $6\ dBFS$ OOB blocker, noise folding at the first integrator stage, with $IIP_3 = 23\ dBFS$, can significantly deteriorate the ADC sensitivity by 30 dB, turning weak desired signals undetectable. Furthermore, in presence of large OOB blockers, the noise folding problem raises the IIP_3 requirement on the first stage in the loop filter to extremely high values ($\sim 39\ dBFS$). A potential solution is proposed to mitigate the sensitivity to noise folding through current-mode integration at the ADC input stage.

8. SUMMARY AND CONCLUSIONS

This dissertation studied the use of CT ΔΣ modulators in future multi-standard and SDR receivers along two main flow lines; particularly, the sensitivity to OOB blockers appearing at the ADC input and sensitivity to PWJ in DAC sampling clock. The proposed research analysis and solutions promise significant improvement in power budgeting and are feasible for low-cost silicon-based technologies.

The sensitivity of single-bit CT ΔΣ modulators to OOB has been studied and shown to exhibit a quantizer sampling jitter-like effect especially in case of weak in-band signals. The adopted argument has been demonstrated through system-level simulations by examining the performance of a fifth-order single-bit ΔΣ modulator in a CRFB structure in presence of OOB blockers. A reduction in the achievable SNDR, that can be as large as 10 dB when applying a 0 dBFS OOB blocker tone along with a weak desired tone, has been observed. The premise adopted in the argument and verified by the simulation results suggests that the performance of single-bit CT ΔΣ modulator is sensitive to OOB and shows noticeable degradation in presence of sufficently high OOB signals.

The sensitivity of ΔΣ modulators with CT loop filters to DAC PWJ in presence of blockers has been investigated in details. The developed analysis covered the commonly used DAC types including SI RZ, SI NRZ, and SCR with exponentially-decaying waveform. It has been shown that for all types of multi-bit DACs, the IBJN induced by a blocker signal increases proportionally with the power of the blocker

component in the feedback path and also varies periodically with the blocker frequency through a squared sinusoidal factor for multi-bit NRZ DACs. In contrast, single-bit ΔΣ modulators are shown to be completely robust to blocker induced IBJN since the signal swing in their feedback waveforms is independent of the quantizer input signal and hence the blocker component power. In addition to difference in types of quantizers, comparison between different classes of ΔΣ modulators also covered different loop filter structures. According to results obtained by simulations, the IBJN due to blockers dominates the total IBN for feedforward multi-bit ΔΣ modulators and can increase the total IBN by 10 dB. However, for a given blocker power at the ADC input, multi-bit feedback ΔΣ modulators show more robustness to PWJ than their feedforward counterparts, owing to their stronger low-pass filtering characteristic.

The limitations on the achievable performance caused by loop filter nonlinearities in presence of large OOB blockers were discussed and it has been shown that, in presence of a $6\ dBFS$ OOB blocker, noise folding at the first integrator stage, with $IIP_3 = 23\ dBFS$, can significantly deteriorate the ADC sensitivity by 30 dB, turning weak desired signals undetectable. Furthermore, in presence of large OOB blockers, the noise folding problem raises the IIP_3 requirement on the first stage in the loop filter to extremely high values ($\sim 39\ dBFS$). A potential solution is proposed to mitigate the sensitivity to noise folding through current-mode integration at the ADC input stage.

A hybrid CS-SCR DAC solution, based on feedforward spectral shaping for the jitter induced error using a NRZ rectangular waveform CS DAC and SC DAC

combination, has been proposed. The new technique is shown to achieve high robustness to DAC PWJ without requiring faster settling or higher GBW in the op-amp used in the load circuit. Furthermore, this proposed hybrid CS-SCR DAC maintains the inherent anti-aliasing capability of CT ΔΣ modulators. The potential of the proposed hybrid DAC solution is demonstrated on silicon through a 90nm CMOS prototype chip. The jitter-tolerant DAC chip provided attenuation for in-band jitter induced noise by 26.7dB and in-band DAC noise by 5dB, compared to conventional CS DAC. The hybrid DAC consumes 719µwatts from 1.3V supply.

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