DESIGN OF A 20MHZ TRANSIMPEDANCE LOW-PASS FILTER WITH AN ADAPTED 3RD ORDER INVERSE CHEBYSHEV RESPONSE

A Thesis

by

EMMANUEL OSEI BOAKYE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2012

Major Subject: Electrical Engineering

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ABSTRACT

Design of a 20MHz Transimpedance Low-pass Filter with an Adapted 3rd Order Inverse Chebyshev Response. (August 2012)

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Chair of Advisory Committee: Dr. Aydin Karsilayan

In Multi-Standard receivers, multiple radios co-exist in close proximity. A desired signal can be accompanied by significantly stronger out-of band interferers or blockers, which can severely degrade a receiver's sensitivity through gain compression of the blocks in the receiver chain. This work presents a new Transimpedance Amplifier (TIA) low-pass filter architecture which seeks to solve the out-of-band blocker problem of the existing architectures.

A higher order filtering is embedded within the TIA in the form of an active feedback to provide more attenuation to out-of-band blockers. The active feedback circuitry feeds back an equivalent amount of current to the input node to cancel out incoming out-of-band blockers while maintaining an acceptable voltage swing at the output of the TIA. The proposed TIA filter has a channel bandwidth of 20MHz, and can processes interferers of ±10mA fully differential without saturating the opamps. The maximum single ended voltage swing at all the nodes is ±200mV.

All the circuits were designed in IBM 180nm CMOS process with a supply voltage of 1.8V.

DEDICATION

To my parents, Eric Oppong-Bediako and Victoria Mensah-Oppong

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1 INTRODUCTION

1.1 Background

In today's wireless industry, there is a growing interest in Multi-Standard receivers. There are three main groups of communication standards: network, cellular and satellite. The network communication standards include WLAN (Wireless Local Area Network), Bluetooth, Wi-Fi, LTE (Long Term Evolution) and UWB (Ultra Wide Band). The cellular communication standards include Global System for Mobile communications (GSM), General Packet Radio Service (GPRS) and WCDMA (Wideband Code Division Multiple Access). The satellite communication standards include GPS (Global Positioning System). The number of standards is continuously increasing. The motivation now is to design systems which support as many standards as possible.

It is a challenge to design a receiver with a wide range of reconfigurability for the above mentioned standards, especially when two or more standards operate concurrently at a given time. In [1], a reconfigurable RF front end based on narrow-band tunable Low Noise Amplifiers (LNAs) is presented. With such an architecture, the complexity and occupied chip area of the receiver increase as the number of supported standards increases. An alternate solution is a single broadband receiver which supports any of the

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standards. To make such receiver architecture more attractive on the market, the solutions presented should be cost effective. The most conventional receiver, heterodyne architecture, requires a bulky RF filter to suppress the unwanted image signal from down converting to IF. The RF filters must have a high quality factor and can only be implemented with discrete passive components (capacitor and inductors). These RF filters are very expensive [2].

The cost of the receiver can be reduced by full integration, implementing the radios as silicon on chip (SoC), sharing resources and removing the expensive bulky SAW filters from the RF section of the receiver [3, 4]. The direct conversion or direct conversion architecture provides the most cost effective solution for the implementation of a fully integrated Multi-Standard Radio Receiver [5],[6]

In direct conversion receivers, the desired signal is converted directly to baseband, where a fully integrable low-pass filter can be used to filter out the unwanted signals. However, because the signal is converted directly to DC, the system becomes susceptible to flicker noise. Generally, the major source of flicker noise in the receiver front end comes from the mixer switching pair but as demonstrated in [7] and [8] , a current driven passive mixer can drastically reduce the flicker noise in the switching devices. No DC current flows through a current passive mixer, so its flicker noise contribution is minimal. Shown in Figure 1 is a fully differential current-mode passive mixer.

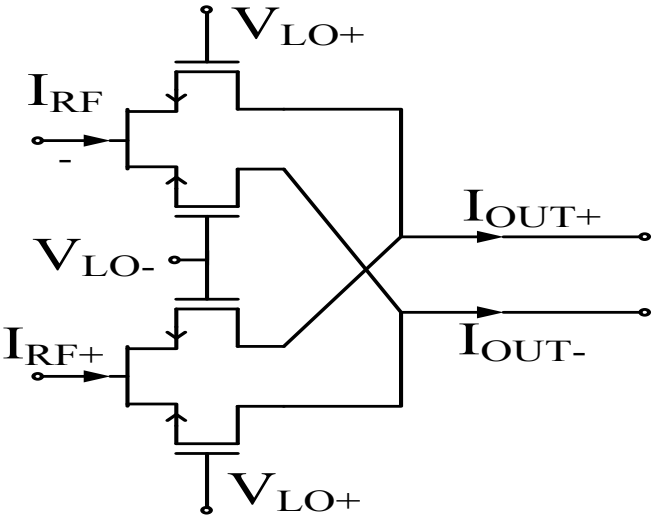

Figure 1 Fully different current driven mixer

The receiver block diagram for a direct conversion receiver is shown in Figure 2. It comprises of a Low Noise transconductance Amplifier (LNTA) which converts the received RF signal to current, a current-mode passive mixer which drives a low impedance node, TIA low-pass filter, to convert the down converted current to voltage and also to filter out all the unwanted signal components, and an Analog-to-Digital Converter (ADC) to process and convert the signal from analog to digital domain. The focus of this thesis is the TIA low-pass filter block in the receiver chain.

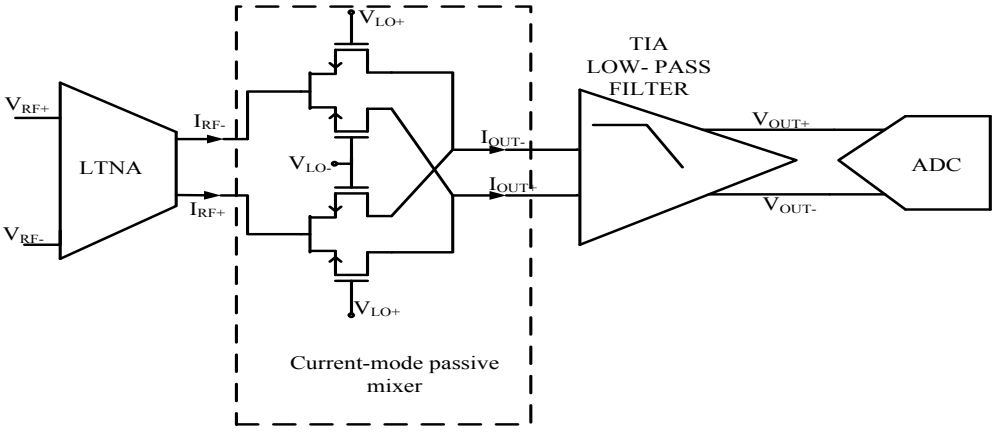

Figure 2 Direct conversion receiver with current driven passive mixer

Generally, the TIA used in direct conversion receivers consist of an opamp and feedback networks. Most commonly the TIA is implemented with a first-order attenuation [9],[10]. The transistors in the current driven passive mixer operate in the triode region. In order to preserve their linearity, the drain to source voltage for all the transistors should always be much lower than their corresponding over-drive voltage. The output voltage swing of the mixer is always small because the TIA input impedance is low due to the shunt feedback to its input.

In Multi-Standard receivers, multiple radios exist in close proximity. A desired signal can be accompanied by interferers. The impact of an interferer on a system depends on its magnitude and location. In a receiver chain, there is always a high probability of interferers downconverting to frequencies near the desired signal bandwidth, or the cross products of two or more interferers falling close to or in the signal bandwidth. These

unwanted signals may experience the same process the desired signal goes through, corrupting the required information. The problem worsens if the interferers are significantly stronger because their cross product terms which fall in the band of interest can easily saturate the blocks jeopardizing all forms of communication. Also a strong interferer can severely degrade receiver's sensitivity through gain compression. Such a phenomenon can even happen when the interferer is at frequencies far from the band of interest.

In [9] and [10], the TIA uses a single pole RC circuit to filter out the interferers. First-order filtering may not be adequate especially in the presence of strong interferers. The authors' assumption is that the blockers are accommodated by a high dynamic range ADC, which in effect increases power consumption, cost and complexity of the ADC. In [11], a single pole TIA cascaded with a higher order filter is proposed. Although this may help suppress the blockers to the ADC, the large signal performance of the first stage which is the TIA does not change. Any strong interferer can easily saturate the first stage, desensitizing the whole receiver chain.

In this thesis, a TIA with an adapted 3rd order lowpass inverse Chebyshev response is presented. Extra circuitry is added to the feedback of the existing first-order TIA to provide more attenuation to the interferers. The proposed TIA still maintains the desirable low impedance property while providing better out-of-band linearity performance. Also, with the proposed TIA, the oversampling ratio and resolution of the

ADC can be relaxed; consequently, cost, complexity and power consumption of the ADC can be reduced. The proposed TIA handles ±5mA interferer at 60MHz and beyond without any saturation.

1.2 Thesis Organization

The thesis has six sections. Section 1 is the introduction. It discusses the various communication standards, conventional receiver architectures and general issues with direct conversion receivers. Existing solutions are discussed and the concept of the proposed TIA is introduced.

Section 2 reviews the general design metrics for TIAs and their impact on the overall system performance. Some system level issues in the design of TIAs are also explained.

Section 3 details the concept of the proposed TIA filter and the bottlenecks of the design. The transfer function and the circuit implementation of the various blocks are presented. The various constraints that set the component values for the blocks are discussed.

In Section 4, the main considerations in the transistor level design for the proposed TIA are discussed. The optimization process in determining the Gain-Bandwidth products of the opamps is also analyzed. System level simulations with a novel V-I differentiator are presented and its linearity and noise impact on the whole system are also discussed. Also the layout for the proposed TIA is introduced.

In Section 5, the schematic and post-layout simulation results of the proposed TIA low-pass filter are presented. The out-of band linearity of the proposed filter is presented which shows a considerable improvement of linearity over the existing architectures

Conclusions and possible future work are presented in Section 6.

2 GENERAL DESIGN CONSIDERATION FOR A TRANSIMPEDANCE FILTER

Transimpedance amplifier (TIA) is an important active element in analog integrated circuits and systems. It basically transforms current signals to voltage signals. In most receivers, it is used at the output of a current mode down–conversion mixer to convert the current signals to voltage signals. In this section the various design parameters for TIA are briefly discussed.

2.1 Gain

The conventional TIA architecture is shown in Figure 3. The gain is defined as the ratio of the output voltage (V_{OUT}) to the input current (I_{IN}). For example, a TIA with a gain of 60dB (1000) produces a change of 1mV at the output in response to 1μA of current at its input.

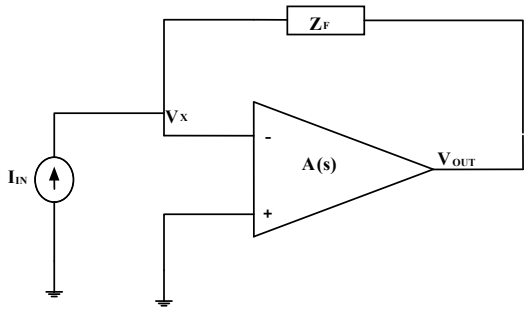

Figure 3 The basic transimpedance amplifier

Using nodal analysis at V_X, the gain for Figure 3 can be expressed as

$$\frac{T}{I_I} \quad \frac{A(s)}{1 \quad A(s)} \quad F \tag{2-1}$$

If $|A(j\omega)| >> 1$, the TIA gain reduces to

$$\frac{T}{I_I} \approx \quad F \tag{2-2}$$

For large values of the opamp gain, the transimpedance gain is simply the feedback impedance. Most often, Z_F is a combination of passive elements and its value is well defined. As a result, the sensitivity of the output voltage to variations in A(s) is very minimal. The unit for the gain can easily be deduced from (2-2) as ohms (Ω).

In most direct conversion receivers, Z_F is a parallel combination of a resistor and a capacitor. Using (2-2) , the gain for Figure 4 is given as:

$$\frac{T}{I_I} \quad \frac{}{1 \quad s \quad C} \tag{2-3}$$

The above equation gives first-order attenuation after the corner frequency (bandwidth) 1/RC.

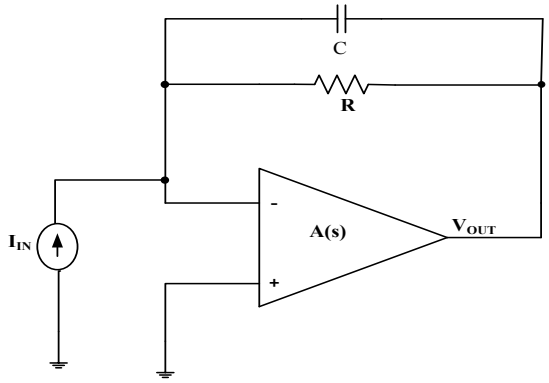

Figure 4 Single pole RC TIA filter

2.2 Input Impedance

One desirable property of a TIA is the low input impedance it offers to mixers in the receiver chain. This attribute helps to preserve the linearity of the mixer. Considering Figure 3, the input current can be defined as

$$I_I \quad \frac{(1 \ A(s))}{F} \tag{2-4}$$

which can rearranged as

$$I \quad \frac{F}{I_I} \quad \frac{F}{1 \ A(s)} \tag{2-5}$$

As can be observed, for large values of |A (jω)|, the input impedance is very small.

Again considering Figure 4, its input impedance can be found by replacing Z_F in (2-5) with $\| {}^{1}/_{sC}$, resulting in

$$I \quad \frac{}{(1 \ s \ C)(1 \ A(s))} \tag{2-6}$$

For instance, with 1000Ω and C 7.9pF, the DC gain and bandwidth for Figure 4 are 1000 (60dB) and 20MHz, respectively. Assuming the gain for the opamp is 1000 (60dB) and with no frequency dependency, (2-6) becomes

$$I \quad \frac{0.999}{1 \;\; 7.9 \times 10^{-9}\ \mathrm{s}} \qquad (2\text{-}7)$$

The above equation exhibits a first-order low-pass response. At low frequencies, the input impedance is equal to 0.999 Ω, and at frequencies higher than the bandwidth, the input impedance starts to decrease as shown in Figure 5.

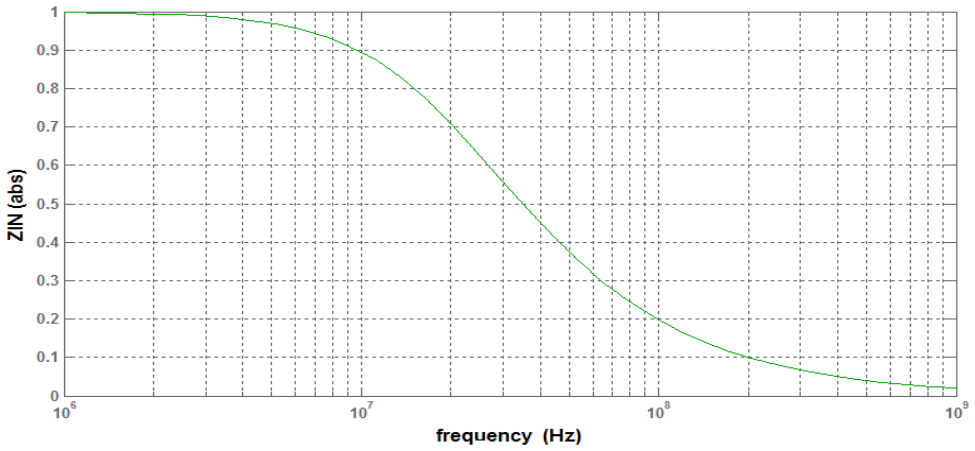

Figure 5 Input impedance of first-order TIA

2.3 Effect Of Finite Gain-Bandwidth Product (GBW) Of An Opamp On System Performance

As the name suggests, the gain-bandwidth product is defined as the product of the DC gain and bandwidth of the opamp. In reality, opamps have finite gain with poles and

zeros. To simplify the analysis, the opamp is assumed to have a single pole with the transfer function given as

$$A(s) = \frac{A_0}{1 \quad \frac{s}{\omega_{dB}}} \tag{2-8}$$

Equation (2-8) can be rewritten as

$$A(s) \quad \frac{A_0 \omega_{dB}}{s \quad \omega_{dB}} \tag{2-9}$$

The Gain-Bandwidth Product from the definition is given as

$$GB \qquad A_0 \omega_{dB} \tag{2-10}$$

Substituting (2-10) into (2-9) gives

$$A(s) \quad \frac{GB}{s \quad \omega_{dB}} \tag{2-11}$$

The impacts of the GBW of the opamp on the overall system performance are discussed below.

2.3.1 Gain

With the gain of the opamp defined in terms of GBW and the bandwidth as in (2-11), (2-1) can now be written as

$$\frac{out}{I_{in}} \qquad \frac{GB}{GB \quad \omega_{dB} \quad s} \quad f \tag{2-12}$$

Using the first-order transimpedance filter shown in Figure 4 as an example, its transfer function using (2-12) is given as

$$\frac{out}{I_{in}} \quad \frac{\left(1 \quad \frac{1}{A_0}\right)}{1 \quad \frac{s}{GB \quad \omega_{dB}}}\left(\frac{}{1 \quad s \quad C}\right) \tag{2-13}$$

$A_0 \gg 1$, therefore (2-13) can be reduced to

$$\frac{out}{I_{in}} \quad \frac{1}{1 \quad \frac{s}{GB \quad \omega_{dB}}}\left(\frac{}{1 \quad s \quad C}\right) \tag{2-14}$$

Comparing (2-3) and (2-14), it can be seen that (2-14) has an additional pole, which changes the -20db/decade roll-off from the feedback impedance to -40db/decade. This additional pole adds more phase to the loop, which potentially could introduce stability issues. The situation becomes worse in reality because an opamp usually has more than one pole.

2.3.2 Input impedance

The input impedance equation shown in (2-5) has the gain of the opamp as a variable. Substituting (2-11) into (2-5) gives

$$_{I}(s) \quad \frac{}{A_0 \quad 1} \quad \frac{(s \, \omega_{dB} \quad 1)}{(1 \quad s \quad C)(s\,(w_{dB} \quad GB \quad) \quad 1)} \tag{2-15}$$

From the above equation,

$$\text{Impedance at DC} = \frac{R}{A_0 + 1} \tag{2-16}$$

$$_{1} \quad \frac{1}{C} \tag{2-17}$$

$$_{2} \quad GB \quad \omega_{dB} \tag{2-18}$$

$$_{1} \quad \omega_{dB} \tag{2-19}$$

The position of P_1 and Z_1 are dependent on the bandwidth specification and the dominant pole of the opamp, respectively. The second pole P_2 is generally greater than P_1 and Z_1. $Z_{IN}(s)$ can take two forms; $P_1<Z_1$, shown in Figure 6 and $Z_1<P_1$, shown in Figure 7.

For Figure 6, the input impedance function stays flat at the DC value of Z_{IN} until it encounters P_1. From this point, the Z_{IN} decreases with a slope of -20db/decade. This effect is cancelled as soon as the input impedance function hits the zero, Z_1. It remains flat until the function encounters P_2. From here on, Z_{IN} again decreases with a slope of -20dB/decade.

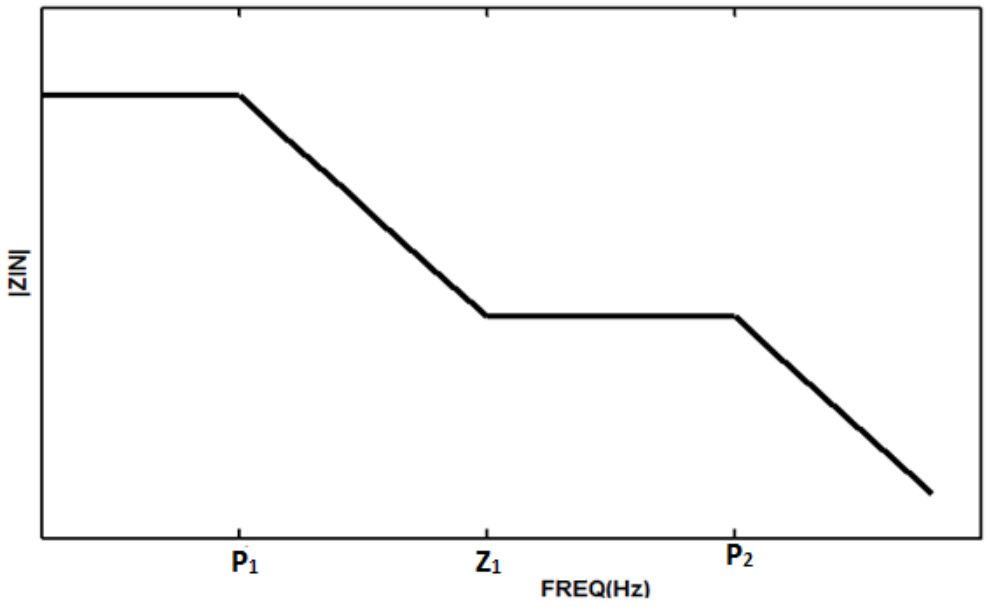

Figure 6 Input impedance function for $P_1<Z_1$

In Figure 7, Z_{IN} starts at its DC value but unlike Figure 6 , it rises with a positive slope of 20db/decade after the zero Z_1. $Z_{IN}(s)$ is flattened as soon as the input impedance function hits the pole P_1. Once Z_{IN} reaches P_2, it decreases with a roll-off of -20db/decade.

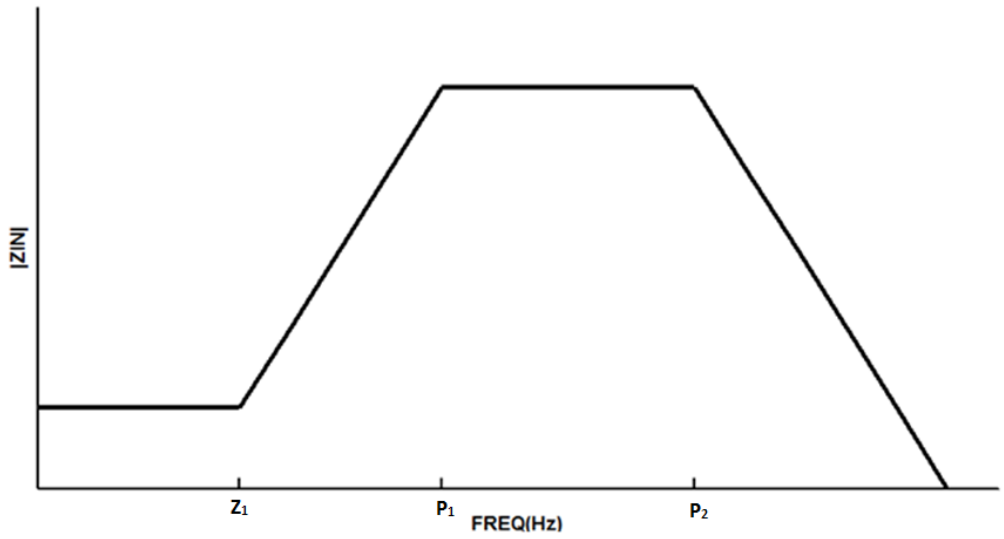

Figure 7 Input impedance transfer with for $Z_1<P_1$

The following deductions can be made from Figure 6 and 7:

(i) For the TIA to offer very low input impedance to the mixer, the gain of the opamp should be as high as possible to reduce the impedance at DC.

(ii) For the same DC gain, the higher the GBW of the opamp, the higher the frequency of Z_1 and the smaller the rise in Z_{IN} before P_1 flattens Z_{IN}.

(iii) The positions of P_1 and Z_1 depend on the bandwidth specification and the dominant pole of the opamp. These two parameters should be placed close to

each other as much as possible by the designer to cancel the input impedance increment as shown in Figure 7.

2.4 Noise

The input referred noise current of the TIA is very crucial to the performance of the overall receiver chain. The minimum noticeable signal depends on the amount of noise produced by the device.

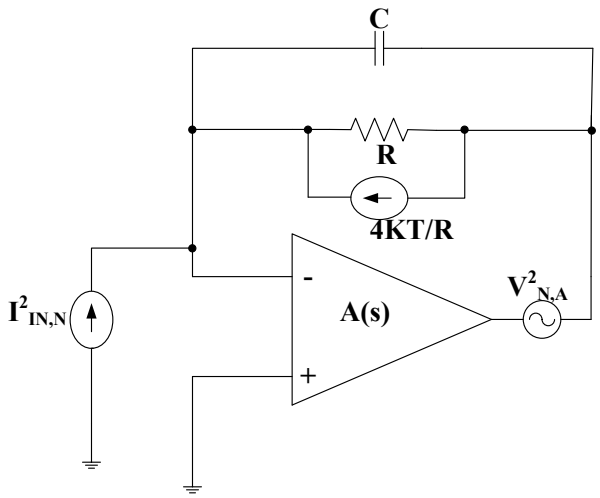

Figure 8 First-order TIA with equivalent noise sources

The total input referred noise current for the first-order TIA filter shown in Figure 8 can be approximated as

$$I^2_{I,} \quad ^2_{,A}\left(\frac{sC \quad 1}{}\right)^2 + \frac{kT}{} \tag{2-20}$$

where k is the Boltzmann constant, T is the temperature in degrees Kelvin and $V^2_{N, A}$ is the output referred noise of the opamp. At low frequencies, the impact of the noise contribution from the opamp is minimized by the high pass filter formed by the resistor and capacitor in the feedback. The main noise source at low frequencies is the feedback resistor. A bigger R contributes less thermal noise to the TIA but increasing this also increases the TIA's DC gain. Therefore, the value of R should be carefully chosen to satisfy both the noise requirement and the filter specifications. At high frequencies the noise from the opamp becomes critical which needs to be considered during design.

2.5 Linearity

Most analog and RF circuits are non-linear in nature. For large signal behavior, linearity of the various blocks in the receiver chain is very important, especially for systems where multiple radios operate in the same band or adjacent bands.

Figure 9 Black box representation of a system

A linear system is basically a system whose output (V_O) is proportional to its input (V_I).

$$= C_1 \quad _I \tag{2-21}$$

The output of a non-linear system can be approximated with polynomials as

$$C_0 \;\; C_1 \quad _I \;\; C_2 \quad _I^2 \;\; C \quad _I \qquad . \tag{2-22}$$

As a result of the non-linearity, the output will have a signal at the input frequency and signals at the harmonics of the input frequency.

There are many interesting phenomena that occur due to the non-linearity nature of a system. Some of the phenomena are cross modulation, gain compression, inter modulation, blocking of desired signal due to strong interferer and desensitization of blocks.

Assuming there are two signal components at the input of Figure 9,

$$_I \quad _1\cos(\omega_1 t) \quad _2\cos(\omega_2 t) \tag{2-23}$$

the output can be approximated as

$$\begin{aligned} o \quad C_0 \;\; C_1((\;\; _1\cos(\omega_1 t) \quad _2\cos(\omega_2 t)) \;\; C_2((\;\; _1\cos(\omega_1 t) \quad _2\cos(\omega_2 t))^2 \\ C \;\; (\;\; _1\cos(\omega_1 t) \quad _2\cos(\omega_2 t)) \end{aligned} \tag{2-24}$$

The square term can be expanded into

$$\frac{C_2}{2}\left[\;\; _1^2(1 \;\; \cos 2\omega_1 t) \quad _2^2(1 \;\; \cos 2\omega_2 t) \quad _1 \;\; _2(\cos(\omega_1 \;\; \omega_2)t \;\; \cos(\omega_1 \;\; \omega_2)t)\right] \tag{2-25}$$

The cubic term can be expanded as

$$C\left[\frac{1}{}(\cos\omega_1 t \cos\omega_1 t) \frac{2}{}(\cos\omega_2 t \cos\omega_2 t)\right. \tag{2-26}$$

$$\left.\left(\frac{2}{2}\left(\frac{\cos\omega_1 t}{2} \frac{\cos(2\omega_2 \omega_1)t}{}\right) \frac{2}{1}\left(\frac{\cos\omega_2 t}{2} \frac{\cos(2\omega_1 \omega_2)t}{}\right)\right)\right]$$

From the above equations, it can be observed that, the output has signals at the harmonics of the input frequencies and cross modulation terms from mixing of the two signal components. The harmonics for ω_1 are at $2\omega_1$ and $3\omega_1$, and the harmonics for ω_2 are at $2\omega_2$ and ω_2. The cross modulation products are at (ω_1 ω_2), ($2\omega_1 \pm \omega_2$) and ($2\omega_2 \pm \omega_1$). These signal components can fall anywhere in the band of interest. For instance, if there are two close undesired interferers, their harmonics may be at high frequencies, but the cross product terms can fall into baseband, which potentially can corrupt the desired signal. Usually in a down conversion receiver chain, a low-pass filter is usually required at the output of the mixer to attenuate the out-of-band interferers, which helps to minimize the impact of harmonics and cross product terms on the desired band.

One significant focus of this work is that the proposed a low-pass TIA filter can achieve high large signal linearity while dealing with interferers in the adjacent bands. The proposed TIA is to be designed to tolerate blockers of ±5mA from 60MHz and beyond.

3 PROPOSED FILTER

This section presents the details of the theory and the design of the proposed TIA filter. Overall system implementation and simulations are also presented. All the system level considerations that affect stability and noise are also discussed.

3.1 Concept

In a low-pass TIA, the feedback impedance is relatively high and constant within the bandwidth, but at frequencies beyond the bandwidth, the feedback impedance reduces. Shown in Figure 10 is a first-order low-pass TIA filter [9] [10].

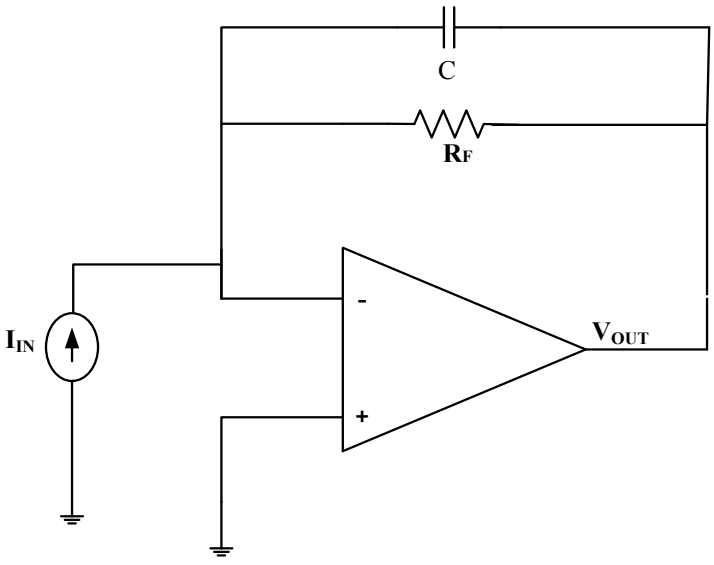

Figure 10 First-order TIA filter

At DC and low frequencies, the capacitor C is an open circuit, so most of the current flows through the resistor, R_F. The output voltage at DC and low frequencies is given as

$$T \quad -\frac{F}{\frac{1}{A_0} \; 1} I_I \qquad -I_I \quad F \tag{3-1}$$

At higher frequencies, C functions as low impedance and shares the input current with R_F. As the frequency increases, the capacitive impedance becomes smaller; therefore the overall feedback impedance also decreases.

The limitation of this topology is that it only provides a first-order rejection. For a filter with a bandwidth of 20MHz and a gain of 60dB, the rejection at 60MHz is just 10dB. So for an input current of 5mA at 60MHz, the output voltage will be 1.6V. In most of the recent technologies with limited supply voltages, such voltage level will easily saturate the TIA.

One way to mitigate the saturation problem is to increase the supply voltages and this technique was employed in [10] . The down side of the technique is that the designer has to utilize extra circuitries to protect the transistors or use more expensive technologies with drain extended devices. Also a single pole filtering will require an ADC with a higher dynamic range and resolution to process the baseband signals. This may increase the complexity and power consumption of the ADC.

Another option is to increase the stop-band rejection of the TIA which relaxes the requirements of the ADC. For instance, for a third order system the attenuation at 60MHz for a TIA with a bandwidth of 20MHz and 60MHz is 28dB. For 5mA input, the output voltage is approximately 0.2V, a manageable voltage level in short channel technologies. So, with an improved stop-band rejection in the low-pass TIA, ADCs with lower resolutions can be used to process the baseband signals to save power.

Figure 11 shows the conceptual idea for the proposed TIA filter. It is similar to the topology in Figure 10 but the capacitor has been replaced with F(s), which is voltage (V_{OUT}) to current (I_X) transfer function given as

$$F(s) \quad \frac{I}{T} \tag{3-2}$$

Under large signal conditions, F(s) feeds back an equivalent amount of current to the input node to cancel out incoming out-of-band blockers while maintaining an acceptable voltage swing at the output of the TIA. F(s) is inactive in the pass-band and only becomes active in the stop-band. The resistor provides the DC gain; F(s) and the resistor together define the bandwidth of the system.

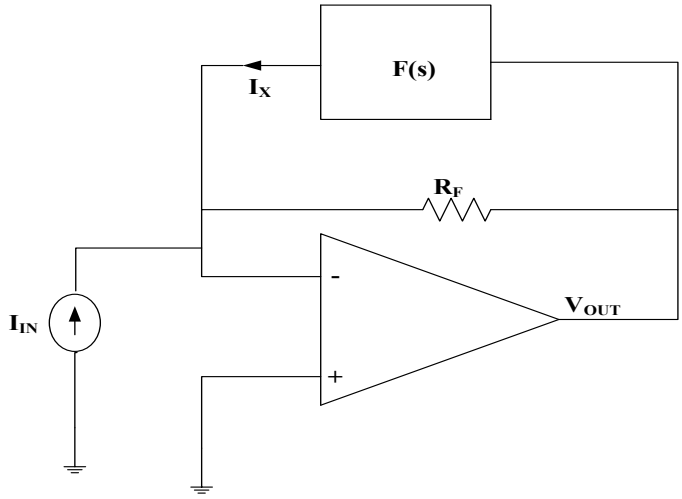

Figure 11 Conceptual TIA architecture

The transfer function for Figure 11 is given as

$$\frac{T(s)}{I_I(s)} \quad T(s) \quad -\frac{F}{1 \quad {}_F F(s)} \tag{3-3}$$

3.2 Filter Transfer Function

An ideal low-pass filter is shown in Figure 12, where ω_p is the pass-band frequency.

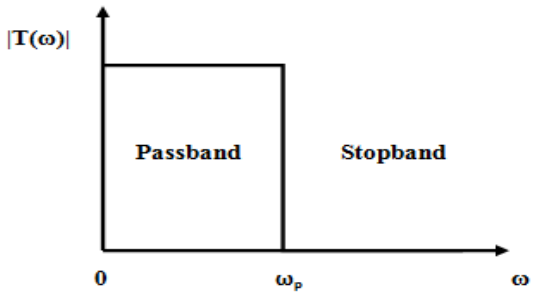

Figure 12 Ideal low-pass filter

In practice, the transfer function in Figure 12 is not realizable, but there are mathematical approximations which can be used to mimic an ideal low-pass filter. The traditional filter approximations are Butterworth, Chebyshev, inverse Chebyshev, and elliptic. Table 1 shows a summary of the pass-band and stop-band characteristics of these approximations.

Table 1 Characteristics of the filter approximations

Approximation	**Pass-band**	**Stop-band**
Butterworth	Flat	Flat
Inverse Chebyshev	Flat	Ripples
Chebyshev	Ripples	Flat
Elliptic	Ripples	Ripples

For the same filter order, Butterworth and Elliptic have the least and the most stop-band attenuation, respectively. Another important parameter is group delay variation, which is a measure of the time delay variations offered by the system to the various signal components. For the same order, elliptic gives the maximum group delay variation while Butterworth gives the minimum group delay variation.

For a given filter order, inverse Chebyshev gives the best compromise in terms of group delay variation and attenuation. Also, inverse Chebyshev approximation has no ripples in the pass-band and offers a sharper roll-off from the pass-band to stop-band. Due to

these reasons, the inverse Chebyshev approximation is used in the design of the proposed TIA filter.

For a transfer function with a gain of 60dB, a bandwidth of 20MHz and a stop-band frequency at 60MHz, the inverse Chebyshev transfer function is given as

$$T(s) \quad \frac{1. \quad 10^{10}s^{2} \quad 2.\ 2 \quad 10^{27}}{s \quad 2.\ 2 \quad 10 \quad s^{2} \quad .\ 19 \quad 10^{1} \quad s \quad 2.\ 2 \quad 10^{2}} \tag{3-4}$$

The magnitude response of T(s) is shown in Figure 13.

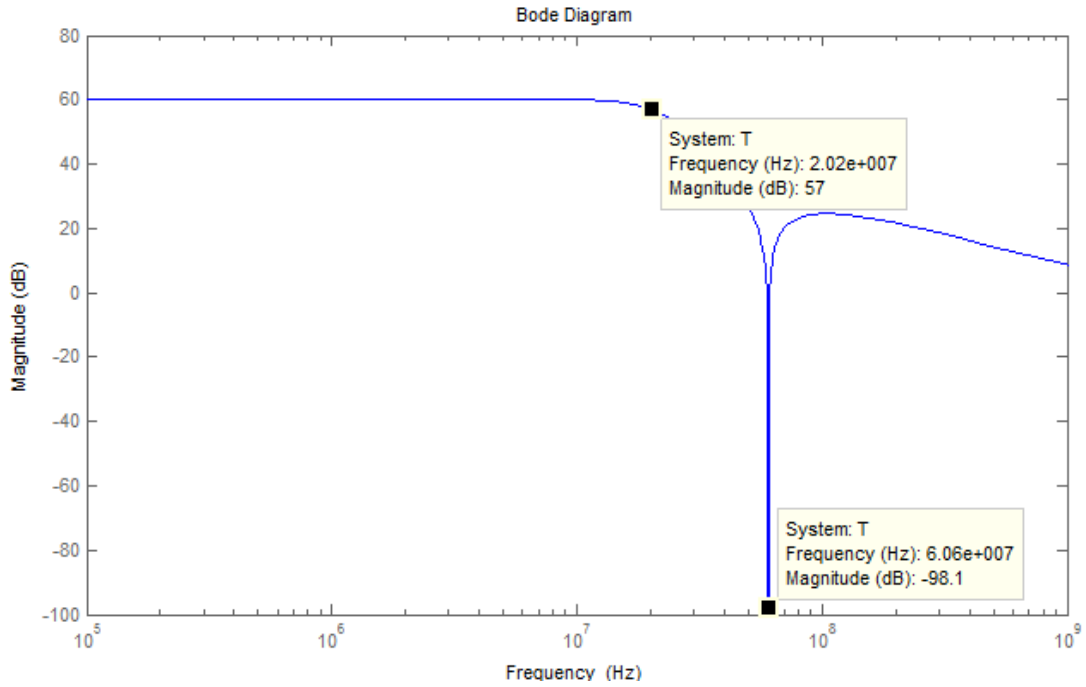

Figure 13 Magnitude response of a 3rd order inverse Chebyshev transfer function

Equation (3-3) can be rearranged as

$$F(s) \quad \frac{1}{T(s)} \quad \frac{1}{F} \tag{3-5}$$

For a gain of 60dB, the value of the resistor is 1000Ω. Substituting R_F 1000Ω and (3-4) into (3-5) gives

$$F(s) \quad \frac{s \quad 2.5 \quad 10 \; s^2 \quad .19 \quad 10^1 \quad s}{1. \quad 10^{10} \; s^2 \quad 2.2 \quad 10^{27}} \tag{3-6}$$

Equation (3-6) can be decomposed into (3-7) as shown in Figure 14.

$$F(s) \quad sC_F \quad B(s)G_m(s) \tag{3-7}$$

where

$$B(s) \quad \frac{}{T} \tag{3-8}$$

$$G_m(s) \quad \frac{I}{} \tag{3-9}$$

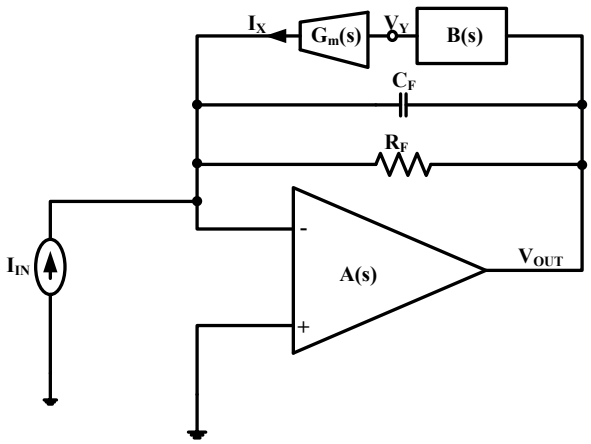

Figure 14 Proposed structure of the TIA

It is possible to implement $G_m(s)$ and B(s) in several ways. However, noise requirement, voltage swing and the maximum signal the system needs to tolerate set the constraints on the circuit implementations and the components value. $G_m(s)$ is a voltage to current differentiator and can be realized with a capacitor, C_{IN}. Substituting $G_m(s) = sC_{IN}$ into (3-7), transfer function for B(s) can be given as

$$B(s) \quad \frac{F(s)\ sC_F}{sC_{IN}} \tag{3-10}$$

$$B(s) \quad \frac{1}{C_{IN}}\left(\frac{s^2 \quad 2.5 \quad 10 \quad s \quad .19 \quad 10^1 \quad C_F\,(1. \quad 10^{10}\,s^2 \quad 2.\ 2 \quad 10^{27})}{1. \quad 10^{10}\,s^2 \quad 2. \quad 2 \quad 10^{27}}\right) \tag{3-11}$$

B(s) has an infinite Q which makes it impractical to realize. The infinite Q introduces the notch shown in Figure 13. A notch at a specific frequency is not crucial to the overall performance of the TIA, because the objective of this work is to design a TIA filter which can handle blockers over a wide frequency range (60MHz and beyond) and not just at a particular frequency. By introducing a Q into (3-11), the transfer function becomes

$$B'(s) \quad \frac{1}{C_I}\left(\frac{s^2 \quad 2.5 \quad 10 \quad s \quad .19 \quad 10^1 \quad C_F\,(1. \quad 10^{10}\,s^2 \quad 2.\ 2 \quad 10^{27})}{1. \quad 10^{10}\,s^2 \quad s\left(\frac{.29 \quad 10^1}{Q}\right) \quad 2.\ 2 \quad 10^{27}}\right) \tag{3-12}$$

Now, with the introduction of Q in B(s), T(s) becomes

$$T(s) \quad \frac{1. \quad 10^{10}s^2 \quad s\left(\frac{.29 \quad 10^1}{Q}\right) \quad 2.\ 2 \quad 10^{27}}{s \quad 2.2 \quad 10 \quad s^2 \quad .19 \quad 10^1 \quad s \quad 2.\ 2 \quad 10^2} \tag{3-13}$$

Figure 15 shows how the magnitude response of T'(s) varies with Q. As shown in Figure 15, a Q of 1.5 provides a rejection of approximately 30dB at 60MHz. An input current of

5mA to such a system translates to 0.158V at the output. The maximum voltage swing set for this work is ±200mV single ended, so a Q of 1.5 is sufficient to provide the rejection the system needs to tolerate the expected blocker magnitude. It will be shown in later in this section of how the Q for the system is selected.

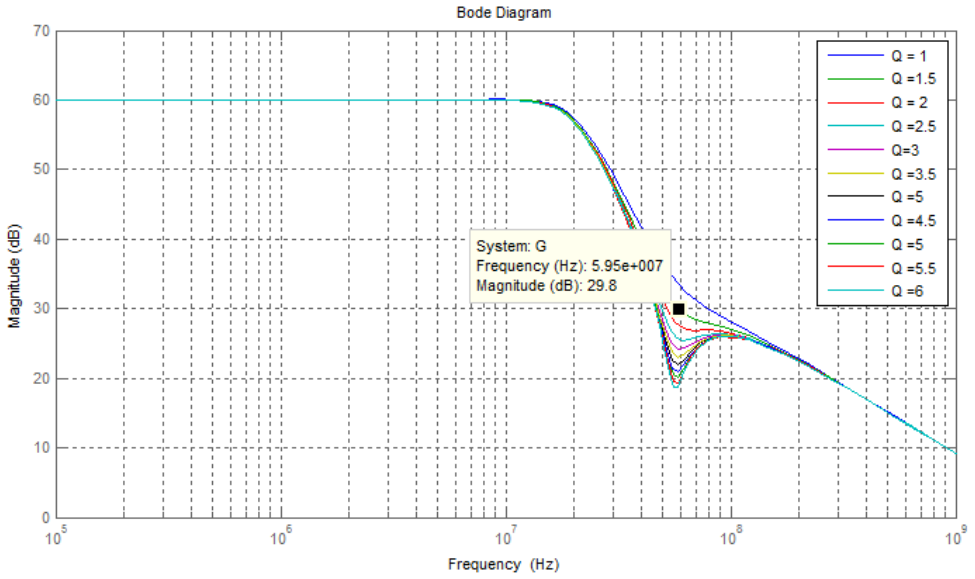

Figure 15 Magnitude response of T'(s) with variation of Q

3.3 Circuit Implementations Of B'(s) And $G_m(s)$

B'(s) is second order transfer function with transmission zeros. B'(s) can be realized using any of the well-known biquad implementations such as Tow Thomas, Ackerberg-Mosberg (shown in Figure 16) and General Impedance Converter. Most of these biquads require at least two opamps which increases the power consumption for the whole system. Biquads such Sallen-Key (shown in Figure 17) and Delyiannis-Friend can be

implemented with a single opamps. However in a fully differential implementation, B'(s) may have to be realized using two identical single ended Sallen-Key or Delyiannis-Friend filters.

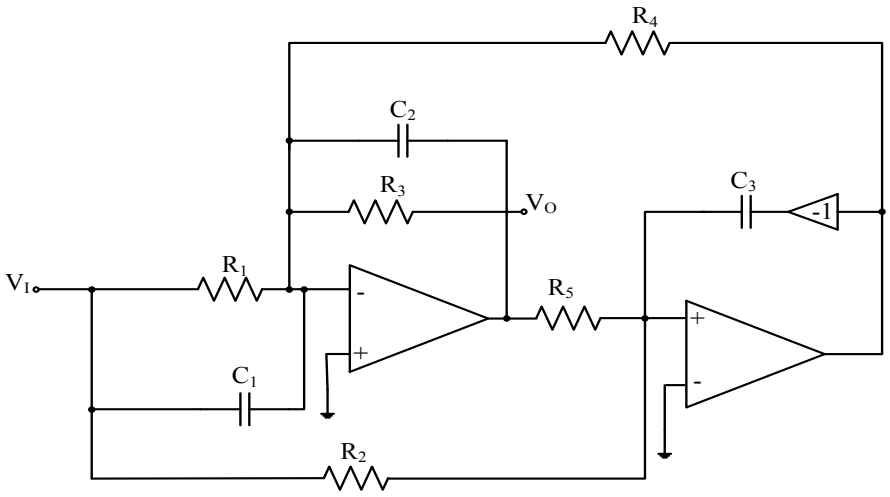

Figure 16 Ackerberg-Mossberg biquad

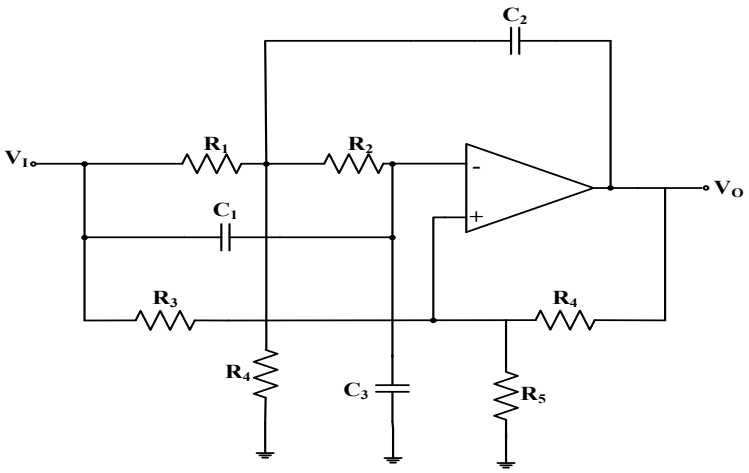

Figure 17 Sallen-Key biquad

In Figure 18, an alternative biquad implementation is presented. The feedback element consists of a T-RC-network connected in parallel with a capacitor. The feedback network creates one real zero and two complex poles. The input element is formed by a parallel combination of a capacitor and a resistor which produces another real zero.

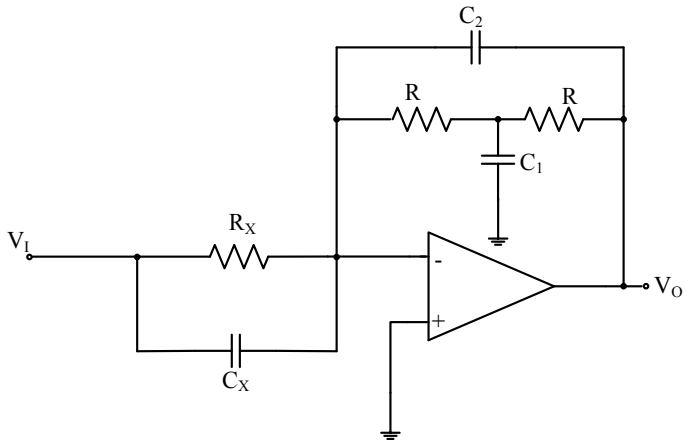

Figure 18 Second order voltage to voltage filter

The transfer function for Figure 18 is given as

$$\frac{o}{I} \quad \frac{(1 \; s \quad C \;)\left(1 \quad \frac{sC_1}{2}\right)}{s^2 \quad {}^2C_1C_2 \quad s2C_2 \quad 1}\left(\frac{2}{\quad}\right) \tag{3-14}$$

The general second order transfer function has the form

$$(s) \quad \frac{{}_1s^2 \quad {}_2s}{\frac{s^2}{\omega_0^2} \quad \frac{s}{Q\omega_0} \quad 1} \tag{3-15}$$

Because the poles are real, (3-15) can be rewritten as

$$(s) \quad \frac{\left(\frac{s}{1} \quad 1\right)\left(\frac{s}{2} \quad 1\right)}{\frac{s^2}{\omega_0^2} \quad \frac{s}{Q\omega_0} \quad 1} \tag{3-16}$$

Comparing (3-14) and (3-16) gives

$$\omega_0 \quad \frac{1}{\sqrt{C_1 C_2}} \tag{3-17}$$

$$Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} \tag{3-18}$$

$$\frac{2}{} \tag{3-19}$$

$$^{1} \quad \frac{1}{C} \tag{3-20}$$

$$^{2} \quad \frac{2}{C_1} \tag{3-21}$$

From algebraic manipulation of equations (3-17) to (3-19) , it can be shown that, the Q for the filter in Figure 18 is given as

$$Q = \frac{\omega_0}{Z_2} \tag{3-22}$$

One thing that is obvious from (3-17), (3-18) and (3-22) is that the Q cannot be independently varied without affecting $\omega_{O.}$ The rest of parameters can be partially adjusted by changing at least two components. For instance, if the gain is to be increased, the value of R_X can be reduced. Although this increases Z_1, it can be adjusted by increasing C_X. The same can be done for the other parameters except for the quality factor which is set by the ratio of C_1 and C_2.

In the order to implement B'(s) with the circuit shown in Figure 18, the zeros of B'(s) have to be real. As can be seen from (3-7), the positions of the zeros depend on the capacitance of C_F. As shown in the plot in Figure 19 , for the zeros to be real the capacitance of C_F should be at least 7.1pF. Any capacitance value of C_F less than 7.1pF makes the zeros of B'(s) complex. In order to give some room for margin of error, C_F=8pF is selected for the synthesis of B'(s) and G_m(s).

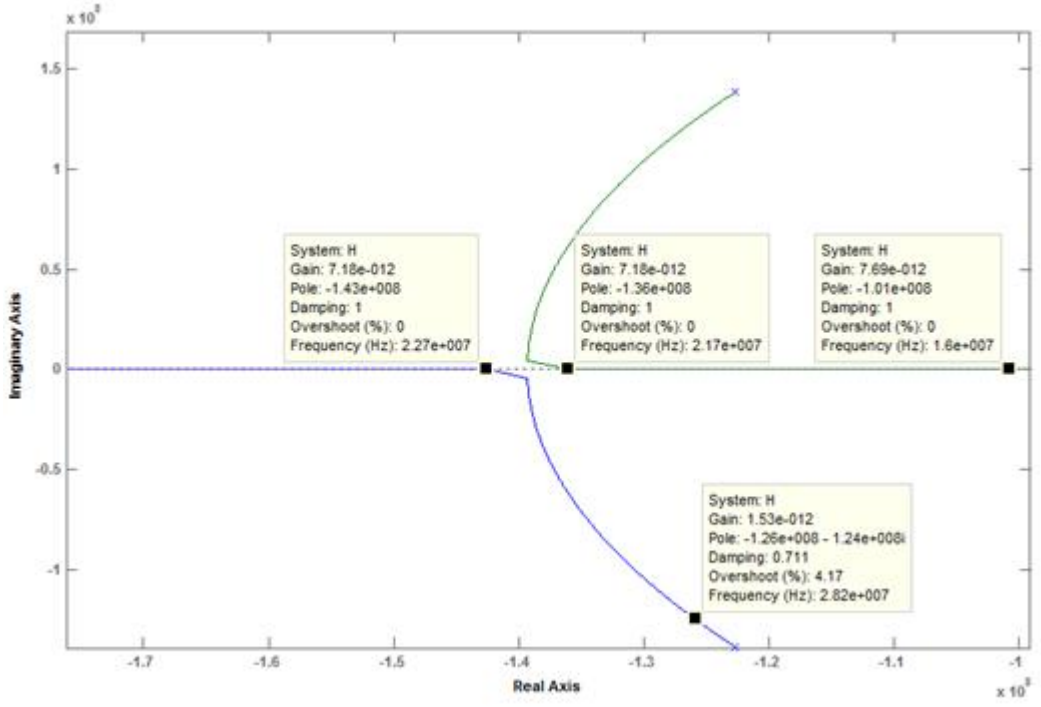

Figure 19 Location of the zeros of B'(s) while sweeping C_F

At high frequencies, the current which is fed back to cancel the blockers mostly comes from $G_m(s)$ and the capacitor C_F. The maximum output voltage swing set for the TIA filter is ± 200mV single-ended, so the current that would be fed back by C_F = 8pF at 60MHz is

$$I = \omega C_F o \quad = 0.\ mA \tag{3-23}$$

Effectively the current expected from $G_m(s)$ to cancel out an interferer of 5mA at 60MHz is 4.4mA and its required capacitance, C_{IN} is given as

$$C_{IN} \quad \frac{I_{MA}}{\omega} = 5 \ . 5\ pF \tag{3-24}$$

V_O 200m and ω 2π* 0M z . In the synthesis, C_{IN} = 60pF is used to allow some margin of error.

$$C_F \qquad 10^{12}s \tag{3-25}$$

$$G_m(s) \ \ sC_I \quad 0 \quad 10^{12}s \tag{3-26}$$

With C_{IN} and C_F selected, B'(s) can now be synthesized by substituting (3-25) and (3-26) into (3-12) to give

$$B(s) \ \frac{0.1059\left(1.101 \ \ 10 \quad s \ \ 1\right)\left(5.20 \ \ 10^{9}\, s \quad 1\right)}{.9\ 1 \ \ 10^{1} \ \ s^2 \ \ s\left(\frac{2. \qquad 10^{9}}{Q}\right) \quad 1} \tag{3-27}$$

3.3.1 Selection of Q for B'(s)

From (3-17) to (3-21), R_X, C_X, C_1 and C_2 can be written in-terms of R as illustrated in (3-33)-(3-36).

$$\frac{2}{} \tag{3-28}$$

$$C \quad \frac{}{2 \quad 1} \tag{3-29}$$

$$C_1 \quad \frac{2}{2} \tag{3-30}$$

$$C_2 \quad \frac{2}{2\omega_0^2} \tag{3-31}$$

Since there are two zeros, there can be two scenarios for the selection of Q. In Figure 20, $_1$ $1/$ C $= 1/5.20\ 10^{-9}$ and $_2$ $2/C_1$ $= 1/1.101\ 10^{-}$, and using (3-33)-(3-36), is swept from 100Ω to 1.5kΩ and the corresponding values for C_X, R_X, C_1 and C_2 are plotted. The Q for B'(s) as demonstrated in (3-22) in this case is 4.15.

It can be seen that, for a given R, the capacitor ratio between C_1 and C_2, and C_1 and C_X are quite huge. For instance, for 500Ω, the corresponding value for C_1, C_2 and C_X are approximately 44pF, 630fF and 560fF, respectively. The ratio between C_1 and C_2 is 70, and the ratio between C_1 and C_X is 78. These capacitance ratios are quite huge, which makes matching between the components very difficult. Also it can be observed that, the required capacitance for the implementation of C_1 is very large, so the overall power consumption and area may be relatively higher for Q = 4.15.

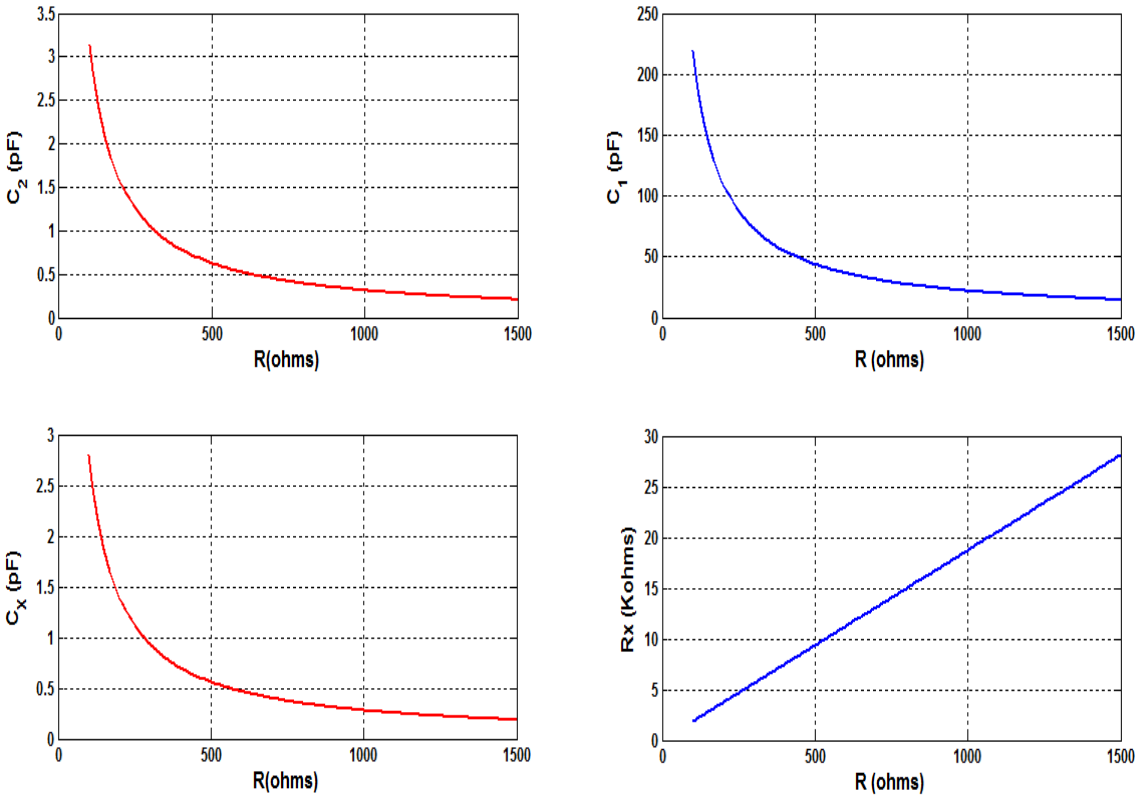

Figure 20 A sweep of R against R_X, C_X, C_1 and C_2 for $Z_1 = 1/R_X C_X = 1/5.2\times10^{-9}$ and $Z_2 = 2/C_1 R = 1/1.101\times10^{-8}$

Figure 21 shows the case for which $_1$ 1/ C = 1/1.101 10^{-} and $_2$ $2/C_1$ = 1/5.20 10^{-9}. The Q in this case as illustrated in (3-22) is 2.

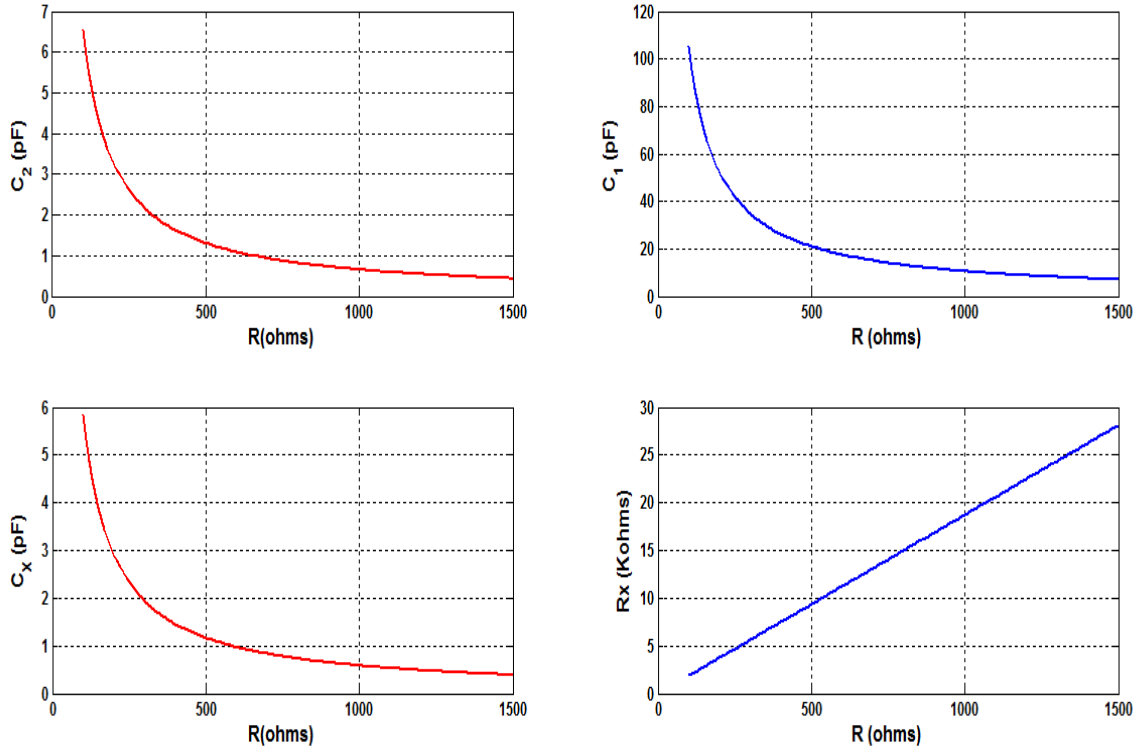

Figure 21 A sweep of R against R_X, C_X, C_1 and C_2 for $Z_1= 1/R_XC_X =1/1.101\times10^{-8}$and $Z_2= 2/C_1R=1/5.2\times10^{-9}$

As can be seen the capacitance ratios for C_1 and C_2, and C_1 and C_X are relatively lower for the case of Q =2. In addition, the corresponding C_1 for a given R are comparatively smaller in this case. Considering all these, the case with Q=2 would be the better option.

3.3.2 Synthesized transfer functions for B'(s) and T'(s)

ith Q selected as 2, B'(s) becomes

$$B(s) \quad \frac{0.1059\left(1.101 \quad 10 \quad s \quad 1\right)\left(5.20 \quad 10^{9} s \quad 1\right)}{.9\,1 \quad 10^{1} \quad s^{2} \quad 1.\ 2 \quad 10^{9} s \quad 1} \qquad (3\text{-}32)$$

After synthesising the various blocks for F(s) , the overall transfer function now becomes

$$T(s) = \frac{1. \quad 10^{10}\, s^2 \quad .1729 \quad 10^{1}\, s \quad 2.\ 2 \quad 10^{27}}{s \quad 2.2 \quad 10 \quad s^2 \quad .19 \quad 10^{1}\, s \quad 2.\ 2 \quad 10^{2}} \tag{3-33}$$

Matlab plots of the magnitude responses of T'(s) and T(s) are shown in Figure 22. The bandwidth for T'(s) has been reduced. However, this can easily be compensated by adjusting the components value as shown in Figure 23. The opamps used for the plot in Figure 23 are ideal and the various components' values are shown in Table 2. As stated earlier, although the notch in T(s) is removed, the modified TIA Transfer function still provides adequate attenuation to out-of-band blockers at 60MHz and beyond.

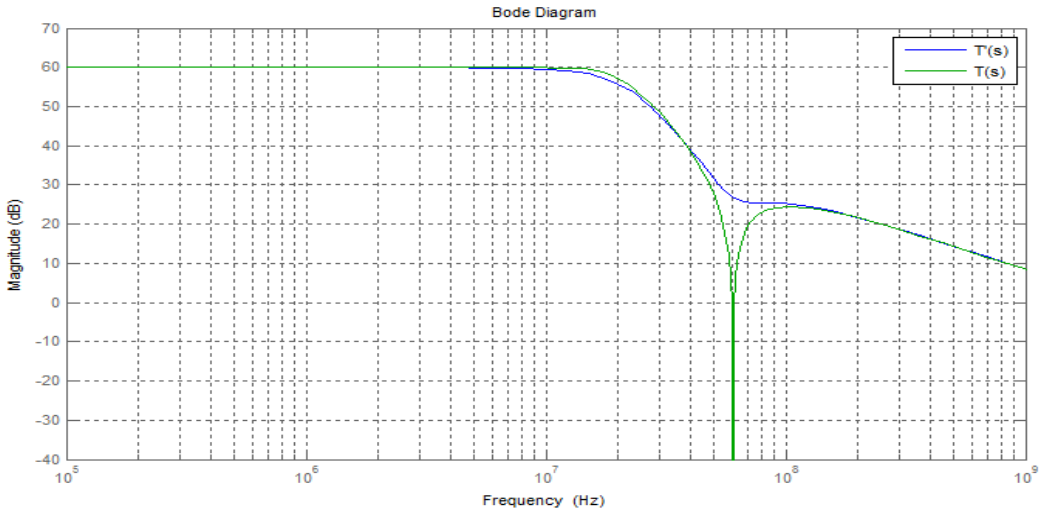

Figure 22 Magnitude response of T(s) and T'(s)

Table 2 Summary of the components with ideal opamps after bandwidth adjustment

Parameter	**Value**
R_F	1 Ω
C_F	8p
C_{IN}	60pF
C_X	0.99pF
R	5 0Ω
R_X	1 .5kΩ
C_1	16pF
C_2	1.14pF

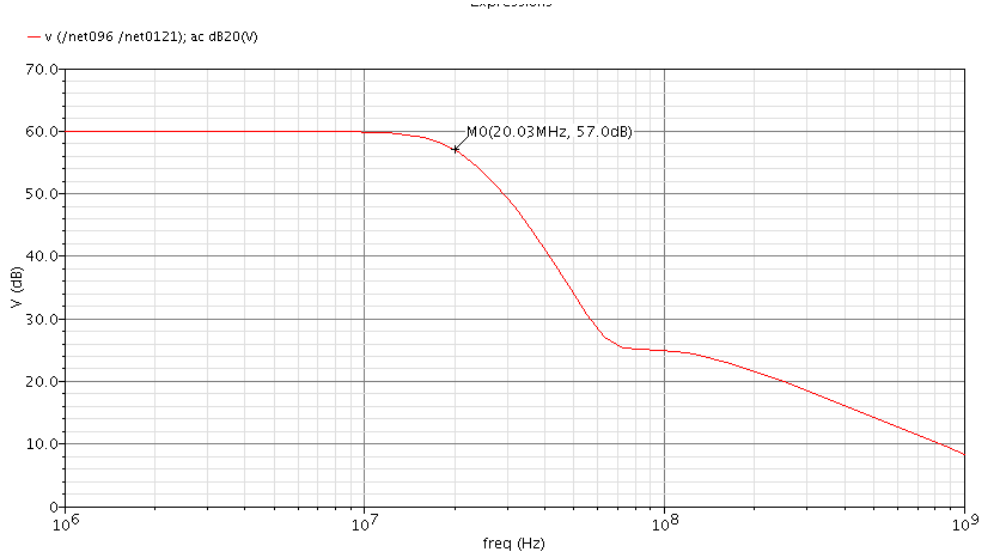

Figure 23 Transfer function of the TIA with ideal opamps after adjusting components' values as given in Table 2

3.3.3 Sensitivity analysis of B(s)

In dealing with the circuit in Figure 18, the sensitivity of the various components needs to be examined. Sensitivity is a measure of how variations in a component value alter the behavior of a circuit. The commonly used definition is the bode sensitivity which is defined as [12]

$$S \quad \frac{d}{d} \tag{3-34}$$

The sensitivity of ω_O, Q, Z_1 and Z_2 to the various passive components are given as

$$S_{C_1}^{\omega_0} \quad S_{C_2}^{\omega_0} \quad \frac{1}{2}, \quad S^{\omega_O} \quad 1 \tag{3-35}$$

$$S_{C_1}^{Q} \quad S_{C_2}^{Q} \quad \frac{1}{2} \tag{3-36}$$

$$S \quad S \quad 1 \tag{3-37}$$

$$S_{R_X}^{Z_1} \quad S_{C_X}^{Z_1} \quad 1 \tag{3-38}$$

$$S_{C_1}^{2} \quad S^{2} \quad 1 \tag{3-39}$$

As can be seen from (3-35) to (3-39), all the sensitivity values are equal to or less than unity. Therefore the circuit can be classified as insensitive to component variations.

4 CIRCUIT OPTIMIZATION AND TRANSISTOR LEVEL DESIGN

The proposed TIA filter is shown in Figure 24. It consists of a second order voltage to voltage filter, a V-I differentiator in the form of a capacitor and a feedback resistor to provide the in band gain. The circuit is realized as a fully differential circuit so the inverter in the feedback will be ignored in the analysis.

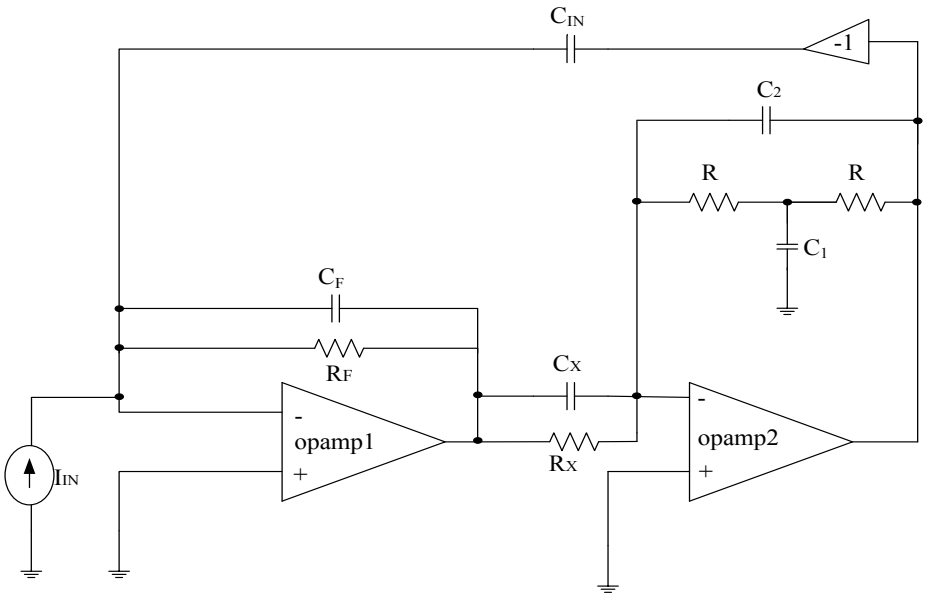

Figure 24 Proposed single ended TIA Filter

4.1 V-I Differentiator

As shown in section 3, to provide a current of ±5mA for the cancellation of the out-of-band blockers, the capacitor C_{IN} needs to be as large as 60pF. C_{IN} is directly coupled to the output of opamp2. Such a high load can introduce a low frequency pole which can

limit the high speed operation of the system. Also to drive such a huge load, the opamp needs to burn a great deal of current to provide an appreciable GBW and slew rate. Another thing is that, a capacitor of such magnitude will require a large chip area.

The value of C_{IN} can be reduced by cascade of a smaller capacitor C_M and a current amplifier with a gain of N as demonstrated in Figure 25. The current amplifier provides low impedance at X for the linear conversion of the voltage V_O to the current I_{IN}.

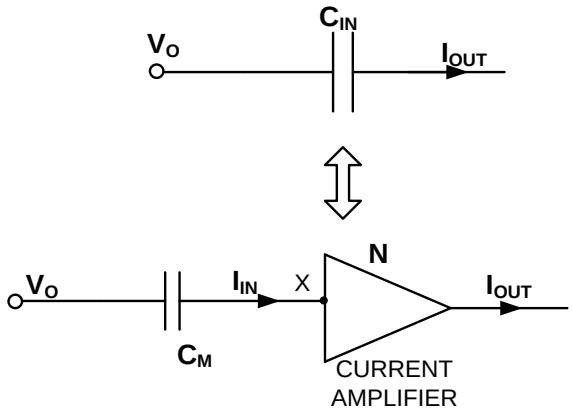

Figure 25 Concept of reduction of C_{IN}

$$\frac{I_T}{I_I} \tag{4-1}$$

$$C_M \quad \frac{C_I}{} \tag{4-2}$$

The circuit in Figure 26 implements a voltage to current high pass filter with a pole at g_{m1}/C_M. The general principle is simple; M_1 provides a low impedance node at X and the

voltage to current differentiation is done by the capacitor. The differentiated current is then mirrored to the input of opamp1. So with such a circuit, C_{IN} can be reduced by a factor of N as given in (4-2) .

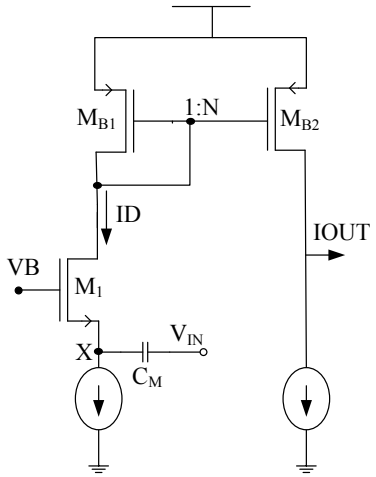

Figure 26 First-order V-I differentiator

The transfer function for Figure 26 is given as

$$\frac{I_T}{I} \quad \frac{s\ C_M}{1\ \frac{sC_M}{g_{m1}}} \tag{4-3}$$

The differentiation is cancelled as soon as (4-3) encounters the pole, g_{m1}/C_{IN}. Therefore, the pole needs to be pushed to a very high frequency. This can be done by reducing the C_M or increasing g_{m1}. Although not shown in (4-3), the current mirror also adds another pole to the transfer function. For a fixed $C_{IN,}$ reducing C_M requires N to increase which will definitely decrease the current mirror pole.

The g_m of M_1 can be increased by increasing the width or the biasing current. The latter requires more current which increases the static power consumption, and the former adds more capacitance at X which limits the bandwidth. Alternatively, g_{m1} can be increased with a gain boosting amplifier as shown in Figure 27.

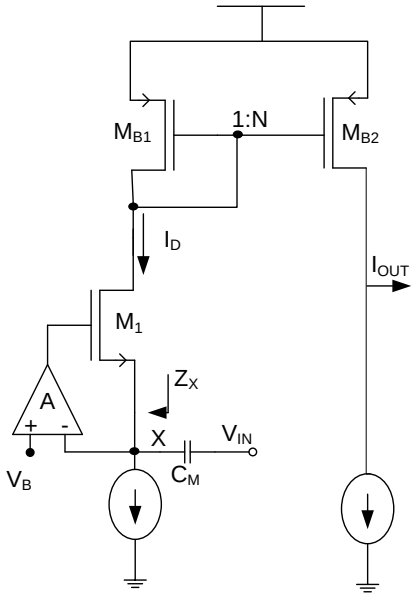

Figure 27 V-I differentiator with gain boosted g_m circuit

Now Z_X in Figure 27 becomes

$$\frac{1}{g_{m1}(A\ \ 1)} \tag{4-4}$$

The impedance is reduced by a factor of (A+1). For an amplifier with a gain of 20dB, the pole in (4-3) is increased by a factor of 11. The frequency of operation is improved

by a decade. Although the amplifier greatly helps mitigate the earlier problem, a local feedback, formed by the amplifier and M_1 could introduce stability issues.

In the Figure 28, a cascade of two g_m stages shown in Figure 26 can be used to create a virtual ground at X. This idea is explored in [13] to implement a second order low-pass current mode biquad.

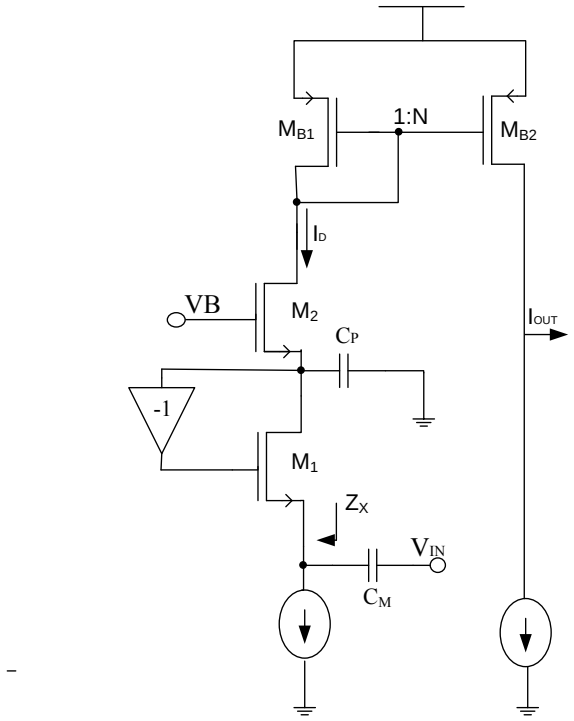

Figure 28 V-I differentiator with cascade of two g_m stages to create a virtual ground

At DC, C_P is an open circuit, so the currents through M_1 and M_2 are equal. If the transconductance of M_1 and M_2 are designed to have the same value, Z_X is zero (virtual

ground) at DC. As the frequency increases, the current in C_P also increases. The technology used for this work is IBM 180nm CMOS, which is a short channel process. C_P is a parasitic capacitor and is usually very small in such process. The current through C_P becomes substantial only at high frequencies. However, over a wide range of frequencies, I_{M1} I_{M2}. With such a topology, the input impedance can be close to zero from DC to very high frequencies without burning much power.

Assuming $g_{m1}=g_{m2}= g_m$, Z_X is given by

$$\frac{sC_P}{g_m^2}\frac{1}{1\ \frac{sC_P}{g_m}} \tag{4-5}$$

Even for frequencies beyond $\omega_P=g_m/C_P$, Z_X is $1/g_m$, which can still be considered small.

The overall voltage to current transfer function for Figure 28 is

$$\frac{I_T}{I}\ \ \frac{s\ C_M}{s^2\left(\frac{C_PC_M}{g_m^2}\right)\ \ \frac{sC_P}{g_m}\ \ 1} \tag{4-6}$$

The desired response is described in the numerator of (4-6) but the equation has two parasitic poles with a center frequency and quality factor given as

$$\omega_o\ \ \frac{g_m}{\sqrt{C_PC_M}} \tag{4-7}$$

$$Q\ \ \sqrt{\frac{C_M}{C}} \tag{4-8}$$

In short cannel technologies, these poles are mostly at high frequencies, so its impact on the system is usually minimal but the designer should be aware of these parasitic poles.

4.1.1 Noise

The noise from the V-I differentiator is directly fed to the input of the TIA, which impact the overall signal to noise ratio. Therefore, the various noise sources for the V-I differentiator shown in Figure 29 need to be investigated.

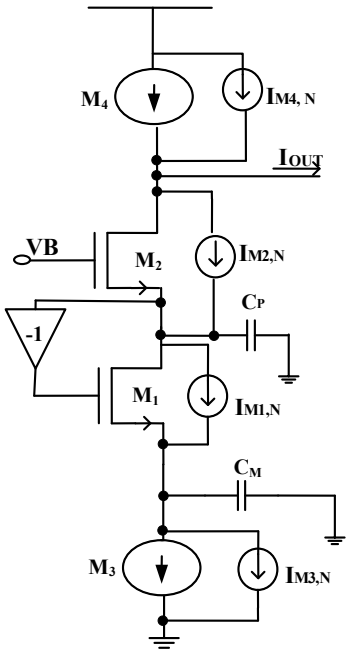

Figure 29 Noise sources for the V-I differentiator

The noise transfer function of M_1 and M_2, M_3 and M_4 are given as

$$\left|\frac{I_T}{I_{M1,}}\right|^2 \quad \left|\frac{sC_M}{s^2\frac{C_PC_M}{g_m^2} \quad \frac{sC}{g_m} \quad 1}\right|^2 \tag{4-9}$$

$$\left|\frac{I_T}{I_{M2,}}\right|^2 = \left|\frac{s^2\frac{C_MC_P}{g_m^2} \quad \frac{s(C_P \; C_M)}{g_m}}{s^2\frac{C_PC_M}{g_m^2} \quad \frac{sC}{g_m} \quad 1}\right|^2 \tag{4-10}$$

$$\left|\frac{I_T}{I_{M\ ,}}\right|^2 = \left|\frac{1}{s^2\frac{C_PC_M}{g_m^2} \quad \frac{sC}{g_m} \quad 1}\right|^2 \tag{4-11}$$

$$\left|\frac{I_T}{I_{M\ ,}}\right|^2 = 1 \tag{4-12}$$

The noise transfer function for M_1 has a band-pass response with the center frequency at ω_o. The bandwidth of the system is far less than ω_o, so most of the noise from M_1 is filtered out in the band of interest. The noise transfer function of M_2 has a high pass characteristic and again most of its noise is filtered in the bandwidth.

The major sources of noise are M_3 and M_4. Noise of M_3 has low-pass characteristic so nothing is filtered out in the band of interest while the noise of M_4 is injected directly to the output. Therefore, the dimensions and over-drive voltages of these transistors should be carefully optimized to reduce their noise impact on the system.

4.1.2 Optimum values for N and C_M

The following design equations can be considered in the design of the V-I differentiator.

$$C_M = \frac{60 \times 10^{-12}}{N} \tag{4-13}$$

$$g_m \quad \omega_0 \sqrt{C \; C_M} \tag{4-14}$$

Equation (4-14) can also be rewritten as

$$g_m \quad \omega_0 \sqrt{\frac{C \quad 0 \quad 10^{12}}{}} \tag{4-15}$$

The total current in Figure 28 is given as

$$I_{total} \quad (1+N) I_d \tag{4-16}$$

The following deductions can be made from the above equations. Increasing the current gain by N:

(i) Increases the power consumption by a factor of 1+N.

(ii) Reduces the current mirror pole by approximately N. A low frequency pole from the V-I differentiator can cause stability issues and also degrade its performance. (4-6) has band pass response with a centre frequency at ω_0. Any pole lower than ω_0 can cancel the differentiating characteristics of (4-6), which is from DC to ω_0. Therefore, the pole from the current mirror needs to be placed at a high frequency.

(iii) Also increases the output current noise of M_3 and M_4 by N^2. As discussed earlier, the main sources of noise in the band of interest are M_3 and M_4. The

noise contribution of these transistors need to be considered in choosing the current gain

(iv) Reduces C_{IN} by a factor N which is the objective of this V-I differentiator.

The fully differential V-I differentiator circuit is shown in Figure 30. Cascode current mirrors are used to provide high output impedance. It also helps to match the drain to source voltage of the transistors to reduce the deviations of the current gain from the desired number.

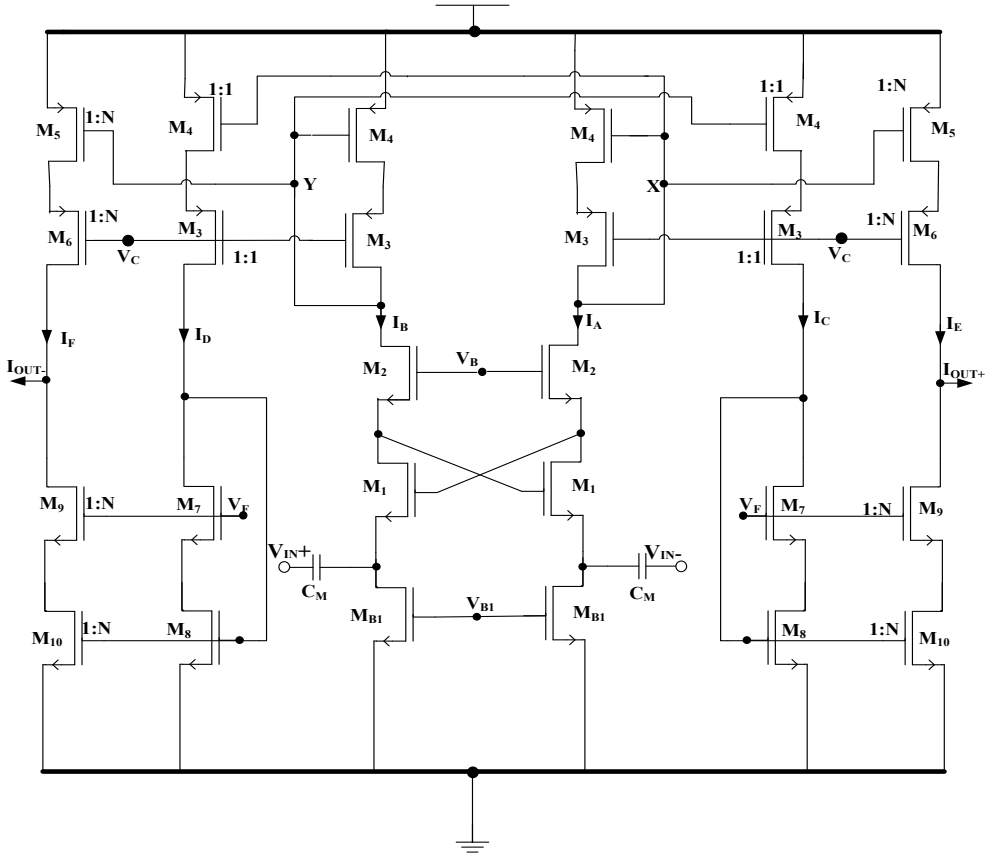

Figure 30 Fully differential V-I differentiator

In Figure 30, I_A is mirrored to I_D and I_E. I_B is also mirrored to I_C and I_F. The current gains to the various branches are specified in Figure 30. I_C and I_D are also mirrored to I_F and I_E, respectively, by a current ratio of N. With this topology, the currents fed to the input terminals of opamp1 are $2\times N\times I_A$ and $2\times N\times I_B$. Figure 31 compares the magnitude response of C_{IN} = 60pF with equivalent response from the V-I differentiator for N = 7,8,10 and 12.

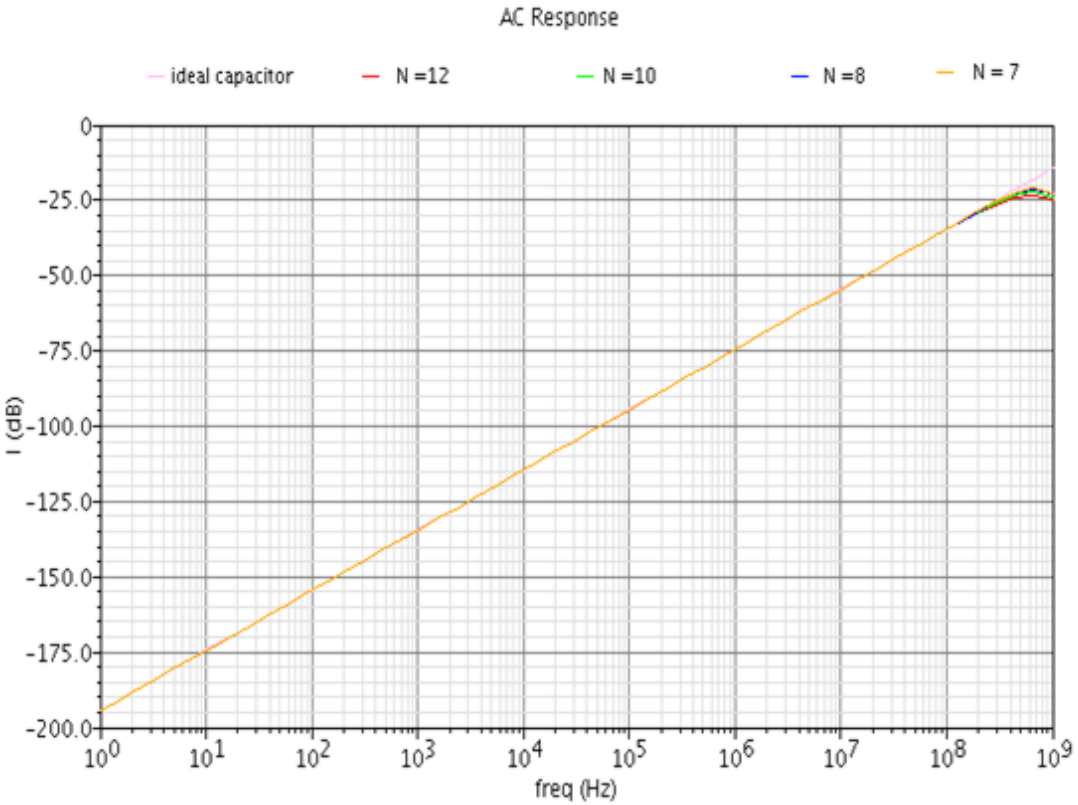

Figure 31 Magnitude responses of a 60pF capacitor and the V-I differentiator with N = 7, 8, 10, 12 from DC to 1GHz

The magnitude response of the V-I differentiator from DC to approximately 600MHz is almost the same as the ideal response. However, beyond 600MHz, the parasitics start to degrade the response. Mostly, TIAs in direct-conversion receivers have a large shunt capacitor at their input node to supplement the bandwidth limitation of the amplifiers. At high frequency most of the signal processing is done by the shunt capacitors, so the effect of these parasitics may not affect the overall system performance.

Table 3 is a summary of the values of current mirror ratio N, transconductance g_m of M_1 and M_2 and the capacitor C_M that were chosen from system level simulations.

Table 3 Summary of optimum parameter values for the design of V-I differentiator

Parameter	**Optimum value**
N	8
C_M	3.75p
g_m	3.67mV/A

4.1.3 Layout of the current amplifier

The layout of the current amplifier is shown in Figure 32. The transistors are designed with multiple fingers to reduce the parasitic capacitance and resistance, and are matched using common centroid technique. With this layout technique, linear processing gradients that affect the transistor's electrical properties are averaged over the matched

devices. M_1 and M_2 are closely matched to ensure they have the same transconductance. As shown in Figure 32, M_1 and M_2 are placed close to each other, and in the same guard ring. The guard ring isolates M_1 and M_2 from the other devices, and putting M_1 and M_2 in close proximity ensures that they generally experience the almost the same device conditions.

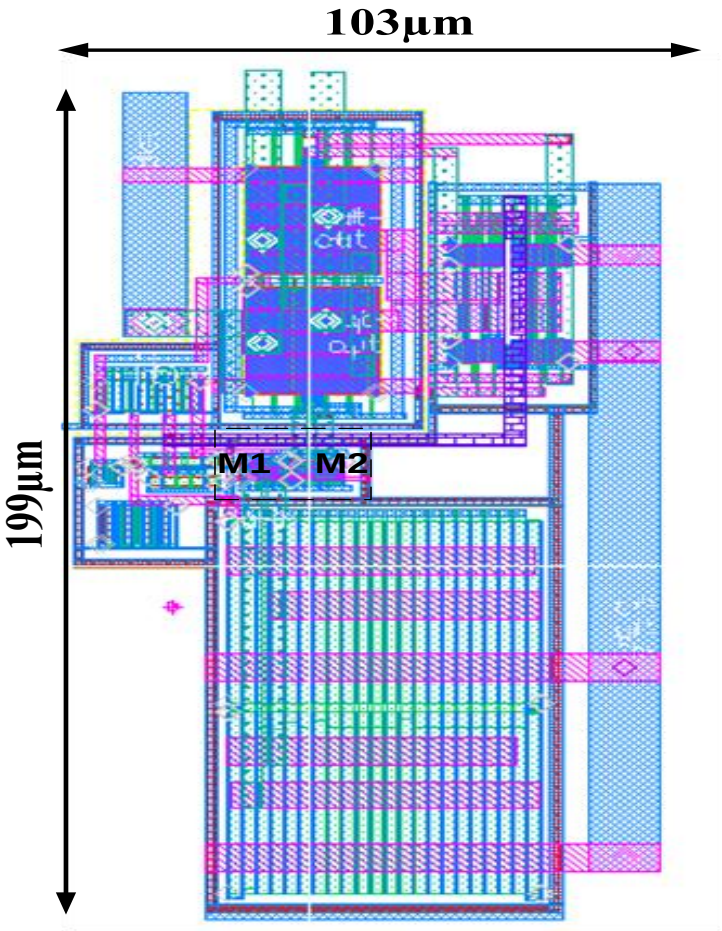

Figure 32 Layout of current amplifier

4.2 Optimum GBW For Opamp1 And Opamp2

In the analysis above, the GBWs for the amplifiers were assumed to be infinite but as discussed in section 2, opamps are band-limited with a finite gain. Also, there is an added circuitry in the feedback which can cause stability issues. System instability may lead to transient ringing or oscillations. Therefore, the best possible GBWs for the opamps which do not affect the stability need to be found. Another important reason to find optimum GBWs for the opamps is to avoid overdesigning the opamps with large power dissipation.

Figure 33 shows the transient response of the TIA to an input current step of 400uA, the GBW of the opamp1 is set to 3GHz (an anticipated achievable GBW in the IBM 180nm process) and the GBW of the opamp2 is varied from 200MHz to 3GHz. All the responses exhibit slight rings before they settle to their final value. The settling time for each case is approximately 70ns. It can be observed that, the overshoot and settling time of the TIA are less sensitive to variations in the GBW of the opamp2.

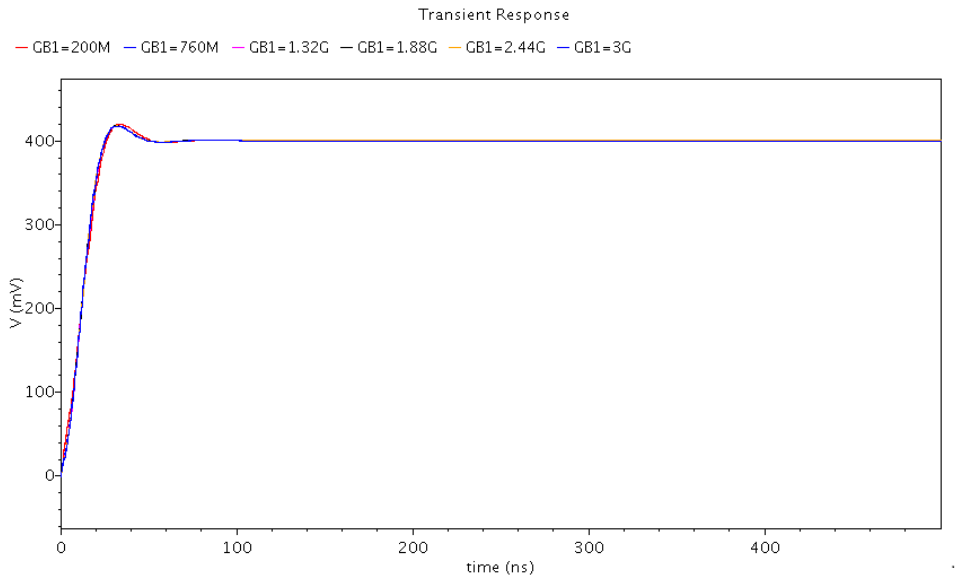

Figure 33 Transient response of the TIA to a current step of 400uA with the GBW of opamp1 set to 3GHz and the GBW of opamp2 varied from 200MHz to 3GHz.

Under the same conditions used for Figure 33, the input impedance to the TIA filter is also plotted in Figure 34. From 1MHz to 50MHz, the input impedance in all the cases is almost the same. Input impedance for GBW =200MHz is slightly lower than the rest by a few mΩs. ow ever, from 55MHz to around 300MHz (thus the critical frequencies in handling the out-of-band blockers), the overall input impedance is reduced for large GBW. Beyond 300MHz, the input impedance peaks to a certain value and then falls. A GBW of 1GHz was selected for opamp2 because it offers a tolerable input impedance value while keeping the power consumption low. A lower GBW can be selected but the designer should be aware of second order effects from the transistor level design, which may cause incessant ringing in the output response.

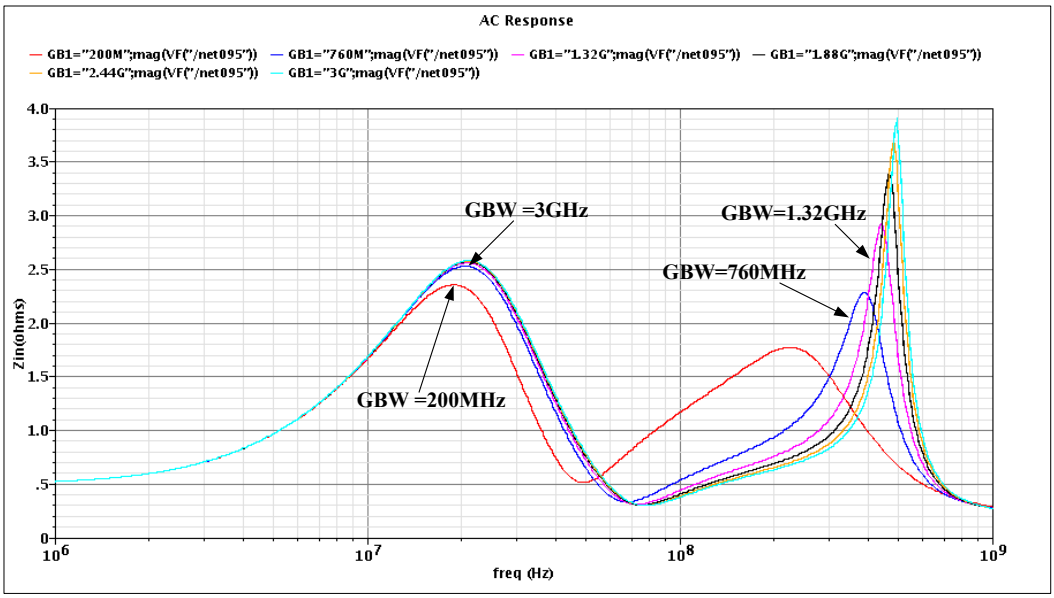

Figure 34 Input impedance of the TIA with the GBW of opamp1 set to 3GHz and the GBW of opamp2 varied from 200MHz to 3GHz.

In Figure 35, the step response of the TIA is shown with GBW of opamp2 is set to 3GHz and the GBW of opamm2 is varied from 200MHz to 3GHz. In all the case there are small transient ringing in the response with GBW = 200MHz and 3GHz exhibiting the most and least ringing, respectively. The overshoot and settling time also decrease with increasing GBW. The settling time for GBW of 200MHz and 3GHz are 240ns and 70ns, respectively.

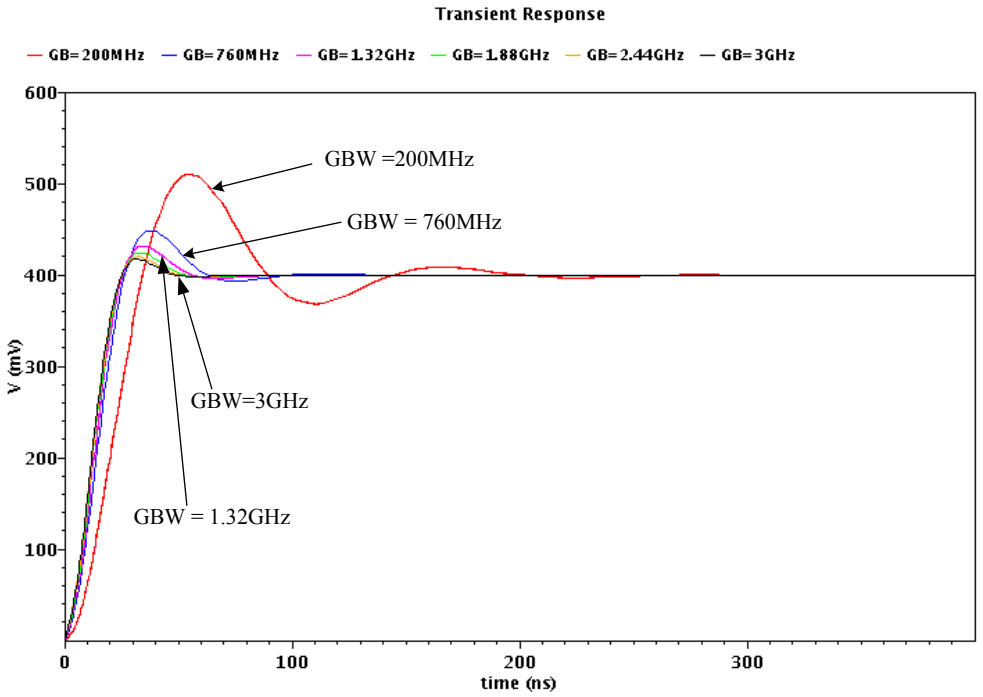

Figure 35 Transient response of the TIA to a current step of 400uA with the GBW of opamp2set to 3GHz and the GBW of opamp1 varied from 200MHz to 3GHz.

Figure 36 shows the input impedance of the TIA filter with the same settings used for Figure 35. The overall input impedance reduces for large GBW. However, from GBW of 1.32GHz to 3GHz, the improvement in the input impedance by increasing the GBW is not that substantial. For instance the peak value for the case with GBW of 1.32GHz is 5. Ω while the peak value for GB of 1. G z is Ω, so there is an improvement of just 1. Ω for a considerable amount of power which may be required to achieve a GB of 1.88GHz. A GBW of 1.4GHz is used for opamp1, because it gives a better compromise in terms of overshoot, settling time, input impedance and power consumption.

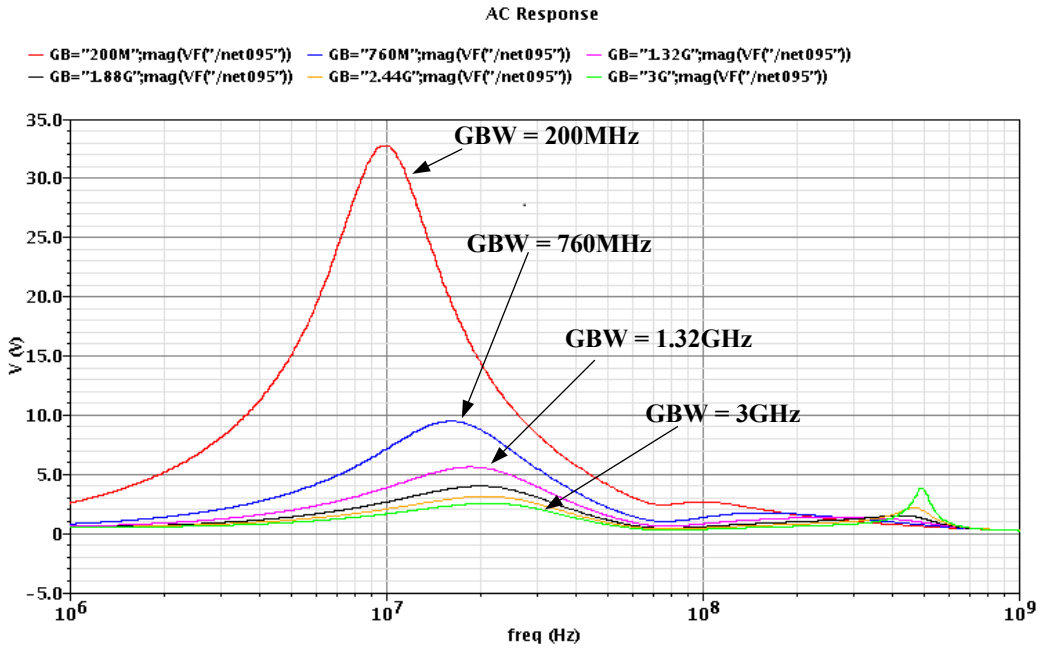

Figure 36 Input impedance of the TIA with the GBW of opamp2 set to 3GHz and the GBW of opamp1 varied from 200MHz to 3GHz.

Figure 37 shows the response of the TIA filter with GBW for opamp1 and opamp2 set to 1.4GHz and 1GHz, respectively. The bandwidth is somewhat degraded to 17.45MHz but this can be compensated by slightly changing the components' values.

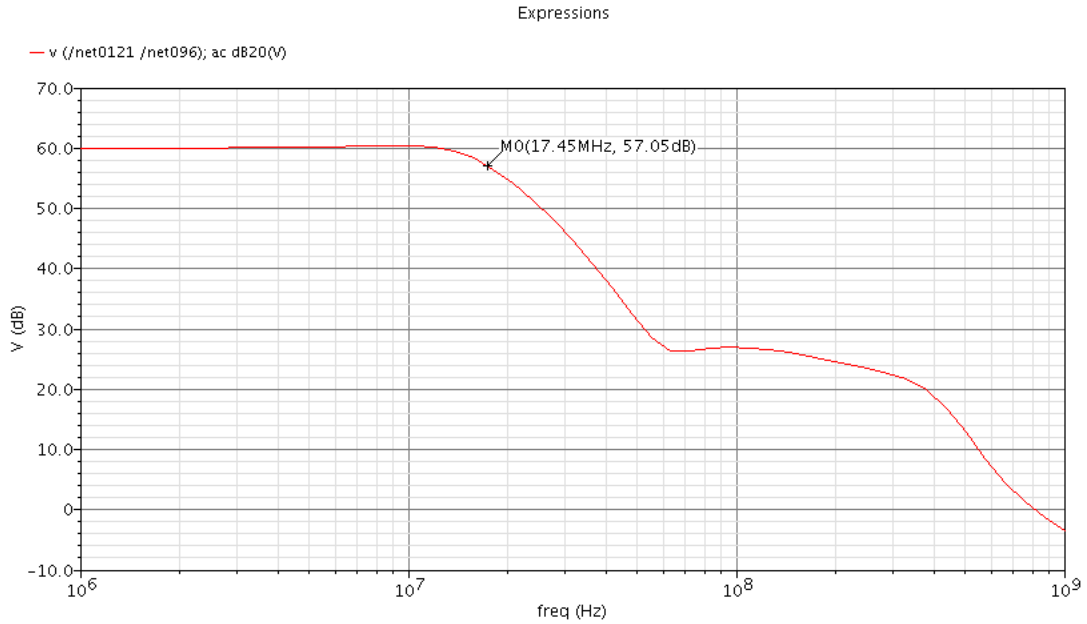

Figure 37 Magnitude response with GBW of opamp1 and opamp2 set to 1GHz and 1.4GHz, respectively.

Altering the components values helps to increase the bandwidth of the TIA but the attenuation at some critical frequencies are reduced. As shown in Figure 38, the attenuation is reduced by 2.73dB, but as discussed earlier attenuation of approximately 30dB is sufficient to suppress the large blockers. A summary of the final components' values and GBW of the opamps are shown in Table 4.

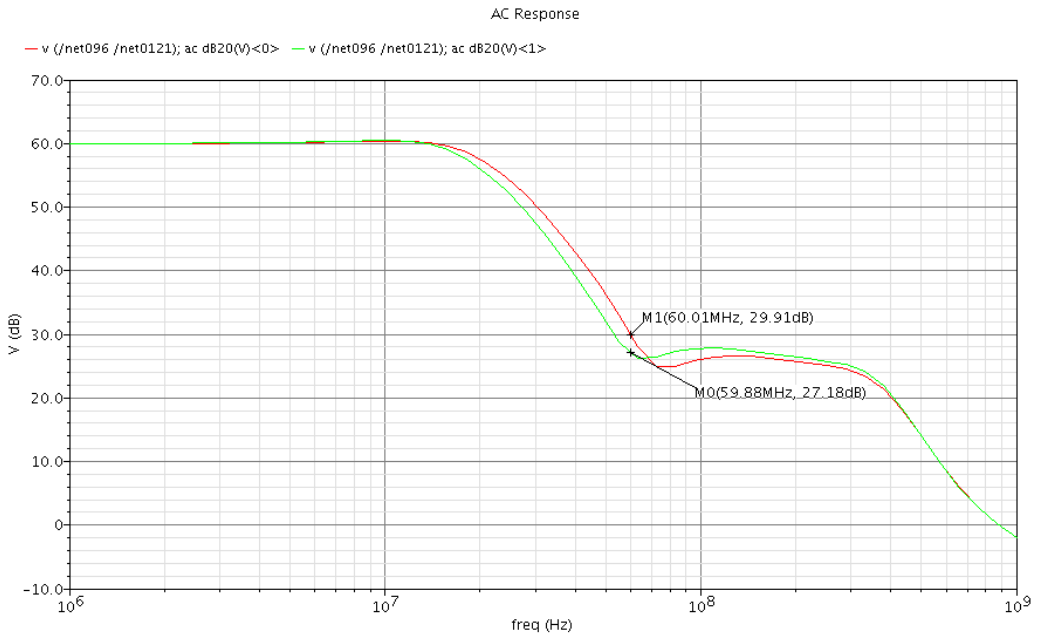

Figure 38 Comparing the transimpedance gain before and after changing the components' values to achieve the desired bandwidth.

Table 4 Summary of components values used in the implementation

Parameter	**Value**	**Parameter**	**Value**
R_F	1 Ω	R	0Ω
C_F	9.5pF	R_X	5kΩ
C_M	3.75pF	C_1	16pF
C_X	0.9pF	C_2	1pF
GBW for Opamp1	1.4GHz	GBW for Opamp2	1GHz

4.3 Amplifier Design

From system simulations, it is obvious that opamps with high gain and high bandwidth are required in the system. It is always difficult to design an amplifier with a high gain and high GBW, especially in short channel technologies. The most common scheme for designing such opamps is by cascading two or more stages. However, each stage adds a pole and degrades the phase margin. The conventional scheme to ensure stability in a cascade of stages is Miller compensation, which uses capacitors to split the poles of the various stages. The downside of the Miller compensation scheme is that, it forces the dominant pole to a lower frequency and this limits the bandwidth. The non dominant poles are pushed to high frequencies. Also a right half zero is also introduced, degrading the phase margin further. There are many reported schemes that use a resistor or a positive phase feed-forward stage to cancel the right half zero [14] - [15].

In [16], a feed-forward compensation technique known as no-capacitor feed-forward (NCFF) compensation is presented. The feed-forward path and the normal path have the same phase. With such a topology, a left-half-plane (LHP) zero is created and its positive phase shift can be used to cancel the negative phase shift of the poles to achieve a good phase margin. The dominant pole is not forced to lower frequencies, resulting in a higher bandwidth with a fast step response. The block diagram of the amplifier is shown in Figure 39.

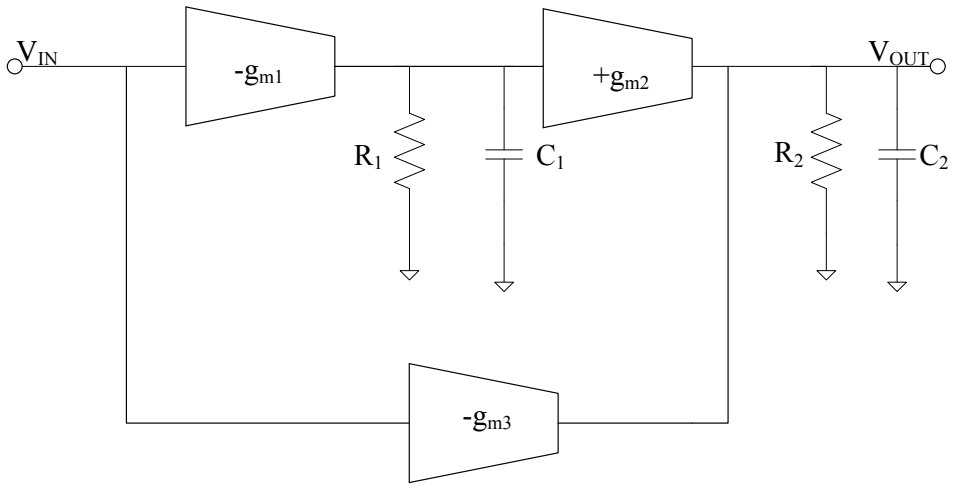

Figure 39 Block diagram of the amplifier with feed-forward compensation technique

The amplifier in Figure 39 has two main poles given by $\omega_{p1} = 1/R_1C_1$ and $\omega_{p2} = 1/R_2C_2$. The overall transfer function is given as

$$(s) \quad \frac{(g_{m1}\ _1 g_{m2}\ _2\ g_{m}\ _2)\left(1 - \frac{g_{m}\ _2}{(g_{m1}\ _1 g_{m2}\ _2\ g_{m}\ _2)\omega_{p1}}\right)}{\left(1 - \frac{s}{\omega_{p1}}\right)\left(1 - \frac{s}{\omega_{p2}}\right)} \qquad (4\text{-}17)$$

The DC gain is given as

$$Ao \quad g_{m1}\ _1 g_{m2}\ _2\ g_{m}\ _2 \qquad (4\text{-}18)$$

and the zero created is given as

$$\omega_z \quad \frac{(g_{m1}\ _1 g_{m2}\ _2\ g_{m}\ _2)}{g_{m}\ _2}\omega_{p1} \quad \frac{g_{m1}g_{m2}}{g_m\ C_1} \qquad (4\text{-}19)$$

The negative phase effect of ω_{p2} can be annulled by choosing ω_{p2} ω_Z. Pole-zero mismatches may degrade the settling time of amplifiers. However the settling time

requirement for opamps for continuous time filters is relaxed; hence such mismatches can be tolerated [17].

4.3.1 Circuit implementation of opamp1

Opamp1 is a two stage fully differential opamp with feed-forward compensation. Figure 40 shows the schematic implementation of opamp1. The first stage is similar to the first stage in [10] and is optimized for high gain. The dominant pole is at the output of the first stage and it is designed to be as high as possible to achieve the required GBW. The second-stage and feed-forward stages are designed for high bandwidth and medium gain to move the second pole to high frequencies. The second-stage transconductance gain is sum of g_{m6} and $g_{m2.}$ M_6 reuses the bias currents from M_2 and M_3 to conserve power.

The main contributor of distortion at lower frequencies is the output stage whereas the input stage is the main contributor at higher frequencies [18]. The swing at the output of the first stage is low because the signal is further amplified by the second stage. The second stage experiences large output swing; therefore its biasing should be carefully done to lessen its impact on distortion of the system. Due to the nature of the output stage, the drain-source voltages of the various transistors are much higher than the over-drive voltage, so the distortion from the g_{ds} of the output transistors is minimal. The main sources of distortion are the transconductance of the output stage transistors, consequently the over-drive voltage of the output transistors need to be chosen as high as possible.

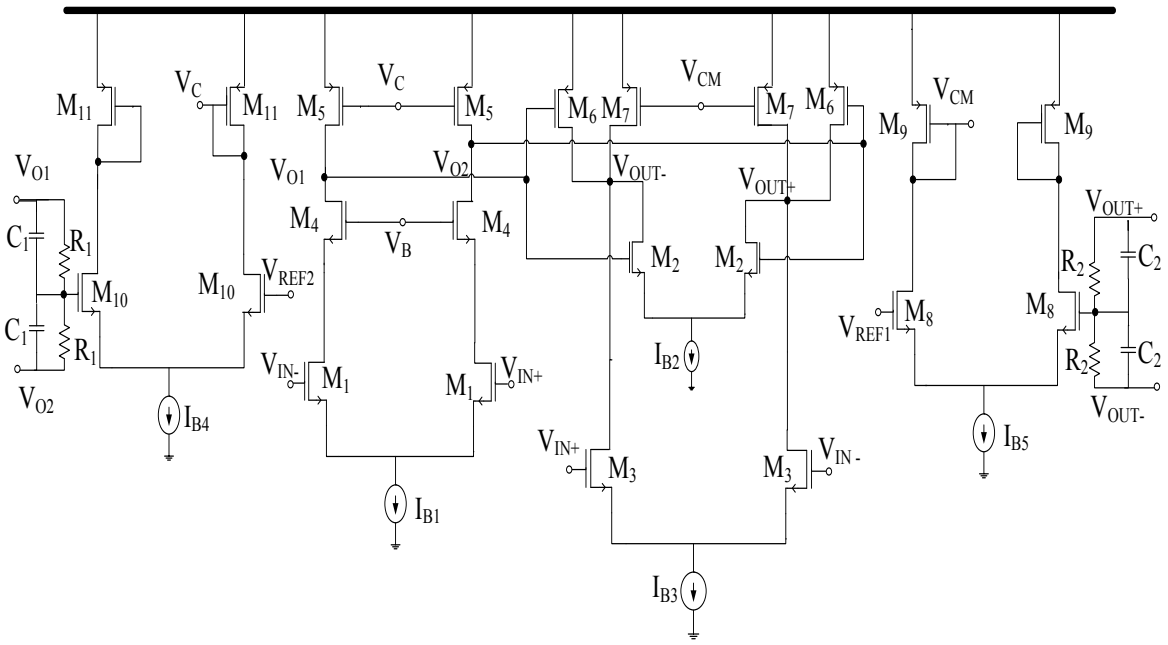

Figure 40 Schematic of the main amplifier (opamp1)

Each stage of opamp1 has a common mode feedback circuit (CMFB) which sets its output DC common mode level. The DC common mode voltages at the first and second stages are 1.1V and 0.9V, respectively. The first stage CMFB consists of M_{10} and M_{11}, and the second stage CMFB is formed by M_8 and M_9. The CMFBs use resistive averaging to detect the common mode voltage and feed back the error to the main circuit to correct the DC output voltage to the desired DC level. CMFB for the first and second stage have a left hand zero at R_1C_1 and R_2C_2, respectively. The zeros are used to improve the stability of the common mode loops. A summary of opamp1 components is shown in Table 5.

Table 5 Transistor dimensions, passive component values and bias current for opamp1

Device	**Dimensions**		**Device**	**Value**
	Multiplier	**(W/L)**		
M_1	10	4.76µm/0.6µm	I_{B1}	500µA
M_2	10	8µm/0.3µm	I_{B2}	1.1mA
M_3	40	40µm/0.3µm	I_{B3}	16.35mA
M_4	2	3.42µm/0.3µm	I_{B4}	530uA
M_5	5	13.02µm/0.3µm	I_{B5}	2mA
M_6	20	34.61µm/0.3µm	R_1	150kΩ
M_7	30	23.34µm/0.3µm	C_1	200fF
M_8	20	15µm/0.6µm	R_2	150kΩ
M_9	20	13.77µm/0.3µm	C_2	200fF
M_{10}	5	15µm/0.6µm		
M_{11}	8	8.65µm/0.3µm		

4.3.1.1 Layout of opamp1

The layout of opam1 is shown Figure 41. Wide transistors are broken into multiple fingers to reduce the drain and source area. This helps to reduce the parasitic capacitance and resistance. Matched devices have the same geometries and are matched with interdigitization and common centroid technique. With such techniques, the processing gradients that affect the matched transistors' electrical properties can be averaged across them.

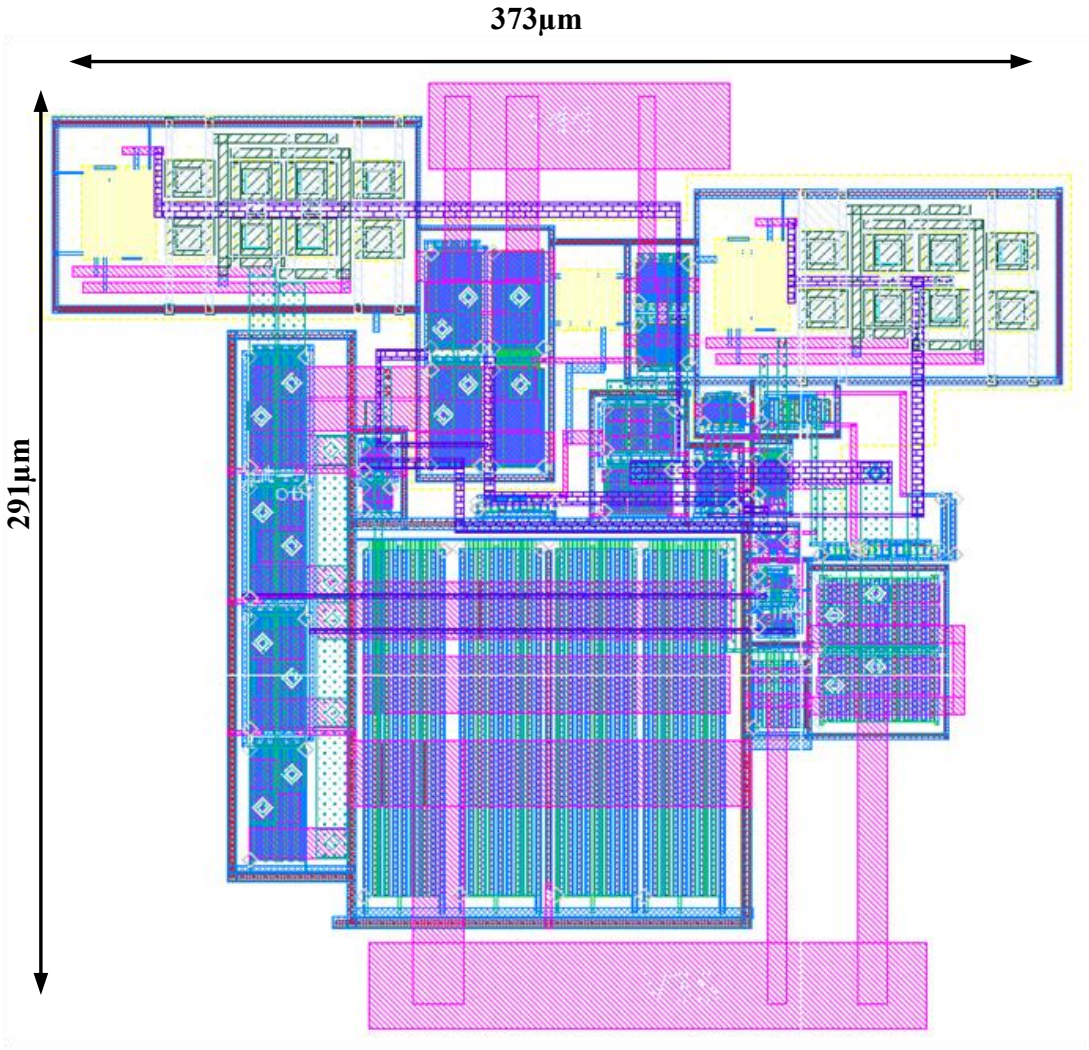

Figure 41 Layout of opamp1

4.3.2 Circuit implementation of opamp2

The schematic of opamp2 is very similar to opamp1. The only difference is the first stage, which as shown in Figure 42 is a simple differential pair with active loads. From

system level simulations, the GBW for opamp2 has to be at least 1GHz and its gain does not need to be as high as the gain of opamp1. Since the DC gain requirement for opamp2 is relaxed, the cascode transistor M_4 in Figure 40 which is used to improve the gain of the first stage can be removed to push the dominant pole to a higher frequency. The first stage uses a shunt feedback resistor load R_1 to set the common mode level[19]. The second stage CMFB is the same as the CMFB in Figure 40. The summary of the component values and dimensions are shown in Table 6.

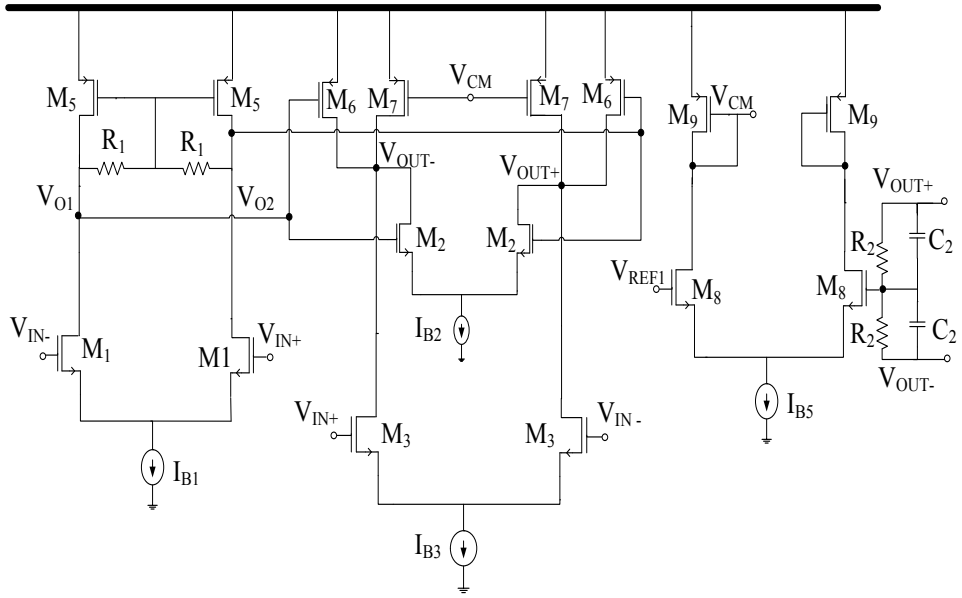

Figure 42 Schematic of the feedback amplifier (opamp2)

Table 6 Transistor dimensions, passive components value and bias current for opamp2

Device	**Dimensions**		**Device**	**Value**
	Multiplier	**W/L**		
M_1	5	5.84µm/0.6µm	I_{B1}	300µA
M_2	8	5µm/0.3µm	I_{B2}	530µA
M_3	25	26.02µm/0.4µm	I_{B3}	6.3mA
M_5	8	4.95µm/0.3µm	I_{B5}	900uA
M_6	15	27.76µm/0.2µm	R_1	0 Ω
M_7	5	15.1µm/0.2µm	C_2	300f
M_8	10	15.0µm/0.6µm	R_2	80 Ω
M_9	8	8.66µm/0.3µm		

4.3.2.1 Layout of opamp2

The same layout techniques for opamp1 are used for opamp2. The layout for opamp2 is shown in Figure 43.

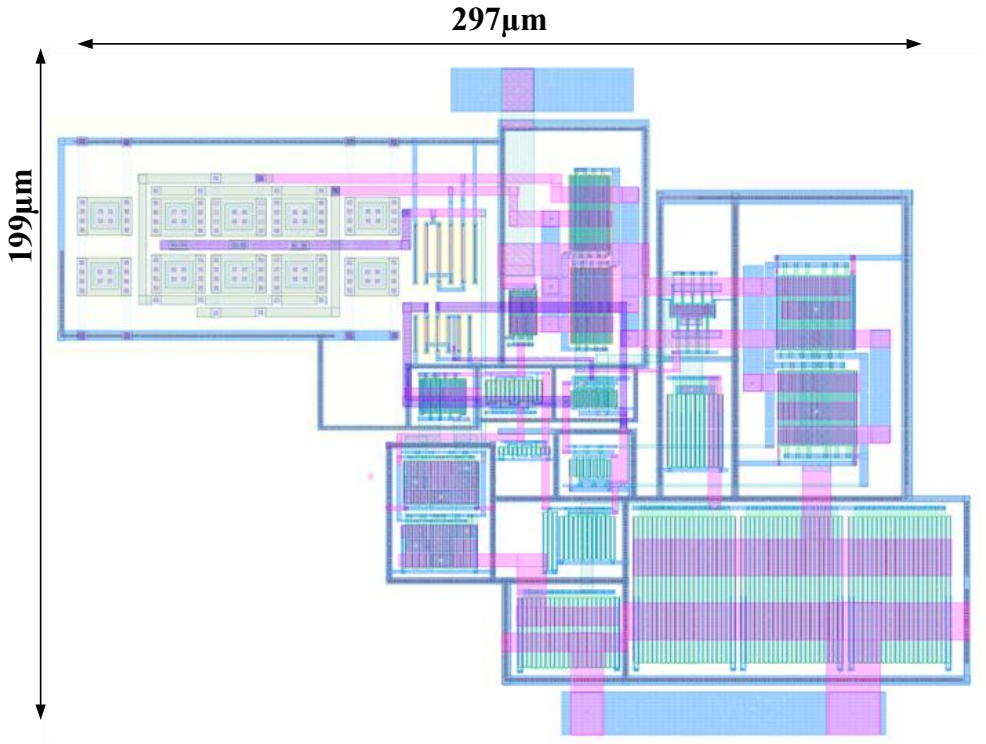

Figure 43 Layout of opamp2

A summary of the performance parameters of the opamps are shown in Table 7.

Table 7 Summary of performance parameter for opamp1 and opamp2

Parameter	**Opamp1**	**Opamp2**
DC gain (dB)	56	51
GBW (GHz)	1.4	1.3
Phase Margin	75	0 . 7
Power Consumption (mA)	21	8.4

4.4 Transistor Level Implementation Of The Proposed TIA

Figure 44 shows the top level implementation of the proposed TIA. Opamp1, Opamp2 and the current amplifier are at transistor level. The shunt capacitors (C_Y, mC_Y) at the input node are used to supplement the bandwidth limitations of the amplifiers. At high frequencies, most of the signal processing is done by the shunt capacitors.

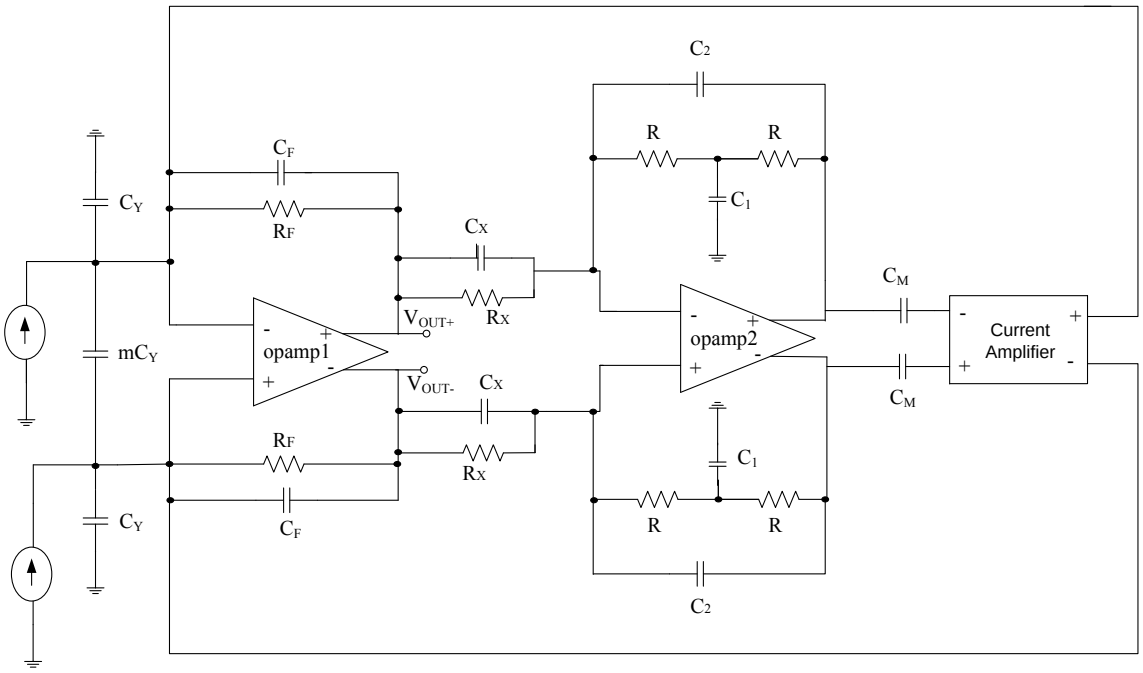

Figure 44 Top Level implementation of the proposed TIA with C_Y = 40pF and m =3.

5 RESULTS

In this section, the filter test setup, layout and simulations results are presented. A comparison of post layout and schematic simulation results are also described. The TIA was designed, laid out and simulated with IBM 180nm CMOS technology.

5.1 Layout

The complete layout is shown in Figure 45. The total chip area is approximately 1.3mm×1.22mm. Interdigization and common centroid techniques are employed throughout the layout to minimize mismatches. Dummy transistors are also used as ending elements to ensure etching and diffusion processes are equalized over all segments of the various devices. All the capacitors are matched with common centroid technique and laid out with square geometries to curtail random mismatches due to peripheral variations.

The metal lines are carefully routed to reduce parasitic capacitances and to ensure the same parasitic impedance in the differential paths. The metal with the least sheet resistance is used for the power lines and are also made as wide as possible to reduce the resistive voltage drops. Metal lines carrying significant amount of current are also made as wide as possible to reduce the voltage drops. The devices are located such that the metal routing distances are considerably lessened. All routing metal widths in critical signal paths are designed to comply with electrical migration rules.

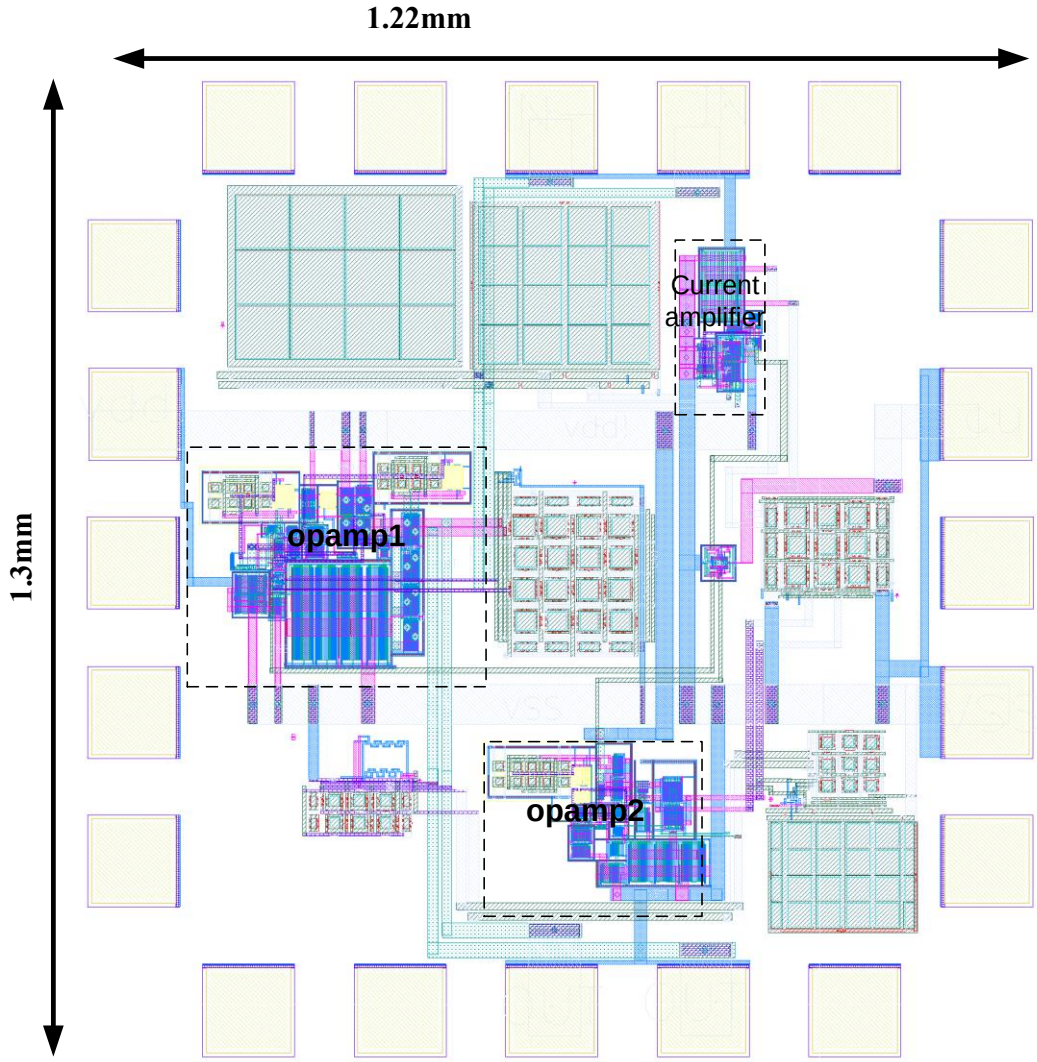

Figure 45 Layout of the TIA

5.2 Filter Setup

In the test bench shown in Figure 46, the input is modeled as a Norton current with an output impedance of 1MΩ. A capacitive load of 1pF is connected at the output to model the package parasitic. The bias current is set by an external resistor. The bias current

with a couple of current mirrors in the design are used to provide the current to set the bias voltages for the opamp1, opamp2 and V-I differentiator. DC voltage sources are used as the supply voltages (vdd! and VSS).

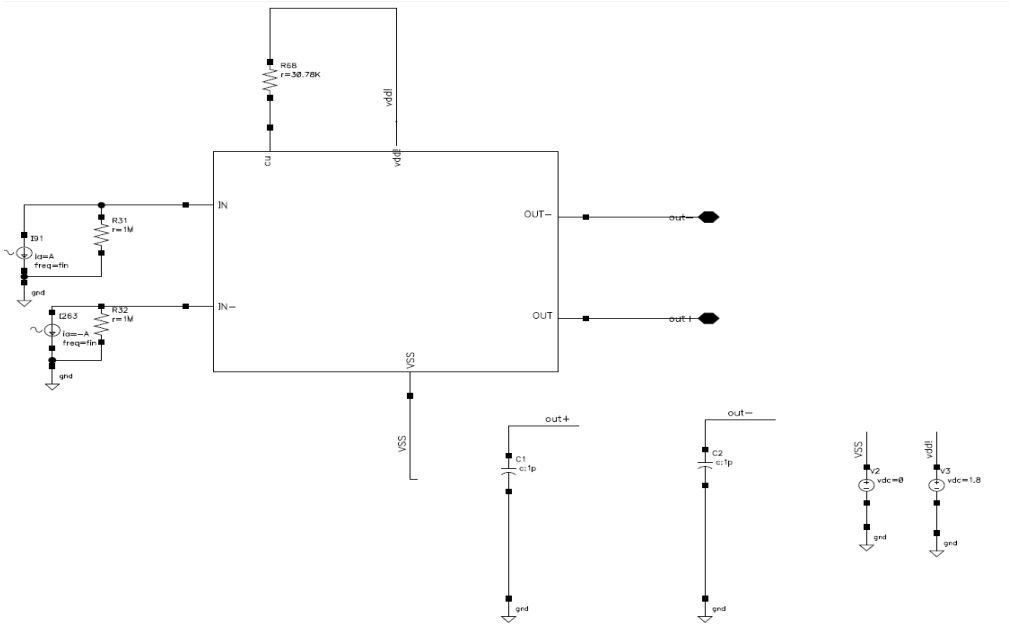

Figure 46 Testing circuit setup

5.3 Simulation Results

The post layout and schematic magnitude response of the proposed TIA is shown in Figure 47. The magnitude response of the conventional TIA is also shown in Figure 47 for comparison. At 60MHz, the attenuation for the post layout, schematic and the first-order are 29.18dB, 28.18dB and 10dB, respectively. In both the schematic and the post layout, the attenuation provided by the proposed TIA is improved by at least 19dB. From

50MHz to 200MHz, the attenuation provided by the schematic and layout are comparable, but beyond 200MHz, the attenuation provided by the layout is slightly higher than the schematics due to the added parasitics in the layout. Also the bandwidth for the layout is slightly reduced due to the parasitics.

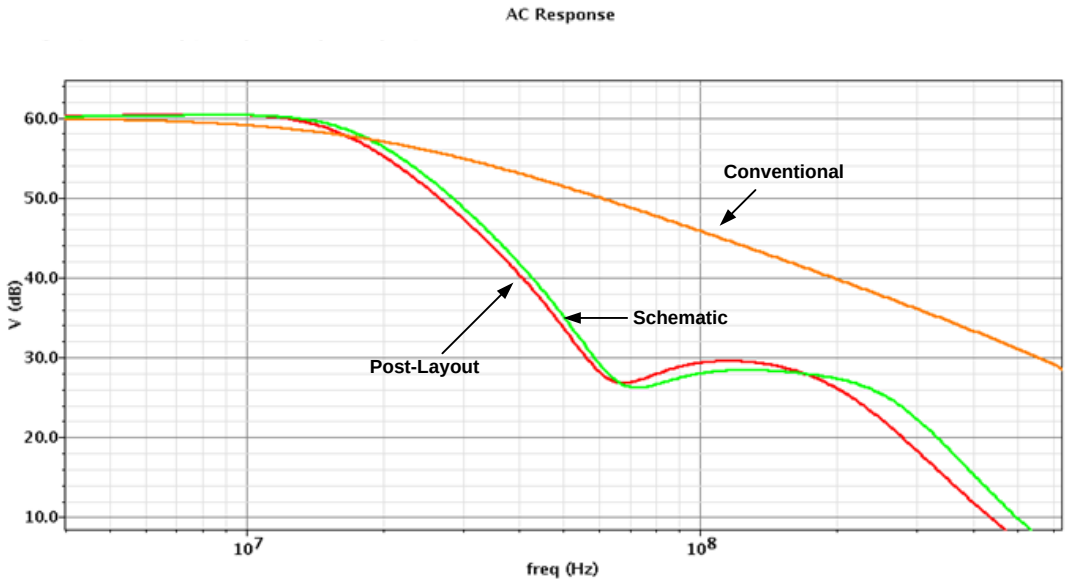

Figure 47 Magnitude response of the conventional and the proposed TIA

To verify the response shown in Figure 47 , the system was tested with an input current with amplitude of 5mA (10mA differential) at 60MHz. As shown in Figure 48, the amplitude of the post layout and schematic output voltage levels are 252mV and 290.6mV, respectively while the amplitude of the output voltage level of the conventional TIA is 3.15V. IBM 180nM process supports a supply voltage level of 1.8V, so the opamp for the conventional TIA is implemented with a macromodel to

prevent the opamp from saturating. Evidently a first-order TIA designed in this process cannot tolerate blockers of such magnitude unless the supplies are increased and some complex circuitries are employed to protect the transistors. Again as expected, the amplitude of the output voltage in the post layout is slightly lower than the schematics due to the lower attenuation offered by the layout as shown in Figure 47

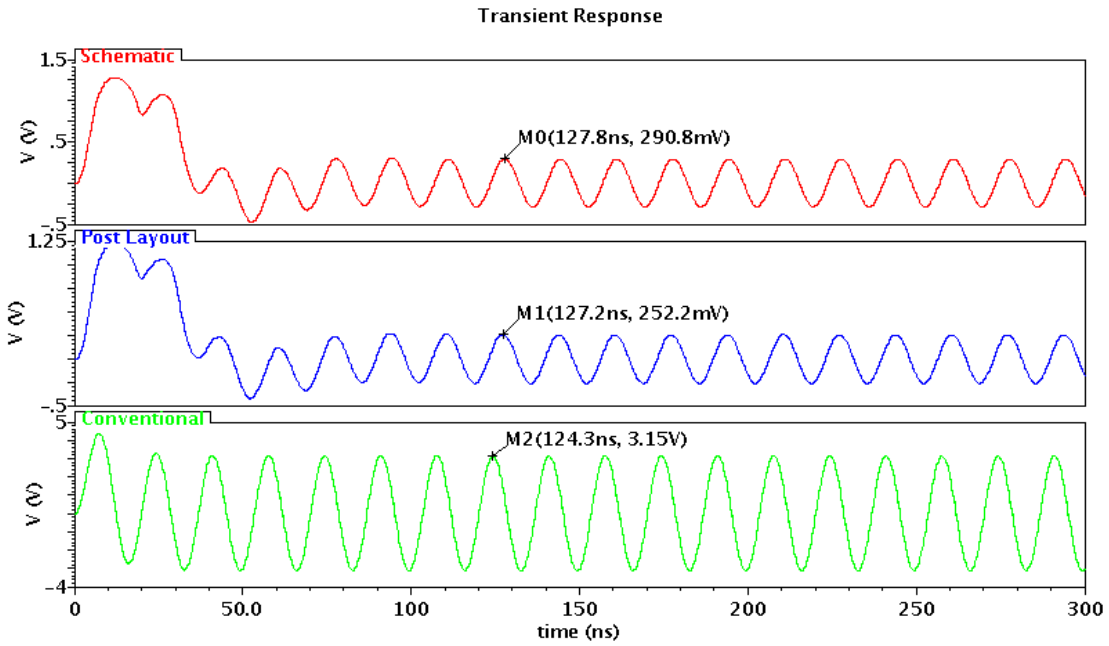

Figure 48 Transient response of the conventional and proposed TIA to an input current of 5mA at 60MHz

Figure 49 shows the magnitude response of the input impedance. There is a slight difference in the input impedance for the layout and the schematic. The parasitic impedance of the metal connectors accounts for the difference observed. The conventional TIA shows a peak input impedance of 14.74Ω at frequencies greater than

60MHz, whereas the schematic and post-layout of the proposed TIA exhibits a peak impedance of . Ω and 5.7Ω, respectively. So, at frequencies beyond 60MHz, where the large interferers are expected, and the proposed TIA input impedance is considerably lower than the conventional TIA. Therefore, the linearity of the mixer at the input is improved at the critical frequencies. Figure 50 demonstrates the effect of the reduced input impedance of the proposed TIA in the presence of an out-of-band blocker of 10mA at 60MHz. The amplitude of the input voltage in the proposed TIA (post-layout) is reduced by a factor of almost 10, which can significantly impact the out-of-band linearity performance of the triode operating current mode mixer.

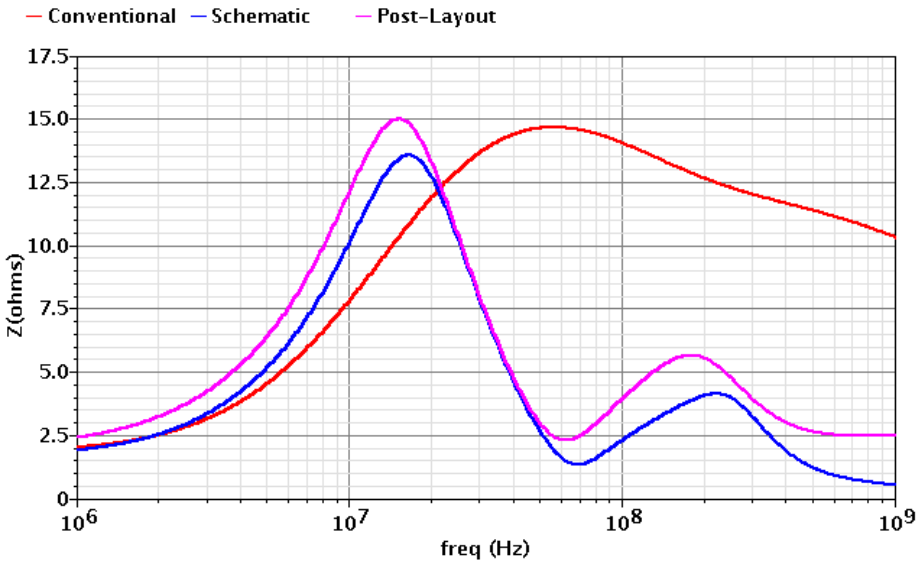

Figure 49 Input impedance of the filter

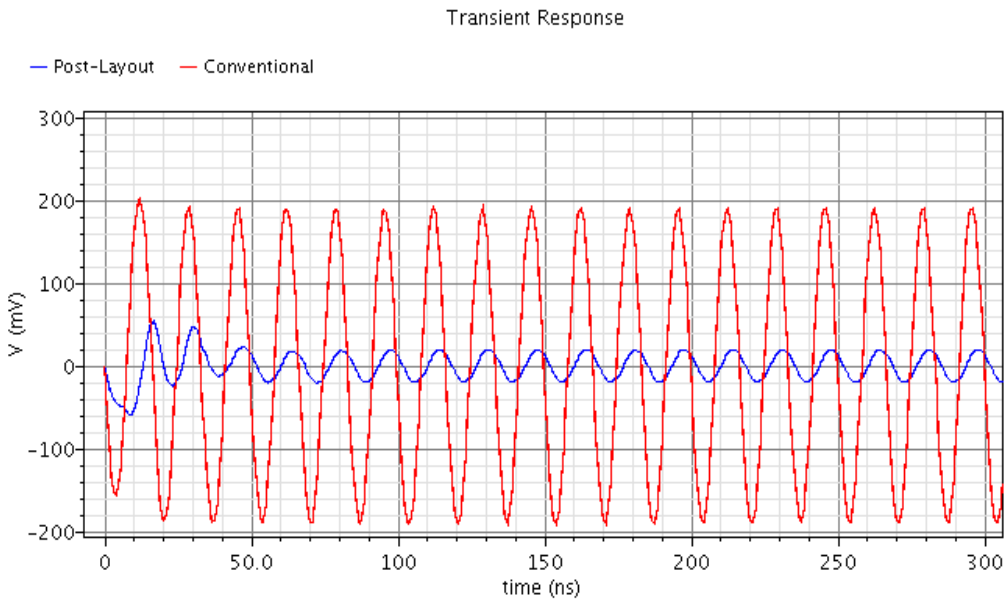

Figure 50 Transient input voltage to an input current of 10mA at 60MHz

In Figure 51, the transient response of the TIA to an input step of 400uA is shown. In all cases the output follows the input. As anticipated, there is slight ringing and overshoot in the step response of the proposed TIA while the conventional TIA approaches its final value in an exponential manner. For the conventional TIA, the settling time is around 70ns and for the proposed TIA, the post-layout and schematic response show a settling time of 101ns and 97ns, respectively.

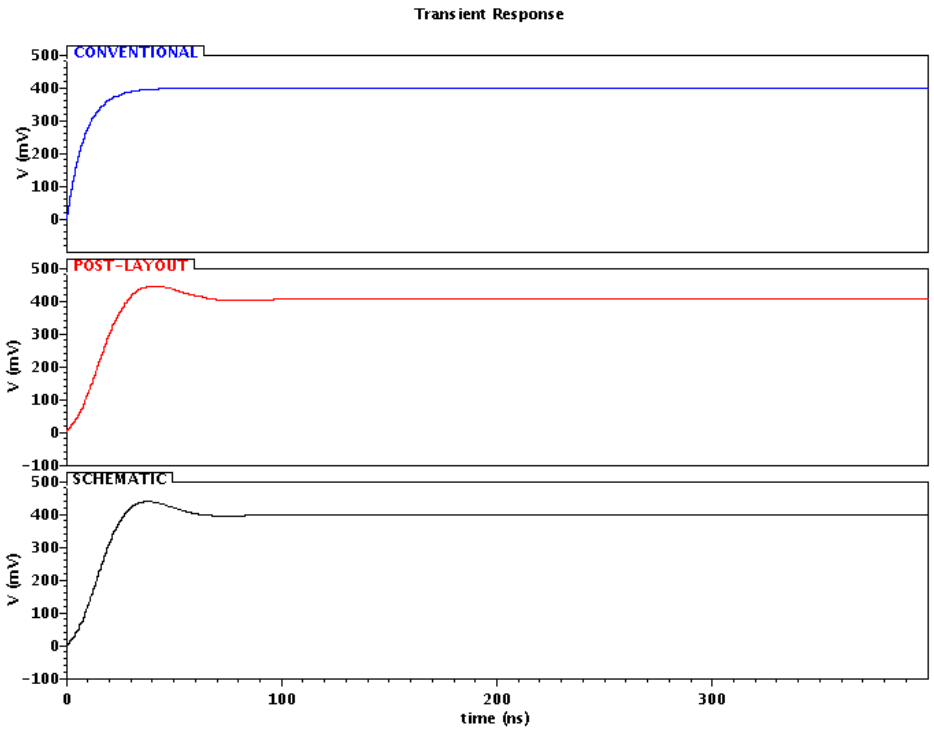

Figure 51 Step response of the TIA

Figure 52 shows the noise performance of the proposed TIA. The noise current of the proposed TIA is higher than the conventional TIA. The major noises are from the V-I differentiator block. There is a trade-off between power and noise. As discussed in section 4, the use of large capacitor places a huge power and slew rate burden on opamp2. The use of the V-I differentiator helps to mitigate this requirement. Also in systems where linearity of large out-of-band blockers is more critical than noise, the noise levels shown in the proposed TIA may not be that crucial. Table 8 shows a summary of the integrated noise current of the proposed and conventional TIA.

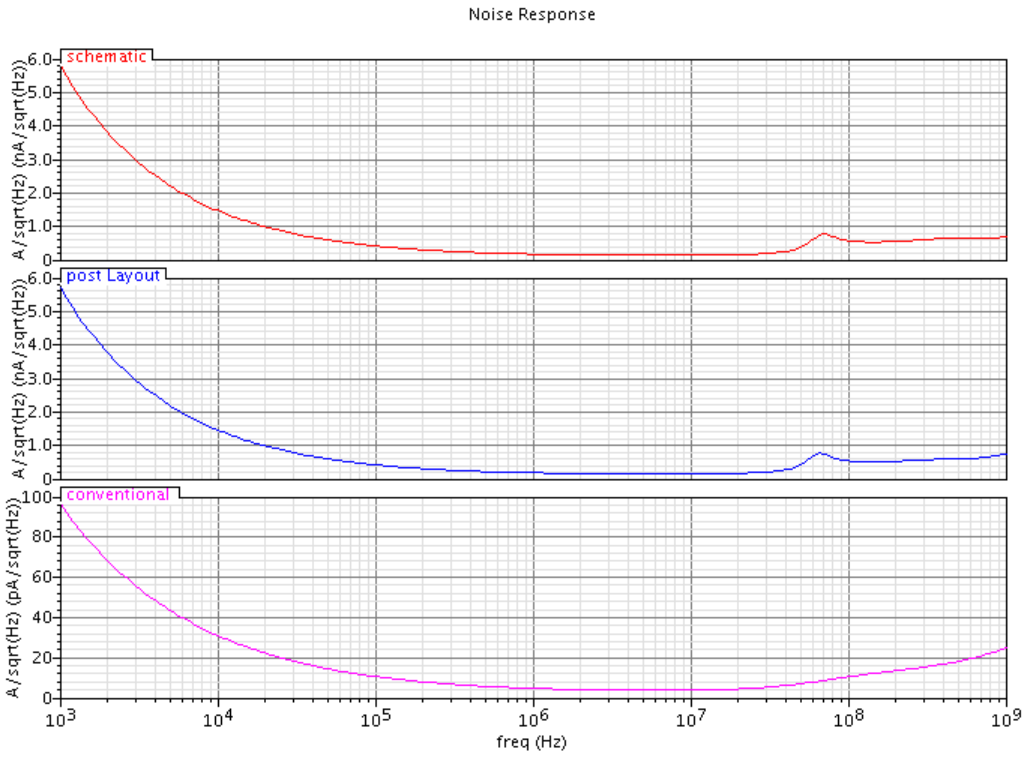

Figure 52 Input noise current of the conventional proposed TIA

Table 8 Input referred integrated noise current

TIA Filter	**Integrated noise (1KHz-20MHz) /nA**
Conventional	20
Proposed Schematic	764
Proposed Post Layout	800

Figure 53 compares the transient response of the proposed and convenitonal TIA to in-band signal of 100uA at 10MHz in the presence of an out-of-band blocker of amplitude 10mA at 60MHz. The amplitude of the output signal for the proposed TIA is 350mV,

whereas the amplitude of the conventional TIA is 1.75V. The amplitude of the proposed TIA is relaxed by almost 1.4V. The DFT of Figure 53 is also shown Figure 54. The attenuation of the 10mA component at 60MHz in the proposed TIA is improved by 17dB when compared to the corrresponding component in the conventional TIA.

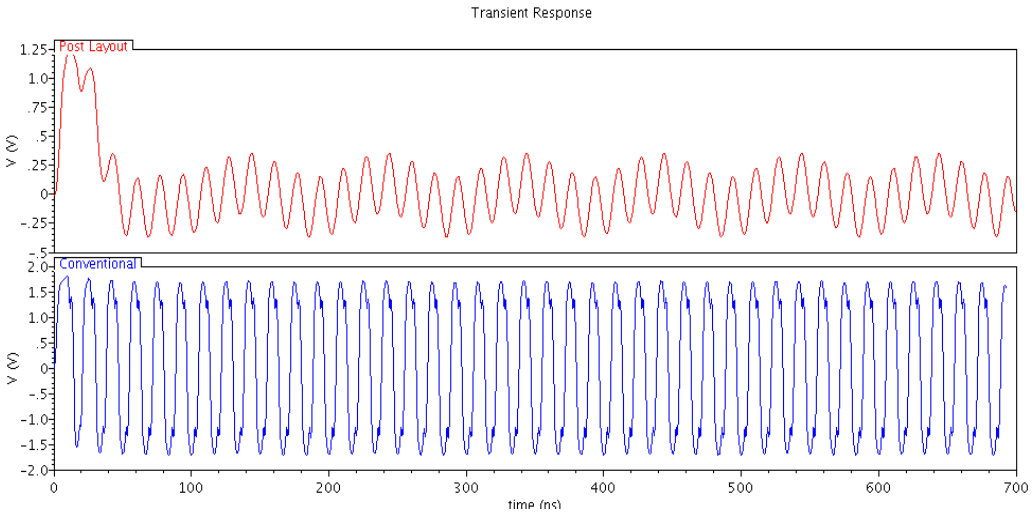

Figure 53 Transient response of TIA to an in-band current of amplitude 100µA at 10MHz and out-of-band block of 10mA at 60MHz

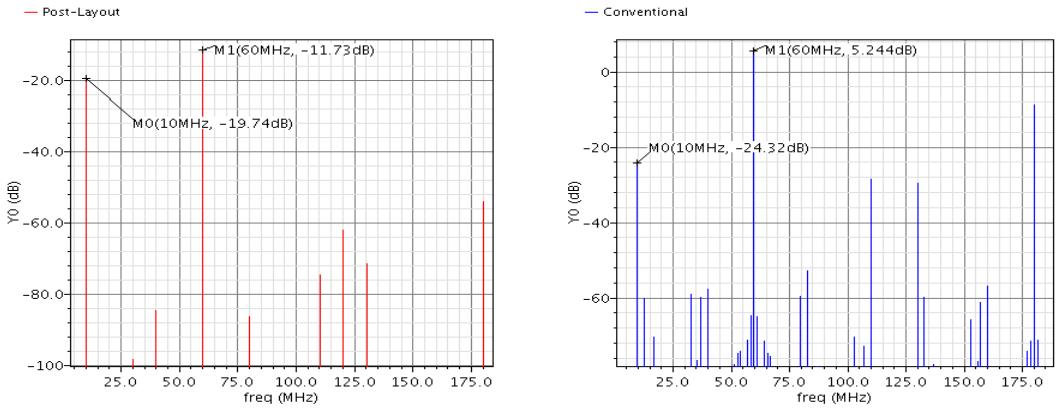

Figure 54 DFT of the transient response of TIA to an in-band current of amplitude 100µA at 10MHz and out-of-band block of 10mA at 60MHz

Figure 55 shows the intermodulation product of two out-of-band interferers. The input to the TIAs has two components at 60MHz and 110MHz with amplitude of 10mA. The intermodulation product of importance is the $2f_1$-f_2, which falls in the band of interest. As discussed earlier, the impact of the $2f_1$-f_2 can drastically degrade the system performance through gain compression and desensitization of the TIA. For f_1 = 60MHz and f_2 = 110MHz, the intermodulation product at $2f_1$-f_2 is 10MHz. Compared to the conventional TIA, the intermodulation product at 10MHz in the schematic and post-layout of proposed TIA are reduced by 10.84dB and 10.54dB , respectively. This improvement is due to the increase in stop-band attenuation of the proposed TIA.

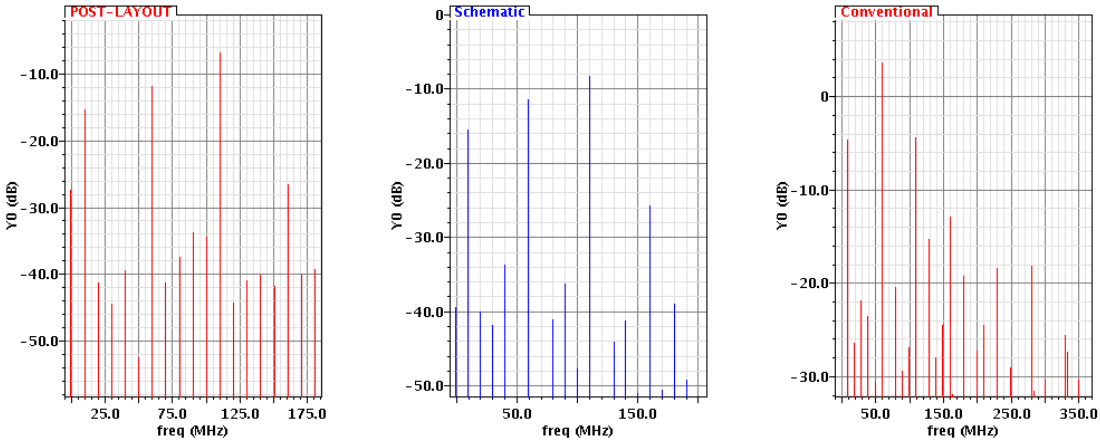

Figure 55 DFT of the TIA to an input of 10mA at 60MHz and 110MHz

Non-linear systems tend to lose gain as its input levels are increased. In Figure 56, the single tone 1dB compression levels of the conventional and the TIA are compared. The plot shows the amplitude of the input current that causes the gain of the output signal to compress by 1dB at various frequencies. As can be seen, the in-band 1dB compression for the conventional and the proposed TIA are almost the same. The difference lies in the stop-band where the 1dB compression point for the proposed TIA is significantly higher than the conventional TIA. From 40MHz and beyond, the proposed TIA can handle a current of at least ±5mA (single ended) before the gain is compressed by 1dB. At 60MHz, the post layout simulation shows that, the TIA can handle up to 15mA of current before its gain compresses by 1dB. Input current with amplitude of 15mA translates to an output voltage with amplitude of approximately 0.47V, which means the system should be able to cope with output swing of such magnitude. However, the TIA was designed for a blocker level of ±5mA with maximum swing of ±200mV. Operating

the TIA at amplitudes higher than ±5mA may cause opamps to be slew-limited across process and temperature increasing the overall distortion. Finally, a summary of the performance of the proposed TIA filter in comparison to the conventional TIA filter is shown in Table 9.

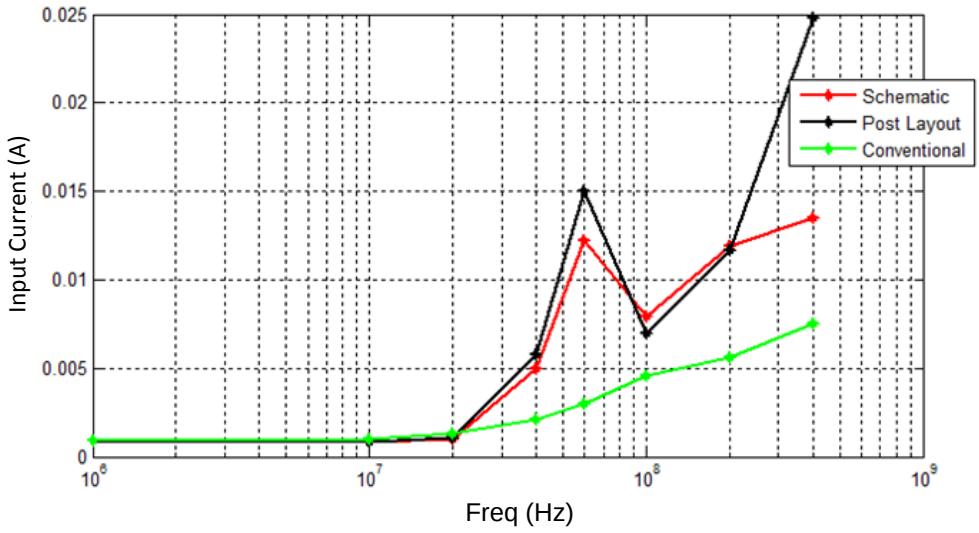

Figure 56 1dB compression point

Table 9 Proposed TIA performance summary

Parameter	**Units**	**Single-Pole TIA**	**Proposed TIA**
Transimpedance gain	dBΩ	60	60
f-3dB	MHz	20	20
Z_{IN}, single-ended (60MHz and beyond)	Ω	< 14.74	< 5.7
-1dB compression level for single OOB tone at 60MHz	mA	3	15
Vsupply	V	1.8	1.8
Total current consumption	mA	21	35
Maximum output voltage swing	mV	±200	±200
Max interferer level at 60MHz	mA	0.63	5
Input referred integrated noise (1kHz - 20MHz)	nA	20	800
Area	mm^2	-	1.3×1.22

6 SUMMARY AND CONCLUSIONS

In this work, a novel TIA architecture is presented. The TIA was designed and laid out in IBM 180nm CMOS process with a power supply of 1.8V. The topology is similar to the conventional TIA with a resistor and a capacitor in the feedback, which provides first order attenuation in the stop-band. The capacitor is replaced with higher order high-pass filter which provides more attenuation or suppression to out-of-band blockers in the stop-band. The desirable in-band performance of the conventional TIA is maintained in the proposed TIA.

The TIA was implemented with a 3rd order inverse Chebyshev approximation. This was chosen because it provides a significant attenuation in the stop-band and offers optimum group delay variation to incoming signals in the pass-band.

The added block in the feedback has two paths from the output to the input. The first path is a cascade of a second-order voltage to voltage filter (biquad) and a V-I differentiator. The second path is a feedback capacitor which converts the output voltage directly to current at the input node. The high current conversion from a low voltage swing at the output of opamps necessitates the use large capacitor sizes for implementation of the V-I differentiator in the feedback. To alleviate the large capacitor requirement, a V-I differentiator is proposed. The details of the design and impact of the proposed V-I differentiator were presented. Also to save power, the biquad in the

feedback uses a novel single opamp architecture which requires real transmission zeros. It was shown that, by careful selection of the value of the feedback capacitor, the zeros of the transfer function for the implementation of the biquad can be made real.

Compared to the existing first order architecture, the proposed TIA achieves attenuation of more than 20dB to large interferers at 60MHz. The TIA handles blockers of magnitude ±10mA (differential) at 60MHz and beyond with maximum voltage swing of ±400mV (differential) at the output of the opamps. In addition to improving the attenuation to interferers, the input impedance of the TIA in the region where large interferers are anticipated is considerably improved. Reduced input impedance helps to improve the linearity of the preceding mixer.

Power consumption and noise are higher in the proposed TIA. The increased power and noise are due to the additional blocks in the feedback. Future work should be dedicated to improving the noise performance and decreasing power consumption.

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