ELECTROMAGNETIC INTERFERENCE (EMI) RESISTING ANALOG INTEGRATED CIRCUIT DESIGN TUTORIAL

A Thesis

by

JINGJING YU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2012

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sanchez-Sinencio
Committee Members,	Samuel Palermo
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ABSTRACT

Electromagnetic Interference (EMI) Resisting Analog Integrated Circuit Design Tutorial.

(August 2012)

Jingjing Yu, B.S., Shanghai Jiao Tong Univerisity, China

Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

This work introduces fundamental knowledge of EMI, and presents three basic features correlated to EMI susceptibility: nonlinear distortion, asymmetric slew rate (SR) and parasitic capacitance. Different existing EMI-resisting techniques are analyzed and compared to each other in terms of EMI-Induced input offset voltage and other important specifications such as current consumption.

In this work, EMI-robust analog circuits are proposed, of which the architecture is based on source-buffered differential pair in the previous publications. The EMI performance of the proposed topologies has been verified within a test IC which was fabricated in NCSU 0.5um CMOS technology. Experimental results are presented when an EMI disturbance signal of 400mV and 800mV amplitude was injected at the input terminals, and compared with a conventional and an existing topology. The tested maximal EMI-induced input offset voltage corresponds to -222mV for the new structure, which is compared to -712mV for the conventional one and -368mV for the one using existing source-buffered technique in literature. Furthermore the overall performances of the circuits such as current consumption or input referred noise are also provided with the corresponding simulation results.

DEDICATION

To my family and friends

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincere appreciations to my advisor, Dr. Edgar Sinencio-Sanchez for giving me this great honor and opportunity to join his group as a master student. With his patient and professional supervising, I have finished my graduate study confidently and well. I would also like to thank all my committee members, Dr. Samuel Palermo, Dr. Sunil Khatri and Dr. Rainer Fink for their precious time, and valuable suggestions.

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Last but not the least, I would love to express my deepest gratitude to my parents for their unconditional affection with no limits. In the early stage of my life, they have taught me about the right and wrong, and the spirit of never giving up and adhering to the end. I could never reach this far without their support.

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1. INTRODUCTION

1.1 Research Motivation

As the integrated circuit technology is scaling down, the density of components packed on printed circuit boards is much higher, and the request for high speed applications is increasingly intense, the electromagnetic interference has gradually become a critical issue for IC designers to consider during the design phase. Ignoring those aspects might result in failures on circuits induced by spurious signals arising from a variety of sources, e.g. EMI at high frequencies out of the working range of the circuits.

EMI can affect lots of electrical or electronic equipments with interconnections. For instance, aircraft might be susceptible to electronic interferences because they rely on radio communication and navigation systems whose electromagnetic spectrum ranges from 10 KHz (e.g. navigation systems) up to above 9 GHz (e.g. weather radar). Moreover, the massive introduction of electronics in automobiles might cause problems, e.g. cellular telephone transmitters can disturb braking systems (ABS). EMI might become significant inside the automobile, where there are many potential sources of such disturbances, like alternator, ignition system, switching solenoids, electric starter, and lamps [1]. The electromagnetic interference pollution collected by these modern electronic system harnesses has significantly increased the level of radio frequency interference (RFI), which might be significantly higher than that of nominal signals.

Generally EMI is picked up by wires and traces in printed circuit board and RFI

This thesis follows the style of *IEEE Journal of Solid State Circuits.*

can be derived from it or even from the RF signals which are generated on the same chip where RF amplifiers, power supplies and digital subsystems are integrated (Fig. 1. 1) [2]. In present day, the integrated circuit susceptibility on EMI can be under control by filters, shielding, a posteriori layout adjustment and so on. However, in some applications these solutions are often very expensive and complex, and even rarely viable because most of control, communication and power circuits are fully integrated on silicon as they are in smart power ICs [3]. Therefore, in recent years, the integrated circuits, especially the high-performance digital or analog circuits that might include operational amplifiers, should be designed to be intrinsically immune to EMI without the support of the off-chip filters, and EMI should be deeply researched theoretically and experimentally to obtain better prevention methods.

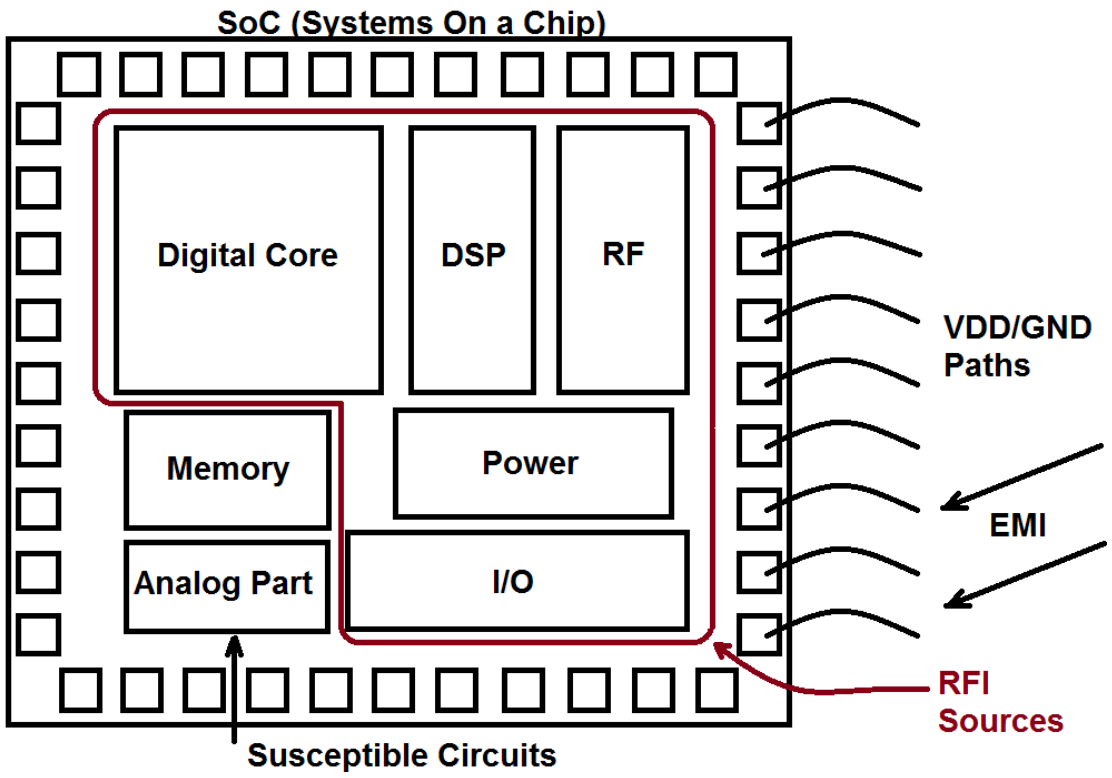


Fig. 1. 1. Sources of EMI/RFI in a System on a Chip (SoC) typical architecture

1.2 Research Objectives

As operational amplifiers are one of the most common analog building blocks employed in the design of analog and mixed-signal ICs, and they are sensitive to the present day more and more critical EMI/RFI issues, the main goals of this research are to obtain a detailed understanding of EMI/RFI effects, analyze and summarize the basic phenomena related to EMI susceptibility of operational amplifiers, compare the performance of the existing EMI-resistant techniques and extract the corresponding advantages and disadvantages, and design EMI-robust operational amplifier with better performance not only at relatively low EMI frequency but also in high frequency range.

This work is also aimed to deal with the comparison between the final new design and other reference topologies, from both a circuit and a measurement point of view, of EMI-induced failures. To investigate the EMI effects on a generic amplifier, the interfering signals should be modeled by a waveform easily reproducible with a standard function generator, which are often modeled by a sinusoidal waveform generated with a zero dc voltage source superimposed on the pins connected to long wires (long wires act as antennas from EMI) [4] – [6]. One of the most undesirable effects of interferences is a shift of the output DC mean value which might asymptotically force the amplifier, or a subsequent stage, out of the normal operation as shown in Fig. 1. 2 [1]. Moreover, the interfering signals among all the possible ones, coupled on the input pins of the operational amplifiers are the most difficult and important to take care of. This is because of the fact that the adoption of external filters is usually not viable, since they might attenuate the intentional input signals that are often weak. Instead, as far as the power pins are concerned, external filtering can prevent the dangerous dc offset to be generated [7].

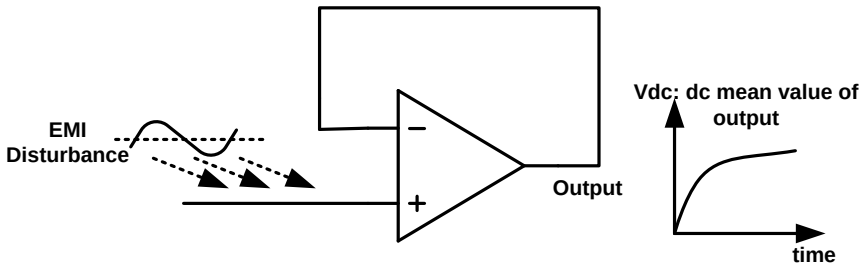


Fig. 1. 2. Effect of EMI/RFI conveyed to the input pin

1.3 Thesis Organization

This thesis is composed of eight sections.

Section 1 introduces EMI briefly from an industrial prospective, discusses why EMI is so important to be considered of, and then describes the objectives for this EMI research.

Section 2 gives an introduction of basic definitions for four EMC terms according to some specific references, and two different EMI transmission types; then illustrates conducted EMI/RFI Effects in integrated active devices, e.g. bipolar and MOS transistors and compare the effects in analog versus digital integrated circuits; finally presents three basic Features correlated to EMI susceptibility: nonlinear distortion, asymmetric slew rate (SR) and parasitic capacitance.

Section 3 discusses and studies several basic circuit topologies, which illustrate theoretical observations of EMI susceptibility versus weak nonlinearity, followed by its relationship with strong nonlinear behavior and asymmetries.

Section 4 analyzes the EMI susceptibility of different transistor structures and existing techniques, and compares each other in terms of EMI-Induced input offset voltage and other important specifications such as current consumption. The effects are discussed in relation to the most significant phenomenon here, which is the weak nonlinear behavior of the input pairs to which a high-frequency EMI signal is conveyed and when it does not force the circuit into cut-off operation.

Section 5 proposes EMI-robust structure at the base of the original source-buffered scheme in the previous publications. Transistor-level implementations, pre-layout and post-layout simulations are well explained in this section.

Section 6 shows the testing results. A comparison of start-of-art works is listed in this section as well.

Section 7 summarizes the EMI research in this thesis and makes the conclusions.

Section 8 is the appendix section, which introduces how to submit the layout project in NCSU 0.5um CMOS technology to MOSIS website.

2. EMI FUNDAMENTALS AT IC LEVEL

2.1 Basic Definitions

Electromagnetism is a scientific discipline which is generally considered to be a standalone subject, dealing with antennas, transmission lines and radio waves, and not tied to electricity and electronics directly; however, its impact on EMC (Electromagnetic compatibility) is basic and profound. Related to the design of electrical applications and general electromagnetic principles, EMC is an interdisciplinary scientific domain that has introduced and maintained its own typical vocabulary, conventions, definitions and design guidelines over the years [8]. In order to describe the theory of EMC, a variety of definitions are applicable, while the definition shown here is of clearness and unambiguity, which the one offered in [9]:

Electrical and electronic devices are said to be electromagnetically compatible when electrical noise generated by each does not interfere with the normal performance of any of the others. Electromagnetic compatibility is that happy situation in which systems work as intended, both within themselves and within their environment.

If there is no EMC, this is because of EMI. The culprits that should be controlled include RFI, TVI (television interference) and EMI actually. The former two interferences can be defined as high-frequency electromagnetic waves that emanate from electronic devices such as chips, and from electronic devices causing interference to television reception. When an electrical disturbance in a system due to natural phenomena, low-frequency waves from electromechanical devices or high frequency waves (RFI) from chips and other electronic devices, it can be specified as EMI. Quoted from [9]:

EMI is said to exist when undesirable voltages or currents are present to influence adversely the performance of a device. These voltages or currents may reach the victim devices by conduction or by electromagnetic field radiation, (the term "radiated interference" comprised two phenomena, named "near field coupling" and "far field coupling").

If there is EMI, there is at least one EMI source resulting in an insufferable emission, which is susceptible to the emanated disturbance. According to the description by the International Electrotechnical Commission (IEC), which is a worldwide organization for standardization comprising all national electrotechnical committees, the Electromagnetic Emission (EME) is the phenomenon by which electromagnetic energy emanates from a source. Similarly, the IEC also describes the Electromagnetic Susceptibility (EMS) as the inability of a device, circuit or system to perform without degradation in the presence of an electromagnetic disturbance. The immunity, which represents to what extent EMI may be injected into a system before performance failures begin to occur, is complementary to the susceptibility.

The four phenomena explained above and their relationships between each other are displayed in Fig. 2. 1.

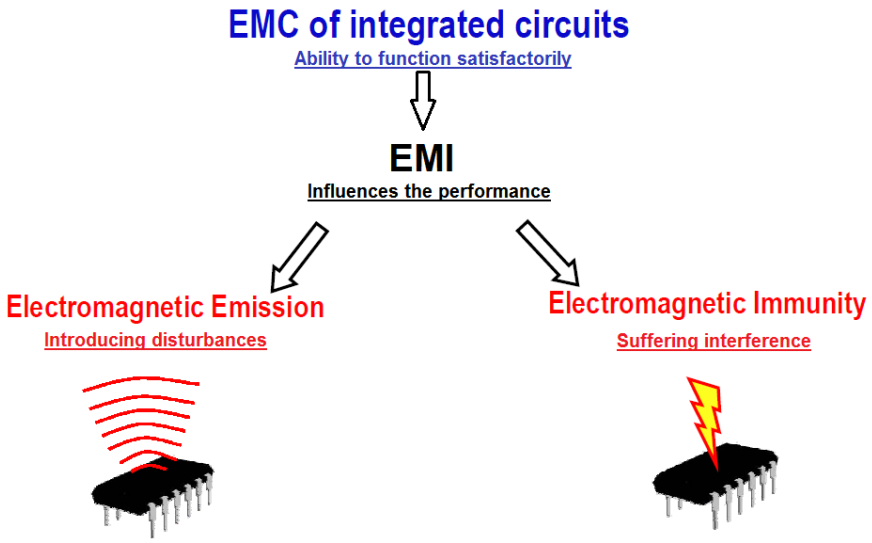


Fig. 2. 1. Commonly-used terms in EMC and their interrelationships

2.2 EMI Transmission

As discussed above, emission and susceptibility are the two constituents of EMC; furthermore, the path between them should be given special attention (Fig. 2. 2). For example, the electric motor brush arcing is one of the unwarranted EMISSIONS; and the AM radio's picking up the noise through the PATHS (power line, and/or through the air), is the unnecessary SUSCEPTIBILITY.

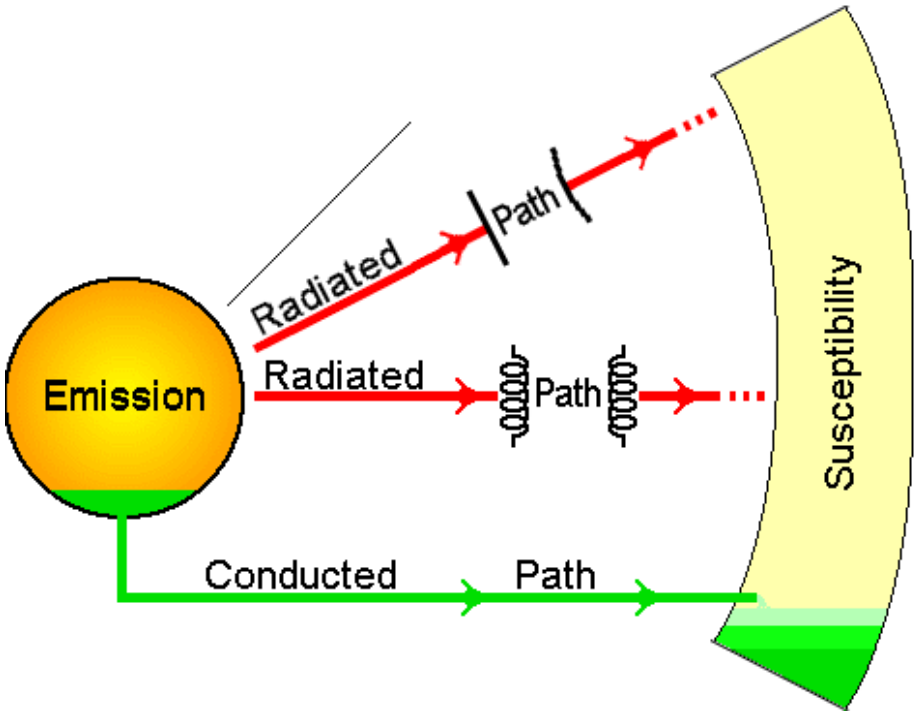


Fig. 2. 2. Block diagram of EMC paradigm

The path consists of radiated and conducted energy, which could be radiated (electromagnetic field), inductively coupled (magnetic field), capacitively coupled (electric field) (shown in Fig. 2. 3), and conducted (electric current). The radiated EMI is most often measured in the frequency range from 30MHz to 10GHz; while the conducted EMI is usually often measured in the frequency range of several kHz to 30MHz.

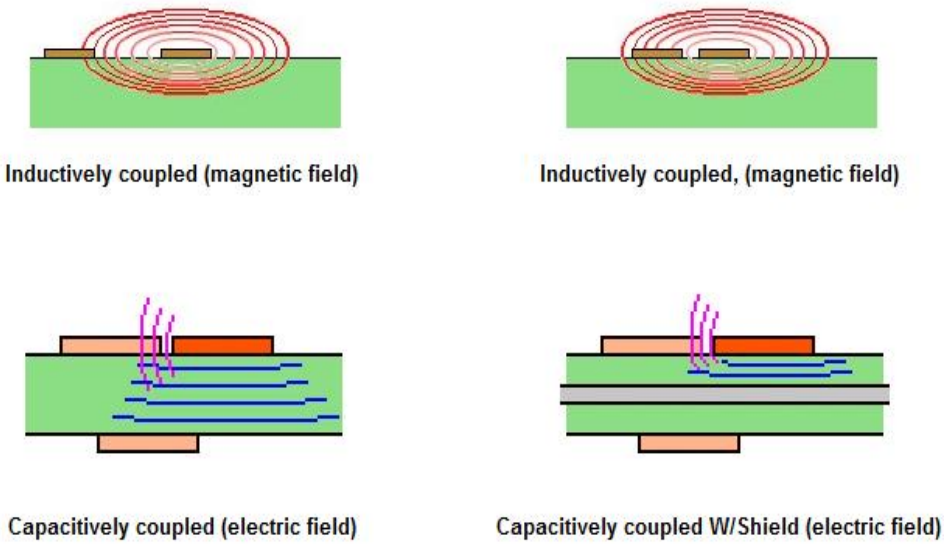


Fig. 2. 3. Inductively coupled vs. capacitively coupled

Table 2. 1 and Table 2. 2 show emission sources and susceptibility of both radiated and conducted EMI.

Table 2. 1. Emission sources and susceptibility of radiated EMI

Emission Sources	**Susceptibility**
Clocks, clock lines, data lines; switching power supplies	Clock lines & data lines poorly laid out, improperly terminated
Solutions	**Solutions**
Balanced transmission lines, proper terminations, ground planes, shielding, limited rise & fall time drivers	Shielding, layout, filtering, ground planes, differential line receivers,

Table 2. 2. Emission sources and susceptibility of conducted EMI

Emission Sources	**Susceptibility**
Power supplies (switching), power rails, motors, relays	A.C. power cord poorly filtered, power rails poorly decoupled,
Solutions	**Solutions**
Good bypassing & decoupling practices, layout, ground planes, shielding	Good bypassing & decoupling practices, layout, ground planes, shielding, power line filtering

Although it is assessed that the interfering signals might propagate mainly in these two different ways: conduction and radiation [4], [10], the former seems the most relevant way of propagation when the chip size and the working frequency range of the electronic appliances which act as EMI sources.

2.3 Integrated Circuit Susceptibility to Conducted EMI/RFI

2.3.1 EMI/RFI Effects in Integrated Active Devices

All inherently nonlinear electronic devices, when driven by a large signal, generate output signal with distortion. When continuous-wave RFI voltage is applied to the base-emitter junction of a bipolar transistor that is polarized active, the transistor quiescent operating point is varied due to the emitter current crowding and base-emitter junction rectification phenomena. After experimental evaluations of the quiescent operating point offset, it is indicated that the quiescent current level is modified; Fig. 2. 4 shows the comparison results, in which circles indicate measurement results executed in the presence of RFI and crosses represent measurements executed without interference [11].

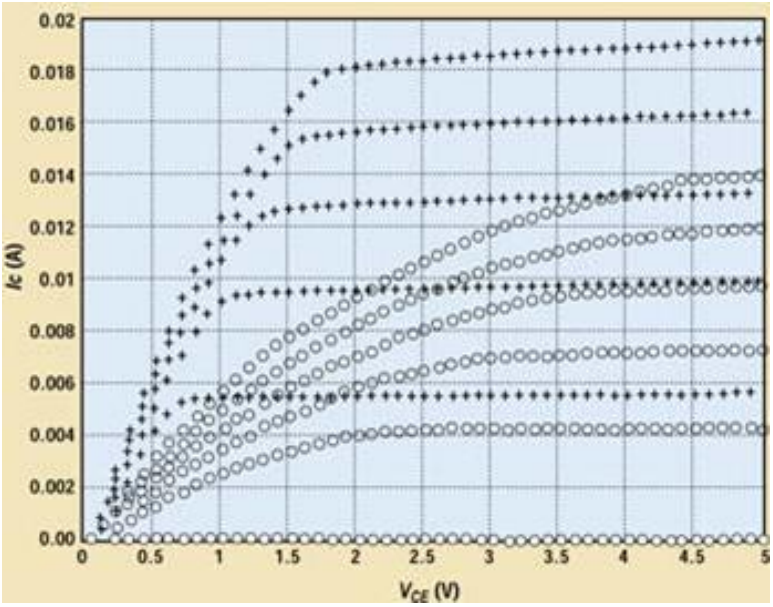


Fig. 2. 4. Experimental results of immunity tests on a bipolar transistor [11]

In order to obtain the susceptibility of MOS transistors, take advantage of the similar test setup to that is used for bipolar transistors. The experimental results of the

drain current versus the drain-to-source voltage in the same labels are displayed in Fig. 2. 5. RF disturbances on the gate-source terminals increase the mean value of the drain current. MOS transistors are more immune to EMI/RFI than bipolar transistors, because the interference results in higher variation of collector current in bipolar transistors than that of drain current in MOS transistors. In reality, because of the smoother nonlinearity, the field-effect transistors are more resistant to EMI/RFI than bipolar transistors [11].

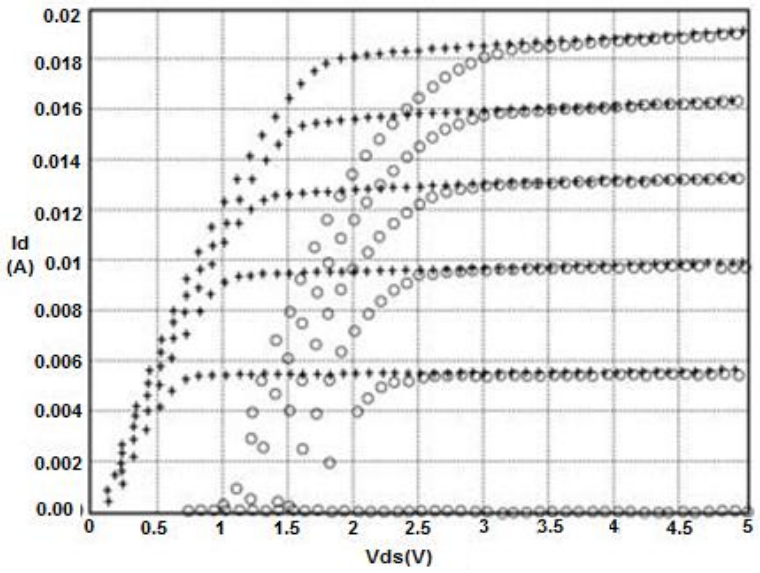


Fig. 2. 5. Experimental results of immunity tests on a MOS transistor [11]

2.3.2 Analog versus Digital Integrated Circuits

For high performance complex CMOS ICs, especially for modern integrated mixed circuits, due to fast switch of digital parts, EMI can be coupled on the terminals (e.g. supply rails), and cause failures and skews to other analog blocks of embedded system. Moreover, EMI can also affect the outside enclosure of an apparatus and be coupled through skin aperture to its interior and the resulting internal electromagnetic

fields induce unwanted voltages or current on the system cables which are conducted to the terminals of circuits and semiconductor devices [12] [13] [14].

Analog and digital circuits in complex ICs can be integrated on the same die because of the IC technology nowadays. However, analog circuits are inherently less immune to EMI than the digital counterparts, which is because of the fact that digital circuits have the nature of being resistant against small level interferences due to the characteristic of using thresholds between logic levels. Additionally, although digital integrated circuits exhibit higher immunity to EMI, they are still affected seriously in some particular cases. When EMI level is large enough to change the logic state of a digital signal and the propagation delay, digital circuits can even generate significant defects in data operation since some important bits were permanently flipped into another state. Therefore, interferences injected to complex ICs cause inter-modulation, cross-modulation, and other harmful effects which induce the circuit failures. Though generally digital circuits are very susceptible to pulsed interference, if some basic precautions are taken to minimize the EMI injection, they have better immunity to RFI compared to analog ones. Therefore, this research focuses on how to find a way to increase the immunity of the analog circuits to EMI.

2.3.3 IC Susceptibility Conclusion

In summary, analog blocks are less susceptible to conducted EMI/RFI compared to digital ones, and thus being designed with low distortion; choosing circuit topologies that account for pre-distortion and post-distortion can help achieve desired immunity. Using MOS transistors rather than bipolar transistors can obtain better performance.

Besides, operational amplifiers are analog circuit cells widely used in the design of analog and mixed-signal ICs; however, they are extremely sensitive to conducted EMI/RFI [4], [11].

2.4 Basic Features Correlated to EMI Susceptibility

2.4.1 Nonlinear Distortion

The intrinsic nonlinear behavior of active devices is a common source of EMI related problems in analog IC, particularly when a disturbance signal is generated in the frequency out of working range. Nonlinear distortion, which amounts to the distortion of the signal amplitude and to the position of spectral components, exists in nonlinear circuits. There are two different nonlinear distortion types: harmonic and intermodulation distortion. Even for the input signal is within working frequency band, DC offset problem is also inevitable for a nonlinear system.

For a memoryless, weakly nonlinear system whose input and output signals are described by the following equation: (Here y and x are the output and input of the system respectively)

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.1}$$

Assume that x is a sinusoidal EMI signal,

$$x(t) = A\cos(\omega t) \tag{2.2}$$

Then,

$$y(t) = a_0 + a_1 A\cos(\omega t) + a_2 A^2 \cos^2(\omega t) + a_3 A^3 \cos^3(\omega t) \tag{2.3}$$

$$y(t) = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \tag{2.4}$$

Therefore, when nonlinear circuits are excited with a single sinusoidal signal, the DC component deviates from the value for a linear system due to the influence of even order terms which are correlated to asymmetrical behavior; the output frequency spectrum also contains the spectral component at the fundamental frequency and other harmonic frequencies. Harmonic components from the nonlinear distortion of sinusoidal out-of-band EMI signals might appear in the signal band, so it is very hard to filter the interfering EMI harmonic components. Even worse, the induced undesirable EMI signal may additionally cause severely DC voltage shift errors on some critical node which drive some transistors out of operation region or into total cut-off, forcing the IC circuit to malfunction, [8] [15].

There is another nonlinear distortion behavior named intermodulation distortion when the EMI signal is a complex waveform consisting of multiple waves or with the desired input signal. All the sine frequency terms interfere with each other and generate intermodulation products.

Assume that the input x is the sum of two sinusoidal waves at different frequencies,

$$x(t) = A\cos(\omega_1 t) + B\cos(\omega_2 t) \tag{2.5}$$

Then,

$$y(t) = a_0 + a_1\left(A\cos(\omega_1 t) + B\cos(\omega_2 t)\right) + a_2\left(A\cos(\omega_1 t) + B\cos(\omega_2 t)\right)^2 + a_3(A\cos(\omega_1 t) + B\cos(\omega_2 t))^3 \tag{2.6}$$

The 2nd-order term is shown as follows:

$$a_2x^2(t) = \frac{1}{2}a_2(A^2 + B^2) - \frac{1}{2}a_2A^2\cos(2\omega_1 t) - \frac{1}{2}a_2B^2\cos(2\omega_2 t) - a_2AB\cos((\omega_1 + \omega_2)t) + a_2AB\cos((\omega_1 - \omega_2)t) \tag{2.7}$$

In the 2nd-order term of the output there is the dc term, the 2nd-order harmonics of both inputs and two 2nd-order intermodulation products.

The 3rd-order term is shown as follows:

$$a_3x^3(t) = a_3A^3\sin^3(\omega_1 t) + 3a_3AB^2\sin^2(\omega_2 t)\sin(\omega_1 t) + 3a_3BA^2\sin^2(\omega_1 t)\sin(\omega_2 t) + a_3B^3\sin^3(\omega_2 t) \quad (2.8)$$

The 3rd-order term of the output includes fundamental frequencies, 3rd-order harmonics and 3rd-order intermodulation products ($\omega_1 \pm 2\omega_2$ and $\omega_2 \pm 2\omega_1$). However, it can be observed that no dc component exists in the 3rd-order term; it appears due to even-order nonlinear behavior [16]. Intermodulation might mix out-of-band interference signals, and converted them into the working band, which is especially harmful. For example, when an audio amplifier picks up and demodulates the GSM signals emanating from a neighboring cell phone. Both devices work at different frequencies, but the GSM signals are still intermodulated by the nonlinearity in the audio amplifier, resulting in recognizable repetitive sound in e.g. computer speakers because of intermodulation components in the audio frequency band [8].

As discussed above, the nonlinear distortion behavior has an extremely serious effect on the IC performance, especially the most detrimental dc shift phenomenon, disturbing the normal operation of the circuits, or even debiasing them completely. Since the dc shifting is a dc effect, it might be impossible to filter it when it has already taken place. Therefore, it is useful to filter the EMI disturbance before it reaches and interferes with the sensitive and nonlinear circuit nodes, which is a linear way; additionally, if the circuit's bandwidth can be increased to be larger than the most significant EMI induced harmonics and intermodulation terms (which is difficult in design phase), the dc accumulation might be minimized.

2.4.2 Asymmetric Slew Rate (SR)

When large input signals are applied at the input terminals of a specific circuit (e.g. a one-stage operational amplifier), there is a very undesirable effect: slewing. If the small-signal bandwidth of the amplifier suggests a fast time domain response, the large-signal speed is limited by the slew rate because the current which is maximally available to charge and to discharge the dominant capacitor in the circuit is not large enough [17]. Hence, there are a lot of distortions introduced during slewing and the input and output are related to each other nonlinearly. It is analyzed in the previous section that nonlinear distortions result in harmful effects including dc accumulation, which depend on the interference of even-order harmonics and intermodulation products.

Ideally, the positive and negative slew rates are equal to each other, which in other words mean the circuit is fully symmetrical, and so the resulting nonlinearity is purely odd-ordered. However in reality, the perfect SR symmetry rarely exists; asymmetrical slew rates can generate dc shift phenomenon because asymmetries cause even-order nonlinear distortion. Take the classic one-stage operational transconductance amplifier (OTA) which is connected in a unity-gain configuration as an example (Fig. 2. 6), the EMI-induced slew rate asymmetries are studied, for which the unity-gain configuration is often used during analysis due to its benefit of the highest voltage swings on the input differential pair [4]. Actually, the unity-gain setup is the main test-bench when the dc shift is necessary to evaluate, which will be explained in details in the later parts.

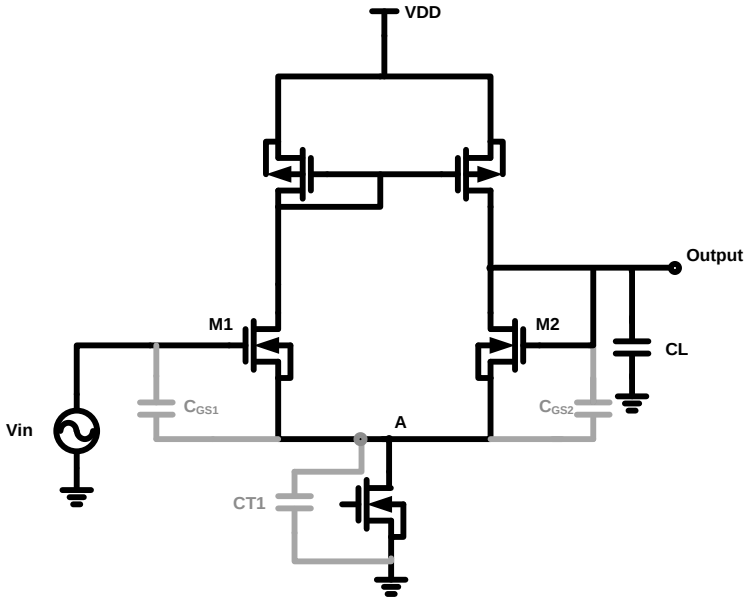


Fig. 2. 6. One-stage OTA connected as a voltage follower, with parasitic capacitors

Ideally, the positive and negative slew rates of the OTA are equal:

$$SR = SR_+ = SR_- = \frac{I_b}{C_L} \tag{2.9}$$

But practically they are never exactly the same with each other. The difference between SR_+ and SR_- mainly depend on three effects [14], [6]:

1) Charge modulation across the tail current transistor Mb. If a negative voltage step with falling time is applied at the input of the configuration, the voltage at the source of M1 decreases, forcing the tail current to a lower value owing to the channel length modulation of Mb, which is smaller than its quiescent value and used to discharge the loading capacitor CL. In contrary, a positive step applied at the input increases the voltage at the source of the input transistors, as well as the output voltage (and the gate of M2) [14].

2) Asymmetries in the topology or mismatch of the transistors. Either one causes the dominant capacitor to charge faster or slower than to discharge [14].

3) Parasitic capacitances, especially the parasitic capacitance CT coupling the sources of the input transistors M1 and M2 to ground and the gate-to-source capacitances of the input pairs [6], which will be explained more detailedly in the following section.

Therefore, the positive and negative slew rates are different from each other; the reference [14] reported that the variations are about 10% up to 20%. It has been obtained that asymmetric slew rates can generated dc shift. This effect is illustrated in Fig. 2. 7. If the output waveform has the approximately constant slope for both rising and falling transients, shown as the following dashed curve, of which the slew rates are also equal in magnitude, then the output voltage will not exhibit a DC component. However, if the magnitude of the positive slew-rate is higher than that of the negative slew rate, rising transient will be faster than the falling ones, which results in the existence of positive output offset voltage; in the same way, if SR+ is lower than SR-, the negative output offset voltage will be induced.

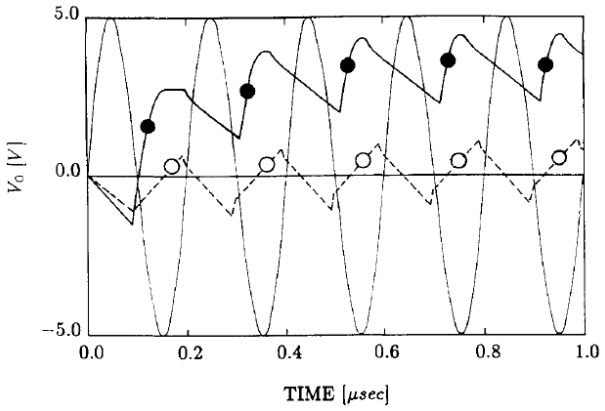


Fig. 2. 7. Transient response to a sinusoidal interfering signal for OpAmps with symmetric and asymmetric slew-rate

In order to achieve a good equality between the positive and negative slew rates, some rules had better be followed:

(1) Minimize the channel length modulation effect of the tail current transistor by increasing the channel length [14];

(2) Take advantage of fully differential circuit topologies and mirrored signal paths for high topological symmetry;

(3) Try to minimize the effect especially the parasitic capacitance across the tail current source transistor [6].

It should be noticed that the slew rate asymmetry plays a major role for low to medium EMI frequency, which is around unity frequency of the OpAmp. At very high EMI frequencies, no slew rate induced DC shift occurs, since the input signal is filtered by parasitic capacitances of input transistors which are relevant at high frequencies, and cannot be acted as large signal.

2.4.3 Parasitic Capacitance

In some reference, e.g. [14], the effect of parasitic capacitance is usually referred as the effect of strong nonlinear behavior of the input stage. When the input pair is driven by a very large EMI signal with high frequency above the amplifier's unity gain frequency, e.g. the one-stage OTA in Fig. 2-6, the parasitic capacitances of the differential transistors M1 and M2 are dominant. Additionally, the gain is very small at those high EMI frequencies, so the output is a quasi dc signal; since most of the ac drain current flows through the parasitic capacitances, so the ac drain currents of the input transistors are ignorable. Also, as load capacitor is generally much larger than parasitic

capacitance, they can be seen as shorted to ground in high frequency. Eventually, the one-stage OTA can be modeled in Fig. 2. 8.

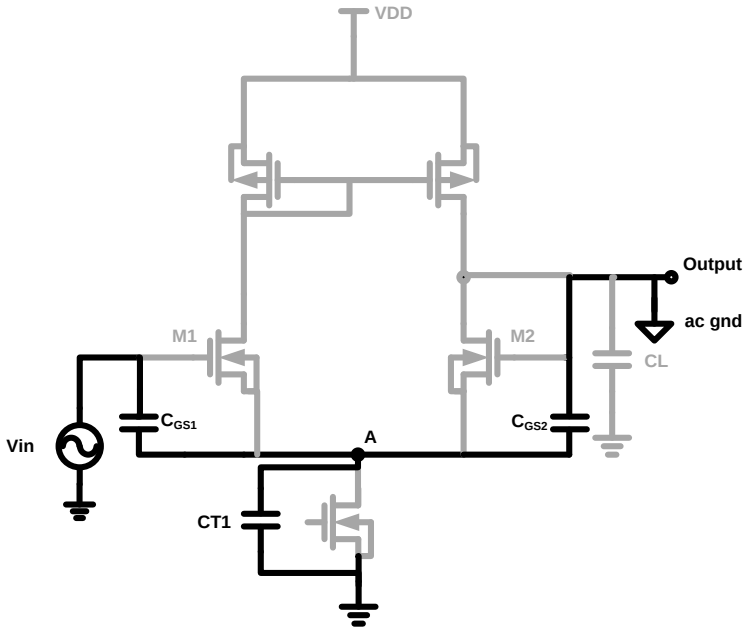


Fig. 2. 8. One-stage OTA circuit simplified at high frequency

Assume that the gate-sources capacitances of M1 and M2 are the same; it is easy to establish the gate-source voltage of M1 and M2 as follows:

$$v_{gs1}(t) = v_{in}(t)\frac{C_{gs}+C_{T1}}{2C_{gs}+C_{T1}} \tag{2.10}$$

$$v_{gs2}(t) = -v_{in}(t)\frac{C_{gs}}{2C_{gs}+C_{T1}} \tag{2.11}$$

Since $|v_{gs1}| > |v_{gs2}|$, the magnitude of the ac drain current through M1 is larger than that of M2, which means M1 is forced into cut-off longer than M2 [6], and the distortion in the drain current of M1 is larger than that of M2. Hence, the unbalanced voltages due to parasitic capacitances in high frequency range result in strong nonlinear distortions and yield dc shift phenomenon.

But the definition is very confusing sometimes, because parasitic capacitances influence the slew rates, the strong and also the weak nonlinear distortion in the input stage. When a high frequency EMI signal that does not force the transistors into cut-off is applied to the inputs, the dc offset is generated which is proportional to the scalar product of the differential and common-mode components of the EMI signal that is injected into the inputs [8]. This will be described in detail, and it can be derived that the weak nonlinear behavior is related to parasitic capacitances, which is the most intricate EMI effect disturbing the performance of input stage.

3. EMI SUSCEPTIBILITY VERSUS NONLINEARITY AND ASYSMMETRY

3.1 Introduction

As has been illustrated in the previous sections, nonlinearity or asymmetric slew rate is one of the origins of electromagnetic susceptibility on integrated circuits. In practice, circuits are seldom fully linear or symmetrical. It is IC designers' responsibility to make the circuits behave as linearly and symmetrically as possible. Take linearity as the example, as long as the injected signals are small, the circuits are biased in the correct operating regions, the harmonic components (as well as intermodulation products) stay below the noise floor, they can be considered as being approximately linear. Therefore, it is very important to minimize the injected EMI signal amplitude before it reaches a nonlinear circuit node. The smaller the amplitude of a signal reaching a nonlinear node, the smaller the experienced curvature of the active device and the better the linearity is [8].

In this section, several basic circuit topologies are studied to illustrate theoretical observations of EMI susceptibility versus weak nonlinearity, followed by its relationship with strong nonlinear behavior and asymmetries.

3.2 EMI Susceptibility of Different Topologies versus Weak Nonlinearity

A nonlinear circuit, which can be accurately described by the first three terms of its converging Volterra series for the applied input signal, is viewed as behaving in a weakly nonlinear way [16]. In fact, this illustration means weak nonlinearity can be described by the linear signal component with its lowest even- and odd-order distortion terms; the weak nonlinear behavior is caused by the curvature of the active devices in the saturation regions [8]. For high EMI amplitude, this is the case for strong nonlinear distortion, which is explained in the later sections.

3.2.1 Diode-connected Transistors

Take a diode-connected NMOS transistor, which is biased in strong inversion region by the current source I_{DC} shown in Fig. 3. 1, as the example; and assume that the EMI ac current i_{emi} is superposed on I_{DC}, the total current flowing through the mirror transistor I_{in} is the sum of the desired dc current and the unwanted EMI ac current.

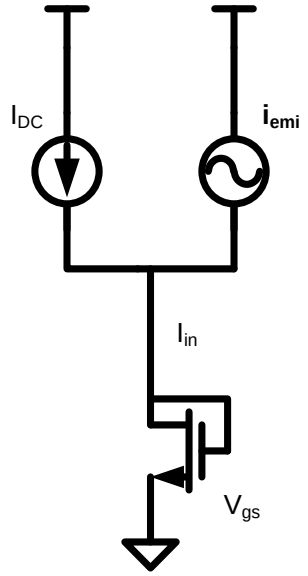


Fig. 3. 1. Diode-connected NMOS transistor

If using first-order MOS transistor formulas, the gate-source voltage is expressed by:

$$V_{GS} = \sqrt{\frac{2I_{in}}{\mu C_{ox}\frac{W}{L}}} + V_t \tag{3.1}$$

where the input current $I_{in} = I_{DC} + i_{emi} = I_{DC} + I * \sin(\omega t)$. Therefore, the gate-source voltage is:

$$V_{GS} = \sqrt{\frac{2(I_{DC}+I*\sin(\omega t))}{\mu C_{ox}\frac{W}{L}}} + V_t \tag{3.2}$$

Using Taylor series to expand the V_{GS} expression [18] if I/I_{DC} is smaller than 1,

$$V_{GS} = V_t + \sqrt{\frac{2I_{DC}}{\mu C_{ox}\frac{W}{L}}}\left(1 + \frac{I}{2I_{DC}}\sin(\omega t) - \frac{I^2}{8I_{DC}^2}\sin^2(\omega t) + \frac{I^3}{16I_{DC}^3}\sin^3(\omega t) - \cdots\right) \tag{3.3}$$

The mean value over time of the gate-source voltage is equal to [18]:

$$\overline{V_{gs}} = \lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{gs}\cdot dt = V_t + \sqrt{\frac{2I_{DC}}{\mu C_{ox}\frac{W}{L}}}\left(1 - \frac{I^2}{16I_{DC}^2} - \frac{15I^4}{1024I_{DC}^4} - \frac{105I^6}{16384I_{DC}^6} - \cdots\right) \tag{3.4}$$

Therefore, the mean value $\overline{V_{gs}}$ decreases due to the existence of EMI disturbance. The relationship of EMI effect versus nonlinearity is also represented in the visual illustration in Fig. 3. 2. Since nonlinearity can be viewed as variations of small-signal gain with input level, the dc operating point changes from A to B due to i_{emi},, thus moving the average value $\overline{V_{gs}}$ downward.

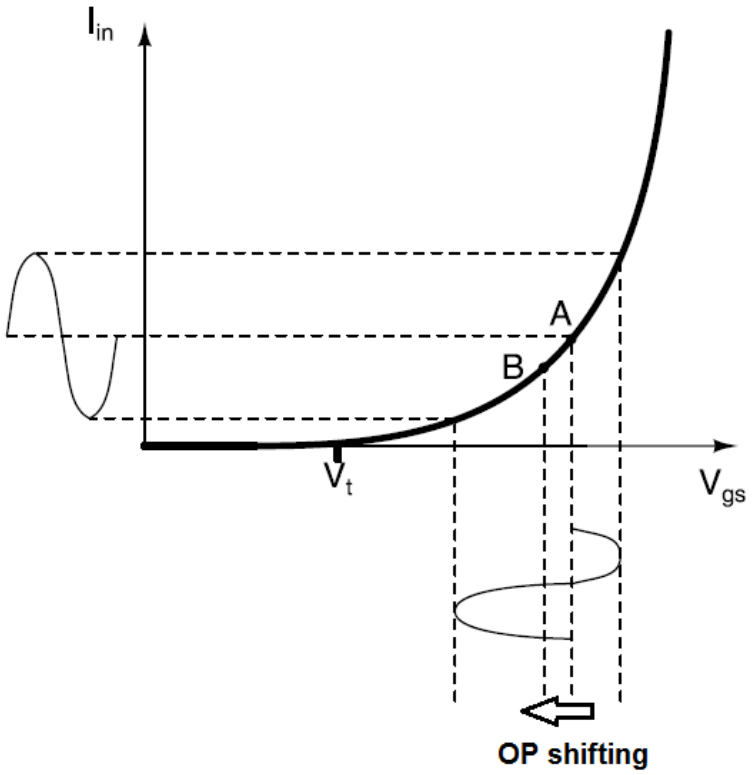


Fig. 3. 2. DC shifting of V_{gs} in diode-connected transistor

3.2.2 Current Mirror Circuits

If the diode-connected transistors are used in current mirror, the output current is disturbed by EMI. In order to block i_{emi}, decoupling and protective devices can be added externally. However, lots of applications do not tolerate the presence of such components at IC pins owing to extra cost associated to an increased bill of material or large areas, even if they could offer sufficient EMI filtering capability in the full EMI frequency range while they cannot in practice.

As an instance, if a capacitor is added at the IC pin to filter EMI, which is shown in Fig. 3. 3, the EMI signals of which the frequency is beyond the bandwidth of the current mirror are attenuated. However, the bandwidth is limited by g_m, so C has to be

sufficiently high to make the pole g_{m1}/C in small-signal analysis be smaller enough than the lowest EMI frequencies. For example, to obtain an arbitrary attenuation of at least -40dB at 1MHz, the pole should be placed below 10 KHz; if g_{m1} = 140 uS, then C is necessarily larger than 2.2 nF, which is too large to integrate. In addition, such a large decoupling capacitor may be useful at low EMI frequencies; but at high EMI frequencies, its parasitic equivalent series resistor (ESR) and inductor (ESL) cannot be ignored, it may not be effective [8].

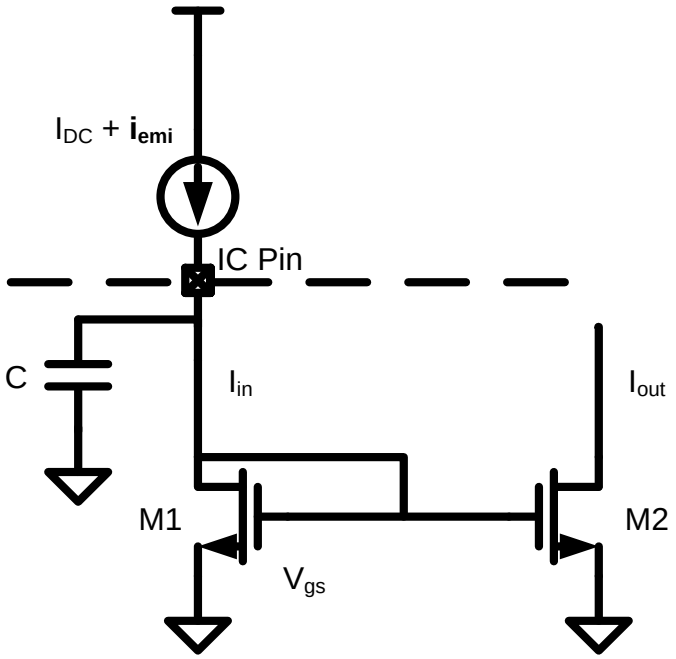


Fig. 3. 3. Current mirror with a capacitor at IC pin

As mentioned before, if the amplitude of i_{emi} is smaller than the dc bias current, weak nonlinear behavior results from small EMI signals. The average value over time of the output current from the current mirror circuit is expressed as:

$$\overline{I_{out}(t)} = \overline{I_{in}(t)} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \frac{1+\overline{\lambda V_{ds2}}}{1+\overline{\lambda V_{ds1}}} \approx \overline{I_{in}(t)} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \frac{1+\lambda V_{DS2}}{1+\lambda V_t+\lambda \sqrt{\frac{2I_{DC}}{\mu C_{ox}\frac{W}{L}}}\left(1-\frac{I^2}{16I_{DC}^2}-\cdots\right)} \tag{3.4}$$

This equation shows a negligibly small amount of DC shifting can possibly occur because of the early effect. Therefore, the output current can be yielded as:

$$I_{out} = I_{in} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = (I_{DC} + \frac{I}{I_{DC}} \sin(\omega t) I_{DC}) \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \quad (3.5)$$

If an external coupling capacitor is added, the output current during weak nonlinear operation is:

$$I_{out} = I_{in} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = (I_{DC} + \frac{I}{I_{DC}} H(j\omega) \sin(\omega t) I_{DC}) \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \quad (3.6)$$

where $H(s) = \frac{g_{m2}/g_{m1}}{1+\frac{sC}{g_{m1}}}$.

The EMI signal which flows through the diode-connected transistor and thus being coupled to the output, is attenuated by |H(jw)|, and hereby improving the EMI amplitude boundary between the weak and strong nonlinear region; but the capacitor value is supposed to be large.

According to the above analysis, since the current mirror is susceptible to EMI signals which are coupled at IC input pins, external capacitors are either too large or ineffective at specific EMI frequencies, protection or filtering must be used internally in order to reduce the effect of such interfering disturbances, for example, by reducing the current mirror circuit bandwidth below the smallest EMI frequencies.

A seemingly possible method shown in Fig. 3.4 is to add a low-pass RC filter in the mirror node, generating the cut-off frequency significantly lower than the EMI frequencies; its advantage is that the value of C can be small and the resistor does not load the input node.

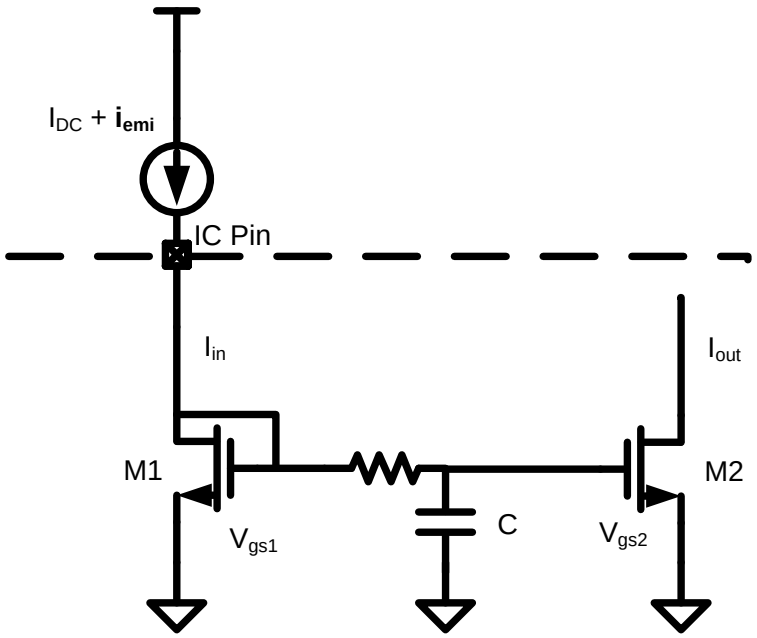


Fig. 3. 4. Current mirror with RC LPF between transistor gates

If the interference i_{emi} is modeled as a sinusoidal wave, from the small-signal point of view, the output current I_{out} is:

$$I_{out} = I_{in} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = (I_{DC} + \frac{I}{I_{DC}} H_1(j\omega)\sin(\omega t) I_{DC}) \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \quad (3.7)$$

where $H_1(s) = \frac{g_{m2}/g_{m1}}{1+sRC}$. Compared to the equation (3.6), the current expression shows that this topology has a better EMI filtering result with a much smaller capacitor because R can be made much larger than $1/g_m$ easily. However, according to (3.3) & (3.4), the voltage in the mirror node is a nonlinear function of the input current, and consequently the nonlinear distortion generates dc shifting, harmonics and intermodulation products, the linear RC filtering results in accumulation. Especially the dc shift phenomenon may drive the current mirror into the wrong operating region and thereby lowering the mean

output current value. As long as the EMI frequencies lie above the RC cut-off frequency, V_{gs2} is approximately equal to the average dc value of V_{gs1}.

$$V_{gs2} = \overline{V_{gs1}} = V_t + \sqrt{\frac{2I_{DC}}{\mu C_{ox}\frac{W}{L}}}\left(1 - \frac{I^2}{16I_{DC}^2} - \frac{15I^4}{1024I_{DC}^4} - \frac{105I^6}{16384I_{DC}^6} - \cdots\right) \tag{3.8}$$

Then the mean value of the output current can yield:

$$\overline{I_{out}} = I_{DC}\frac{W_2/L_2}{W_1/L_1}\left(1 - \frac{I^2}{16I_{DC}^2} - \frac{15I^4}{1024I_{DC}^4} - \frac{105I^6}{16384I_{DC}^6} - \cdots\right) \tag{3.9}$$

The average output current is not equal to the original output current without EMI due to the existence of additional terms as functions of I/I_{DC}. Fig. 3. 5 shows the detrimental nonlinear effect of EMI on the dc shift [8]. When the amplitude of the disturbance signals is larger than the nominal bias current of 10 uA (e.g. 15 uA and 20 uA), strong nonlinear effects happen, which lead to much worse DC shifting.

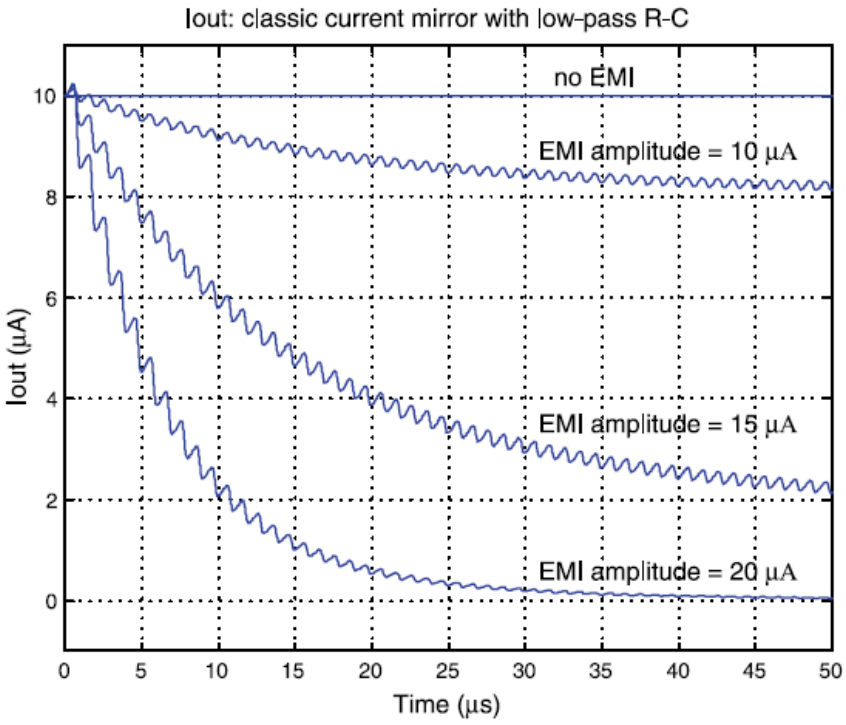


Fig. 3. 5. Current mirror with RC LPF between transistor gates

In the previous solution the EMI current flows through the diode-connected transistor without any attenuation, the circuit would be driven into the strongly nonlinear region if I/I_{DC} is smaller than 1, where I is the amplitude of the EMI amplitude. Another internal filtering approach is to add a low-pass RC filter in the way shown in Fig. 3. 6.

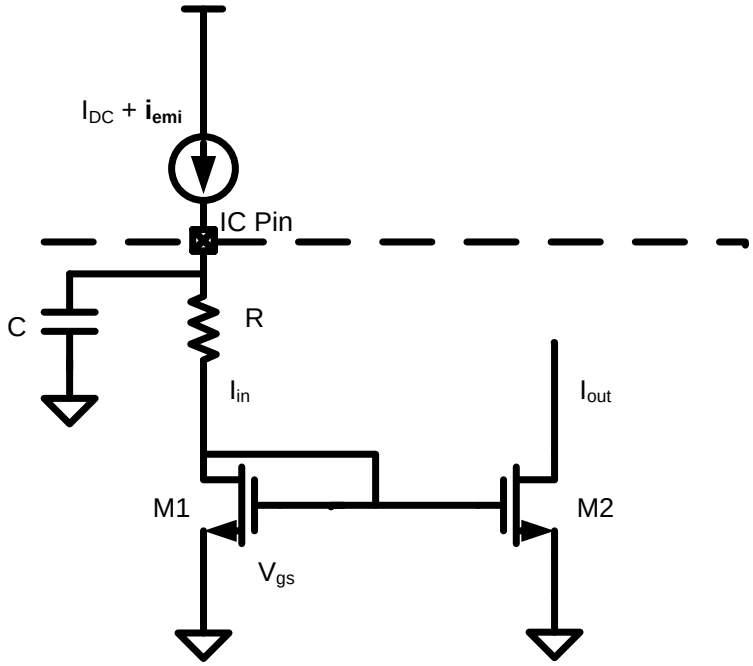


Fig. 3. 6. Current mirror with RC LPF in series with the diode-connected transistor

The corresponding output current is expressed as follows:

$$I_{out} = I_{in} \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = (I_{DC} + \frac{I}{I_{DC}} H_3(j\omega)\sin(\omega t) I_{DC}) \cdot \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \tag{3.10}$$

where $H_3(s) = \frac{g_{m2}/g_{m1}}{1+s(RC+\frac{C}{g_{m1}})}$.

Its extra advantage compared to the circuit in Fig. 3. 4 is that DC shift is significantly suppressed because the EMI filtering happens before the interference reaches the nonlinear node; however, the main disadvantage is the voltage headroom reduction due to the resistor R, especially in low voltage applications.

To sum up, these previous basic circuits help to clarify and analyze the relationship between EMI issues and weakly nonlinear behavior in analog integrated circuits: the diode-connected transistor circuit introduced the DC shifting effect and its relation with weak nonlinearity; the different current mirror circuits derive the EMI issues mathematically. From this section, it is apparent that even very small and basic analog circuits can operate uncertainly once the EMI disturbance reaches the internal circuit nodes, mixes with the desired inputs and generates nonlinear distortion in those nodes.

3.3 EMI Effect versus Strong Nonlinearity

In the previous section, weak nonlinearity which takes place as long as the transistors that EMI disturbance is injected into are biased in the saturation region at all times, has been illustrated in details. While for high EMI amplitude signals, active devices are switched off and strong nonlinear behavior is generated, which was shown in Fig. 3. 5. This effect is often viewed as the "effect of parasitic capacitances" in ref [14], which is very confusing because parasitic capacitances affect the slew rate and the strongly- and weakly-nonlinear distortions in the input stage.

Take the basic one-stage OTA in unity-gain configuration as the example, which is shown in Fig. 3. 7. At frequencies above the bandwidth of the amplifier in voltage-follower connection, the parasitic capacitances of the input transistors are dominant. Assume that the gate-source capacitances of M1 and M2 are the same, i.e. $C_{gs1} = C_{gs2} = C_{gs}$.

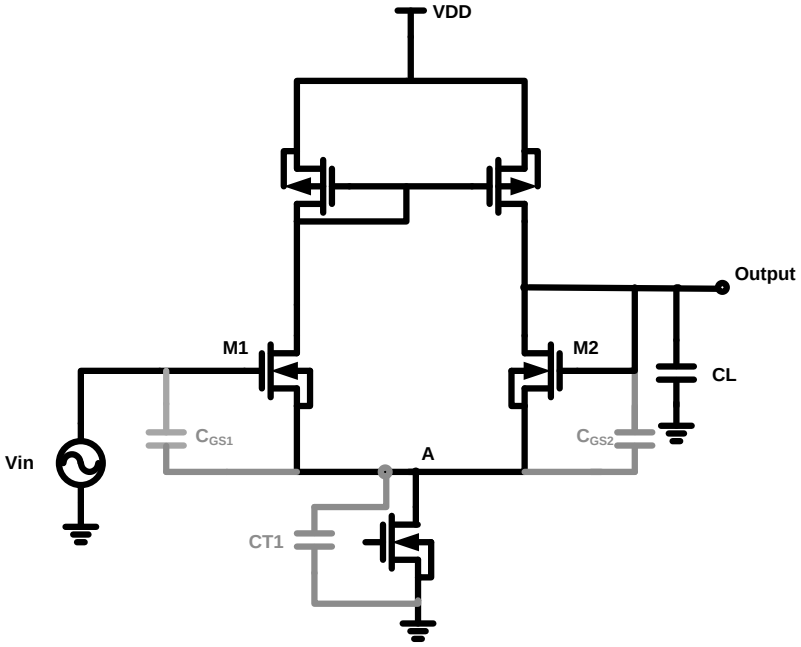


Fig. 3. 7. Basic one-stage OTA connected in a voltage follower configuration

Therefore, M1 and M2 conduct much less AC drain current if considering the AC coupling effect of parasitic capacitances. In addition, as load capacitor is generally much larger than parasitic capacitance, they can be regarded as AC shorted to ground in high frequencies. Eventually, the one-stage OTA is simplified in Fig. 3. 8.

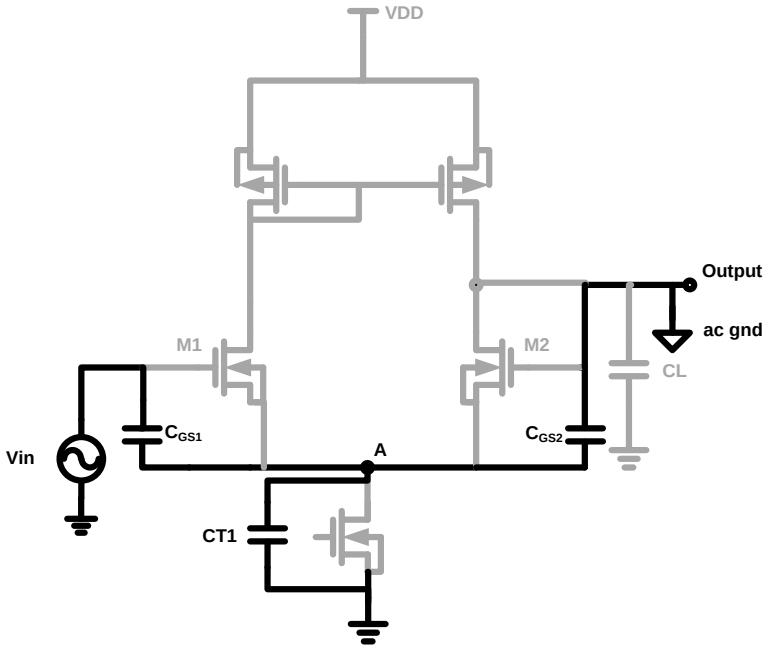


Fig. 3. 8. One-stage OTA circuit simplified at high EMI frequencies

Hence, in terms of capacitance dividing law, the gate-source voltage of M1 and M2 are approximated as follows:

$$v_{gs1}(t) = v_{in}(t)\frac{C_{gs}+C_T}{2C_{gs}+C_T} \tag{3.11}$$

$$v_{gs2}(t) = -v_{in}(t)\frac{C_{gs}}{2C_{gs}+C_T} \tag{3.12}$$

The previous relationship shows signs of unequal gate-source voltages due to parasitic capacitances during high EMI frequency range. The voltage difference results in larger magnitudes of AC drain currents flowing through M1 than that of M2, which means a large sinusoidal input voltage vin(t) drives M1 into cut-off region for longer time than M2 [6], and the strongly nonlinear distortion in the drain current of M1 is larger than that in M2. The DC shift at the output node equivalently converges to a value which is characterized by the DC mean value of the gate-source voltages of M1 and M2, which are functions of C_{gs} and C_T. Therefore, in order to suppress the strong nonlinearity effect, the parasitic capacitance C_T should be minimized and the gate-source capacitances C_{gs} increased.

From another point of view, when the input transistors are driven by high-amplitude disturbance signal, especially with frequencies lying well above the amplifier's unity-gain bandwidth, the circuit exhibits asymmetrical behavior which yields DC shifting at the output. It means that strong nonlinearity overlaps with the theoretical effects of asymmetric slew rates, as is explained analytically in the next section. If the high-amplitude EMI signal has very high frequency, the input signal is filtered by the parasitic capacitances of the input transistors with the equivalent series resistors and

inductors, which represent the weakly nonlinear behavior.

3.4 EMI Susceptibility versus Asymmetric Slew Rates

When large input signals are applied at the input terminals of some given circuits, it is necessary to take the undesirable slewing into consideration. A fast time domain response is illustrated by the small-signal bandwidth, while the large-signal speed is limited by the slew rate because the current which is maximally available to charge and to discharge the dominant capacitor in the given circuit is not sufficient [17]. Therefore, the relationship between the input and the output is nonlinearly distorted during the slewing; and especially the slew rate asymmetry can generate even-order distortion, thus causing DC voltage shift [15].

For intermediate frequencies, during a period of the interference signal, the total charge flowing through the input transistor M1 in one-stage OpAmp, e.g. that in Fig 3.7, is different from the total charge in the transistor M2, thus changing the dc voltage value on the loading capacitor and the mean value of the output voltage. In order to minimize the charge increase on C_L and compensate such effect,

$$\int_{\tau}^{\tau+T} I_{D1}(t)dt = \int_{\tau}^{\tau+T} I_{D2}(t)dt \tag{3.13}$$

where I_{D1} and I_{D2} are the drain currents of M1 and M2, and T is the period of the sinusoidal interfering signal. This equation entails that the mean value of the current flowing through M1 during the first semi-period is necessary to be equal to that forced by the tail transistor, and so is the current flowing through M2 during the second semi-period [14]. However, if a positive voltage step is applied at the input in Fig 3.7, the voltage at the source of M1 increases, which makes the tail current larger due to the

channel length modulation. This current which is used to charge the loading capacitor, is higher than the quiescent value. Conversely, when a negative voltage step applied at the input, the output voltage decreases and so does the gate voltage of M2; the tail current also decreases owing to the channel length modulation of the tail transistor [14]. Therefore, the SR+ and the SR- is not equal to each other.

Differently, the reason of high-frequency output voltage shift is mainly owed to the parasitic capacitances of the differential pair and the tail transistor. As mentioned in the previous section, the gate-source voltages of M1 and M2 are not the same, which are shown in (3.11) and (3.12).

According to the analysis, the transistors work asymmetrically, and the positive and negative slew rates are seldom perfectly equal to each other, which affects the susceptibility of the circuits to EMI signals. Detailed analyses for opamps have been developed describing analytically the divergences between positive and negative slew rate, e.g. in two-stage Miller opamps as in [19]. In order to obtain a good correspondence between the positive and negative slew rates, increasing the channel length of the tail current transistor is available for minimizing the channel length modulation; minimizing the parasitic capacitances of the input differential pair, especially the parasitic capacitance across the tail current source transistor is also useful.

Finally, the slew rate asymmetry plays a key role during low to medium EMI frequencies around the unity gain frequency of the OpAmp, which has been certified with measurements and calculations in [4] and [14]. At really high EMI frequencies, no slew rate induced DC voltage shift happens, because the input signal is filtered or attenuated by the parasitic capacitances of the input differential pair [8].

3.5 Summary

Operational Amplifiers are one of the first analog integrated circuit blocks of which EMI susceptibility has been analyzed, measured and reported in many papers, but misconceptions still exist concerning the immunity to EMI which is injected into the input terminals, as well as possible countermeasures and circuit improvements, for example, many publications describe and focus on one immunity aspect of the opamps without considering the other. This fact is even more complicated by proposed design methods which were studied for solving one issue but which sometimes turned out to be effective against the other one. Take asymmetric slew rates as the example, avoiding slew rate asymmetries was effective against the nonlinearity of the input stage [20]. This matter is desirable when improving the design topologies, while it complicates the accurate understanding of the EMI effect of the global circuit. [8]

4. EMI SUSCEPTIBILITY OF DIFFERENT STRUCTURES

4.1 Introduction

In this section the EMI susceptibility of different transistor structures and existing techniques are analyzed and compared to each other in terms of EMI-Induced input offset voltage and other important specifications such as current consumption. The effects are discussed in relation to the most significant phenomenon here, which is the weak nonlinear behavior of the input pairs to which a high-frequency EMI signal is conveyed and when it does not force the circuit into cut-off operation.

Take a conventional differential pair as an example in Fig. 4.1, it is induced that the DC offset is proportional to the scalar product of the differential and common-mode EMI disturbance component of the EMI signal that is injected into the input transistors [8].

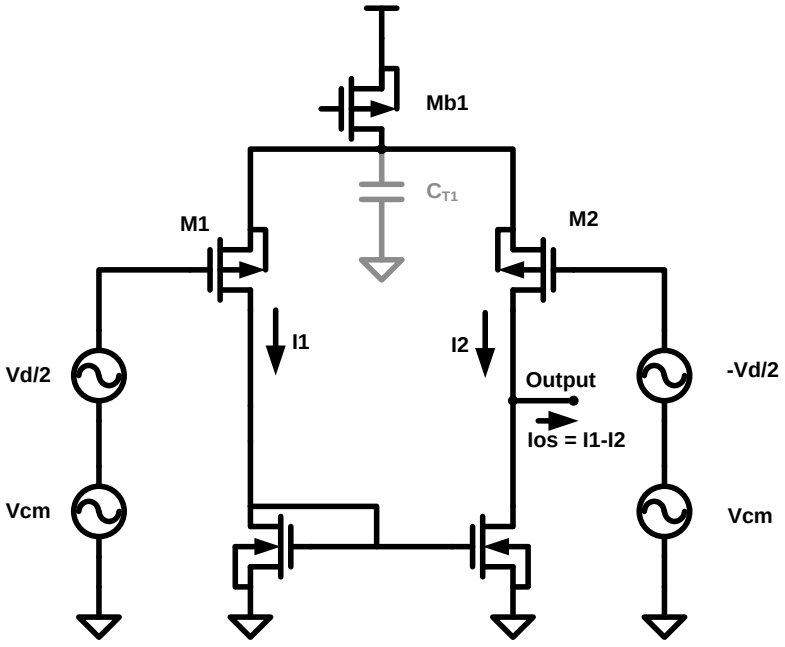
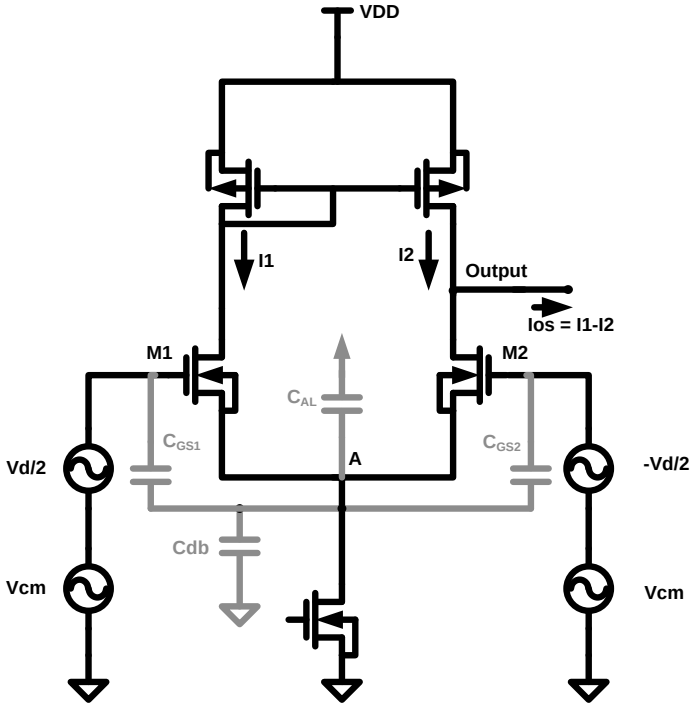
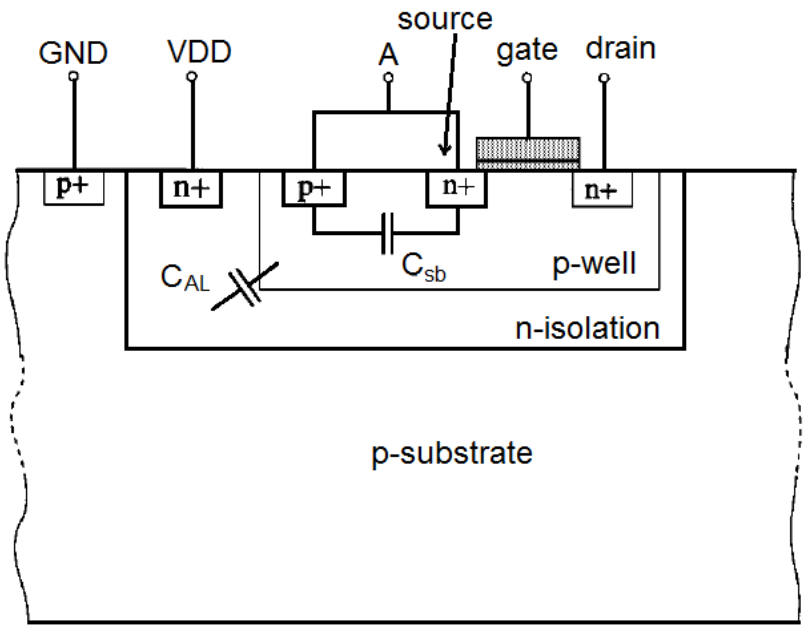


Fig. 4. 1. Conventional differential pair

When a high-frequency EMI signal is coupled to the input terminals, the output impedance of the tail current source becomes finite, which includes the parasitic capacitance between the sources of the input transistors and ground and the output resistance of the transistor Mb1. During the analysis of EMI effects, the latter is neglected. The former comprises the parasitic drain-bulk capacitance of Mb1, and the parasitic junction capacitance: if NMOS transistors are used, the junction capacitance is C_{AL} between the bulk and the isolating well of input transistors in twin-tub CMOS process in Fig. 4.2 (a) & (b); if PMOS transistors are used, the parasitic junction capacitance is C_{GND} between the substrate and the isolating well of the input transistors in Fig. 4.3 [21]. The parasitic junction capacitance can be removed by connecting the bulk of the input transistors to the substrate, which increases the threshold voltage; moreover, the substrate noise impacts the normal operation of the transistors through the body effect and varies the threshold voltage together with the bulk transconductance [22]. Besides, there is another important EMI phenomenon related to NMOS and PMOS, which is the positive EMI-induced offset voltage for NMOS input differential pair and negative one for PMOS in general cases if the current flowing out of the output node is viewed as the positive direction.



(a) NMOS differential pair including parasitic capacitances



(b) NMOS transistor cross-section including parasitic capacitances

Fig. 4. 2. Parasitic capacitances of NMOS transistor

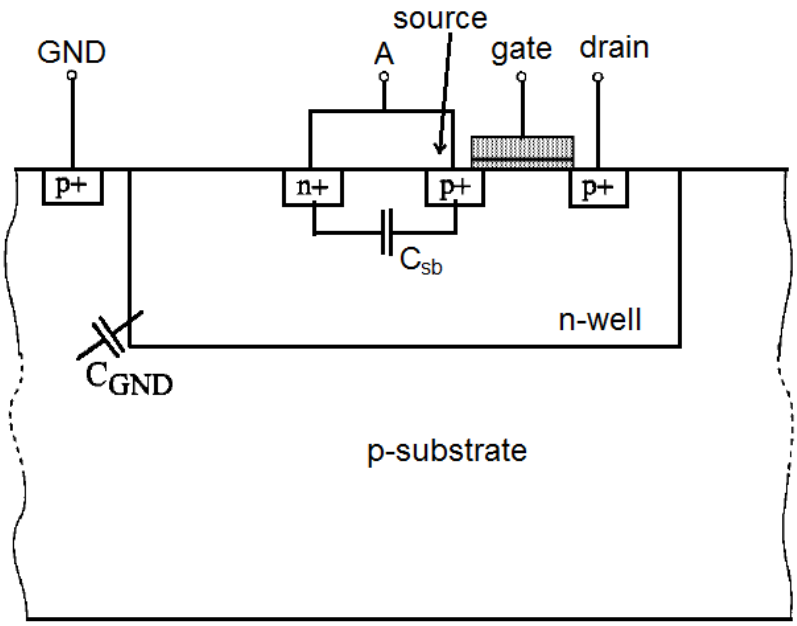


Fig. 4. 3 PMOS transistor cross-section including parasitic capacitances

Therefore, the output DC shift is generated, which is derived mathematically as follows. In the analysis of weak nonlinear input transistors, the expressions for saturation operation are used. The input offset voltage is expressed as the ratio of the output offset current and trans-conductance of input transistors, and the offset current is the difference of the current flowing through M1 and M2:

$$V_{OS} = I_{OS}/g_{m1} \tag{4.1}$$

$$I_{OS} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[\overline{(V_{gs1} - V_T)^2} - \overline{(V_{gs2} - V_T)^2}\right] = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[\overline{v_{gs1}{}^2} - \overline{v_{gs2}{}^2}\right] \tag{4.2}$$

According to the Parseval identity for Fourier integrals states that the total energy contained in a transient waveform summed across all of time is equal to the total energy of the waveform's Fourier transform summed across all of its frequency components [23] [24] [25].

$$\overline{v_{gsi}{}^2(t)} = \lim_{T\to\infty}\int_{-T/2}^{T/2} v_{gsi}{}^2(t)dt = \int_{-\infty}^{\infty} |V_{gsi}(j\omega)|^2 d\omega \tag{4.3}$$

$$I_{OS} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[\int_{-\infty}^{\infty}|V_{gs1}(j\omega)|^2 d\omega - \int_{-\infty}^{\infty}|V_{gs2}(j\omega)|^2 d\omega\right] \quad (4.4)$$

The next step is to compute $V_{gs}(j\omega)$, which is decomposed of the terms related to common mode and differential mode input voltages in Fig. 4. 4.

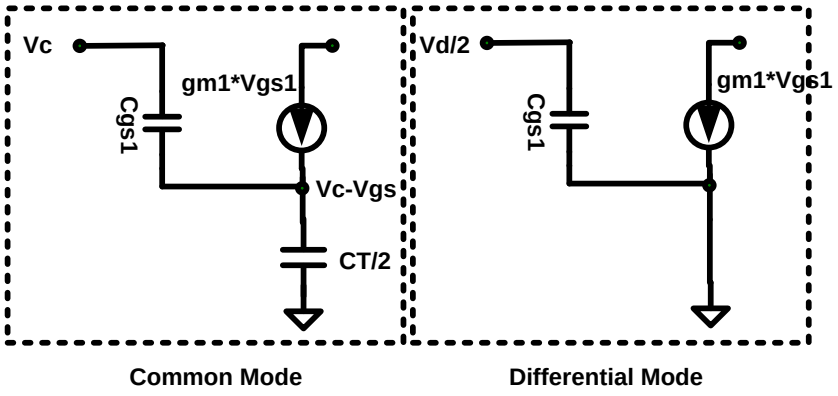


Fig. 4. 4. Small signal model circuit for common-mode & differential-mode signals

The transfer functions for common-mode and differential-mode signals are expressed as below, provided that M1 and M2 are matched with each other perfectly:

$$H_c(j\omega) = \frac{j\omega C_T}{2g_{m1}+j\omega(C_T+2C_{gs1})} \quad (4.5)$$

$$H_d(j\omega) = 1 \quad (4.6)$$

The gate-source voltage expressions of M1 and M2 are:

$$V_{gs1}(j\omega) = H_c(j\omega)V_c(j\omega) + H_d(j\omega)\frac{V_d(j\omega)}{2} \quad (4.7)$$

$$V_{gs2}(j\omega) = H_c(j\omega)V_c(j\omega) - H_d(j\omega)\frac{V_d(j\omega)}{2} \quad (4.8)$$

The input offset voltage of one-stage OTA can be rewritten as:

$$V_{OS} = \frac{I_{OS}}{g_{m1}} = \frac{2\beta}{g_{m1}}\int_{-\infty}^{\infty}|H_c(j\omega)V_c(j\omega)V_d(j\omega)|\cos\Phi d\omega \quad (4.9)$$

where:

$$\beta = \frac{\mu C_{ox}}{2}\frac{W}{L} \quad (4.10)$$

$$\Phi = \tan^{-1} \frac{\mathrm{Im}\{H_{cm}(j\omega)\cdot V_{cm}(j\omega)\cdot V_{dm}(j\omega)\}}{\mathrm{Re}\{H_{cm}(j\omega)\cdot V_{cm}(j\omega)\cdot V_{dm}(j\omega)\}} \quad (4.11)$$

Therefore, in order to decrease the input offset voltage owing to EMI effect, larger overdrive voltage should be satisfied. However, the offset caused by mismatch is increased with large overdrive voltage, so it is difficult to get an optimum value using (V_{gs}-V_t) as the design parameter. The offset current can also be decreased by increasing the gate-to-source capacitances of the input transistors, and by decreasing C_{T1}. According to (4.5), and (4.9), moreover, it is necessary to notice that PMOS is more sensitive to the EMI effect than NMOS with the same effective g_m and bias current, owing to the smaller mobility and thus larger parasitic capacitances.

According to the mathematical illustration above, some design solutions were reported for EMI susceptibility. It is necessary to clarify and summarize effective transistor topologies and circuit techniques for superior EMI performance. Hence, EMI susceptibility of basic circuit connections and existing techniques will be described in details in the following sections, for purpose of proposing robust circuit designs.

4.2 Conventional Differential Pair Using Source Degeneration

It is useful to compare the EMI effects when the bulk terminals of the input differential pair are connected to the substrate, the input source and another middle point such as the one between two source-degeneration resistors in Fig. 4.5. For these three cases, the drain-bulk capacitance of Mb1 in Fig. 4.1 has different effects on the input offset voltage because of its relationship compared to the bulk capacitance of M1-2. Besides, g_{mb} also plays an important role in the analysis.

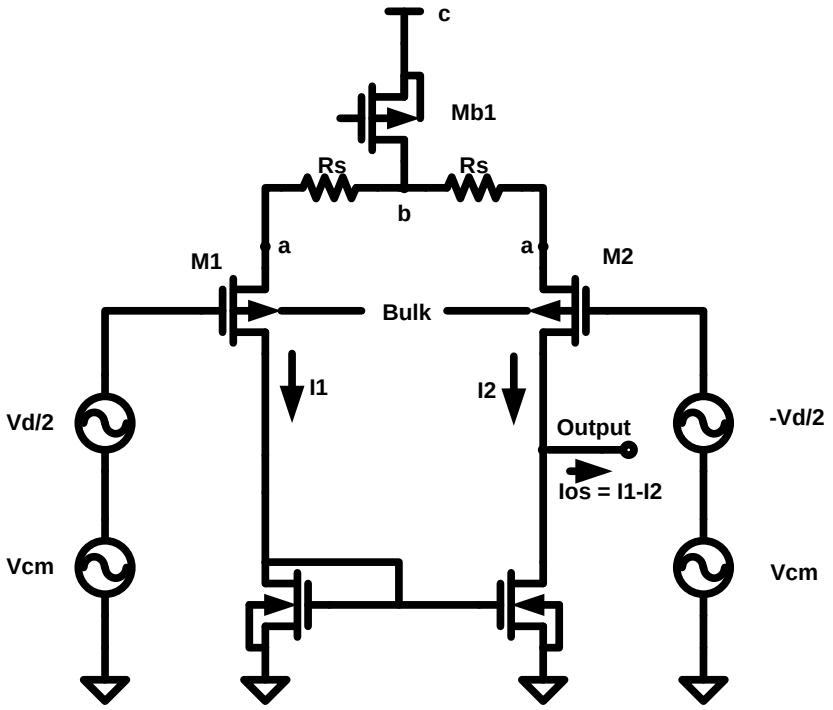


Fig. 4. 5. Bulk connected to different nodes a, b and c

When the input bulk is connected to the source (a point), the drain-bulk capacitance of C_{tail} can be neglected, compared to the much larger isolation well to substrate junction capacitance of M1 and M2. The small-signal circuit models for common mode and differential mode are shown in Fig. 4. 6:

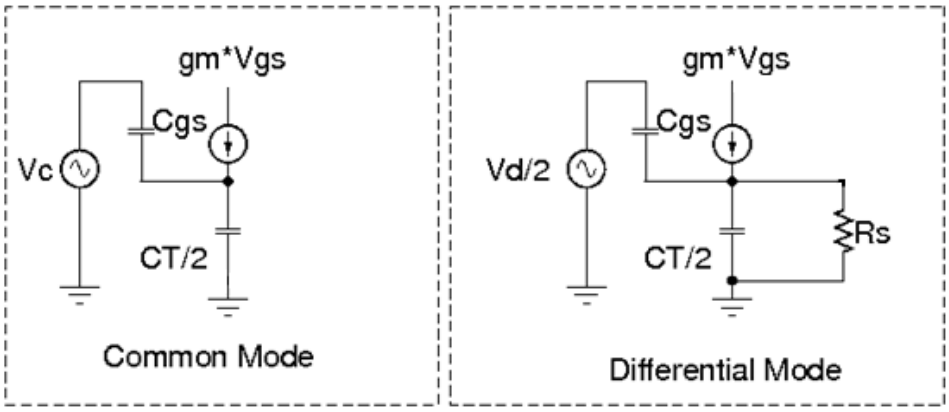


Fig. 4. 6. Small-signal mode circuits without body effect

The common mode and differential mode transfer functions are:

$$H_c(s) = \frac{sC_T}{2g_{m1} + s(C_T + 2C_{gsl})} \rightarrow |H_c(jw)| = \frac{wC_T}{\sqrt{4g_{m1}^2 + w^2(C_T + 2C_{gsl})^2}} \quad (4.12)$$

$$H_d(s) = \frac{2 + sR_sC_T}{2(1 + g_{m1}R_s) + s(2C_{gsl}R_s + C_TR_s)} \quad (4.13a)$$

$$|H_d(\infty)| \approx \frac{C_T}{2C_{gsl} + C_T} \quad (4.13b)$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{\infty}^{\infty} H_c(j\omega)V_c(j\omega)H_d(j\omega)V_d(j\omega)|\cos\varphi d\omega \quad (4.14)$$

According to (4.12), $|H_c(j\omega)|$ becomes larger with increasing interference signal frequency, which is inferior for EMI performance; $|H_d(j\omega)| < 1$, the EMI-induced input offset voltage is smaller than the one in (4.9). But at high EMI frequencies, $|H_d(j\omega)|$ is limited to $|H_d(\infty)|$. The disadvantage of this topology is the larger input referred noise because of the source resistors.

In the case with the input bulk connected to the highest level (c point), C_{T1} is mainly the parasitic drain-bulk capacitance C_{db} of transistor M_{tail}. the small-signal circuit models for common mode and differential mode are shown in Fig. 4. 7:

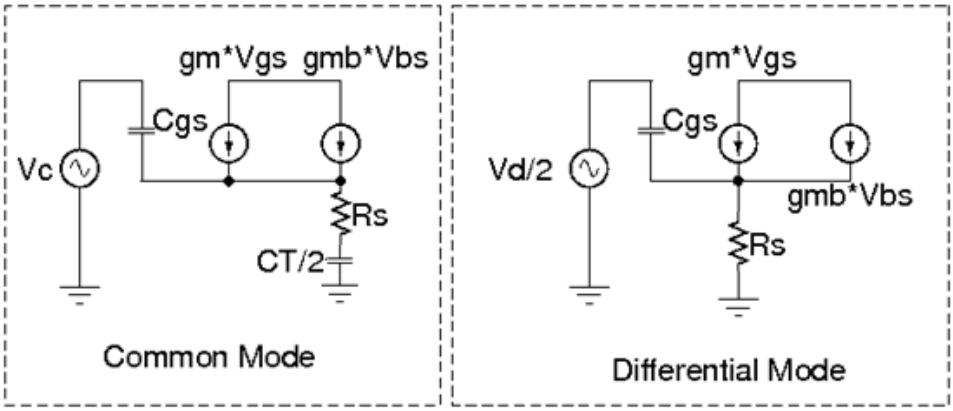


Fig. 4. 7 Small-signal mode circuits with body effect for c type

Therefore, it is easy to get the common mode and differential mode transfer function according to KCL:

$$H_c(s) = \frac{\frac{sC_{db}}{2+sR_sC_{db}} + g_{mb}}{(g_m + g_{mb}) + s(\frac{C_{db}}{2+sR_sC_{db}} + C_{gs})} \tag{4.15}$$

$$H_d(s) = \frac{1+g_{mb}R_s}{(1+g_mR_s + g_{mb}R_s) + s(C_{gs}R_s)} \tag{4.16}$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{\infty}^{\infty} H_c(j\omega)V_c(j\omega)H_d(j\omega)V_d(j\omega) \mid \cos\varphi d\omega \tag{4.17}$$

In practice, the drain-to-bulk parasitic capacitance of the tail current transistor is much smaller than the junction capacitance C_T in the case without body effect, and g_{mb} is small. At an intermediate frequency range which is around the unity-gain frequency of the amplifier which can viewed as relatively low to medium EMI frequencies, the common-mode transfer function is simplified as:

$$H_c(s) = \frac{sC_{dbl}(1+g_{mb}R_s) + 2g_{mb}}{2(g_{m1} + g_{mb}) + s(C_{dbl}(1+g_mR_s + g_{mb}R_s) + 2C_{gsl})} \tag{4.18}$$

Compare equation (4.18) to (4.12) using the extracted transistor parameters, it is clear that both magnitudes increase with EMI frequencies but (4.18) has a slower slope when the frequency increase.

The magnitudes of (4.12) and (4.18) increases until the frequency reaches a value which is high enough. The two common-mode transfer functions are rewritten respectively at the frequencies much higher than the unity-gain frequency of the circuit:

$$H_{c\_a}(s) = \frac{C_T}{C_T + 2C_{gsl}} \tag{4.19}$$

$$H_{c\_c}(s) = \frac{\frac{1}{R_s} + g_{mb}}{(g_{m1} + g_{mb} + \frac{1}{R_s}) + sC_{gs1}} \tag{4.20}$$

Therefore, the EMI-Induced input offset voltage decreases when the frequency continues to increases, and there is a maximum offset at the intermediate value which represents the worst EMI effect on the circuits.

In the circuit with the input bulk connected to the interconnecting point between the source degeneration resistors (b point), the bulk-isolation well junction capacitance of M1 and M2 and the parasitic drain-bulk capacitance C_{db} of transistor M_{tail} cannot be ignored during the analysis. The small-signal circuit models for common mode and differential mode are shown in Fig. 4.8:

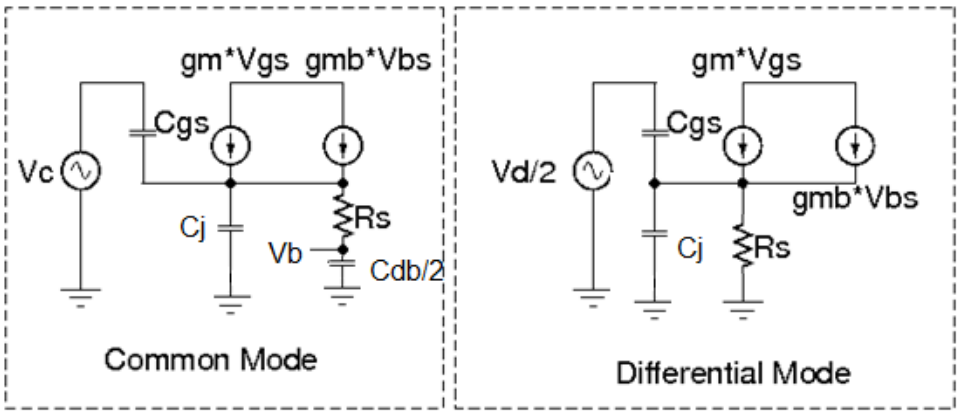


Fig. 4. 8. Small-signal mode circuits with body effect for mid-point type

$$H_c(s) = \frac{2C_j s + s(1 + R_s g_{mb})C_{db} + s^2 C_{db} C_j R_s}{2g_m + s(C_{db} + g_{mb} R_s C_{db} + g_m R_s C_{db} + 2C_{gs} + 2C_j) + s^2 C_{db}(C_j + C_{gs})R_s} \tag{4.21}$$

$$H_d(s) = \frac{1 + g_{mb} R_s + sR_s C_j}{(1 + g_{m1} R_s + g_{mb} R_s) + s(C_{gs} + C_j)R_s} \tag{4.22a}$$

$$|H_d(\infty)| = \frac{C_j}{2C_{gs} + C_j} \tag{4.22b}$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{\infty}^{\infty} H_c(j\omega) V_c(j\omega) H_d(j\omega) V_d(j\omega) |\cos\varphi d\omega \tag{4.23}$$

From the mathematical analysis, $|H_d(j\omega)|$ is smaller than 1, and at high EMI frequencies $|H_d(j\omega)|$ is limited to $|H_d(\infty)|$. At the intermediate frequency range which can be viewed as relatively low to medium EMI frequencies, the common-mode transfer function is simplified as:

$$H_c(s) = \frac{sC_{dbl}(1 + g_{mb}R_s) + s2C_j}{2(g_{m1} + sC_j) + s(C_{dbl}(1 + g_m R_s + g_{mb}R_s) + 2C_{gsl})} \tag{4.24}$$

According to the extracted transistor parameters, the junction capacitance Cj is several hundreds fF, and the unit of g_{mb} is uS, so if comparing equation (4.24) to (4.18), it is derived that the magnitude of (4.24) is smaller than that of (4.18), while both increase with EMI frequencies.

The magnitude of (4.24) also reaches a maximum value at the specific EMI frequency.

$$H_{c\_b}(s) = \frac{C_j}{C_j + 2C_{gsl}} \tag{4.25}$$

In summary, the topology with the input bulk connected to the intersection point between the source degeneration resistors has the best EMI performance when comparing the largest input offset voltage. This conclusion is proved in the simulations, which are shown in Fig. 4.9 and Table 4.1.

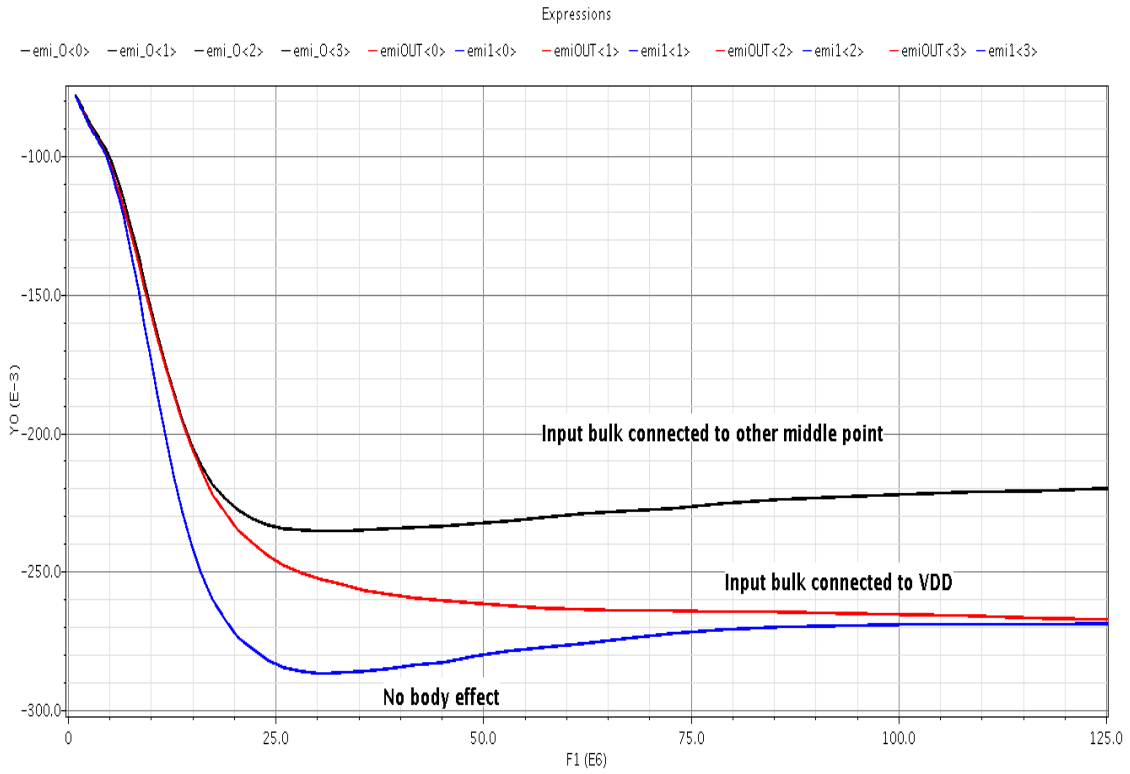


Fig. 4. 9. Offset voltage with three bulk connections throughout intermediate EMI frequency range

Table 4. 1. Input offset voltage in circuits with three bulk connections when EMI amplitude = 800mV & VDD = 3V

EMI Frequency (MHz)	**Offset in (a) Input bulk connected to source (mV)**	**Offset in (b) Input bulk connected to middle point (mV)**	**Offset in (c) Input bulk connected to VDD (mV)**
1	-78.6	-78.1	-78.55
2	-85.2	-84.1	-84.9
4	-96.1	-94.3	-95.9
8	-140.6	-129.8	-132.6

Table 4. 1. Continued

EMI Frequency (MHz)	Offset in (a) Input bulk connected to source (mV)	Offset in (b) Input bulk connected to middle point (mV)	Offset in (c) Input bulk connected to VDD (mV)
10	-173.0	-154.8	-156.5
20	-271.6	-227.5	-233.1
40	-284.2	-234.0	-258.5
80	-270.7	-224.7	-264.4
100	-268.7	-221.8	-265.1

4.3 Classic Differential Pair with RC Low-pass Filter at the Inputs

In order to suppress the EMI effect on the circuit, one effective method is to avoid the EMI sources. In Reference [26], [27], [28], the circuit is proposed with a RC low-pass filter in front of the different pair, of which the point is to reject any out-of-band common-mode and differential-mode EMI disturbances superposed on the input signal. The circuit is illustrated in Fig. 4.10.

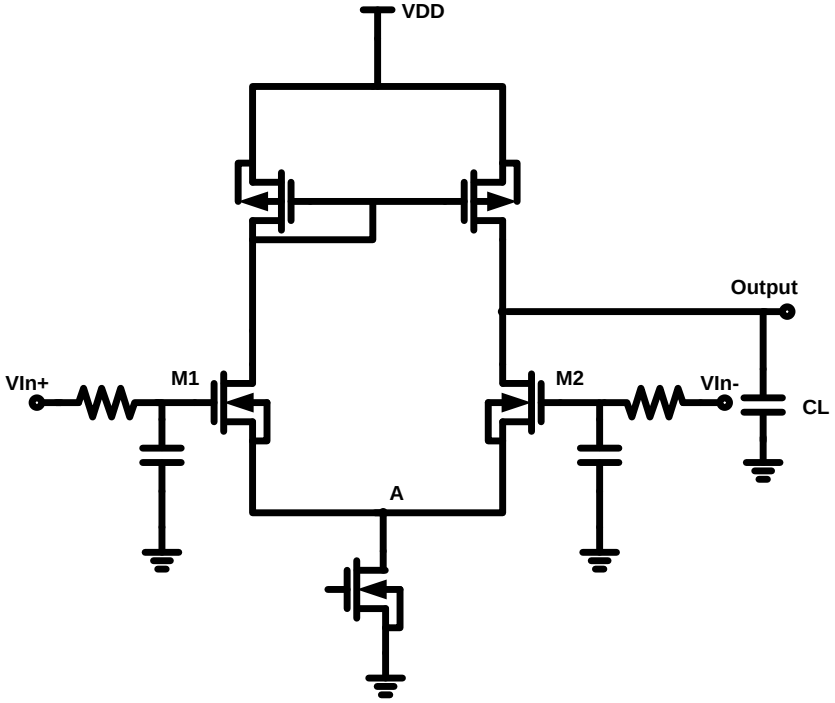


Fig. 4. 10. Differential pair with low-pass RC filter

Because the common-mode and differential-mode input voltages are attenuated before reaching the gates of the input transistor pair, the voltage swings at the gates and sources of the input transistors are smaller, which gives a more accurate small-signal approximation [26]. The input offset voltage expression is:

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{-\infty}^{\infty} \frac{|H_{cm}(j\omega)V_{cm}(j\omega)V_{dm}(j\omega)|}{|1+j\omega RC|^2} \cos\varphi d\omega \qquad (4.26)$$

where the common-mode transfer function H_c is expressed in (4.5).

Since an extra pole is introduced into the input offset voltage, there is less offset integrated over high frequency range, which generates less DC shift. This conclusion is proved from the following simulations with NMOS transistors as input pairs in three cases, which are shown in Table 4.2 and Fig. 4.11: (1) Classic differential pair without RC filters; (2) R=1KOhms, and C=1pF; (3) R=1KOhms, and C=3pF. In case 3 a larger capacitance is used to achieve the smaller cut-off frequency, thus enabling better filtering function for EMI signal at relatively lower frequency range compared to the former two cases.

Table 4. 2. Comparison of the maximum input offset voltage in three cases

	Case (1): without RC low-pass filter	Case (2): R=1KOhms, C=1pF	Case (3): R=1KOhms, C=3pF
Maximum input offset voltage (mV)	348mV	194mV	55mV

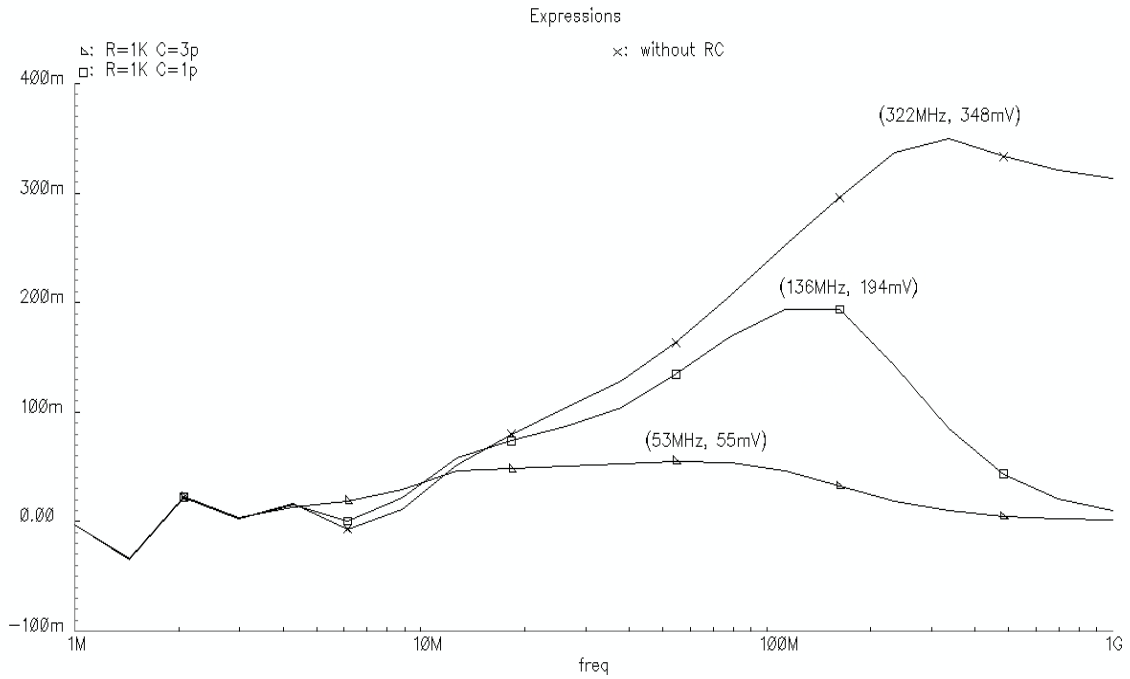


Fig. 4. 11. Offset simulations in three different cases with and without RC filters

From the simulation results above, it is obtained that the maximum input offset voltages for the three cases are 348mV, 194mV and 55mV respectively. Thus, RC implementation does successfully filter out out-of-band EMI input signal. Larger R or C can results a better filtering effect because of lower bandwidth.

However, the adoption of the RC low pass filters may modify the original input signals that are usually very weak; besides, the noise contribution which stems from the thermal noise associated with resistors is bad news for circuit design; and additionally, the presence of the filters at the input terminals of the differential pair might degrade the closed-loop stability.

4.4 Cross-coupled Differential Pair with RC High-pass Filter

In order to avoid the EMI effect, an additional differential pair can be added to generate the complimentary EMI-induced DC offset, which is used to cancel the original DC shift. In Reference [29], the circuit with a cross-coupled differential pair was proposed, which is shown in Fig. 4.12. It is composed of two differential pairs (M1-M2, M3-M4) which are cross coupled at the drains. The RC high-pass filters, of which the cut-off frequency is above the desired frequency band, couple the input signals in the pass-band to the gates of M3-M4. The offset current generated by M1-M2 is subtracted from that caused by M3-M4 by cross coupling. If the two differential pairs and RC pairs are ideally matched to each other, the resulted output offset current is free of DC shift. The theoretical input offset voltage can be calculated as:

$$V_{OS} = \frac{I_{OS_{M12}} - I_{OS_{M34}}}{g_{m1}} \tag{4.27}$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{-\infty}^{\infty} |H_{cm}(j\omega) V_{cm}(j\omega) V_{dm}(j\omega)| \left(1 - \left|\frac{j\omega RC}{1+j\omega RC}\right|^2\right) \cos\varphi \, d\omega \tag{4.28}$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{-\infty}^{\infty} \frac{|H_{cm}(j\omega) V_{cm}(j\omega) V_{dm}(j\omega)|}{|1+j\omega RC|^2} \cos\varphi \, d\omega \tag{4.29}$$

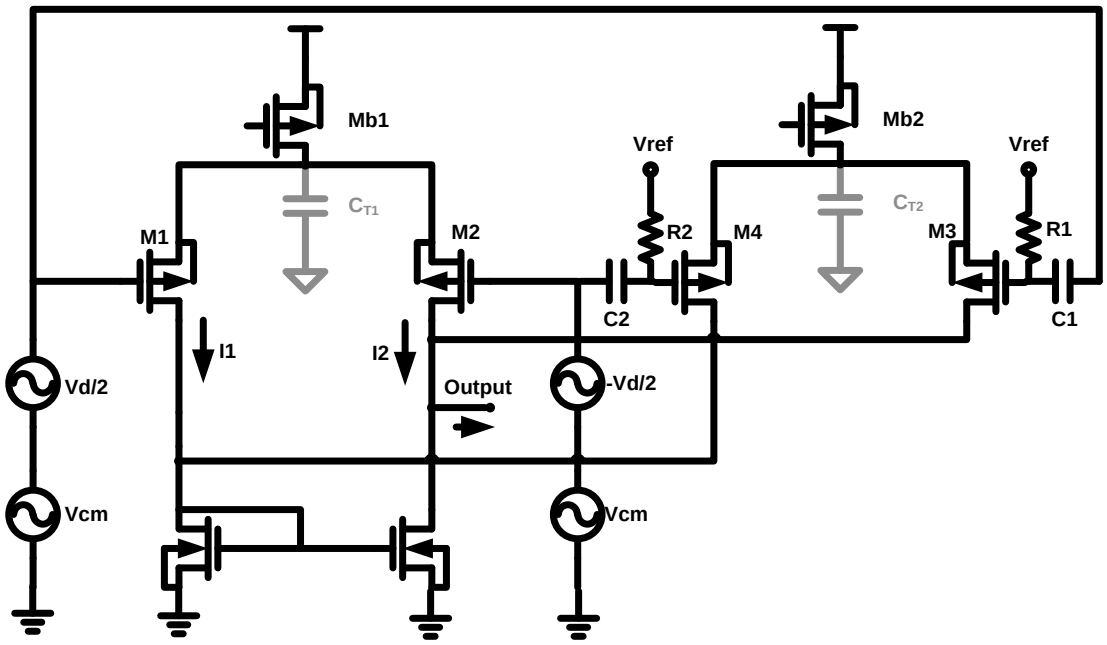


Fig. 4. 12. Cross-coupled differential pair

Similar to the differential pair with RC low-pass filter, the high-frequency EMI disturbance is filtered and V_{OS} is close to zero. The effectiveness of the cross-coupled structure can be verified by the simulation results in Fig. 4. 13 compared to the classic one in Fig. 4. 14 which is very susceptible to EMI signal. NMOS transistors are used as the input differential pairs. From Table 4.3, the maximum offset voltages for input signal of 50mV, 425mV and 800mV in the classic differential pair are 2.4mV, 182.1mV and 460.6mV, separately, while the maximum offset voltages for input signal of 50mV, 425mV and 800mV in the cross-coupled circuit are 2.76mV, 46.6mV and 78.9mV. Cross-coupled differential pair effectively reduces the EMI-induced offset, especially for high frequency range.

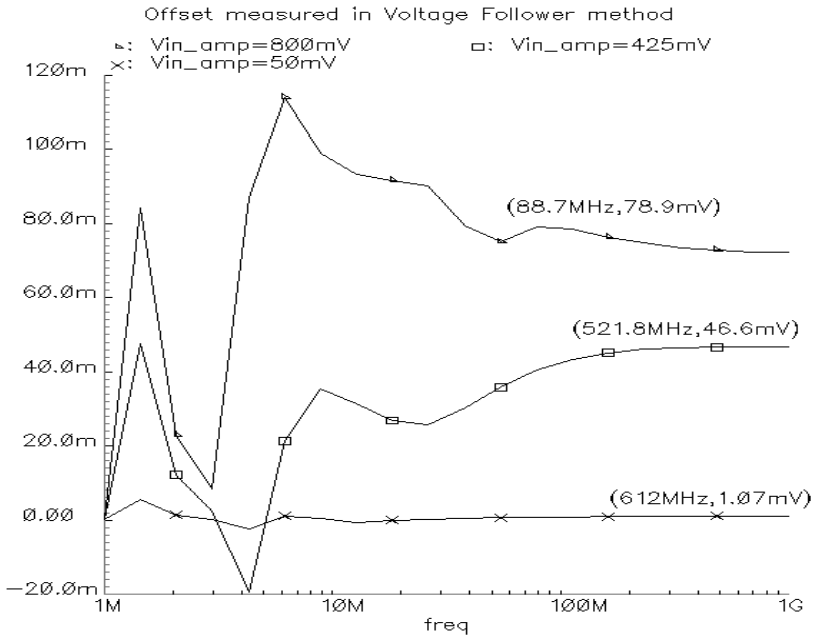


Fig. 4. 13. Offset measured for cross-coupled differential pair

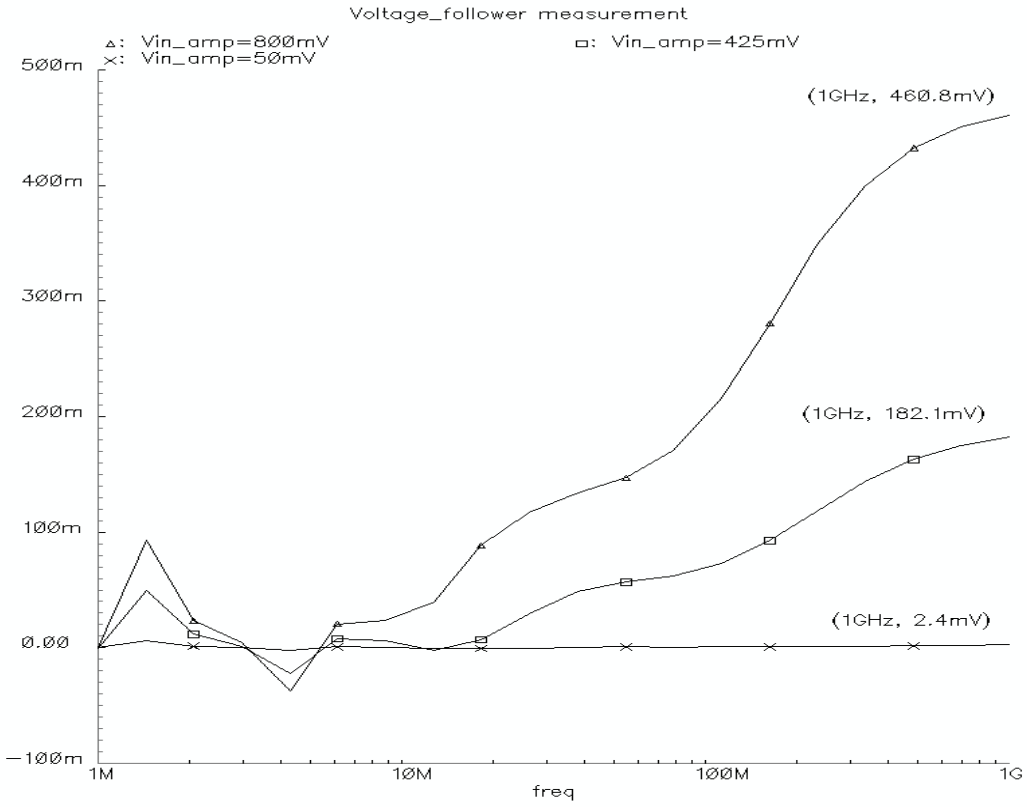


Fig. 4. 14. Offset measured for classic differential pair

Table 4. 3. Input offset voltages of classic and cross-coupled differential pairs with different EMI amplitudes

	Classic	**Cross couple**
Offset voltage (EMI Amp = 50mV)	2.4mV	2.76mV
Offset voltage (425mV)	182.1mV	46.6mV
Offset voltage (800mV)	460.6mV	78.9mV

However, the cross-coupled differential pair is susceptible to noise owing to the extra transistor pair and the resistors used in RC high pass filter; and it has large power dissipation and a larger area for the same reason. Besides, the RC filters at the inputs of the differential pair might impair its closed-loop stability. Moreover, a reference voltage V_{REF} is to bias the differential pair M3-M4, which is required to be equal to the DC bias voltage of M1-M2 for better offset compensation; most importantly, this differential-pair is very sensitive to mismatch because it is directly dependent on a perfect subtraction of generated EMI-induced offsets [8].

4.5 Source-Buffered Differential Pair without/with Source Degeneration

In Reference [30], an effective source-buffered differential pair is presented, which is referred to Fig. 4.15. The auxiliary transistors M3 and M4 back bias the input transistors M1 and M2, of which the bulk-source voltage is bootstrapped and hence the average drain current kept being constant. And the output offset current is null ideally.

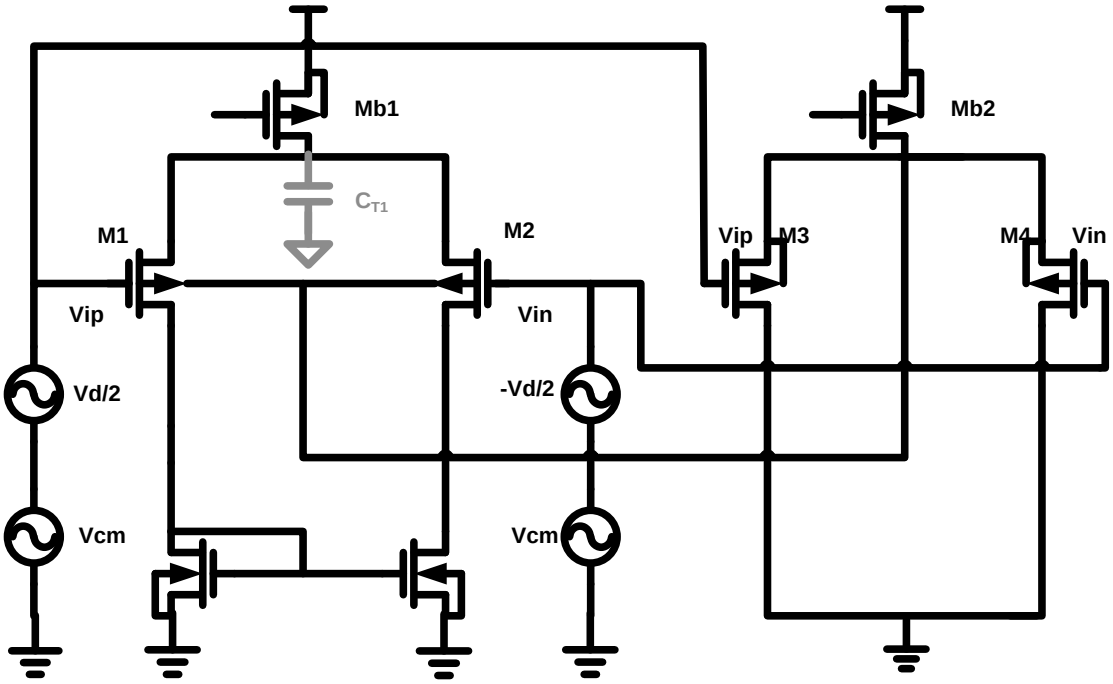


Fig. 4. 15. Source-buffered differential pair

Assume that the input pair is weakly nonlinear (most intricate EMI effect). Take advantage of the expression for transistors in saturation region:

$$I_{OS} = \frac{\mu C_{OX}}{2}\frac{W}{L}(\overline{(V_{gs1} - V_{t1})^2} - \overline{(V_{gs2} - V_{t2})^2}) \tag{4.30}$$

$$I_{OS} = \frac{\mu C_{OX}}{2}\frac{W}{L}(\overline{(V_{gs1} - V_{t0} - \gamma\sqrt{2\Phi_F + V_{sb1}} + \gamma\sqrt{2\Phi_F})^2} - \overline{(V_{gs2} - V_{t0} - \gamma\sqrt{2\Phi_F + V_{sb2}} + \gamma\sqrt{2\Phi_F})^2}) \tag{4.31}$$

If v_{sb} is much smaller than $(2\Phi_F+V_{sb})$, a first Taylor expansion can be used to expand (4.31) [30]:

$$I_{OS}=\frac{\mu C_{OX}}{2}\frac{W}{L}\left(\left(v_{gs1}-\gamma\sqrt{2\Phi_F+V_{SB1}}-\frac{\gamma\cdot v_{sb1}}{2\sqrt{2\Phi_F+V_{SB1}}}\right)^2-\left(v_{gs2}-\gamma\sqrt{2\Phi_F+V_{SB2}}-\frac{\gamma\cdot v_{sb2}}{2\sqrt{2\Phi_F+V_{SB2}}}\right)^2\right) \tag{4.32}$$

$$I_{OS}=\frac{\mu C_{OX}}{2}\frac{W}{L}\left(\left(v_{gs1}-\frac{\gamma\cdot v_{sb1}}{2\sqrt{2\Phi_F+V_{SB1}}}\right)^2-\left(v_{gs2}-\frac{\gamma\cdot v_{sb2}}{2\sqrt{2\Phi_F+V_{SB2}}}\right)^2\right)=\frac{\mu C_{OX}}{2}\frac{W}{L}\left(\left(v_{gs1}-\frac{g_{mb1}v_{sb1}}{g_{m1}}\right)^2-\left(v_{gs2}-\frac{g_{mb2}v_{sb2}}{g_{m2}}\right)^2\right) \tag{4.33}$$

Provided that $v_x=v_{gs}-g_{mb}/g_m\cdot v_{sb}$,

$$V_x(j\omega)=H_c(j\omega)V_c(j\omega)+V_d(j\omega)/2 \tag{4.34}$$

The common-mode transfer function H_c is approximated to the following expression with ideal matching assumption:

$$H_c(j\omega)=\frac{A\cdot s\left(s+\frac{2g_{m3}C_{T1}(g_{m1}+g_{mb1})}{A}\right)}{B\cdot\left(s+\frac{2g_{m3}}{C_{T2}+2C_{gs3}}\right)\cdot\left(s+\frac{2(g_{m1}+g_{mb1})}{C_{T1}+2C_{gs1}}\right)} \tag{4.35}$$

where A and B are equal to:

$$A=g_{m1}C_{T1}C_{T2}-2g_{mb1}C_{gs1}C_{T2}+2(g_{m1}+g_{mb1})\cdot C_{T1}C_{gs3}+2g_{m1}C_{bs1}\cdot(C_{T1}+C_{T2}) \tag{4.36}$$

$$B=g_{m1}\cdot(C_{T1}+2C_{gs1})\cdot(C_{T2}+2C_{gs3}) \tag{4.37}$$

According to (4.35), the common-mode transfer function has two zeros, one of which is at the origin, and two poles. In order to minimize the offset voltage, the second zero should be pushed to very high frequencies by increasing Cgs1 and minimizing K to be zero; this can be illustrated in the simplified bode plot of $|H_c(s)|$ of the source-buffered structure in Fig. 4.16.

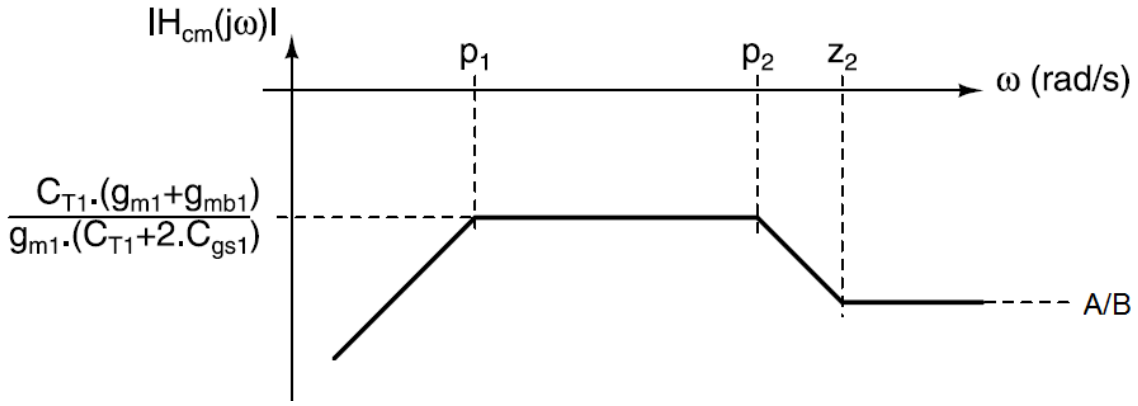


Fig. 4. 16. Simplified bode plot of $|H_c(s)|$ [8]

Therefore, there is an optimal value for C_{gs1}: larger total gate-to-source capacitance is useful for decreasing the maximum level of $|H_c(s)|$; while too large C_{gs1} is not desirable for minimized A in (4.36).

$$C_{gsl} = \frac{g_{ml} \bullet C_{Tl} \bullet C_{T2} + 2g_{ml} \bullet C_{bsl}(C_{Tl} + C_{T2}) + 2C_{Tl} \bullet C_{gs3}(g_{ml} + g_{mbl})}{2C_{T2}g_{mbl}} \qquad (4.38)$$

Generally, the gate-to-source capacitances of the input differential pair are not large enough, so two on-chip capacitors are added to comply with the relation.

The important advantage of this topology is smaller DC offset when dealing with large input signals with relatively high EMI frequencies. An extra benefit is less input referred noise which is similar to that of the classic differential pair, because the auxiliary differential pair does not disturb the signal path of the nominal differential pair. Its effectiveness can also be verified by the simulation results in Fig. 4.17 and Table 4.4 compared to the classic one in the following figure and table. The maximum offset voltages for input signal of 50mV, 425mV and 800mV in the source-buffered differential pair are -0.9mV, -75.4mV and -218.6mV, respectively.

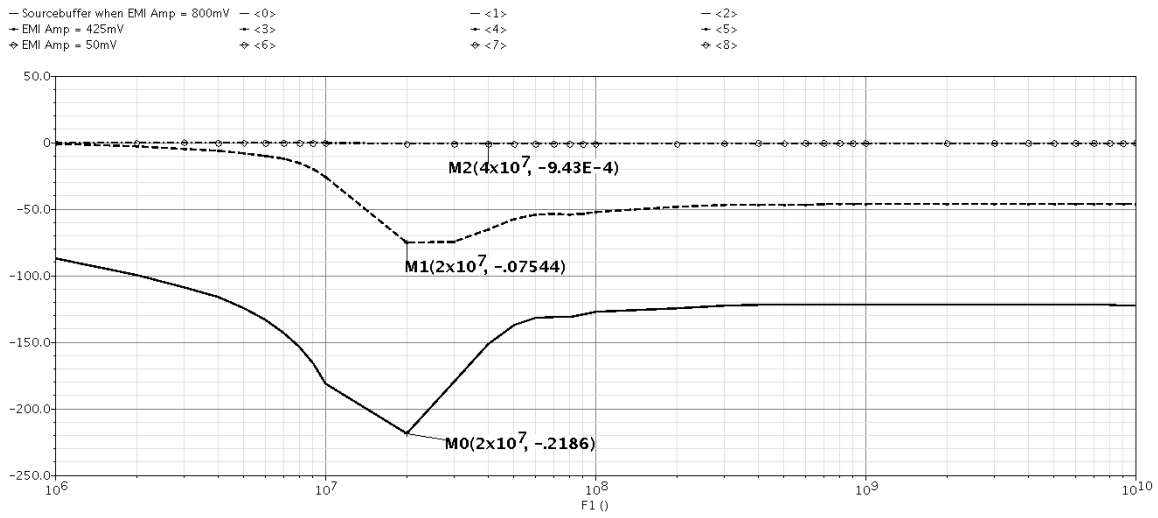


Fig. 4. 17. Offset measured for source-buffered differential pair

Table 4. 4. Input offset voltages of classic and source-buffered circuits with various EMI amplitudes

	Classic	**Source-Buffered**
Offset voltage (EMI Amp = 50mV)	-5.421mV	-0.9mV
Offset voltage (425mV)	-238.3mV	-75.4mV
Offset voltage (800mV)	-428.2mV	-218.6mV

The major disadvantage of the source-buffered differential pair is its high dependence on tightly specified tolerances of on-chip capacitors C_{in}. Actually, C_{in} exhibits some systematic error which cannot be ignored when integrated. So the A term in (4.35) and (4.36) is not zero or minimized, which results in larger input offset voltage. In Reference [31], it is illustrated that C_{in} has considerable variability in the order of 20%

~ 30%, due to process and temperature variations. Using the topology with source degeneration resistor in Fig. 4.18 can suppress the issue effects.

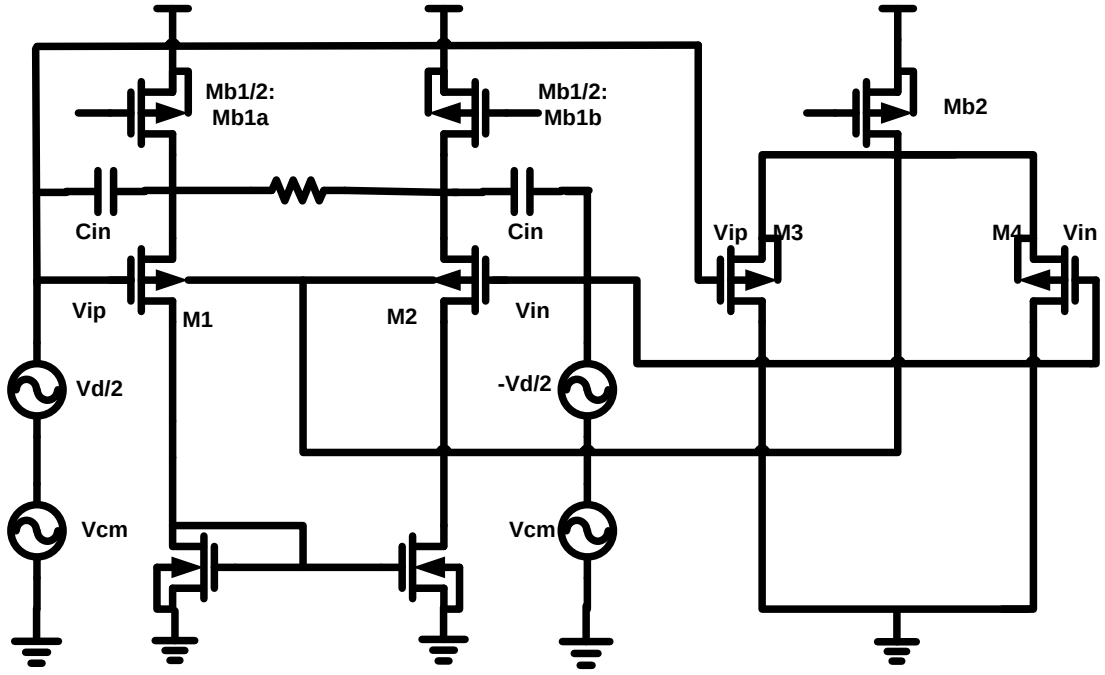


Fig. 4. 18. Source-buffered topology with source degeneration resistors

The offset analysis is similar to that in the previous case, only with different differential-mode transfer function.

$$V_{x1,2}(j\omega) = H_c(j\omega) \bullet V_c(j\omega) \pm H_d(j\omega) \bullet V_d(j\omega)/2 \tag{4.39}$$

$$H_d(j\omega) = \frac{4 + j\omega \bullet (C_{T1} \bullet R_s + 2C_{bs1} \bullet R_s - 2C_{gs1} \bullet R_s \bullet \frac{g_{mb1}}{g_{m1}})}{4 + 2(g_{m1} + g_{mb1}) \bullet R_s + j\omega \bullet (C_{T1} \bullet R_s + 2C_{bs1} \bullet R_s + 2C_{gs1} \bullet R_s)} \tag{4.40}$$

$$V_{OS} = \frac{2\beta}{g_{m1}} \int_{\infty}^{\infty} H_c(j\omega) V_c(j\omega) H_d(j\omega) V_d(j\omega) |\cos\varphi d\omega \tag{4.41}$$

In order to minimize the input offset voltage, $|H_c(jw)|$ should be decreased as much as possible. However, due to the variations of the integrated capacitors C_{in}, it is very difficult to keep $|H_c(jw)|$ minimized as zero. The source degeneration resistor connected

between the sources of M1 and M2 is effective for decreasing $|H_d(jw)|$ at high EMI frequencies. According to (4.40), the differential-mode transfer function at high frequencies is simplified as:

$$H_d(\infty) = \frac{C_{T1} + 2C_{bsl} - 2C_{gsl} \bullet \frac{g_{mb1}}{g_{m1}}}{C_{T1} + 2C_{bsl} + 2C_{gsl}} \tag{4.42}$$

Since C_{gs1} (containing the on-chip capacitor C_{in}) is much larger than C_{bs1} and C_{T1}, the input offset voltage for high EMI frequencies is approximated to:

$$V_{OS} \approx \frac{2\beta}{g_{m1}} \int_{\infty}^{\infty} \frac{g_{mb1}}{g_{m1}} \bullet \frac{A}{B} | \bullet | V_c(j\omega) \bullet V_d(j\omega) | \bullet \cos\varphi \bullet d\omega \tag{4.43}$$

Because of the source degeneration resistor, $|H_d(\infty)|$ is equal to g_{mb1}/g_{m1} and the contribution of A term is suppressed at higher frequencies; additionally, the source resistor also improves the linearity of the input stage by decreasing the effective transconductance. The following plots are the comparison results from voltage-follower configuration for input referred offset voltage of source-buffered structure with/without source resistors for different Cin. The improvement at high frequencies is significant.

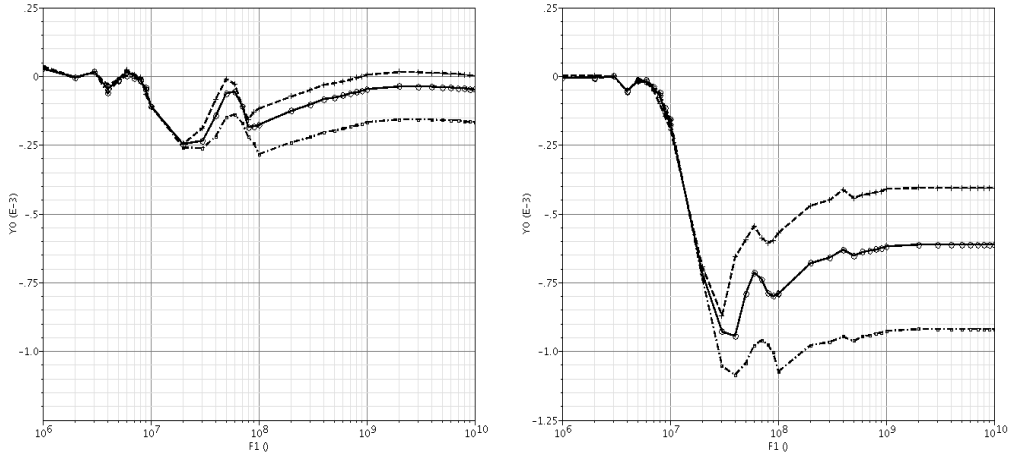


Fig. 4. 19. Comparison of offset voltage of topologies with (L)/without (R) Rs for different C_{in}

According to Fig. 4.19, the effect of source resistor R_S can be verified. The sensitivity to mismatch and systematic offset of integrated capacitors C_{in} is less, especially during relatively high EMI frequencies. It is obtained from Fig. 4.16 that the levels of $|H_C(jw)|$ at high frequencies are related to C_{in}; if using R_S, the contribution of A term in the common mode transfer function has been reduced.

In order to illustrate the effectiveness of the source buffered scheme with source resistor compared to classic and original source buffered differential pairs, the offset voltage results are summarized as follows in Table 4.5 and Fig. 4.20. Since the bulk of the nominal differential pair is connected to the auxiliary part, an isolated well area is desired for the input transistors when doing the layout. Here, PMOS transistors are used as the input differential pair, which could be the reason for larger offset compared with the previous topologies using NMOS.

Table 4. 5. Input offset voltages of classic and source-buffered differential pairs with/without R_S for different EMI amplitudes

	EMI Amplitude	Classic	Source-buffered	Source-buffered with R_S
Maximum Offset(mV)	800mV	-428.2	-218.6	-110.3
	425mV	-238.3	-75.4	-17.4
	50mV	-5.421	-0.9	-0.247

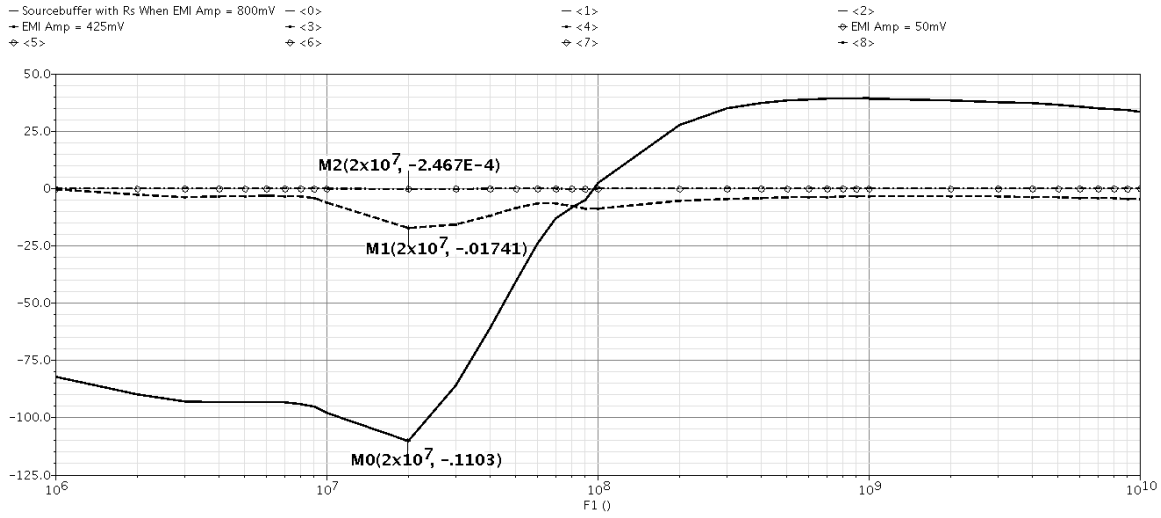


Fig. 4. 20. Comparison of offset vs. EMI frequencies @ 50mV, 425mV, 800mV in source-buffered topology with R_S

Although the source buffered differential pair generate net zero output offset current in ideal case according to (4.35) and (4.38), it is difficult to obtain an optimum value for the on-chip capacitors C_{in}, not only for the process variations, but also for the trouble of extracting the required parameters in (4.38). Owing to this issue, it might not be possible to guarantee the minimum value for A in (4.38), or high frequency zero which is even worse. If the second zero is not high enough, for example, it is located between the two poles, then $|H_c(jw)|$ increases with higher EMI frequencies, until reaches the upper limit that could be much larger than the ideal case, which is illustrated in Fig. 4.21.

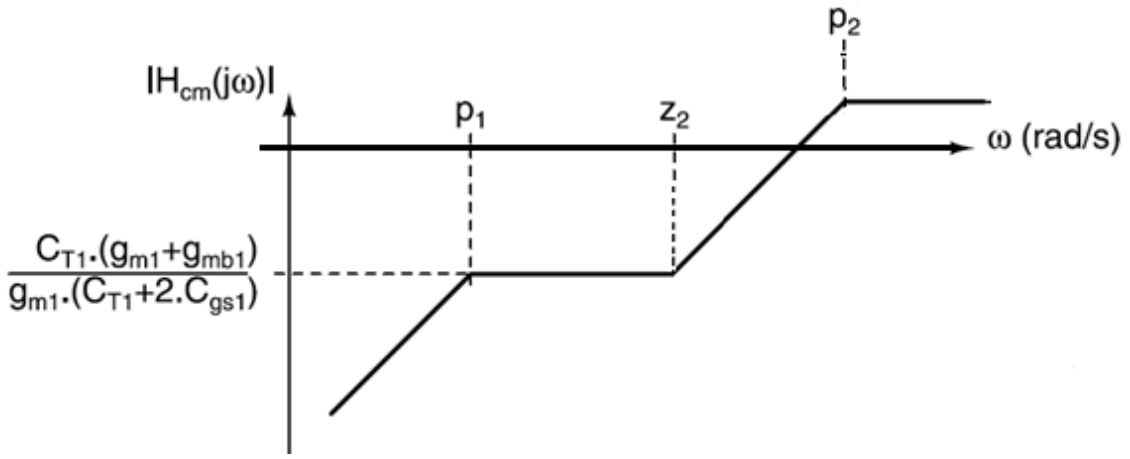


Fig. 4. 21. Simplified bode plot when the second zero is not high enough

Another major drawback of the source buffered differential pair with source resistor is the larger input referred noise. Due to the existence of the source resistor R_S, the two tail current sources M_{b1a} and M_{b1b} introduce some differential error, which means the circuit suffers from higher noise (and offset voltage). If the two noise sources are not considered, the total input noise is:

$$\overline{V_{n,in}^{\ 2}} = 8kT\left(\frac{2}{3g_{m1}} + \frac{R_S}{2}\right) \tag{4.44}$$

In the real case, if the output noise current of each current source is equal to I_n^2, then the input referred noise voltage is higher than that in (4.44) by $2I_n^2 \cdot (0.5R_S)^2$ approximately:

$$\overline{V_{n,in}^{\ 2}} = 8kT\left(\frac{2}{3g_{m1}} + \frac{g_{m1a}R_S^2}{6} + \frac{R_S}{2}\right) \tag{4.45}$$

From this point of view, the source-buffered differential pair with source resistance is comparable to the classic differential pair, and could not be a very perfect choice.

5. DESIGN OF NEW SOURCE-BUFFERED TOPOLOGY

5.1 Introduction

According to the previous sections, three factors are necessary to be present together to generate EMI-induced DC shift: the EMI source, nonlinearity of the input devices and parasitic capacitances from the input transistors' source to the ground. Hence, it is sufficient to get rid of one of the factors to suppress the EMI effects, which is shown in Fig. 5.1 [32]. In order to eliminate the EMI effects, various circuit topologies were proposed with the respective advantages and disadvantages.

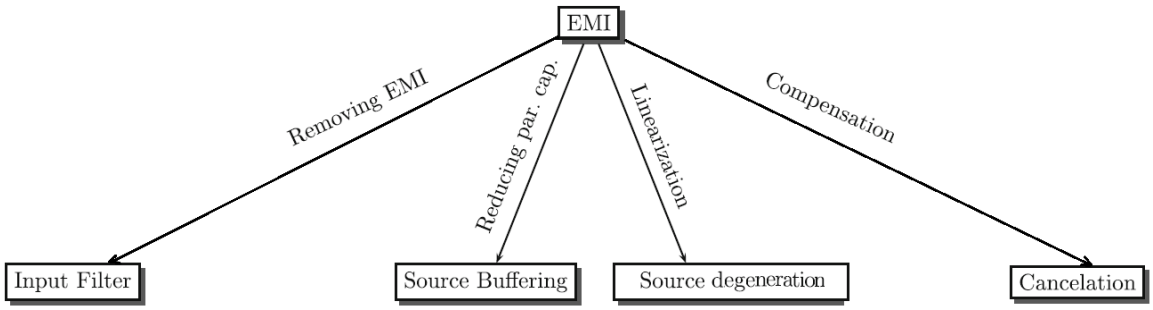


Fig. 5. 1. Possible EMI solutions

5.1.1 Input Filter

For the topology with low pass RC filter in front of the input differential pair, the purpose is to prevent any EMI disturbances from entering the actual circuit. However, there are important drawbacks which make it not so desirable. First, the RC low pass filters might attenuate the original input signals which are generally weak. Secondly, the RC filters introduce an extra pole which might degrade the phase margin; In order not to degrade the stability, the pole must be pushed far beyond the dominant pole of the circuit:

$$\frac{1}{2\pi RC} \geq 10 \cdot GBW = \frac{10g_m}{C_L} \tag{5.1}$$

Thirdly, the thermal noise associated with resistors increases the total input referred noise. According to (5.1),

$$R \leq \frac{1}{20\pi g_m}\frac{C_L}{C} \tag{5.2}$$

The noise spectral density of the resistor and the input transistors are:

$$\overline{v_{Rn}^2} = 4kTR \tag{5.3}$$

$$\overline{v_{Tn}^2} = \frac{4\gamma kT}{3g_m} \tag{5.4}$$

$$\frac{\overline{v_{Rn}^2}}{\overline{v_{Tn}^2}} = \frac{3g_m R}{\gamma} \leq \frac{3C_L}{20\pi\gamma C} \tag{5.5}$$

In order to obtain the negligible thermal noise for the resistor, C has to be large enough according to (5.5), which is undesirable in the integrated circuit design.

5.1.2 Source Degeneration

Distortion phenomenon is suppressed by adding source degeneration resistors to linearize the differential pair. Its drawback is the larger input referred noise because of the source resistors ($2R_S$) in the signal path.

$$\overline{v_{n,in}^2} = 8kT(R_S + \frac{2}{3g_{m,in}}) \tag{5.6}$$

In addition, the source degeneration resistors are infeasible at high EMI frequencies, because they could be shortened by the parasitic source ground capacitance, and the offset reduction is not substantial due to the limited to $|H_d(\infty)|$.

5.1.3 Cross Couple

If none of the three dominant factors, which are the EMI source, nonlinearity of the input devices and parasitic capacitances from the input transistors' source to the ground, can be removed, then the compensation topology e.g. cross-coupled differential pair can be used. The EMI-induced offset can be eliminated by applying the EMI disturbances to a second differential pair with opposite effect on the offset and cross connecting the outputs of both pairs.

In order not to weaken the desired input signal while attenuating the EMI signals, two matched RC high-pass filters must be added in front of the second differential pair with the cut-off frequency large enough. However, the disadvantages associated with the filters and the cross-coupled differential pair are the higher noise owing to the resistors and the extra transistors, the larger current consumption and integrated area, and the closed-loop stability issue. Additionally, a reference voltage is to bias the second differential pair which adds the complexity of the design. Most importantly, since the mismatch cannot be ignored, and the reference voltage is not equal to the DC bias voltage of the nominal differential pair due to the large process variations, the offset compensation worsens dramatically, which makes this topology difficult to achieve in practice.

5.1.4 Source Buffer with/without Source Resistors

Because parasitic capacitances from the source of the input transistors to the ground is one influence factor of the EMI-induced offset voltage, the source buffered differential pair is proposed for achieving sufficient common mode rejection for higher frequencies, by removing the large bulk source capacitance and decoupling the bulk from

the input sources [32]. An extra advantage is less input referred noise which is similar to that of the classic differential pair, because the auxiliary differential pair does not disturb the signal path of the nominal differential pair. The major drawback of the source-buffered differential pair without source resistors is its high dependence on tightly specified tolerances of on-chip capacitors C_{in}, which exhibits systematic error. The topology with source degeneration resistor in Fig. 4.16 can suppress the issue effects.

Though the source buffered differential pair generate net zero output offset current in ideal case according to (4.35) and (4.38), it is difficult to extract the required parameters in (4.38), especially with large process variations in practice, which makes the design target not easy to achieve. Another major disadvantage of the source buffered differential pair with source resistor is the larger input referred noise. Due to the existence of the source resistor R_S, the two tail current sources M_{b1a} and M_{b1b} introduce some differential error, which means the circuit suffers from higher noise (and offset voltage). From the point of view of the noise, the source-buffered differential pair with source resistance is comparable to the classic differential pair, and could not be a very perfect choice.

5.1.5 Proposed Design

In consideration of EMI-induced input offset, matching constraints, input referred noise, and closed-loop stability issue, the source buffered structure with source resistors generates a much smaller input offset voltage, has a much more favorable noise behavior, and is more insensitive to process variations and mismatch, if compared to other EMI resisting differential structures. However, the source-buffered scheme has its own disadvantages which make the design with good EMI performance not very easy. The

target is to overcome the inadequacy of the differential pair while taking advantages of the merits in the meantime. It means that the total input referred noise must be minimized and the dependence of the on-chip capacitors on process variations suppressed in the new topology; meanwhile the advantages of reducing the effect of parasitic capacitances thus increasing the common-mode rejection has to be maintained.

5.2 Circuit Implementation of Proposed Source-Buffered Topology

5.2.1 Another Source Degeneration Connection

Because the source-buffered scheme in Fig. 4.18 has relatively larger input referred noise owing to both the tail current transistors contributing to the differential noise, the differential pair can be degenerated as shown in Fig. 5.2 with small degeneration resistors. The source degeneration resistors R_{S1} must be small enough, since the bias current I_B flows through them and thus consuming voltage headroom of $I_B R_{S1}/2$, which is an important issue if resistors with high value are used or low-voltage applications are expected. Small degeneration resistors improve the noise behavior further because R_{S1} is one of the dominant terms in the input referred noise. In addition, the replica stage reduces the capacitive loading of the source as the original source-buffered structure does, but without the risk of forward biasing the body source junction of the input transistors for high EMI amplitude. Nevertheless, the disadvantage is slightly higher body effect and thereby more coupling of substrate noise.

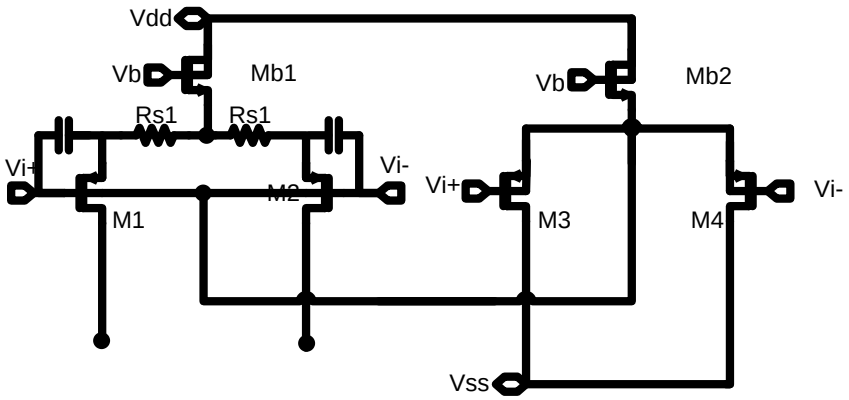


Fig. 5. 2. Another differential pair with source degeneration resistors applied

When the input sources are connected as shown in Fig. 5.2, the large isolation well to p-substrate capacitance at the drain of M_{b1} is removed, so the drain-bulk capacitance C_{Tb1} can be neglected, if compared to the much larger parasitic capacitance C_{Tb2} at the drain of M_{b2}. The small-signal circuit for common mode is shown in Fig. 5. 3:

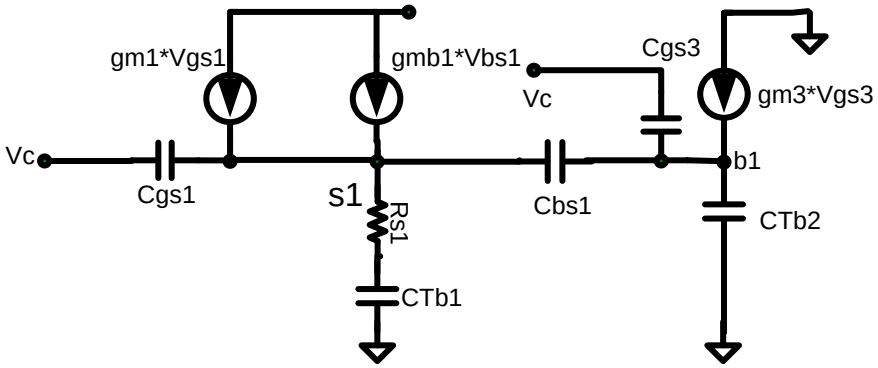


Fig. 5. 3. Small-signal analysis in common mode

The common mode transfer function is obtained in the following procedure:

$$v_{xi} = \frac{1}{g_{mi}}(g_{mi}v_{gsi} + g_{mbi}v_{bsi}) \rightarrow v_{s1} = \frac{g_{m1}v_c + g_{mb1}v_b - g_{m1}v_x}{g_{m1} + g_{mb1}} \tag{5.7}$$

From the small-signal model shown at the left side in Fig. 5.3 and the equation (5.7),

$$sC_{gs1}V_{gs1} + g_{m1}V_{x1} = \frac{V_{s1}}{R_{S1} + \frac{1}{sC_{Tb1}}} + V_{sb1}sC_{bs1} \tag{5.8}$$

Practically, $C_{gs1} >> C_{Tb1}$, especially after two on-chip capacitors are added, so the following expression is obtained:

$$[g_{m1}(R_{S1} + \frac{1}{sC_{Tb1}})(g_{m1} + g_{mb1} + sC_{gs1}) + \frac{g_{m1}sC_{bs1}}{g_{m1} + g_{mb1}}]V_{x1} - [g_{mb1}sC_{gs1}(R_{S1} + \frac{1}{sC_{Tb1}}) - \frac{g_{m1}sC_{bs1}}{g_{m1} + g_{mb1}}]V_{b1}$$
$$= V_c[(g_{m1} + g_{mb1}) - g_{mb1}sC_{gs1}(R_{S1} + \frac{1}{sC_{Tb1}}) + \frac{g_{m1}sC_{bs1}}{g_{m1} + g_{mb1}}] \tag{5.9}$$

From the small-signal model shown at the right side in Fig. 5.3,

$$(g_{m3} + sC_{gs3})V_{gs3} + sC_{bs1}V_{sb1} = sC_{Tb2}V_{b1} \rightarrow V_{b1} \approx V_c \frac{g_{m3} + sC_{gs3}}{g_{m3} + s(C_{gs3} + C_{Tb2})} \tag{5.10}$$

Therefore, the common-mode transfer function $H_c = V_x/V_c$ is:

$$H_c(s) \approx \frac{s(g_{m1} + g_{mb1})[(C_{gs3} + C_{Tb2})(g_{m1} + g_{mb1})C_{Tb1} - g_{mb1}C_{Tb2}C_{gs1}][\frac{g_{m3}(g_{m1} + g_{mb1})C_{Tb1}}{(C_{gs3} + C_{Tb2})(g_{m1} + g_{mb1})C_{Tb1} - g_{mb1}C_{Tb2}C_{gs1}} + s]}{(g_{m3} + sC_{gs3} + sC_{Tb2})[g_{m1}(g_{m1} + g_{mb1})(sC_{Tb1}R_{S1} + 1)(g_{m1} + g_{mb1} + sC_{gs1})]} \tag{5.11}$$

if $(g_{m1}+g_{mb1})g_{mb1}C_{gs1}R_{S1} = g_{m1}C_{bs1}$.

According to (5.11), there are three poles and two zeros in the common mode transfer function, of which the poles are:

$$p_1 = \frac{g_{m3}}{C_{gs3} + C_{Tb2}}; p_2 = \frac{g_{m1} + g_{mb1}}{C_{gs1}}; p_3 = \frac{1}{C_{Tb1}R_{S1}} \tag{5.12}$$

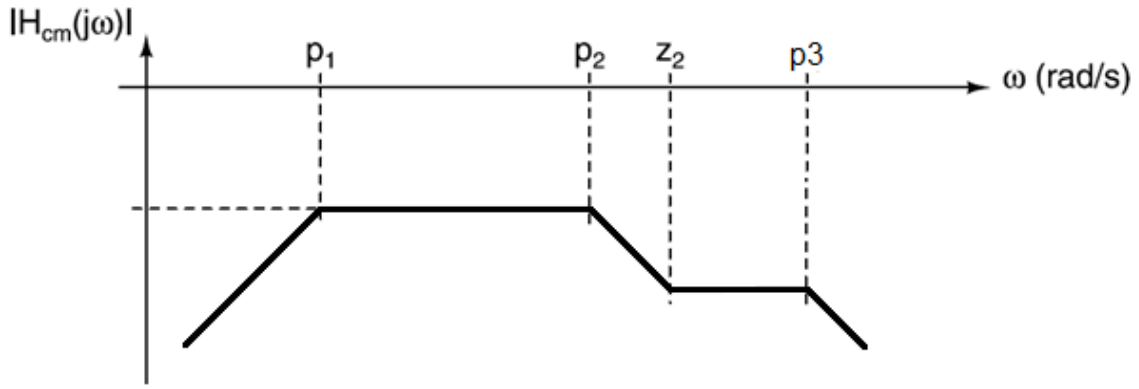
Because C_{Tb1} is a very small parasitic capacitance, the extra pole in (5.11) is at very high frequency. Besides, in order to minimize the input offset voltage, the second zero has to be wrapped to very high frequencies, which is similar to the way in original source-buffered differential pair:

$$C_{gs1} = \frac{(C_{gs3} + C_{Tb2})C_{Tb1}(g_{m1} + g_{mb1})}{g_{mb1}C_{Tb2}} \tag{5.13}$$

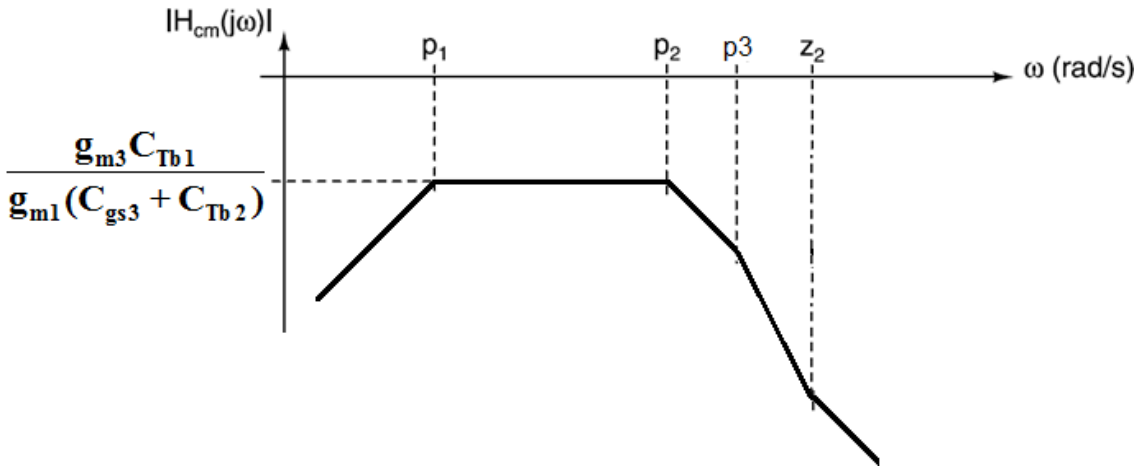
Hence, in order to reduce $|H_c(s)|$, the following conditions should be satisfied:

$$C_{gs1} = \frac{(C_{gs3} + C_{Tb2})C_{Tb1}(g_{m1} + g_{mb1})}{g_{mb1}C_{Tb2}} = \frac{g_{m1}C_{bs1}}{g_{mb1}(g_{m1} + g_{mb1})R_{S1}} \tag{5.14}$$

From the point of view of common-mode rejection, the advantages of this source degeneration connection scheme are to generate an extra high frequency pole as shown in Fig. 5. 4, together with the benefits of the original source-buffered one; while the drawbacks of headroom and substrate noise have been analyzed previously.



(a) p3 > z2



(b) p3 < z2

Fig. 5. 4: Simplified bode plot of common mode transfer function

The small-signal circuit for differential mode is shown in Fig. 5. 5:

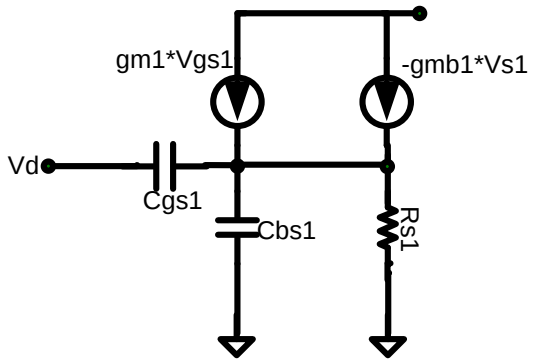


Fig. 5. 5. Small-signal analysis in differential mode

$$H_d(s) = \frac{1 + s(R_{S1}C_{bs1} - C_{gs1}R_{S1}\frac{g_{mb1}}{g_{m1}})}{1 + (g_{m1} + g_{mb1})R_{S1} + s(C_{bs1}R_{S1} + C_{gs1}R_{S1})} \tag{5.15}$$

After comparing (5.15) to (4.40), (C_{bs1}+C_{Tb1}/2) in the latter equation is replaced by C_{bs1} in the former one, which reduces the impact of the on-chip capacitors at relatively high EMI frequencies further.

5.2.2 Proposed Scheme Suppressing High-frequency EMI Effects

One dominant drawback of the source-buffered structure in Fig. 5.2 is higher body effect and thereby more coupling of substrate noise. In order to suppress this inferior effect, another source buffered structure is proposed as shown in Fig. 5. 6.

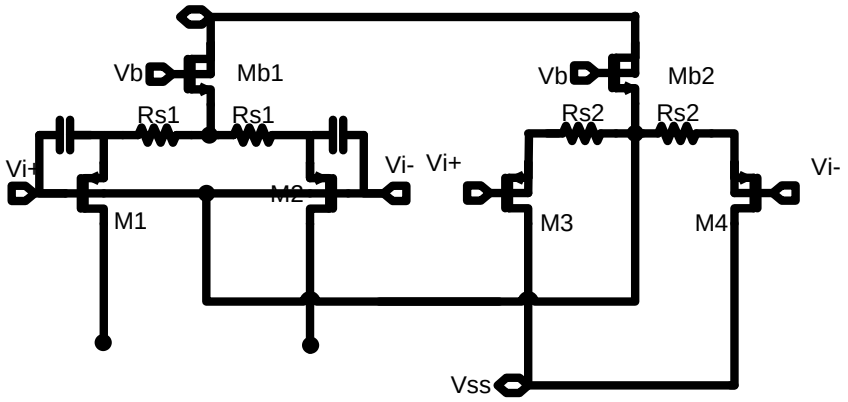


Fig. 5. 6. Proposed source buffered structure

When two pairs of source resistors are used in the source buffered circuit, if $R_{S1} = R_{S2}$, and the bias current in the input and auxiliary branch is the same, the body effect is lower and the coupling of substrate noise as compared to connecting the bulk to the source of the auxiliary differential pair. In Fig. 5.6, both of the large isolation well to p-substrate capacitances at the drain of M_{b1} and M_{b2} are eliminated, but the isolation well to p-substrate junction capacitance at the source of M_3 and M_4 cannot be ignored. The small-signal circuit for common mode is shown in Fig. 5. 7:

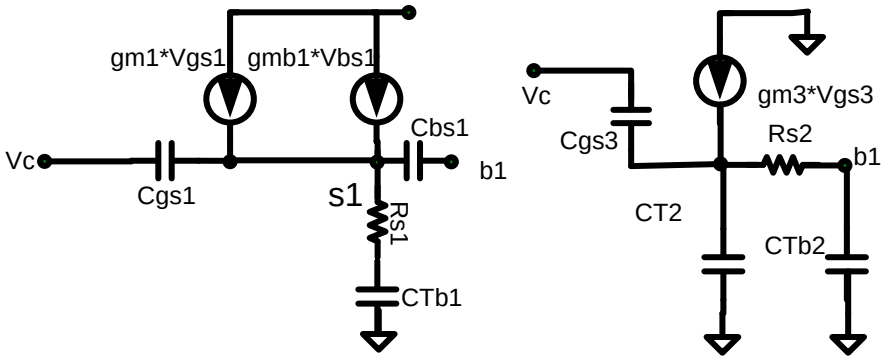


Fig. 5. 7. Small-signal analysis in common mode of Fig. 5.6

The common mode transfer function is obtained as follows. The small-signal model shown at the left side in Fig. 5.7 and the equation (5.7) are used to obtain the final common-mode transfer function. Moreover, the following relations are present: $C_{T2} >> C_{Tb1} \approx C_{Tb2;}\, C_{gs1} >> C_{Tb1}$; $R_{S1} = R_{S2}$.

$$sC_{gs1}V_c + g_{m1}V_{x1} = V_{s1}\left(\frac{sC_{Tb1}}{sC_{Tb1}R_{S1}+1} + sC_{gs1} + sC_{bs1}\right) - sC_{bs1}V_{b1} \tag{5.16}$$

From the small-signal model shown at the right side in Fig. 5.7,

$$(g_{m3} + sC_{gs3})(V_c - V_{s2}) = sC_{T2}V_{s2} + \frac{V_{s2} - V_{b1}}{R_{S2}} \tag{5.17}$$

$$\frac{V_{s2} - V_{b1}}{R_{S2}} + (V_{s1} - V_{b1})sC_{bs1} = V_{b1}sC_{Tb2} \tag{5.18}$$

According to (5.7), (5.16), (5.17), and (5.18), therefore, the common-mode transfer function $H_c = V_x/V_c$ is approximated to:

$$H_c(s) \approx \frac{s(g_{m3} + sC_{gs3} + sC_{T2} + sC_{bs1})[s(g_{m1}C_{bs1} - g_{mb1}C_{gs1})C_{Tb1}R_{S1} + (g_{m1}C_{bs1} - g_{mb1}C_{gs1})] + \dfrac{sg_{mb1}C_{Tb1}(g_{m3} + sC_{gs3})}{[s(C_{Tb2} + \dfrac{g_{m1}C_{bs1}}{g_{m1}+g_{mb1}})R_{S1}+1]}}{g_{m1}(g_{m3} + \dfrac{1}{R_{S1}} + sC_{gs3} + sC_{T2})[s(C_{Tb2} + \dfrac{g_{m1}C_{bs1}}{g_{m1}+g_{mb1}})R_{S1}+1][(g_{m1}+g_{mb1}) + s(C_{gs1}+C_{bs1})]} \tag{5.19}$$

If a simple condition of $g_{m1}C_{bs1} = g_{mb1}C_{gs1}$ is satisfied, the magnitude of common-mode transfer function is suppressed significantly at high EMI frequencies:

$$H_c(s) \approx \frac{sg_{mb1}C_{Tb1}(g_{m3} + sC_{gs3})}{g_{m1}(g_{m3} + \dfrac{1}{R_{S1}} + sC_{gs3} + sC_{T2})[s(C_{Tb2} + \dfrac{g_{m1}C_{bs1}}{g_{m1}+g_{mb1}})R_{S1}+1]^2[(g_{m1}+g_{mb1}) + s(C_{gs1}+C_{bs1})]} \tag{5.20}$$

According to (5.20), the first zero is at the origin, which increases the magnitude at a rate of 20dB/decade; after the plot reaches the first pole p_1, the magnitude of the function is flat; then the second pole p_2 decreases the magnitude of the function by -20dB/decade after its frequency; after the second zero frequency g_{m3}/C_{gs3}, the magnitude is flat again;

finally, when the frequency is larger than the pole p_3, the magnitude of the transfer function is decreased at the rate of -40dB/decade. The previous illustration is present in Fig. 5. 8.

$$p_1 = \frac{g_{m3} + \frac{1}{R_{S1}}}{C_{gs3} + C_{T2}}; p_2 = \frac{g_{m1} + g_{mb1}}{C_{gs1} + C_{bs1}}; p_3 = \frac{1}{(C_{Tb2} + \frac{g_{m1} C_{bs1}}{g_{m1} + g_{mb1}}) R_{S1}} \tag{5.21}$$

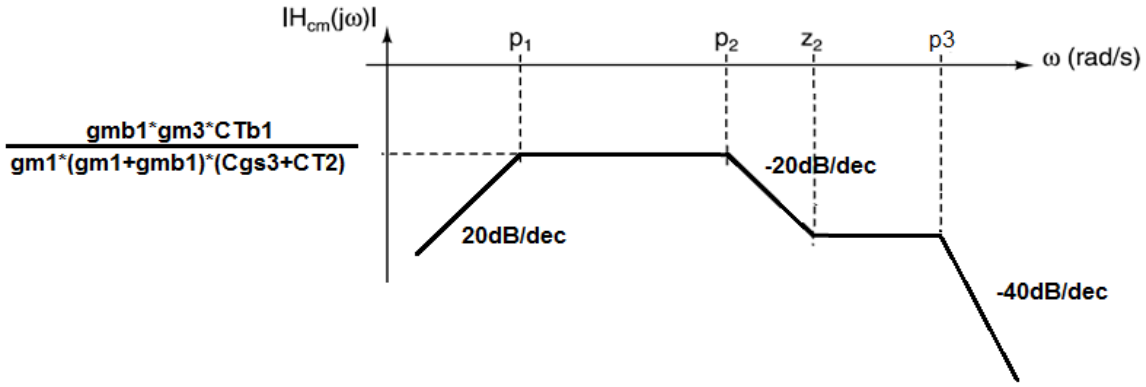


Fig. 5. 8: Simplified magnitude plot of common mode transfer function

The small-signal circuit for differential mode is the same as shown in Fig. 5.5, so the differential-mode transfer function can be expressed as (5.15), which reduces the impact of the on-chip capacitors at relatively high EMI frequencies as well.

The advantage of this proposed scheme is the stronger common-mode rejection compared to the previous cases as shown in Fig. 5.8, as well as the insensitivity of the on-chip capacitance variations; additionally, the coupling of the substrate noise is less.

5.2.3 Proposed Scheme Suppressing EMI Effects in Whole Frequency Range

As illustrated in the previous section, the major advantage of the proposed source buffered scheme is its high common-mode rejection at high EMI frequencies. However, low-frequency EMI induced offset voltage is also necessary to study and decrease. This

issue is meant to be overcome in the circuit, depicted in Fig. 5.9, in which two matched R-C high-pass filters are added in front of the auxiliary differential pair.

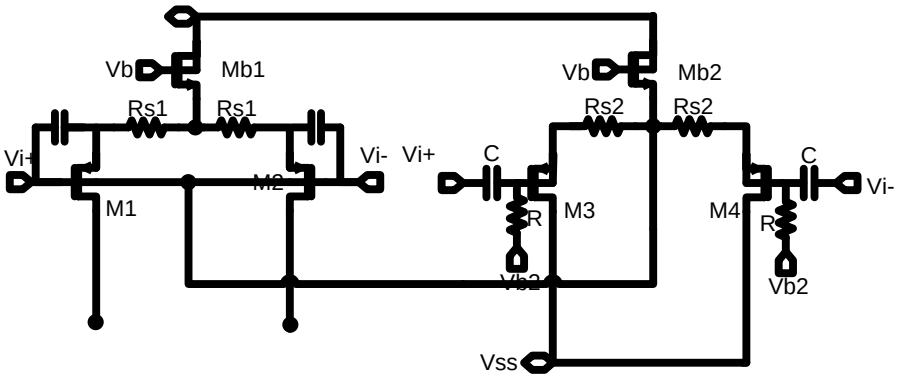


Fig. 5. 9. Proposed scheme suppressing EMI effect in whole frequency range

Analogously to the derivation obtained in the previous section, the merits of lower body effect and less substrate noise are presented as before. Since the two R-C high-pass filters are not in the signal paths, the cut-off frequency must not lie above the nominal frequency band, which is not the same as what the cross-coupled structure requires, and the closed-loop stability is not affected. This circuit needs an additional biasing voltage V_{b2}, which requires extra biasing circuits; but it is not sensitive to matching the input common-voltage of M1-M2, which is also due to the fact that the filters are not in the signal paths, and has been verified through the simulations.

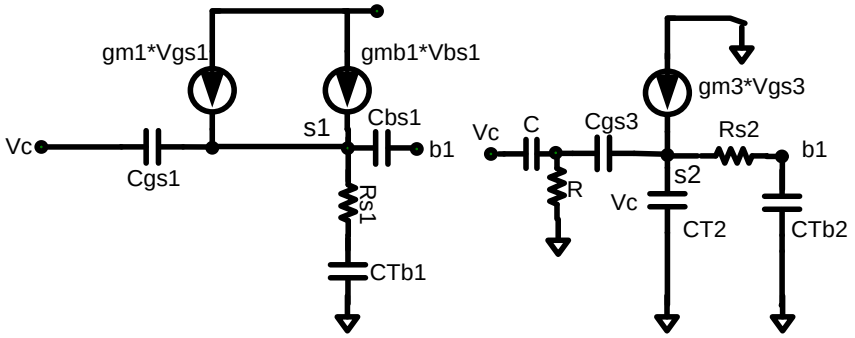


Fig. 5. 10. Small-signal analysis in common mode of Fig. 5.9

The common mode transfer function is derived in the following procedure. The small-signal model shown at the left side in Fig. 5.10 and the equation (5.7), (5.16) are used to obtain the final common-mode transfer function. Additionally, $C_{T2} >> C_{Tb1} \approx C_{Tb2;}$ $C_{gs1} >> C_{Tb1}$; $R_{S1} = R_{S2}$.

$$g_{m1}[(sC_{Tb1}R_{S1}+1)(g_{m1}+g_{mb1}+sC_{gs1}+sC_{bs1})+sC_{Tb1}]V_{x1}+s[(sC_{Tb1}R_{S1}+1)(g_{m1}C_{bs1}-g_{mb1}C_{gs1})-g_{mb1}C_{Tb1}]V_{b1}$$
$$=s[(sC_{Tb1}R_{S1}+1)(g_{m1}C_{bs1}-g_{mb1}C_{gs1})+g_{m1}C_{Tb1}]V_c \quad (5.22)$$

From the small-signal model shown at the right side in Fig. 5.10,

$$sCV_c-(sC+\frac{1}{R})V_{s2}=V_{gs3}(sC_{gs3}+sC+\frac{1}{R}) \quad (5.23)$$

$$V_{gs3}(sC_{gs3}+g_{m3})=sC_{T2}V_{s2}+\frac{V_{s2}-V_{b1}}{R_{s2}} \quad (5.24)$$

$$\frac{V_{s2}}{R_{s2}}+\frac{g_{m1}}{g_{m1}+g_{mb1}}sC_{bs1}(V_c-V_x)=(\frac{1}{R_{s2}}+sC_{Tb2}+\frac{g_{m1}}{g_{m1}+g_{mb1}}sC_{bs1})V_{b1} \quad (5.25)$$

If $g_{m1}C_{bs1} = g_{mb1}C_{gs1}$ is satisfied, According to (5.7), (5.16), (5.22), and (5.25), the common-mode transfer function $H_c = V_x/V_c$ is approximated to:

$$H_c(s)\approx\frac{sRC}{sRC+1}\cdot\frac{sg_{mb1}C_{Tb1}(g_{m3}+sC_{gs3})}{g_{m1}(g_{m3}+sC_{gs3}+sC_{T2})(sC_{Tb1}R_{S1}+1)(sC_{Tb2}R_{S2}+1)[(g_{m1}+g_{mb1})+s(C_{gs1}+C_{bs1})]} \quad (5.26)$$

Compare (5.26) to (5.20) and it is obtained that the magnitude of $H_c(s)$ can be attenuated if the EMI frequency is smaller than the cut-off frequency (1/RC) of the high-pass filters; otherwise $H_c(s)$ stays the same as (5.20), of which the simplified bode plot is as shown in Fig. 5.11. Therefore, this proposed source-buffered structure can suppress EMI effects very well at low frequency range, meanwhile reserving the advantages of the structure in 5.2.2.

The differential-mode transfer function can still be expressed as (5.15), hereby reducing the sensitivity of the on-chip capacitors to process variations.

5.3 EMI-Induced Offset Measurement Setup

As mentioned in the former sections, the EMI effect was estimated by simulating the amplifiers connected in voltage-follower configuration. In this section, the measurement setup is present in details.

In order to investigate the EMI effects on the operational amplifiers, the interfering signals are often modeled as a continuous sinusoidal waveform generated by a voltage source with zero dc mean value superimposed on the pins connected to long wires as antennas for EMI. There are some advantages for the modeling: it can simplify the numerical simulation and the laboratory measurements to compare the behaviors of different amplifiers which work in the non-linear conditions, as the waveforms of the interfering signals vary in shape; the continuous signal always represents the worst case condition when we want to check the regime response of the amplifiers impinged by an EMI input signal, because the interfering signal decay in time generally; the performance of the amplifiers with large signal working out of band can be tested since such an input waveform can be varied in the amplitude and frequency.

One of the most undesirable effects of the EMI is the shift of the output dc mean value, which is acted as offset voltage [33] [34]. Generally, a zero dc output voltage is expected for a zero dc value sinusoidal input, of which the amplitude is lower than the linear dynamic range of an amplifier. However, there is some distortion in the output voltage waveform at high EMI frequencies, and the distorted output voltage exhibits the mean value that could asymptotically reach a final dc value, which can easily force the next stage amplifiers into saturation. Because of the limit of the common-mode input range and the output swing of the amplifiers, sometimes the EMI may be sufficient to drive the amplifiers themselves into hard saturation.

When the EMI signal is subjected to the analog integrated circuits, the performance of the amplifier should be checked by the time-domain simulation, which is time consuming. Performing very long transient analysis, by lasting several or even hundreds of periods of the input signal (Fig. 5. 11), is due to the fact that the time constants of the amplifiers are generally much larger that the EMI period, therefore, the output wave must reach the steady-state condition [35].

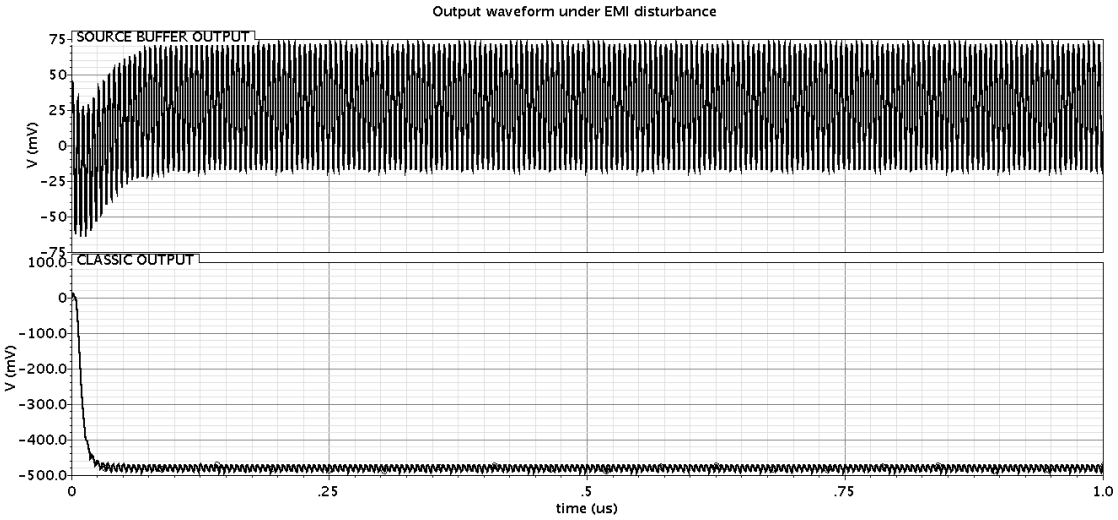


Fig. 5. 11. Output waveforms steady after long transient analysis

The EMI Induced offset is proportional to the scalar product of the differential and common mode component of the EMI signal that is injected into the inputs of the amplifiers, so in order to evaluate the performance under the effect of EMI, the induced offset must be maximized, which represents the worst case offset voltage. Actually, during the measurement for our design, two configurations can be used for the whole range of EMI frequencies: voltage follower and double opamps.

The voltage follower configuration in Fig. 5.12is used in most measurement setups [36]. If the opamp is considered as a one pole system, the open loop gain can be expressed as below:

$$A(s) = \frac{A_{DC}}{1 + s/p_1} \tag{5.27}$$

Therefore, the output voltage is derived as:

$$v_o(s) = \frac{A \bullet v_{emi}}{1 + A} = \frac{p_1 \bullet A_{DC} \bullet v_{emi}(s)}{s + p_1 \bullet A_{DC}} \tag{5.28}$$

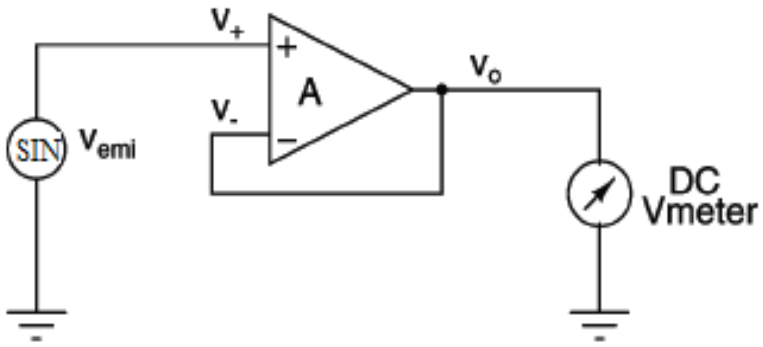


Fig. 5. 12. Voltage follower configuration

This is equal to the signal at the inverting input. So for the EMI frequencies which are higher than GBW of the amplifier, the ac signal at the output approximates to zero, and the common mode and differential mode signals at the inputs are:

$$V_d = v_{emi} \tag{5.29}$$

$$V_{cm} = V_{dc} + v_{emi}/2 \tag{5.30}$$

which represent the worst case of the EMI Induced offset. For frequencies close to or lower than GBW, the differential mode component decreases to a smaller value, which may not yield the worst case that is expected.

The double opamp structure in Fig. 5.13 is proposed by separating the DC feedback from the AC feedback loop and by using a Miller integrator to filter the AC loop [37]. The double opamp measuring structure needs two operational amplifiers A1 and A2 in the following figure. A1 is the opamp whose offset is measured while A2 forms the Miller integrator which not only filters the AC feedback but also completes the DC feedback loop [38]. Pick R2 much smaller than R1, the signal at the inverting input can be approximated as:

$$v\_(s) = \frac{1}{1 + R_1 \bullet C_1 \bullet s} \frac{p_1 \bullet A_{DC} \bullet v_{emi}(s)}{s + p_1 \bullet A_{DC}} \tag{5.31}$$

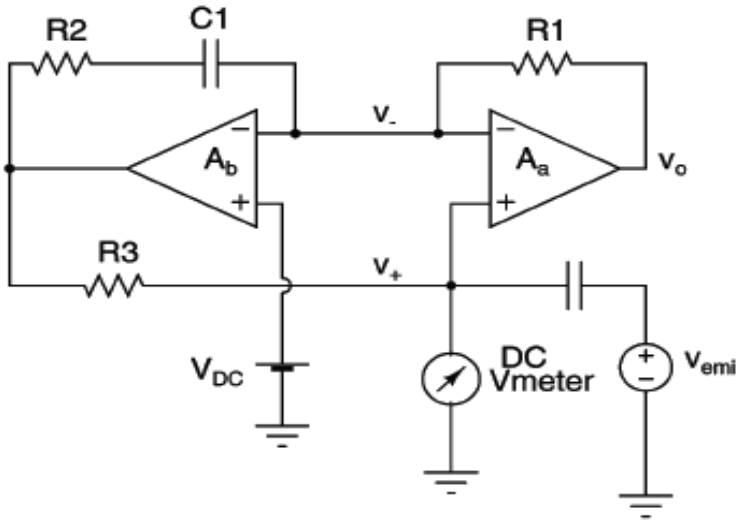


Fig. 5. 13. Double-opamp measurement setup

If the EMI frequencies are much larger than 1/(R1*C1), then its common mode and differential mode components are equal to the worst case. Because 1/(R1*C1) can be chosen very small, it is possible for us to measure the offset voltage at the low EMI frequencies. Actually the lowest EMI frequency is independent of the GBW or the opamp characteristics. The input referred offset can be obtained by measuring the DC voltage

shift at the non-inverting input of A1 [8]. However, since the two opamps are present in the feedback loop, it is important to ensure the stability of the whole circuit; moreover, at high EMI frequencies, R_1 as well as the parasitic effects impact the EMI induced offset, and a more reasonable result is obtained if using voltage-follower configuration.

5.4 Pre-layout Simulation Results

From the previous section, it is known that one of the measurement setups must be chosen to estimate the EMI performance of the circuits using the worst case offset voltage. Generally, the EMI performance at high EMI frequencies is more important than that at low ones; the largest EMI induced input offset voltage is generated at high EMI frequencies larger than the GBW of the circuits, so the voltage-follower configuration in specific frequency range is chosen in the following simulations.

Since the parasitic capacitance is one dominant factor which cause the undesired EMI effect, the different circuits are designed in the NCSU 0.5-um CMOS technology, which may have worse performance compared to those in smaller CMOS technology; in other words, the circuits designed in smaller technologies always operate on higher frequencies, so that the EMI range shifts further out of band, which can be filtered easily and relax the EMI requirements for the analog parts [32]. Additionally, it is generally known that by using the folded-cascode architecture the opamps can have enough gain, and good frequency performance which makes the circuit faster than the nominal one, even without the difficulty in shorting the inputs and outputs. According to Ref [4], since the slew rate of the folded cascode circuit is larger than that of cascode or classic one, the susceptibility of the FC circuits is more significant at higher frequencies. Therefore, five different differential pairs, which are conventional, source-buffered in Ref [15], and other

three proposed source-buffered ones in Section 5.2 respectively, have been implemented in the designs of otherwise identical folded cascode opamps at 3V power supply with the load capacitance of 3pF. All the opamps are designed based on the same input transistor size and transconductance according to the equation (4.14). Fig. 5.14 shows one proposed structure in the folded cascode design. For EMI disturbance signal, the sinusoidal wave has been added at the non-inverting input terminal while the other one is connected to the output, so that the worst case offset voltage can be generated. The EMI induced input offset voltage has been simulated for the input wave amplitude of 400mV, and 800mV, to account for the spectrum of most of the current possible interfering signals, including the cellular phone bands [1].

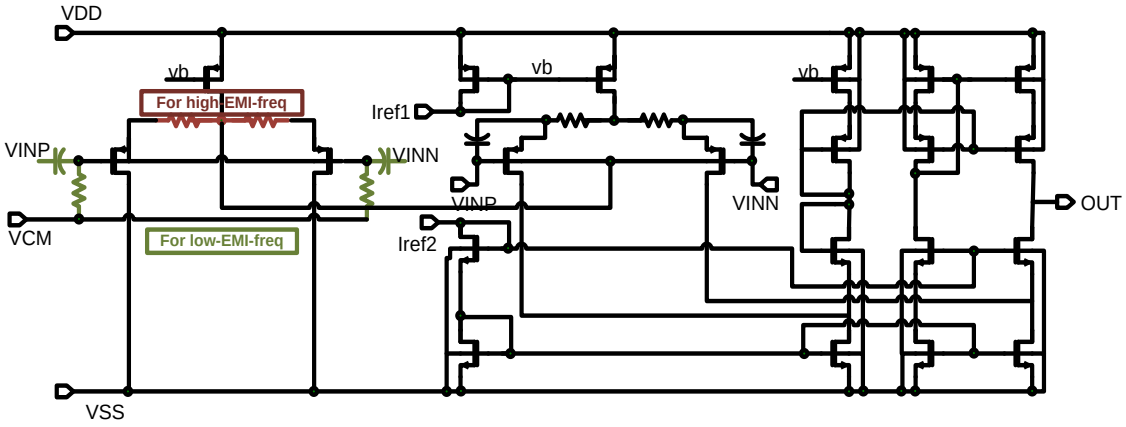


Fig. 5. 14. Proposed source-buffered structure in the folded-cascode design

Table 5.1 and Table 5.2 in the following pages summarize the performance of the proposed structures which are compared to the ones using existing EMI robust techniques.

Table 5. 1. Performance summary (a) of proposed structure compared to previous techniques

	Conventional	**Source Buffered**	**Source Buffered with proposed R_S connection**
Power supply (VDD/VSS)	3V/0V	3V/0V	3V/0V
Gm1 (uS)	715.1	723.9	719.3
Adc (dB)	69.14	61.32	61.18
GBW(MHz)	31.55	11.86	11.77
PM(deg)	68.9	71.7	66.6
Power(mW)	2.351	2.753	2.753
CMRR(dB)	111.6	102.9	103.24
Integrated Input Referred Noise (uV)	82.4	141.06	134.73
HD2(dB) (amp = 400mV @ 100MHz)	-21.36	-24.76	-37.74
Offset(mV) (AMP=800mV)	-493.5	-114.3	156.5

Table 5. 2. Performance summary (b) of proposed structure compared to previous techniques

	Proposed Source Buffered in 5.2.2	***Proposed Source Buffered in 5.2.3***
Power supply	3V/0V	3V/0V
Gm1 (uA/V)	717.8	717.8
Adc (dB)	61.20	61.20
GBW(MHz)	11.82	11.82
PM(deg)	66.6	66.6
Power(uW)	2.749	2.749
CMRR(dB)	100.1	102.23
Integrated Input Referred Noise (uV)	134.38	134.37
HD2(dB) (amp = 400mV @ 100MHz)	-34.4	-36.77
Offset(mV) (AMP=800mV)	-131.9	-72.52

Based on previous simulation results, the proposed source-buffered structure in 5.2.3 offers the best alternative compared to the structures using the conventional

technique and the existing one in literature, and presents better performance than the other two proposed designs as well. First, it has the smallest EMI induced offset voltage of -72.52mV even with large EMI signals; besides, although the total input referred noise is larger than that of the classic scheme, it is still attractive compared to other solutions due to the not too large source resistors, especially the cross-coupled differential pair mentioned before; moreover, the power consumption is comparable to other structures; furthermore, it maintains the benefits of the structure in [15], which has higher insensitivity to process variations.

Rewrite the output expression of (2.4), for a memoryless, weakly nonlinear system with a sinusoidal EMI input signal of the amplitude A,

$$y(t) = (a_0 + \frac{a_2 A^2}{2}) + (a_1 A + \frac{3a_3 A^3}{4})\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \quad (5.32)$$

Therefore, the DC term deviates from the value for a linear system due to the influence of even order terms, and the larger the input amplitude, the worse the DC shift. The following figures (from Fig. 5.15 to Fig. 5.19) show the relationship of EMI induced offset voltage with the disturbance amplitude and the dependence of the offset on nonlinearity.

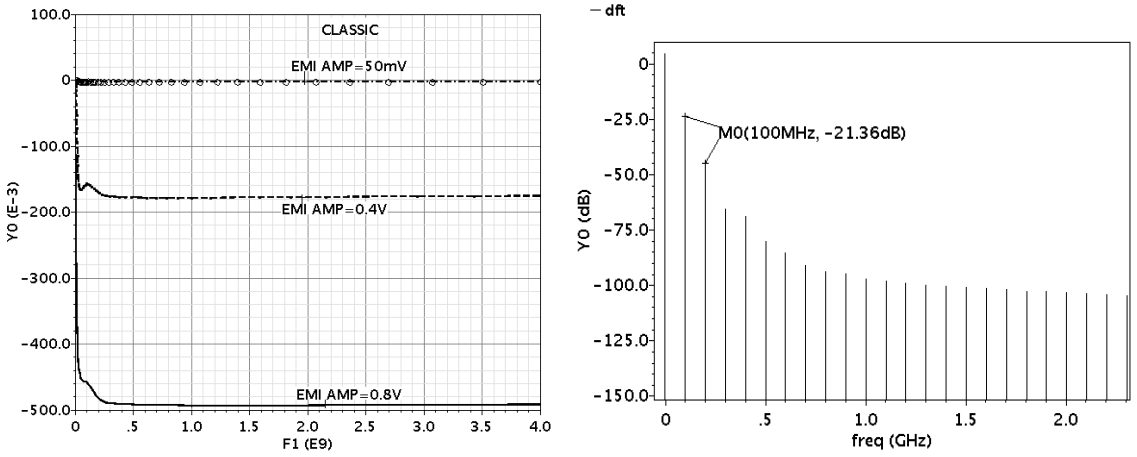


Fig. 5. 15. Input offset voltage vs. frequency; DFT simulation of classic structure

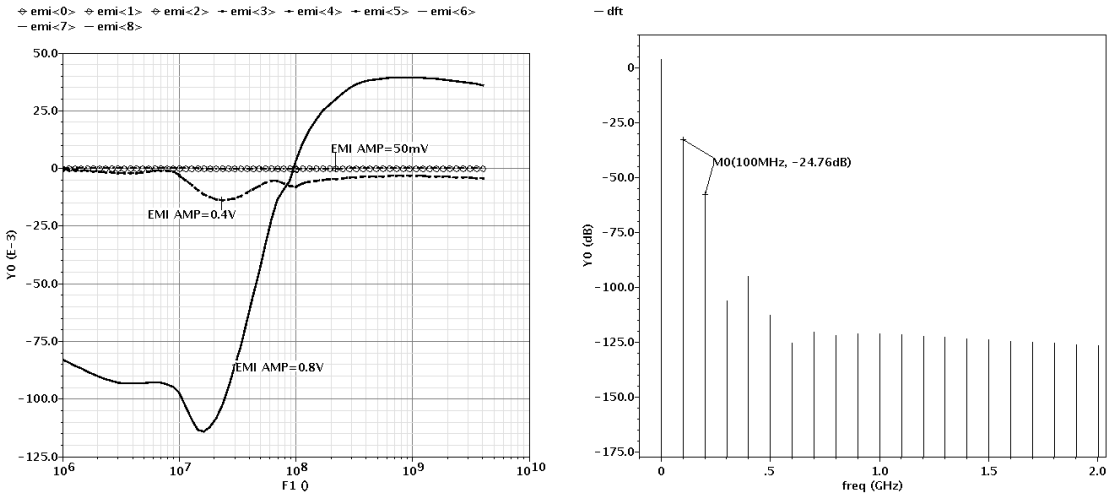


Fig. 5. 16. Input offset voltage vs. frequency; DFT simulation of topology in [15]

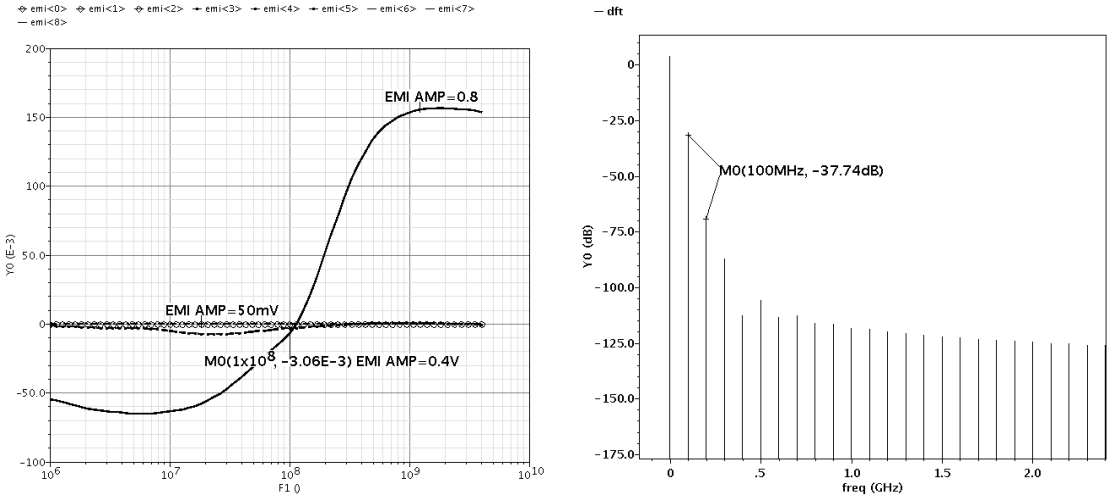


Fig. 5. 17. Input offset voltage vs. frequency; DFT simulation of source buffer with proposed R_S connection

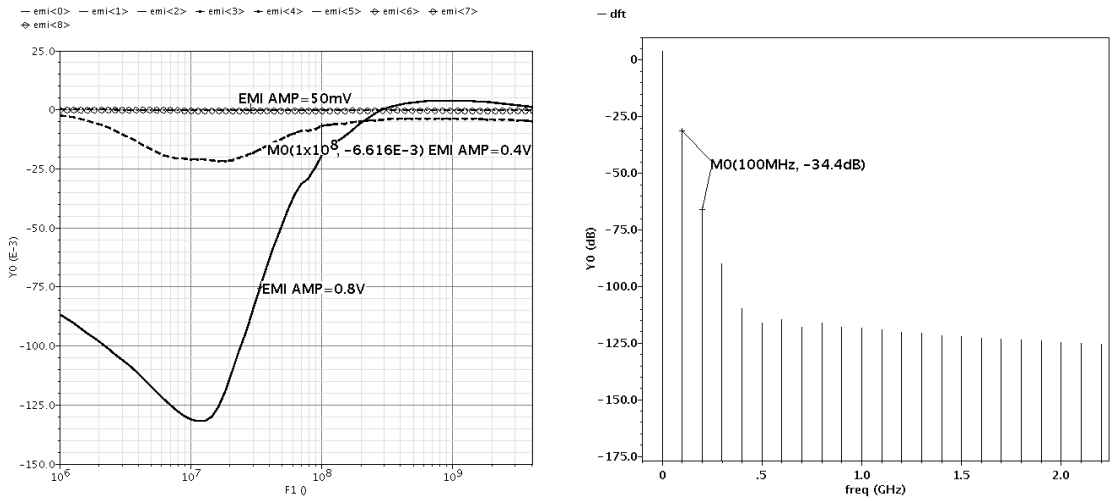


Fig. 5. 18. Input offset voltage vs. frequency; DFT simulation of structure in 5.2.2

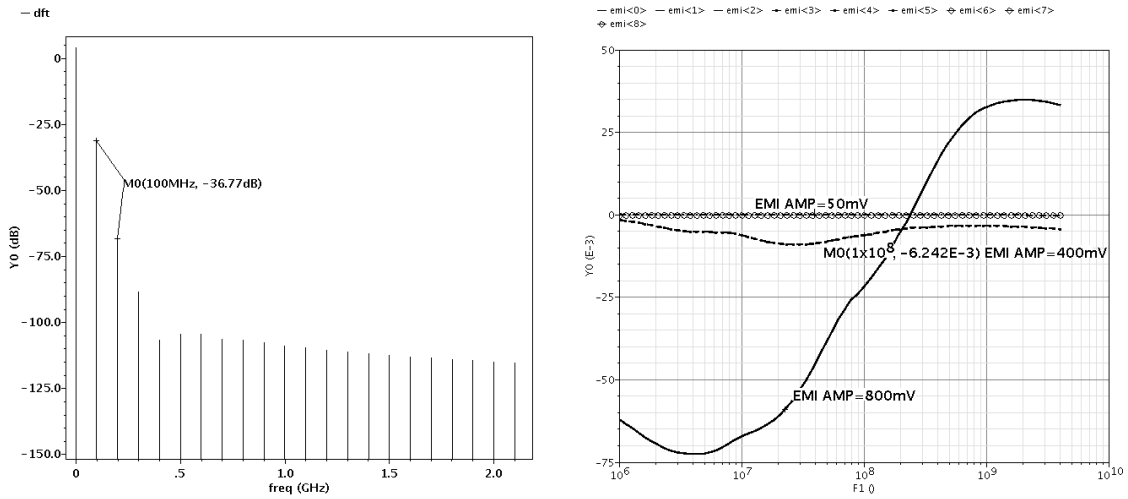


Fig. 5. 19. Input offset voltage vs. frequency; DFT simulation of structure in 5.2.3

As illustrated in the simulation plots, it is obvious that when the input amplitude varies from 50mV to 800mV, the EMI induced DC shift becomes more severe, which means the input offset voltage is larger.

Additionally, from the output expression shown previously, the larger the term of a2, the larger the offset voltage, so a2 needs to be extracted for those cases in order to

verify the dependence of the offset on nonlinear distortions. The DC gain is approximated to a1, so a1 for the five structures is 2864.18, 1164.13, 1145.51, 1148.15, and 1148.15 respectively. Because HD2 (dB) = $20*\log_{10}[(a2*A)/(2*a1)]$ and A = 0.4V, a2 for the five different circuits is 1224.53, 336.39, 74.30, 109.39, 83.27. Since HD2 is simulated with the input signal of the 400mV amplitude and 100MHz frequency, for which the offset voltages are obtained from Fig. 5.15 to Fig. 5.19, thereby demonstrating the importance of the linearity.

5.5 Post-layout Simulation Results

The layout of the test IC containing five different circuits as well as the version with extracted parasitic capacitances are shown in Fig. 5.20.

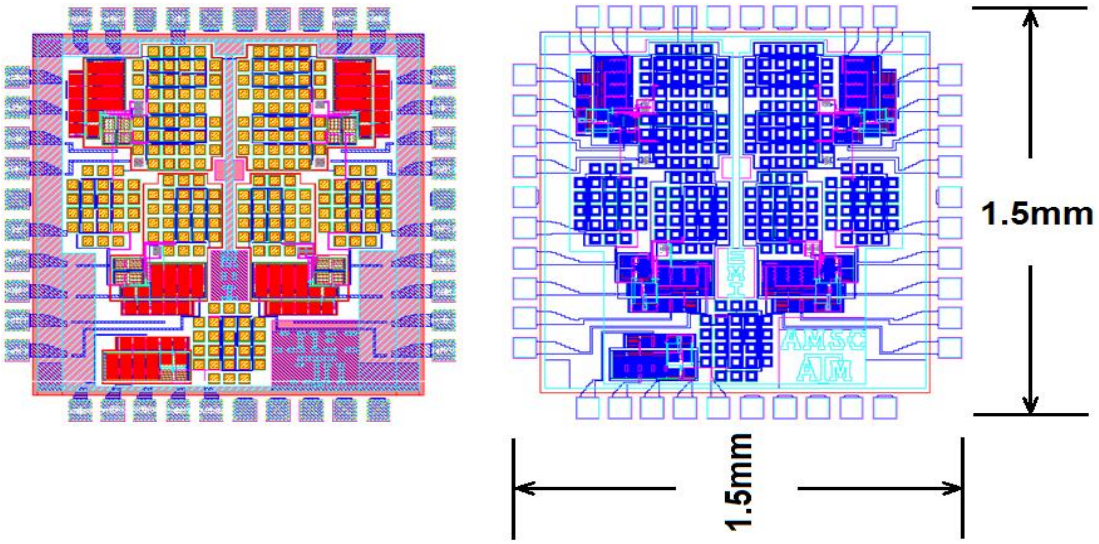


Fig. 5. 20. Layout & Extract version of test IC

The post-layout simulation results of EMI induced offset voltage, as function of the EMI frequency when the input signal of the 800mV amplitude is applied at the inputs, are shown in Fig. 5.21.

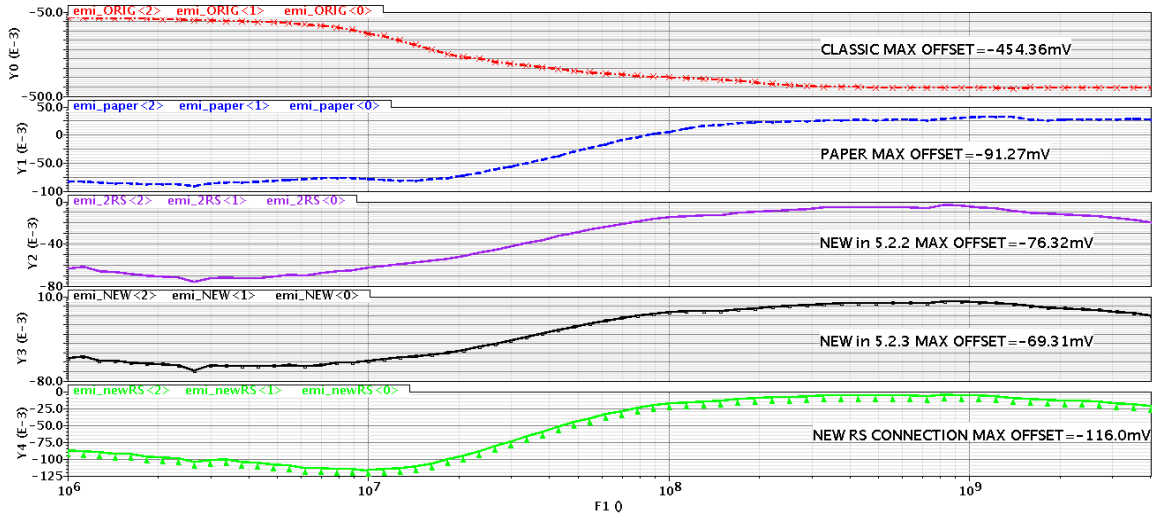


Fig. 5. 21. EMI performance comparison of five different topologies for V_{pp} = 1.6V

Therefore, it is obtained that the proposed source-buffered structure in 5.2.3 generates the smallest input offset voltage. And from Fig. 5.21, the DC shifting phenomena in the circuits using conventional and the published techniques reach the largest limit or become even worse when the EMI frequency increases, which might be suppressed in the latter three ones.

6. TESTING RESULTS

A test integrated circuit with five different circuits has been implemented in the NCSU 0.5um CMOS technology. The floor-plan as well as the microphotograph of the circuit is depicted in Fig. 6.1 and Fig. 6.2. The chip has an active area of 0.907mm2 and packaged with DIP40. The basic equipments used during EMI offset testing comprise of the multimeter, oscilloscope, voltage source, signal generator as well as other components such as capacitors, trimmer resistors, and so on. The testing results are presented in this section.

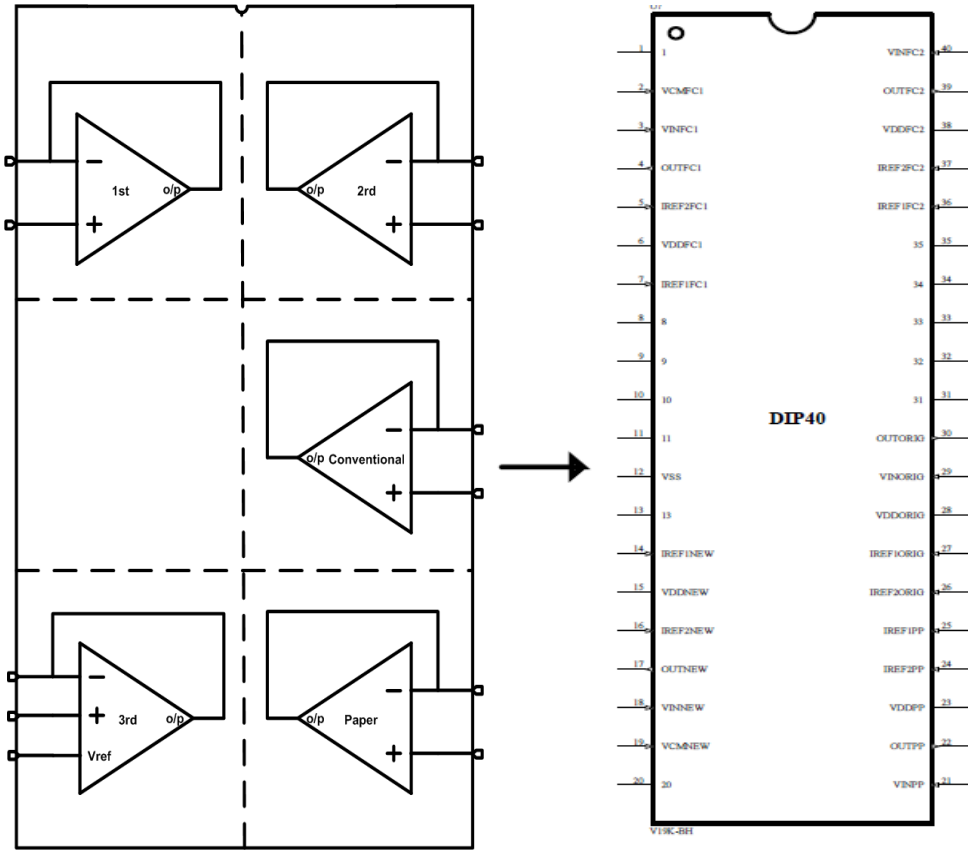


Fig. 6. 1. Floor-plan of test IC

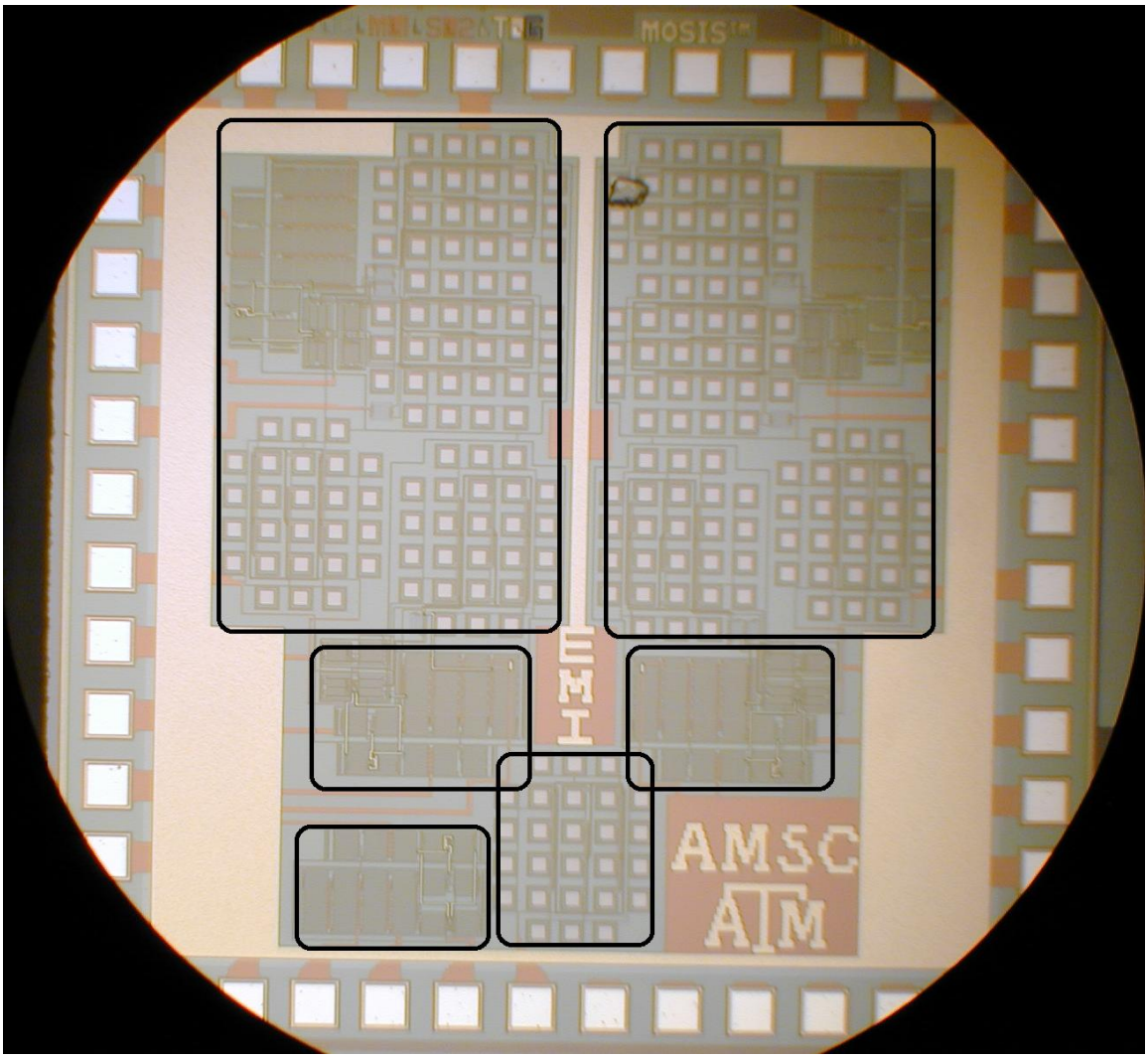


Fig. 6. 2. Microphotograph of test IC

6.1 Testing Setup

Fig.6.3 shows the testing setup. With regard to the PCB (printed circuit board) design, the board interconnections must be designed as short as possible along with ground shields and straight paths, in the purpose of minimizing all the undesired signals from the measurement setup itself. For the same reason, three capacitors with the values of 100pF, 100nF and 10uF were connected between the power line and ground. A low-pass filter (LPF) is connected between the output pins and the multimeter to prevent any residual RF from disrupting the multimeter operation and to evaluate the mean voltage, which quantifies the EMI effects easily and accurately [1]. Fig. 6.4 and 6.5 are the PCB and lab measurement pictures, in which the SMA inputs on the board are connected to PSG vector signal generator of the E8267D model (250KHz – 20GHz), and the outputs to oscilloscope. During the testing process, it is better to shield the board by RF metal box.

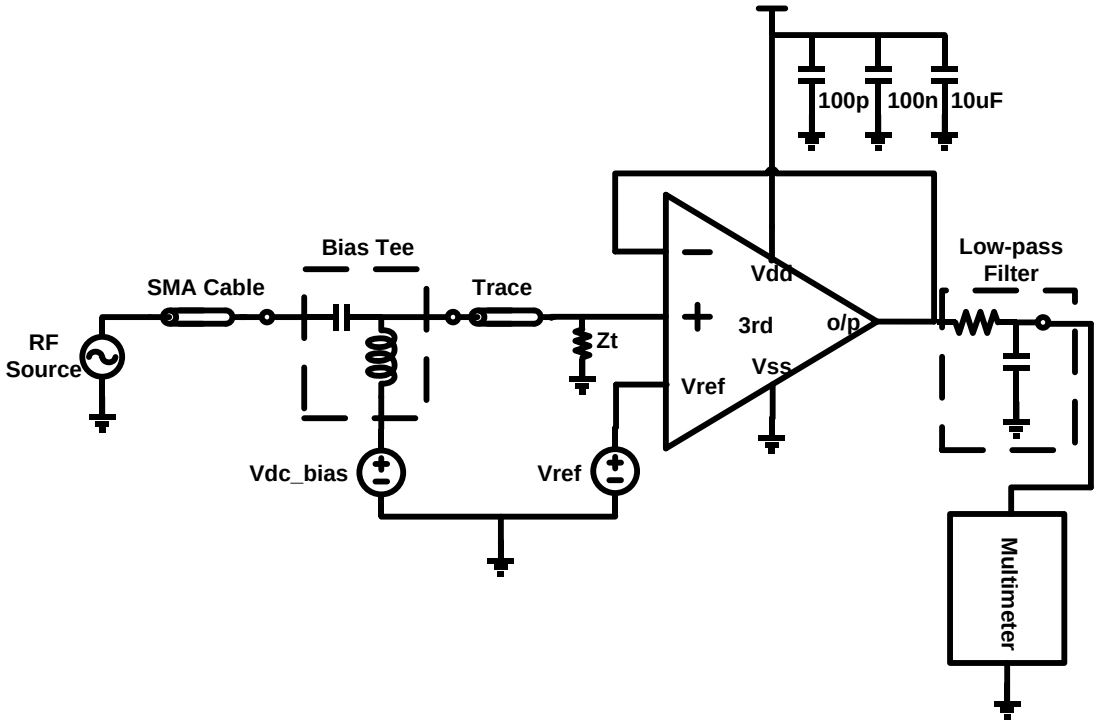


Fig. 6. 3. EMI measurement setup

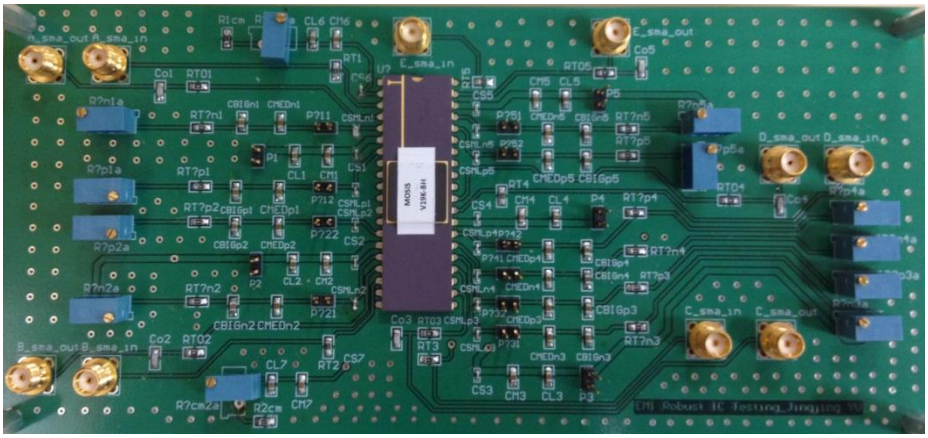


Fig. 6. 4. PCB

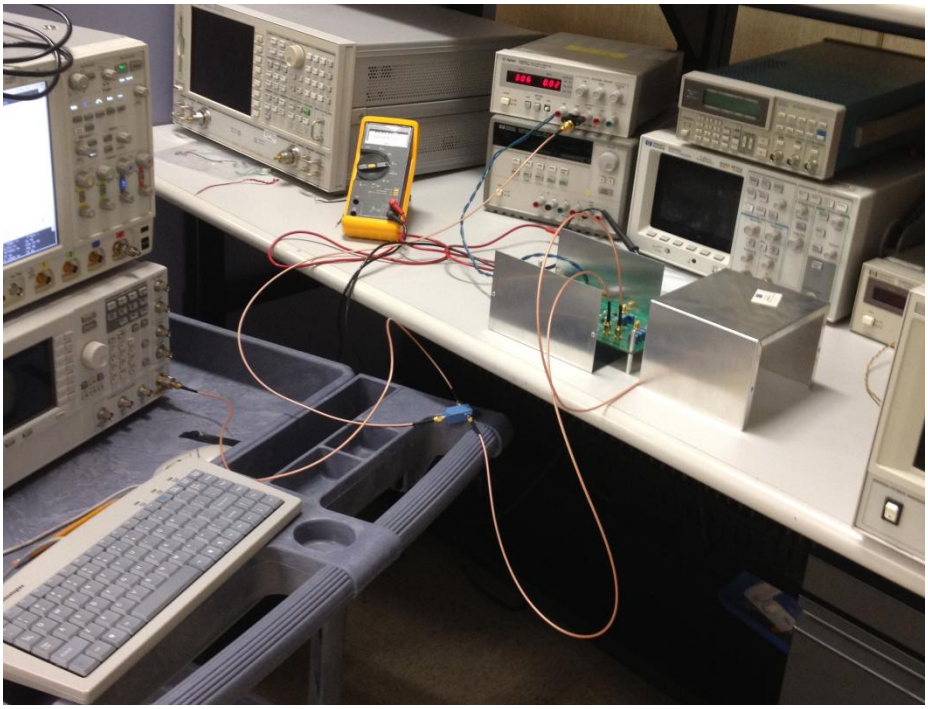


Fig. 6. 5. Lab testing setup

6.2 Testing Results

In order to clearly comprehend the EMI effects on the operational amplifiers, the output offset voltage was measured at 15 different frequencies: 1MHz, 2MHz, 4MHz, 8MHz, 10MHz, 20MHz, 40MHz, 80MHz, 100MHz, 200MHz, 400MHz, 800MHz, and 1GHz, with two Vpp values of 800mV and 1.6V. The supply voltage is 3V/0V. It is necessary to point out that a voltage will be present at the opamp output which is related to the inherent input offset voltage. This offset is not related to the offset created by applying the RF signal and should not be included when measuring the EMI-induced offset voltage. In order to remove this offset from the multimeter measurement, first the dc output offset of the opamp is sampled multiple times with the RF source of the signal generator turned off; then turn on the RF source and sample the output offset of the op amp again. The averages of these two sampling periods are subtracted, and the difference is the amount of output offset produced by dc rectification of the RF signal [38]. This procedure is repeated for all RF frequencies for which the EMI-induced offset voltage of the opamp is characterized. Four chips have been tested, and the testing results vary within the order of 3%.

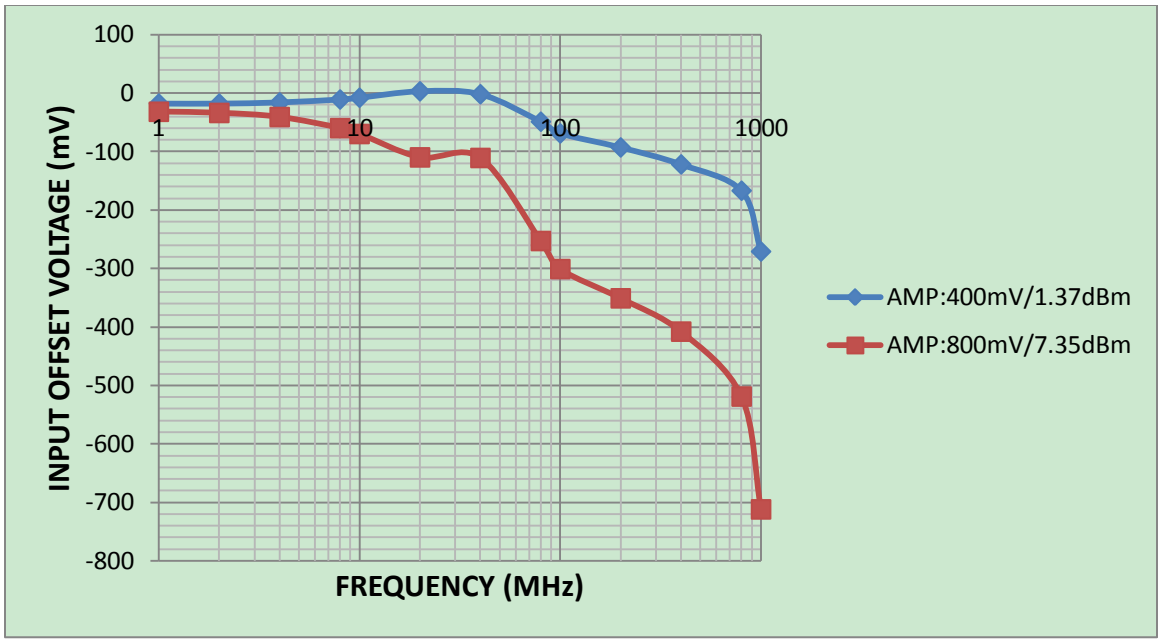


Fig. 6. 6. Offset voltage vs. frequency of conventional folded-cascode circuit

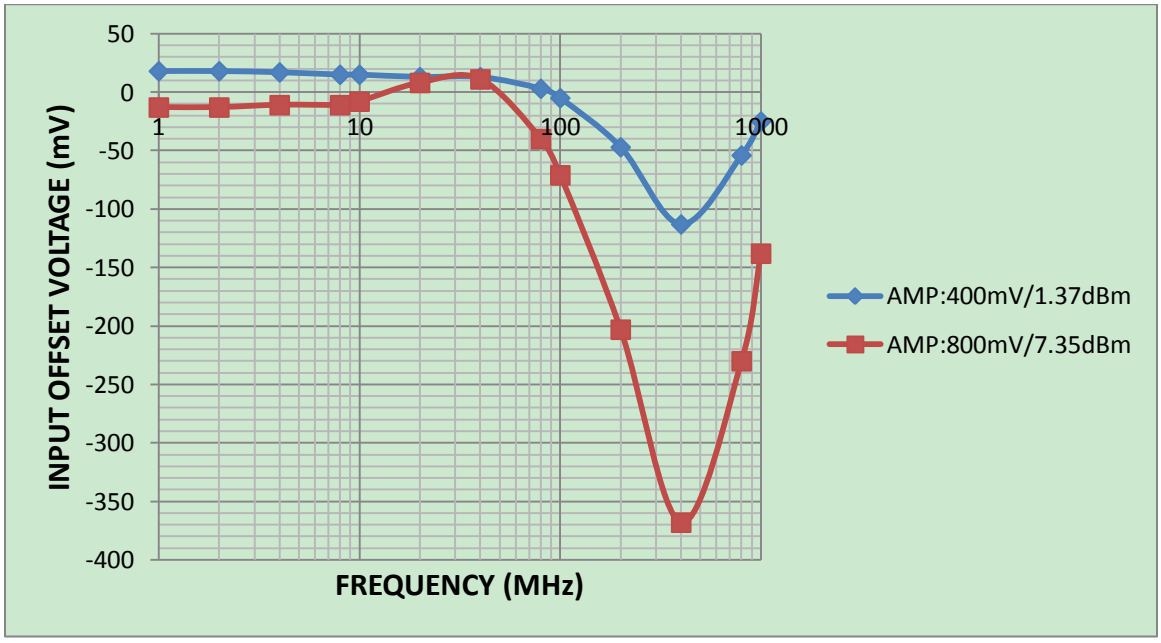


Fig. 6. 7. Offset voltage vs. frequency of structure using published technique

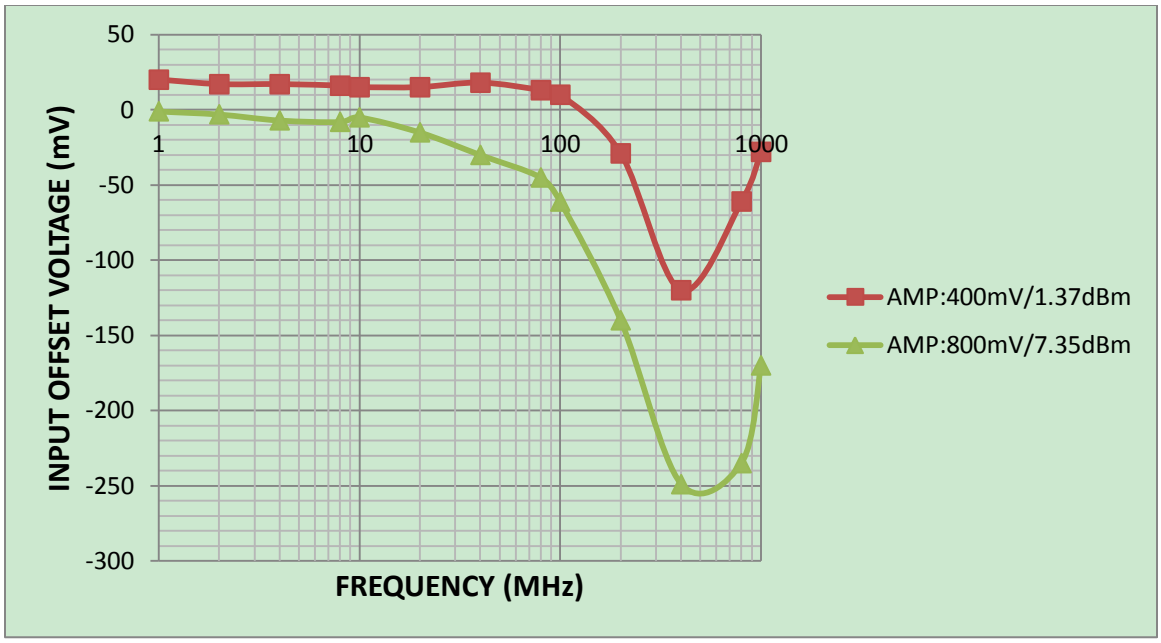


Fig. 6. 8. Offset voltage vs. frequency of proposed structure in 5.2.2

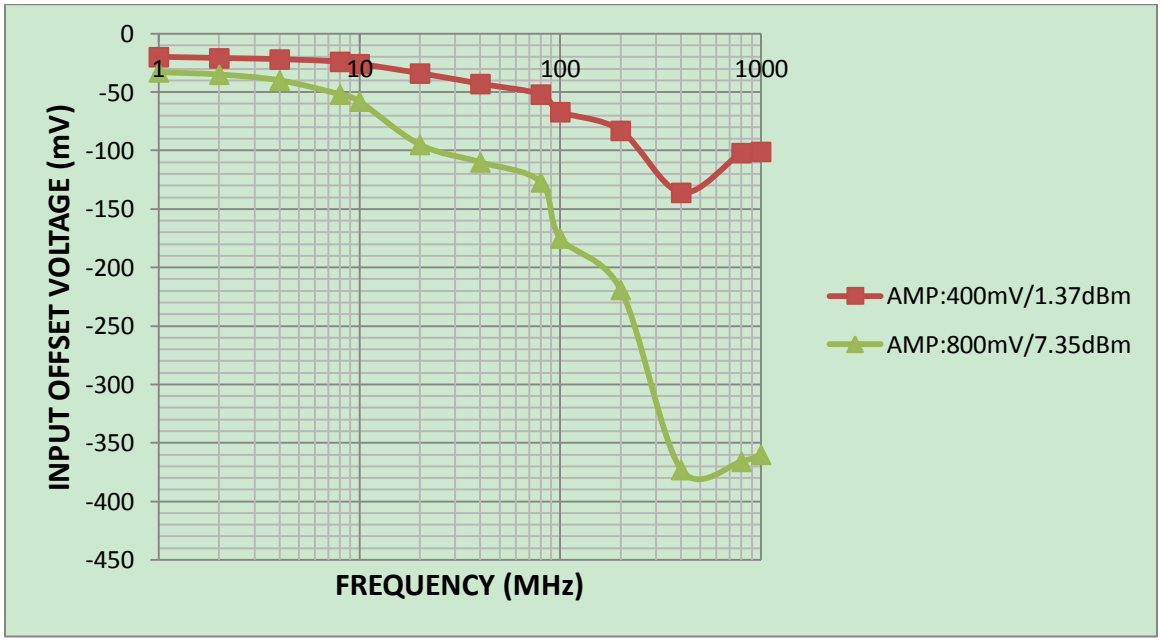


Fig. 6. 9. Testing offset voltage vs. frequency of proposed RS connection

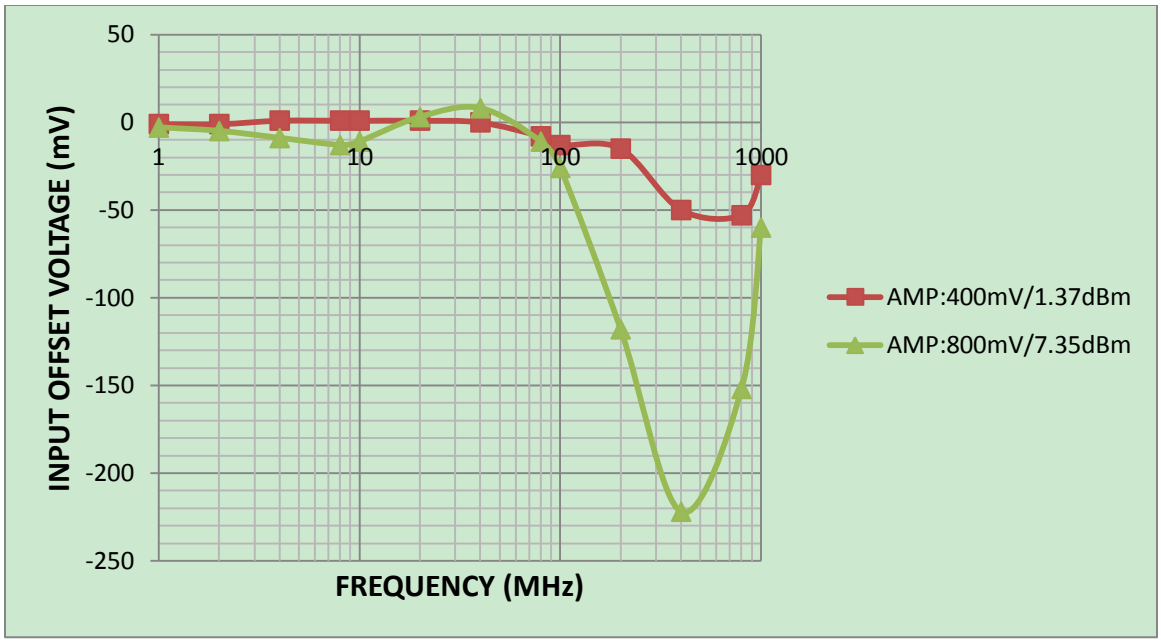


Fig. 6. 10. Offset voltage vs. frequency of proposed source-buffered circuit in 5.2.3

As shown in Fig. 6.6 to 6.10, the EMI performance of the amplifiers is different from the theoretical analysis or the simulation results. For EMI frequencies exceeding 1GHz, the parasitic effects of the DIP40 package and the bonding wires could cause the measured curve to diverge from the theoretical model, of which the EMI-induced offset voltages are not included in the plots; for EMI frequencies lying below 80MHz, the voltage-follower configuration yields inaccurate results, which is due to the configuration not being the worst case during the frequency range.

Fig. 6.11 shows the EMI induced offset voltage comparison results for a large EMI input signal of the 800mV (7.35dBm) amplitude using the voltage-follower configuration.

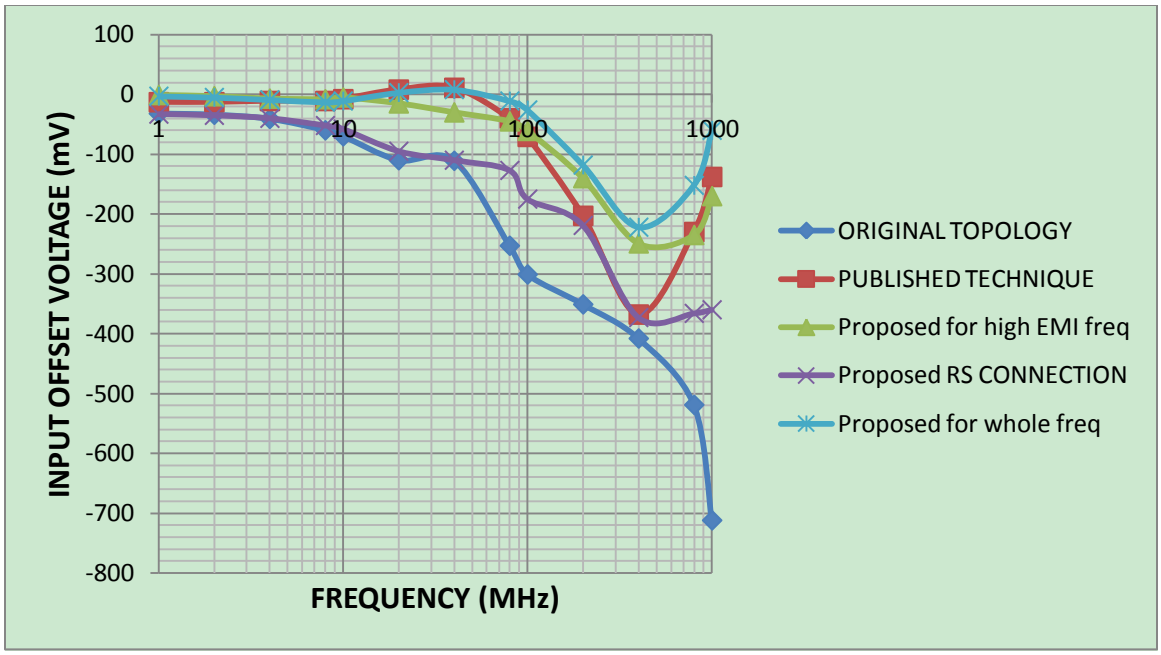


Fig. 6. 11. Testing offset comparison of five different structures when V_{pp} =1.6V

The measured maximal EMI-induced input offset voltage corresponds to -222mV for the 3rd proposed structure, which is compared to -712mV for the conventional one and -368mV for the one using existing source-buffered technique in literature, which means better offset reduction can be achieved by using the proposed structure than by other solutions.

To describe how effectively the opamps reject the EMI effects, a useful metric EMIRR (EMI rejection ratio) defined by [38] is used. EMIRR is a logarithmic ratio where higher decibel values correspond to better rejection and higher immunity. EMIRR is calculated by the following equation. V_{RF_PEAK} is the peak amplitude of the applied RF voltage. ΔV_{OS} is the dc voltage offset shift that takes place in response to the applied RF; it is the input referred change in offset voltage. The second logarithmic term in the equation references the EMIRR to an input signal of 100 mV_P.

$$EMIRR(dB) = 20\log(\frac{V_{RF\_PEAK}}{\Delta V_{OS}}) + 20\log(\frac{V_{RF\_PEAK}}{100mV_P}) \quad (6.1)$$

Figure 6.12 plots EMIRR versus several frequencies for different topologies using the testing offsets and equation (6.1).

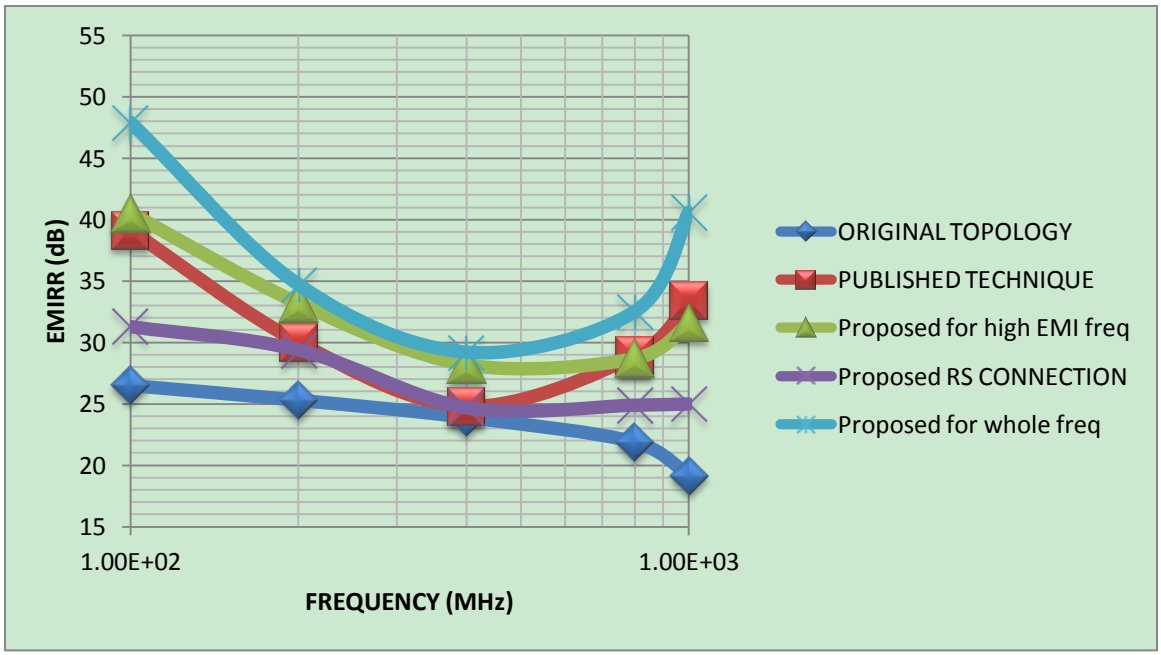


Fig. 6. 12. EMIRR versus frequencies for five different structures when V_{pp} =1.6V

In addition to the EMI performance of the opamps, the measurement of several other typical parameters such as dc gain, power consumption, GBW (Gain-Bandwidth Product), and inherent offset voltage, should be performed too. Table 6.1 and 6.2 summarize the main measured features of the five different amplifiers inside the chips. And Table 6.3 compares the testing results of the proposed topology with best EMI performance with previous works; this work uses NCSU 0.5um and the supply voltage of 3V which represent the worse case for EMI generation compared to previous ones, but still have competitive EMI performance even with higher disturbance signal amplitude and frequency.

Table 6. 1 Testing results I in NCSU 0.5um technology

	Conventional	**Source Buffered**	**Source Buffered with proposed R_S connection**
Adc (dB)	48	38	32
Power (mW)	2.768	3.155	3.464
GBW (MHz)	29	12	12
Inherent Offset (mV)	-3	-53	8
Worst Offset(mV) (AMP=400mV)	-271	-113	-136
Worst Offset(mV) (AMP=800mV)	-712	-368	-373

Table 6. 2 Testing results II in NCSU 0.5um technology

	2nd Proposed Topology	**3rd Proposed Topology**
Adc (dB)	36	34
Power (mW)	3.183	3.471
GBW (MHz)	12	12
Inherent Offset (mV)	-9	--11
Worst Offset(mV) (AMP=400mV)	-120	-53
Worst Offset(mV) (AMP=800mV)	-249	-222

Table 6. 3 EMI performance of 3rd proposed circuit compared to previous works

	LPF [15]	**Source Degeneration [7]**	**Cross-coupled [16]**	**Source-buffered [5]**	**3rd Proposed Topology**
Technology	UMC 0.18um	N/A	BiCMOS 1um	AMIS 0.35um	NCSU 0.5um
Power supply	N/A	N/A	5V/0V	N/A	3V/0V
Gain	N/A	21dB	N/A	51dB	34dB
EMI signal amplitude	200mV	200mV	200mV	750mV	400mV
EMI frequency	3MHz	100MHz	3MHz	200MHz	800MHz
Offset(mV)	-10	500	-45	116	-53

7. MOSIS SUBMISSION PROCESS FOR NCSU 0.5 MICRO KIT

MOSIS offers C5 process runs through on-semiconductor, which is formerly AMIS 0.5um. For those projects using NCSU 0.5um Kit, the submission process is different from that using ON-SEMI/AMIS 0.5um Kit. In this appendix section, how to submit the wafer project in NCSU 0.5um Kit is illustrated in details. First, it is necessary to notice that a design must be no larger than an area of 1.5mm*1.5mm in order to fit into one Tiny Chip unit. Then the submission process is explained as follows.

Submission Procedure:

1. Open the layout and run a DRC. If there are no errors, you are ready to export this file.
2. From the icfb window, click **File → Export → Stream,** you will see a window as the one shown in Fig. 7. 1:

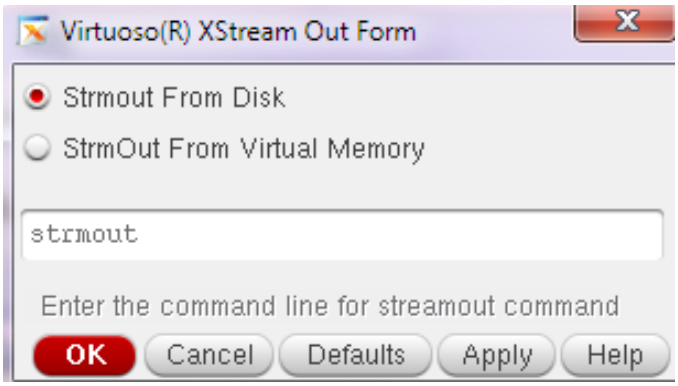


Fig. 7. 1. Xstream out window

Click **OK**.

Then another window will open up as the one shown in Fig. 7.2. Give a new name for the **Stream file*,** for example, emitemp.gds. For **Technology Library**, select

NCSU_TechLib_ami06; for **Library***, select the one which your final layout is in; **Toplevel Cell(s),** select the cell which the layout is in; **View**: your final layout.

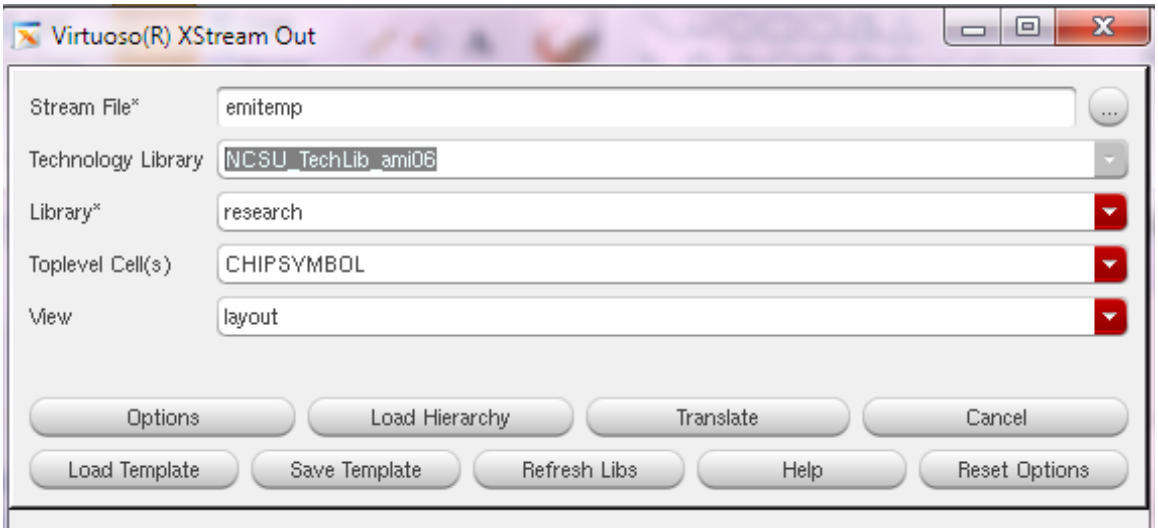


Fig. 7. 2. Xstream out with new definitions

3. Select the proper **Layer Map Table** in Fig. 7. 3**:** Click **Options → Layers**; then **Load file**, add the folder where GDS layer map for your technology is located: **(/amsc/ncsu1.6/pipo/streamInLayermap**)

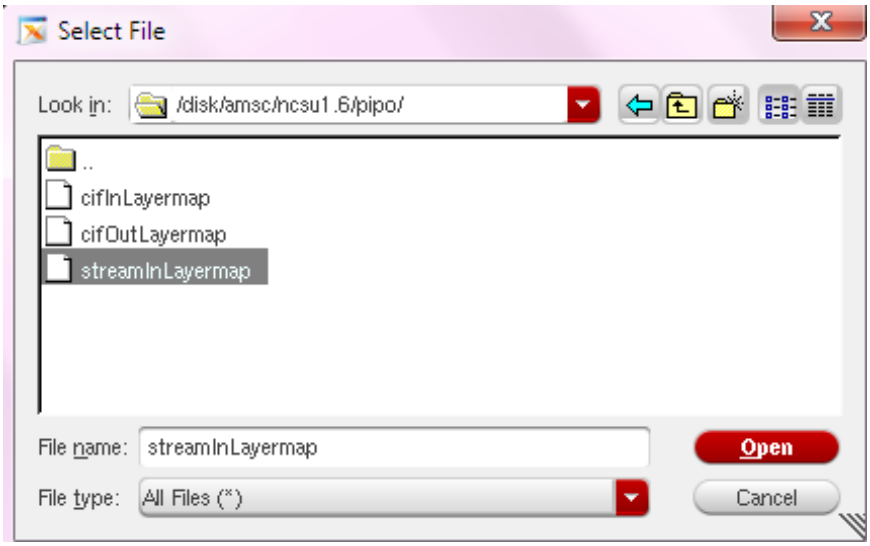


Fig. 7. 3. Select proper layer map table file

For NCSU 0.5Kit, during streaming out, two more mappings should be added in the Layer Map Table in Fig. 7. 4: **nactive, and pactive**; otherwise, there will be **missing layer (ACTIVE) error** when you try to submit to the MOSIS.

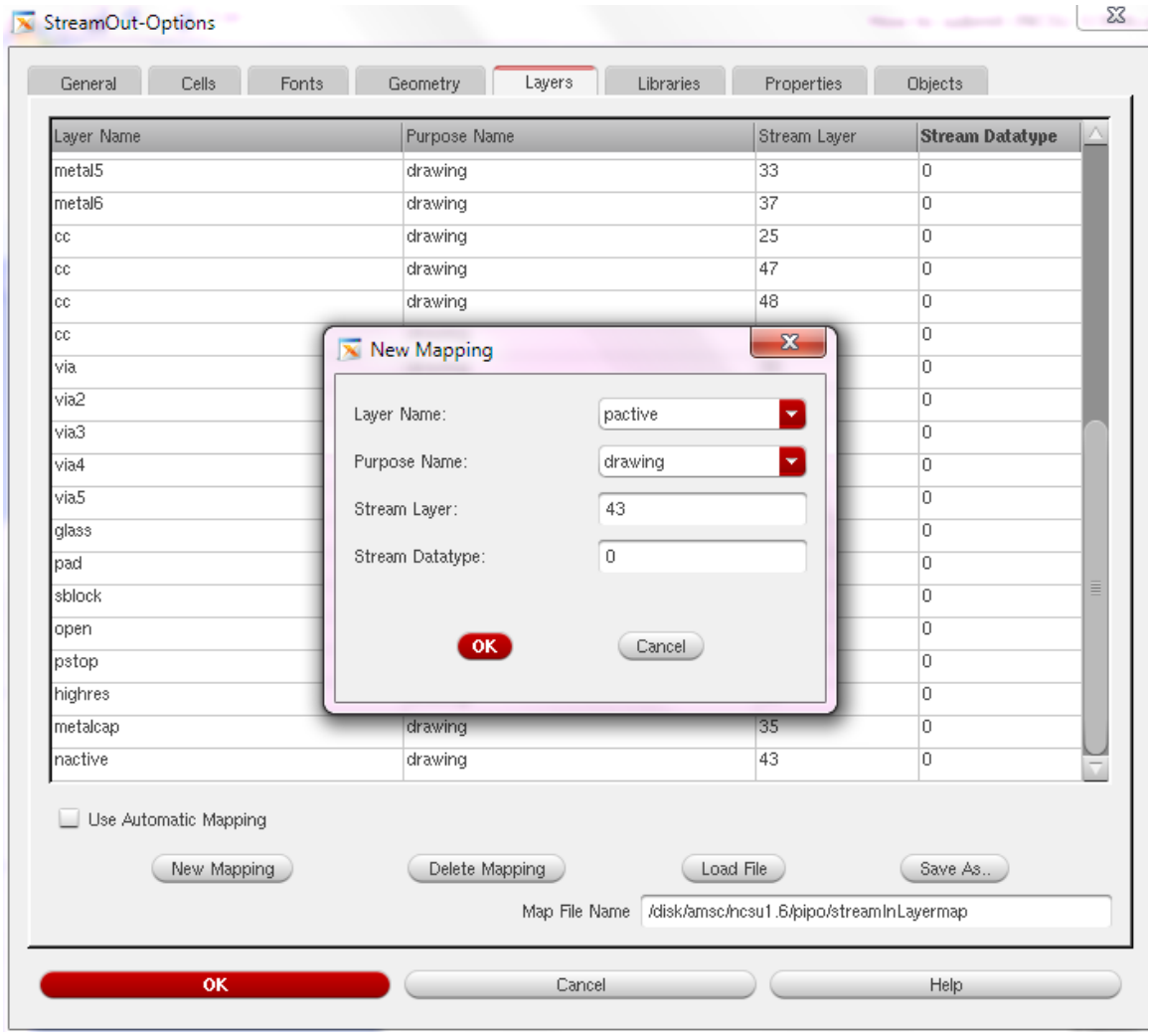


Fig. 7. 4. Add two more mapping layers

4. Go back to the icfb window and create a new library (e.g. emistrmtemp). This library should be clean of everything and attached to the technology you will be fabricating in (**NCSU_TechLib_ami06**). Once it is done, the streaming in should be started.

5. **File → Import → Stream: Stream File*:** select the stream file **filename.gds** created when streaming out, here is emitemp.gds; **Destination Library*:** select the library created in Step 4; **Attach Technology Library: NCSU_TechLib_ami06**; **Top Cell**: should be the **filename**, here is emitemp in Fig. 7. 5.

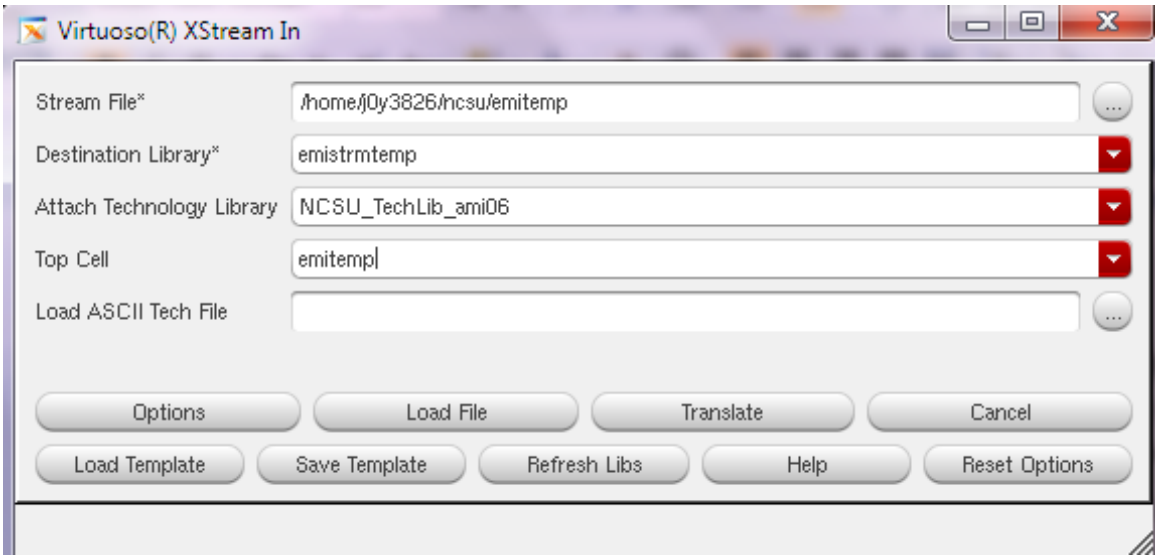


Fig. 7. 5. Xstream in window

Click **Options** in Fig. 7. 6: **Run Directory**: should be the directory where you run your cadence; **Uncheck the Overwrite Existing Cells**, in order to avoid some warnings that can be ignored.

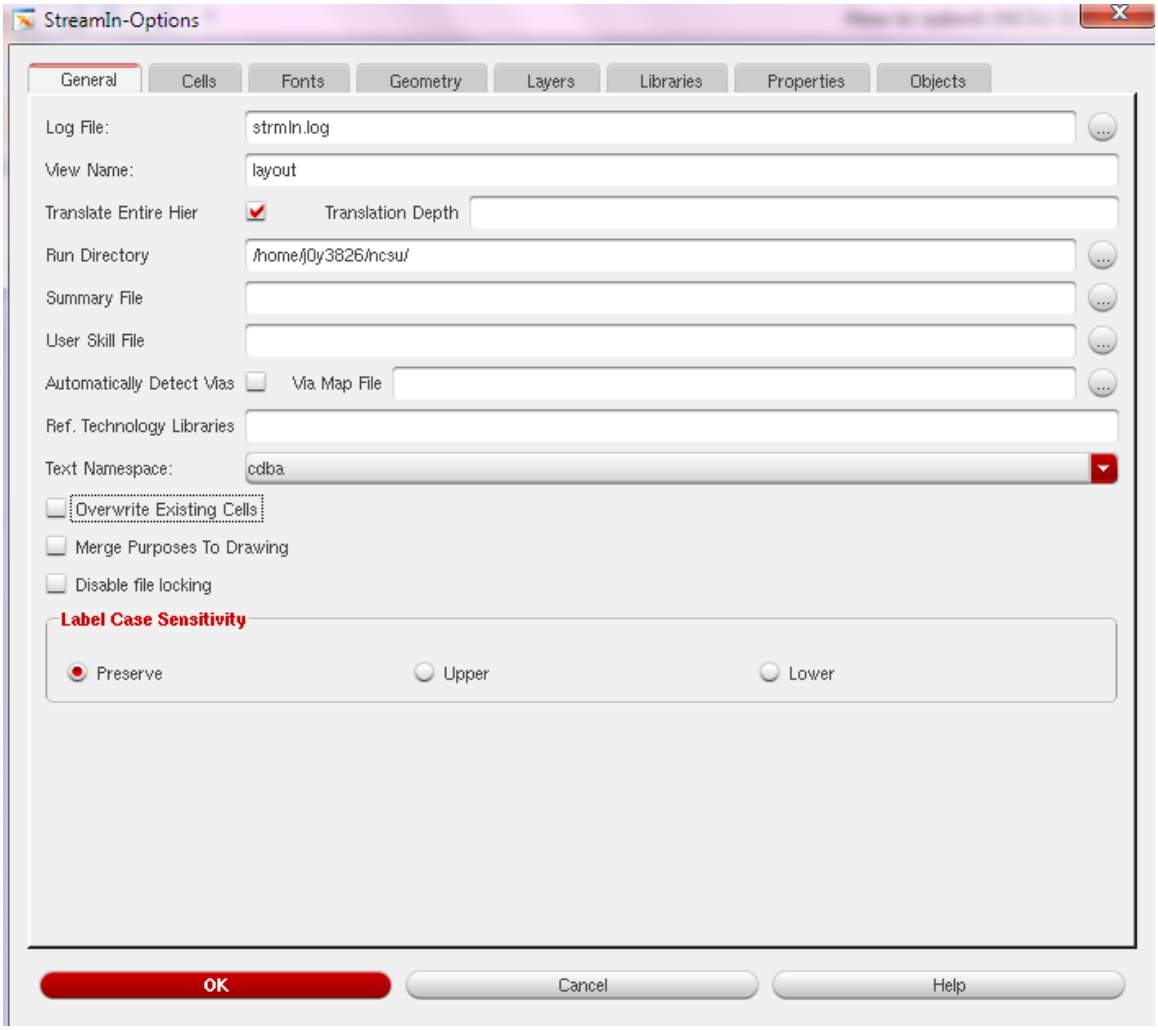


Fig. 7. 6. Stream in window-general option

6. If you are using the existing technology file for which you don't have write permission [37]: click "Options"→"**Geometry**" in Fig. 7. 7, check **"Skip Undefined Layer Purpose Pair".** So usually in our situations, we should check it.

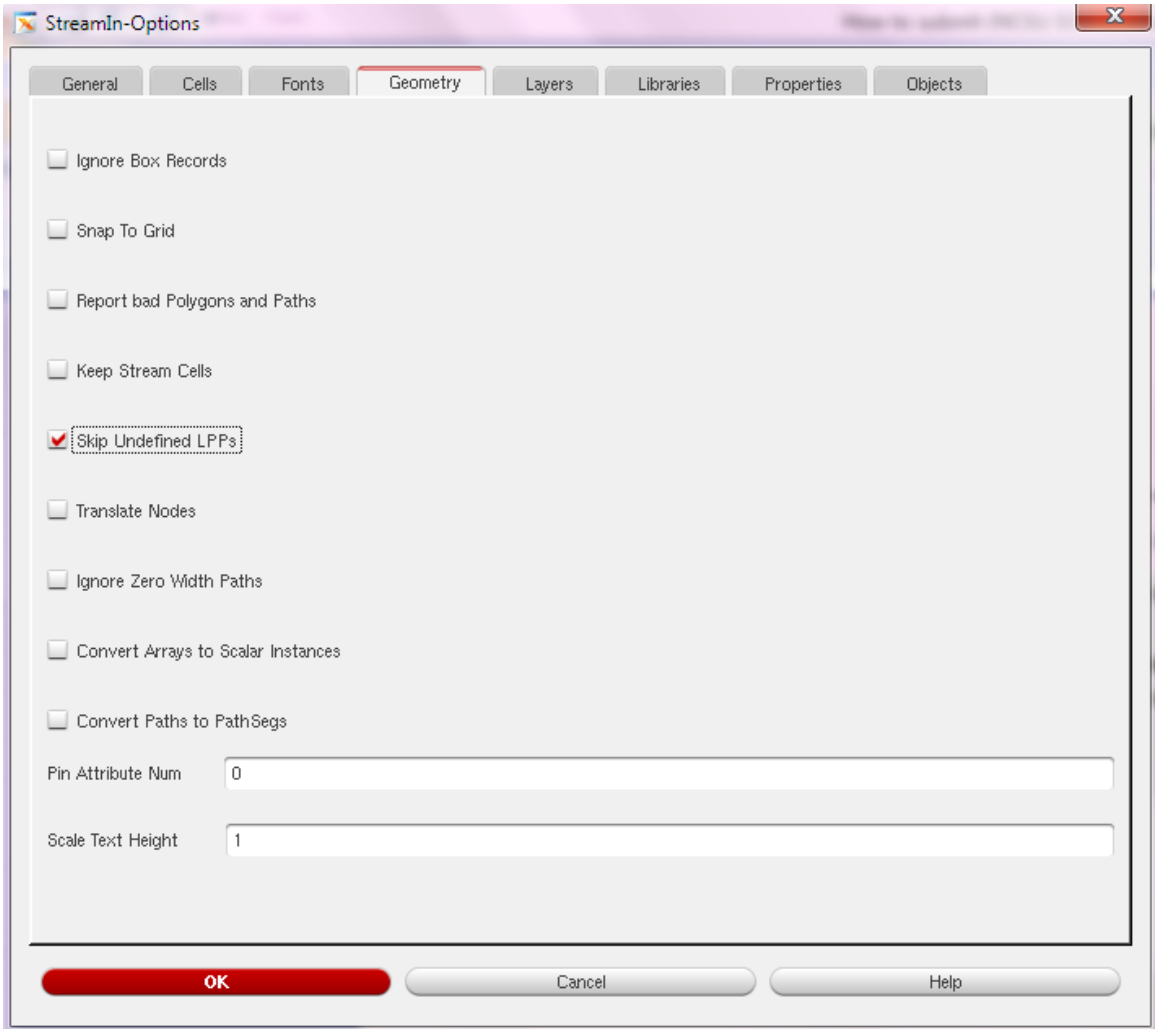


Fig. 7. 7. Stream in window-geometry option

7. Select the proper **Layer Map Table:** Click **Options → Layers**; then **Load file**, add the folder where GDS layer map for your technology is located:

(/amsc/ncsu1.6/pipo/streamInLayermap).

When streaming in, you don't need to add nactive or pactive, because they are simply convenience layers for the user, not mask layers, and are treated as "active" for the purposes of streaming out, DRC and extraction [37].

8. Install the mosiscrc.c on your account. You can find the source code or the executable at http://www.mosis.com/support/mosiscrc.c or http://www.mosis.com/support/mosiscrc.exe. Go to the terminal, type in the command: **gcc -O3 -o mosiscrc mosiscrc.c,** and then **./mosiscrc –b filename.gds**. The resulting 10 digit and 6 digit numbers in the terminal will be the CHECK SUM and COUNT.
9. Then you can submit your chip to MOSIS.

8. CONCLUSIONS

This thesis gives introduction of EMI fundamental knowledge, and presents three dominant factors which are EMI sources, nonlinear distortion and parasitic capacitance correlated to EMI susceptibility. And this work has also analyzed and compared the performance of different existing EMI-resisting structures, e.g. EMI-Induced input offset voltage.

EMI-robust analog circuits are proposed, of which the architectures are based on source-buffered differential pair in literature. They were fabricated in NCSU 0.5um CMOS technology. Experimental results are presented in terms of EMI immunity, and compared with a conventional and an existing circuit. Moreover the overall performances of the circuits such as current consumption or input referred noise are provided with the corresponding simulation results as well.

REFERENCES

[1] A. Richelli, L. Colalongo, and Z. M. Kovacs-Vajna, "Increasing the immunity to electromagnetic interferences of CMOS OpAmps," *IEEE Transactions on Reliability*, vol. 52, no. 3, September 2003.

[2] F. Fiori, P. S. Crovetti, "Investigation on RFI effects in bandgap voltage references," *Microelectronics Journal,* vol. 35, pp. 557-561, 2004.

[3] F. Fiori, "On the susceptibility of analog circuit to EMI," in *Proc. of Advances in Analog Circuit Design (AACD)*, Apr. 2006, pp. 183-202.

[4] G. Masetti, S. Graffi, D. Golzio, and Z. M. Kovacs-Vajna, "Failures induced on analog integrated circuits from conveyed electromagnetic interferences: A review," *Microelectronics and Reliability*, vol. 36, no. 7/8, pp. 995-972, 1996.

[5] G. Setti and N. Speciale, "Design of a low EMI susceptibility CMOS operational amplifier," *Microelectronics and Reliability*, vol. 38, pp. 1143, 1998.

[6] G. Masetti, G. Setti, and N. Speciale, "On the key role of parasitic capacitances in the determination of susceptibility to EMI of integrated operational amplifiers," in *Proc. EMC Zurich*, 1999, pp. 625-630.

[7] Z. M. Kovacs-Vajna, E. Sardini, and N. Speciale, "Chaotic behavior of 741 OpAmps subjected to EMI conveyed to power supply rails," in *Proc. ISCAS2000 Geneva*, vol. 1, May 2000, pp. 727-730.

[8] J. –M. Redoute and M. Steyaert, *EMC of Analog Integrated Circuits*. Springer, New York: Ohio State Univ. Press, 2010.

[9] B. Keiser, *Principles of Electromagnetic Compatibility*. Ann Arbor, Michigan, U.S.A.: Artech House, 1987.

[10] A. S. Poulton, "Effect of conducted EMI on the DC performances of operational amplifiers," *Electronics Letters,* vol. 30, pp. 282-284, 1994.

[11] F. Fiori, "Integrated circuit susceptibility to conducted RF interference," http://www.ce-mag.com/archive/2000/novdec/fiori.html, 02/13/2012.

[12] J. –J. Laurin, S. G. Zaky, and K. G. Balmain, "Prediction of delay induced by in band RFI in CMOS inverters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 37, no. 2, pp. 167-174, 1995.

[13] J. F. Chappel and S. G. Zaky, "EMI effects and timing design for increased reliability in digital systems," *IEEE Transactions on Circuits and Systems I*, vol. 44, no. 2, pp.130-142, 1997.

[14] S. Graffi, G. Masetti, and A. Piovaccari, "Criteria to reduce failures induced from conveyed electromagnetic interference on CMOS operational amplifier," *Microelectron. Reliab.,* vol. 37, no. 1, pp.95-113, 1997

[15] J. –M. Redoute and M. Steyaert, "A CMOS source-buffered differential input stage with high EMI suppression," in *Proc. Eur. Solid-State Circuits Conf.*, Sep 2008, pp. 318-321.

[16] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Dordrecht, the Netherlands: Kluwer Academic, 1998.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, U.S.A.: McGraw-Hill, 2001.

[18] J. Glyn, *Modern Engineering Mathematics*. Vaasa, Finland: Pearson Prentice Hall, 2007

[19] M. Yavari, N. Maghari, and O. Shoaei, "An accurate analysis of slew rate for two-stage CMOS opamps", *IEEE Transactions on Circuits and Systems II*, vol. 52, no. 3, pp. 164-167, 2005.

[20] M. Corradin, G. Spiazzi, and S. Buso, "Effects of radio frequency interference in OPAMP different input stages", in: *Proc. of International Symposium on Electromagnetic Compatibility,* Aug. 2005, vol. 3, pp. 866-871.

[21] G. B. Arfken and H. J. Weber, *Mathematical Methods for Physicists*. San Diego, U.S.A.: Academic Press, 1995.

[22] M. R. Spiegel, *Schaum's Outline of Theory and Problems of Fourier Analysis: With Applications to Boundary Value Problems*. New York, U.S.A.: McGraw-Hill, 1974.

[23] F. Michel, and M. Steyaert, "Comparison of high impedance input topologies with low EMI susceptibility", *Analog Integrated Circuit Signal Process,* vol. 65, pp. 299-309, 2010.

[24] F. Fiori and P. S. Crovetti, "Nonlinear effects of radio-frequency interference in operational amplifiers", *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.* vol. 49, no. 3, pp. 367-372, Mar. 2002.

[25] M. R. Spiegel, *Schaum's Outline of Theory and Problems of Laplace Transforms*. New York, U.S.A.: McGraw-Hill, 1994.

[26] Y. Zinzius, E. Lauwers, G. Gielen, and W. Sansen, "Evaluation of the substrate noise effect on analog circuits in mixed-signal designs", in *Proc. of the Southwest Symposium on Mixed-signal Design (SSMSD),* Feb. 2000, pp. 131-134.

[27] M.T. Abuelma'attit, "Analysis of the effect of radio frequency interference on the DC performance of CMOS operational amplifiers", *Analog integrated circuits and signal processing (Springer),* vol. 45, pp. 123–130, 2005.

[28] C. Walravens, S. Van Winckel, J. –M Redoute, and M. Steyaert, "Efficient reduction of electromagnetic interference effects in operational amplifier", *IEE Electronics Letters*, vol. 43, no. 2, pp. 84-85, 2007.

[29] F. Fiori, "Operational amplifier input stage robust to EMI", *IEE Electronic Letters*, vol. 37, no. 15, pp. 930-931, 2001.

[30] J. –M. Redoute and M. Steyaert, "EMI resisting CMOS differential pair structures", *IEE Electronics Letters*, vol. 42, no. 21, pp. 1217-1218, 2006.

[31] A. Hasting, *The Art of Analog Layout*. New York, U.S.A.: Prentice Hall, 2001.

[32] W. Sansen, *Analog Design Essentials*. Leuven, Belgium: Springer Verlag, 2006

[33] J. G. Tront, J. J. Whalen, C. E. Larson, and J. M. Roe, "Computer-aided analysis of RFI effects in operational amplifiers", *IEEE Trans. Electromagn. Compat.,* vol. EMC-21, pp. 297-306, Nov. 1979.

[34] S. Graffi, G. Masetti, and D. Golzio, "EMI-Induced failures in integrated circuit operational amplifier", *Microelectron, Rel.* vol. 32, no. 11, pp. 1551-1557, 1992.

[35] F. Fiori, "A new nonlinear model of EMI-Induced distortion phenomena in feedback CMOS operational amplifiers", *IEEE Trans.on EMC,* vol. 44, no. 4, Nov. 2002.

[36] A. Richelli, L. Colalongo, Z. M. Kovacs-Vajna, and M. Quarantelli, "Design of an integrated CMOS operational amplifier with low probability EMI induced failures", in *Proc. of the Solid-State Circuits Conference,* Sep. 2001, pp. 361-364.

[37] A. J. Lopez Martin, *Tutorial Cadence Design Environment*. New Mexico State, U.S.A.: Klipsch School of Electrical and Computer Engineering, New Mexico State University, Oct. 2002

[38] C. Hall and T. Kuehl, "EMI Rejection Ratio of Operational Amplifiers," Texas Instruments, SBOA 128, Aug. 2011

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