HIGH PERFORMANCE CLASS-AB OUTPUT STAGE OPERATIONAL AMPLIFIERS FOR CONTINUOUS-TIME SIGMA-DELTA ADC

A Thesis

by

LAKSHMINARASIMHAN KRISHNAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
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ABSTRACT

High Performance Class-AB Output Stage Operational Amplifiers for Continuous-time Sigma-delta ADC. (August 2011)

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Chair of Advisory Committee: Dr. Jose Silva-Martinez

One of the most critical blocks in a wide-band continuous time sigma delta (CTSD) analog-to-digital converter (ADC) is the loop filter. For most loop filter topologies, the performance of the filter depends largely on the performance of the operational amplifiers (op-amps) used in the filter. The op-amps need to have high linearity, low noise and large gain over a wide bandwidth.

In this work, the impact of op-amp parameters like noise and linearity on system level performance of the CTSD ADC is studied, and the design specifications are derived for the op-amps. A new class-AB bias scheme, which is more robust to process variations and has an improved high frequency response over the conventional Monticelli bias scheme, is proposed. A biquadratic filter which forms the input stage of a 5^{th} order low pass CTSD ADC is used as a test bench to characterize the op-amp performance. The proposed class-AB output stage is compared with the class-AB output stage with Monticelli bias scheme and a class-A output stage with bias current reuse. The filter using the new op-amp architecture has lower power consumption than the other two architectures. The proposed class AB bias scheme has better process variation and mismatch tolerance compared to the op-amp that uses conventional bias scheme.

DEDICATION

To God

To my parents

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1. INTRODUCTION

1.1 Motivation

The rapid growth in the wireless communication industry has increased the performance expectations from analog and RF circuits. The next generation products are aimed at integrating multiple communication standards into a single chip [1]. Digital signal processing techniques are gaining large popularity for these implementations. Digital circuits occupy smaller area, are more robust to process variations and provide a large dynamic range at a low cost. In order for the digital circuits to interface with the real world analog signals ADCs are needed. Hence the performance of ADCs is extremely critical for rapid development of DSP solutions. Figure 1 shows the architecture of a generic wireless receiver. While demands from the RF and analog circuits are increased, the increase in process variations with each new process generation motivates the designer to move the ADC as much closer to the antenna as possible. This facilitates in performing filtering and frequency translation in the digital domain in a less complex and more reliable fashion. A digital implementation leads to easier portability of circuits across process generations. As the ADC is moved closer to the receiver antenna, the demands on the speed and dynamic range of the ADC become severe.

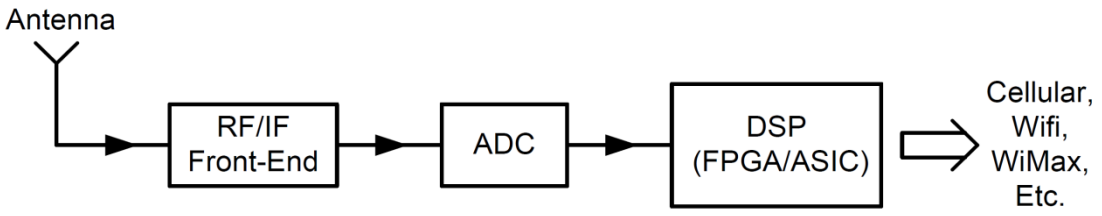

Figure 1 Generic wireless receiver architecture

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

Continuous-time sigma-delta (CTSD) ADC is considered as a viable solution for several wireless receiver applications where large bandwidth (> 10MHz bandwidth) and high resolution (≥ 11 bits) are required [2]. Figure 2 shows the block diagram of a generic continuous-time sigma-delta ADC.

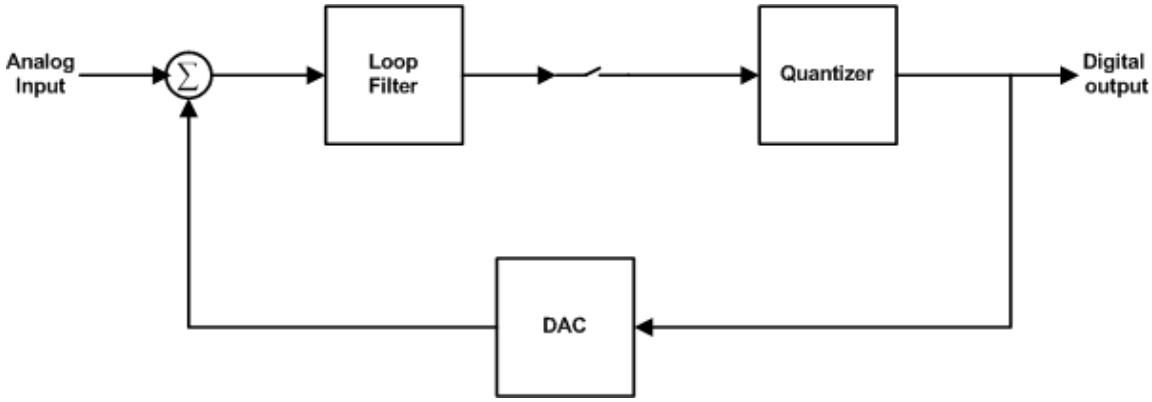

Figure 2 Block diagram of a generic continuous-time sigma-delta ADC

The loop filter is a critical analog block in the design of a continuous-time sigma-delta ADC. The transfer function of the loop filter in the CTSD ADC determines the noise transfer function of the ADC. The stability of the ADC depends on the locations of the poles and zeros of the filter. High bandwidth and high resolution of the ADC translates into high bandwidth and high order loop filters. The loop filters used in sigma delta ADCs have a pass-band gain greater than unity, hence active filter topologies are used to implement the loop filter.

The performance of any active filter depends largely on the performance of the op-amps used in the filter. The gain-bandwidth product of an op-amp used in an active filter needs to be much greater than the gain-bandwidth product of the filter, so that the op-amp appears to be ideal over the frequency range of interest. In a wide band, high performance ADC, the loop filter has a high pass band gain and a large bandwidth; hence the op-amps need to have a very large gain-bandwidth product.

Thermal noise and noise due to non-linearity of the circuit blocks in the ADC should be well below the quantization noise power of the ADC in-order for the ADC to

realize the desired resolution. The loop filter is at the input of the ADC, and any input referred noise from the filter adds directly to the input signal and significantly degrades the signal to noise ratio of the ADC. Hence the op-amps used in designing the filter need to have low input referred noise and a highly linear output swing greater than or equal to the full scale swing of the ADC while being loaded by small resistors (larger resistors produce more thermal noise).

Most of the wireless receivers are portable in nature; this naturally poses a limit on the power consumption of the components used. In a CTSD ADC a major portion of the power consumption is contributed by the filter. Since in most active filters the number of op-amps used increase with the order of the filter, in a higher order filter, even a small reduction in power of the individual op-amps could lead to significant power savings in the entire filter. Hence the design of such low-power, large gain-bandwidth, low noise and highly linear op-amps pose a significant challenge.

In a wireless receiver, the input signal power received is much smaller than the full scale power that the receiver can handle most of the time. The input signal power equals the full scale power less frequently. Hence circuits with high power efficiency are desired to reduce the static power consumption. In the particular case of op-amps used in the loop-filter of a CTSD ADC, the idea of increasing power efficiency motivates us to explore the use of class-AB amplifiers in this thesis.

In this work, the problem of designing low power, high performance op-amps suitable for use in the loop filter of a continuous time sigma delta ADC has been addressed. The effects of non-idealities of the loop filter on the performance of the CTSD ADC have been studied and the generic design criteria that the op-amps need to meet are obtained. An existing loop filter implementation is chosen (from [3]) and the design specifications of the op-amps needed are identified. The merits and de-merits of using a class-AB output stage in the amplifiers used in the filter is highlighted. A new class-AB output stage that is robust to process variations and provides good high-frequency response is proposed. Op-amps using the new class-AB output stage and the conventional class-AB bias technique (Monticelli bias scheme [4]) are designed to match

the specifications of the existing amplifiers in [3], and comparisons are made between the three amplifiers. Filters are designed using the three amplifier topologies and the filter performances are compared.

1.2 Thesis organization

The organization of this thesis is highlighted next. Section 2 briefly outlines the working of an ideal CTSD ADC. It highlights the non-idealities of the loop filter that impact the overall performance of the ADC.

Section 3 introduces the loop filter that was designed in [3]. Noise contribution of each element in the filter is derived. The design criteria for the amplifiers are obtained.

Section 4 discusses the amplifier topology in detail and analyses the merits and de-merits of a class-A output stage and a conventional class-AB output stage with Monticelli bias. The new class-AB output stage is introduced and analyzed. A comparison between the three output stages are made by embedding them in an amplifier.

Sections 5 and 6 present a comparison of the amplifiers by embedding them into a biquadratic filter. Section 5 presents the schematic-simulation results and Section 6 presents the post-layout simulation results.

Section 7 presents the conclusion of the thesis.

2. CONTINUOUS TIME SIGMA DELTA ADC

This section describes the architecture and working of a continuous time sigma delta ADC and emphasizes the performance of the loop filter as the key to enhance the performance of the CTSD ADC. The impact of non-idealities in a practical ADC is outlined. Finally, the non-idealities of the filter and its effects are discussed.

2.1 Ideal continuous-time sigma-delta modulator

Analog signals are continuous in time and amplitude, while digital signals are associated with discrete time instants and discrete levels of amplitude. An ADC converts an analog signal to digital signal by sampling the continuous-time signal at periodic instants in time, holding the sampled value over the entire sampling period and mapping the sampled value to a corresponding digital code. This is illustrated in Figure 3.

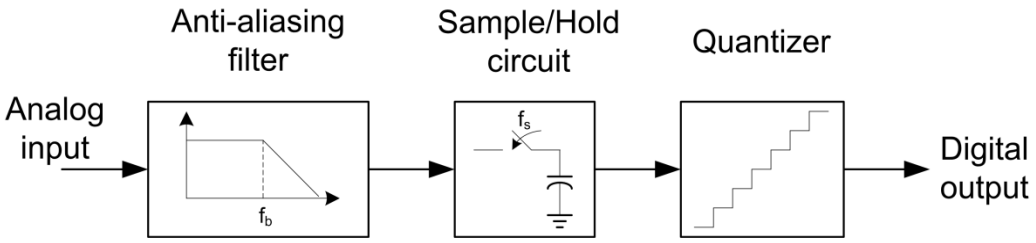

Figure 3 Analog to digital conversion

The sample and hold circuit takes care of discretizing the continuous signal in time domain and the quantizer takes care of mapping the sampled values into digital codes. According to Nyquist criterion, the sampling frequency, f_s, needs to be at least twice the signal bandwidth of interest, f_b, which needs to be processed. If this criterion is not satisfied, the information in the signal bandwidth of interest gets corrupted after sampling due to a phenomenon known as aliasing. If the input signal has some unwanted

frequency information beyond f_b, then it can cause aliasing and corrupt the in-band signal. The anti-aliasing filter takes care of filtering out the signals beyond f_b.

The quantizer maps a signal that is continuous in voltage to discrete levels; hence the process of quantization introduces a quantization noise that is uniformly spread from $-f_s/2$ to $f_s/2$ in the frequency domain. For an N-bit ADC, quantization noise power depends on the quantization step size Δ ($=V_{fullscale}/N$) and is equal to $\Delta^2/12$. The corresponding signal to quantization noise ratio (SQNR) of the ADC is given as, [5]

$$\mathrm{SQNR(dB)} = 6.02\mathrm{N} + 1.76\ \mathrm{dB} \tag{2.1}$$

If the sampling frequency of the ADC is increased beyond the Nyquist value of $2*f_b$, then the quantization noise power is now spread over a wider bandwidth and hence the noise floor is reduced. This in-turn reduces the quantization noise power present in the signal band of interest. This process of increasing the sampling frequency to lower the in-band quantization noise is called over-sampling, and the ratio of the sampling frequency in the over-sampling case to the Nyquist sampling frequency is called over-sampling ratio (OSR). For example, an OSR of 2 will reduce the in-band quantization noise by 3dB. The spreading of the quantization noise due to over-sampling is illustrated in Figure 4.

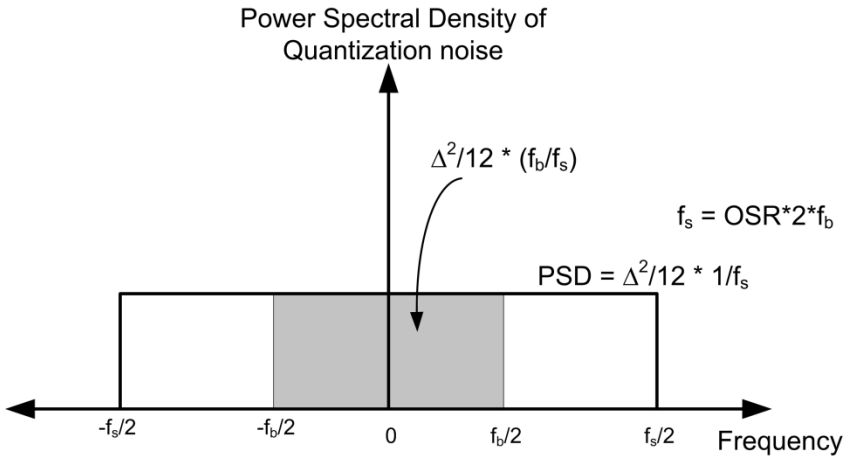

Figure 4 Over-sampling

The improvement in SQNR of the ADC due to over-sampling is given as,

$$\mathrm{SQNR(dB)} = 6.02\mathrm{N} + 1.76\ \mathrm{dB} + 10\log_{10}(\mathrm{OSR}) \tag{2.2}$$

Sigma-delta modulators employ the over-sampling technique to achieve high resolution. Another technique employed to improve the resolution in a sigma-delta ADC is noise-shaping.

In a sigma-delta modulator the in-band noise is attenuated and pushed out of band. This noise shaping can be easily understood from the block diagram shown in Figure 5. The loop of a CTSD ADC consists of a loop filter H(s), which defines the nature of the ADC – low pass or band pass, a quantizer and a DAC in the feedback path. For small signal analysis, the quantizer and the DAC are assumed to have a combined gain of unity and the quantization noise, Q_{noise}, is added at the input of the quantizer. The quantization noise is assumed to be additive white Gaussian noise. H(s) represents the transfer function of the loop filter. Equations (2.3) and (2.4) give the signal transfer function (STF) and noise transfer function (NTF) respectively.

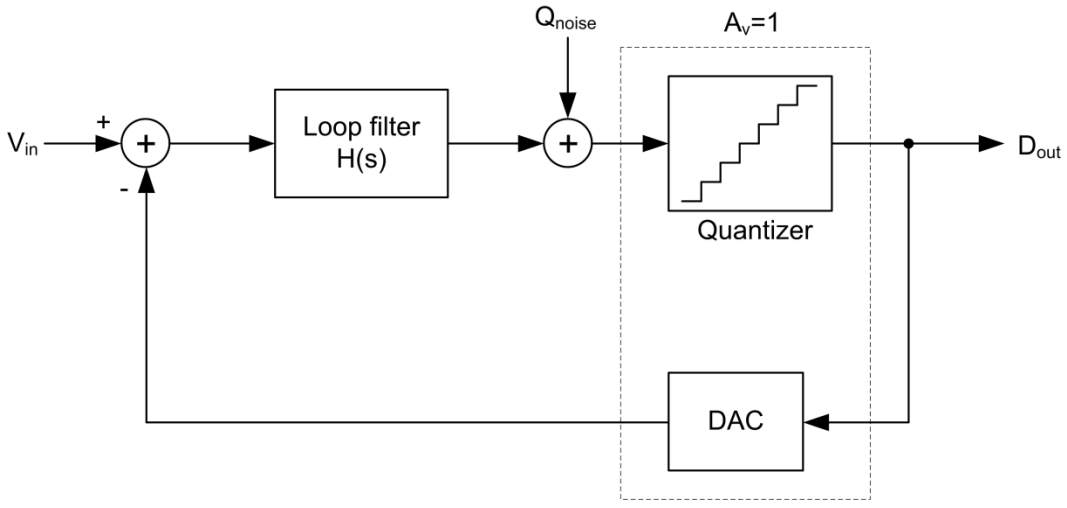

Figure 5 Block diagram of ideal CTSD ADC

$$\mathrm{STF} = \frac{D_{out}}{V_{in}} = \frac{H(s)}{1 + H(s)} \tag{2.3}$$

$$\mathrm{NTF} = \frac{D_{out}}{Q_{noise}} = \frac{1}{1 + H(s)} \tag{2.4}$$

Let's consider the case of a low pass CTSD ADC, where the transfer function H(s) of the loop filter is a low pass transfer function with a pass band gain greater than unity. For frequencies, where H(s) is significantly larger than unity, it can be seen that the STF is almost unity and the NTF is approximately the reciprocal of the gain provided by H(s). As the value of H(s) decreases with increase in frequency, the STF decreases from unity and NTF increases towards unity. Hence the STF has a unity gain response for in-band frequencies, while the NTF attenuates the in-band quantization noise. This attenuation of in-band quantization noise without affecting the STF is the noise-shaping effect of sigma-delta modulators. A simple qualitative sketch of STF and NTF is shown in Figure 6.

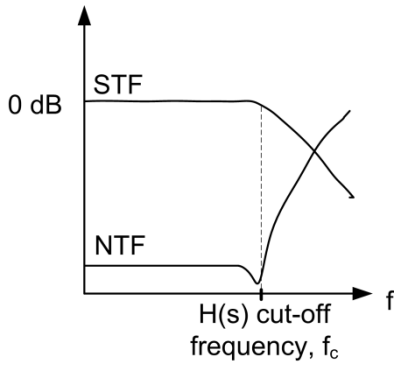

Figure 6 Signal transfer function (STF) and noise transfer function (NTF)

Apart from noise-shaping and over-sampling, the sigma-delta ADC also has an inherent anti-aliasing effect from the loop filter H(s). The expression of SQNR for a sigma-delta ADC is given by equation (2.5) (from [5]).

$$\mathrm{SQNR\ (dB)} = 6.02\mathrm{N} + 1.76 + (20\mathrm{L} + 10)\log_{10}(\mathrm{OSR}) - 10\log_{10}\frac{\pi^{2\mathrm{L}}}{2\mathrm{L}+1} \tag{2.5}$$

In equation (2.5), N indicates the number of bits in the quantizer, L indicates the order of the loop filter transfer function (which is the order of the ADC as well) and OSR is the over-sampling ratio defined earlier. From equation 2.5 we can see that increasing the order of the loop filter L impacts the performance of the ADC significantly. Hence the performance of the loop filter is critical to enhance the performance of the CTSD ADC.

2.2 Non-idealities in a practical ADC

From the previous discussion, we saw that the ideal sigma delta modulator can realize a very high SQNR and hence achieve high resolution by using a higher order filter which has a high pass-band gain and hence greatly attenuates the in-band quantization noise. However, in practice there are several circuit non-idealities which impact the performance of the ADC. The different non-idealities that impact the performance of the CTSD ADC arise from non-idealities in the filter, DAC and quantizer, clock jitter, thermal noise of all circuit components [6].

Figure 7 highlights the non-idealities that impact the performance of the CTSD ADC significantly. The filter non-idealities such as harmonic distortion and thermal noise from the filter have been referred to the input of the filter. This is similar to a noise that is added to the input of the ADC as it has the same transfer function as the input signal information. Hence the filter non-idealities impact the performance of the closed loop ADC greatly. Similarly, the non-idealities of the DAC referred to its output and clock jitter impact the performance of the ADC greatly. The DAC non-idealities are primarily in the form harmonic distortion caused due to mismatch in the DAC elements. Clock jitter gets convolved with the out-of-band noise and raises the in-band noise floor. The noise introduced due to non-idealities in the quantizer is shaped by the sigma-delta

loop, and doesn't impact the performance of the ADC significantly. Hence it has not been shown in Figure 7.

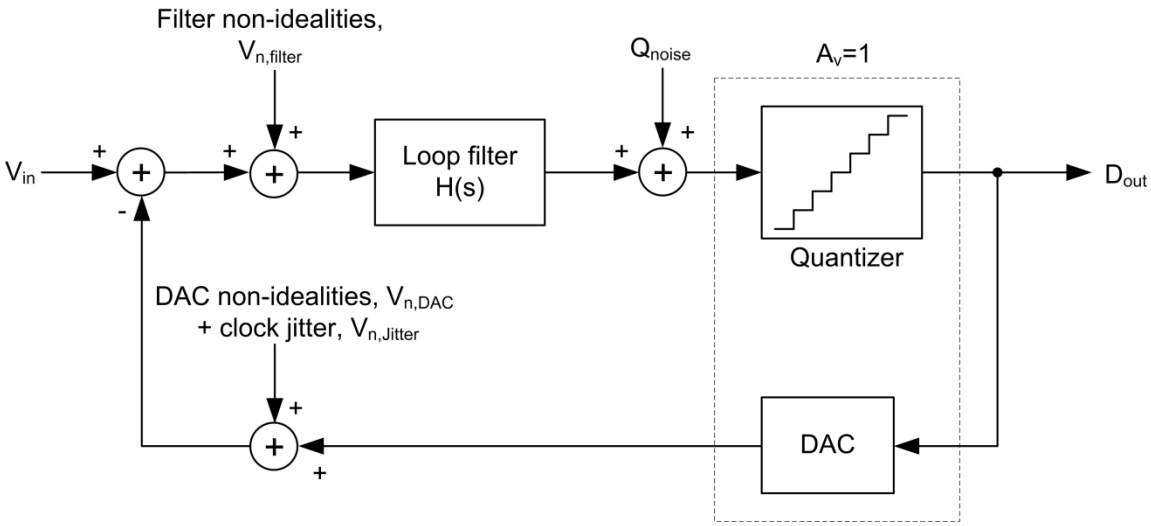

Figure 7 Block diagram of CTSD ADC with significant non-idealities

Equation (2.6) shows the output expression of the ADC in presence of non-idealities.

$$D_{out} = \left(V_{in} + V_{n,filter} + V_{n,DAC} + V_{n,Jitter}\right) * \frac{H(s)}{1 + H(s)} + Q_{noise} * \frac{1}{1 + H(s)} \tag{2.6}$$

It can be seen that the noise voltages due to the non-idealities from the filter, DAC and clock jitter have the same transfer function to the output as the input signal, V_{in}. Hence they directly affect the signal to noise ratio of the ADC.

2.3 Filter non-idealities

The non-idealities of the filter impacting the performance of the ADC manifest itself as harmonic distortion introduced by the filter, thermal noise of the filter, excess phase introduced by amplifiers/transconductors in the filter and the variation of pole-zero locations due to variation in values of the passives across process corners [6]. The excess phase introduced by the filter can cause additional delay to the signal traveling through the loop and lead to stability problems. In order to counter this the amplifiers used in the filter need to introduce minimal excess phase to the signal. Additionally designers resort to several compensation techniques to deal with the problem of loop excess phase of the sigma delta modulator [6, 7, 8]. Variation in the value of passive values is taken care of by trimming or tuning of the resistors or capacitors used. A bank of passive elements is implemented and the value of the passives is tuned by applying a digital code.

The thermal noise at the input of the ADC consists mostly of the input referred thermal noise of the filter, since it is the only input-referred thermal noise present at the input of the ADC. Thermal noise from all other circuit components is shaped by the NTF of the ADC. When we design a CTSD ADC of a certain resolution, in order to realize the signal to noise and distortion ratio (SNDR) corresponding to the resolution, the noise introduced by the non-idealities should be smaller than the quantization noise of the ADC. Hence the input-referred thermal noise of the filter should be much smaller than quantization noise of the ADC, such that the power of thermal noise when added with noise power due to other non-idealities is less than or equal to the quantization noise power. For instance, if we consider an ADC with 12-bit resolution, which ideally promises a SQNR of 74dB, the noise power due to all the non-idealities put together should be at least -74dB smaller than the full scale power of the input signal. [2] indicates that the thermal noise should be smaller than -80dB with respect to full scale power for a 12-bit CTSD ADC. For large bandwidth ADCs, this forms a stringent noise specification on the filter.

Another non-ideal effect which is of large focus in this thesis, is the harmonic distortion introduced by the filter. In Subsection 2.1, we saw that the filter needs to have an in-band gain in-order for the ADC to produce a noise shaping effect. In-order to embed, gain in the filter, the filters need to be active filters which contain a gain element in them. These gain elements (amplifiers) are inherently non-linear. The distortion introduced by the filter should be of the same magnitude as the thermal noise. This imposes stringent linearity requirements on the filter design. Fully differential operation gets rid of even order harmonics, and only odd harmonics of distortion contribute to noise. The linearity of the amplifiers generally relates to linear range of the transistors used in them. The linear range can be increased but at the expense of power consumption. The loop filter in a CTSD ADC is generally realized using a cascade of biquadratic filters and integrators. All the biquadratic filters and integrators possess an in-band gain greater than unity. Hence the noise and distortion of the blocks in the cascade following the first block is shaped by the gain of the first biquadratic filter or integrator (based on the design). The noise and distortion of the first section of the loop filter appears directly at the input of the loop filter and hence the ADC and is most critical. In most CTSD ADCs the SNDR that can be achieved is often limited by the distortion in the first section of the loop filter [3].

3. BIQUADRATIC FILTER DESIGN

The previous section highlighted the importance of the loop filter in a CTSD ADC and indicated that the first section of the loop filter provides the performance bottle neck of the loop filter. In this section, an existing design of a loop filter that has been published in [3, 9] is introduced. The design of the first section of the filter which is a biquadratic filter is explored, and the design constraints that need to be placed on the amplifiers used in the biquadratic filter are discussed.

3.1 Loop filter

In this thesis, our main focus is on developing a new operational amplifier topology for a continuous time sigma delta modulator; hence we make use of an existing design of a continuous time sigma delta modulator reported in literature, identify the specifications of the op-amps in the loop filter and design op-amps using the new topology to strike a comparison. We consider the continuous-time sigma-delta ADC published in [9], which is 5th order low-pass continuous-time sigma-delta ADC with 12-bit resolution and 25 MHz bandwidth and 400MHz sampling frequency. The loop filter of this ADC is shown in Figure 8.

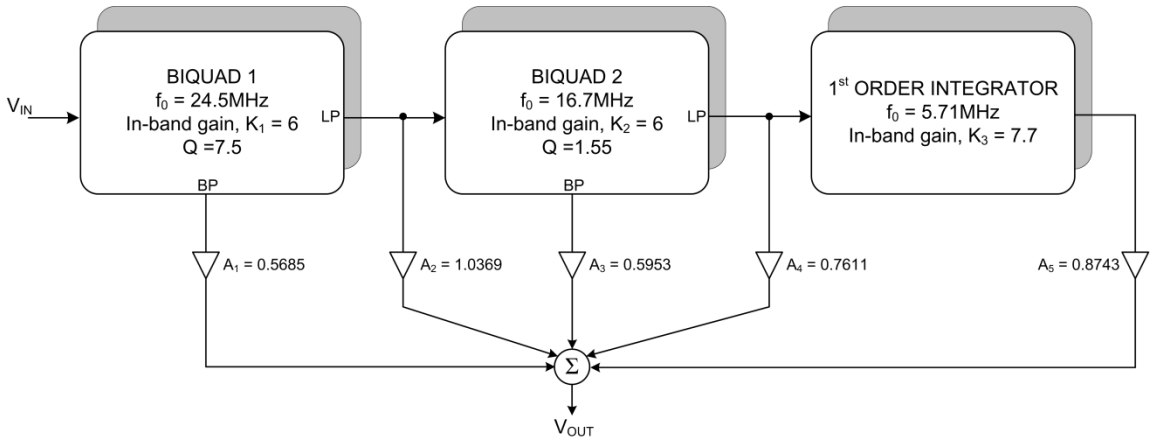

Figure 8 Loop filter in [3, 9]

The 5th order low-pass ADC has a 5th order Chebyshev filter with 25MHz low-pass bandwidth and 49dB pass band gain. The filter achieves an IM3 of -72dB with a full scale swing of $400mV_{p\text{-}p}$ differential swing. The filter consists of two biquadratic filter sections and a lossy integrator as shown in Figure 8. From Figure 8, it can be seen that the loop filter has a feed-forward topology with each biquadratic filter producing a low-pass and band-pass output and the 1st order integrator producing a low-pass output. All the three filter sections have an in-band gain, K_i and a cut-off frequency f_0. Q represents the quality factor of the biquadratic sections, and A_i represents the feed-forward coefficients from the individual outputs to the loop filter output. The transfer function of the overall loop filter, H(s), and the way in which it is split across the three sections is shown in equations (3.1) and (3.2) respectively.

$$H(s) = \frac{5.25e6(s^2 + 3.842e8\,s + 8.821e16)(s^2 + 1.606e5\,s + 5.567e16)}{(s + 3.58e7)(s^2 + 6.78e7\,s + 1.1e16)(s^2 + 2.04e7s + 2.37e16)} \tag{3.1}$$

$$\begin{aligned} H(s) = K_1 &\left(\frac{A_1\frac{s}{\omega_{01}} + A_2}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{01}}}\right) \\ &+ K_2\left(\frac{K_1}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{01}}}\right)\left(\frac{A_3\frac{s}{\omega_{02}} + A_4}{1 + \frac{s}{\omega_{02}Q_2} + \frac{s^2}{\omega_{02}}}\right) \\ &+ K_3\left(\frac{K_1}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{01}}}\right)\left(\frac{K_2}{1 + \frac{s}{\omega_{02}Q_2} + \frac{s^2}{\omega_{02}}}\right)\left(\frac{A_5}{1 + \frac{s}{\omega_{03}}}\right) \end{aligned} \tag{3.2}$$

By looking at the specifications of the three filter sections indicated in Figure 8, it can be easily noted that the first biquadratic filter section has the most stringent requirements on the op-amps since it has the highest quality factor and cut-off frequency (this will be explained in detail later). Hence we focus only on designing the op-amps for the biquadratic filter. In [9], the loop filter is implemented as an active-RC filter. The

design and implementation details of the first biquadratic section are discussed in the next section.

3.2 Active-RC biquadratic filter

Active-RC biquadratic filters provide good linearity at high frequencies but at the expense of power consumption. In the previous sections, we have seen that the first biquadratic section of the loop filter forms the performance bottlenecks of the entire ADC with respect to low noise and linearity. Hence the design of the active-RC filters become challenging due to the contradicting requirement of low-noise and low-power. Also, power savings in the first stage of the sigma-delta ADC contributes to significant power savings for the whole ADC. The design challenge of the active-RC filters boils down to designing the op-amps since they are the elements responsible for non-linearity and power consumption. Figure 9 shows the single-ended equivalent of the active-RC filter implemented in [3] ([3] describes in detail the loop-filter implementation of [9]).

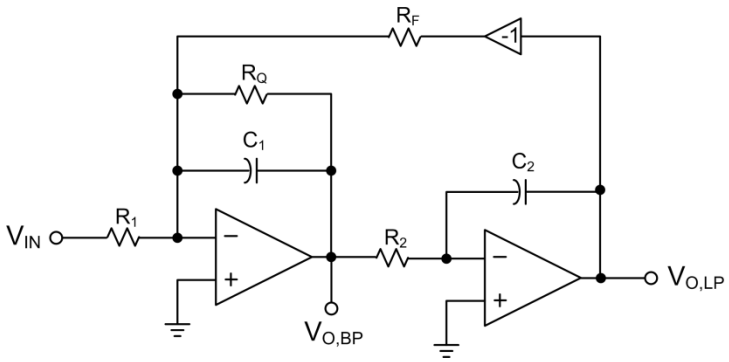

Figure 9 Active-RC biquadratic filter (single-ended)

The design equations used for the filter are listed in equations (3.3), (3.4) and (3.5).

$$f_0 = \frac{1}{2\pi\sqrt{R_2 R_f C_1 C_2}} \tag{3.3}$$

$$Q = \frac{R_Q}{\sqrt{R_2 R_f}}\sqrt{\frac{C_1}{C_2}} \tag{3.4}$$

$$A_v = \frac{R_f}{R_1} \tag{3.5}$$

The transfer function of the filter at the low-pass and band-pass nodes, assuming that the op-amps are ideal with an infinite gain, is given by the expressions in equations (3.6) and (3.7). The resistor and capacitor values used in the design of the first biquadratic section in [3] are shown Table 1.

$$\frac{V_{O,LP}}{V_{IN}} = \frac{\frac{R_f}{R_1}}{1 + sC_2\frac{R_f R_2}{R_Q} + s^2 R_2 R_f C_1 C_2} \tag{3.6}$$

$$\frac{V_{O,BP}}{V_{IN}} = \frac{sR_2\left(\frac{R_f}{R_1}\right)C_2}{1 + sC_2\frac{R_f R_2}{R_Q} + s^2 R_2 R_f C_1 C_2} \tag{3.7}$$

Table 1 Resistor and capacitor values used in the first biquadratic filter

Parameter	**Value**
R_1	1.083 KΩ
R_2, R_f	6.498 KΩ
R_Q	40 KΩ
C_1, C_2	0.7 – 1.4 pF

The capacitors C_1 and C_2 have been implemented with a tuning range in [3]. In our case, since we only need the biquadratic filter as test bench to the new operational amplifier topology, the nominal value of 1pF has been used.

3.3 Noise analysis of the active-RC biquadratic filter

Thermal noise in the active-RC filters arise primarily from the resistors and amplifiers. The noise sources present in the biquadratic filter are shown in Figure 10.

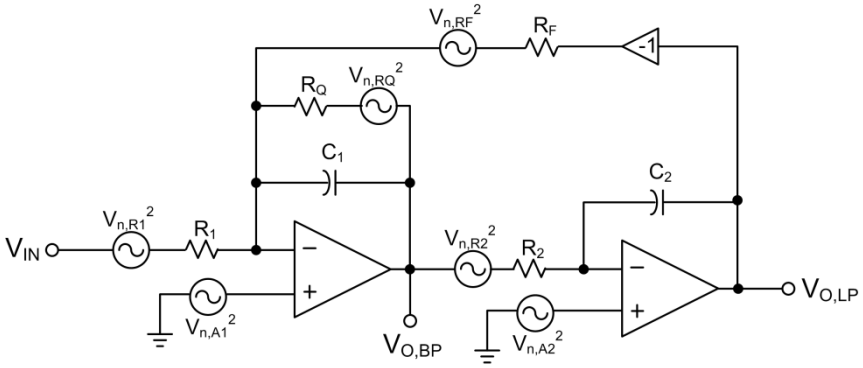

Figure 10 Noise sources in the biquadratic filter

In Figure 10, the noise spectral density of the amplifiers, $V_{n,A1}^2$ and $V_{n,A2}^2$ have been referred to the positive input of the amplifier to simplify the analysis. The thermal noise power spectral density of the resistors is given by $V_{n,Ri}^2 = 4kTR_i$. The input-referred noise of the biquadratic filter can be approximately expressed as

$$V_{in,n}^2 = 4kTR_1\left(1 + \frac{R_1}{R_Q} + \frac{R_1}{R_F}\right) + 4kTR_2|sC_2R_2|^2 + \left(V_{n,A1}^2 + V_{n,A2}^2|sC_2R_2|^2\right)\left|\frac{R_1}{R_Q} + sC_1R_1\right|^2 \quad (3.8)$$

From equation (3.8), it can be seen that the noise of the filter is primarily dominated by the noise due to resistor R_1 at low frequencies. The noise due to the first amplifier is scaled by the ratio R_1/R_Q. The noise due to resistor R_2 and the second amplifier is irrelevant at low frequencies since it is multiplied by the term sC_2R_2. But at high frequencies this noise can become significant.

We already saw that for a 12-bit ADC the thermal noise should be at least -74dB below full scale power (smaller than quantization noise). Since most of the noise is contributed from the first biquadratic filter, we can assume that the noise of the first biquadratic filter should be at least -74dB below full scale power. The full-scale power (0dBFS) corresponding to $400mV_{p\text{-}p}$ differential swing is -14dBV. Hence the input-referred noise from the biquadratic filter that can be tolerated is -74dBFS or $40\mu V_{rms}$ noise. The noise is budgeted so that half the noise comes from R_1 and the remaining noise arises from other terms in equation (3.8). Since the scaling factor of the first amplifiers noise is approximately 1/40, the noise from the amplifier would be sufficiently negligible if the amplifier's noise is of the same order as the resistor R_1. So we aim for a noise of $20\mu V_{rms}$ from the first amplifier. The second amplifier's noise requirement is slightly relaxed since the gain due to the first integrator in the biquadratic filter scales the noise, when we refer it to the input of the filter.

It should also be noted that the noise fixes the upper-limit on the value of resistors that can be used in the filter. Using smaller resistors would decrease the noise of the filter, but the load they impose on the amplifiers will necessitate burning a lot of current in-order to achieve high gain.

3.4 Distortion analysis of the filter

The filter is implemented in a fully differential fashion; hence the most significant source of distortion is the third harmonic component. We can use IM3 as the metric to measure distortion as it directly reflects the level of the 3rd harmonic component present at the input of the filter. In this design, an IM3 of -74dB is targeted.

Similar to noise, the distortion of the second amplifier is scaled when referred back to the input. Hence we need to focus mainly on the linearity of the first amplifier. In order to arrive at the linearity requirements, the linearity of a generic inverting amplifier shown in Figure 11 is first considered.

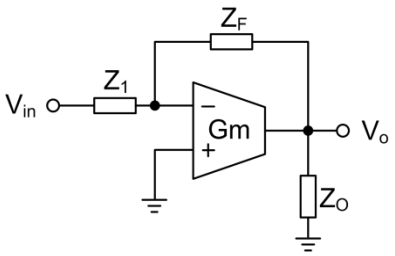

Figure 11 Inverting amplifier

The op-amp in an inverting amplifier has been represented using the transconductance stage Gm and output impedance Z_O. In-order to identify the loading effect of the feedback element, the circuit can be redrawn as shown in Figure 12.

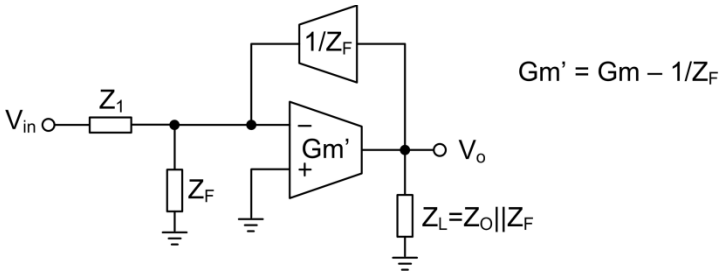

Figure 12 Inverting amplifier illustrating feedback loading

In-order to identify the loop gain, the loop is broken in the feedback path as shown in Figure 13.

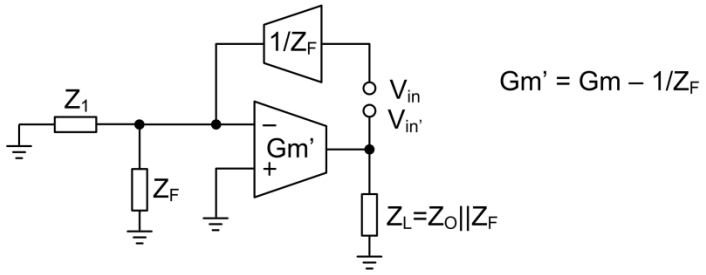

Figure 13 Inverting amplifier - Loop gain

$$\text{Loop Gain} = \frac{V_{in}'}{V_{in}} = -\frac{1}{Z_F}\frac{Z_1 Z_F}{Z_1 + Z_F} Gm' Z_L \tag{3.9}$$

We can identify the forward path gain from Figure 12 and the loop gain from Figure 13. Hence by applying Mason's gain formula, the transfer function from V_{in} to V_o can be written as,

$$\frac{V_{in}}{V_o} = -\frac{\left(\frac{Z_F}{Z_1 + Z_F}\right) Gm' Z_L}{1 + \left(\frac{Z_F}{Z_1 + Z_F} Gm' Z_L\right)\left(\frac{Z_1}{Z_F}\right)} \tag{3.10}$$

The feedback system in equation (3.10) can be modeled as shown in Figure 14.

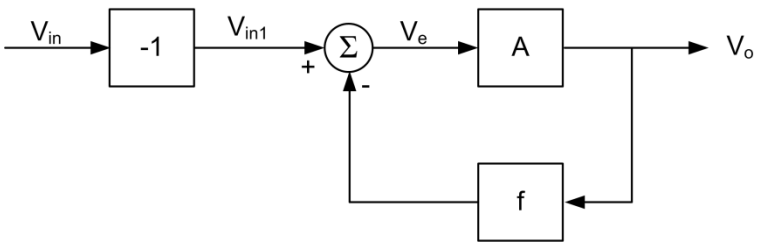

Figure 14 Feedback model for the inverting amplifier

$$A = \left(\frac{Z_F}{Z_1 + Z_F}\right) Gm' Z_L \tag{3.11}$$

$$f = \frac{Z_1}{Z_F} \tag{3.12}$$

$$\frac{V_o}{V_{in1}} = \frac{A}{1 + Af} \tag{3.13}$$

The forward gain block A is non-linear due to the presence of Gm' in its expression. The non-linear gain of A can be expanded as shown in equation (3.14).

$$\begin{aligned} A &= a_1 V_e + a_2 {V_e}^2 + a_3 {V_e}^3 + \cdots \\ &= \frac{Z_F Z_L}{Z_1 + Z_F}\left(g_1 V_e + g_2 {V_e}^2 + g_3 {V_e}^3 + \cdots\right) \end{aligned} \tag{3.14}$$

The coefficients, g_i, represent the non-linear expansion coefficients of Gm' and coefficients, a_i, represent the non-linear expansion co-efficients of the open-loop gain element A. Let b_i represent the non-linear co-efficients of the closed loop transfer function V_o/V_{in1}. From [10] we have the expressions for b_i in terms of a_i and loop gain as shown in equations (3.15), (3.16) and (3.17).

$$b_1 = \frac{a_1}{1 + Af} \tag{3.15}$$

$$b_2 = \frac{a_2}{(1 + Af)^3} \tag{3.16}$$

$$b_3 = \frac{a_3(1 + Af) - 2{a_2}^2 f}{(1 + Af)^5} \tag{3.17}$$

In equation (3.17), if $2a_2^2 f << a_3(1+Af)$, then we can rewrite the equation as shown in equation (3.18).

$$b_3 = \frac{a_3}{(1+Af)^4} \tag{3.18}$$

Since our system is a fully differential system, the even-order non-linearities cancel each other and the third order non-linearity becomes the most important non-linearity. Intermodulation distortion gives a good measure of the linear performance of the circuit. Intermodulation distortion is defined as the ratio of the amplitude of the intermodulation product in a two-tone test to the amplitude of the fundamental. The expression for the 3rd order intermodulation distortion for the closed loop system is shown in equation (3.19) [11].

$$IM3 = \frac{3}{4}\frac{b_3}{b_1}V_{in}^{\ 2} \tag{3.19}$$

Substituting the expression for b_3 and b_1 from equations (3.18) and (3.15) respectively, into equation (3.19), we can rewrite the expression for IM3 as shown in equation (3.20).

$$IM3 = \frac{\frac{3}{4}\frac{a_3}{a_1}V_{in}^{\ 2}}{(1+Af)^3} \tag{3.20}$$

The numerator in equation (3.20) represents the IM3 of the gain element A if it was used in open loop with the input V_{in} directly applied to it. Hence we can generalize the relation between IM3 of a gain element used with linear feedback and in open loop as shown in equation (3.21).

$$\text{Closed loop IM3} = \frac{\text{Open loop IM3}}{(1 + \text{Loop gain})^3} \tag{3.21}$$

In the case of the filter, that is being implemented in this thesis, two factors influence the IM3 of the closed loop filter – the open loop IM3 of the op-amps and the loop gain of the filter. In-order to attain an IM3 of -74dB, the requirement from the open-loop IM3 of the amplifier is relaxed if the loop gain is high. If the loop gain is 20dB, the open loop IM3 will be diminished by approximately 60dB. Hence in our design we aim for the amplifiers to have a gain such that the loop gain is at least 20dB. In-order to find the gain requirement of the first amplifier, we break the loop as shown in Figure 15.

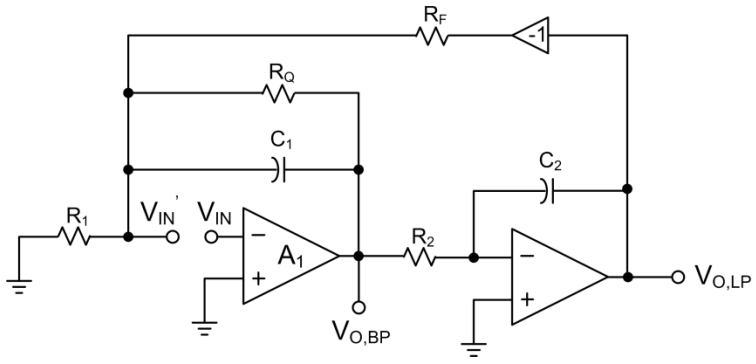

Figure 15 Biquadratic filter with loop broken at first amplifier input

The resistor R_2 is connected to the output of the first amplifier on one end and to a virtual ground node on the other end. Hence it can be considered as a load on the first amplifier. Figure 15 can be redrawn in a much simpler fashion as shown in Figure 16.

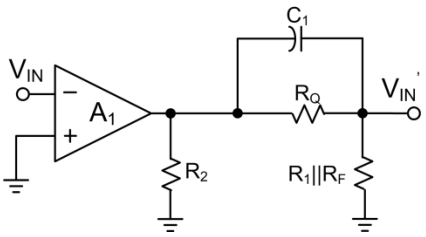

Figure 16 Simplified circuit to find loop gain

Let A_1 be the gain of the first amplifier with its load. In Figure 16, R_2 forms the load, however in an actual CTSD ADC, there may be additional resistor which feeds the signal at that node to the summing amplifier which will load the first amplifier (will be illustrated later). The expression for the loop gain can now be easily written down as shown in equation (3.22).

$$\text{Loop gain} = \frac{V_{IN}'}{V_{IN}} = A_1 \frac{R_1 || R_F}{R_1 + (R_Q || \frac{1}{sC_1})} \tag{3.22}$$

Equation (3.22) is used to find the gain requirement of the amplifier A_1, which guarantees a loop gain of 10. We see in [3] that the first amplifier needs to have at least 50dB gain at low frequencies and 44dB voltage gain at 25MHz, to guarantee good in-band linearity.

4. AMPLIFIER DESIGN

In Section 3, an insight was given into the amplifier specifications that are required for the amplifiers used in the biquadratic filter. In this section, a summary of the specifications are listed and the design of the amplifier is discussed in detail. The merits and demerits of operational amplifiers with class-A and class-AB (with conventional Monticelli bias) output stages are discussed. A new class-AB bias scheme is proposed and is compared with the other two output stages.

4.1 Amplifier specifications

Table 2 summarizes the design specifications required from the first amplifier of the biquadratic filter.

Table 2 Amplifier specifications

Parameter	**Value**
DC Gain	$\geq$ 52.26 dB
Gain up to 25MHz	$\geq$ 44 dB
Gain-bandwidth product	3.96 GHz
Output linear range (fully-differential)	$\geq$ 400mV
Power	minimal
Input referred noise in 25MHz	$\leq 20\mu V_{rms}$
Load	1.34 KΩ

In Section 3, it was discussed that the design specifications on amplifier 1 are more challenging than the second amplifier; hence this amplifier is chosen to illustrate design topology. From the specifications it can be seen that the amplifier needs to have a

very large gain-bandwidth product running to few GHz. Also, the op-amp is loaded by a small resistor and needs to achieve a high gain; hence reducing the power consumption of this amplifier is a significant challenge.

4.2 Amplifier topology

A key observation that needs to be made based on the application is that the amplifier never going to be operated up to its unity gain frequency which is of the order of few GHz, as the sampling frequency is only 400MHz for the CTSD ADC. Hence this property can be exploited to reduce power consumption. The high gain and high bandwidth requirement can be achieved by using a multi-stage amplifier using several compensation techniques like nested Gm-C compensation [12], nested Miller compensation [13], etc. But as we increase the number of stages, the power consumption increases. Hence using a two-stage amplifier with a suitable compensation technique would the ideal solution in this case. Also, most of the compensation techniques are based on Miller compensation, which achieves stability at the expense of bandwidth as it pushes the dominant pole to lower frequencies. Using Miller compensation would consume large power in this case as the amplifier requires a high gain and high bandwidth.

In this design, we make use of feed-forward compensation [14]. This technique provides a fast path for the signals. The technique is explained briefly using Figure 17.

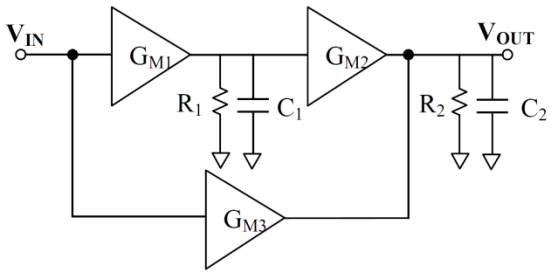

Figure 17 Feed-forward Gm compensation technique

The amplifier in Figure 17 has two-gain stages with transconductance G_{M1} and G_{M2} respectively. G_{M3} is a feed-forward stage. R_i and C_i represent the resistance and capacitance present at the output of the i^{th} stage. G_{M3} provides a fast path and creates a phantom zero to compensate for the negative phase shift introduced by the stages G_{M1} and G_{M2}. Since this technique does not the push the dominant pole at the first stage output to lower frequencies (which is the case in Miller compensation technique), this scheme can be used to realize amplifiers that need a large bandwidth.

$$\frac{V_{OUT}}{V_{IN}}(s) = \left(\frac{G_{M1}R_1}{1 + s/\omega_{P1}}\right)\left(\frac{G_{M2}R_2}{1 + s/\omega_{P2}}\right) + \left(\frac{G_{M3}R_2}{1 + s/\omega_{P2}}\right) \tag{4.1}$$

If $G_{M2} = G_{M3}$, we can simplify equation (4.1) as:

$$\frac{V_{OUT}}{V_{IN}}(s) = G_{M1}R_1G_{M2}R_2\left(1 + \frac{G_{M3}}{G_{M1}R_1G_{M2}}\right) * \left(\frac{1 + \frac{s}{\left(1 + G_{M1}R_1\left(\frac{G_{M2}}{G_{M3}}\right)\right)\omega_{P1}}}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}\right) \tag{4.2}$$

From equation (4.2) we can see that, having an additional path to the output through the feed-forward stage creates a LHP zero. The position of the zero can be moved by varying G_{M3} relative to G_{M2}. If G_{M3} is increased with respect to G_{M2}, then the zero introduced moves to lower frequencies and improves the phase margin, and vice versa. One of the key features of this technique is that it allows one or more non-dominant pole to exist within the unity gain frequency of the amplifier, as long as the zero is close enough to the pole to cancel its effect.

In this design, the first stage of the amplifier needs to provide low input noise and high bandwidth (since the dominant pole is at the output of the first stage). The gain

requirement from the first stage is fairly high, since the output stage of the amplifier is loaded by a small resistance. In-order to meet these requirements, we use a conventional differential pair input stage with current source load. The feed-forward stage, needs to be a low-noise stage, since its noise directly adds to the amplifier's input referred noise. Additionally, the feed forward stage should have a large bandwidth. Hence the feed-forward stage is also a differential pair with current source load. The output stage of the amplifier needs to be highly linear in the presence of a small resistive load. The output stage can have high output impedance, since the small resistive load will take care of pushing the pole to high frequencies and the feed-forward compensation doesn't require the pole to be outside the unity gain frequency of the amplifier. In the next few subsections, we will explore the different output stages that can be used.

4.3 Class-A output stage

Since the op-amps need to be very linear, class-A output stage is a popular solution [9, 15, 16]. In class-A operation, the amplifier is always ON for the entire excursion of the signal. This is achieved by biasing using a fixed current source. Figure 18 shows a simple class-A output stage and its small signal i_{OUT} versus v_{in} characteristics.

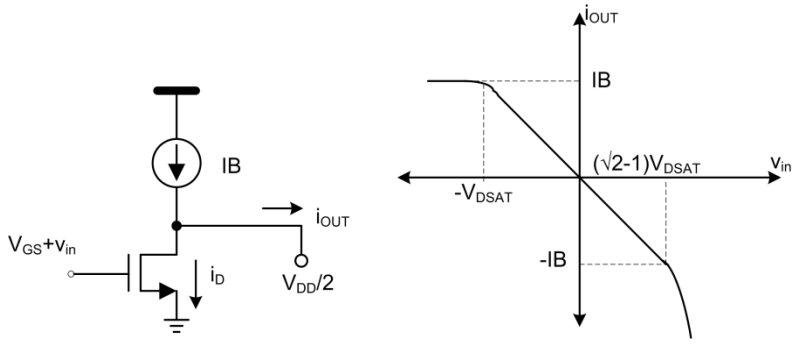

Figure 18 Class-A output stage and its I-V characteristics

The output stage is a transconductance stage which delivers the current i_{OUT} into an output load. The expression for output current can be written as shown in equation (4.3).

$$i_{OUT} = IB - i_D \tag{4.3}$$

When $v_{in} > -V_{DSAT}$ and the drain-source voltage $V_{DS} \geq V_{GS} - V_T$, the transistor is in saturation and equation (4.3) can be rewritten as shown below.

$$i_{OUT} = IB - K(V_{DSAT} + v_{in})^2$$

$$V_{DSAT} = V_{GS} - V_T; K = \frac{Kn'(W/L)}{2}; IB = K V_{DSAT}^2$$

$$i_{OUT} = -K V_{DSAT} v_{in} - K v_{in}^2; \text{for } v_{in} > -V_{DSAT} \tag{4.4}$$

From equation (4.4) and the I-V characteristics, we can see that for small values of v_{in}, the output current varies linearly with v_{in}. As v_{in} increases in the positive direction, the quadratic term starts dominating. As v_{in} is reduced below $-V_{DSAT}$ the transistor enters the cut-off region, and the output current saturates to IB. This corresponds to the hard non-linearity shown in the I-V characteristics. The peak current that the transistor can sink when v_{in} is increased depends on the load connected at the output. In presence of a capacitive load, C_L, at the output, the slew rate corresponding to the scenario when i_{OUT} increases can be written as shown in equation (4.5).

$$SR^+ = \frac{IB}{C_L} \tag{4.5}$$

Since the peak output current is limited to the bias current, for applications that require a high peak value of output current, the class-A output stage consumes a lot of power. The good thing about class-A amplifiers, apart from providing good linearity for small signals is that they are highly robust across process corners, since the current source, IB, is generally implemented as a current mirror that mirrors a reference current.

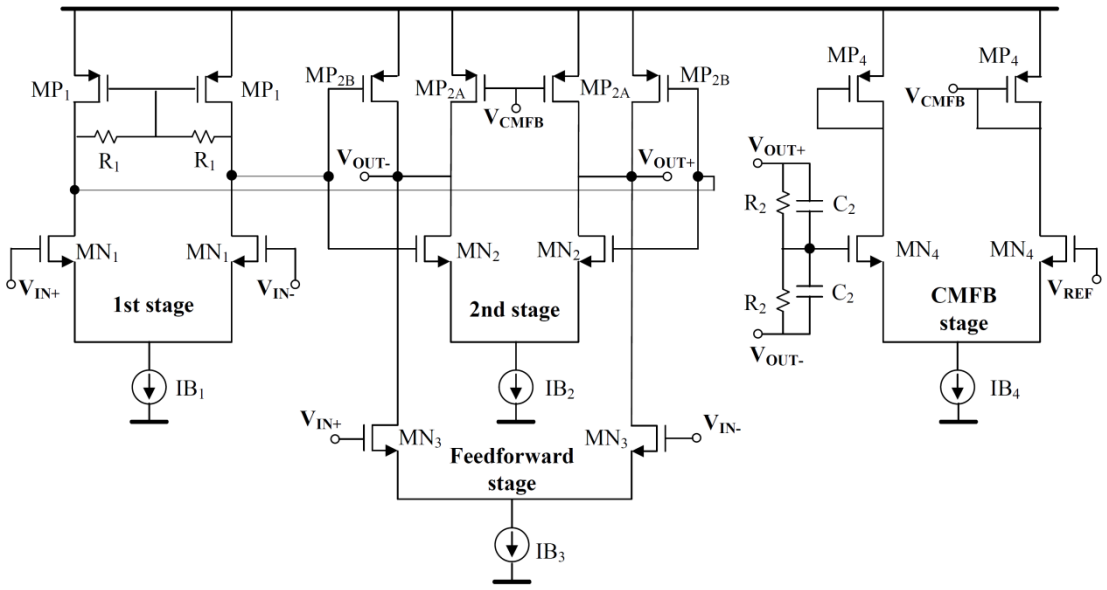

Figure 19 Amplifier with class-A output stage and feed-forward compensation

Figure 19 shows the amplifier implemented in [3]. The amplifier has a feed-forward Gm compensation scheme similar to the one detailed in Subsection 4.2 and a class-A output stage. In-order to reduce power-consumption, the PMOS devices MP_{2B} reuse the current in the feed-forward stage to provide additional gain in the second stage, and hence the current flowing through the transistors MN_2 can be reduced. Also, this scheme of complementary transistors at the output stage eliminates the problem of swing-limitation as there are two active devices at the output node whose drain current is controlled by the input signal. However, there is a possibility of cross-over distortion in the case of large swing signals at the output. The other possible problem is that the same DC level that biases the output transistors MN_2 and MP_{2B} is set by the CMFB of the

output stage, which employs resistive shunt feedback. If the signal swing at the output of first stage is larger than the over-drive voltage of the output transistors, the devices will be pushed out of saturation. Hence careful design is required to guarantee that the devices stay in saturation across all process corners.

A key observation that can be made from the implementation in [3] is that the amplifier is able to meet the stringent linearity requirements of the filter despite having a complementary PMOS and NMOS output stage, as long as both the transistors remain in saturation for the entire excursion of the output signal. This observation motivates us to analyze the possibility of using a class-AB output stage, which is discussed in the next section.

4.4 Class-AB output stage

Class-AB amplifiers can theoretically drive infinite current into the load. This motivates designers to choose a class-AB output stage when a large capacitive load or a small resistive load needs to be driven. The schematic of the ideal class-AB output stage and the output current versus input voltage characteristic is shown in Figure 20.

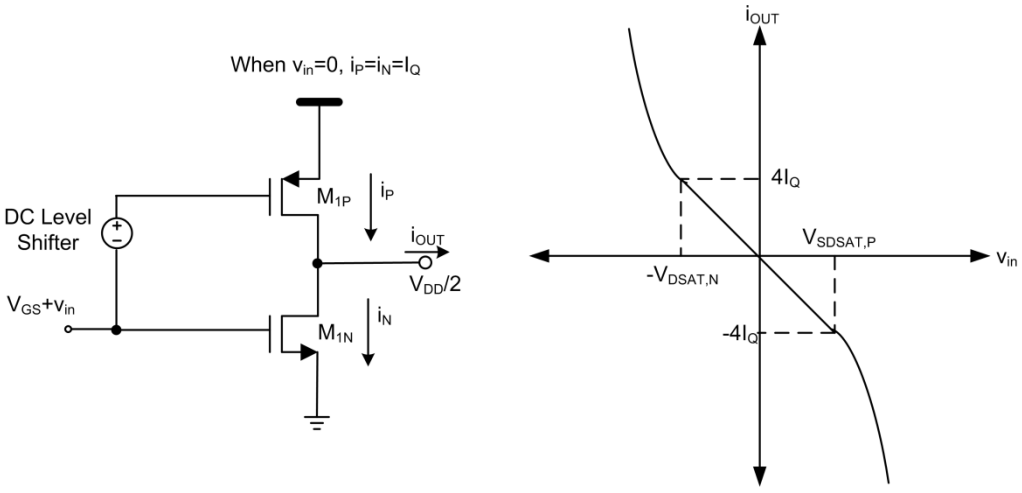

Figure 20 Ideal class-AB output stage schematic and i_{OUT} vs v_{in} characteristic

The ideal class-AB output stage shown in Figure 20 has complementary NMOS and PMOS output devices which can either "push" current into the load or "pull" current from the load. Hence they are also called push-pull output stages. The relationship of output current, i_{OUT}, with input voltage, v_{in}, is shown in equations (4.6), (4.7) and (4.8).

$$i_{OUT} = i_P - i_N$$

$$i_{OUT} = K_P\left(V_{SDSAT,P} - v_{in}\right)^2 - K_N\left(V_{DSAT,N} + v_{in}\right)^2;\ \text{for} - V_{DSAT,N} < v_{in} < V_{SDSAT,P}$$

$$\text{where } V_{SDSAT,P} = V_{SG,M1P} - \left|V_{Tp}\right|;\ K_P = \frac{Kp'(W/L)_{M1P}}{2}$$

$$V_{DSAT,N} = V_{GS,M1N} - V_{Tn};\ K_N = \frac{Kn'(W/L)_{M1N}}{2}$$

If $V_{DSAT} = V_{DSAT,N} = V_{SDSAT,P}$ and $K = Kn'(W/L)_N = Kp'(W/L)_P$, then we can rewrite the above equation for i_{OUT} as:

$$i_{OUT} = -4KV_{DSAT}v_{in};\ \text{for} - V_{DSAT,N} < v_{in} < V_{SDSAT,P} \tag{4.6}$$

$$i_{OUT} = K_P\left(V_{SDSAT,P} - v_{in}\right)^2;\ \text{for } v_{in} \le -V_{DSAT,N} \tag{4.7}$$

$$i_{OUT} = -K_N\left(V_{DSAT,N} + v_{in}\right)^2;\ \text{for } v_{in} \ge V_{SDSAT,P} \tag{4.8}$$

When $-V_{DSAT,N} < v_{in} < V_{SDSAT,P}$, both the transistors M_{1P} and M_{1N} are in saturation. The expression of output current has only a linear term as the quadratic terms of i_P and i_N cancel out as seen in equation (4.6). Hence the output current is very linear in this region. When $v_{in} \le -V_{DSAT,N}$, M_{1N} enters the cut-off region and the current is provided by M_{1P}, which varies with v_{in} in a quadratic fashion as shown in equation (4.7).

Similarly, when $v_{in} \geq V_{SDSAT,P}$, M_{1P} enters cut-off region and M_{1N} conducts the output current as shown in equation (4.8). If the input signal amplitude is less than over-drive voltage of the output transistors, then the output current is extremely linear, else cross-over distortion is observed.

The peak output current delivered in the case of a class-AB output stage depends on the input voltage. There is no hard limit on the peak output current as seen in the class-A output stage. Since the bias current in the output stage when v_{in}=0 is not related to the peak output current delivered, it can be much lower than the peak output current. Hence class-AB output stage consumes lesser power than a class-A output stage designed to deliver the same output current. In presence of a capacitive load, C_L, the slew rate of the class-AB output stage is shown in equation (4.9).

$$SR^{+} = \frac{K_P\left(V_{SDSAT,P} - v_{in}\right)^2}{C_L};\ SR^{-} = -\frac{K_N\left(V_{DSAT,N} + v_{in}\right)^2}{C_L} \tag{4.9}$$

The main design challenge in the implementation of a class-AB output stage is the implementation of the DC level shifter. The DC level shifter, which is implemented using a bias circuit, needs to guarantee the following functions:

1. Bias the output stage transistors M_{1P} and M_{1N} with a fixed-quiescent current across different process corners.
2. Act as a short-circuit to small-signal variations, so that there is no attenuation of small signal information across the level shifter.
3. It should not impose a limitation on the current the output stage can pull or push into the load.

Class-AB output stages have been used for amplifiers in the loop filter in [17, 18]. The small resistors that the op-amps in the filter need to drive form the primary motivating factor to use class-AB output stages. From a small signal point of view, class-AB output stages inherently have the property of bias current re-use, and hence provide larger gain than a conventional class-A stage would using the same bias current.

In other words, for a required gain, the class-AB output stage consumes less power than its class-A counterpart. In a communication receiver, the signal strength is much smaller than full-scale power most of the time. A class-AB amplifier uses a bias current which is a fraction of the peak current that it would be delivered and thus saves power. In a class-A stage a current source that is capable of delivering the peak current biases the amplifying device, and hence increases the static power consumption of a class-A output stage. All these factors motivate the use of a class-AB output stage.

4.4.1 Existing class-AB schemes

Several class-AB schemes have been reported in the literature [19, 20, 4, 21, 22, 23, 24], which focus on the problem of implementing robust DC level shifters which efficiently perform the three functions of the bias circuit highlighted earlier. The class-AB stages reported in [19, 20] suffer from the problem of saturating output current since they are current-mirror based. The implementation in [21] is not suitable for low supply voltages. [22] proposes a DC level shifter implementation but it relies on additional circuitry to fix the output DC level of the previous stage. Monticelli bias [4] is the most popular approach used for implementing class-AB output stages in several applications and is shown in Figure 21.

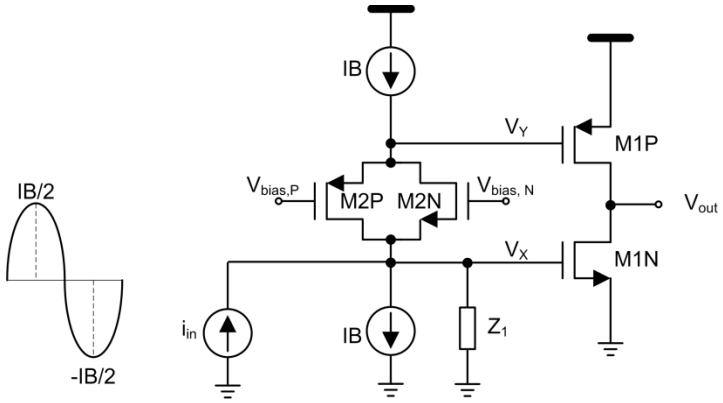

Figure 21 Class-AB output stage with Monticelli bias

Monticelli bias scheme fixes the bias current in the output stage based on quadratic trans-linearity principle [25]. In the Monticelli bias, the bias current IB flowing through the head-to-tail connected transistors M2P and M2N act as a DC level shifter. In the quiescent condition, the current through transistors M2P and M2N is equal to IB/2. When the previous transconductance stage in the op-amp generates a small signal current, i_{in}, it flows across the impedance Z_1 to generate a voltage, V_X, which is copied in V_Y. When i_{in} increases, the voltage V_X increases, and hence the gate-source voltage of M2N decreases and the current flowing through M2N decreases. Since the small signal current circulates between M2N and M2P, the current through M2P increases, and the gate-source voltage of M2P has to increase to support this larger current. Since the gate voltage is fixed, the source voltage, V_Y, moves in the direction towards the supply voltage. When V_X decreases, the current through M2N increases and the current through M2P decrease and hence V_Y is pulled down. Thus small signal variations at the output of the first stage are copied on to the gate of M1P. Since the DC bias current of M2N and M2P is equal to IB/2, this copying action of V_X to V_Y is valid only when the ac current injected in the loop is less than IB/2. The small-signal equivalent of the Monticelli bias network is shown in Figure 22.

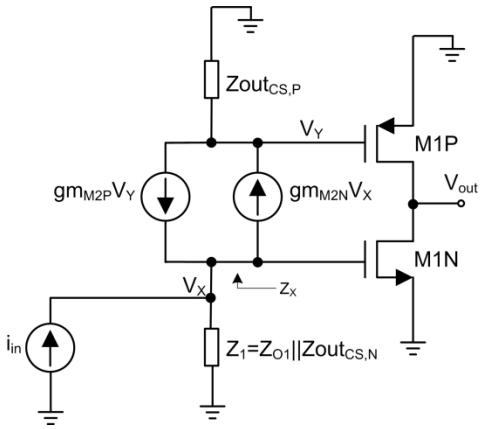

Figure 22 Small signal equivalent of Monticelli bias network

The input impedance from looking into the node X is given in equation (4.10). It can be seen that the input impedance depends largely on $Zout_{CS,P}$. The expressions for voltages V_X and V_Y are shown in equations (4.11) and (4.12). The transfer function of the Monticelli bias network V_Y/V_X is shown in equation (4.13).

$$Z_X = \frac{1 + gm_{M2P} Zout_{CS,P}}{gm_{M2N}} \tag{4.10}$$

$$V_X = i_{in}(Z_1 || Z_X) = i_{in} \frac{Z_1\left(1 + gm_{M2P} Zout_{CS,P}\right)}{1 + gm_{M2P} Zout_{CS,P} + gm_{M2N} Z_1} \tag{4.11}$$

$$V_Y = V_X \left(\frac{Zout_{CS,P}}{Z_X}\right) = i_{in} \frac{Z_1\left(gm_{M2N} Zout_{CS,P}\right)}{1 + gm_{M2P} Zout_{CS,P} + gm_{M2N} Z_1} \tag{4.12}$$

$$\frac{V_Y}{V_X} = \frac{gm_{M2N} Zout_{CS,P}}{1 + gm_{M2P} Zout_{CS,P}} \tag{4.13}$$

In order for the transfer function in equation (4.13) to be close to unity, gm_{M2N} and gm_{M2P} should be equal to each other and $gm_{M2P}Zout_{CS,P}$ should be much greater than unity. We know that the transconductance gm_{M2P} are proportional to square root of the bias current IB and $Zout_{CS,P}$ is inversely proportional to IB, and hence the product $gm_{M2P}Zout_{CS,P}$ varies inversely with the square root of IB. In-order to maximize $gm_{M2P}Zout_{CS,P}$, we need to decrease IB. However, the lower limit on IB is fixed by the peak value of the ac current injected from the previous stage. Also, it is not always possible to match gm_{M2N} and gm_{M2P} in a real implementation; hence the transfer function V_Y/V_X never achieves unity. If V_X and V_Y are not identical, the quadratic terms in the drain current expression of the output transistors M1N and M1P do not cancel each other as they did in equation (4.6). This causes the output current to be non-linear.

Another drawback of the Monticelli bias stage can be observed during large signal operation. When the input current i_{in} is large enough so that the voltage V_X

is large enough to turn the transistor M2N off, it no-longer conducts any current and current circulation between M2N and M2P stops. M_{2P} now acts as a mere cascoding device to the PMOS current source IB, and voltage the node Y gets clamped as shown in Figure 23. The expressions for the voltages V_X and V_Y and the transfer function V_Y/V_X is shown in equations (4.14) through (4.16). As i_{in} increases further, the voltage V_X increase more rapidly and eventually the device M2P enters the linear region and acts as a resistor.

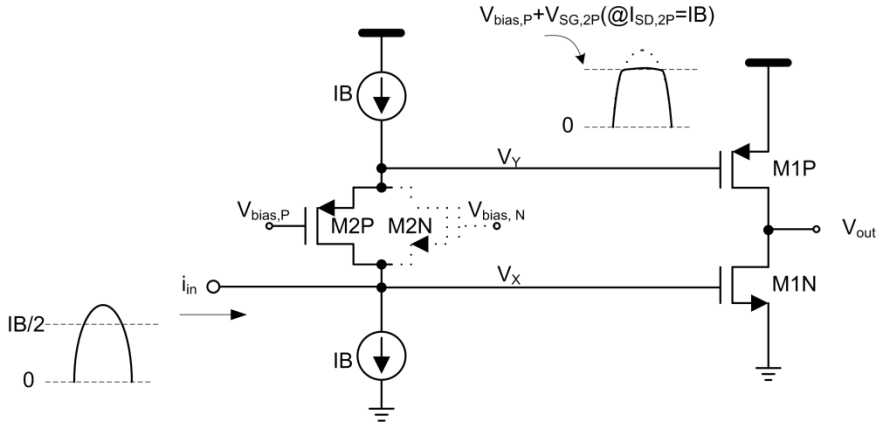

Figure 23 Large signal distortion in Monticelli bias scheme for $i_{in} > IB/2$

$$V_X = i_{in}\frac{Z_1\left(gm_{M2P}r_{o,M2P}Zout_{CS,P}\right)}{gm_{M2P}r_{o,M2P}Zout_{CS,P} + Z_1} \tag{4.14}$$

$$V_Y = i_{in}\frac{Z_1 Zout_{CS,P}}{gm_{M2P}r_{o,M2P}Zout_{CS,P} + Z_1} \tag{4.15}$$

$$\frac{V_Y}{V_X} = \frac{1}{gm_{M2P}r_{o,M2P}} \tag{4.16}$$

Similarly, when i_{in} is large enough in the negative direction and V_X decreases sufficiently so that the M_{2N} draws all of the current provided by the current source on top and M_{2P} is starved for current, M_{2P} enters the cut-off region. The Monticelli network

now acts as a common gate amplifier with M_{2N} as its amplifying device as shown in Figure 24. The corresponding expressions for the voltages V_X and V_Y and the transfer function V_Y/V_X is shown in equations (4.17) through (4.19). As i_{in} increases further in the negative direction, the voltage swing at V_X and V_Y increases and eventually the transistor M_{2N} enters triode region.

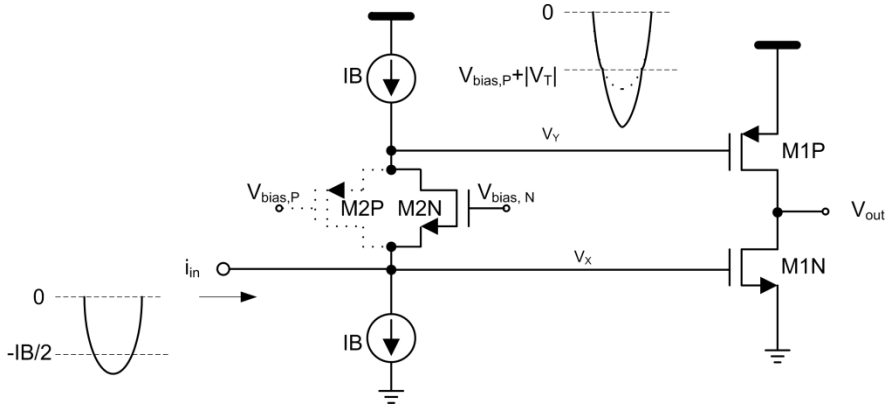

Figure 24 Large signal distortion in Monticelli bias scheme for $i_{in} < -IB/2$

$$V_X = i_{in} \frac{Z_1}{gm_{M2N} Z_1 + 1} \tag{4.17}$$

$$V_Y = i_{in} \frac{gm_{M2N} Z_1 Zout_{CS,P}}{gm_{M2N} Z_1 + 1} \tag{4.18}$$

$$\frac{V_Y}{V_X} = gm_{M2N} Zout_{CS,P} \tag{4.19}$$

From equations, (4.11) through (4.19), it can be observed that there hard discontinuities in the transfer function, V_Y/V_X. These discontinuities have been illustrated as a function of the input ac current in Figure 25.

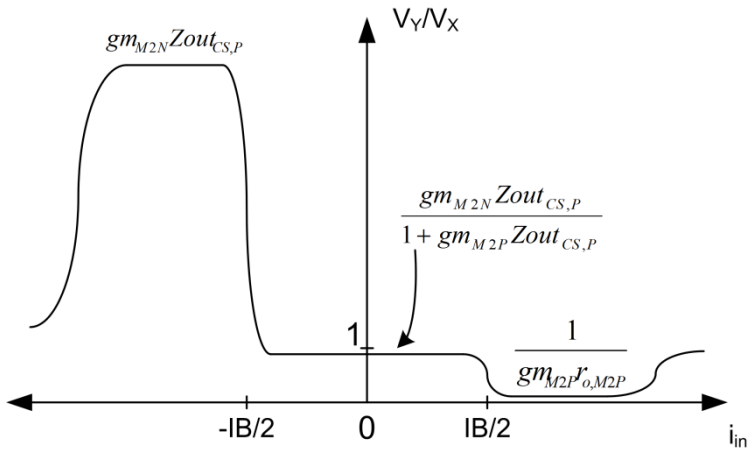

Figure 25 Voltage transfer function of the Monticelli bias network versus input ac current

4.4.2 Proposed class-AB output stage

In this new technique, the DC level shifters required in a class-AB bias stage are realized by sending a fixed current across a resistor as illustrated in Figure 26.

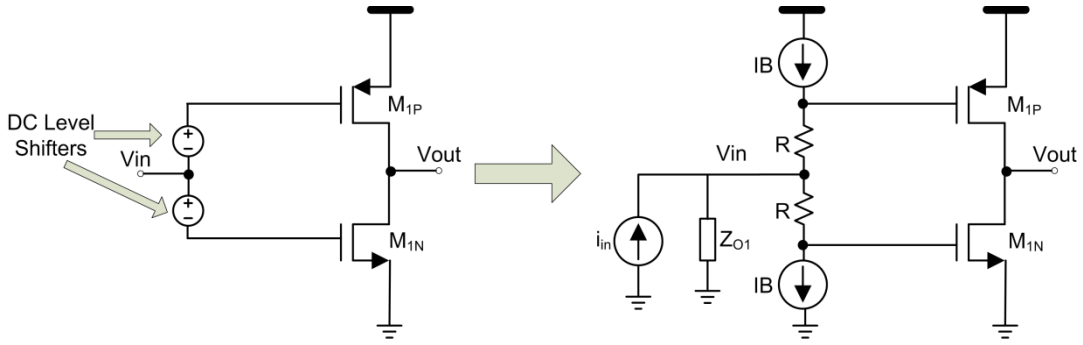

Figure 26 DC level shifter implementation - Basic idea

It is a well-known fact that the current delivered by the current source IB and the value of the resistor R varies widely across process corners. Hence we make use of feedback loops to provide the appropriate bias voltage for the gates of M_{1P} and M_{1N} as shown in Figure 27. The voltage that needs to be applied at the gate of M_{1P} (M_{1N}) is compared with a reference voltage $V_{REF,P}$ ($V_{REF,N}$). The voltage $V_{REF,P}$ ($V_{REF,N}$) is

generated by making the desired output quiescent current through M_{1P} (M_{1N}) flow into a diode connected copy of M_{1P} (M_{1N}). The feedback loop makes sure that the voltage at the node $V_{G,P}$ ($V_{G,N}$) matches $V_{REF,P}$ ($V_{REF,N}$). The accuracy of matching depends on the gain in the feed-back loop which consists of an error amplifier and the current source transistor. Since the feed-back loops are needed mainly to set the DC operating points of the transistor M_{1P} and M_{1N}, they can have a low bandwidth. Hence, the error amplifiers can be designed to have a low bandwidth and consume negligible power.

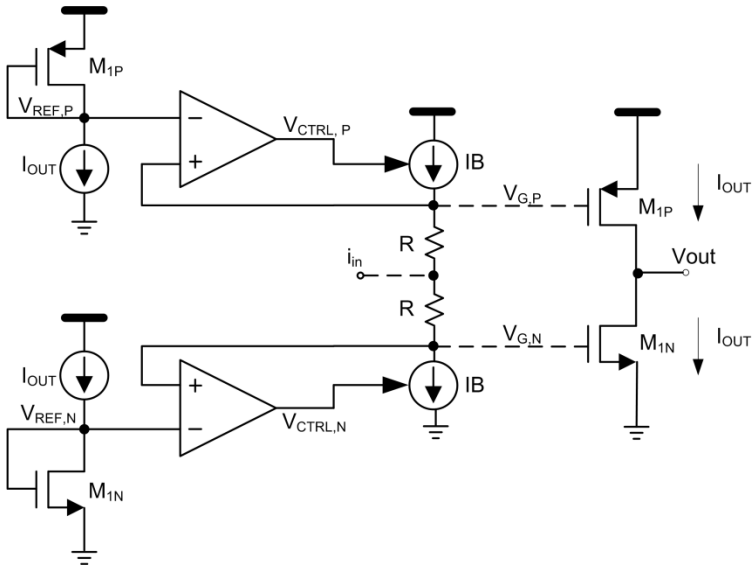

Figure 27 Proposed class-AB bias scheme - Basic idea

This circuit guarantees the DC bias conditions of the transistors M_{1P} and M_{1N} are maintained across all process corners by suppressing any variations at the nodes $V_{G,P}$ and $V_{G,N}$. However, it should be noted that the loop will also suppress any useful signal information present at the nodes $V_{G,P}$ and $V_{G,N}$. Hence the signal path should be isolated (shown in dotted lines in Figure 27) from the feedback loops that guarantee the required DC conditions. This can be done easily in a fully differential implementation, by using a common-mode sensing circuit or a circuit that averages DC level as shown in Figure 28. Since the useful signal information is fully-differential in nature, the bias control circuit is transparent to it. However, the DC bias information is common in both the positive

and negative arms and the average of it is compared with $V_{REF,P}$ and $V_{REF,N}$ to provide the appropriate current in the output transistors. Figure 29 shows the circuit-level implementation of the circuit that averages the DC levels and the error amplifier.

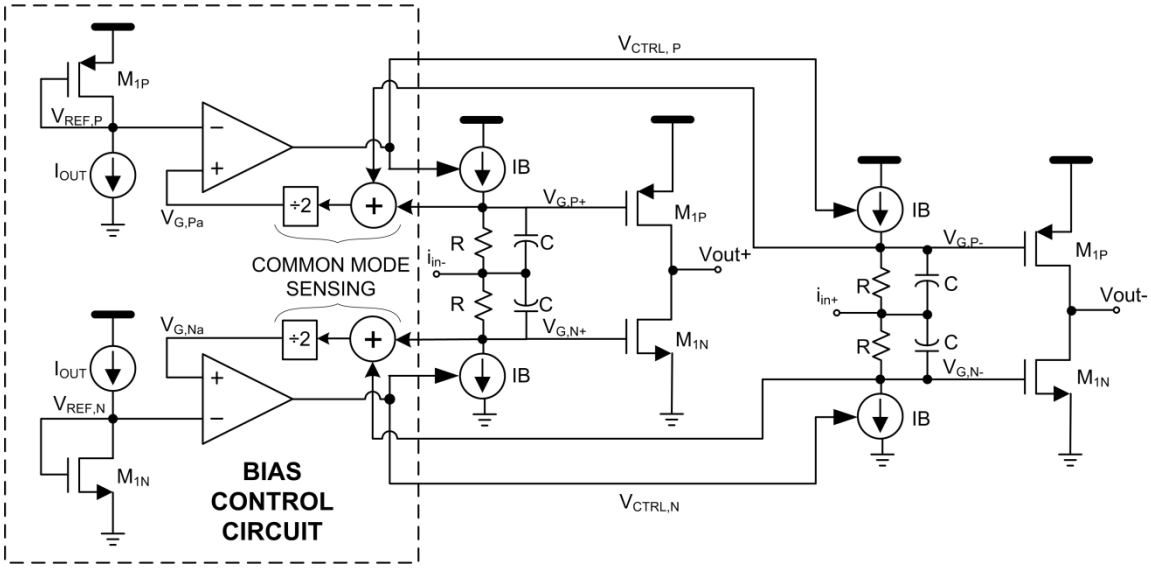

Figure 28 Fully differential implementation of proposed class-AB output stage

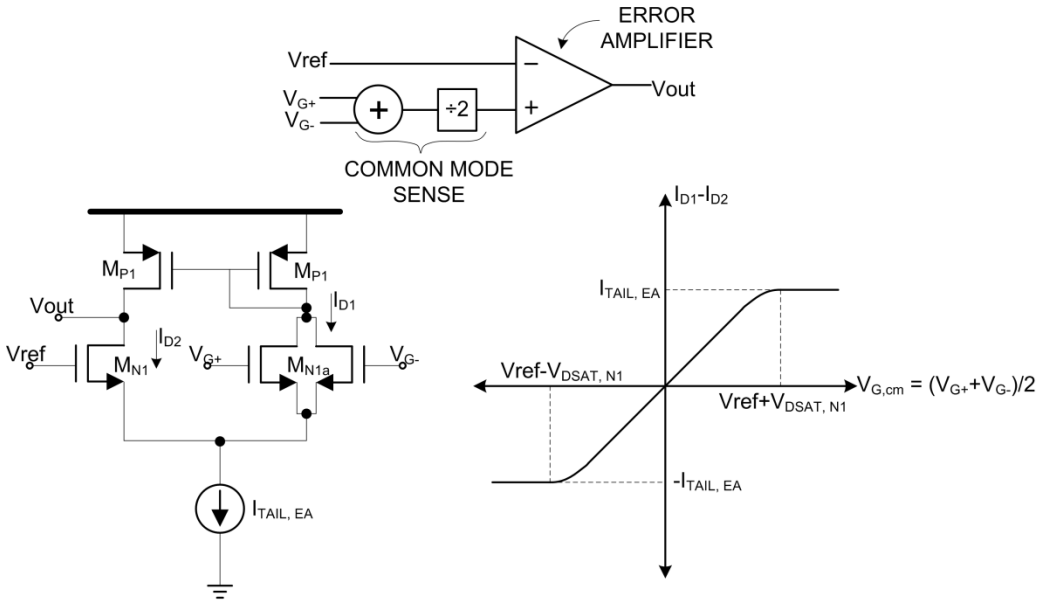

Figure 29 Circuit level implementation of common-mode sense circuit and error amplifier

It should be noted that the common-mode sense circuit imposes a limitation on the differential swing at the nodes V_{G+} and V_{G-}, as it has to be less than $|V_{DSAT,N1a}|$ for the common-mode sense circuit to be linear. This application does not demand a large signal swing at the gates of the output devices, however, if a larger linear range is needed, other common-mode sensing circuits with larger linear range can be used.

The small signal equivalent of the bias circuit present in one of the two output arms of the fully differential output stage is shown in Figure 30.

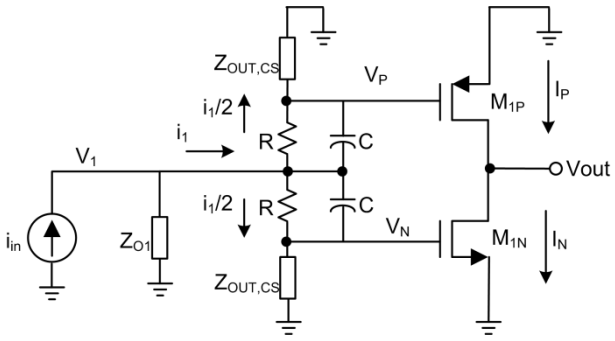

Figure 30 Small signal equivalent of bias arm

We can see that if the output impedance of the NMOS and PMOS current sources are equal then the transfer function from V_1 to V_P or V_N can be written as shown in equation (4.20).

$$\frac{V_P}{V_1} = \frac{V_N}{V_1} = \frac{Z_{OUT,CS}}{Z_{OUT,CS} + \left(R || \frac{1}{sC}\right)} \tag{4.20}$$

It can be seen from equation (4.20) that the signal at the nodes V_P and V_N are equal to each other and hence the non-linearity due to asymmetry as observed in the conventional bias scheme is absent in the proposed output stage. The capacitor, C, in parallel with the resistor, R, in Figure 30, is used to guarantee that the small signal transfer function from Vin to $V_{G,P}$ or $V_{G,N}$ is maintained close to unity at high frequencies. The resistors and capacitors are chosen so that the transfer function is as

close to unity as possible. Another use of the capacitor is that, they introduce LHP zeros in the signal path to compensate for the addition of an extra node to the circuit when compared with the Monticelli bias scheme where the first stage output connects directly to the gate of one of the output transistors.

4.5 Circuit-level implementation and comparison

The circuit-level implementation of the amplifier using the proposed class-AB output stage is shown in Figure 31. The design specifications of the amplifier that were obtained from filter design requirements were previously shown in Table 2 in Subsection 4.1. The input stage (M_{1N} and M_{1P}) is designed to have a high gain and low input noise. The dominant pole is present at the output of the first stage. The output stage (M_{2N} and M_{2P}) and the feed forward stage (M_{3N} and M_{3P}) are designed for high bandwidth and medium gain performance. The transconductance of the output stage and feed forward stage should be increased as much as possible to push the non-dominant poles to high frequencies. The output stage transistors M_{2N} and M_{2P} are designed to have high values of V_{DSAT} ($\geq$ 200mV) for better linearity. The feed forward stage and the input stage are the main contributors of input-referred thermal noise. The DC level at the gates of the output transistors M_{2N} (M_{2P}) is regulated to the reference voltage V_{REF_N} (V_{REF_P}) by the common-mode feedback loop consisting of the Error Amplifier, N – M_{6P}, M_{6Pa} and M_{6N} (Error Amplifier, P - M_{5N}, M_{5Na} and M_{5P}) and the current source transistor M_{7N} (M_{7P}). The DC level at the output of the input stage is set by resistive averaging (R_A and R_B) of the gate voltages of M_{2N} and M_{2P}. The DC level at the output of the second stage is controlled using a common-mode feedback circuit (CMFB) consisting of M_{4N} and M_{4P}. The output common mode level is detected using resistive averaging (R_{cm}) and the common-mode error is feedback to the CMFB stage to regulate voltage at the output nodes to 900mV. Table 3 lists the component values and bias conditions of the amplifier. The amplifier was optimized with respect to stability, noise, linearity and power consumption.

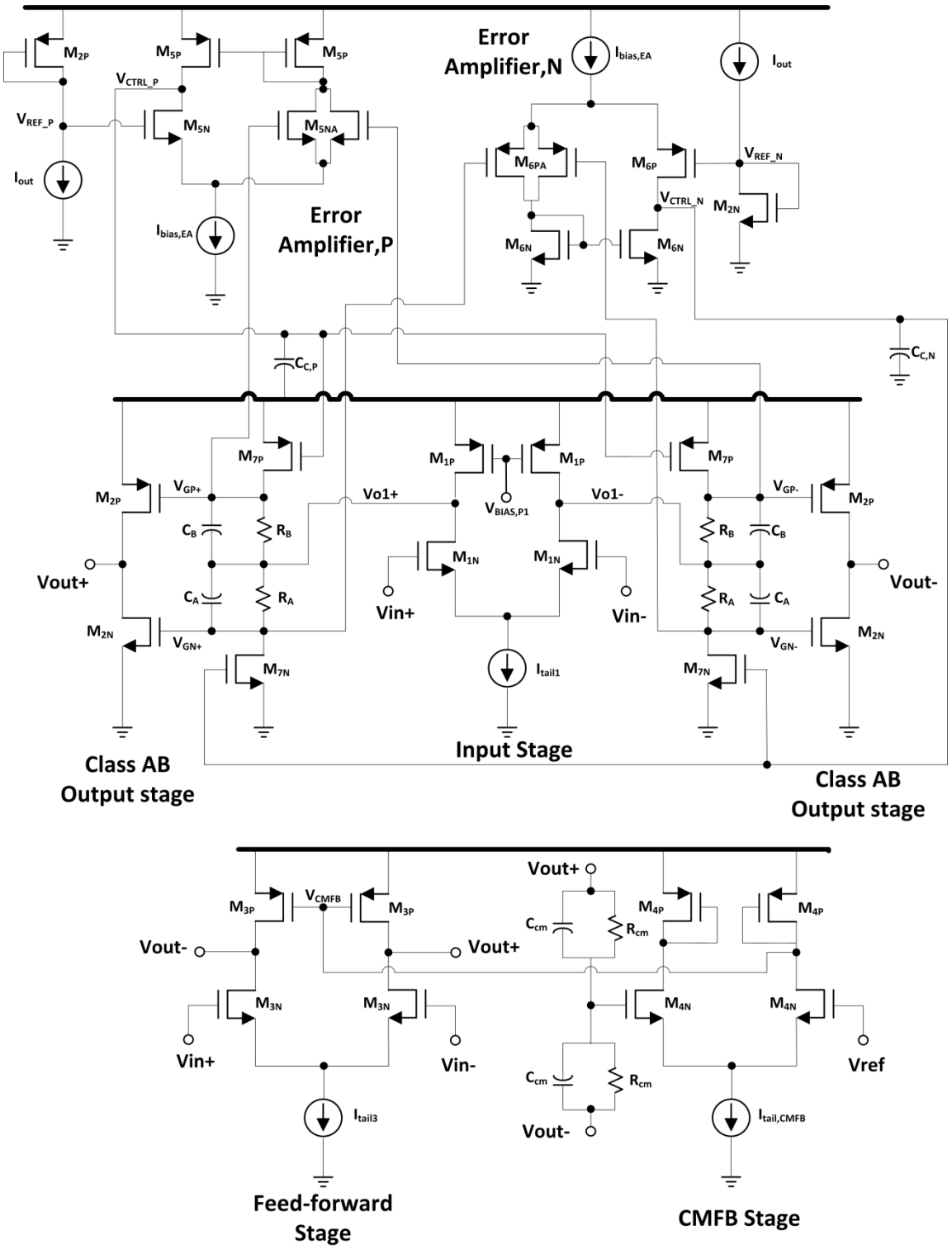

Figure 31 Circuit level implementation of amplifier using proposed class-AB output stage

Table 3 Transistor dimensions, device values and bias currents for amplifier in Figure 31

Device	Dimensions/Value	Device	Dimensions/Value
M_{1N}	(5) 30µm/0.6µm	M_{1P}	(8) 4µm/0.6µm
M_{2N}	(8) 2µm/0.3µm	M_{2P}	(8) 9µm/0.3µm
M_{3N}	(5) 12µm/0.3µm	M_{3P}	(7) 4µm/0.4µm
M_{4N}	(5) 12µm/0.3µm	M_{4P}	(2) 4µm/0.4µm
M_{5N}	(2) 2µm/0.5µm	M_{5P}	(1) 4µm/1µm
M_{5NA}	(1) 2µm/0.5µm	M_{6PA}	(1) 2µm/0.4µm
M_{6N}	(1) 3µm/1.2µm	M_{6P}	(2) 2µm/0.4µm
M_{7N}	(10) 3µm/3µm	M_{7P}	(10) 4µm/3µm
R_A	10 kΩ	R_B	10 kΩ
C_A	200fF	C_B	200fF
I_{tail1}	450µA	I_{out}	300µA
I_{tail3}	350µA	$I_{tail,CMFB}$	200µA
$I_{BIAS,EA}$	2µA	$R_{cm}\|\|C_{cm}$	80kΩ ‖ 100fF

The error amplifiers are single-ended differential amplifiers. Let's consider the error amplifier, P. One of the two input devices needs to average gate voltages V_{GP+} and V_{GP-}. This done by connecting two similar devices with common-drain and common-source but the gates connected to V_{GX+} and V_{GX-}. This drain-source coupled device pair generates a current flowing into the common-drain node which is proportional to the average of V_{GX+} and V_{GX-}. This current needs to be compared with the current generated proportional to $V_{REF,P}$ by M_{5N}; so the transconductance of M_{5N} should be equal to the sum of the transconductances two M_{5NA} devices.

The AC response of the amplifier is shown in Figure 32. The DC gain is 57 dB and gain at 25MHz is 45dB. The phase margin of the amplifier is 56 degrees.

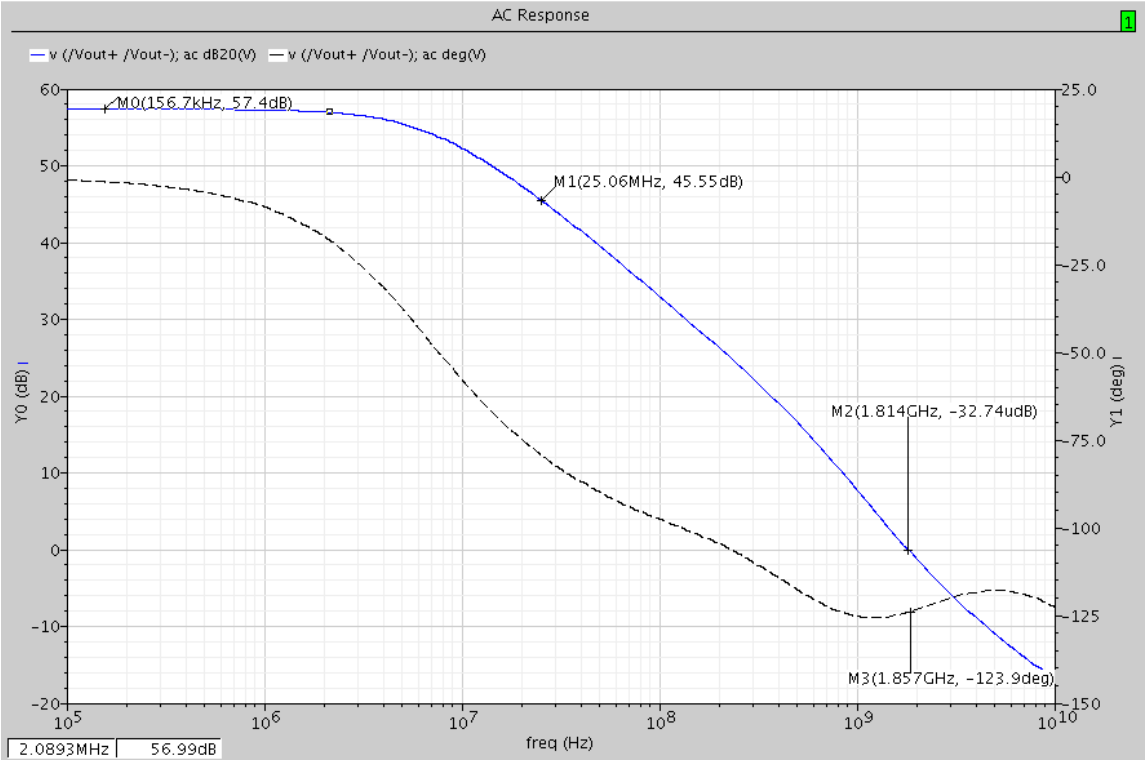

Figure 32 AC response of amplifier in Figure 31

Figure 33 shows the test setup to observe the transient step response of the common mode feedback loop, when a common-mode current in injected at the output nodes. Figure 34 shows the step response of the common mode feedback loop when a 60µA (20% of output stage current) current step is applied at the output nodes of the amplifier. The step response shows that the final value settles within an offset less than 1mV with a settling time less than 4ns.

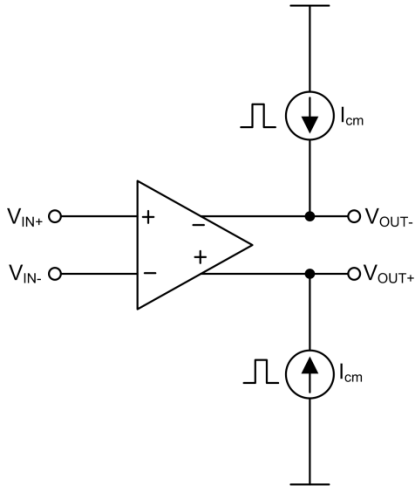

Figure 33 Test setup for common-mode transient step response

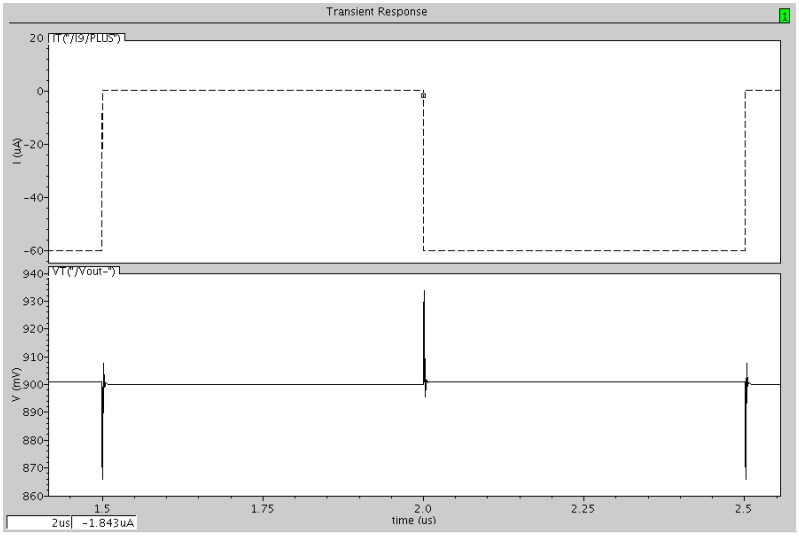

Figure 34 Step response of CMFB circuit

For the sake of comparison of topologies, an amplifier with the same topology but with the Monticelli output stage is also implemented. The circuit implementation is shown in Figure 35. The device dimensions and bias conditions are listed in Table 4.

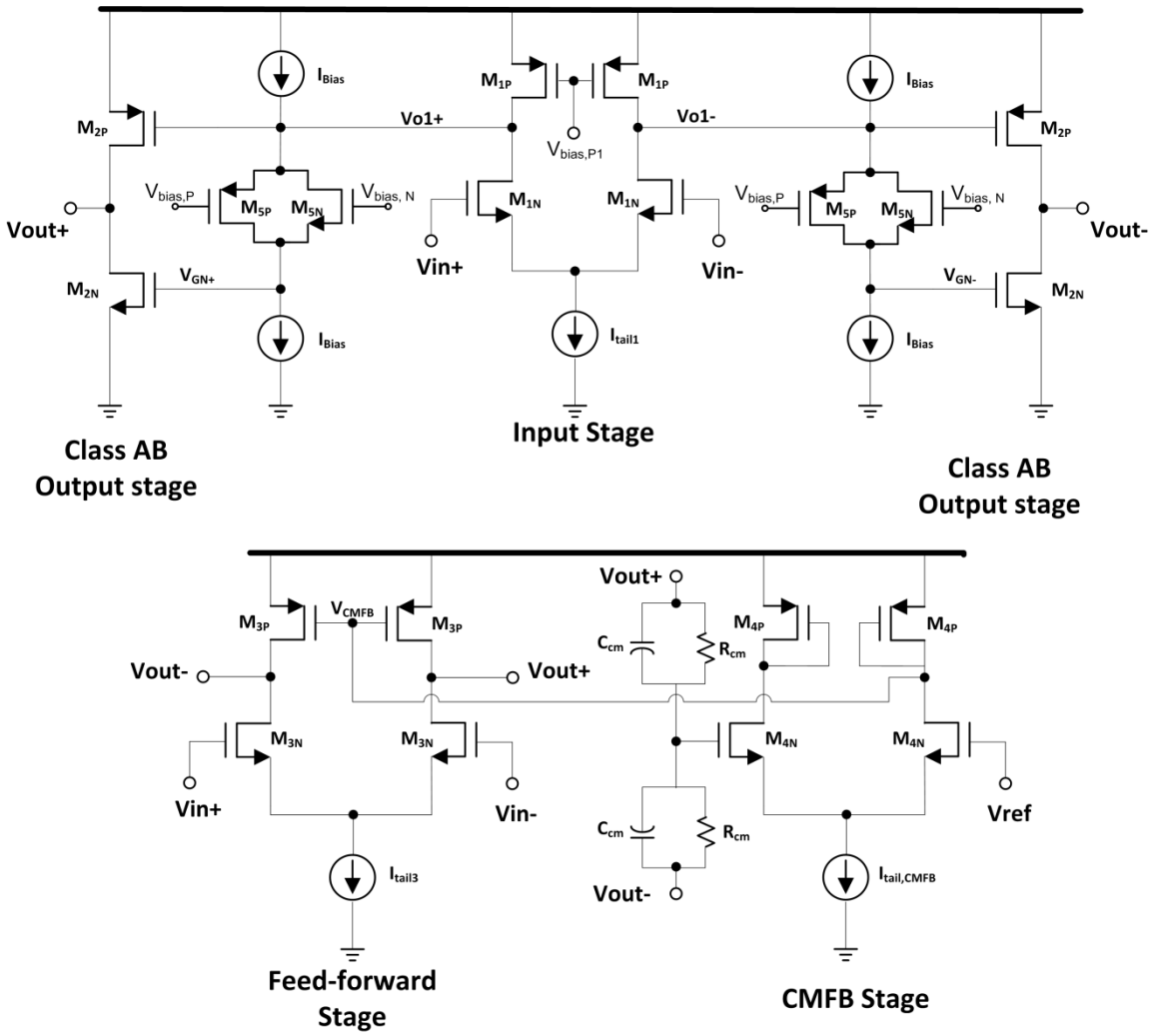

Figure 35 Circuit level implementation of amplifier using class-AB output stage with Monticelli bias scheme

Table 4 Transistor dimensions, device values and bias currents for amplifier in Figure 35

Device	**Dimensions/Value**	**Device**	**Dimensions/Value**
M_{1N}	(5) 30µm/0.6µm	M_{1P}	(7) 9µm/0.4µm
M_{2N}	(10) 11µm/0.3µm	M_{2P}	(10) 9.5µm/0.3µm
M_{3N}	(5) 12µm/0.3µm	M_{3P}	(8) 9µm/0.4µm
M_{4N}	(5) 12µm/0.3µm	M_{4P}	(4) 9/0.4µm
M_{5N}	(1) 3µm/0.3µm	M_{5P}	(1) 3µm/0.3µm
I_{tail1}	450µA	I_{Bias}	25µA
I_{tail3}	350µA	$I_{tail,CMFB}$	200µA
$R_{cm}\|\|C_{cm}$	80kΩ || 100fF		

A comparison is made between three amplifiers – the amplifier with the proposed class-AB output stage, the amplifier with a class-AB output stage using Monticelli bias and the amplifier designed in [3], which was shown in Figure 19. Table 5 compares the performance of the three amplifiers in detail. From the table it can be seen that the amplifiers have comparable performance in terms of both AC and DC characteristics. It is also observed that the amplifier using the new class-AB output stage saves power. The output stage power consumption is reduced by 25% when compared to the op-amp designed in [3], and by 34.78% when compared to the op-amp using the class-AB output stage with Monticelli bias. Although the proposed class-AB stage and the Monticelli class-AB stage have two active devices using the same bias current, the Monticelli bias network is more non-linear, additional current needs to be burnt in the output stage to achieve similar linear performance as the other two architectures. The linearity of the amplifiers is compared by embedding them in their biquadratic filter test benches. The linearity tests and the results are discussed in detail in Section 5.

Table 5 Performance comparison of amplifier implementations with different output stages

Parameter	**Op-Amp with proposed output stage**	**Op-Amp with class-AB output stage with Monticelli bias scheme**	**Op-Amp in [3]**
Gain	57.4 dB	56 dB	53.88 dB
Gain @ 25MHz	45.2 dB	44 dB	45.3 dB
Gain-bandwidth product	4.55 GHz	3.96 GHz	4.6 GHz
Phase Margin	61.6^0	62.5^0	63.7^0
Integrated Noise (in 25MHz)	16.39 µV	19.34 µV	16.09 µV
Tot. Current Consumption	1.5 mA	2.2 mA	2.5 mA
Output stage current	300 µA	460 µA	400 µA
% variation of output current across 17 process corners	3.42%	8.88%	1.69%
Input common mode range	0.77 V	0.9 V	0.77 V
Output Swing Range	1.62 V	1.65 V	1.55 V
Slew Rate	200V/us	222V/us	180V/us
Supply	1.8 V	1.8 V	1.8 V
Technology	TSMC 0.18um	TSMC 0.18um	TSMC 0.18um

Another important result is the percentage variation of output current across different process corners. Temperature was varied from -25C to 80C, and 17 different corners were simulated. The percentage variation in the bias current of the output arm for the class-AB stage using Monticelli is found to 8.88% as compared to only 3.42% in the proposed class-AB which is very close to the 1.69% variation found in the class-A output stage.

5. BIQUADRATIC FILTER SIMULATION AND RESULTS

This section presents the simulation details and schematic level simulation results of the biquadratic filter that has been designed to test the performance of the amplifiers. Three biquadratic filters that have the same transfer function and same values for the passives are implemented. The only difference between the three filters is the amplifiers that have been used in them. The three amplifier topologies discussed in the previous section have been used in different filters.

5.1 Biquadratic filter implementation

The single-ended version of the biquadratic filter designed in [3] was shown earlier in Figure 9 in Subsection 3.2. Figure 36 shows the fully differential implementation of the biquadratic filter used as a test bench.

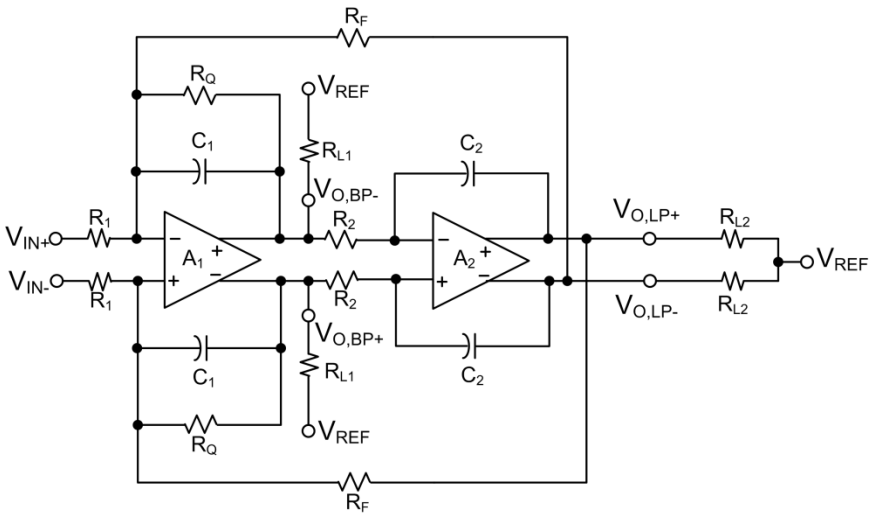

Figure 36 Biquadratic filter implementation

The design values of the passives other than the load resistors, R_{L1} and R_{L2} was shown in Table 1 in Subsection 3.2. R_{L1} is the resistor that connects the band-pass output

($V_{O,BP+}$ and $V_{O,BP-}$) of the filter to the summing amplifier. R_{L2} is a parallel combination of the resistor that connects the low-pass output of the filter to the summing amplifier and the input resistance of the next stage of the filter. V_{REF} is the common-mode level of the filter. The value of the load resistors and V_{REF} is shown in Table 6.

Table 6 Bias and load conditions of the filter

Parameter	**Value**
R_{L1}	1.7 kΩ
R_{L2}	3.03 kΩ || 2.875 kΩ
V_{REF}	900mV

The design, implementation and performance metrics of amplifier A_1 was discussed in detail in the Section 4. The performance requirements from amplifier A_2 are relaxed when compared to the amplifier A_1. However, in-order to minimize design effort, the same amplifier topology has been used to design A_2 as well. Three different amplifiers that use different output stages similar to the amplifier A_1 have been designed. The performance achieved by the three amplifiers is shown in Table 7.

Table 7 Amplifier 2 performance summary

Parameter	**Op-Amp with proposed output stage**	**Op-Amp with class-AB output stage with Monticelli bias scheme**	**Op-Amp in [3]**
DC Gain	53.1 dB	52.4 dB	47.3 dB
Gain at 25MHz	40.66 dB	39 dB	40.65 dB
Phase Margin	56^0	57^0	59^0
Integrated noise in 25 MHz	29.16 μV_{rms}	34.16 μV_{rms}	27.91 μV_{rms}
Power Consumption	1.6 mW	1.96 mW	1.6 mW

5.2 Simulation results

The three filter implementations which differ only in the amplifiers used are compared in this section. Special focus is given to power consumption and linear performance of the filter. Since these parameters are influenced mainly the amplifiers, they serve as a metric of comparison for the amplifiers.

5.2.1 Comparison of basic filter parameters

The basic parameters such as pass-band gain, quality factor, cut-off frequency, input referred noise and current consumption are shown in Table 8. It can be seen that the parameters such as pass-band gain, quality factor and cut-off frequency are set by passives and do not depend on the amplifiers. Hence they are very similar. It was previously shown in Subsection 3.3 that the noise of the filter is primarily dominated by the resistors in the filter, and hence the integrated input referred noise of the three filter implementations from DC to 25MHz are almost the same in the three implementations. However the power consumption of the filter is entirely due to the amplifiers and hence the filter using the proposed op-amps outperforms the other two implementations.

Table 8 Comparison of filter parameters

Parameter	**Filter with op-amps using proposed class-AB stage**	**Filter with op-amps from [3]**	**Filter with op-amps using Monticelli class-AB stage**
Cut-off Frequency	24.84 MHz	24.94MHz	24.7 MHz
Pass band gain	15.93 dB	15.93 dB	15.93 dB
Peak pass band gain	32.56 dB	32.16 dB	32.91 dB
Quality factor	6.78	6.49	7.06
Current consumption	2.5 mA	3.425 mA	3.1 mA
Integrated noise in 25MHz	38.22 μV	38.28 μV	40.48 μV

The AC response of the filter (using the amplifiers with the proposed output stage) at the low-pass and the band-pass outputs are shown in Figure 37 and Figure 38 respectively.

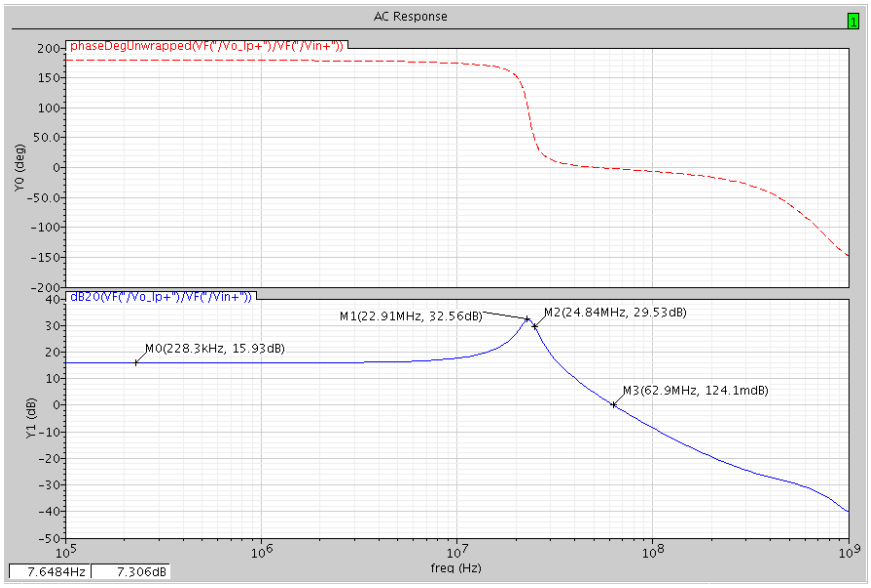

Figure 37 AC response of the filter at the low pass output

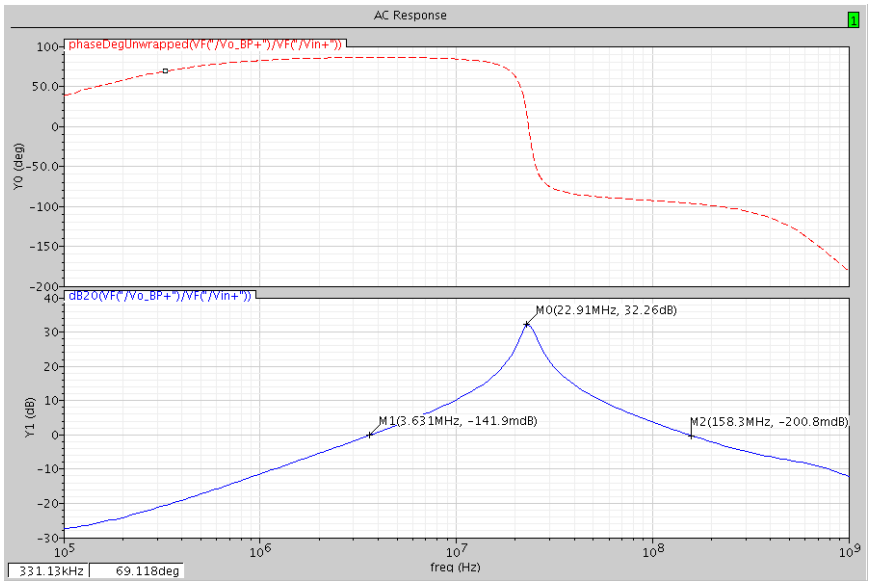

Figure 38 AC response of the filter at the band pass output

It can be seen from the figures that the gain of the filter in the low-pass output is greater than or equal to the gain at the band-pass output in-band frequencies, and vice versa for out-of-band frequencies. This is an important observation for conducting tests on the linearity of the filter, as it is required to have a full-scale swing at the correct output without exceeding the linear range at the other output. Hence in-band linearity tests are conducted with full-scale output swing at the low-pass output and out-of-band linearity tests are conducted with full-scale output swing at the band-pass output. This is the worst case scenario for linearity simulations without exceeding the linear output range of the filter.

5.2.2 In-band linearity

In-order to measure in-band linearity of the filter, two tones that are spaced 1MHz apart in frequency are swept simultaneously in frequency over the entire pass-band. The power of the tones is chosen such that the swing at the low-pass output covers the entire full scale range of $400\text{mV}_{\text{p-p}}$ differential swing at the peak gain of the low-pass transfer function, $A_{V,peak}$. The expression for the input power can be derived as shown in equation (5.3).

$$\text{Total } P_{OUT,rms} = -3\text{dBFS} \tag{5.1}$$

$$\text{Total } P_{IN,rms} = -3\text{dBFS} - A_{V,peak} \tag{5.2}$$

$$\text{Power of each input tone} = \text{Total } P_{IN,rms} - 3\text{dB} \tag{5.3}$$

A plot of IM3 versus the average of the two-input frequencies is shown in Figure 39.

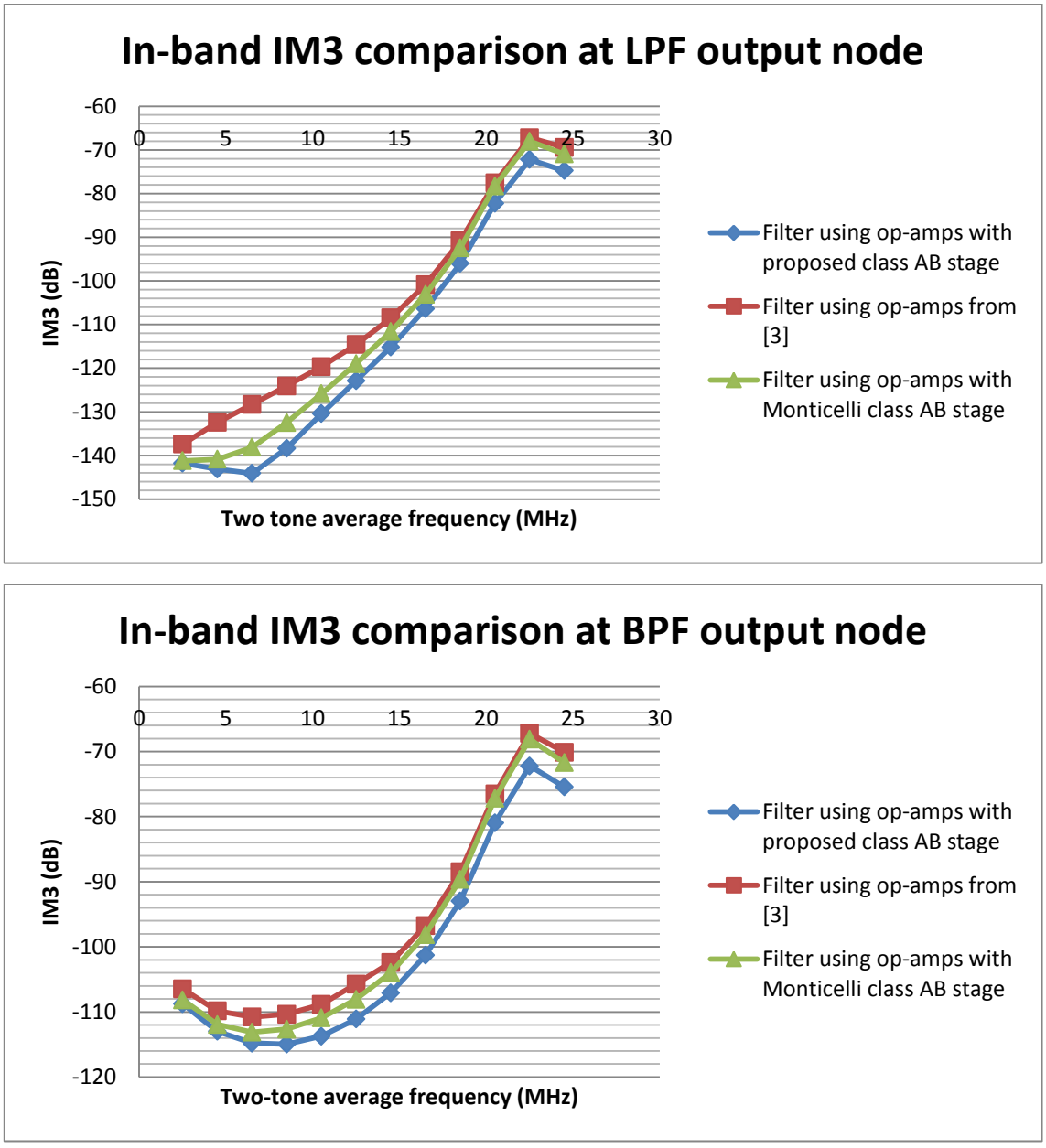

Figure 39 Comparison of in-band IM3 vs the average frequency of the two input tones (that have 1MHz spacing)

It can be seen that the IM3 of the three filters are quite similar. The worst case value of IM3 corresponds to the case when the input tones are applied at 21MHz and 22MHz; this drops an intermodulation product at 23MHz, which corresponds to the peak gain frequency. The output swing corresponds to full-scale power for this set of tones.

The IM3 corresponding to these two tones is around -70dB for all the three implementations. The implementation with the op-amps using the proposed class-AB output stage has marginally better IM3 than the other two implementations owing to the fact that it has a higher V_{DSAT} in the output transistors producing to a larger linear range.

5.2.3 Out-of-band linearity

The ADC designed in [9] is tailored for receiving WIMAX applications in digital television applications, where there are several adjacent channels. These adjacent channels are out-of-band blockers which can have much higher power than the in-band channel being down-converted. Since the filter used in a sigma-delta ADC has a pass-band gain, the gain is greater than unity for frequencies up to three times the cut-off frequency of the filter. Hence the adjacent channels in this frequency range are amplified by the filter. Due to the non-linear nature of the filter, these out-of-band blockers may create intermodulation products that can fall in the in-band frequencies and corrupt the useful signal information. The effect of the intermodulation products is greatest when it occurs at the peak gain frequency, as it will be amplified greatly. Hence the worst case scenario for out-of-band linearity is when two out-of-band tones create an in-band tone at the peak gain frequency.

In order to obtain a measure of out-of-band linearity, two tones of equal power at out-of-band frequencies are chosen such that their intermodulation product appears at the peak gain frequency. The power of the two tones is increased until the band-pass output has full-scale swing (corresponding to -3dBFS output power). This is the very worst case scenario for out-of-band linearity for this set of input tones. This experiment is done for two different sets of frequencies – 40MHz & 57MHz and 55MHz & 87MHz. A plot of input-referred in-band intermodulation tone power versus the total input power for blocker tones at 40MHz & 57MHz is shown in Figure 40. A similar plot for blocker tones at 55MHz and 87MHz is shown in Figure 41.

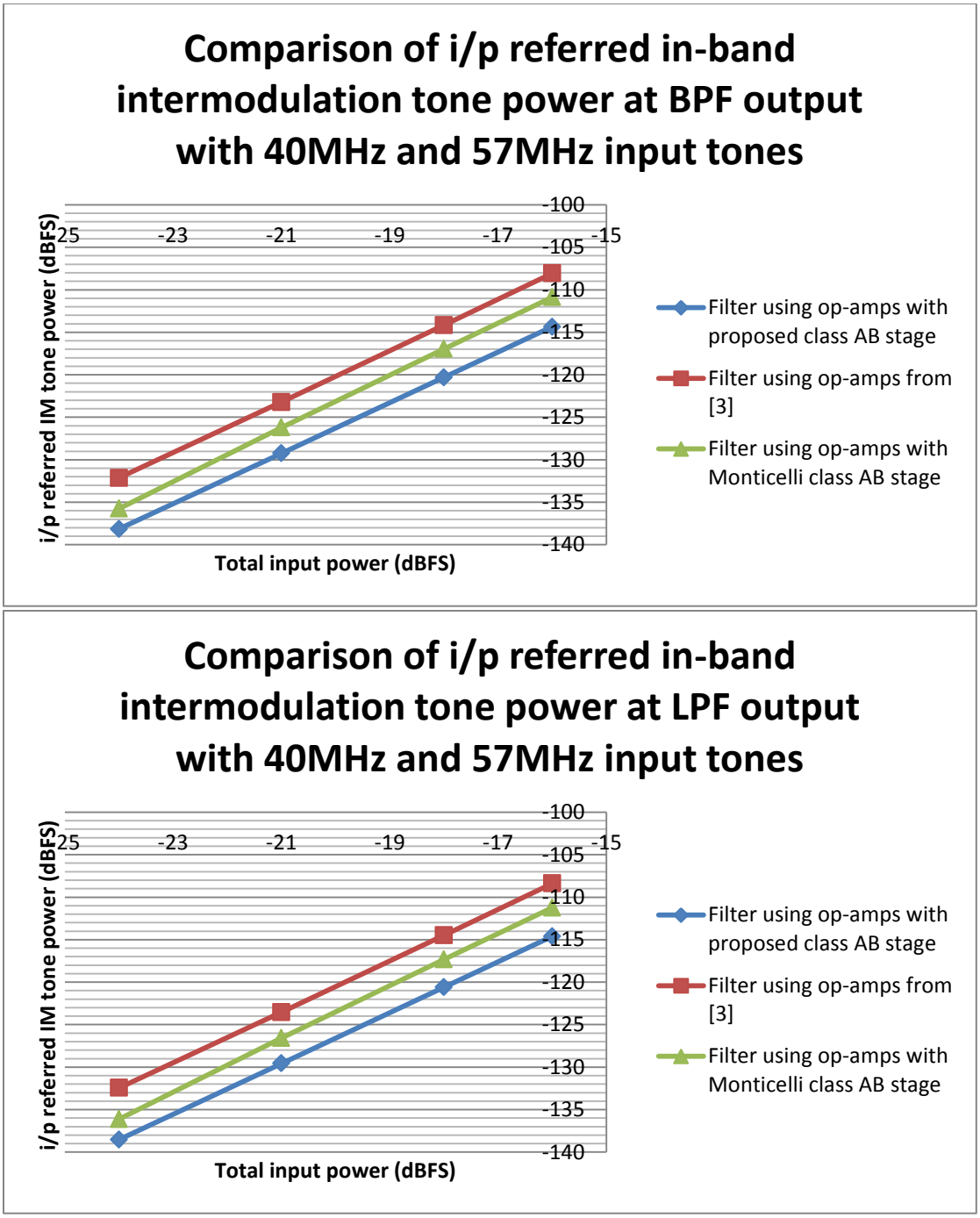

Figure 40 Comparison of input referred in-band intermodulation tone RMS power vs total input RMS power at the LPF and BPF outputs with 40MHz and 57MHz input tones

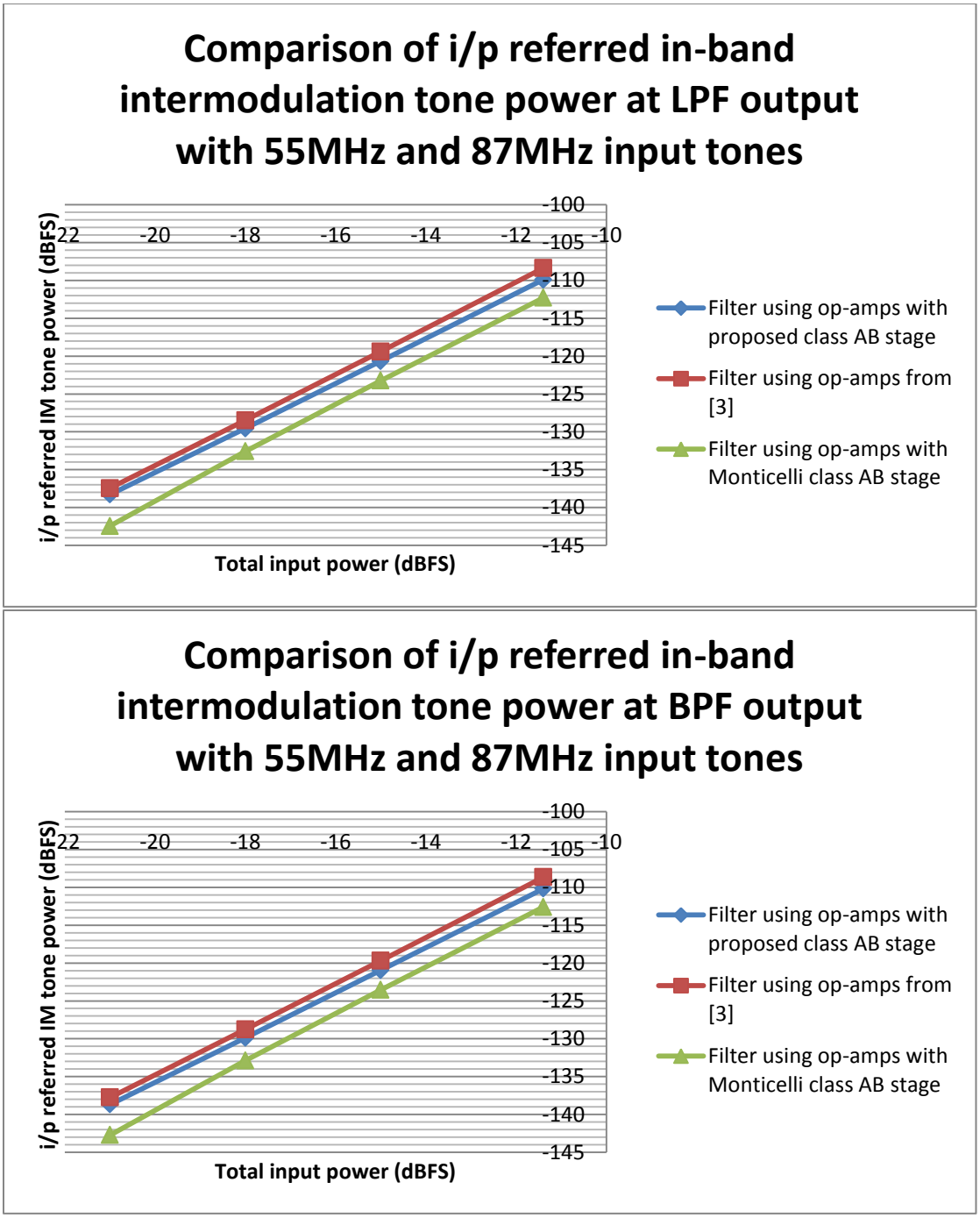

Figure 41 Comparison of input referred in-band intermodulation tone RMS power vs total input RMS power at the LPF and BPF outputs with 55MHz and 87MHz input tones

The input tones chosen in the first case – 40MHz and 57MHz - are such that both the blocker tones are in the transition band of the filter. This is the most critical case for linearity. The input power cannot be increased beyond -16dBFS, as -16dBFS input power causes a full scale output swing at the band pass node. Similarly in the case of 55MHz and 87MHz blockers (one of the two blockers are in the transition band), the maximum input power that can be applied is -11.4dBFS.

The input referred in-band intermodulation tone power at the peak gain frequency (23MHz) is plotted in y-axis in all the 4 graphs. This gives a direct idea of the unwanted intermodulation tone power that will appear at the input of ADC. It is seen that the intermodulation tone power is well below the ADC quantization noise power (-74dBFS).

5.2.4 Even-order distortion

In the in-band and out-of-band linearity simulations done in Subsection 5.2.3 and Subsection 5.2.4, the amplifier is assumed to be purely differential with a fully differential output, hence the third harmonic component was considered to be the most important component of harmonic distortion. The even-order terms were assumed to cancel out. However in a practical scenario, due to mismatch the even-order harmonics don't cancel out perfectly, and the second-order harmonic component forms the significant even-order component for distortion.

In order to find the effect of even-order distortion, Monte-Carlo simulations modeling mismatch are run and the power of the input referred second-order intermodulation product tone is observed. Both in-band and out-of-band characterization is done. Two tones are applied at 25MHz & 2MHz and 35MHz & 58MHz, so that the second-order intermodulation product appears at 23MHz (peak gain frequency of the pass-band). The input power of the tones are set to such a value that the output power of the tones is swinging full scale at the low pass output for in-band input tones or at the band pass output for out-of-band input tones. The mismatch models from the process

vendor are used. For a device area of 1µm x 1µm, the mismatch in area is approximately 1% and the mismatch in the threshold voltage of the devices is 2%. The percentage of mismatch introduced is inversely proportion to the square root of device area. The total number of runs for Monte-Carlo simulations was 50.

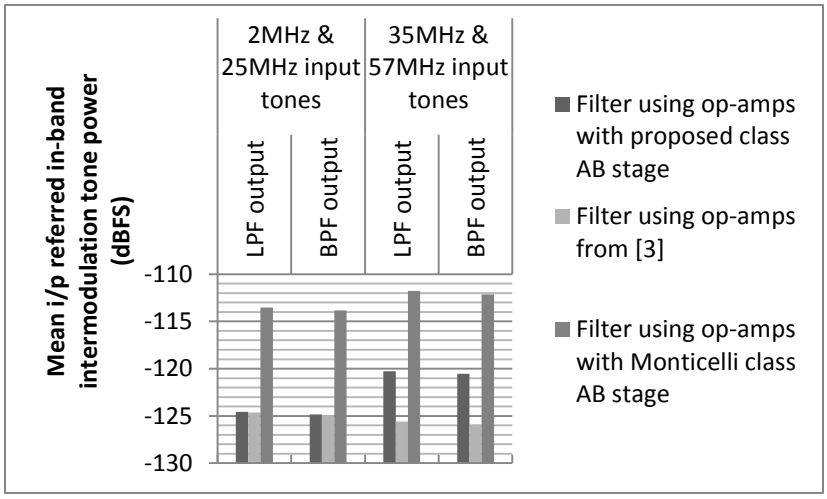

Figure 42 Mean of input-referred second-order intermodulation product power for the three filter implementations with 2 sets of input tones - 2MHz & 25MHz and 35MHz & 57MHz

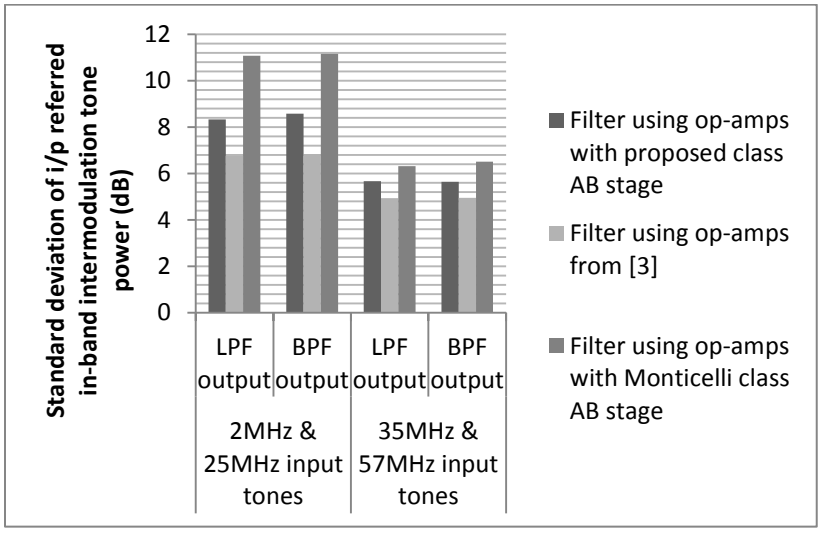

Figure 43 Standard deviation of input-referred second-order intermodulation product power for the three filter implementations with 2 sets of input tones - 2MHz & 25MHz and 35MHz & 57MHz

The plot of mean and standard deviation of input-referred second-order intermodulation product power for the three different implementations are shown side by side in Figure 42 and Figure 43 respectively. From the figures, we can see that the filter using amplifier with the proposed output stage is more tolerant to mismatch when compared to the one using amplifiers with class-AB output stage using Monticelli bias. It was previously explained in Subsection 4.4.2 that the bias information present at the gates of the output stage transistors are extracted using a common-mode sensing circuit and regulated to match a reference voltage by using a feedback loop. Hence the bias circuit provides the function of an additional common-mode feedback circuit in the signal path, which explains the better mismatch tolerance of the proposed output stage. From the figures, it also evident that the tolerance to mismatch of the proposed amplifiers is comparable to the mismatch tolerance of class-A amplifiers in [3].

6. LAYOUT AND POST-LAYOUT SIMULATION RESULTS

This section shows the layout of two biquadratic filter implementations, namely, the filter using amplifiers with the proposed class-AB output stage and the filter using amplifiers with conventional class-AB output stage. Since we have already established from the results in the previous section that the three amplifier topologies achieve comparable performance and our aim is to propose a new class-AB output stage, only the class-AB output stage amplifiers have been chosen for post-layout simulations. The list of pins on the layout and details of bias conditions that are required are mentioned and the post-layout simulation results are presented.

6.1 Layout implementation

The layout of the filter implemented using the op-amps with the proposed class-AB bias stage is shown in Figure 44. The layout occupies an area of 0.4mm x 0.28mm.

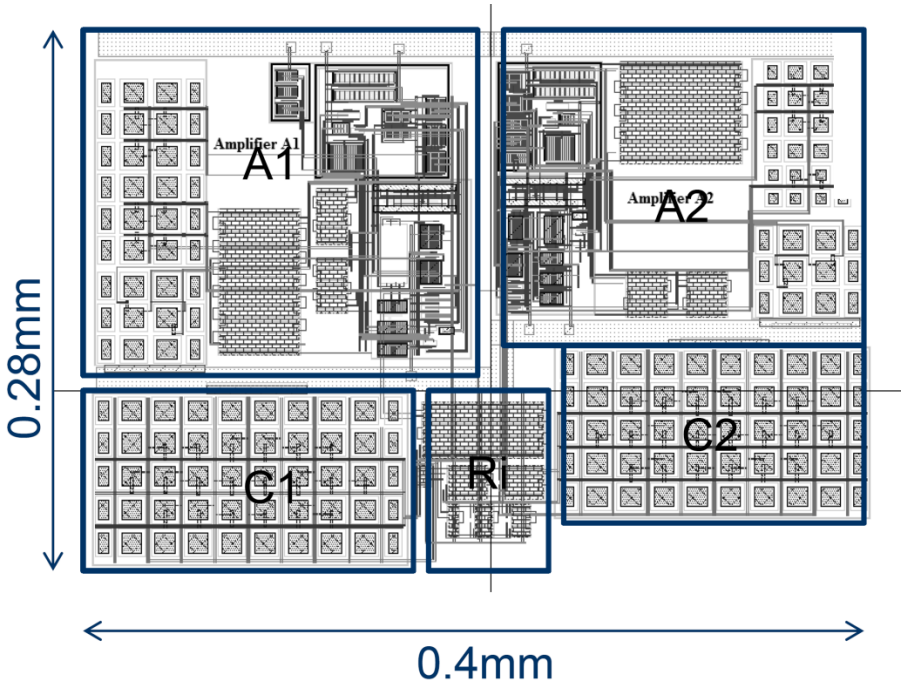

Figure 44 Filter layout with op-amps using proposed class-AB output stage

The implementation was done in TSMC 0.18µm technology. The list of pins on the filter and the corresponding connections that need to be made are tabulated in Table 9. For the currents listed in Table 9, a positive value of current indicates that a current source sourcing current needs to be connected to the pin and a negative value of current indicates that a current sink needs to be connected to the pin.

Table 9 Pin connections for filter with op-amps using proposed class-AB output stage

Pin	**Connection**	**Pin**	**Connection**
Vin+	Input stimulus	Vout_LP+	Probe
Vin-	Input stimulus	Vout_LP-	Probe
Vref	900mV	Vout_BP+	Probe
Vdd	1.8V	Vout_BP-	Probe
Amp1_50uA	50µA	Amp1_2u	2µA
Amp2_50uA	50µA	Amp2_2u	2µA
Amp1+_Iout	300µA	Amp1-_Iout	-300µA
Amp2+_Iout	150µA	Amp2-_Iout	-150µA
Gnd	0V		

The layout of the filter implemented using Monticelli output stage based op-amps is shown in Figure 45. The layout dimensions are 0.35µm x 0.25µm. It can be seen that the new op-amps occupy more area than the Monticelli op-amps due to the additional capacitors that were used in the bias network as shown in Figure 31. The list of pins and the corresponding connections that need to be made are shown in Table 10.

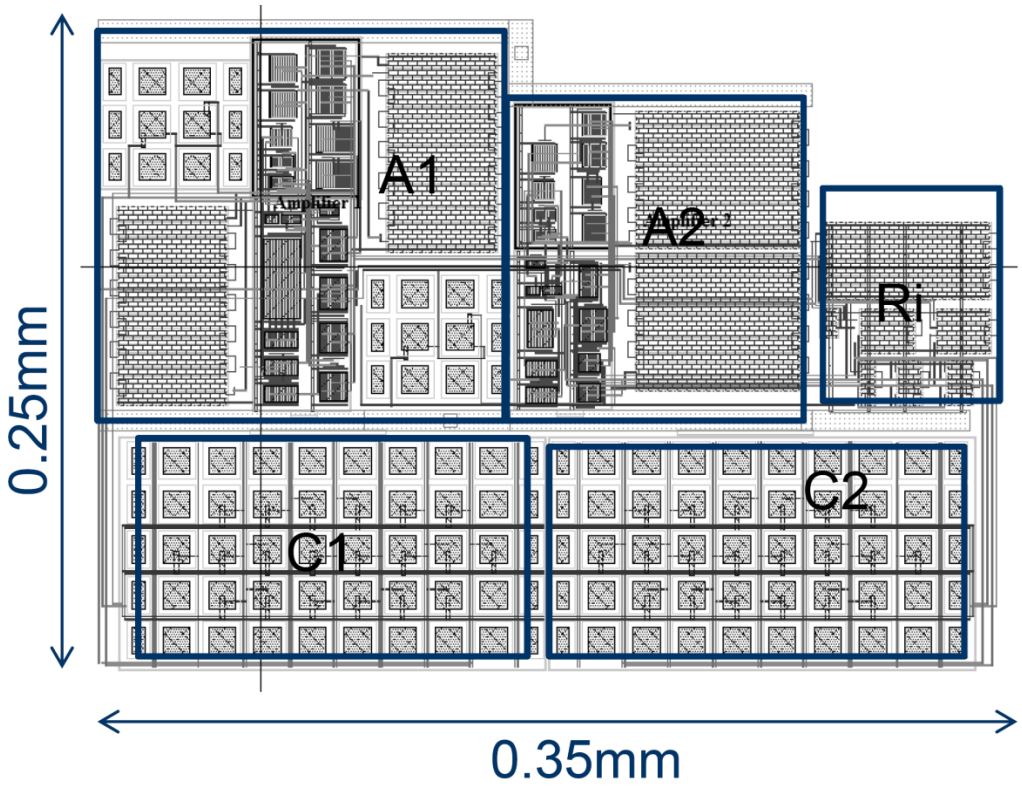

Figure 45 Filter layout with op-amps using Monticelli based class-AB output stage

Table 10 Pin connections for filter with op-amps using Monticelli based class-AB output stage

Pin	Connection	Pin	Connection
Vin+	Input stimulus	Vout_LP+	Probe
Vin-	Input stimulus	Vout_LP-	Probe
Vref	900mV	Vout_BP+	Probe
Vdd	1.8V	Vout_BP-	Probe
Amp1_50uA	50µA	Amp2_50u	50µA
Gnd	0V		

6.2 Post-layout simulation results

6.2.1 Amplifier parameters

The post-layout simulation results of the two amplifiers using the proposed class-AB output stage are shown in Table 11. Similarly the post-layout simulation results of the two amplifiers using conventional class-AB output stage are shown in Table 12.

Table 11 Post-layout simulation results for amplifiers with proposed output stage

Parameter	**Amplifier 1**	**Amplifier 2**
DC Gain	57.4 dB	53.1 dB
Gain at 25MHz	44.44 dB	39.73 dB
Phase Margin	52.8^0	52^0
Integrated noise in 25MHz	16.82 μV_{rms}	30.08 μV_{rms}
Current Consumption	1.5 mA	0.9 mA

Table 12 Post-layout simulation results for amplifiers with conventional class-AB output stage

Parameter	**Amplifier 1**	**Amplifier 2**
DC Gain	56 dB	52.37 dB
Gain at 25MHz	43.08 dB	38.76 dB
Phase Margin	50.6^0	49^0
Integrated noise in 25MHz	19.97 μV_{rms}	34.76 μV_{rms}
Current Consumption	2.2 mA	1.09 mA

From the results of the amplifier simulations we can observe that the DC and low frequency parameters such as DC gain and current consumption remain unaffected in the

post-layout simulations. However, the gain of the amplifiers at 25MHz is lower than the value obtained in schematic simulations. This is due to the presence of parasitics in the layout which reduces the frequency of the dominant pole. The decrease in phase margin indicates that the non-dominant pole at the output node has also been pushed to lower frequencies due to the presence of layout parasitics. The marginal increase in input-referred noise can be attributed to the decrease in gain at high frequencies, while referring the noise to the input.

6.2.2 Comparison of basic filter parameters

The basic parameters of the filter such as pass-band gain, cut-off frequency, quality factor, input referred noise and current consumption are shown in Table 13. It can be seen that the cut-off frequency and quality factor are slightly affected by the addition of parasitics of the layout and hence show a small difference in values when compared to the schematic simulations. But process-variations are likely to cause up to 30% variations in these values; hence these minor differences can be ignored. The other values are fairly consistent with schematic level simulations.

Table 13 Post-layout simulation results - Comparison of filter parameters

Parameter	**Filter with op-amps using propose class-AB output stage**	**Filter with op-amps using Monticelli based class-AB output stage**
Cut-off Frequency	24.31 MHz	22.58 MHz
Pass band gain	16.17 dB	16.17 dB
Peak pass band gain	32.29 dB	31.15 dB
Quality factor	6.4	5.62
Current consumption	2.5 mA	3.1 mA
Integrated noise in 25MHz	39.53μV	43.2 μV

The AC responses of the two filters are shown in Figure 46 and Figure 47. Each figure shows the AC response at both the low-pass and band-pass outputs. It can be seen that they are fairly consistent with their schematic-level simulation counterparts.

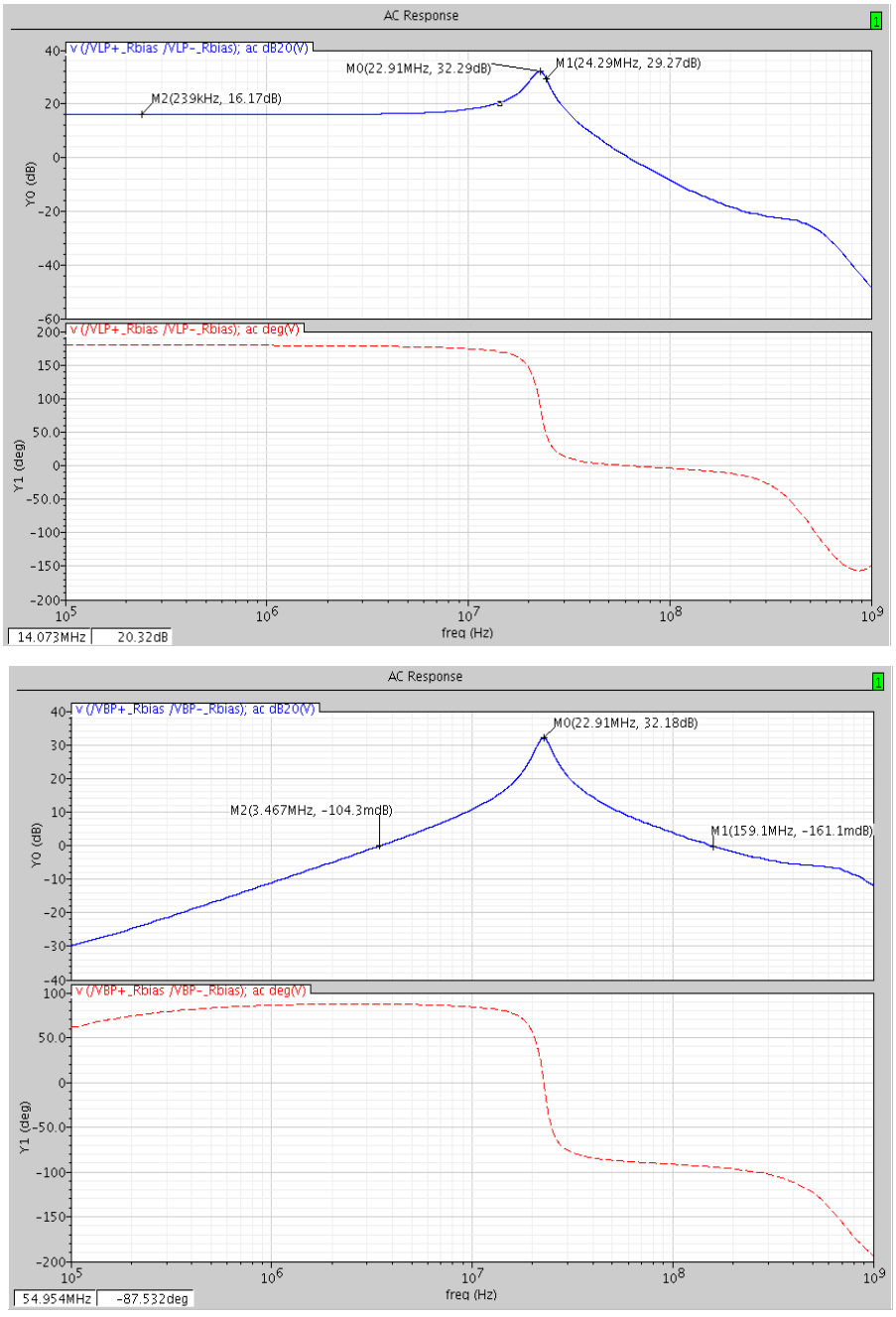

Figure 46 Post-layout results - AC response of filter using op-amps with proposed class-AB output stage

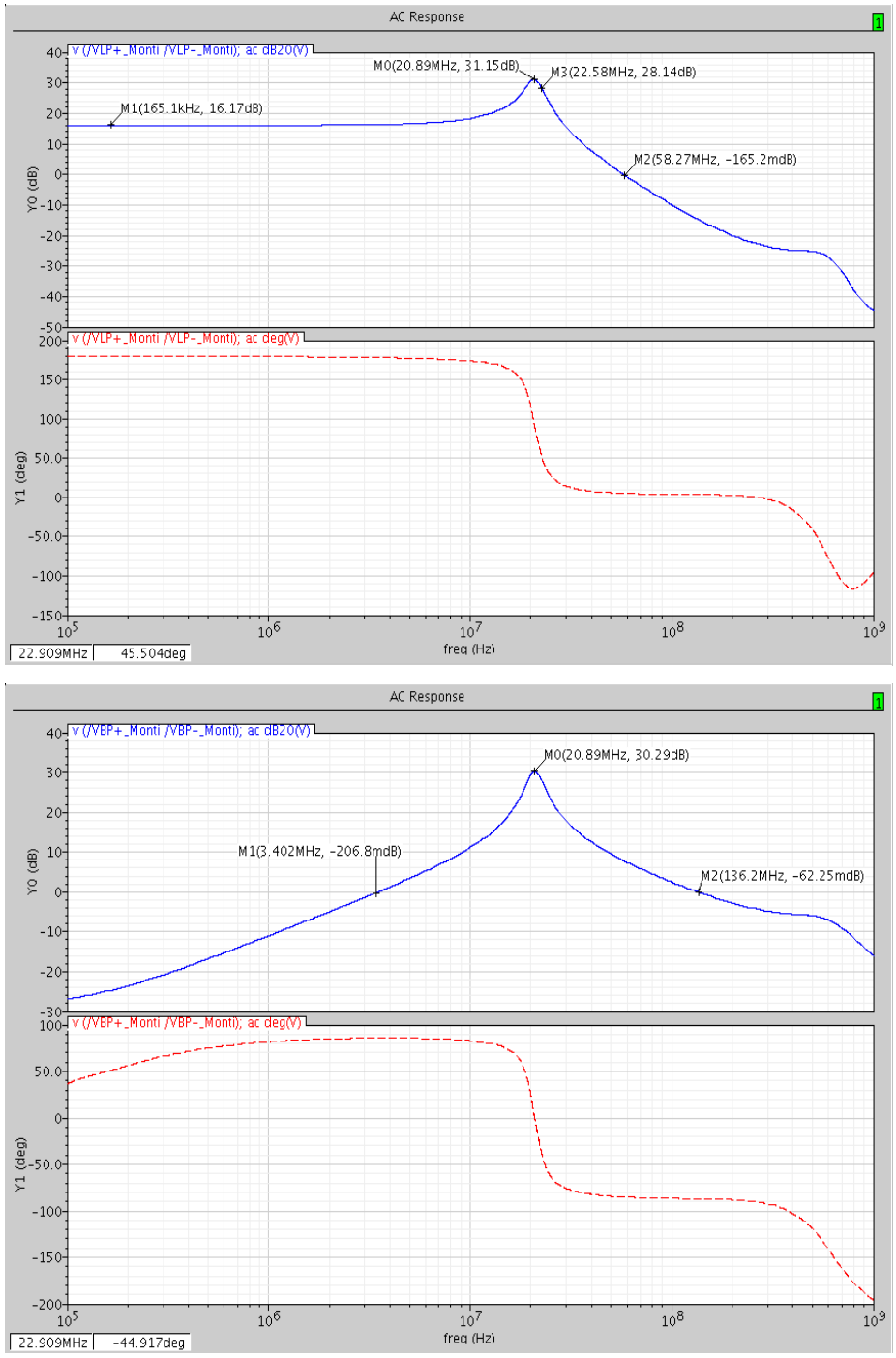

Figure 47 Post-layout results - AC response of filter using op-amps with Monticelli based class-AB output stage

6.2.3 In-band linearity

The two tone test explained in Subsection 5.2.2 is repeated. The power of the input tones is different from the ones used in schematic level simulations, since the peak gain has dropped in the layout. However the criterion to set the input power of the two tones is the same as the one described in Subsection 5.2.2. The plots are shown in Figure 48.

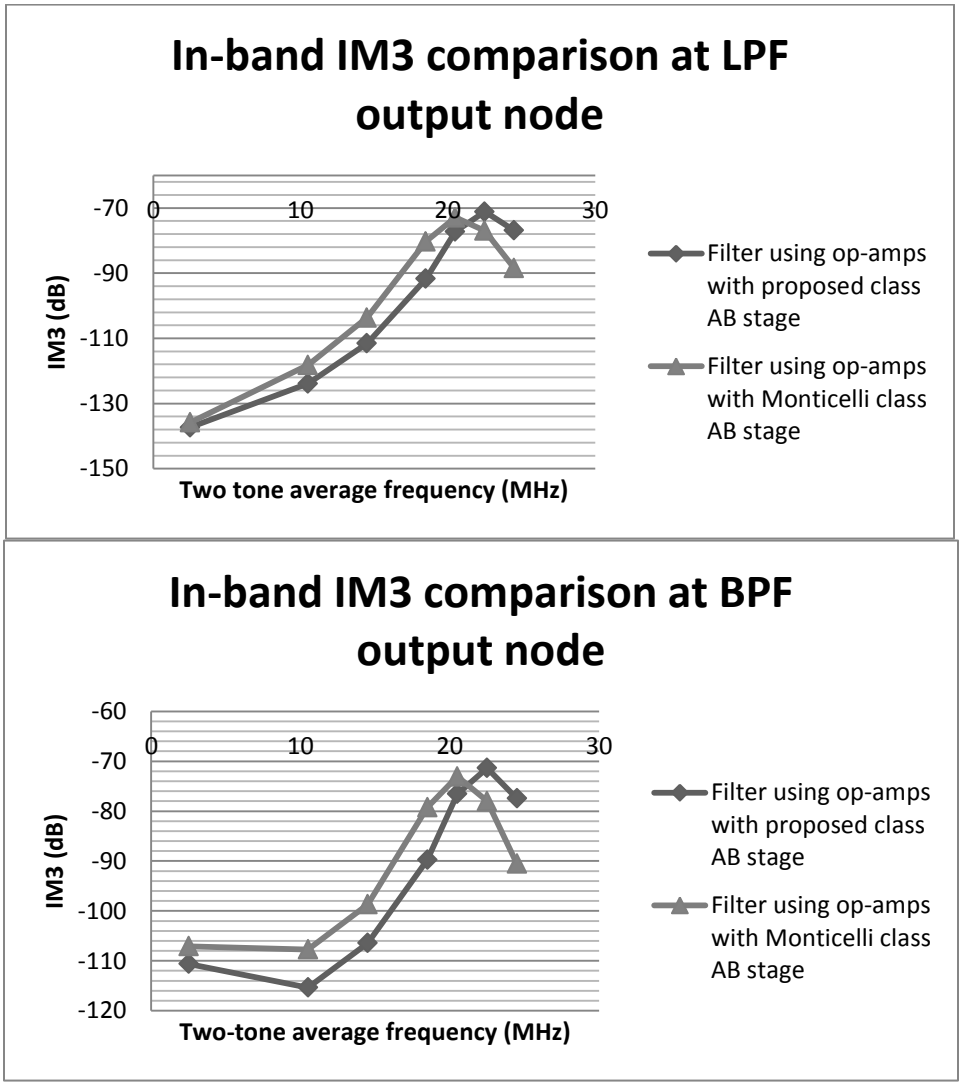

Figure 48 Post-layout results - Comparison of in-band IM3 versus average frequency of input tones (which are spaced 1MHz apart)

From Figure 48 we can see that both the filters have a worst case in-band IM3 of -72dB when the output is swinging full-scale (output power is -3dBFS), which is the same value of IM3 reported for the filter in [3] as well.

6.2.4 Out-of-band linearity

For analyzing the linearity performance of the filters in the presence of out-of-band blockers the experiment explained in Subsection 5.2.3 is repeated. However in this case the frequencies of blockers need to be adjusted so that the intermodulation product appears at the peak-gain frequency of that filter. For the case of the filter using the op-amps with proposed output stage, the peak gain frequency is the almost same as the case of schematic simulations (23MHz), but in the other filter, the peak gain frequency occurs at 21MHz. Hence one of the blocker frequencies is adjusted and we use 40MHz & 59MHz as one set of tones and 55MHz & 89MHz as the other set of tones for the filter using op-amps with Monticelli-based class-AB output stage. The filter using op-amps with proposed class-AB output stage is tested with the same tones as in Subsection 5.2.3, which are 40MHz & 57MHz and 55MHz & 87MHz.

The plot of input-referred 3rd order intermodulation product power versus input power is shown in Figure 49. The input power is swept until the output power is -3dBFS at the band pass node. The peak input power that can be applied in the case of 40MHz & 57MHz blockers is -16dBFS. It can also be observed that the power of the intermodulation product generated is almost the same in both cases, and well below the quantization noise level.

Similarly, a plot of input referred 3rd order intermodulation product versus input power is shown in Figure 50. In this case, the input power is swept up to -11.4dBFS to obtain -3dBFS output power at the band-pass output.

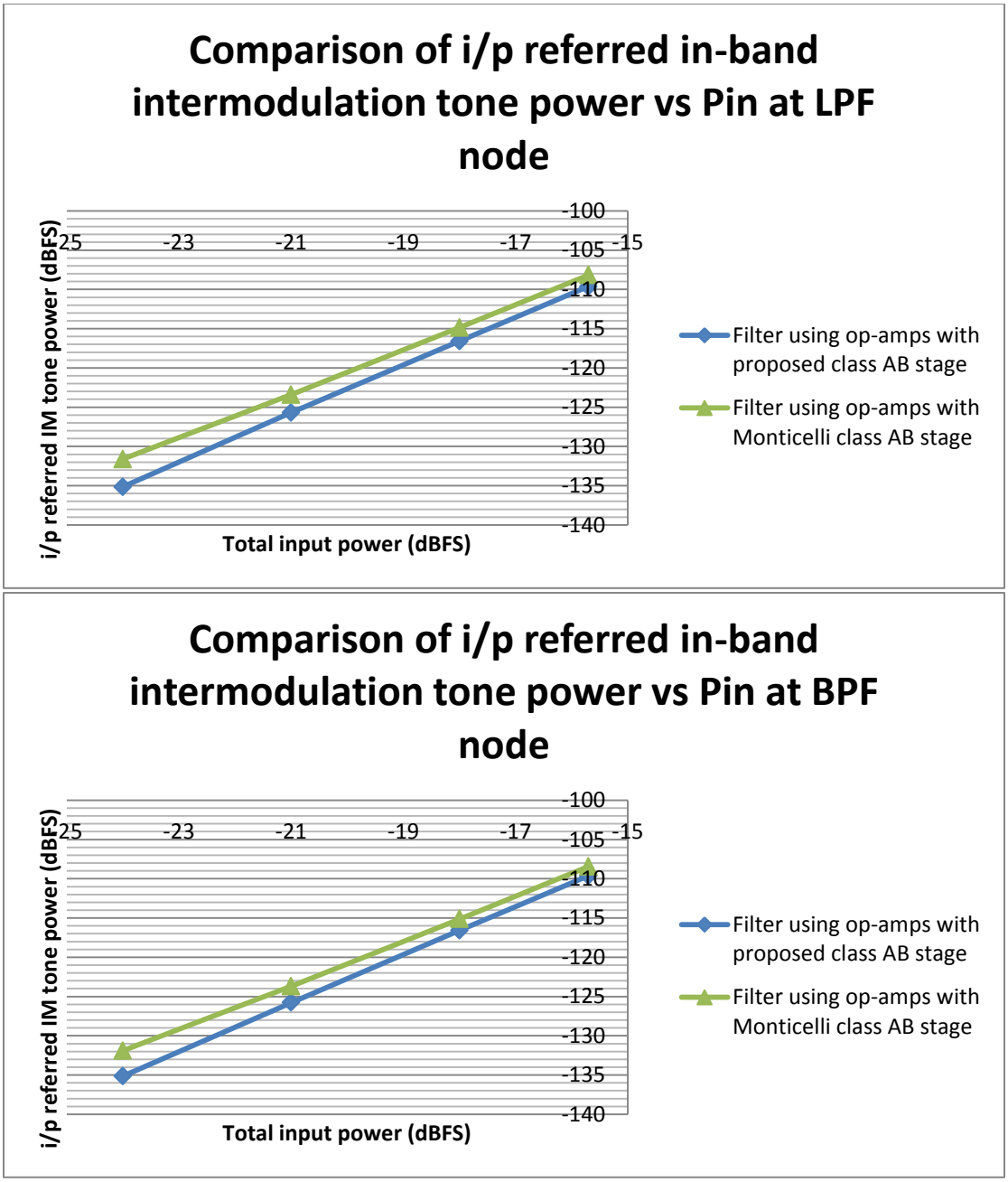

Figure 49 Comparison of input-referred in-band intermodulation tone RMS power vs total input RMS power at the LPF and BPF outputs with 40MHz and 57MHz tones (59MHz for Monticelli) at biquad input

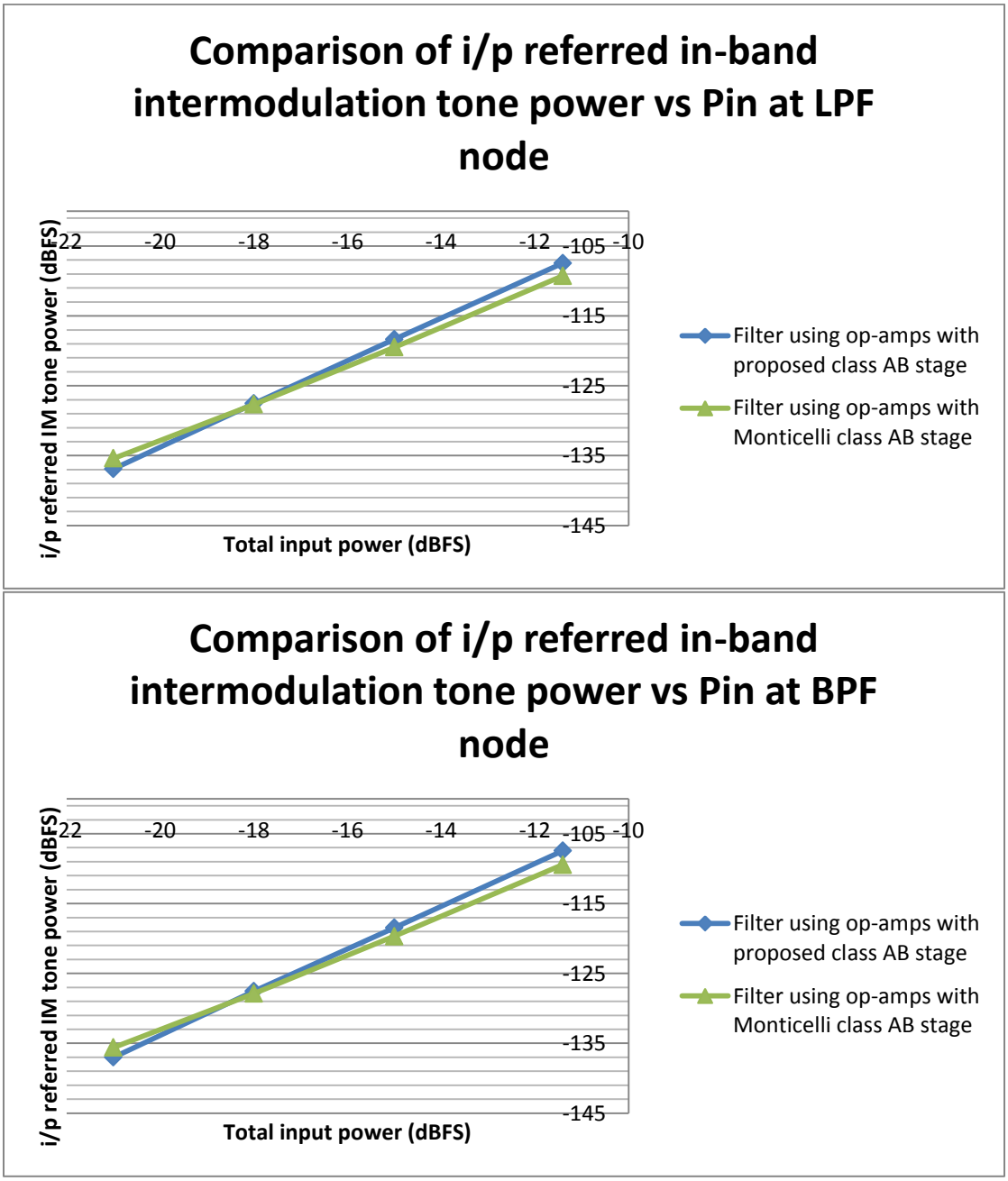

Figure 50 Comparison of input referred in-band intermodulation tone RMS power vs total input RMS power at the LPF and BPF outputs with 55MHz and 87MHz tones (89MHz for Monticelli) at biquad input

It can also be observed that the power of the intermodulation product generated is almost the same in both cases, and well below the quantization noise level. The linearity

performance is slightly worse in the post-layout simulations compared to schematic-simulations. This can be attributed to the role played by parasitics at high frequencies.

7. CONCLUSION

In this thesis work, an amplifier using a new class-AB output stage has been proposed and a high-performance biquadratic filter used in a continuous-time sigma-delta ADC with 25MHz low-pass bandwidth and 12-bit resolution was used as a test bench to test the performance of the amplifier. The need for high-performance amplifiers in continuous-time sigma delta ADCs was discussed and the design requirements of the amplifiers were calculated from the performance requirements of the ADC in a top-down fashion. The particular case of a class-AB output stage amplifier has been considered and an improved bias stage for class-AB circuits in general has been proposed. The new bias scheme has good tolerance to process and mismatch variations, along with the ability to perform well over a wide range of frequencies. The new bias scheme has been tested in a realistic environment by using it to design a biquadratic filter and the results have been compared against similar amplifiers with class-A output stage and conventional class-AB output stage reported in literature. Apart from the variation tolerance and mismatch tolerance, the new scheme promises a significant saving in power consumption. The implementation has been carried out in TSMC 0.18μm.

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