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Towards Logic Functions as the Device using Spin Wave Functions Nanofabric

Prasad Shabadi
University of Massachusetts Amherst

TOWARDS LOGIC FUNCTIONS AS THE DEVICE USING SPIN WAVE FUNCTIONS NANOFABRIC

A Thesis Presented

by

PRASAD SHABADI

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Approved as to style and content by:

Csaba Andras Moritz, Chair

Israel Koren, Member

C. Mani Krishna, Member

C.V. Hollot, Department Chair
Electrical and Computer Engineering

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ABSTRACT

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MAY 2012

PRASAD SHABADI

B.E, BANGALORE UNIVERSITY

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Csaba Andras Moritz

As CMOS technology scaling is fast approaching its fundamental limits, several new nano-electronic devices have been proposed as possible alternatives to MOSFETs. Research on emerging devices mainly focusses on improving the intrinsic characteristics of these single devices keeping the overall integration approach fairly conventional. However, due to high logic complexity and wiring requirements, the overall system-level power, performance and area do not scale proportional to that of individual devices.

Thereby, we propose a fundamental shift in mindset, to make the devices themselves more functional than simple switches. Our goal in this thesis is to develop a new nanoscale fabric paradigm that enables realization of arbitrary logic functions (with high fan-in/fan-out) more efficiently. We leverage on non-equilibrium spin wave physical phenomenon and wave interference to realize these elementary functions called *Spin Wave Functions (SPWFs).*

In the proposed fabric, computation is based on the principle of wave superposition. Information is encoded both in the phase and amplitude of spin waves; thereby providing an opportunity for compressed data representation. Moreover, spin wave propagation does not involve any physical movement of charge particles. This provides a fundamental advantage over conventional charge based electronics and opens new horizons for novel nano-scale architectures.

We show several variants of the SPWFs based on topology, signal weights, control inputs and wave frequencies. SPWF based designs of arithmetic circuits like adders and parallel counters are presented. Our efforts towards developing new architectures using SPWFs places strong emphasis on integrated fabric-circuit exploration methodology. With different topologies and circuit styles we have explored how capabilities at individual fabric components level can affect design and vice versa. Our estimates on benefits vs. 45nm CMOS implementation show that, for a 1-bit adder, up to 40x reduction in area and 228x reduction in power is possible. For the 2-bit adder, results show that up to 33x area reduction and 222x reduction in power may be possible.

Building large scale SPWF-based systems, requires mechanisms for synchronization and data streaming. In this thesis, we present data streaming approaches based on Asynchronous SPWFs (A-SPWFs). As an example, a 32-bit Carry Completion Sensing Adder (CCSA) is shown based on the A-SPWF approach with preliminary power, performance and area evaluations.

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CHAPTER 1

INTRODUCTION AND MOTIVATION

The growth in the IC industry is primarily driven by CMOS technology scaling. This scaling trend is fast approaching its fundamental limits forcing researchers to look beyond the MOSFETs, the top-down CMOS manufacturing mindset, and the associated hierarchical multi-level logic organization. New devices based on alternate state variables like electron spin [11], molecular level physical phenomenon [45, 12], phase change [24] etc. are being actively investigated. In addition, novel FETs based on emerging nanomaterials e.g. built with nanowires [31, 47, 43], graphene ribbons [48] and carbon nanotubes [27, 25] are also being explored.

The focus of the device community has been on improving the intrinsic characteristics like switching delay, power, area and leakage in a single device. It is assumed that the rest of the paradigm for designing chips and the integration approach could remain unchanged from CMOS. Even novel computation paradigms that are based on alternate state variable also envision a simple controlled/gated switch as a basic device. The mindset here is to build complex logic functions with high fan-in using several basic gates with low fan-in/fan-out that are constructed using simple switches. However, due to high logic complexity and wiring requirements, the overall system-level power, performance and area does not scale proportional to that of individual devices. Furthermore, it is increasingly accepted that charge-based electronics is very competitive and there is no alternate state variable based switch on the horizon that would be much faster [14].

Can there be then a better, game-changing way to build future nanoscale systems? While there are many possible pathways to attack the nanoscale fabric problem, we propose to shift the focus towards new types of devices that can be made more functional than simple switches. Our goal is to develop a new nanoscale fabric paradigm that enables realization of arbitrary logic functions (with high fan-in/fan-out) more efficiently.

In this thesis, we explore one possible approach to realize the above fabric goal that is based on non-equilibrium spin wave physical phenomenon. Information is encoded in the phase and amplitude of propagating spin waves and computation is based on wave interference. Circuits exploiting wave interference enable accomplishing complex logic functions such as high fan-in majority function(s) in a single computational step. We introduce the concept of such magnonic functions also called as Spin Wave Functions (SPWFs) and discuss several variants. Since information is encoded both in phase and amplitude of spin waves, SPWFs enable compressed data representation and communication. Moreover, spin wave propagation does not involve physical movement of charge particles. Thereby, this computational paradigm is expected to be extremely energy efficient.

The main contributions of this thesis are

- We present our vision for computation in the future based on sophisticated logic functions as new devices.
- We introduce the fabric concept of Spin Wave Functions (SPWFs) for constructing magnonic logic circuits.
- Design of non-volatile simple arithmetic circuits like full adders and parallel counters using the proposed SPWFs
- We explore the need for integrated fabric circuit exploration for development of future nanofabrics.

- We evaluate benefits of SPWF designs vs. state-of-the-art CMOS designs.
- We present our initial explorations on Asynchronous SPWF pipeline designs.

The rest of the thesis is organized as follows: the background on spin waves and physical fabric components are presented in Chapter 2. The concept of SPWFs and its variants are discussed in Chapter 3. SPWF-based design of simple logic circuits is presented in Chapter 4. An integrated fabric circuit exploration methodology for SPWF nanofabric and evaluations of benefits vs. 45nm CMOS designs are discussed in chapter 5. Chapter 6 presents our initial explorations on Asynchronous SPWFs and a 32-bit Carry Completion Sense Adder is shown as an example. Chapter 7 concludes the thesis.

CHAPTER 2

SPIN WAVES FABRIC BACKGROUND

In this chapter, we present the background on spin waves physical phenomenon, fabric structure and discuss various fabric components. A brief theoretical background on magnetic dynamics for modelling spin wave propagation is also presented. Recent progress on experimental work on proof-of-concept demonstration of spin waves based logic and voltage controlled magnetization rotation in Magneto-Electric (ME) cell is also shown.

2.1 Introduction to Spin Waves

Spin waves, also called as magnons are the collective oscillations of electrons spins in a spin lattice around the direction of magnetization in ferromagnetic materials [38] [20]. Information may be encoded in the phase and amplitude of the propagating waves. Thereby, information on multiple waves can be represented in a compressed manner using a single spin wave. Spin wave propagation does not involve any physical movement of charge particles and thereby this computational paradigm is expected to be extremely energy efficient. Spin waves coherence length can be greater than tens of micro meters (at room temperature), which makes them highly suitable for logic realization [9].

Experimental work at the Device Research Laboratory at UCLA has demonstrated the room temperature operation of 5-input majority gate [40]. Fig. 2.1 shows a five-terminal spin wave test structure used in the experimental study of the prototype majority gate. The material structure from the bottom to the top consists of a silicon

substrate, a 300nm thick silicon oxide layer, a 20nm thick ferromagnetic layer made of $Ni_{81}Fe_{19}$, a 300nm thick layer of silicon oxide and a set of five conducting wires on top. The distance between the wires is $2\mu m$. Each of the five wires can be used as an input or an output port. In order to demonstrate a three-input one-output majority gate, three of the five wires were used as input ports, and two other wires were connected in a loop to detect the inductive voltage produced by the spin wave interference.

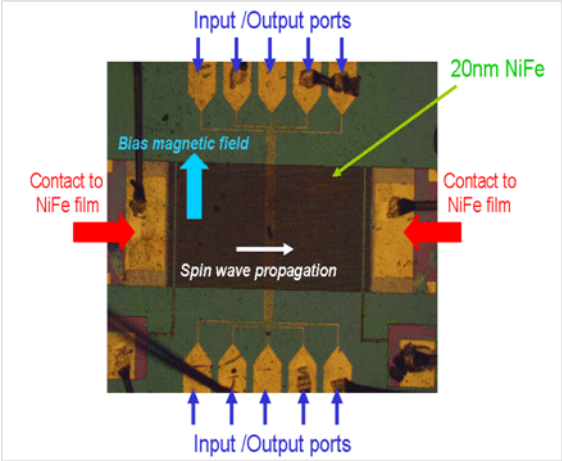


Figure 2.1. Image of the experimental prototype spin wave device for majority functions [40].

The plot in Fig. 2.2 shows the output inductive voltage detected for different combinations of input spin wave phases. An electric current passing through each wire generates a magnetic field, which, in turn, excites spin waves in the ferromagnetic layer. The direction of the current flow (the polarity of the applied voltage) defines the initial spin wave phase. The curves of different color in Fig. 2.2 depict the inductive voltage as a function of time for different combinations of the input spin wave phases (e.g. 000, 010, 011 and 111). These results show that, phase of the output inductive voltage corresponds to the majority of phases of the interfering spin waves. The data are taken for 3GHz excitation frequency and at bias magnetic field of 95Oe

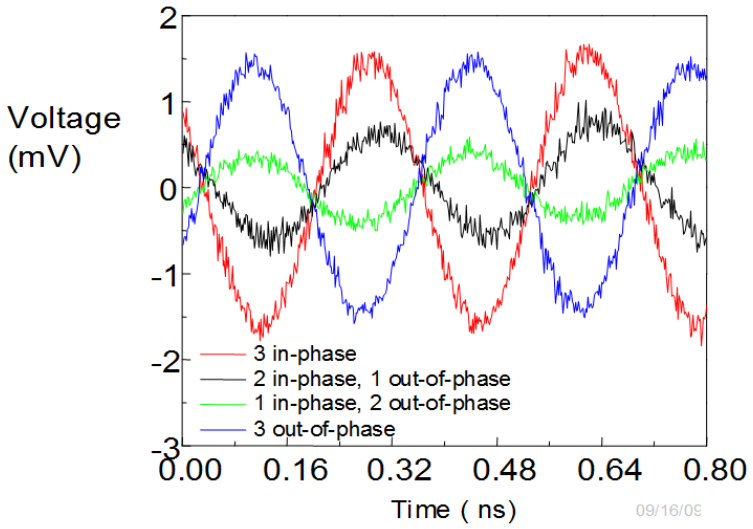


Figure 2.2. Experimental data illustrating majority device operation [40]. Image of the prototype is shown in Fig. 2.1. The frequency of operation is 3GHz. All data are measured at room temperature.

(perpendicular to the spin wave propagation). All measurements were accomplished at room temperature.

2.2 Physical Fabric Components

Fig. 2.3 shows the physical fabric structure and key physical components of the spin wave nanofabric. It consists of the Magneto-Electric (ME) cells and the Spin Wave Bus (SWB). The ME cells provide the essential coupling mechanism between the spin and charge domain. Based on the voltage polarity of the primary inputs, spin waves with corresponding phases are excited. In addition to providing the I/O mechanism, the ME cells also enable non-volatile storage of information via electric field control. In magnonic logic circuits, the ME cells are also used to provide amplification of intermediate waves to realize useful logic functionality. ME cells may also be used on the interconnect SWBs for signal restoration of propagating spin waves. Spin waves propagate and interfere in the Spin Wave Bus (SWB).

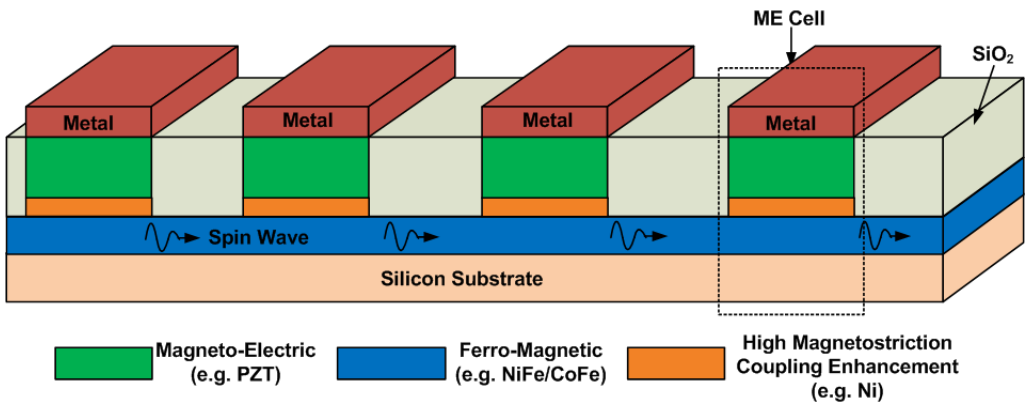


Figure 2.3. Physical structure of the spin wave nano-fabric showing ME cells and the spin wave bus.

Equation 2.1 shows the Landau-Lifshitz-Gilbert (LLG) formulation that is widely used for spin wave transport modelling [23] [15]. Prior research has shown that this formulation has good agreement with experimental data on spin wave transport (e.g. in NiFe thin films) [9].

$$\frac{\partial \vec{m}}{\partial t} = -\gamma \left[\vec{m} + \vec{H}_{eff}\right] + \alpha \left[\vec{m} * \frac{\partial \vec{m}}{\partial t}\right] \tag{2.1}$$

where, $\vec{m} = \frac{\vec{M}}{M_s}$ is the unit magnetization vector, M_s is the saturation magnetization, γ is the gyro-magnetic ratio and α is the phenomenological Gilbert coefficient.

$\vec{H}_{eff}$ is the effective field given as follows:

$$\vec{H}_{eff} = \vec{H}_d + \vec{H}_{ex} + \vec{H}_a + \vec{H}_b \tag{2.2}$$

Where, $\vec{H}_d$ is the magneto-static field associated with magnetization of the SWB due to application of external field. It is observed that, a change in $\vec{H}_{eff}$ results in change in M, which in turn changes the static field $\vec{H}_d$. Thereby, $\vec{H}_d$ is recursively used in the calculation of $\vec{H}_{eff}$. $\vec{H}_a$ is the anisotropy field generated due application of external voltage on the ME cell, $\vec{H}_{ex}$ is the exchange field due to incoming spin waves and $\vec{H}_b$ is the external bias field applied to align all the individual magnetic moments.

2.2.1 Voltage Controlled Magnetization Rotation in ME cells

A critical requirement for energy efficient generation, modulation, and detection of spin waves is the control of magnetization using electric fields (i.e. voltage) as opposed to currents (e.g. spin transfer torque or inductive coupling to current loops [4, 19, 5]). To realize voltage control of magnetization, layered heterostructures of piezoelectric and ferromagnetic films can be used [13]. A critical requirement for this scheme is that the magnetic films need to have a large magnetostriction coefficient, while still maintaining other properties critical to spin wave propagation such as low damping factor and small coercive field. Recent experimental progress at the Device Research Laboratory at UCLA has demonstrated non-volatile storage and voltage controlled magnetization rotation in ME cells. This is extremely important for low power operation of magnonic circuits [41].

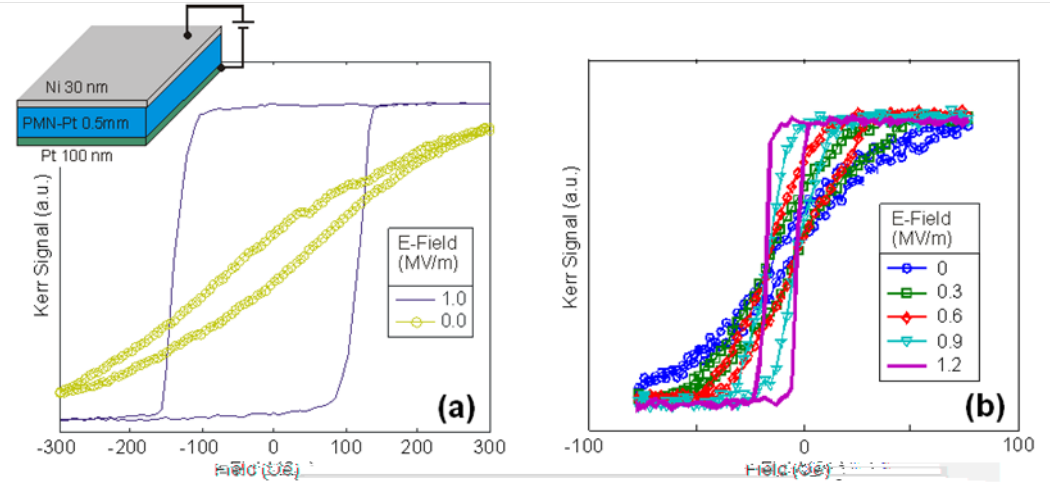


Figure 2.4. Experimental work on voltage controlled magnetization rotation in ME cells. (a) 30nm Ni films and (b) 30nm Ni 30 nm CoFeB bilayers on a piezoelectric PMN-PT substrate. A full 90 degree reorientation of the magnetic easy axis is achieved with approximately 1 MV/m field.

Fig. 2.4 shows an example of voltage control of magnetization for ferromagnetic single and bilayers. Fig. 2.4a shows Magneto-Optical Kerr Effect (MOKE) measure-

ments on a 30nm Ni film deposited on a piezoelectric PMN-PT substrate[1]. A 90 degree reorientation of the easy axis can be observed with approximately 1 MV/m field. It was also reported that the Ni film exhibits a rather large coercivity (approx. 100Oe), which is undesirable for high-frequency spin wave propagation. Fig. 2.4b illustrates a similar effect where a 30nm CoFeB film is added to the structure. While the magnetization rotation is achieved with a similar field, the coercivity is reduced to 10 Oe, significantly improving the soft magnetic characteristics required for the spin wave bus material. This is the first experimental demonstration of voltage-controlled magnetization rotation. In section 5.3.2, we show how these experimental results are used to estimate ME cell switching energy.

2.3 Chapter Summary

In this chapter, a brief background on spin waves physical phenomenon was discussed. Details of the physical fabric components namely the SWB and the ME cell were presented. The Magneto-Electric (ME) cell is a key component of the proposed fabric. It enables voltage control of magnetization which is critical for low energy operation. The ME cell is mainly responsible for i) I/O coupling ii) Amplification iii) Latching and iv) Synchronization.

The next chapter discusses the concept of Spin Wave Functions. Different flavours of the proposed SPWF concept are also presented.

[1]These results are based on the experimental work at Device Research Laboratory, UCLA, California.

CHAPTER 3

SPIN WAVE FUNCTIONS

In this chapter we introduce the concept of Spin Wave Functions (SPWFs). The principle of ***Compressed Data Representation*** in SPWFs is also introduced in this chapter. Detailed discussion on a simple 1-bit SPWF adder design that utilizes the compressed data representation feature is presented in section 4.2. Three types of SPWFs are discussed namely i) High Fan-in Majority (HFM) ii) Weighted High Fan-in Majority (WHFM) iii) Frequency Modulated WHFM (FM-WHFM), depending on different fabric level tuning knobs. Tuning based on amplitude of spin waves, number of control inputs, topology and excitation frequency of spin wave is presented. These SPWFs form the basic building blocks for the design of arithmetic circuits discussed in the next chapter. This chapter also summarises some of the major benefits of logic design using the proposed SPWF approach.

3.1 Concept of Spin Wave Functions (SPWFs)

Several proposals have been made towards implementing a highly efficient computational system at nanoscale. The primary focus in the emerging devices research community is to improve the intrinsic characteristics of single devices/switches keeping the overall integration approach fairly conventional. In contrast, our vision is to use sophisticated devices that can implement logic functions in one physical step as building blocks for more complex systems. Fig. 3.1 shows the basic idea of the device in conventional computational systems and our envisioned approach.

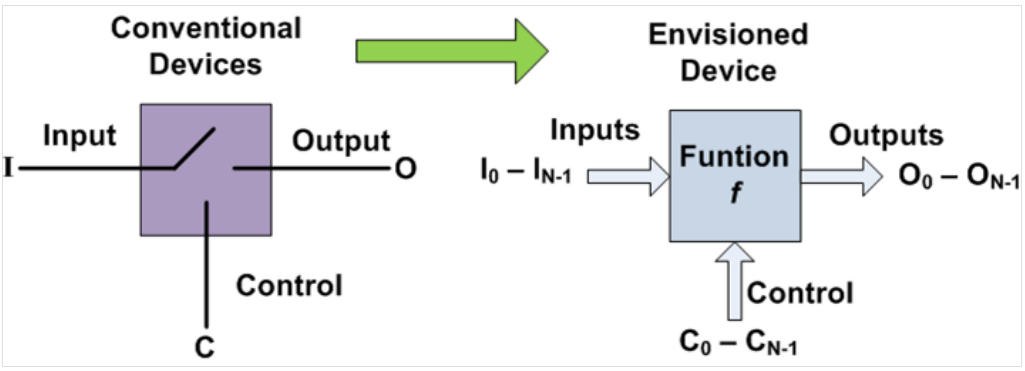


Figure 3.1. Our vision for devices in the future with alternate state variables.

In our approach, a single device simultaneously processes a large number of inputs and accomplishes sophisticated logic functions based on external control. The key requirements for such a device would be i) alternate ways to encode information utilizing novel physical phenomena (alternate state variables) and ii) new types of interactions between inputs/control achieving desired logic functionality.

Use of electron spin for computation has been identified as a promising alternative for building future nanoscale systems [14, 1]. Non-equilibrium physical phenomena with wave-based interactions could be leveraged to meet the above requirements. In a non-equilibrium fabric, switching times are lower than the thermal relaxation time, leading to fast processing. Information may be encoded in the amplitude and/or phase of a wave. Interactions between waves, such as interference or superposition, may then be utilized for achieving specific logic functions called as the ***Spin Wave Functions (SPWFs)***.

3.2 Compressed Data Representation in SPWFs

As described in the previous section, SPWFs encode information both in wave phase and amplitude. For example, a wave with phase '0' can represent 'logic 0' and a wave with phase 'π' can represent 'logic 1'. While additional wave phases

(like $\pi/4,\ 3\pi/4$) could potentially be used for **multi-valued** logic representation, currently we restrict the possible wave phases to only two values (phase '0' and 'π'). Adding more phases would reduce the noise margins due to higher sensitivity to phase distortions. However, since wave amplitude can also be used for information encoding, data on multiple waves can be represented in a compressed manner using only single (or few) wave. This significantly improves overall circuit implementation efficiency. Without such ***Compressed Data Representation*** feature, the individual waves would have to travel on separate waveguides. An example of compressed data representation in majority SPWFs is shown in this section.

Superposition interactions between spin waves naturally lend themselves to majority function implementation. For example, consider interference of three spin waves with equal amplitudes. If two of the waves are in phase '0' and the third wave is in phase '1', the resultant wave will be of phase '0'. Majority logic is an efficient way of implementing digital logic [3, 28, 30, 2]. Instead of using Boolean logic operators (e.g. AND, OR, NAND), majority logic represents and manipulates digital inputs on the basis of majority decision.

Fig. 3.2a shows schematics of majority logic gates in conventional (e.g. CMOS-based) Boolean logic. As shown in the Fig. 3.2a, the output provides a boolean representation of the majority of the three inputs. The output signal does not represent any information about the actual inputs participating in the majority function. In comparison, the output wave of the SPWF based majority gate shown in Fig. 3.2b, encodes information about inputs in the output wave amplitude. The output wave not only represents the majority decision, but also the actual number of logic '1's (or logic '0's) in the three inputs. The output wave phase represents the majority decision and the amplitude provides information about the inputs. This additional information is extremely useful in the design of efficient parallel counters, adders and other arithmetic circuits. A detailed description of this is provided in section 4.2.

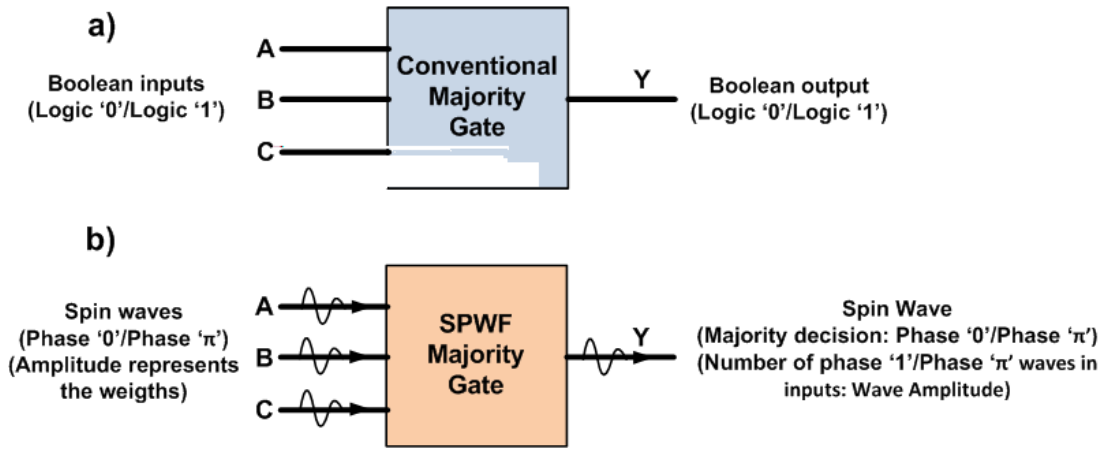


Figure 3.2. Comparison of data representation in SPWF and conventional majority logic gates. a) Data representation in conventional boolean logic based majority gates. b) Data representation in SPWF based majority gates. Output wave phase represents the majority decision and amplitude represents the actual number of input waves with phase '0'/phase 'π'.

3.3 Types of SPWFs

The majority function described in the previous section is an example Spin Wave Function (SPWF). Additional functionality can be obtained by adjusting various other physical parameters: i) Amplitude of input signals and control can be manipulated using ME cells; ii) Frequency multiplexing can be used to simultaneously transmit several spin waves over a waveguide with different functionalities realized for different frequencies; iii) Control inputs (inputs that alter, for example, the majority decision) can be modified to achieve arbitrary functionality. Moreover, a small number of control signals can be used with a large number of inputs by adjusting the amplitude of the control; and iv) Topology of the circuits can be adjusted to modify spin wave interactions. These knobs provide much flexibility to achieve sophisticated logic functions in a single step.

Three flavours of the SPWFs are described here i) High Fan-in Majority(HFM) ii) Weighted High Fan-in Majority(WHFM) and iii) Frequency Modulated WHFM (FM-WHFM).

3.3.1 High Fan-in Majority SPWF (HFM-SPWF)

Fig. 3.3 shows the SPWF-based schematic of a HFM. Here, all inputs ($I_0 ... I_{n-1}$) are of equal amplitude but may have different phases. A simple superposition of the waves would yield a majority function at the output node. Furthermore, by using a control signal C(A) whose amplitude is modulated by an ME cell, different Boolean logic operations may be obtained. A circular arrangement of inputs may be used to address the signal attenuation: spin-waves travel an equal distance before interacting and are therefore attenuated by the same amount, leading to correct superposition.

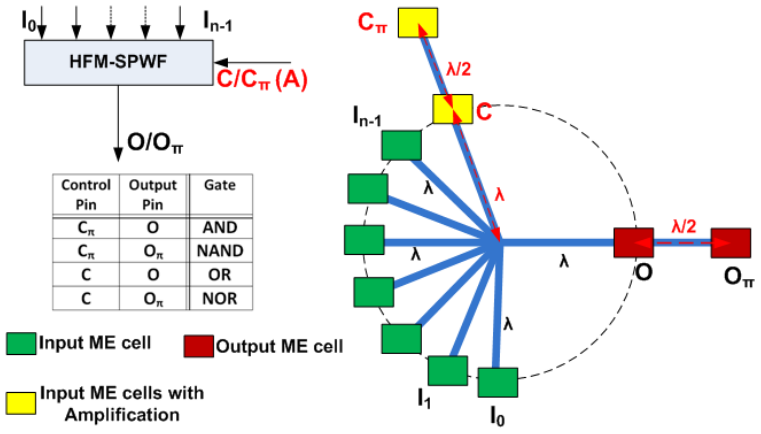


Figure 3.3. Block diagram and schematic representation using waveguides and ME cells for realizing High Fan-in Majority Function (HFM) SPWF.

3.3.2 Weighted High Fan-in Majority SPWF (WHFM-SPWF)

In the HFM-SPWFs, all the interfering spin waves have equal amplitude and by varying the amplitude of the control input, arbitrary functions could be implemented. Additional functionality may be obtained by modulating the amplitudes of input spin waves for realization of a weighted majority function. Fig. 3.4 shows the schematic of a WHFM-SPWF where data inputs and control inputs not only encode information in phase, but also in the amplitude of propagating spin waves. This leads to compressed transmission of information, thereby resulting in efficient implementation of

large scale systems. WHFM-SPWF based adder designs that leverage on the data compression feature are presented in the next chapter.

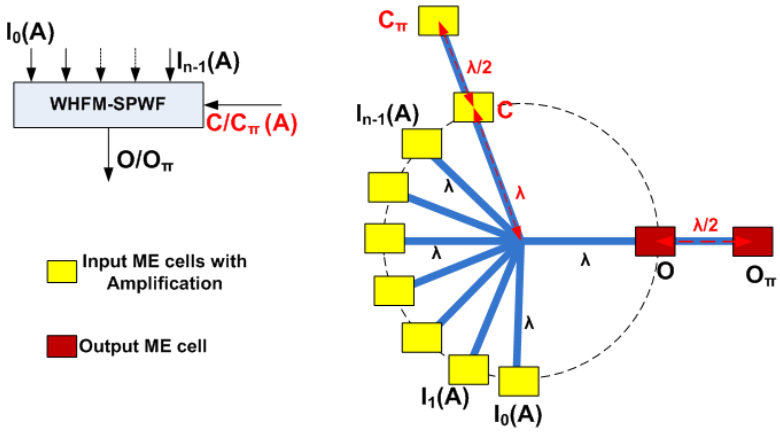


Figure 3.4. Block diagram and schematic representation using waveguides and ME cells for realizing Weighted High Fan-in Majority Function (WHFM) SPWF.

3.3.3 Frequency Modulated WHFM-SPWF (FM-WHFM-SPWF)

Fig. 3.5 shows the block diagram of a Frequency Modulated WHFM-SPWF. The general idea here is that multiple inputs of different frequencies can be simultaneously transmitted and evaluated over the ferromagnetic waveguide. Spin wave interference is frequency dependent and thus the information on individual spin waves can be preserved. Similarly by multiplexing the control input, we can realize a large number of sophisticated functions simultaneously.

3.4 Chapter Summary

In this chapter, we presented the concept of Spin Wave Functions which enable realization of sophisticated logic functions in a single step. Three types of SPWFs were also discussed.

In the past, there have been other proposals for realization of high majority gates. For example, based on capacitive threshold logic [35, 26, 37]. But, such a logic

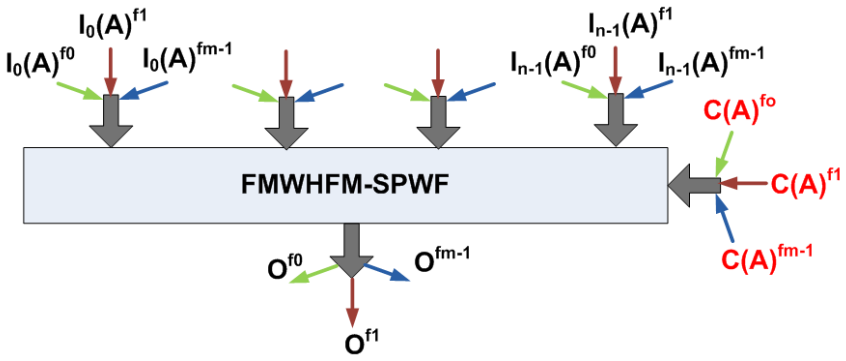


Figure 3.5. Block diagram of Frequency Modulated Weighted High Fan-in Majority Function (FMWHFM) device. Multiple inputs and control signals at different frequencies can be multiplexed over the same waveguide.

style has significant drawbacks due to difficulty in implementing accurate capacitors and its sensitivity to soft errors. Majority gates based on emerging technologies like Quantum-Dot Cellular Automata (QCA) and Magnetic Quantum-Dot Cellular Automata (MQCA) have also been shown [36, 39, 51, 18, 10]. In such technologies, the range of interactions is extremely limited, thereby leading to significant fan-in limitations.

On the contrary, wave superposition principle naturally enables efficient realization of high fan-in majority functions with significant reduction in logic complexity and overall gate count. The proposed SPWF approach provides several significant advantages that include:

- Enables compressed data representation and transmission
- Non-volatile operation which eliminates the need for separate latching circuits with significant reduction in static power dissipation
- Use of a Magneto-Electric element (ME) cell with electric field control of spin waves using novel materials (e.g. multiferroics) can be scaled down to the order of 40kT, minimizing dynamic power

- Preserves compatibility with CMOS with respect to fabrication and electronic-magnetic-electronic interface allowing for hybrid architectures

In subsequent chapters, WHFM-SPWF based logic design approaches are presented. The design of a SPWF based full adder is shown next and implications of following an integrated fabric-circuit exploration approach are discussed later.

CHAPTER 4

SPWF LOGIC DESIGN

4.1 Introduction: Possible Approaches

Generally, CMOS logic circuits are implemented using Boolean gates (e.g. AND/OR) based on SOP or POS realizations. In this approach, 2-input or 3-input standard gate libraries are constructed and larger circuits are built by cascading a large number of these elementary gates. However, it is well known that such a logic design approach, has two major drawbacks, i) exponential degradation in performance is observed for high fan-in, ii) Leads to inefficient implementation with large number of logic levels and gates.

Several alternate styles have been proposed to overcome the drawbacks of the conventional Boolean logic. One of the popular alternatives is based on threshold/majority logic. Threshold gates fundamentally realize more complex logic functions compared to conventional Boolean gates (AND, OR etc.); consequently, reducing the number of logic levels and the overall gate count required to realize a given circuit [50, 34, 6].

Equation 4.1 gives the general form of a threshold function (schematic is Fig. 4.1):

$$f(x_1, x_2, ..., x_n) = \begin{cases} 1 & if \ \sum_{i=1}^{n} x_i w_i \ \geq \ T \\ 0 & if \ \sum_{i=1}^{n} x_i w_i \ < \ T \end{cases} \tag{4.1}$$

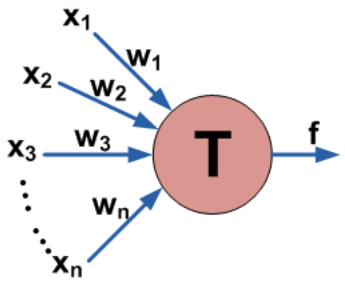


Figure 4.1. General symbol of a threshold function.

Where, 'T' is the threshold value, 'x_i' and 'w_i' represent the inputs and weights respectively. It can be observed that, if $w_i = 1$ for all 'i' and T = n/2, then the above function results in a ***Majority function***.

However, since the physical implementations (e.g. CMOS based) of the threshold gates are known to be highly complex, this logic style has had little impact on CMOS VLSI design. Moreover the fan-in for majority based implementations is generally limited to 3 or 4. Several algorithms have been proposed for designing high fan-in majority gates using 3-input majority gates [3, 28, 29]. This multi-level implementation further increases the implementation complexity. In this work, we illustrate this principle based on our analysis of a (7,3) parallel counter.

Parallel counters are digital circuits with 'n' inputs and '$log_2(n+1)$' output bits representing the number of 1's in the 'n' input bits set [44, 22]. Generally, parallel counters are used in the realization of fast parallel multipliers. Realization of parallel counters based on the principle of threshold logic, enables highly optimal circuits; with the implementation style being suitable for wave interference phenomenon.

Fig. 4.2 shows the layout of (7,3) parallel counter implemented using standard Boolean gates. The layout is implemented using 45nm NANGATE standard cell library and it uses approximately 100 transistors. P. Celinski et. al. have shown a threshold logic gate based implementation for (7,3) counter (see Fig. 4.3) [8]. It can

be clearly observed that the majority based implementation uses fewer gates than the corresponding Boolean gates based design (layout shown in Fig. 4.2).

However, Fig. 4.4 shows that MOSFET based implementation of the threshold logic gate is significantly complex. This significantly reduces the benefits expected due to fewer logic levels and gates.

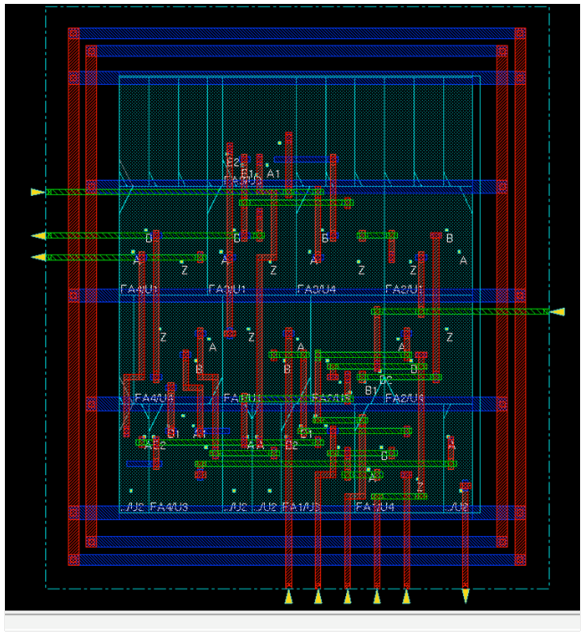
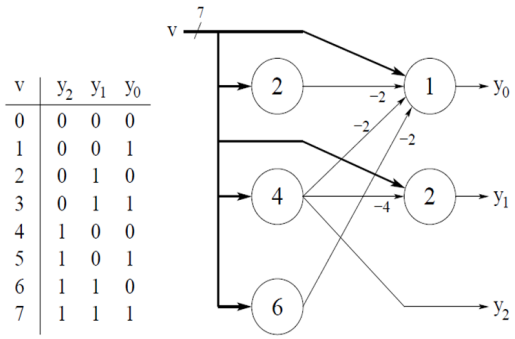


Figure 4.2. 45nm Standard Cell Library based CMOS Layout for (7,3) Counter.

On the contrary, SPWFs leverage on the wave interference phenomenon and thus no special gate/component is required to realize the majority function. Fig. 4.5 shows the SPWF based implementation of (7,3) parallel counter with only 13 ME cells. The principle of wave interference and compressed data representation are the primary factors for such complexity reduction.

4.2 1-Bit SPWF Full Adder

Fig. 4.6 shows the layout of a full adder implemented using WHFM-SPWFs. The three inputs (A,B,C_{in}) are assumed to be available in electrical domain and input



V	y_2	y_1	y_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Figure 4.3. (7,3) Parallel Counter design using threshold logic gates. Only five threshold gates are used, but individual gates are highly complex[8].

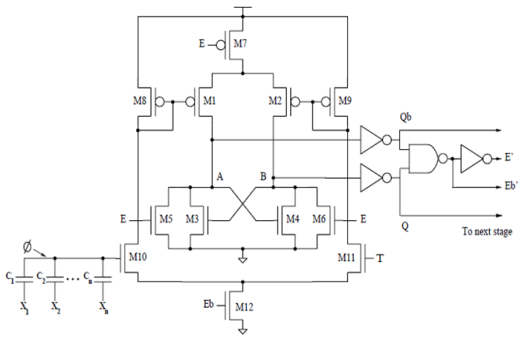


Figure 4.4. MOSFET based threshold logic gate implementation [8].

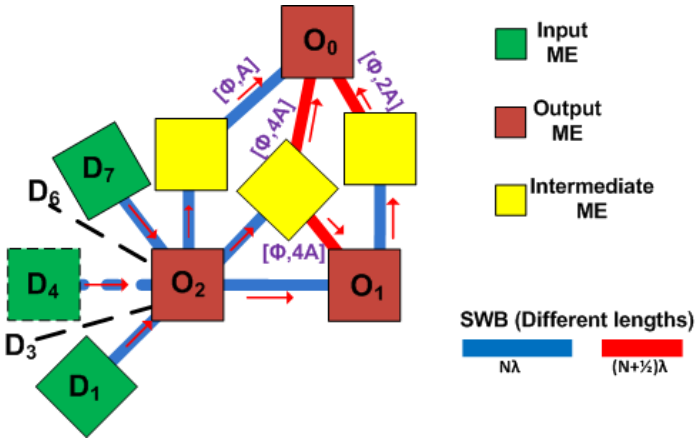


Figure 4.5. SWPF based (7,3) parallel counter layout.

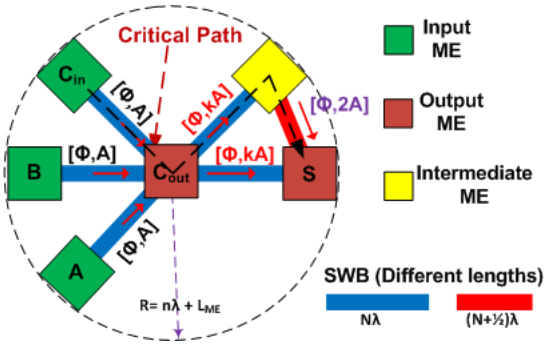


Figure 4.6. Weighted majority SPWF based 1-bit full adder layout.

ME cells are used to generate corresponding spin waves. Output ME cells (for C_{out} and SUM) are used to capture the logic information in the resultant spin waves and convert it back to electrical domain. Since WHFM-SPWFs encode information both in phase and amplitude, a highly efficient layout is expected.

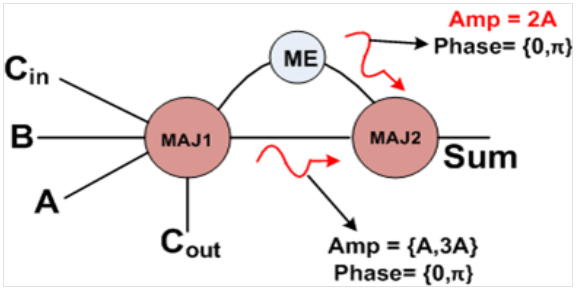


Figure 4.7. Schematic diagram of WHFM-SPWF based full adder design. Compressed information transmission is used between MAJ1 and MAJ2.

An important benefit of using the WHFM-SPWF approach is that it enables ***Compressed Data Representation***. This is illustrated in the schematic shown in Fig. 4.7, where the spin wave travelling from the 'C_{out}' ME cell to the SUM ME cell represents the number of logic '1's input spin waves in a compressed manner. We expect even higher benefits for large designs where information can be transmitted across the fabric in a compressed form.

4.3 Chapter Summary

Different approaches for logic design were discussed in this chapter. The (7,3) parallel counter example illustrated that majority gates are more efficient in logic mapping than conventional Boolean logic. However, MOSFET based majority/threshold gate implementations are highly complex, often negating the benefits due to reduced gate count. SPWFs leverage on wave interference phenomenon and thus no special gate/component is required to realize the majority function. Highly efficient layouts for a (7,3) counter and 1-bit full adder were also discussed. Detailed comparisons of SPWF layout vs. 45nm custom CMOS implementation for the 1-bit full adder are presented in section 5.3.4.

CHAPTER 5

INTEGRATED FABRIC CIRCUIT EXPLORATION

Historically, the first step in a new computational paradigm is the development of efficient devices. Circuit designers and architects then use these devices to build bigger systems. We argue that for development of breakthrough post-CMOS nanofabrics, an integrated fabric-circuit exploration is necessary. Our efforts towards developing new architectures using magnonic logic places strong emphasis on integrated exploration across multiple design levels aimed at solving problems from a particular fabric perspective. This work also shows how design topology may drive ME cell structure/characteristics and vice versa.

Two type of ME cells are discussed; one with **Amplitude Tracing** (AT) capabilities and other without Amplitude Tracing capabilities. Dual-rail logic based inversion-free designs are also presented showing how circuit styles can impact the manufacturing and physical fabric related constraints. In addition, trade-offs have been analysed with relevant comparisons with 45nm custom CMOS adder implementations.

5.1 Adder Designs with/without Amplitude Tracing ME Cells

Amplitude Tracing refers to the ability of the ME cells to re-generate new spin waves with variable/dynamic amplitudes depending on the amplitude of the incoming spin waves. Amplification of spin waves and its dependence on the total field (H_{eff}) is shown in Fig. 5.1. Fig. 5.1.a shows that with increase in angle of rotation of easy axis, the amplitude of output spin waves increases. However, it can clearly be seen in Fig.

5.1.b that the output wave amplitude quickly saturates to M_z, thereby the output spin wave may not be able to trace the entire amplitude range of incoming spin wave. This would imply that only a small range of spin wave amplitudes would be allowed for information encoding. Thus, additional explorations on ME cell structure and materials may be required to support the amplitude tracing feature. In this section, we show the design of 1-bit/2-bit adders without using Amplitude Tracing ME cells.

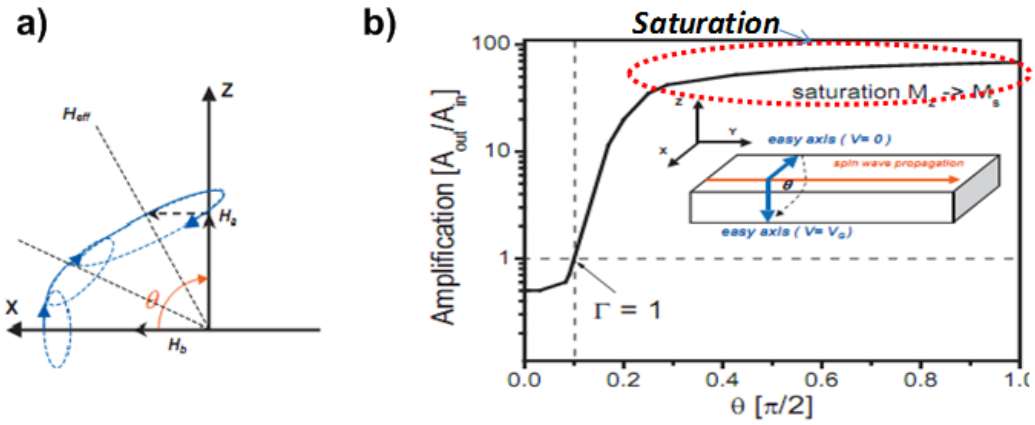


Figure 5.1. Amplitude saturation in ME cells [21]. a) Illustration of amplification process. Increased precession (blue curve) with higher degree of rotation of easy axis. b) Plot showing spin wave amplification as a function of angle of rotation of easy axis. It shows that the output wave amplitude quickly saturates to M_z.

One of the primary constraints for the design shown in Fig. 5.2.a is that it requires re-generation of spin waves with variable/dynamic amplitudes. For example, in Fig. 5.2.a amplitude of the wave from the Cout ME cell to the Intermediate ME and the SUM ME will be dynamic based on the interference of the three inputs waves. This may require additional feedback mechanism in the ME cells to trace both phase and amplitude of incoming waves. The ME cell structure discussed in section 2.2, is phase-only ME cell without any amplitude tracing capabilities. In contrast, the design in 5.2.b and Fig. 5.2.c does not have this requirement of Amplitude Tracing. After superposition, the resultant waves with additional information encoded in the

amplitude are preserved for further computation. Thereby, all ME cells generate waves of fixed amplitude. This can significantly reduce the complexity of ME cells.

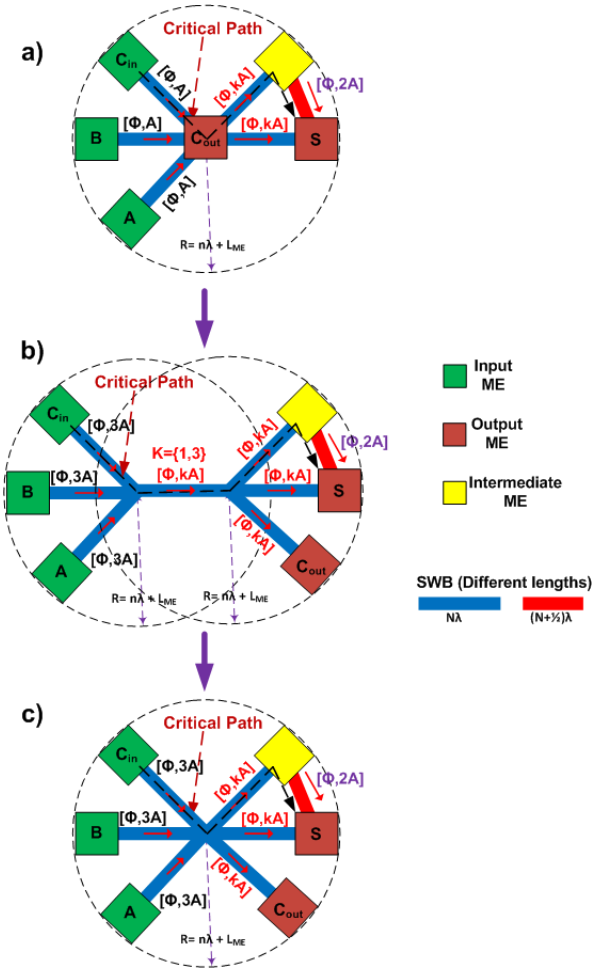


Figure 5.2. 1-bit SPWF adder design without Amplitude Tracing MEs. a) Basic 1-bit SPWF adder that requires *Amplitude Tracing* ME cells. b) Intermediate design showing circuit topology changes that enable realization of 1-bit adder without Amplitude Tracing MEs. c) Final 1-bit adder layout without Amplitude Tracing MEs (more compact).

Fig. 5.3.a shows the realization of 2-bit ripple adder using two (3;2) parallel counters. Both designs, with and without Amplitude Tracing MEs are shown. Note that the second design (Fig. 5.3.c) uses the same number of ME cells as the first design (Fig. 5.3.b). However there is only a slight penalty in area for the second

design which is acceptable given the fact that it significantly relaxes the constraints on ME cell design. Another benefit of the second design is that it reduces the number of ME cells on the critical path. Only 4 ME cells are on the critical path for the Amplitude Tracing Free design, while the Amplitude Tracing design has 5 ME cells. A detailed comparison of the adder designs and projected benefits vs. CMOS is presented in section 5.3.4.

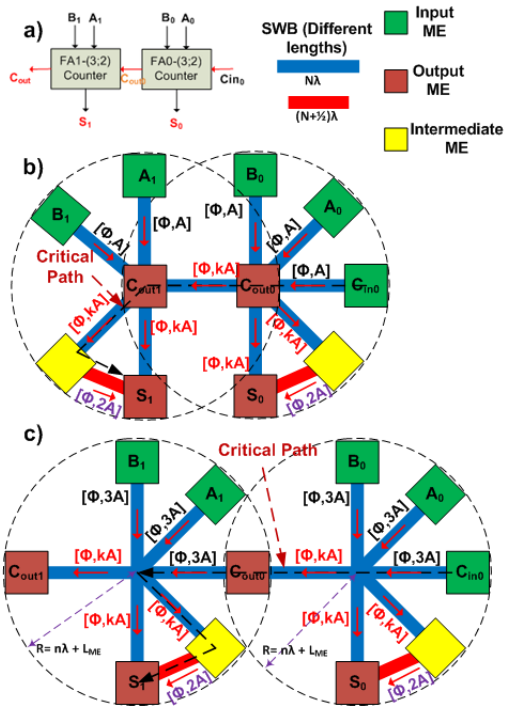


Figure 5.3. 2-bit SPWF adders with/without Amplitude Tracing MEs. a) Block diagram of 2-bit ripple adder. b) SPWF implementation of 2-bit adder with Amplitude Tracing MEs. c) SPWF implementation of 2-bit adder without Amplitude Tracing MEs.

5.2 Inversion-Free Full Adder Design

The designs shown in Figures 5.2 and 5.3, require realization of odd phase shifts for the wave propagating from the 'Intermediate' ME cells to 'SUM' ME cells. This

may enforce more stringent waveguide patterning requirements to achieve accurate phase shifts, and may also affect spin wave propagation velocity.

Fig. 5.4 shows a SPWF 2-bit adder layout based on dual-rail principle that eliminates the need to have any intermediate inversion in the design. Thereby, relative to the designs shown in Figures 5.2 and 5.3, this design has more relaxed patterning constraints. A key observation here is that, in a ripple adder circuit only the carry signals are propagated across different bits, thus duals of only the 'carry-out' signals are needed. This would help in reducing the area and power consumption overhead associated with dual-rail designs. Fig. 5.5 shows the inversion free design without the use of Amplitude Tracing ME cells. Similar to the Amplitude Tracing Free designs shown previously, this design has fewer ME cells on the critical path.

Dual-rail SPWF designs also enable implicit mechanisms for ***completion detection***. This is based on 1-hot encoding of each signal on two separate waveguides. This feature is used in the design of asynchronous circuits discussed in Chapter 6.

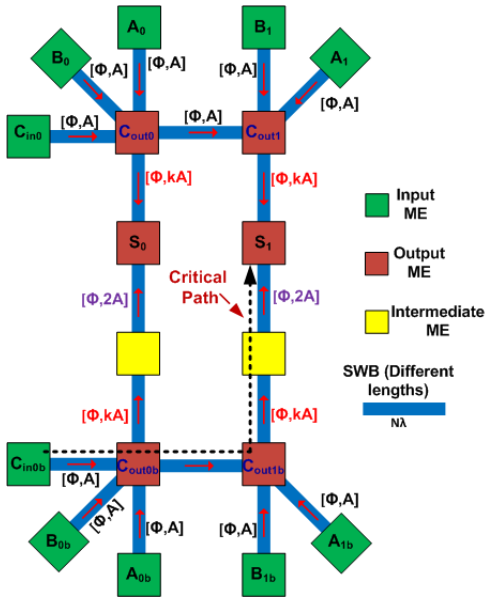


Figure 5.4. Inversion free 2-bit SPWF adders with Amplitude Tracing MEs. The length of all waveguides are integral multiples of spin wave length. This topology does not require any intermediate inversion of spin waves.

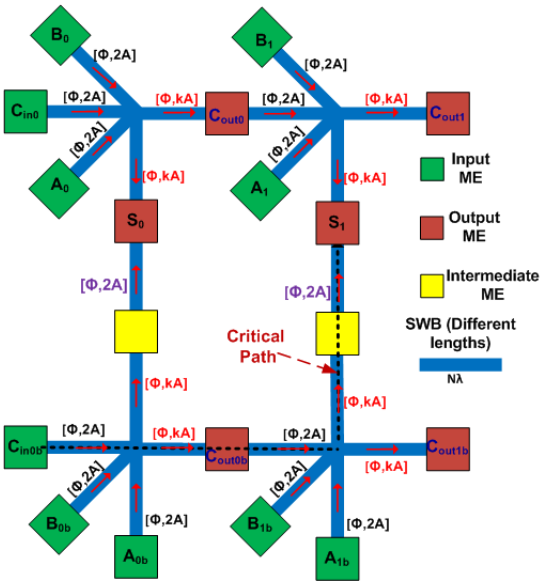


Figure 5.5. Inversion free 2-bit SPWF adders **without** Amplitude Tracing MEs. The length of all waveguides are integral multiples of spin wave length. All the ME cells generate waves of fixed amplitude. This topology does not require any intermediate inversion of spin waves.

5.3 Projected Benefits vs. 45nm CMOS

In this section, we present our initial evaluations of the proposed adder designs vs. equivalent 45nm CMOS designs. The assumptions used for these evaluations are also presented along with the evaluation methodology. Table 5.1 and Table 5.2 show the power, delay and complexity comparisons for both the 1-bit and 2-bit adders. Projected benefits vs. CMOS are shown for all design styles; Amplitude Tracing (AT), W/O Amplitude Tracing (W/O AT) and the Inversion Free (IF) designs. Table 5.1 and Table 5.2 also show how the SPWF designs would compare with the corresponding CMOS designs without the presence of I/O ME cells. This type of evaluation would enable us to estimate the benefits of internal SPWFs whose inputs are not the direct primary inputs. In this case, we assume that the inputs are directly available as input spin waves without any I/O ME cells.

5.3.1 Fabric Assumptions

In this section, the fabric parameters and assumptions are presented. For SPWF design evaluation, ME cell dimension of 100nm*100nm with a switching delay of 100ps is used. Spin wave length (λ) is assumed to be 100nm and group velocity of spin waves in the proposed Spin Wave Bus (SWB) is assumed to be 10^4m/s [20]. The switching energy and power consumption of ME cells and the methodology for estimating SPWF circuit power is shown in the next section. All the CMOS design (Fig. 5.7) evaluations were done on a custom 45nm CMOS design (using NCSU 45nm PDK) based on Hspice simulations.

5.3.2 Energy Estimates for SPWF Circuits

In this section, we provide our estimates on energy consumption in SPWF circuits. It should be noted that spin wave propagation does not involve any physical movement of charge particles. Thereby, energy consumption is mainly attributed to ME cell switching for generating new waves, amplification and latching. The total energy of a SPWF circuit is calculated based on the number of ME cells (N_{ME}) and the energy consumption per ME cell (E_{ME}):

$$E = N_{ME} \times E_{ME} \tag{5.1}$$

Voltage controlled magnetization rotation is an important step towards achieving low power ME cells. The ME cell structure represents a parallel plate capacitor consisting of a non-magnetic metallic layer (e.g. Al), a layer of piezoelectric material (e.g. PZT), and a conducting magnetostrictive material (e.g. Ni). As a conservative estimate, the total energy consumed by ME cell per switch can be calculated as follows:

$$E_{ME} = \frac{CV^2}{2} = \frac{\epsilon_0 \epsilon_r A V_{\pi/2}^2}{2d} \tag{5.2}$$

Where 'ϵ_0' is the vacuum permittivity, 'ϵ_r' is the relative permittivity of the piezoelectric, 'A' is the surface area of the ME cell, 'd' is the thickness of the dielectric layer, '$V_{\pi/2}$' is the voltage required for 90 degree magnetization rotation. In order to provide high-frequency spin wave excitation, the thickness of the piezoelectric layer should be adjusted to the spin wave frequency (e.g. $d = 0.8\mu m$ for resonance frequency of 1GHz). Taking the following data: $\epsilon_0 = 8.854 \times 10^{-12} F/m$, $\epsilon_r = 1700$ for PZT, $A = 100nm * 100nm$, $d = 0.8\mu m$, $V_{\pi/2} = 1MV/m \times 0.8\mu m = 0.8V$, we would require approximately 60aJ of energy for ME cell switching.

The energy per switch scales proportional to the size of the ME cell and can be reduced by optimizing the material structure and switching dynamics. It is also possible to reduce the switching energy by decreasing the applied voltage (e.g. accomplish switching with less than 90 degree easy-axis rotation). ME cell is magnetically coupled with spin wave bus within the circuit. It may be possible to exploit the interplay between the magnetic field of the ME cell (e.g. shape anisotropy) and the magnetic field of the spin wave bus (exchange coupling) to reduce the switching angle.

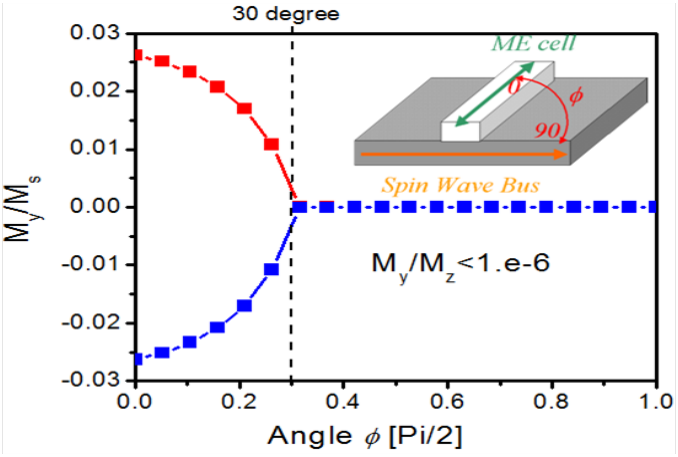


Figure 5.6. Numerical simulations illustrating the magnetization states (M_y) of the ME cell as a result of the interplay between the shape anisotropy field of the ME cell and exchange coupling with the spin wave bus [41]. ME cell switching by spin wave is possible at easy axis rotation by 30 degrees.

Fig. 5.6 shows micro-magnetic simulations on ME cell switching [41]. It can be observed that, ME switching is possible with magnetization rotation of about only 30 degrees[1]. This would reduce the switching electric field from 1 MV/m to about 0.4 MV/m, $V_{\pi/6} = 0.4MV/m0.8um = 0.32V$, resulting in the energy per ME cell as low as 10aJ. We use this to estimate the projected benefits of SPWF designs vs. CMOS.

5.3.3 Evaluation Methodology

The delay calculation for both the SPWF and the CMOS designs is determined by the amount of logic and interconnect along the critical path. For a 2-bit adder, the critical path is from the Cin_0 to S_1. SPWF design delay is determined by the number of ME cells and length on the SWB encountered along the critical path. For example, for the design shown in Fig. 5.3c, there are 4 ME cells along the critical path and the delay is approximately 535ps including the delay on the SWB. The worst case transition delay for the CMOS design is determined using Hspice simulations on the spice netlist extracted from the layout shown in Fig. 5.7.

Power consumption for the SPWF designs in mainly associated with the ME cell switching. The overall power consumption is estimated based on the number of ME cells in the design. The power consumption for the 45nm CMOS layout is calculated based on Hspice simulations. The average power over 40 trials with 1000 random transitions in each is reported here. Area for both the SPWF and CMOS designs are calculated directly from the layouts of the adder designs.

5.3.4 Discussion on Projected Benefits vs. CMOS

Table 5.1 and Table 5.2 show the overall comparison results. As expected, these results show that SPWF designs are highly power efficient. Table 5.1 shows an estimated power reduction of approximately 228X for the 1-bit regular SPWF w/o AT

[1]This is based on numerical simulations by Dr. Alexander Khitun from University of California, Riverside, California

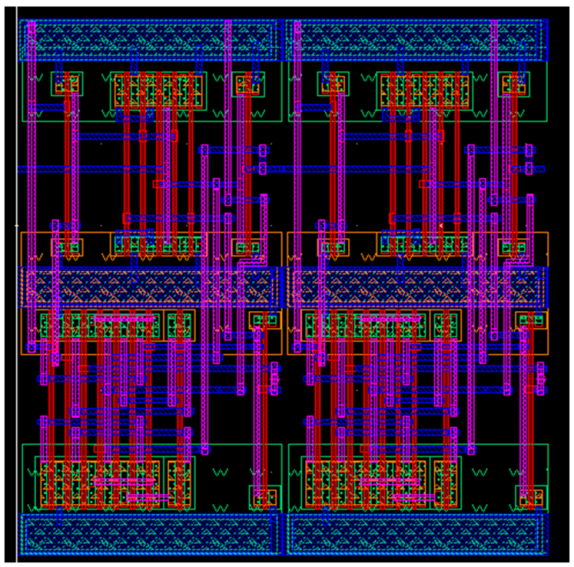


Figure 5.7. NCSU 45nm PDK based 2-bit CMOS adder layout.

adder design. For the 2-bit SPWF version, a reduction of up to 222X is expected (Table 5.2). This huge reduction in power consumption is also attributed to the significant reduction in overall design complexity of the SPWF designs. The CMOS design requires up to 64 transistors for the 2-bit adder, while the SPWF design needs only 11 ME cells for the regular Amplitude Tracing Free designs (Fig. 5.3.c). These results are encouraging and show that SPWFs logic is one of the promising options for post-CMOS chip designs.

Table 5.1. Projected Comparisons: SPWF 1-BIT Adder vs. NCSU PDK based 45nm Custom CMOS Layout.

Fabric	**Design**	**Delay**	**Power**	**Complexity**
CMOS	Custom	250ps	$36.5\mu W$	$Area = 20\mu m^2$ Transistor Count = 32
SPWF with I/O ME	With AT	475ps	$0.12\mu W$	$Area = \pi * (4\lambda)^2 = 0.5\mu m^2$
	W/O AT	375ps	$0.16\mu W$	ME Count = 6
SPWF without I/O ME	With AT	275ps	$0.08\mu W$	$Area = \pi * (3\lambda)^2 = 0.28\mu m^2$ ME Count = 2
	W/O AT	175ps	$0.06\mu W$	$Area = \pi * (3\lambda)^2 = 0.28\mu m^2$ ME Count = 1

Table 5.1 and Table 5.2 show that the overall delays of the SPWF and CMOS design are comparable. While the results presented in [40], show a large performance benefit for high fan-in logic functions (with inherent parallelism in the operations), these results show that small designs with bit-wise dependencies may not benefit in terms of performance with the SPWF implementations without further improvement on ME cell delay.

Significant area benefits can also be expected for SPWF designs. For a regular w/o AT 1-bit SPWF adder, an area reduction of up to 40x may be possible (Table 5.1). Table 5.2 shows that for a 2-bit SPWF adder, up to 33x area reduction can be expected. As mentioned earlier, these benefits are mainly due two factors; i) due to compressed data representation in SPWFs, and ii) due to the highly efficient/simple majority logic realization using spin wave interference.

Table 5.2. Projected Comparisons: SPWF 2-BIT Adder Comparison vs. NCSU PDK based 45nm Custom CMOS Layout.

Fabric	**Design**	**Delay**	**Power**	**Complexity**
CMOS	Custom	400ps	$44.5\mu W$	$Area = 40\mu m^2$ Transistor Count = 64
SPWF with I/O ME	With AT	605ps	$0.18\mu W$	$Area = 12\lambda * 8\lambda = 0.96\mu m^2$ ME Count = 11
	W/O AT	535ps	$0.2\mu W$	$Area = 15\lambda * 8\lambda = 1.20\mu m^2$ ME Count = 11
	IF-AT	600ps	$0.3\mu W$	$Area = 12\lambda * 17\lambda = 2.04\mu m^2$ ME Count = 18
	IF-W/O AT	530ps	$0.34\mu W$	$Area = 15\lambda * 17\lambda = 2.55\mu m^2$ ME Count = 18
SPWF without I/O ME	With AT	375ps	$0.1\mu W$	$Area = 6\lambda * 9\lambda = 0.54\mu m^2$ ME Count = 4
	W/O AT	295ps	$0.1\mu W$	$Area = 11\lambda * 6\lambda = 0.66\mu m^2$ ME Count = 3
	IF-AT	370ps	$0.15\mu W$	$Area = 9\lambda * 13\lambda = 1.17\mu m^2$ ME Count = 6
	IF-W/O AT	290ps	$0.1\mu W$	$Area = 11\lambda * 13\lambda = 1.43\mu m^2$ ME Count = 4

Our evaluation also shows that, SPWF design may even have larger benefits when all the inputs are directly available as incoming spin waves (without any I/O ME cells). We can expect up to 300x reduction in overall power consumption, up to 60x area benefit for the 2-bit regular w/o AT adder design (Table 5.2). Similar benefits are also seen for the 1-bit adder design as shown in Table 5.1. Due to reduction in the number of ME cells on the critical path and reduction of SPWF area, a delay reduction of up to 25% can also be expected for these internal SPWF based circuits.

5.4 Chapter Summary

Our explorations on integrated SPWF fabric-circuit development were discussed based on the Amplitude Tracing and without Amplitude Tracing designs. Alternate circuit styles and waveguide topologies enable realization of inversion-free designs with relaxed waveguide patterning constraints. Detailed comparisons in terms of area, power and performance vs. 45nm CMOS adder design were also presented. Our estimates show that, for a 1-bit adder, 40x reduction in area and 228x reduction in power may be possible with the spin wave based implementation. For the 2-bit adder, results show that 33x area reduction and 222x reductions in power may be possible. SPWF based data streaming approaches for building large scale designs is discussed in the next paper.

However, performance comparisons show that SPWF designs may not compare favourably vs. CMOS. This is mainly due to lower spin wave group velocity compared to charge propagation speeds.

CHAPTER 6

ASYNCHRONOUS SPIN WAVE FUNCTIONS

6.1 Overview of Asynchronous Circuits

In the previous chapters, the basic concept of SPWFs, logic design examples and our integrated fabric circuit explorations were presented. Building large scale SPWF-based circuits would need mechanisms for data synchronization and data streaming. Currently, CMOS digital design is primarily focused on synchronous architectures. However, designing circuits with synchronous approach, with one or more global clocks, leads to large amount of power consumption and performance of circuits will be mainly limited by the worst case behaviour. Moreover, synchronous designs are more susceptible to timing faults due to variability.

In contrast, asynchronous designs do not use global clocks for synchronization and streaming [33, 32, 42, 49]. The basic concept of synchronous vs. asynchronous pipelines is shown in Fig. 6.1. In the asynchronous approach, communication is based on completion detection and local handshaking between neighbouring blocks. Asynchronous designs leverage on the fact that computation delay in circuits is based on the input data operands. This allows for average case pipeline performance vs. worst case. Local handshaking also eliminates the problems (e.g. skew) and reduces the overheads associated with clock distribution (e.g power consumption, buffer insertion etc). Asynchronous circuits have also been shown to be less vulnerable to timing faults and have greater resilience to variability [42]. In addition, signal transitions occur only during computation leading to fewer glitches and thereby enable significant reduction in power consumption.

Moreover, synchronous approach for SPWFs would require careful layout balancing and special type of ME cells with 'instant-on' behaviour. It should be noted that, in SPWF designs waveguide length affects both computational delay and also functionality. Thereby, synchronous SPWF designs would require careful layout balancing. This chapter presents our initial explorations on data streaming approaches using asynchronous SPWFs (A-SPWFs). Detailed description of various components and mechanisms involved in A-SPWF based pipeline design is provided. As an example, a 32-bit Carry Completion Sensing Adder (CCSA) is designed using A-SPWFs and preliminary evaluations are shown in this section.

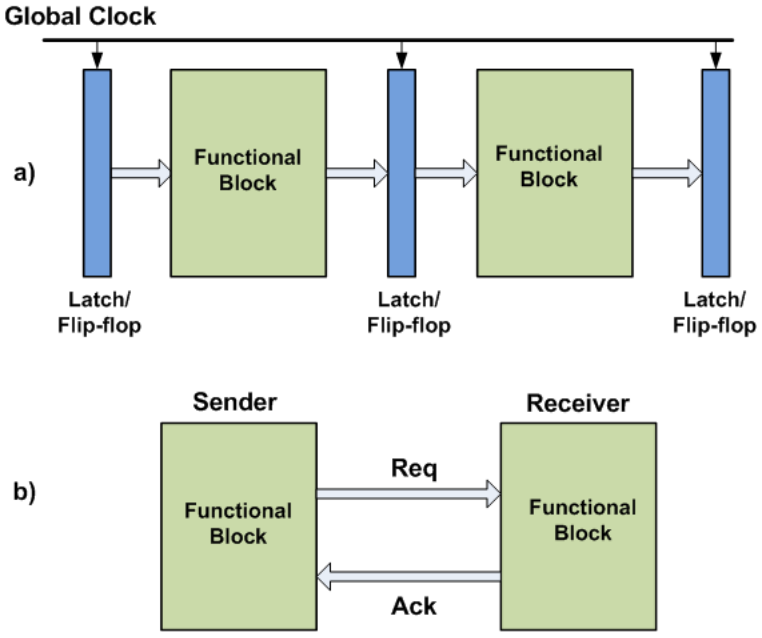


Figure 6.1. Generic pipeline block diagrams. a) Synchronous b) Asynchronous

6.2 Components and Mechanisms for A-SPWF Designs

Asynchronous circuits work based on local handshaking between computing blocks. In contrast with synchronous circuits, where data on a given wire is 'VALID' after a certain fixed time, asynchronous designs have arbitrary delays to obtaining 'VALID'

data bits. This is primarily due to the data-dependent computational delay of asynchronous logic blocks. Thereby, asynchronous designs require additional design components and mechanisms for a) detecting completion of a given computation - Completion detection, b) Handshaking between sender and receiver. Thereby, in addition to computing the actual data values, computing blocks also need to communicate information about validity of signals. Several handshaking protocols e.g. 4-phase dual rail, 2-phase dual rail, bundled data protocols etc. have been proposed in the literature [46]. Compared to the 2-phase protocol, 4-phase dual rail protocol is simple for physical realization. Thereby all the A-SPWF designs explored in this thesis are based on the 4-phase protocol. Table 6.1 shows the 4-phase encoding scheme.

Table 6.1. 4-phase handshaking protocol.

$Data_0$	$Data_1$	Signal
0	0	Reset
0	1	0
1	0	1
1	1	Invalid

In addition to signal encoding schemes shown above, the concept of acknowledgement is very important in asynchronous circuit design. In synchronous circuits, global clock plays the role of establishing the time at which valid data is available at the input of a pipeline stage and also the availability of successive stage to accept new data. In case of asynchronous pipelines, the C-element (also called as Muller C-element [33, 32]) is used for establishing control across different pipeline stages. The truth table for C-element operation is shown in Table 6.2. A simple SPWF layout of a 2-input C-element is shown in Fig. 6.2.

Completion detection in the proposed A-SPWF circuits is based on the above dual-rail encoding scheme. In order to distinguish successive valid data signals, a *'Reset Spacer'* is inserted after every computation. Thereby, when one of the wires

Table 6.2. Truth Table for 2-input C-element.

A(reqi-1)	B(acki+1)	Ci(reqi/acki)
0	0	0
0	1	C_{i-1}
1	0	C_{i-1}
1	1	1

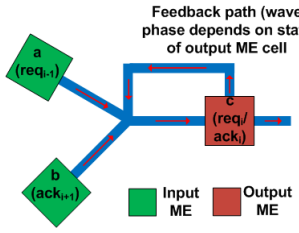


Figure 6.2. SPWF C-element Implementation.

goes to state '1' after a reset, a simple OR gate can used for completion detection. Efficient majority logic based completion detection is also shown in section 6.4.

6.3 A-SPWF Pipelines

Generic SPWF based pipeline designs using the concept of dual rail logic and C-elements is discussed in this section. Each pipeline stage consist of a logic block implemented using dual rail logic. Input and output ME cells are controlled based on the C-elements corresponding to that stage. This section shows how pipeline structures can be different based on the choice of reset mechanism.

6.3.1 Electrical RESET based on feedback

Fig. 6.3 shows the overall pipeline diagram with 'reset' based on voltage control of output ME cells. Here, the output of C-element is converted back to charge domain and this voltage is used to reset ME cells. Since, the 'reset' involves spin-charge-spin conversion, this approach requires more detailed description of how ME cells function

to a) latch incoming wave, b) generate new waves, c) generate output electrical pulses and d) reset.

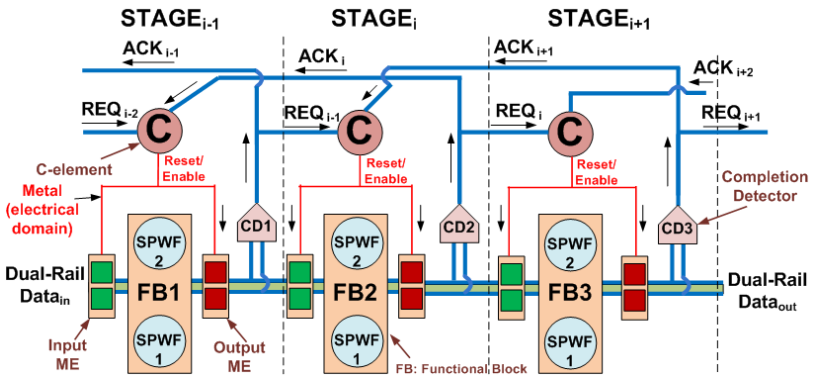


Figure 6.3. A-SPWF Pipeline with electrical signal based RESET. Here, the output from C-elements is converted back to electrical domain. This feedback signal (red color) is used to reset output ME cells after each computation.

6.3.2 RESET inserted as DATA

In this approach (shown in Fig. 6.4), input data to the pipeline is modified to include 'reset' data inputs. These 'reset' inputs would progress through the pipeline similar to actual valid data. One of the main advantages of such a pipeline scheme is that it does not involve any intermediate spin-charge-spin conversions. Thus, we expect this approach to be relatively simple for physical implementation using spin wave guides and ME cells. However, in this scheme 'reset' delay is comparable to the delay for actual data inputs. This may lead to increase in pipeline latency and reduced throughput.

6.4 Carry Completion Sensing Adder

Completion detection in the proposed asynchronous designs is based on dual-rail logic and OR gate to indicate when a new result is available. Dual rail logic results in a large implementation overhead due to duplication of logic blocks. However,

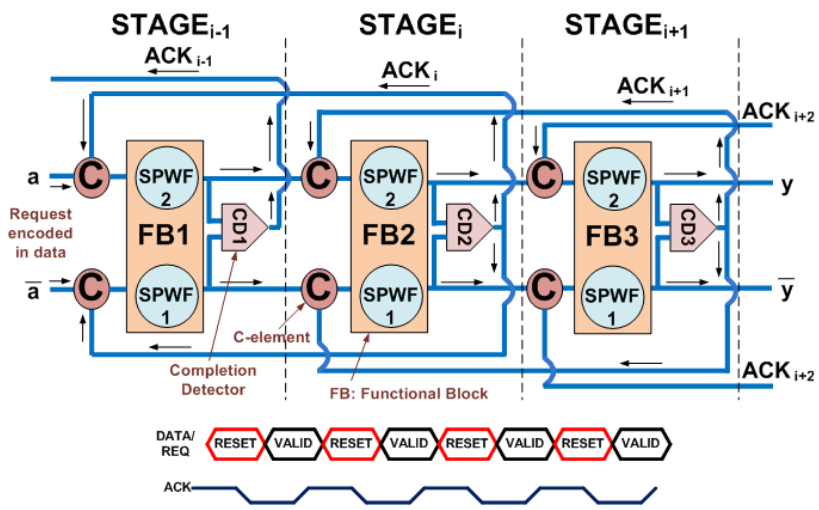


Figure 6.4. A-SPWF Pipeline with RESET spacers inserted as DATA at input of pipelines. Here RESET signals are same as data inputs which RESET output ME cells. This approach implements relatively simple RESET mechanism for SPWF pipelines.

for completion detection, it is sufficient to use dual rail logic only on critical path. Here, we have shown one such example using the Carry Completion Sensing Adders (CCSA) which uses dual-rail only along the carry chain, thereby significantly reducing the overhead of dual-rail implementation. CCSA is based on the principle that for certain inputs (00 and 11), outgoing carry generation is independent of the incoming carry [16, 7]. This feature, in conjunction with a completion detection mechanism, allows the overall carry chain (LSB to MSB) to be broken into smaller independent chains that operate in parallel leading to considerable speed-up. The general principle of operation is illustrated in Fig. 6.5.

Fig. 6.5.a shows the block diagram of a ripple carry adder, where irrespective of the input operands, worst case carry chain delay determines adder performance. In comparison, Fig. 6.5.b shows an example where carry inputs at certain bit positions are available in parallel based on the input operands at these positions. Thereby,

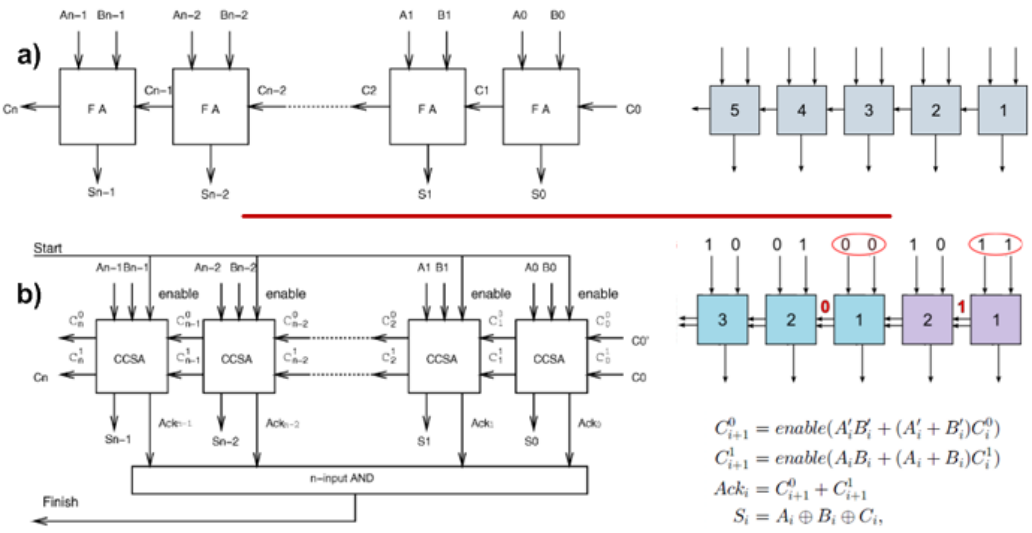


Figure 6.5. General principle of operation in CCSA. a) Shows a generic ripple carry adder where worst case carry chain delay determines the adder performance. b) CCSA block diagram with an example illustrating the operating principle. The actual LSB to MSB carry chain is broken into two smaller carry chains that operate in parallel. CCSA benefits from this feature by using a completion detection block.

the original carry chain is now broken into smaller chains that operate in parallel. A completion detection block is used to indicate completion of a particular addition.

Fig. 6.6.a shows A-SPWF layout design of a 4-bit CCSA. It can be observed that, dual rail logic is used only along the carry chain. Since SPWFs are highly efficient in majority logic realization, we have used direct majority logic based completion detection (Fig. 6.6.b). Thereby, even higher benefits can be expected with the proposed layout.

6.4.1 Preliminary evaluation of 32-bit A-SPWF CCSA

Fig. 6.7.a shows the 4-stage A-SPWF 32-bit CCSA design. Each stage consists of 8-bit CCSA units with an internal completion detection circuit. Communication between individual pipeline stages is enabled by C-elements based on local handshaking. Fig. 6.7.b shows the pipeline phases, where each row corresponds to a time snapshot

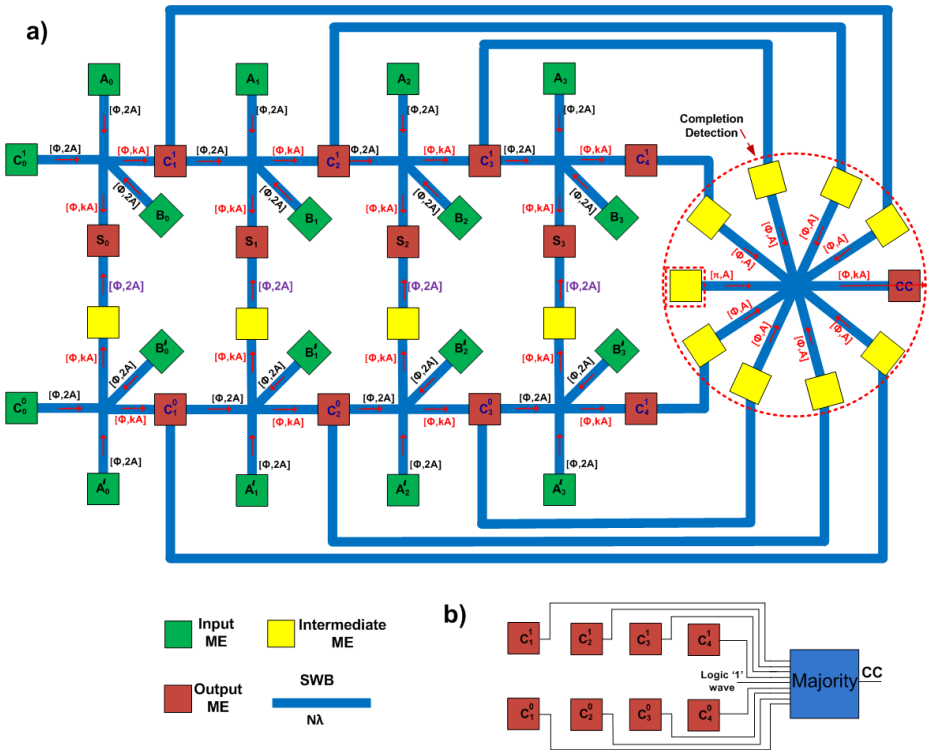


Figure 6.6. a)A-SPWF based 4-bit CCSA layout. Dual rail logic is used only along carry chain path and majority logic is used for completion detection. b)Schematic of completion detection block.

of the 4 stages. It can be observed that, each stage *resets* after every computation and *holds* the state till the successive stage completes its computation.

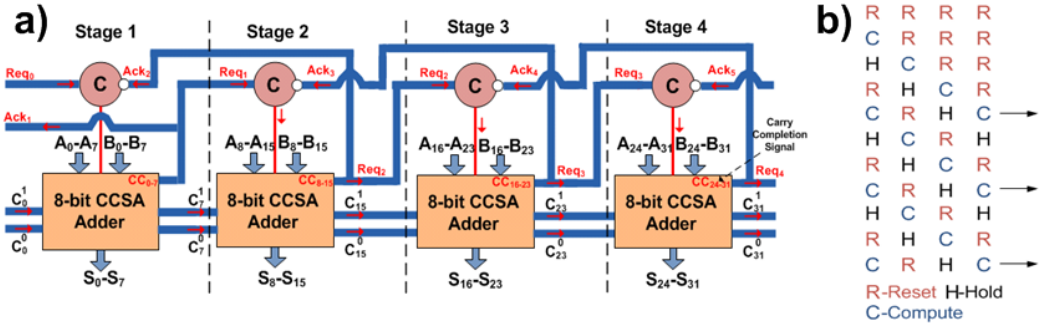


Figure 6.7. a) 32-bit A-SPWF block diagram. b) Pipeline phases of individual stages in the 4-stage A-SPWF 32-bit CCSA.

In our design evaluations, ME cell dimension of 100nm*100nm and 10aJ of energy/switching is assumed with a switching delay of 100ps. Wavelength (λ) is assumed to be 100nm with a group velocity of $10^4 m/s$.

In asynchronous designs computation delay is variable and dependent on several factors like input operands and number of active data tokens in pipeline. Thereby, performance evaluation is one of the key challenges for asynchronous circuits. For CCSA, performance calculation is based on the average case carry chain length. A generic analytical expression ($log_2(5n/4)$, where 'n' is the CCSA bit-width) was proposed by Hendrickson [17] for calculating average carry chain length in CCSAs. Performance evaluations in this work are based on this analytical expression.

In conjunction to evaluating the core CCSA logic, we have also considered overheads due to C-elements and completion detection circuit. Table 6.3 shows the area, power and performance overheads due to C-elements and completion detection circuit. It should be noted that detailed description of how ME cells function to a) latch incoming wave, b) generate new waves, c) generate output electrical pulses, and d) reset, is necessary to further validate these designs and their benefits.

Table 6.3. C-element and Completion Detector overhead.

	C-element	**Completion Detector**
$Area(\mu m^2)$	0.13	0.5
$Power(\mu W)$	0.2	0.7
$Delay(ps)$	200	260

Area, power and performance evaluations for 32-bit SPWF-based CCSA are shown in Table 6.4. For comparison, preliminary evaluations of a synchronous SPWF ripple carry based 32-bit adder are also shown in Table 6.4. It should be noted that the evaluations for the synchronous ripple carry adder are based on the assumption of availability of SPWF based inter-stage latches with 'instant-on' capability. It is expected that these latches and also the overhead due to layout balancing would result in additional area, power and delay for the synchronous designs. For a 4-sate pipeline, our current evaluations show that the synchronous version may compare favourably vs. the A-SPWF design. However, we expect to get larger benefits with the A-SPWF approach as the pipeline depth is increased and with higher bit-width. Designing a A-SPWF based CCSA with variable stage widths may provide additional benefits vs. synchronous designs. These trade-offs and other design alternatives could be explored as future extensions of the proposed A-SPWF CCSAs.

Table 6.4. Preliminary evaluations of 32-bit A-SPWF CCSA and 32-bit synchronous SPWF adder.

	A-SPWF	**Sync-SPWF**
$Area(\mu m^2)$	24	17.5
$Power(\mu W)$	1	0.4
$Latency(ns)$	6 (Avg. case)	4.8 (Worst case)
$Period(ns)$	4.5 (Avg. case)	1.2 (Worst case)

6.5 Chapter Summary

Compared to the clocked designs, asynchronous approach provides several benefits such as i) eliminates the clock distribution related issues (no global clocks) ii) provides average case performance vs. worst case iii) is inherently resilient to timing faults due to local variations. Moreover, a clocked approach would require an '*instant-on*' type of ME cell, which is currently not supported by SPWF fabric. Data encoding, handshaking, completion detection and reset mechanisms were presented with discussion on possible variants. As an example, a 32-bit A-SPWF based Carry Completion Sensing Adder (CCSA) was shown with preliminary area, power and performance evaluations.

CHAPTER 7

CONCLUSION

Spin Wave Functions logic fabric is one of the promising options for building post-CMOS nanoscale systems. Spin wave propagation does not involve any physical movement of charge particles. This provides a fundamental advantage over conventional charge based electronics and opens new horizons for novel nano-scale architectures. In this thesis, we have shown how compressed information representation, in terms of wave amplitude and phase, can significantly reduce circuit level power consumption and area. We have shown several variants of the SPWFs based on topology, signal weights, control inputs and wave frequencies. SPWF based designs of arithmetic circuits like adders and parallel counters were presented. With different topologies and circuit styles we have explored how capabilities at individual fabric components level can affect design and vice versa. In-depth experimental work on ME cell characterization is necessary to further validate the assumptions in this work.

Our estimates on benefits vs. 45nm CMOS implementation show that, for a 1-bit adder, up to 40x reduction in area and 228x reduction in power may be possible. For the 2-bit adder, results show that up to 33x area reduction and 222x reduction in power may be possible. Data streaming approaches based on Asynchronous SPWFs were also discussed with Carry Completion Sensing Adders as example. The proposed SPWFs fabric along with the directions discussed in this thesis have the potential of significantly impacting assumptions and methodologies in important areas of future nanoscale system design.

BIBLIOGRAPHY

[1] *International Technology Roadmap for Semiconductors. Available online at http://public.itrs.net/*, 2009.

[2] Akers, Sheldon B. Synthesis of combinational logic using three-input majority gates. In *Switching Circuit Theory and Logical Design, 1962. SWCT 1962. Proceedings of the Third Annual Symposium on* (oct. 1962), pp. 149 –158.

[3] Amarel, S., Cooke, G., and Winder, R. O. Majority gate networks. *Electronic Computers, IEEE Transactions on EC-13*, 1 (feb. 1964), 4 –13.

[4] Bailleul, Matthieu, Olligs, Dominik, and Fermon, Claude. Propagating spin wave spectroscopy in a permalloy film: A quantitative analysis. *Applied Physics Letters 83*, 5 (aug 2003), 972 –974.

[5] Bao, Mingqiang, Wong, Kin, Khitun, Alexander, Lee, Jooyoung, Hao, Zhibiao, L., Wang K., W., Lee D., and X., Wang S. Determining wave vector and material property from the phase-shift of spin-wave propagation. *Europhysics Letters 84* (2008), 27009.

[6] Beiu, V., Quintana, J.M., and Avedillo, M.J. Vlsi implementations of threshold logic-a comprehensive survey. *Neural Networks, IEEE Transactions on 14*, 5 (sept. 2003), 1217 – 1243.

[7] Briley, B.E. Some new results on average worst case carry. *Computers, IEEE Transactions on C-22*, 5 (may 1973), 459 – 463.

[8] Celinski, P., Lopez, J.F., Al-Sarawi, S., and Abbott, D. Compact parallel (m,n) counters based on self-timed threshold logic. *Electronics Letters 38*, 13 (jun 2002), 633 –635.

[9] Covington, M., Crawford, T. M., and Parker, G. J. Time-resolved measurement of propagating spin waves in ferromagnetic thin films. *Phys. Rev. Lett. 89* (Nov 2002), 237202.

[10] Csaba, G., Imre, A., Bernstein, G.H., Porod, W., and Metlushko, V. Nanocomputing by field-coupled nanomagnets. *Nanotechnology, IEEE Transactions on 1*, 4 (dec 2002), 209 – 213.

[11] Datta, Supriyo, and Das, Biswajit. Electronic analog of the electro-optic modulator. 665–667.

[12] Dichtel, William R, Heath, James R, and Fraser Stoddart, J. Designing bistable [2]rotaxanes for molecular electronic devices. *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences 365*, 1855 (2007), 1607–1625.

[13] Eerenstein, W., Mathur, N. D., and Scott, J. F. Multiferroic and magnetoelectric materials. *Nature 442*, 7104 (2006), 759 – 765.

[14] Galatsis, K., Khitun, A., Ostroumov, R., Wang, K.L., Dichtel, W.R., Plummer, E., Stoddart, J.F., Zink, J.I., Lee, Jae Young, Xie, Ya-Hong, and Kim, Ki Wook. Alternate state variables for emerging nanoelectronic devices. *Nanotechnology, IEEE Transactions on 8*, 1 (jan. 2009), 66 –75.

[15] Gilbert, T.L. A phenomenological theory of damping in ferromagnetic materials. *Magnetics, IEEE Transactions on 40*, 6 (nov. 2004), 3443 – 3449.

[16] Gilchrist, Bruce, Pomerene, J. H., and Wong, S. Y. Fast carry logic for digital computers. *IRE Transactions on Electronic Computers EC-4*, 4 (Dec. 1955), 133–136.

[17] Hendrickson, Herbert C. Fast high-accuracy binary parallel addition. *Electronic Computers, IRE Transactions on EC-9*, 4 (dec. 1960), 465 –469.

[18] Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G.H., and Porod, W. Majority logic gate for magnetic quantum-dot cellular automata. *Science 311*, 5758 (2006), 205–8.

[19] Khalili Amiri, Pedram, Rejaei, Behzad, Vroubel, Marina, and Zhuang, Yan. Nonreciprocal spin wave spectroscopy of thin Ni-Fe stripes. *Applied Physics Letters 91*, 6 (aug 2007), 062502 –062502–3.

[20] Khitun, A., Bao, Mingqiang, and Wang, K.L. Spin wave magnetic nanofabric: A new approach to spin-based logic circuitry. *Magnetics, IEEE Transactions on 44*, 9 (sept. 2008), 2141 –2152.

[21] Khitun, Alexander, Nikonov, Dmitri E., and Wang, Kang L. Magnetoelectric spin wave amplifier for spin wave logic circuits. *Journal of Applied Physics 106*, 12 (dec 2009), 123909 –123909–7.

[22] Koren, Israel. *Computer Arithmetic Algorithms*, 2nd ed. A. K. Peters, Ltd., Natick, MA, USA, 2001.

[23] Landau, L. D., and Lifshitz, E. M. Theory of the dispersion of magnetic permeability in ferromagnetic bodies. *Phys. Z. Sowietunion 8* (1935), 153.

[24] Lankhorst, Martijn H. R, Ketelaars, Bas W. S. M. M., and Wolters, R. A. M. Low-cost and nanoscale non-volatile memory concept for future silicon chips. *Nature Materials 4* (2005), 347–352.

[25] Lastella, S., Mallick, G., Karna, S.P., Joon, Yung, Ryu, Chang, and Ajayan, P. Single walled carbon nanotube junctions for nano-electronics and sensors. In *Nanotechnology, 2006. IEEE-NANO 2006. Sixth IEEE Conference on* (june 2006), vol. 1, pp. 295 – 297.

[26] Leblebici, Y., Ozdemir, H., Kepkep, A., and Cilingiroglu, U. A compact high-speed (31,5) parallel counter circuit based on capacitive threshold-logic gates. *Solid-State Circuits, IEEE Journal of 31*, 8 (aug 1996), 1177 –1183.

[27] McEuen, P.L., Fuhrer, M.S., and Park, Hongkun. Single-walled carbon nanotube electronics. *Nanotechnology, IEEE Transactions on 1*, 1 (mar 2002), 78 –85.

[28] Meo, Angelo Raffaele. Majority gate networks. *Electronic Computers, IEEE Transactions on EC-15*, 4 (aug. 1966), 606 –618.

[29] Miller, H. S., and Winder, R. O. Majority-logic synthesis by geometric methods. *Electronic Computers, IRE Transactions on EC-11*, 1 (feb. 1962), 89 –90.

[30] Miyata, Fusachika. Realization of arbitrary logical functions using majority elements. *Electronic Computers, IEEE Transactions on EC-12*, 3 (june 1963), 183 –191.

[31] Moritz, C.A., Wang, Teng, Narayanan, P., Leuchtenburg, M., Guo, Yao, Dezan, C., and Bennaser, M. Fault-tolerant nanoscale processors on semiconductor nanowire grids. *Circuits and Systems I: Regular Papers, IEEE Transactions on 54*, 11 (nov. 2007), 2422 –2437.

[32] Muller, David E. Asynchronous logics and application to information processing. In *Symposium on the Application of Switching Theory to Space Technology* (1963), Stanford University Press, pp. 289–297.

[33] Muller, David E., and Bartky, W. S. A theory of asynchronous circuits. In *Proceedings of an International Symposium on the Theory of Switching* (Apr. 1959), Harvard University Press, pp. 204–243.

[34] Muroga, Saburo. *Threshold logic and its applications.* Wiley-Interscience, New York, 1971.

[35] Ozdemir, H., Kepkep, A., Pamir, B., Leblebici, Y., and Cilingiroglu, U. A capacitive threshold-logic gate. *Solid-State Circuits, IEEE Journal of 31*, 8 (aug 1996), 1141 –1150.

[36] Rai, Suresh. Majority gate based design for combinational quantum cellular automata (qca) circuits. In *System Theory, 2008. SSST 2008. 40th Southeastern Symposium on* (march 2008), pp. 222 –224.

[37] Schmid, A., and Leblebici, Y. Realisation of multiple-valued functions using the capacitive threshold logic gate. *Computers and Digital Techniques, IEE Proceedings - 151*, 6 (nov. 2004), 435 – 447.

[38] Schneider, T., Serga, A. A., Leven, B., Hillebrands, B., Stamps, R. L., and Kostylev, M. P. Realization of spin-wave logic gates. *Applied Physics Letters 92*, 2 (jan 2008), 022505 –022505–3.

[39] Sen, B., Anand, A.S., Adak, T., and Sikdar, B.K. Thresholding using quantum-dot cellular automata. In *Innovations in Information Technology (IIT), 2011 International Conference on* (april 2011), pp. 356 –360.

[40] Shabadi, P., Khitun, A., Narayanan, P., Bao, Mingqiang, Koren, I., Wang, K.L., and Moritz, C.A. Towards logic functions as the device. In *Nanoscale Architectures (NANOARCH), 2010 IEEE/ACM International Symposium on* (june 2010), pp. 11 –16.

[41] Shabadi, P., Khitun, A., Wong, Kin, Amiri, P.K., Wang, K.L., and Moritz, C.A. Spin wave functions nanofabric update. In *Nanoscale Architectures (NANOARCH), 2011 IEEE/ACM International Symposium on* (june 2011), pp. 107 –113.

[42] Spars, Jens, and Furber, Steve. *Principles of Asynchronous Circuit Design: A Systems Perspective*, 1st ed. Springer Publishing Company, Incorporated, 2010.

[43] Strukov, D.B., and Likharev, K.K. Reconfigurable hybrid cmos/nanodevice circuits for image processing. *Nanotechnology, IEEE Transactions on 6*, 6 (nov. 2007), 696 –710.

[44] Swartzlander, E.E., Jr. Parallel counters. *Computers, IEEE Transactions on C-22*, 11 (nov. 1973), 1021 – 1024.

[45] Tour, James M. Molecular electronics. synthesis and testing of components. *Accounts of Chemical Research 33*, 11 (2000), 791–804.

[46] Verhoeff, Tom. Delay-insensitive codes—an overview. 1–8.

[47] Wang, Teng, Narayanan, P., and Andras Moritz, C. Heterogeneous two-level logic and its density and fault tolerance implications in nanoscale fabrics. *Nanotechnology, IEEE Transactions on 8*, 1 (jan. 2009), 22 –30.

[48] Wang, Z.F., Zheng, Huaixiu, Shi, Q.W., and Chen, Jie. Emerging nanocircuit paradigm: Graphene-based electronics for nanoscale computing. In *Nanoscale Architectures, 2007. NANOARCH 2007. IEEE International Symposium on* (oct. 2007), pp. 93 –100.

[49] Williams, Ted. Latency and throughput tradeoffs in self-timed speed-independent pipelines and rings. Tech. rep., 1990.

[50] Zhang, Rui, Gupta, P., Zhong, Lin, and Jha, N.K. Threshold network synthesis and optimization and its application to nanotechnologies. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on 24*, 1 (jan. 2005), 107 – 118.

[51] Zhang, Rumi, Walus, K., Wang, Wei, and Jullien, G.A. A method of majority logic reduction for quantum cellular automata. *Nanotechnology, IEEE Transactions on 3*, 4 (dec. 2004), 443 – 450.