2008

A Ka Band Switch-lna Mmic For Radiometry Applications

Miguel Alvarado
University of Massachusetts Amherst

A KA BAND SWITCH-LNA MMIC FOR RADIOMETRY APPLICATIONS

A Thesis Presented

by

MIGUEL A. ALVARADO

Submitted to the Graduate School of the
University of Massachusetts Amherst in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE

IN ELECTRICAL AND COMPUTER ENGINEERING

February 2008

Department of Electrical and Computer Engineering

A KA BAND SWITCH-LNA MMIC FOR RADIOMETRY APPLICATIONS

A Thesis Presented

by

MIGUEL A. ALVARADO

Approved as to style and content by:

_____
Robert W. Jackson, Chair

_____
K. Sigfrid Yngvesson, Member

_____
Omid Oliaei, Member

_____
Christopher V. Hollot, Department Head
Electrical and Computer Engineering

To my mother Herminia

ACKNOWLEDGMENTS

First, I would like to thank my advisor Professor Robert W. Jackson for his enduring patience throughtout my graduate career, especially while I was writing my thesis. I would also like to thank Professors Yngvesson and Oliaei for taking time out of their schedules to help answer questions, review my thesis and serve on my thesis committee. I'd also like to thank Professor Steven Reising for giving me two Ka-band LNA MMICs to assist me in my noise figure measurements.

Secondly, this thesis would not have been possible without the wafer space gratiously supplied by Colin Whelan of Raytheon RF Components in Andover Massachussetts. In addition, I would also like to thank Mikael Garcia, Joseph Boseley, and Steve Lardizabal of Raytheon RF Components and Steve Clausen of Monolithics for their assistance during the design and with the layout.

Finally, I would also like to thank my fellow graduate students at UMass. Special thanks to Flavio Iturbide-Sanchez and Fernando Rodriguez-Morales who were always available to discuss my thesis in the design and measurement phase, but especially for their friendship. In addition I'd also like to thank Nino Majurec, Nidhi Khandelwal, Jessel Xavier, John Nicholson and Frances Corgnati for their assistance in various phases of my graduate career.

ABSTRACT

A KA BAND SWITCH-LNA MMIC FOR RADIOMETRY APPLICATIONS

FEBRUARY 2008

MIGUEL A ALVARADO, B.S., UNIVERSITY OF ILLINOICS URBANA-CHAMPAIGN

M.S., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Robert W. Jackson

The need for low cost and low size radiometers have encouraged many to look at the implementation of radiometers using MMICs. Compared to their waveguide counterparts, radiometers implemented with MMICs significantly reduce the size and weight of the radiometer, while still maintaining satisfactory electrical performance at millimeter wave frequencies. Utilizing MMICs can also help in significantly lowering the noise temperature of the radiometer, specifically, metamorphic high electron-mobility transistors (mHEMT) have demonstrated very low noise, high gain performance and comparably low cost. This thesis is focused on designing a combined switch and low noise amplifier IC at 36.5 GHz that lowers the radiometer noise temperature while allowing for an accurate calibration. The measured gain from straight and 90 degree input of the switch-LNA, at 36.5 GHz, was 6.6 dB and 7.1 dB, respectively. Likewise, the noise figure of the MMIC was 3.8 dB and 3.3 dB, respectively. The mHEMT implemented SPDT switch has a measured insertion loss, at 36.5 GHz, of 1.3 dB and 0.88 dB with isolation of 25 dB and 36 dB, respectively. The calculated temperature sensitivity based on measured temperature variations was 0.273 K at 36 GHz.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Overview of Project

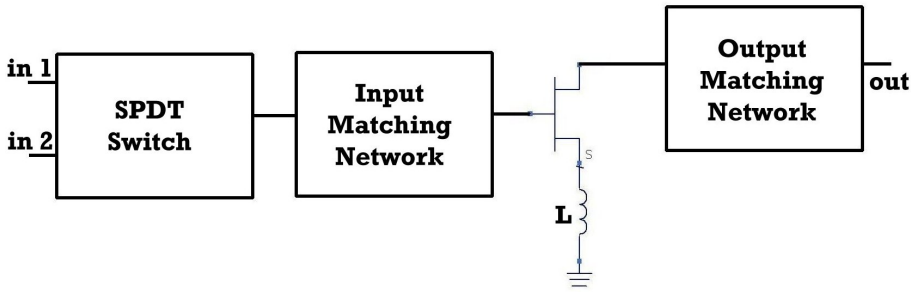

Figure 1.1: Switch-LNA Design Block Diagram

The goal of this project is to design a combination LNA and switch using the low cost mHEMT process. The basic block diagram of the switch and LNA is shown in figure 1.1 above. There are two possible inputs to the switch, and depending on the biasing of the switch, one of those input signals will pass through the switch to the input matching network of the LNA. The input matching network is designed to match the output of the switch to the input of the LNA, its added purpose for this design, is also to aid in stabilizing the LNA. As shown in figure 1.1, an inductance L is used at the source of the FET to allow a good match at the input while also providing minimum noise. Based on the input match, the output matching network is designed to provide a good match at the output while not degrading the noise and gain of the amplifier.

The circuit was fabricated at Raytheon RF Components and characterized in LAMMDA Lab. In addition to the standard s-parameter and noise figure characterization temperature measurements were performed to determine the circuit's

variation versus temperature. Temperature simulations that can be used to predict the performance of the circuit have also been performed and compared to measured results.

1.2 Organization of document

This thesis focused on the design and characterization of the SPDT switch and switch-LNA combination. Chapter 2 covers the background and motivation for this thesis: it provides background information on radiometry, the mHEMT process, switches, low noise amplifiers and the temperature simulation and measurements that were made. Chapter 3 focuses on the design methodology used in the design of the MMIC switch and LNA. It covers the design process and the steps followed to perform the temperature simulations. Chapter 4 provides the considerations that were taken due to the layout constraints; it demonstrated the effects of the final non ideal design. Chapter 5 presents the measured results of the design, both for the individual switch and the low noise amplifier. Additionally it includes the results of the temperature measurements, and discrepancies are also analyzed. Finally, chapter 6 provides a summary of the design and its implementation, as well as suggestions for future work.

CHAPTER 2

BACKGROUND AND MOTIVATION

This chapter provides a background on radiometry, the mHEMT process, switches, LNAs, temperature modeling and the motivation for this thesis.

At the system level one of the most important benefits of implementing radiometers with MMICs is the potential for a significant reduction in size and weight. At mm-wave frequencies the standard waveguide implementation of radiometers can have dimensions of 25x15x4 in^3 and weight approximately 17 kg, however, if the radiometer is implemented with MMICs the dimensions would decrease to 7x9x6 in^3 with a weight reduction to around 3.5 to 4 kg [1]. This thesis seeks to investigate the first components in the radiometer chain after the antenna on a chip level, particularly how a switch-LNA MMIC responds to change in ambient temperature, and whether an accurate calibration would be possible using this chip.

2.1 Radiometry

In general terms radiometers are simply sensitive receivers that measure electromagnetic emissions. Unlike traditional receivers the signal being measured by the radiometer is typically much smaller than the receiver noise power. The specific

function of a radiometer is to measure the intensity of radiation incident upon the antenna and the self-emission by the antenna itself [2]. Therefore one of the important figures of merit of a radiometer is how accurately that measurement can be made. As will be discussed later in this chapter the accuracy of the radiometer is dominated by the gain fluctuations in the amplifier used to amplify the signal from the antenna.

For an ideal blackbody the maximum power that can be emitted at a given temperature T can be defined as P_{MAX}, similarly if a lossless antenna is placed inside a chamber made of perfect absorbing material the power received by the antenna can also be defined as

$$P_{MAX} = kTB \tag{2.1}$$

Where k is Boltzmann's constant, T is the physical temperature and B is the bandwidth of the radiometer. This relationship between power and temperate has led to the term "radiometric temperature" used to characterize the actual power emitted by or received in the real world. For example the brightness temperature of a radiometer is defined as

$$T_B = \frac{P}{kB} \tag{2.2}$$

Where P is the power emitted by the material over the bandwidth B. Similarly the power received by the radiometer antenna, the antenna noise temperature, is defined as

$$T_A = \frac{P_a}{KB} \tag{2.3}$$

where T_A is the average fluctuating noise type signal that the radiometer will measure, it represents all radiation incident upon the antenna, integrated over all possible

directions and weighted according to the antenna directional pattern as well as due to conductor loss within the antenna [2]. Therefore one of the critical and most important figures of merit for radiometers is how well T_A can be measured.

In order for the radiometer measurements to be accurate the calibration the radiometer internally performs must be accurate. The radiometer calibrates itself by means of a single-pole double-throw switch with one input arm of the switch connected to a noise source and the other connected to the antenna. The output of the switch is connected to the input of the LNA. This configuration is shown in figure 2.1, below:

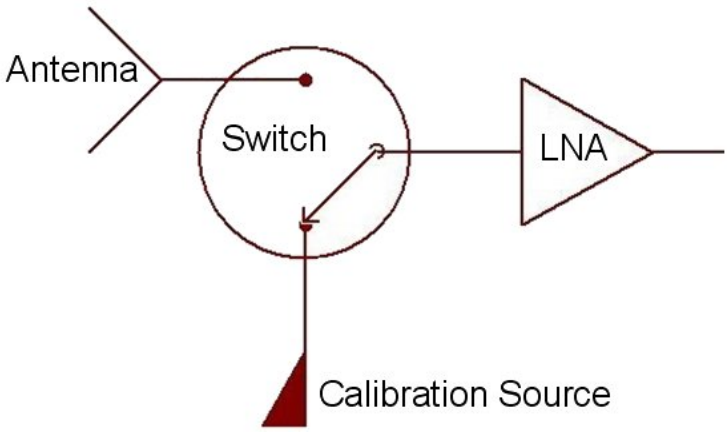

Figure 2.1: Radiometer input Stages

When the switch is biased such that the LNA is connected to the noise source the radiometer system produces an output voltage, V_{out}, as a function of the noise temperature apparent at the LNA input. Since most radiometers utilize square-law detection it will be assumed that a linear relationship exists between the input power

and the output voltage. Therefore it is adequate to measure the output voltage for a few calibration temperatures. Once this relationship is determined by plotting a calibration curve, it can then be used to convert the output voltage to the brightness temperature viewed by the antenna. An example of this calibration curve is in figure 2.2.

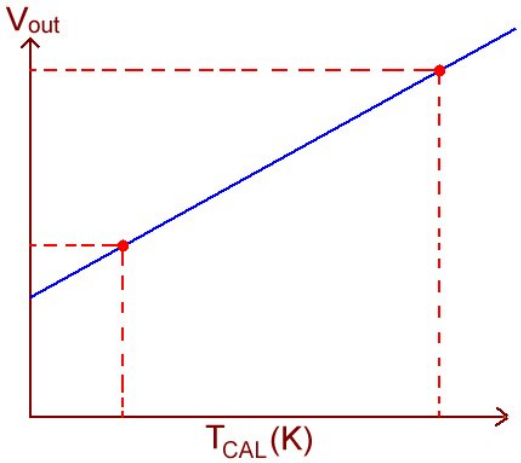

Figure 2.2: Radiometer Calibration Curve

The output voltage consists of both ac and dc components, described below:

$$\boldsymbol{V}_{out}(\boldsymbol{t}) = \boldsymbol{V}_{dc} + \boldsymbol{V}_{ac}(\boldsymbol{t}) \tag{2.4}$$

$$\boldsymbol{V}_{dc} = \boldsymbol{G}_{S}(\boldsymbol{T}_{A} + \boldsymbol{T}_{REC}) \tag{2.5}$$

The dc component is the mean value of the input power while the ac component represents the low-frequency component of the post-detection noise spectrum [2]. In equation 2.5 $\boldsymbol{G}_{S}$ is the system gain factor and $\boldsymbol{T}_{REC}$ is the equivalent receiver input noise-temperature. The rms value of $\boldsymbol{V}_{ac}$ is related to $\boldsymbol{V}_{dc}$ by equation 2.6.

$$\frac{(\boldsymbol{V}_{ac})_{rms}}{\boldsymbol{V}_{dc}} = \frac{1}{\sqrt{\boldsymbol{B}\tau}} \tag{2.6}$$

Where τ is the integration time presented by the integrator. The relationship expressed in equation 2.6 leads to equation 2.7.

$$\Delta T_N = \frac{\left(T_A + T_{REC}\right)}{\sqrt{B\tau}} \tag{2.7}$$

Where ΔT_N represents the precision with which T_A can be obtained from $V(t)$, assuming the receiver gain factor G_S remains absolutely constant over the integration period τ [2].

However, ΔT_N only needs to account for the uncertainty due to the noise fluctuations and does not take the receiver gain fluctuations into account. Equation 2.7 was derived assuming the gain was constant, which can in general be assumed for post detection stages, but not pre detection stages where the gain variations typically occur in the low noise amplifier, mixer and IF amplifier. Since the output voltage measured during the calibration is linearly related to the product $G_S T_{SYS}$ then if the gain varies by ΔG_S that would cause the output to be mistaken by [2]:

$$\Delta T_{SYS} = T_{SYS}\left(\frac{\Delta G_S}{G_S}\right) \tag{2.8}$$

As a result as long as the gain variations occur over long periods of time, in the order of minutes, they can usually be factored out by simply rapidly recalibrating the radiometer before gain variations can occur. However, short term gain variations are difficult to factor out with re-calibrations. The rms uncertainty in T_A due the gain variations can be defined in equation 2.9.

$$\Delta T_G = T_{SYS}\left(\frac{\Delta G_S}{G_S}\right) \tag{2.9}$$

Where ΔG_S is the effective value (rms) of the detected power gain variation (ac component) [2].

Since the noise and gain uncertainties are caused by distinct causes, they can be considered statistically independent; therefore the total rms uncertainty can be given by

$$\Delta T = \left[(\Delta T_N)^2 + (\Delta T_G)^2\right]^{1/2}$$

$$= T_{SYS}\left[\frac{1}{B\tau} + \left(\frac{\Delta G_S}{G_S}\right)^2\right]^{1/2} \tag{2.10}$$

This expression defines the radiometric sensitivity of the total power radiometer, taking into account both the gain and noise variations. In order to obtain a general understanding of the effect of each variation an example using typical values as described in Pozar is shown below [3].

A total power radiometer at a center frequency of 1.4 GHz is characterized by

T_{REC} = 500 K ; B = 100MHz; τ = 0.01 s, and $\frac{\Delta G_S}{G_S} = 10^{-2}$

If the antenna temperature T_A = 300K then ΔT_N = 0.8K, ΔT_G = 8 K and therefore a ΔT = 8.03 K.

The previous example demonstrates that the radiometer sensitivity is primarily affected by the gain variations and not the noise variations. Additionally, the accuracy of the measurements made by the radiometer is highly dependent on the precision of the calibration, specifically how well the calibration noise temperature and gain are known. For present day radiometers the sensitivity desired should be of the order of 0.1 to 0.2 K or less [1]. One way to reduce unwanted gain variations is by controlling the sources that cause these variations, the power supply voltages and the environmental temperature variations. However, gain variations are also intrinsic to the HEMT amplifiers so all variations cannot be removed. In this thesis the gain variations caused predominantly by environmental temperature variations will be observed.

2.2 Process Implementation

Another important characteristic of a radiometer is that the overall noise temperature of the system be low. This improves sensitivity and reduces the time needed for observation. Since the front-end components help determine the overall noise temperature of the radiometer, designing the first stage components to have low noise is one way to improve the noise performance of the radiometer. One approach to improve noise performance is by using a low noise process to design the switch and low noise amplifier.

The idea of High Electron Mobility Transistors (HEMT) was first introduced in 1978 [4] and the first published report of HEMT was done by engineers at Fujitsu which also coined the term HEMT [5]. HEMTs have also been referred to as MODFET (Modulation Doped FET), SDHFET (Selectively Doped Heterostructure FET), and TEGFET (Two-Dimensional Electron Gas FET) [6]. The cross section of a HEMT typically consists of a GaAs substrate, buffer, channel, and n-type AlGaAs barriers; this cross-section is shown in figure 2.3. Figure 2.3, also includes another feature of high performance FETs: a mushroom gate. This type of gate design was conceived to solve the problem of gate resistance. As gate lengths became smaller, down to submicron range, the resistance of the small gate strip increased which has a negative impact on the gain and noise performance at high frequencies [4]. By using a mushroom gate it is possible to have a short gate length and small gate resistance.

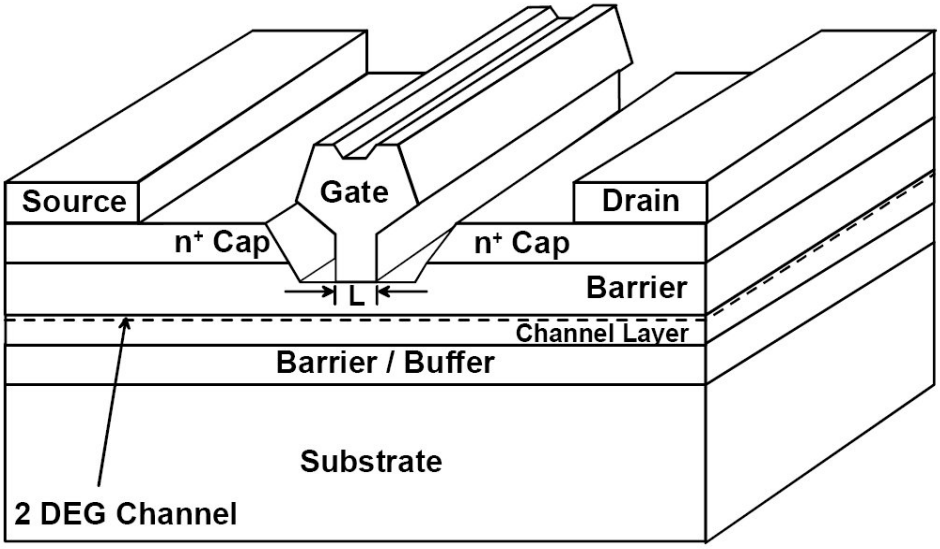

Figure 2.3: Standard HEMT cross section [7]

Additionally, HEMTs make use of heterojunctions that occur when two semiconductors of different compositions and bandgaps are used to form a device. At the interface of the two semiconductors a triangular potential well forms that confines electrons in a two-dimensional electron gas, this separates the free electrons in the channel from the ionized donors and reduces the ionized impurity scattering, in so doing increasing the electron mobility. In general the semiconductors that form the heterojunction should be lattice matched; however, in practical structures some mismatch can be accommodated without degrading the crystalline quality, these structures are referred to as pseudomorphic or metamorphic.

When considering HEMT technology InP-based HEMTs have demonstrated the highest gain and lowest noise performance at millimeter wave frequencies [8, 9]. However, Indium Phosphide based technology is more expensive compared to technologies fabricated on GaAs. There are a few reasons for this, most importantly GaAs substrates are available in a 6" diameter at a cost of $450 while InP substrates come in 3"-4" diameters and cost more than $1000 [10]. InP wafers are also brittle and hard to handle which can lead to poor yield thus increasing the cost per chip. Therefore InP transistors are typically only used for high precision commercial and military applications. For this reason alternatives to InP technology has been investigated. Early on this led to the significant progress in elastically strained layer structures, pseudomorphic HEMT or pHEMT technology.

Although pseudomorphic HEMT has lower performance compared to InP HEMT it does have superior noise and gain performance at high frequencies when compared to the traditional lattice-matched AlGaAs/GaAs HEMTs. The reason for this is because pHEMT uses a small InGaAs layer in between the AlGaAs barrier layer and the GaAs buffer which for low noise applications is undoped. However, this creates a lattice mismatch, because InGaAs is not lattice matched to GaAs, this is shown in figure 2.4, where the numbers 10-90 represent the range, in percentage, of In used in the semiconductor.

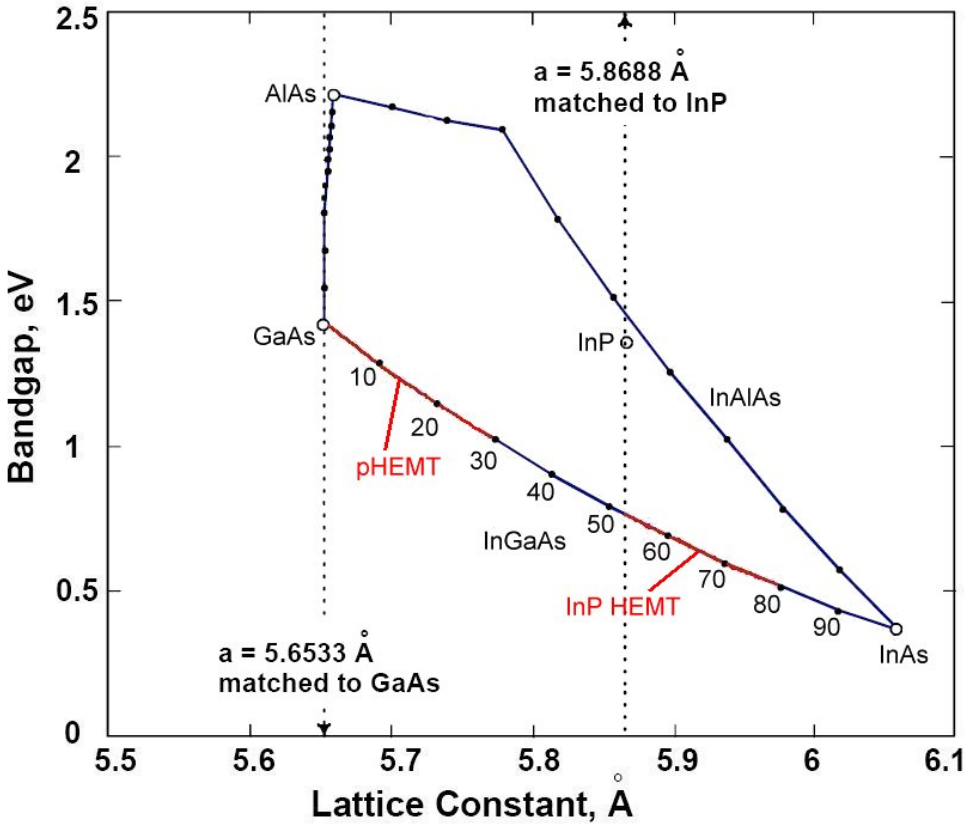

Figure 2.4: Lattice Constant vs Bandgap plots for relevant semiconductors

Effectively in pHEMT the InGaAs layer is distorted from its normal cubic crystalline structure by being compressed to match the lattice constant of GaAs. An example of this compression is shown in figure 2.5, where the arrows indicate the compressive strain occurring in the pseudomorphic InGaAs layer [7].

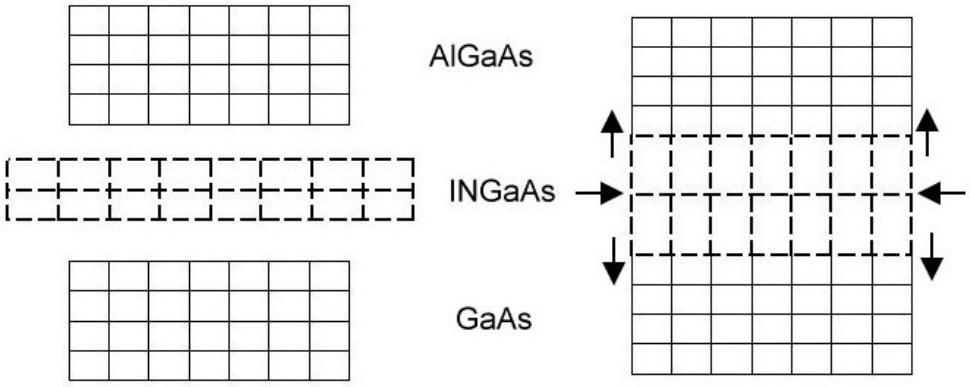

Figure 2.5: pHEMT GaAs-InGaAs-AlGaAs Heterostructure

This lattice mismatch between the two layers can be accommodated elastically up to a critical thickness, typically around 10-15nm thick, with the percent In ranging from 15% to 20%. Since increasing the amount of In increases the mobility of the transistor a higher Indium content is preferable.

An alternative to pHEMT that has been explored since the early 1990s is metamorphic HEMTs or mHEMT. mHEMT allows for any amount of Indium to be deposited due to its use of a graded buffer layer. The graded buffer is much thicker than the critical thickness and is grown on the GaAs substrate. The purpose of the buffer is to transform the lattice constant from that of GaAs to that of the InGaAs channel and to

protect the channel from dislocations that occur when two materials with very different lattice constants are combined [7]. The layer sequence of GaAs mHEMT, GaAs pHEMTs, and HEMTs and are shown in figure 2.6.

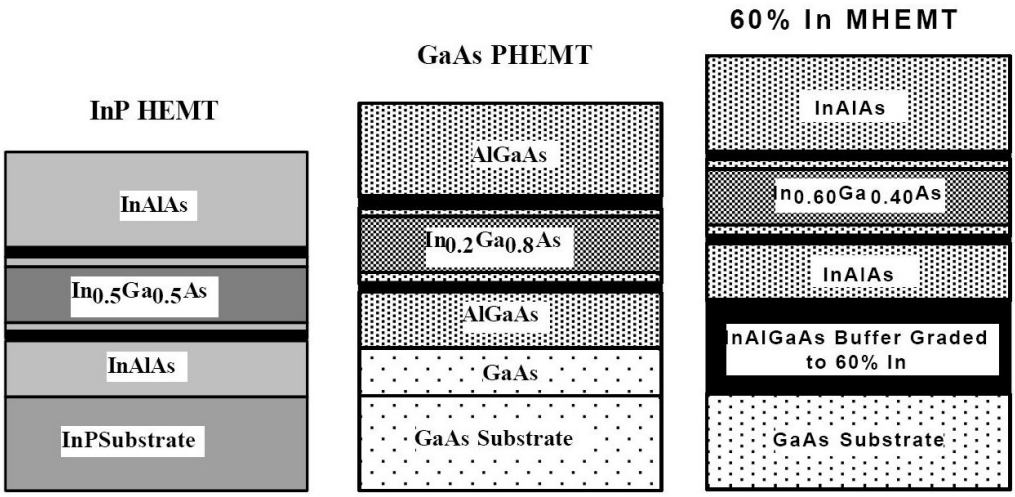

Figure 2.6: Typical layer structures for InP HEMT, GaAs pHEMT, and GaAs mHEMT [11]

From figure 2.6, it can be seen that the InP HEMT consists of an InGaAs channel which as shown on figure 2.4 is lattice matched to InP, the pHEMT structure consists of a InGaAs channel between two AlGaAs barriers grown on a GaAs substrate, the mHEMT structure consists of an InAlGaAs graded buffer with 60% In which allows an InGaAs channel to be formed on InAlAs layers, this is essentially an InP HEMT grown on a GaAs substrate. The InGaAs channel used in mHEMT is also smoother and allows flat interfaces compared to the pHEMT channel, this is shown in the transmission electron microscope (TEM) pictures shown in figures 2.7 and 2.8, both pictures have the same 400 Angstroms scale.

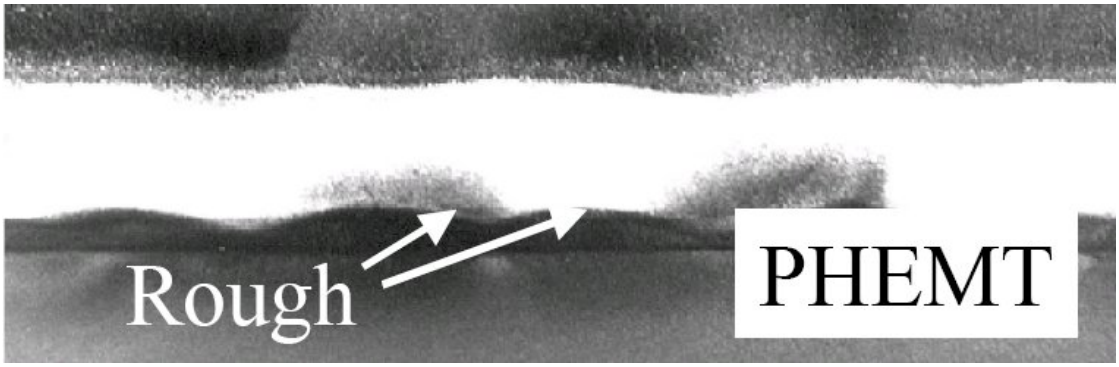

Figure 2.7: pHEMT TEM layer picture [11]

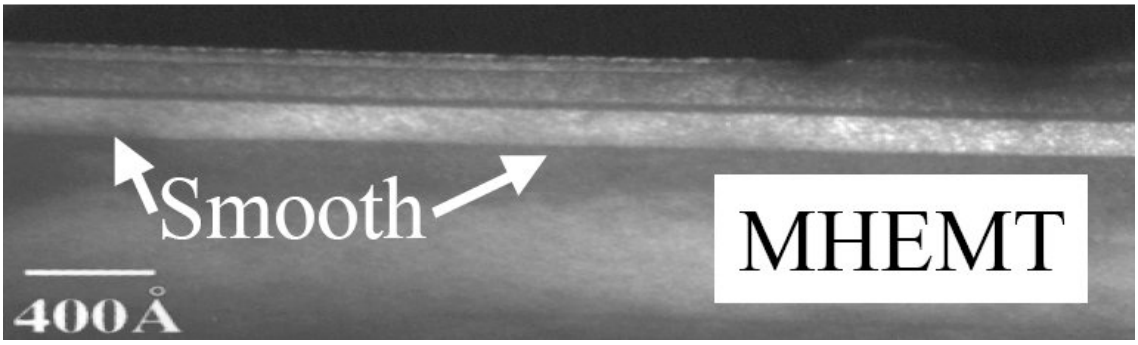

Figure 2.8: mHEMT TEM layer picture [11]

The pHEMT channel layer is much rougher than mHEMT because the dislocations are predominantly located in the graded buffer of the mHEMT structure, while on pHEMT they occur at the InGaAs channel. In figure 2.9 a zoomed in TEM picture of the AlGaInAs graded buffer many dislocations can be seen, these are created during the grading in order to increase the lattice constant.

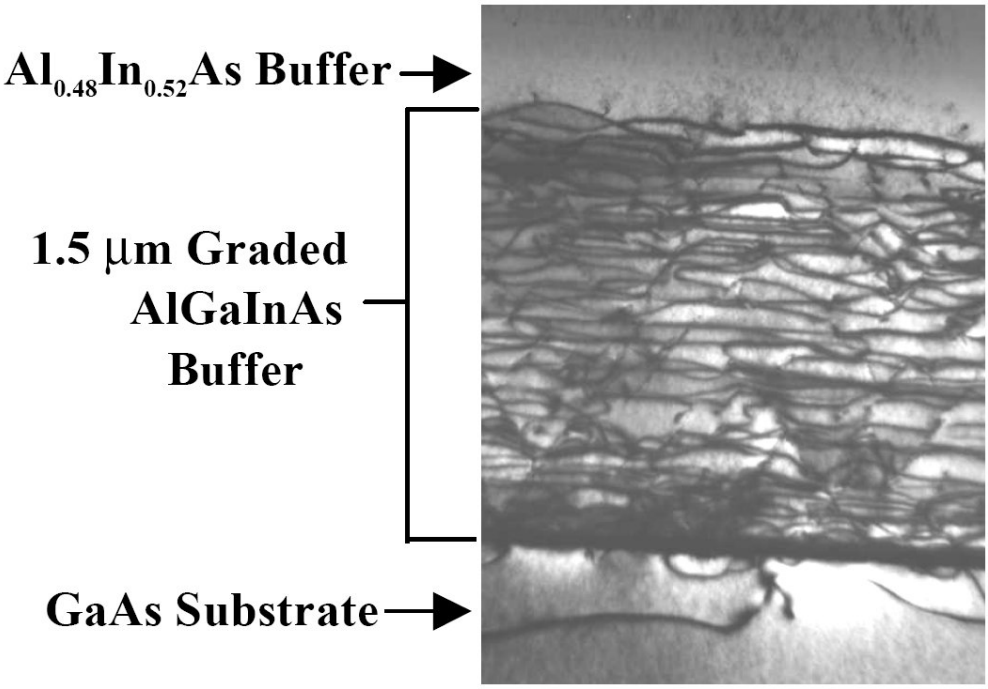

Figure 2.9: TEM picture of mHEMT graded buffer layer [11]

Therefore the graded buffer which allows InP like hetereostuctures to be grown on GaAs substrates have made mHEMT technology an attractive alternative in designs where low noise, high gain and price are equal factors. Published results for this mHEMT process show an F_{min} of less than 0.8 dB and an associated gain of 8 dB for a single stage 100 micron gate FET at 35 GHz [12].

2.3 Switches

Switches are an important part of any system because they can control the path of signals through multiple inputs and outputs. For each input to output path the switch

should be able to block, isolate, the signal when needed, for that reason high isolation is one of the important figures of merit in switches. Conversely the switch should also be able to pass the signal path from the input to the output with as little loss as possible.

At microwave frequencies monolithic p-i-n diode switches have shown high isolation and low insertion loss [13]. However, this is not compatible with the process that is used to implement the other components in a receiver which are typically implemented in HEMT. For this reason passive switches implemented with FETs remain popular. Many configurations and design techniques have been used to implement passive FET switches and among the most popular have been the resonance type switches which have reported isolation better than 30 dB [13,14]. Other techniques have been realized to obtain high isolation. Over 50 dB of isolation has also been reported for Q-band HEMT switches using two-state un-terminated quarter-wave shunt design, but this design required a large chip area [15]. Another successful technique was used for designing a DC-60 GHz heterojunction FET (HJFET) which reported > 25.5 dB of isolation in a compact design but it required a special process for the ohmic electrode-sharing technique used [16]. The traveling wave method using MESFET reported results of less than 2 dB insertion loss and isolation greater than 23 dB for a frequency range of 20-40 GHz [17]. Recently pHEMT passive switches were designed using impedance transformation and the traveling wave technique. These design techniques reported isolation greater than 30 dB and insertion loss of less than 2 dB and 3 dB, respectively [18, 19]. A table summarizing previous switch results is shown in table 2.1.

Table 2.1: Previously Reported Results of Passive FET Switches at Ka-band

Process	Design Approach	Freq Range (GHz)	Insertion Loss (dB)	Isolation (dB)	Chip Size (mm^2)	Reference
MESFET	Traveling Wave, Shunt	20-40	<2	>23	1.25x1.25	M. J. Schindler [17]
MESFET	Traveling Wave, Shunt	DC-40	<3	>23	0.84x1.27	M. J. Schindler [17]
GaAs HEMT	$\frac{\lambda}{4}$, Shunt	42-46	<1.6	35-50	5x2	D.L. Ingram [15]
HEMT Diode	Traveling Wave, Shunt	23-78	<4	>25	2.65x1.33	T. Shimura [20]
HJFET	Ohmic electrode-sharing technology, series shunt	DC-40	<3.5	>25.5	0.86x0.64	Mizutani [16]
MESFET	Shunt	15-30	2~3	>20	2x2.2	Bermkopf [21]
GaAs pHEMT	Impedance Transformation, Shunt	38-43	<2	>30	2x1	Lin et all [18]
GaAs pHEMT	Traveling Wave, Shunt	15-80	<3.6	>25	1.5x1.5	Lin et all [19]
GaAs pHEMT	Traveling Wave, Shunt	DC-60	<3	>25	1x1	Lin et all [19]
GaAs pHEMT	Traveling Wave, Shunt	DC-80	<3	>24	1x0.75	Lin et all [19]

Based on the observations made from the previous switch designs around the Ka-band frequency band the traveling wave method was selected for this design. The main reason is because the traveling wave technique can potentially take up the least amount of chip area while still providing excellent insertion loss at the design frequency of this thesis. The ability to easily control isolation, which will be discussed in chapter 3, is another important reason why this technique is more advantageous.

2.4 Low Noise Amplifiers

High frequency receivers and especially radiometers need to be able to detect small signals that are often downconverted into lower frequencies. Therefore the function of an LNA is to provide enough gain to be able to overcome the noise that's added by subsequent stages which may include a quite noisy mixer with a high conversion loss. From Friis' formula shown below, it can be shown that the total noise figure of the system is by and large determined by the noise of the first components in the system.

$$F = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_1 - 1}{G_1 G_2} + \ldots \tag{2.11}$$

Since the LNA is one of the first components in the system the overall noise figure of the LNA must be small. The LNA should also present a real impedance at the output, typically 50 Ω.

High performance low noise amplifiers that are implemented on InP HEMTs have shown the highest gain and lowest noise performance. InP based LNAs also have less than a fourth the DC power when compared to GaAs HEMT based LNAs [22]. But as previously mentioned in chapter 2.2 InP LNAs are more expensive to manufacture. Previous work in mHEMT has yielded noise figures for LNAs under 2 dB at 32 GHz [12], and 1.6 dB at 30 GHz [23].

In general LNAs at high frequencies are implemented in multiple stages with the first stage using emitter degeneration and the following stages using the standard common source configuration. The low noise amplifier in this project will be designed in a single stage. Low noise is the top priority; however, obtaining a reasonable amount of gain is always important. The reason that a multiple stage LNA was not designed was mainly because the central goal of this thesis is to track the gain variations due to ambient temperature. In a multi-stage LNA the variations observed may not be entirely due to temperature because variations could occur among the LNA stages. Secondly, a multistage LNA would have required considerably more chip area than was available.

2.4.1 Source Degeneration

One of the limitations that confront a low noise amplifier designer is the tradeoff between optimum noise or optimum input match. This tradeoff can be relaxed by the use of source degeneration. The basic idea of source degeneration or negative feedback is to modify the s-parameters of the FET itself by adding a small inductance at the source of the FET. A simplified FET model with and without a source inductance is shown in figure 2.10.

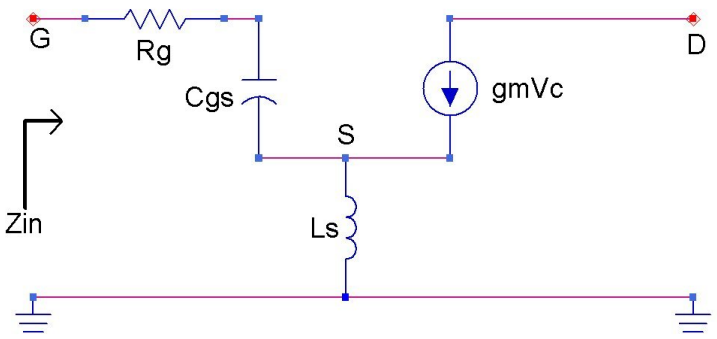

Figure 2.10: Simplified FET model with external source inductance L_s

The input impedance of the model above can be shown to be, from [24]:

$$Z_{in} = R_g + g_m \frac{L_s}{C_{gs}} + j\left[\omega L_s - \frac{1}{\omega C_{gs}}\right] \tag{2.12}$$

If $R_a = g_m \frac{L_s}{C_{gs}}$, then Z_{in} can be simply written as,

$$Z_{in} = R_g + R_a + j\left[X_{ls} - X_{cgs}\right] \tag{2.13}$$

If the source inductance was not present, and the source was grounded the input impedance can easily be calculated to be:

$$Z_{in} = R_g - jX_{cgs} \tag{2.14}$$

This means that the feedback created by the addition of the inductance L_s adds a real impedance that is equal to R_a and a positive reactance equal to X_{ls}. This then allows the value of Γ_{in}^* move closer to the value of Γ_{opt}. An example, unrelated to this design is shown in figure 2.11.

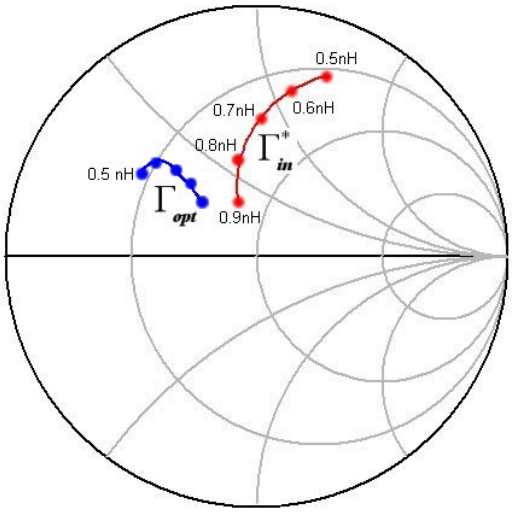

Figure 2.11: Variation of Γ_{in}^{*} due to increasing L_s

Figure 2.11 plots the effect of increasing Ls, and as can be seen the increase of Ls allows for a more optimum noise and input match. An additional advantage to using source degeneration is that the noise circles become broader making the noise figure less sensitive to mismatch, and $F_{\min}$ may decrease. However, the downside of using source degeneration is that gain is inversely proportional to L_s, that's because the feedback is negative [24]. Therefore a tradeoff still exists between the gain, noise and input match though the advantages of adding a source inductance is still an improvement over the standard common source configuration.

2.5 Temperature Simulations

Obtaining models that can predict the performance of a device over temperature can be quite difficult to create, mostly due to the difficulty involved in the modeling itself. For that reason the majority of models used by MMIC designers do not include temperature models. Whenever temperature models are developed they usually involve extensive temperature measurements over frequency and are valid for only a few devices on a specific process. There are, however, several similarities among processes that can be used when a rough estimate of temperature variation is needed. Several papers have been published in which "table models" have been used to model the effect of temperature. MESFET and HEMT temperature modeling has been previously done following this method [25-26]. Although doing an accurate temperature model is beyond the scope of this thesis, these investigations can help in supporting assumptions that were made in the temperature simulations performed to roughly estimate temperature performance.

Among the parameters that can affect the temperature performance are the intrinsic capacitances, resistances and the transconductance, gm. Results obtained for GaAs MESFETs were that the value of gm decreased exponentially from -55 to 25 C and then varies slightly from 25 C to 100 C, additionally it was found that the variation of Cgs, Cdg and Cds is not considerable [27]. In terms of S-parameters, temperature most affected S21 and S22 of the small signal model, with S21 and S22 decreasing from -55 C to 100 C. Another paper characterizing MESFETs observed that the gain S21

increased from room temperature to 100 C at low input power levels; however, at an input power level higher than 3 dBm the gain drops with temperature [28].

HEMT temperature dependence has also been investigated. InP and AlGaAs HEMTs displayed similar characteristics as MESFETs, with intrinsic capacitances increasing slightly while gm has a more significant variation with increasing temperature [29]. The value of gm was observed to drop with increasing temperature, thus the value of S21 would also decrease in a similar fashion. In addition, a study of pHEMT temperature modeling also reported that gm is best modeled by a quadratic temperature dependence. The temperature simulations used in this thesis involves the assumption based on the previous published temperature measurements that the change in gm dominates the temperature variations observed on a mHEMT FET. Therefore, for this thesis the temperature variations of the circuit were estimated by using previously measured temperature data on the same Raytheon process.

The purpose of learning about the temperature dependence of a device is to determine how sensitive the full circuit is to temperature. In radiometry, the sensitivity measurement is highly dependent on the reliability of the calibration. As shown in figure 2.2 the calibration of the radiometer involves voltage measurements at different calibration temperatures when the switch is connected to the calibration source. Once the calibration is complete an output voltage is measured when the switch is connected to the antenna, if the temperature does not track well between both of the switch arms an error will be introduced in the measurement. For radiometry the tracking between the

switch arms should be to the order of 0.1 K [1]. Another important quality that the switch must have is high isolation. This is because when a calibration is being performed the antenna remains connected to the other arm of the switch and if there is not enough isolation then the antenna may interfere during the calibration, thus making any measurements invalid. The amount of isolation needed would be dependent on the sensitivity that is required and the noise temperatures being measured, typically a value above 25-30 dB is acceptable.

CHAPTER 3

DESIGN METHODOLOGY

This chapter describes the design methodology used in designing the switch and LNA. It also includes the circuit performance as simulated by ADS. Additionally the procedure used to predict the temperature performance of the Switch-LNA is presented in detail, as well the simulation results as they relate to radiometry applications.

3.1 SPDT Switch

The single pole double throw switch was designed to have two inputs and one output, though the SPDT can also work having one input and two outputs. The switch was designed to have minimum insertion loss while still having an isolation of less than 25 dB at the operating frequency between 36 and 37 GHz. Additionally, both inputs should be as close as possible to limit variation between both ports.

3.1.1 Design Techniques

As described in the previous chapter the technique utilized for the design of the SPDT switch is the traveling wave method. This method utilizes shunt FETs with the source grounded while the drain is connected to the signal line. The FETs are biased via a large “open gate resistor” at the gate, the source is grounded and there is no drain voltage applied. The open gate resistor serves to isolate the bias voltage from the gate,

thereby creating a virtual open at the gate. A traveling wave single-pole single-throw (SPST) switch is shown in figure 3.1.

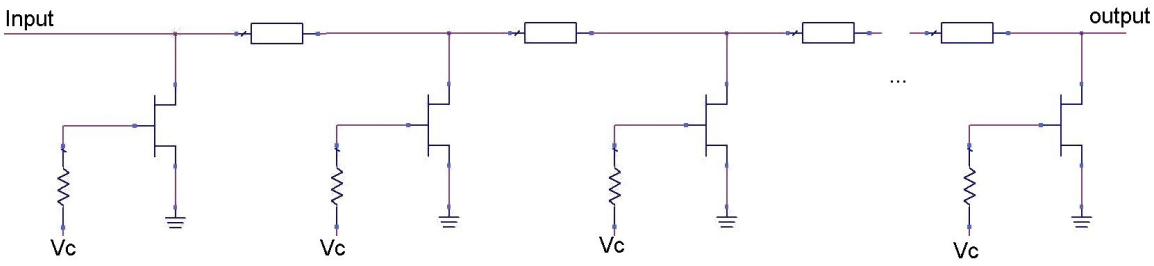

Figure 3.1: A travel1ing wave single-pole single-throw switch

The common-source FET passive small signal model is shown in figure 3.2. The values in the passive mHEMT device model can be obtained by curve fitting the equivalent passive small-signal model to the simulated S-parameters of the common-source FET with an open gate. However, this can be a very time consuming process and not necessary since only a few components dominate the performance of the FET. It has been shown in [18] that the small signal model can be drastically simplified for both operating states of the switch. The simplified models are shown in figure 3.3.

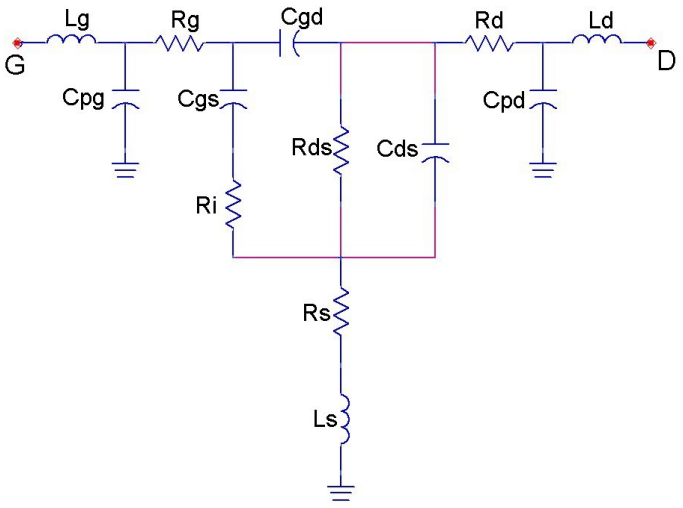

Figure 3.2: Small-signal model of a passive common source FET

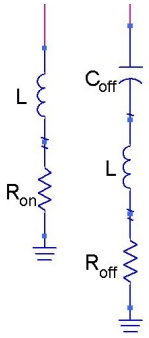

Figure 3.3: Simplified passive FET small-signal model when the switch is in the (a) On state and (b) Off state

The theory behind a traveling wave switch is based on the fact that the combination of the passive mHEMT models in combination with a transmission line, of certain characteristic impedance, shown in figure 3.1 between the FETs, can create a virtual 50 Ω transmission line. This means that when the mHEMT is biased in the off state the input and output of the switch will be connected via a virtual 50 Ω transmission line thus the signal could easily travel from the input to the output with

low loss. Conversely, when the FETs are biased in the on state a small shunt resistance, R_{on}, is present which prevents the signal from passing through, thus isolating the input from the output.

Since the SPDT switch is essentially a combination of two SPST switches the design process will first cover the design of a SPST switch. The first step in the design procedure was to obtain the values of L, R_{on}, C_{off}, R_{off} which make up the simplified passive models. To obtain these values an open gate FET was simulated from 0 to 50 GHz, when the FET was biased both on and off, respectively. The simplified models were then curve fit to the actual response of the open gate FET. An example of the curve fitting is shown for a typical gate width.

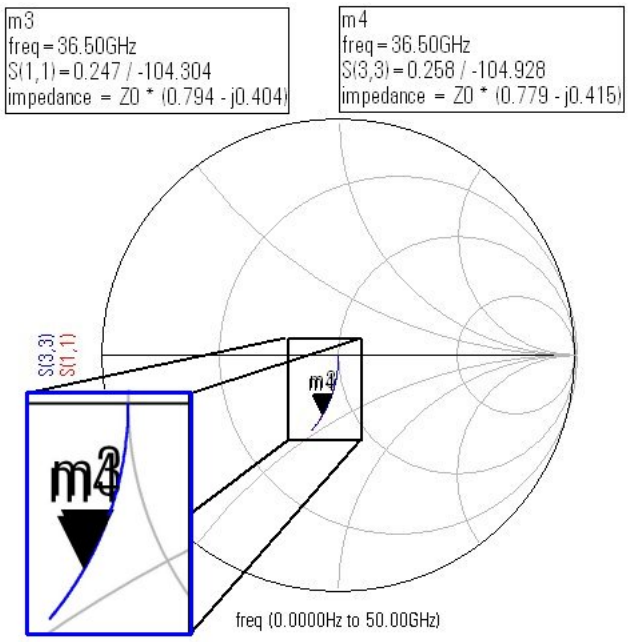

Figure 3.4: Curve fit match of simplified model to actual open gate FET

When the FET was biased in the on position the value of L was seen to be in the order of a few fH, while the value of R was a few Ω, therefore the "on" resistance was the most dominant value when the FET was biased on. When the FET was biased off, the inductance value L was again in the order of a few fH, the value of R_{off} was a few tenths of an Ω while the value of C_{off} was a few pF, then again from the simulations the value of C_{off} will be the dominant component when the FET is biased off. Based on these two simulations it can then be assumed that when the FET is biased on, the model can be thought of a shunt resistance equal to the R_{on}, and similarly when the FET is biased off the passive model can be equivalent to a shunt capacitor, C_{off}.

Once the passive models were obtained the next step in the design was to determine the characteristics of the transmission line between the FETs that could create the virtual 50 Ω transmission line when the FET is biased in the off state. From transmission line theory it is known that an ideal transmission line less than a quarter wavelength can be represented as a lumped element PI model, as shown in figure 3.5.

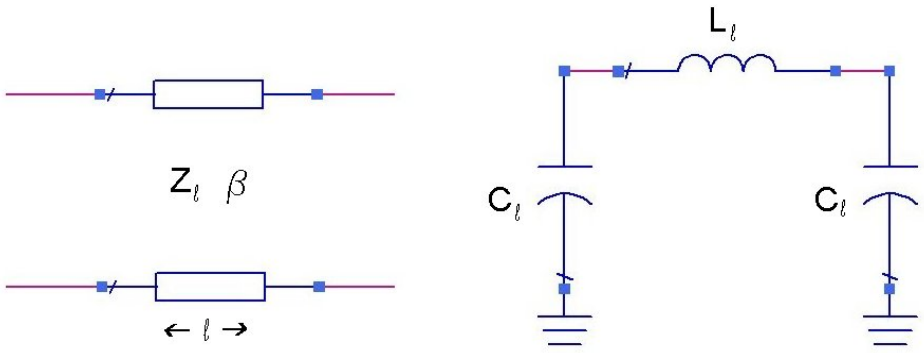

Figure 3.5: (a) Ideal transmission and its (b) PI model representation

In figure 3.5 the values of L_l and C_l are defined with equations 3.1 and 3.2

$$L_l = \frac{Z_l \sin(\beta l)}{\omega} \tag{3.1}$$

$$C_l = \frac{1}{\omega Z_l} \frac{1-\cos(\beta l)}{\sin(\beta l)} \tag{3.2}$$

Z_l is the characteristic impedance of the transmission line, β is the propagation constant and L_l is the physical length of the transmission line. In the critical condition when the FET is biased in the off state the model for the transmission line in combination with the simplified passive model of the FET results in figure 3.6

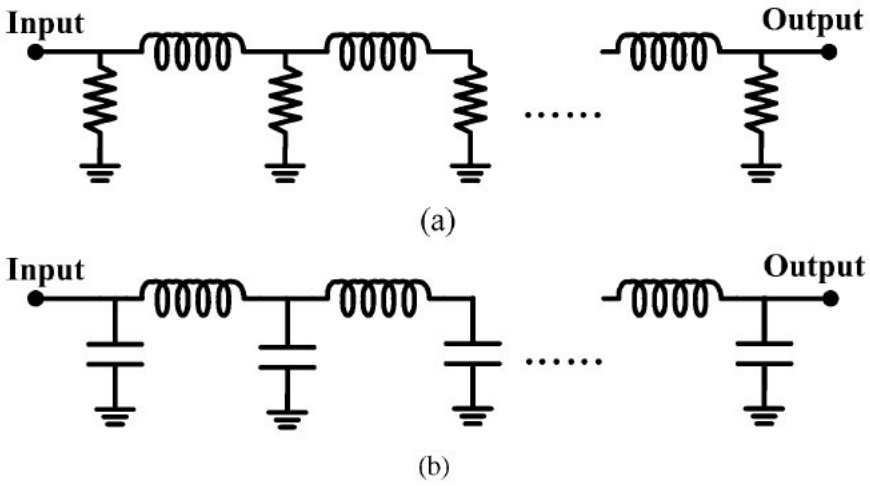

Figure 3.6: Passive model of SPST switch [19]

The shunt capacitance of the passive FET and the shunt capacitance of the transmission line join in parallel, and the total capacitance, C_t, can then be simplified to be equation 3.3.

$$C_t = C_{off} + 2C_l \tag{3.3}$$

The characteristic impedance of the virtual transmission line can then be calculated from

$$Z_0 = \sqrt{\frac{L_l}{C_t}} \tag{3.4}$$

Since the point is to have a 50 Ω transmission line the value that needs to be solved is that of Z_l, which is shown in equation 3.5.

$$Z_l = \frac{Z_0^2 \omega C_{off} + \sqrt{\left[Z_0^2 \omega C_{off}\right]^2 - 8\left[Z_0^2 \cos(\beta l) - Z_0^2\right]}}{2\sin(\beta l)} \tag{3.5}$$

The characteristic impedance of the transmission line used between the FETs can then be calculated using equation (3.5) since all the values are known.

The length of the minimum size transmission line was limited by the minimum via size available in the process, since the FETs would be side by side. It was found in [19] that in traveling wave switches the smaller the transmission between the FETS was the broader the bandwidth of the FET; however the insertion loss also begins to degrade from optimum at higher frequencies as the transmission line becomes larger. Therefore, the minimum design length was chosen based on the smallest vias available in this process. Since the goal was to design a very low insertion loss switch the appropriate gate width was selected to provide the lowest insertion loss, which means a small gate

width <100 um was selected. The small gate width does not provide the best isolation performance because it has larger on state resistance compared to a larger gate transistor. However, it is preferable because it has less insertion loss because it has low off state capacitance. The isolation of the switch can be improved in other ways, for example by increasing the number of shunt FETs that are used. This is because more FETs create more equivalent shunt resistors that can terminate the signal, three FETs were selected for this design because they provided adequate isolation greater than 25 dB while not consuming more chip area.

Finally, the two SPST switches were ready to be combined to form the SPDT switch. Each arm is independently biased although only one arm should be biased in the off state at a time while the other arm should be biased in the on state. Each arm must be isolated from the other and two possible options can be implemented to perform this operation, the first possible implementation is by using series FETs to connect both arms. This method is shown in figure 3.7.

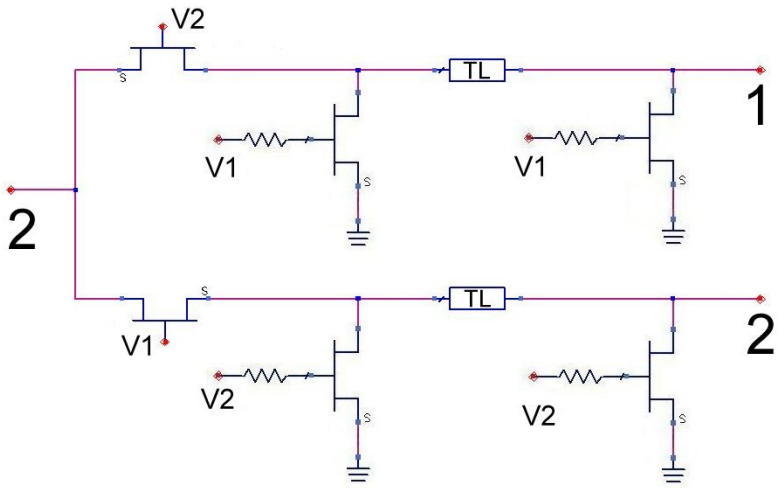

Figure 3.7: SPDT switch implementation using series FETs to provide isolation between the output and the switch arm turned off

With this design the bandwidth of the switch can be increased since the series FET allows for frequencies to go down to DC. The concept works by biasing the series FET in the on arm with the same bias as the shunt FETs on the off arm that is the on arm will have a series resistance between its input and the output of the switch. The off arm will have an FET that can be approximated as an open thus isolating it from the rest of the circuit. However, the improved isolation comes at an expense of insertion loss.

The second option is to use quarter wave transformers. When the two switch arms are connected with quarter wave transformers that have a $50\,\Omega$ characteristic impedance, the arm biased "on" will be the virtual $50\,\Omega$ transmission line and the signal will pass from the input to the output of the switch without any significant insertion loss. However, since the switch arm biased "off" can be approximated as being as a short circuit then the quarter wave transformer transforms the short circuit to

circuit thus providing isolation between both switch arms. The SPDT implemented with quarter wave transformers is shown in figure 3.8.

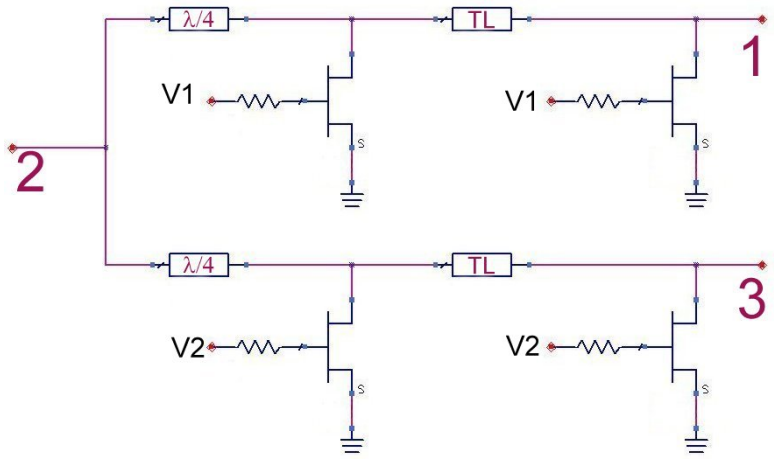

Figure 3.8: SPDT switch implementation using quarter wave transformers to provide isolation between the output and the switch arm turned off

Although the amount of wafer space used would be lower with a series FET, the quarter wave transformer was used because it would provide less insertion loss, which is one of the critical needs of this design.

3.1.2 Simulation Results

The ideal transmission lines were replaced with lossy transmission lines the SPST switch was simulated. Both the on and off states were simulated. Figure 3.9 displays the insertion loss, while figure 3.10 displays the isolation of the switch, both figures also display the input and output return loss during each state.

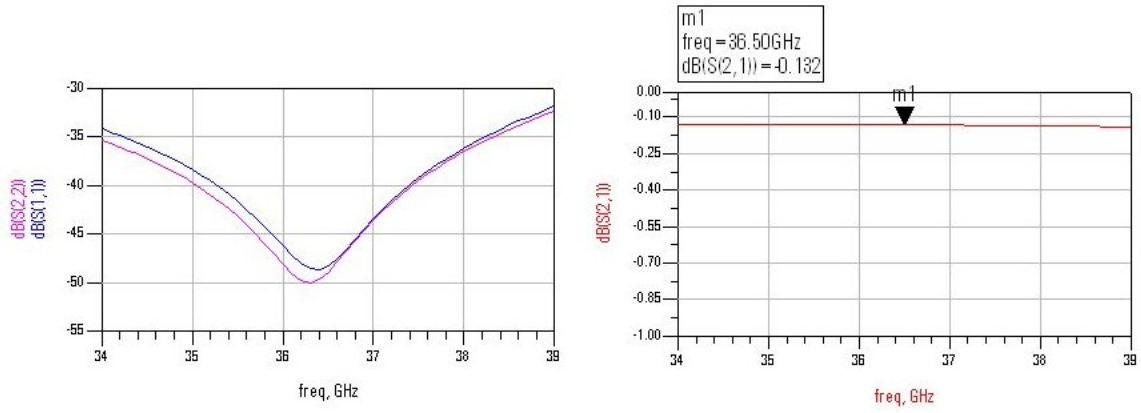

Figure 3.9: Simulated S parameters of the SPST switch in the off position

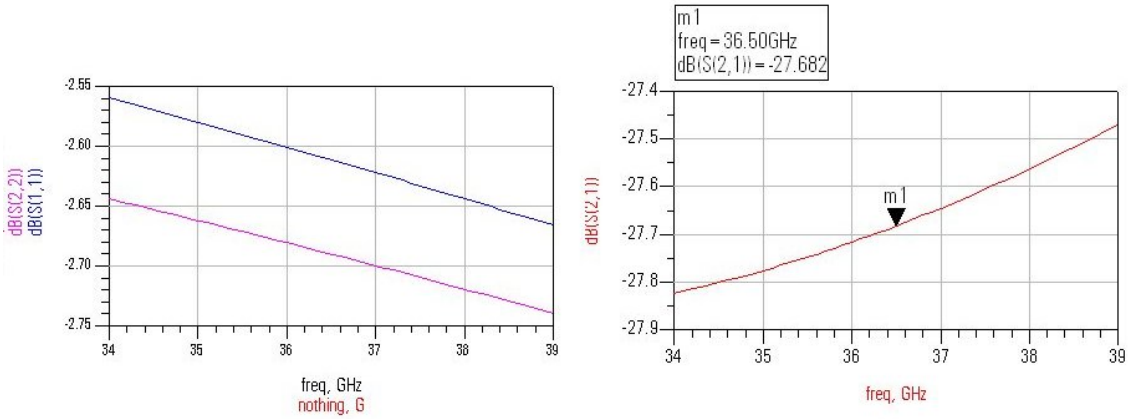

Figure 3.10: Simulated S parameters of the SPST switch in the on position

Additionally, using quarter wave transformers the SPDT switch was simulated and that simulation is shown in figure 3.11.

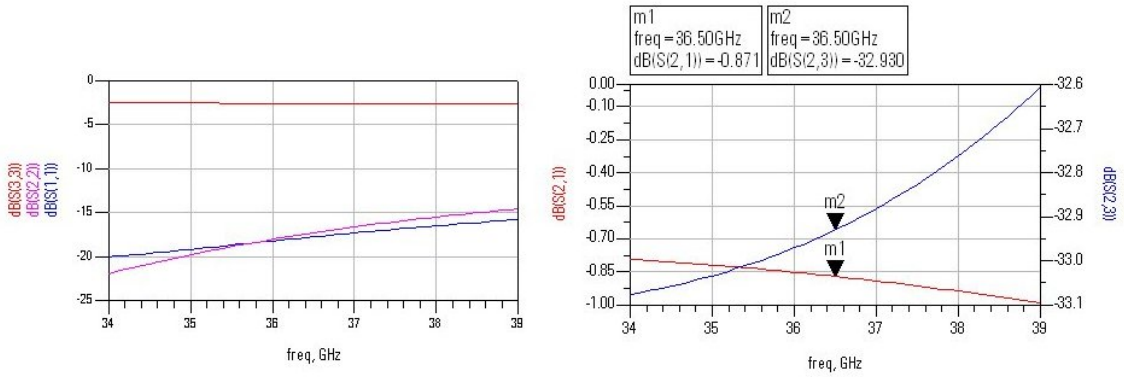

Figure 3.11: Simulated S parameters of the SPDT switch

As can be seen from figure 3.9 the insertion loss is 0.132 dB with an input and output return loss under 45 dB at the design frequency. From figure 3.10, it can be seen that the isolation is around 27.7 dB and the input and output return loss are above 3 dB which is appropriate in this case because of the isolation between the input and output. When the two SPST switches are combined using quarter wave transformers the insertions loss increases to 0.871 dB, but the isolation increases to around 33 dB. The input and output return loss of the critical ports is below 15 dB, and around 3 dB at the isolated port.

3.2 Low Noise Amplifier

Low noise amplifiers typically need to have enough gain to overcome the noise of the following stages in a system. Usually stand alone MMIC LNAs are designed with gain stages, which means FETs. Multiple gain stages are needed to obtain enough gain upwards of 20 to 30 dB. The first stage usually has only enough gain to set the noise

figure of the amplifier because it is usually designed with enough source degeneration to obtain an optimum input match and noise figure, and the second and possibly third stages are designed to provide higher gain. However, due to limited chip size only one stage was used for this design. Therefore a good balance between maximum gain and minimum noise must be met with just one FET.

3.2.1 Design Technique

The one stage low noise amplifier will consist of an FET and an input and output matching network. The input matching network can serve to match the FET for optimal input match or for optimum noise, while the second matching network is usually designed to match for optimum gain and output match. To achieve a good input match the source reflection coefficient must be equal to the conjugate of the input reflection coefficient. However, to obtain optimum noise performance the conjugate of the input reflection coefficient must be equal to Γ_{opt}. Figure 3.12 shows a typical single stage amplifier design with input and output matching networks.

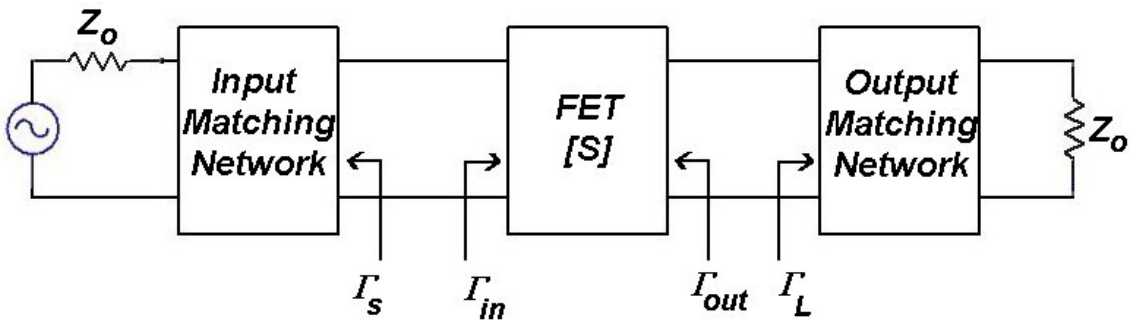

Figure 3.12: Typical one stage amplifier design with input and output matching networks

A tradeoff between input match and optimum noise figure usually has to be made. However, as previously mentioned there is a way to obtain both input match and optimum noise, thus having $\Gamma_{in} = \Gamma_{opt}$, Γ_S. However, this requires a specific value of Γ_L which sometimes is unrealizable. As mentioned in the previous chapter source degeneration can be used to achieve both an input match and optimum noise, however, it comes at a cost to gain. The first step in this design is to add enough source inductance to allow an easy implementation of the design. A tradeoff must still occur because the more source inductance that is added to the FET the less gain the LNA will be able to have. Therefore, a few simulations were performed until a good tradeoff was obtained. As mentioned previously the more inductance introduced to the design increases the negative feedback and thus decreases the gain, since this design will be a single stage design it is unrealistic to utilize the optimum source inductance. Additionally, at this frequency it is not viable to fully implement the needed inductance using on chip transmission lines since it would require long transmission lines in order of hundreds of microns.

Another consideration in the design was determining the gate width. In this case the tradeoff is between noise and linearity. Selecting a small gate width would aid the goal of having a low noise figure since the gate width is proportional to the current noise source. Similarly, the gate width is proportional to the transconductance and inversely proportional to drain source resistance, thus having an FET with a larger gate width would result in a better linearity. The larger gate width produces improved linearity because the width of the FET is proportional to gm and inversely proportional

to the drain source resistance. Additionally, unlike noise figure, in a multi-stage LNA the last stage dominates linearity, and since this design is a single stage design both the linearity and noise figure of the LNA were factors in determining the proper gate width, with preference given to noise figure.

The most critical part of any amplifier is stability. If the transistor is not unconditionally stable a possibility exists that the amplifier will oscillate and make the amplifier useless. The amplifier does not only need to be stable within its operating bandwidth but also at all frequencies. Typically, the stability of a two port device can be tested by using the "k" factor. A circuit is typically unconditionally stable when k >1 and $|\Delta| < 1$ where k is defined in equation 3.6, and Δ is defined in equation 3.7.

$$k \equiv \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \tag{3.6}$$

$$\Delta \equiv S_{11}S_{22} - S_{21}S_{12} \tag{3.7}$$

If the "k" factor test is satisfied at all frequencies then the two port device may be considered unconditionally stable. However, this is not a sufficient stability test for complicated circuits but it is reasonable for a one device amplifier, like the one designed in this project [30].

The next and critical important step is making the FET unconditionally stable. Several methods can be implemented to accomplish this; the method chosen for this design was using a shunt resistor at the input of the FET, this can be seen in figure 3.13. The shunt resistor helps provide stability at DC. Various resistor values were simulated until the FET was unconditionally stable. Once unconditionally stable, any passive matching networks may be designed without causing the amplifier to oscillate.

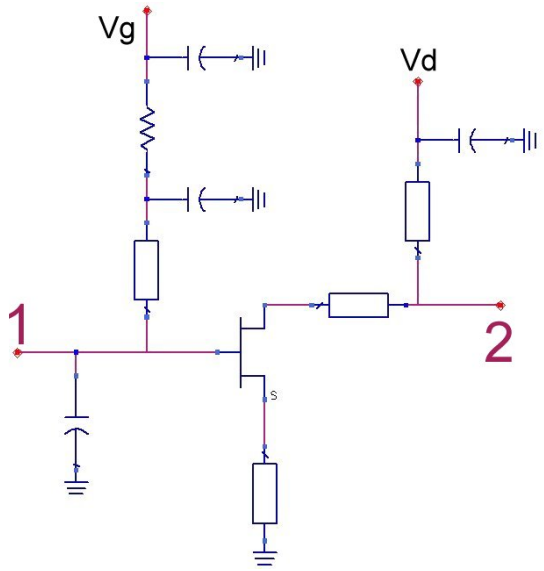

Figure 3.13: Generalized LNA circuit schematic

The following step involved the design of the biasing feeds. A common way to efficiently design the bias feeds of the amplifier is by embedding it with a matching network. The ADS model used included bias condition options, which meant the FET model required a gate and drain voltage. An example of how one can combine the biasing with one of the matching networks is feeding the gate voltage thru a shunt transmission line that can also be part of the input matching network. Similarly, the

drain voltage can also be fed into the FET using a shunt transmission line, this implementation is shown in figure 3.13.

Finally, the input and output matching networks were designed. The input matching network was chosen to provide optimum noise, however, the source degeneration allowed for a simultaneous input matching and for optimum noise match. A shunt transmission line in combination of series capacitor was used to provide a good match. The output matching network was then designed to provide optimum output match, based on the previous calculated Gamma L. Output impedance matching was provided with the shunt transmission line, that also feeds the bias, and a series transmission line after the FET but before the shunt transmission line. Finally, once the matching networks were designed, the stability was verified once again by making sure the stability factor was greater than unity and the stability measure was positive for all frequencies.

3.2.2 LNA Simulation Results

The Simulated S parameters of the LNA are shown in figure 3.14-3.15. Figure 3.14 displays the gain and the input and output return loss, while figure 3.15 plots the noise figure of the LNA.

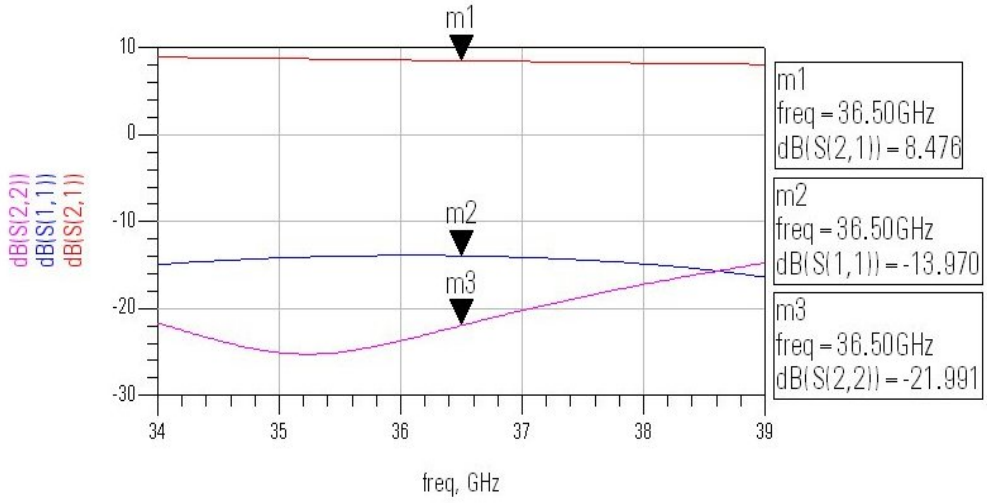

Figure 3.14: Simulated Gain and input and output return loss of the LNA

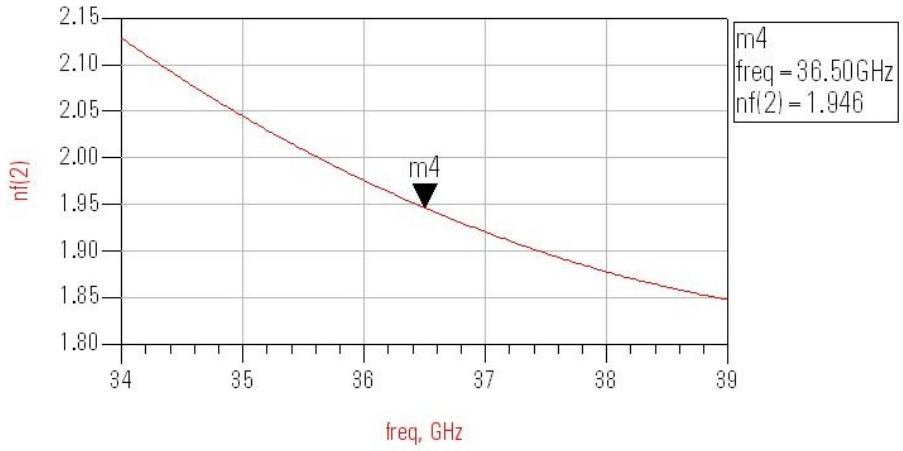

Figure 3.15: Simulated Noise Figure of the LNA

As can be seen in Figure 3.14, the gain of the LNA is around 8 dB while the input return loss is 14 dB, and the output return loss is 22 dB. The noise figure of the LNA, shown in figure 3.15, was simulated to be 1.9 dB at 36.5 GHz.

3.3 Switch and LNA Combination

Once the low noise amplifier and switch were individually designed they were combined and their performance was simulated. The input matching network of the LNA was redesigned to match to the output impedance of the switch, so that minimal reflections would occur between them. During the design process, it was found that the output impedance of the switch was not 50 Ω, but rather 33 Ω. Time limitations did not allow for an investigation into the impedance shift before the LNA could be designed so it was found to be easier to just redesign the input matching network of the LNA. Once the full design was completed, due to time constraints, the switch was corrected to have an output impedance of 50 Ω for the breakout piece, with minimal change in isolation and return loss performance. When the complete switch and LNA circuit were finalized and merged the stability was again verified for the complete circuit. However, since stability analysis on ADS can only be performed on a two port network the unused input port of the switch was replaced with a 50 Ω resistor.

3.3.1 Switch and LNA Combination Simulation Results

The simulation results of the switch LNA combination are shown in figures 3.16 thru 3.19. The Gain and Return loss is shown in figure 3.16, when the switch is in the off state and in figure 3.18 when the switch is in the on state, respectfully. The noise figure is plotted in figure 3.17 when the MMIC is passing the signal, and in figure 3.19 when the MMIC is isolating the signal.

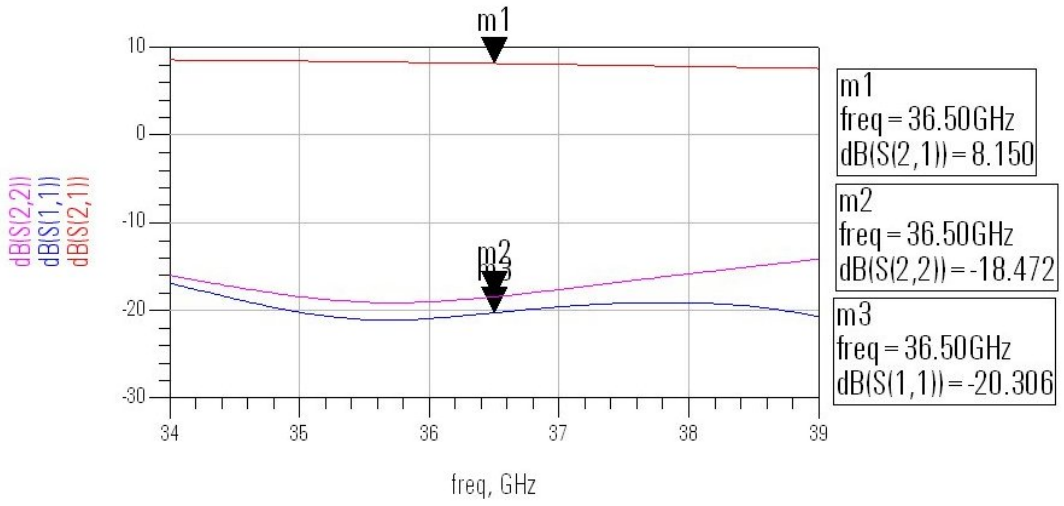

Figure 3.16: Switch-LNA S parameter simulations when the mHEMTs are biased in the off state

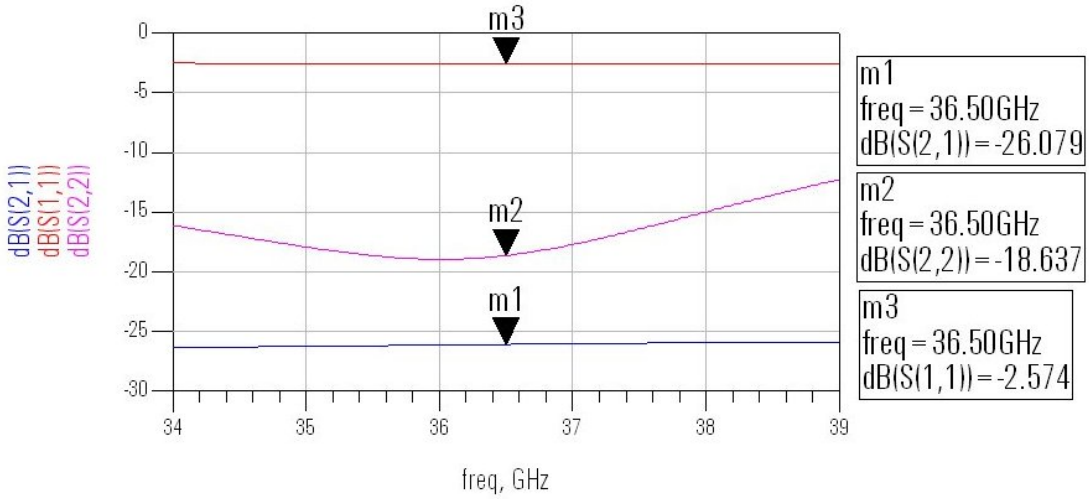

Figure 3.17: Switch LNA S parameter simulations when the mHEMTs are biased in the on state

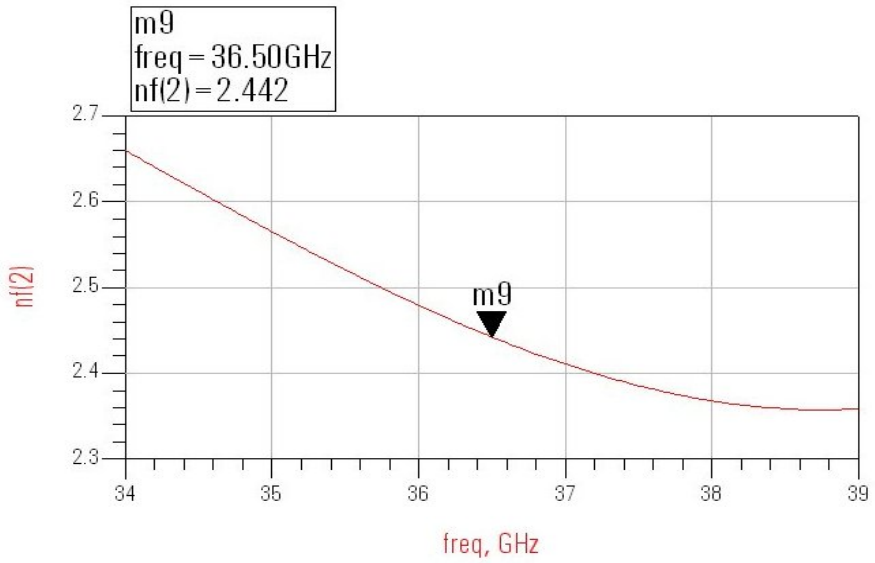

Figure 3.18: Switch-LNA noise figure simulations when the switch is biased in the off state

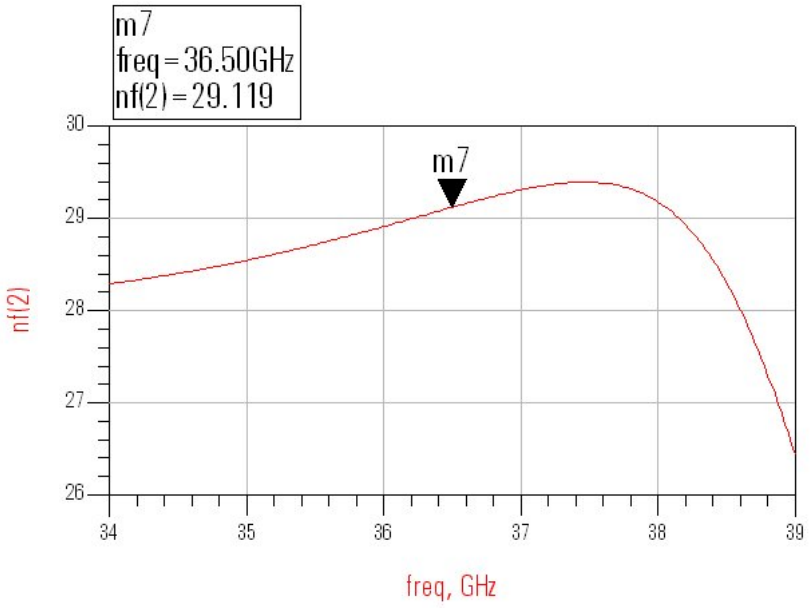

Figure 3.19: Switch LNA noise figure simulations when the switch is biased in the on state

As can be seen from figure 3.16, the gain of the switch and LNA combination is approximately 8.5 dB at 36.5 GHz during transmission. From Figure 3.17 the isolation was simulated to be -26 dB. The input and output return loss was below 18 dB. The simulated noise figure was 2.4 dB when the signal is being passed thru the switch and 29.1 dB when the input signal was isolated from the output of the switch.

3.4 Temperature Modeling/Simulations

The small signal model of the FET was obtained by using the FET models provided by Raytheon. The typical small signal model of HEMT is as shown in figure 3.20.

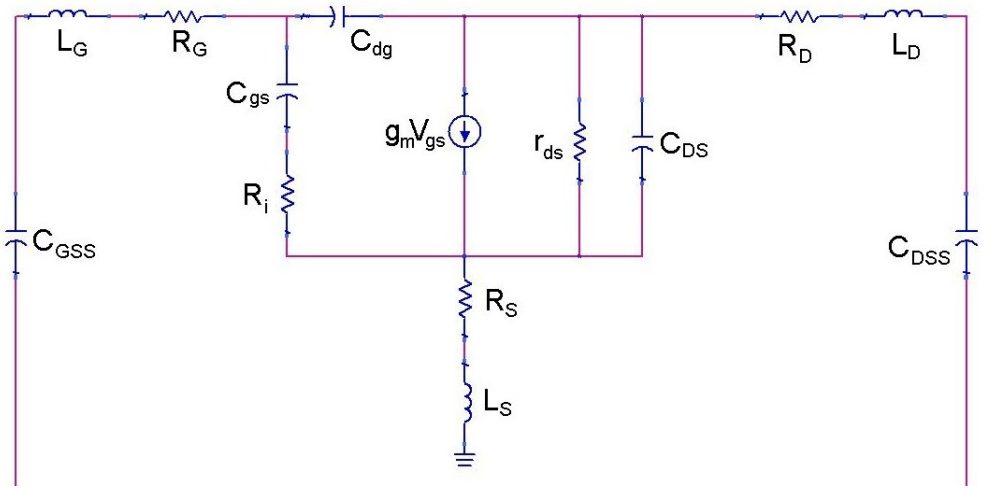

Figure 3.20: Typical small signal model of mHEMT FET

As mentioned in the previous chapter the goal was to simulate the gain and noise variations that occur due to temperature. Since it is possible to simulate the effect of temperature of passive components in ADS simply by changing the simulation temperature, the variations of the active components with temperature were needed. The FET small signal model in ADS was implemented using a table based model that included equations for each component as a function of bias, gate width, and number of fingers. The values were valid at a temperature of 25 $^{\circ}C$, therefore the first step was to calculate the values of each component at 25 $^{\circ}C$ to verify the model for simulation.

The next step was to simulate the model versus temperature. The values of gm used in this thesis were obtained from temperature measurements that were previously performed by William Clausen of Monolithics. He provided small signal equivalent circuit parameters (ECPs) at three different temperatures, namely -55, 25 and 85 $^{\circ}C$, respectively. However, since the measured data was obtained on an mHEMT that had a different size gate width, the values of measured gm that had the same current density as the mHEMT that was used in this thesis were used. A plot of gm versus temperature was created in order to obtain a theoretical relationship between gm and temperature. This plot is shown in figure 3.21.

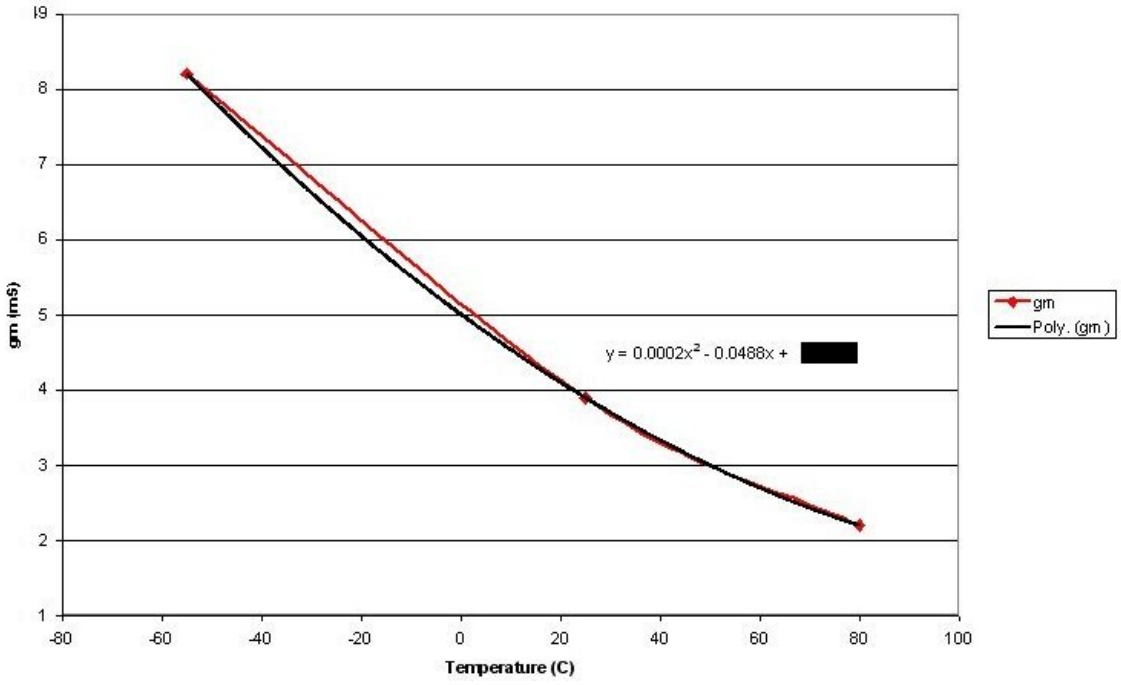

Figure 3.21: gm versus temperature curve fit

Based on the three values of gm recorded a second order polynomial equation best curve fit to the plot. Additionally, a polynomial fit was chosen because previous papers have published that gm has a second order polynomial relationship versus temperature [31]. Since a value of gm was known at 25 $^{\circ}C$ for both the measured gm and the modeled gm the relationship given by the polynomial equation was scaled which allowed for an estimation of gm at practically any temperature between -55 $^{\circ}C$ to 85 $^{\circ}C$.

The main reason for observing these temperature variations was to determine how well the LNA can track with temperature. This temperature variation was determined by creating a fixed gain difference between both input switch arms. A

variation in gain was created by including an impedance mismatch at one of the input arms. The gain variation of 0.1 dB was selected and it was obtained when the impedance of one of the arms was lowered while the other arm remained at an impedance of 50 Ω. The values of gm were then calculated at typical radiometer measurement temperatures of 30 and 35 $^{\circ}C$. The value of gm were obtained from the polynomial approximation and then plugged into the ADS signal model. The ADS simulation temperature was then changed to the desired temperature. The gain was first measured for the straight input arm, and then for the 90 degree switch arm. The difference in gain was then noted, and this procedure was followed at the other two temperatures.

Once this value is known, it can be used to calculate the sensitivity of the radiometer, as shown in equation 2.9. The variable T_{SYS} is equal to the brightness temperature and the temperature of the antenna and the noise temperature, the value G was approximated to be the gain of the system, or 90 dB. A plot showing the sensitivity of the radiometer is shown in figure 3.22. The values of sensitivity are normalized to an ambient temperature of 25 C.

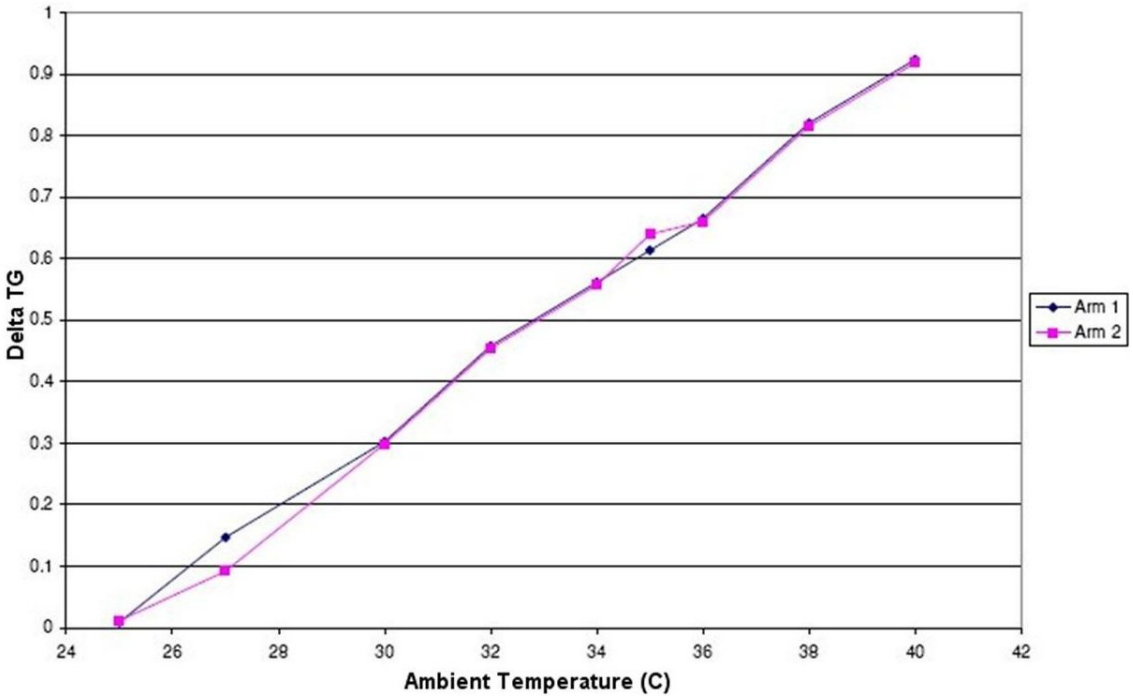

Figure 3.22: Calculated Delta TG as a function of ambient Temperature

CHAPTER 4

LAYOUT

In this chapter the layout of both MMIC chips will be discussed. Chapter 4.1 will discuss the layout and process considerations that were examined throughout the layout of the MMIC design. Chapter 4.2 will discuss the design and layout constraints of the switch and LNA. Finally, Chapter 4.4 will discuss the final layout designs of switch and LNA combination and its simulation performance.

4.1 Process and Layout Considerations

When designing high frequency integrated circuits one of the challenges that can quickly degrade a design is the limitations of the process and transmission line discontinuities that typically add loss. After the switch and LNA circuits were designed, the next step was to decide how to implement them using the process rules provided by Raytheon in the process design guide. Among the effects that are usually ignored when beginning a design are the simple connections between components. For example in the switch design, the connection between the drain of the FET and the main transmission line path is represented by “wires” on ADS in the schematic window. However, in reality this connection is made with a series of additional transmission lines. It is important however that these transmission lines not considerably affect the ideal design of the circuit at this frequency even small transmission lines or transmission line

transitions can degrade the performance of the circuits, this is not as common at lower frequencies. The layout comparison is shown below:

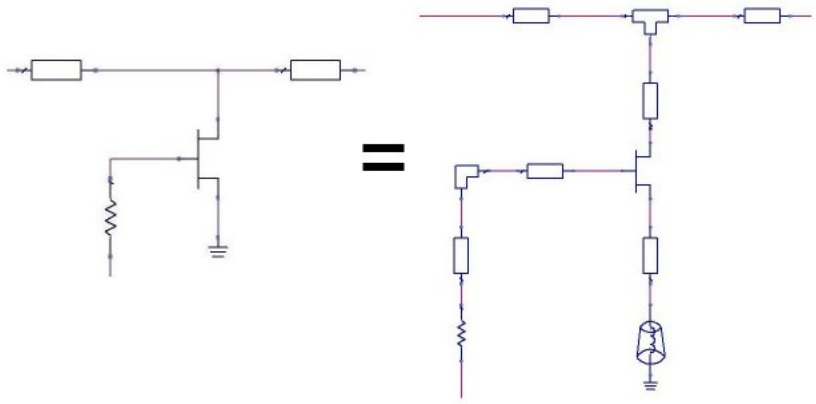

Figure 4.1: Figure of idealized FET connections versus realistic transmission line FET connections

Another limitation placed on the design is the size of chip area available; this often forces a designer to shape the circuit into an odd arrangement to be able to meet the available space requirement. This can cause the circuit to not be easily inspected visually. This requirement also compels the designer to move every circuit component close together, however, consideration of possible coupling between transmission lines, vias, and other components must always be made.

4.2 Switch Design with Layout Considerations

The most difficult layout constraint with the switch design arose from the position of the input arms. The goal was to have one input arm be aligned with the

output while the other arm should be at a 90 degree angle relative to the output. The reasoning behind this layout was based on a current implementation of a switch in a MMIC radiometer. An additional challenge involving the layout of the switch was the interconnecting components that were not taken into account in the ideal schematic design. This is critical because at Ka band frequencies the effect of small transmission lines would be large and therefore be appropriately modeled in ADS throughout most phases of the design.

Additionally, while the circuit was laid out particular consideration was paid to the minimum transmission line widths and the minimum separation between them and other devices using other layers in the circuit. Among the most important was the required separation between a via hole and a transmission line made of the top metal layer. This was an important design rule because it helped determine the size of the small transmission line that would be used to connect the drain of the FET to the main signal transmission line. Additionally, via holes and not just an ideal ground were placed to ground the source of the FET, this has some effects on the electrical performance since the via contains some inductance.

An additional challenge was the need to connect the closest FET to the output to the quarter wave transformer. This could have been done using various discontinuities but a taper was chosen to minimize the effect of the discontinuity that occurs when two transmission lines of different widths are joined. Due to the process minimum spacing design rules a small transmission line also had to be placed in between the taper and the

FET. This was because the taper would otherwise physically collide with the FET. This connecting transmission line was a problem because it could cause the artificial transmission to no longer have a characteristic impedance of 50 ohms. Another aspect that was observed is the possibility of coupling between some of the components so they were placed a certain distance longer than the minimal width and momentum simulations were performed when needed to assume no unneeded coupling occurred.

So that it could be appropriately placed in the final radiometer system, the main consideration was the electrical performance of the switch, with one arm having to turn 90 degrees that meant that the insertion loss of this arm would not be the same as the other arm. The amount of chip space that this junction will consume remains a consideration as well. A few simulations were performed to compare the effect on insertion loss, and its agreement to the other switch arm, since ideally they should be about equal.

Additionally the 90degree arm caused a problem because the 90 degree bend input presents a different impedance to the output of the switch than the straight input arm. This is critical since this is the impedance than by the LNA amplifier input. This transmission line discontinuity is critical and therefore a simple 90 degree bend was not implemented. The affect of the discontinuity can be minimized by implementing it with a swept bend, but this comes at a cost of chip space, it can also be implemented using a mitered bend. The mitered bend reduces the excess capacitance that can cause phase and mismatching errors. The problem was then to minimize the impedance and phase

difference that can occur due to both input arms not being physically the same. Simulations were performed so that there would be minimal difference in terms of impedance and s-parameters between both arms. These results are shown in chapter 4.2.1.

Another aspect that had to be addressed was the biasing. Each transistor within each arm can be biased independently where each transistor could have its own bias pad and each pad could have been wire bonded to a shared off-chip resistor, or an individual resistor. However, this would have complicated the wire bonding process since the resistor pad is not very large and using individual resistors would have created an available space issue and would have also required additional bias probes. Therefore a bias feed was created on chip. This bias feed tied all gate inputs to the same bias pad which was then wire bonded to the off-chip resistor. Since the gate of the switch transistors were modeled to be open circuits, careful attention was paid to not transform that impedance or create a short. The bias pads for each switch arm were placed on opposite sides of the chip.

4.2.1 Simulation Results

The final SPDT switch was then optimized and simulated. The circuit diagram of the SPDT switch is shown in figure 4.2. The S-parameter simulations are shown in figures 4.3 thru 4.6. Figure 4.3 and 4.4 display the insertion loss and the input and

output return loss, and figures 4.5 and 4.6 display the isolation and the corresponding input and output return loss.

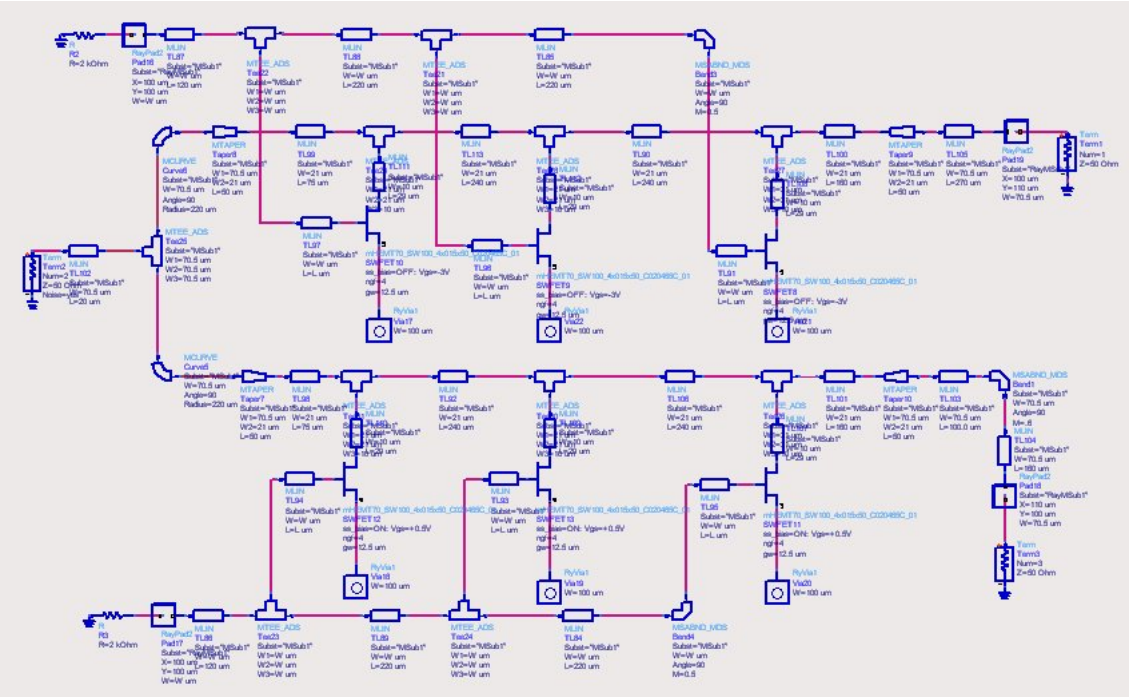

Figure 4.2: Circuit Schematic of Final SPDT switch

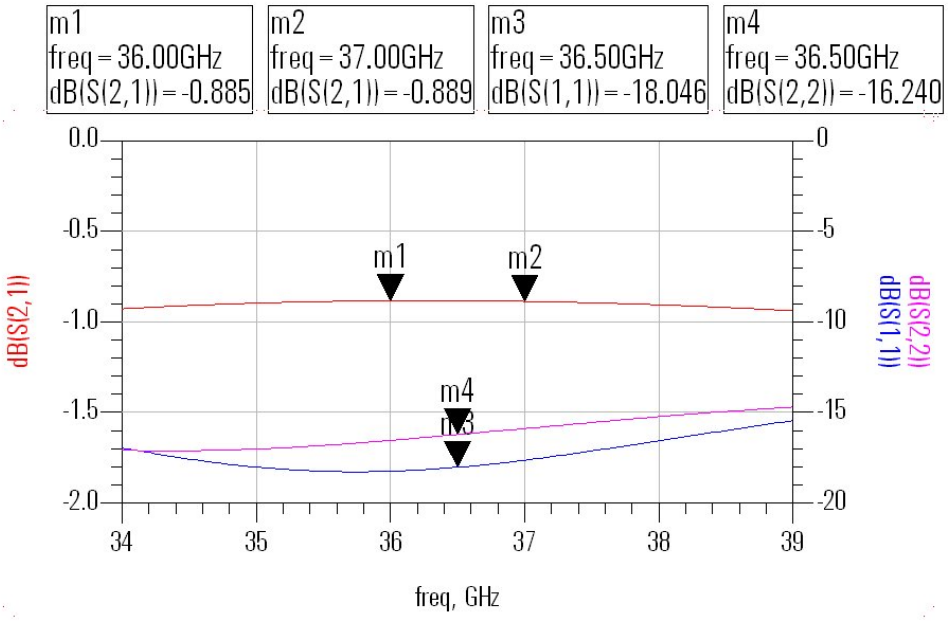

Figure 4.3: Insertion loss and input/output return loss simulation of SPDT switch when straight arm is biased off, and the 90 Deg bend arm is biased on

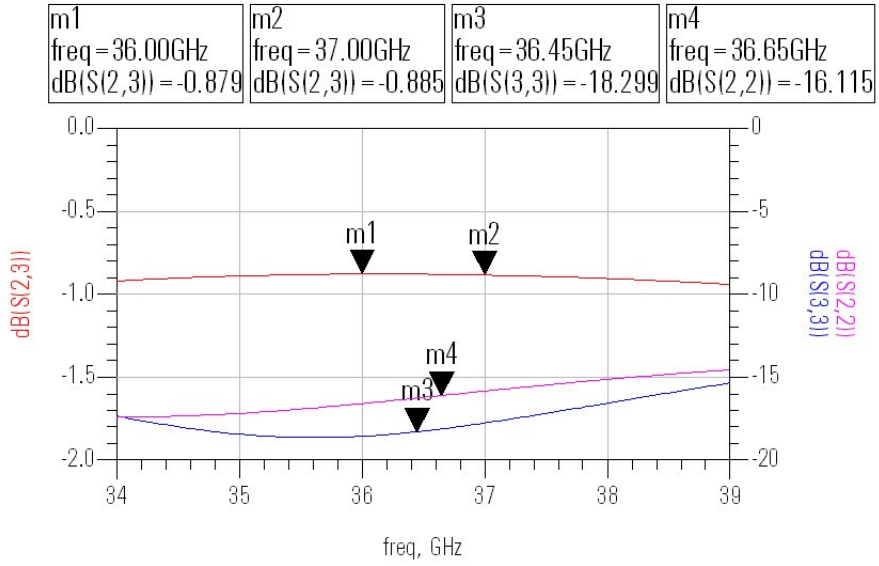

Figure 4.4: Insertion loss and input/output return loss simulation of SPDT switch when 90 Deg bend arm is biased off, and the straight arm is biased on

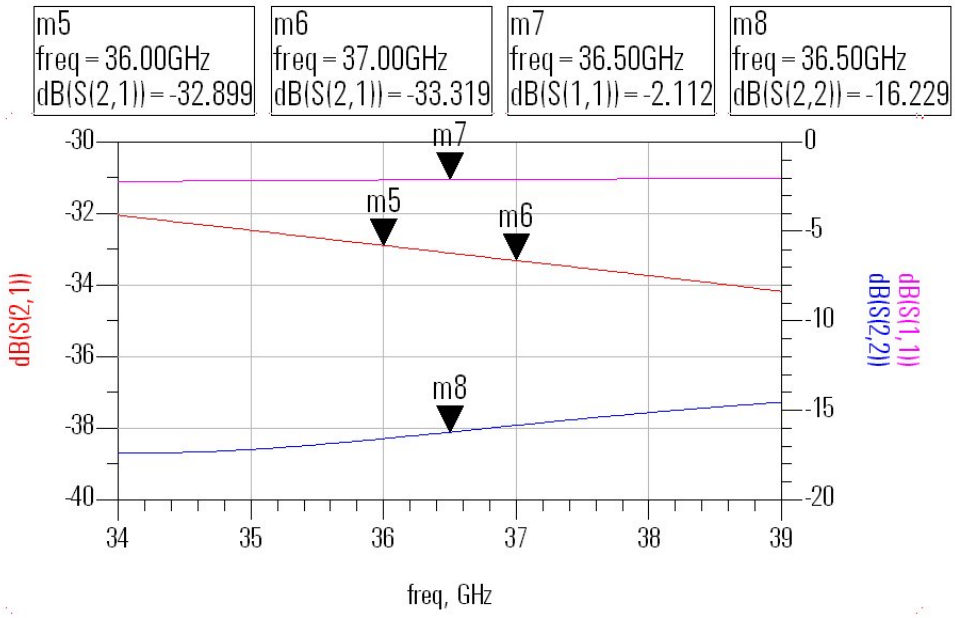

Figure 4.5: Isolation and input/output return loss simulation of SPDT switch when straight arm is biased on, and the 90 Deg bend arm is biased off

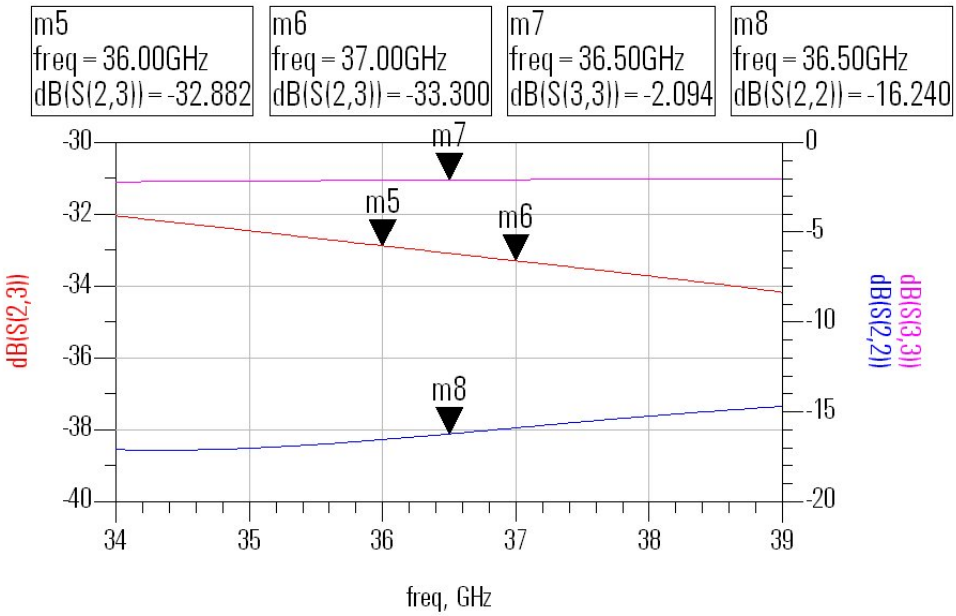

Figure 4.6: Isolation and input/output return loss simulation of SPDT switch when 90 Deg bend arm is biased on, and the straight arm is biased off

As can be seen from figures 4.3-4.6 both input arms of the switch produce a nearly identical response. The insertion loss is 0.9 dB, and the isolation is around 33 dB. Both the input and output return loss is below 15 dB. A summary of the simulated results is shown in table 4.1

Table 4.1: Simulated results for SPDT switch

	Insertion Loss		Isolation	
	36 GHz	37 GHz	36 GHz	37 GHz
	dB			
Straight Arm	0.885	0.889	-32.889	-33.319
90 Deg Arm	0.879	0.885	-32.882	-33.300

4.2.1 Switch Layout

The layout of the switch is shown in figure 4.7, the size of the chip is 0.9 mm x 1.7 mm, which is smaller compared to other MMIC switches designed using quarter wave transformers and comparable to those using series FETs [18]-[19]. The RF pads were designed to have a 150 micron pitch to coincide with the GGB probes available in LAMMDA lab.

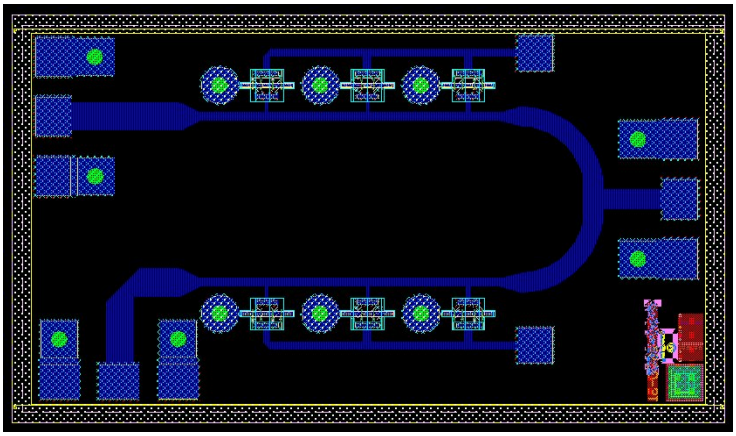

Figure 4.7: Layout of the SPDT Switch

4.3 Switch-LNA Layout Considerations

The layout of the switch-LNA posed more challenges than the switch because of the common integrated circuit design rules rule that gates of all FETs must all align. Since there were more FETs in the switch they were laid out in a way that allowed them to be easily biased and connected to the main signal path. Unfortunately, this meant the FET in the LNA was rotated 90 degrees, with the gate fingers parallel to the switch FETs. This is shown in the layout of the switch-LNA figure 4.8.

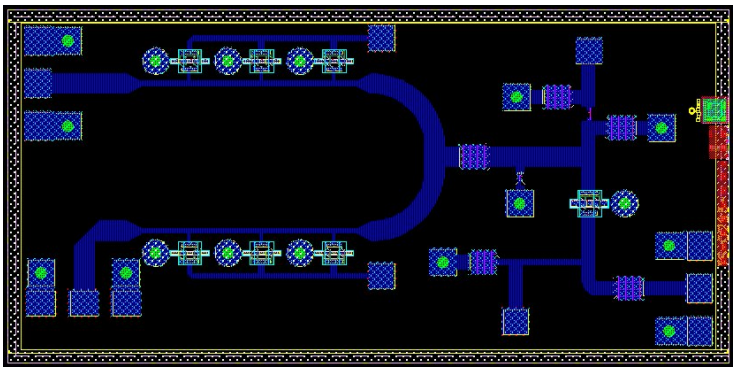

Figure 4.8: Layout of the Switch-LNA MMIC combination

In addition, as can been seen in figure 4.7, since the RF output had to remain aligned with the input another discontinuity had to be placed after the LNA FET. The gate and drain bias pads were placed on opposite ends of the chip and in line with the switch bias points. The transitions used for the input curve was a T junction, connecting to the FET, the drain bias, and to the output, respectively. On the output side, a bias tee approach was used to both match and isolate the RF and bias signals. After the LNA FET a large transmission line is used followed by a 90 degree swept curve was used, though this transition takes up the most chip space its performance is critical and thus preferred in this case. DC blocking capacitors were also placed in the input and output of the LNA circuit, the purpose of DC blocking capacitor between the switch and the LNA was to prevent the DC bias from interfering with the biased switch FETs.

4.3.1 Simulation Results

The combination SPDT switch and LNA schematic is shown in figure 4.9. The inputs of the chip are of the switch and the output is the output of the LNA. This complete circuit was simulated and the resulting s-parameters and noise figure are shown in figure 4.10-4.15. Figures 4.10 and 4.11 show the gain and the input and output return loss of both switch arm inputs, while 4.12 and 4.13 show the isolation obtained from both switch arm inputs. Figures 4.14 and 4.15 show the respective noise figure obtained from each switch arm input.

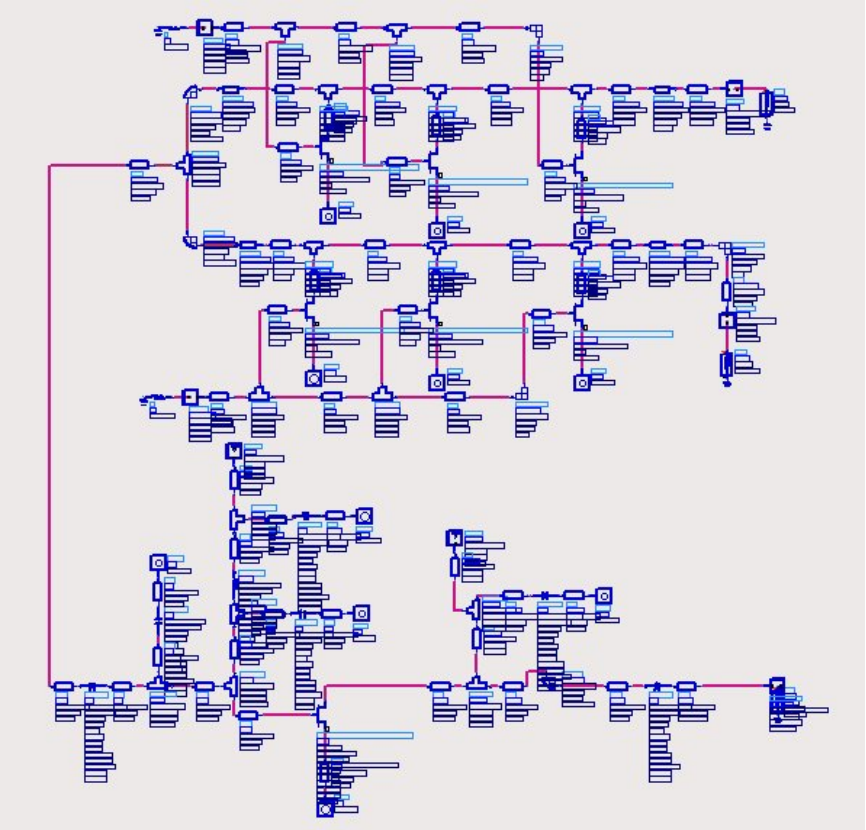

Figure 4.9: Circuit schematic of SPDT switch-LNA combination

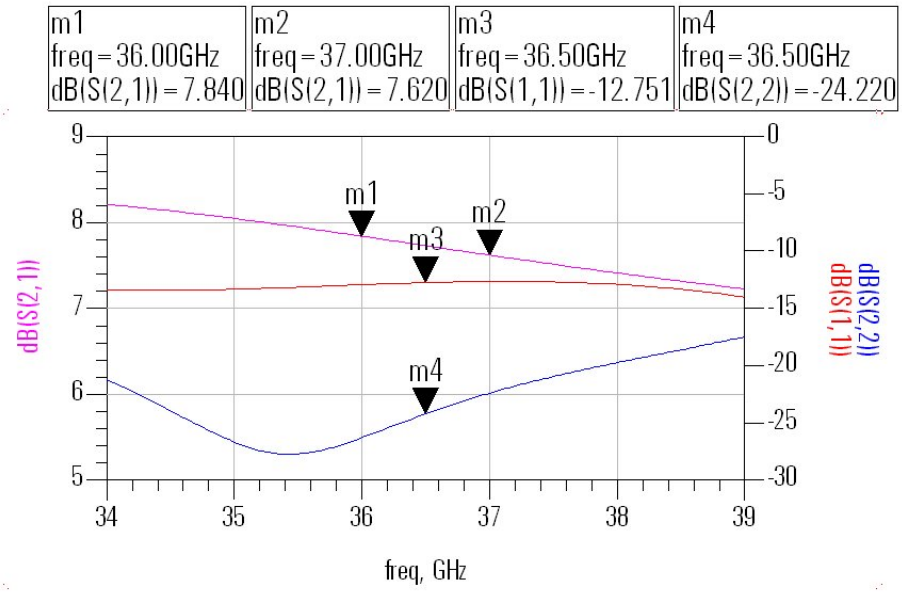

Figure 4.10: Gain and input/output return loss of switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

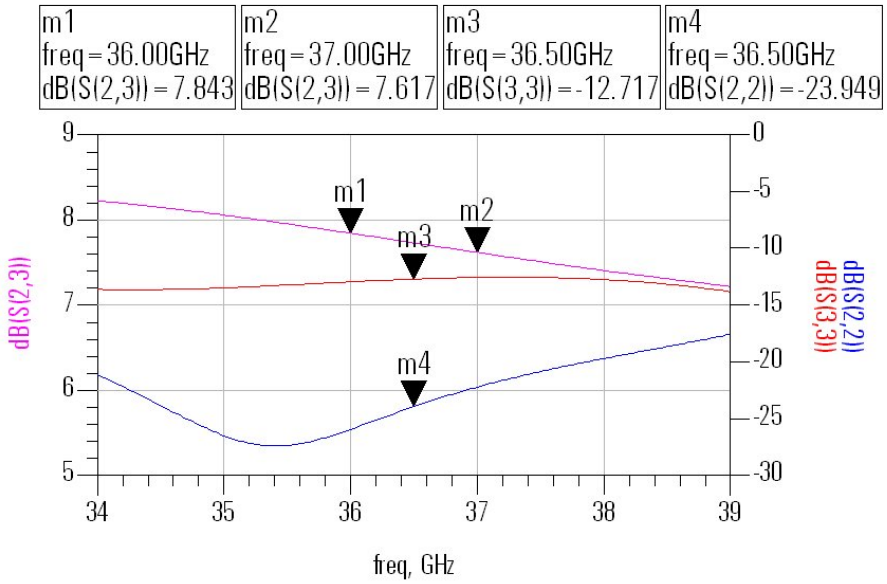

Figure 4.11: Gain and input/output return loss of switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

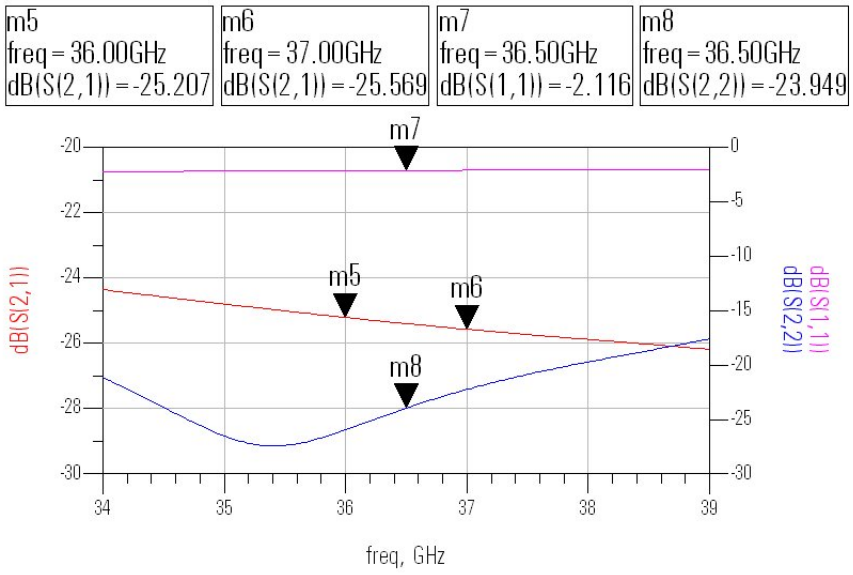

Figure 4.12: Isolation and input/output return loss of switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

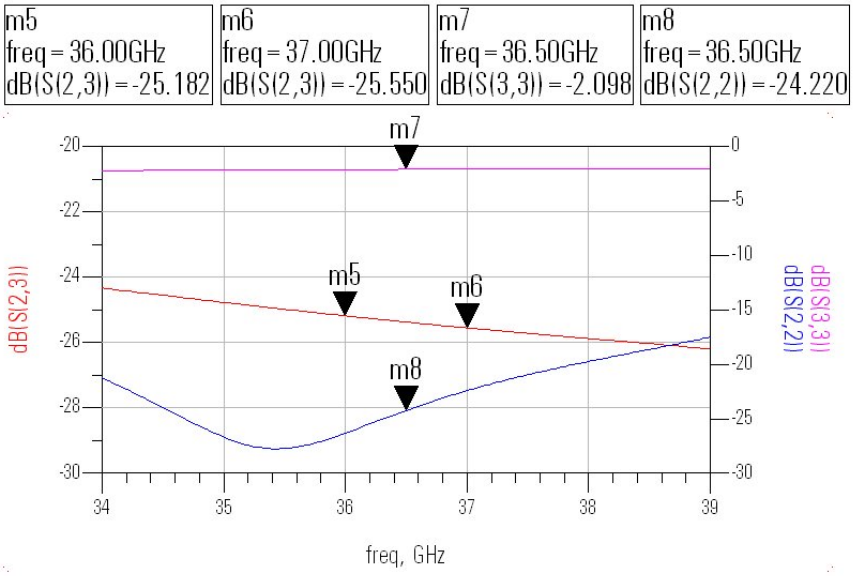

Figure 4.13: Isolation and input/output return loss of switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

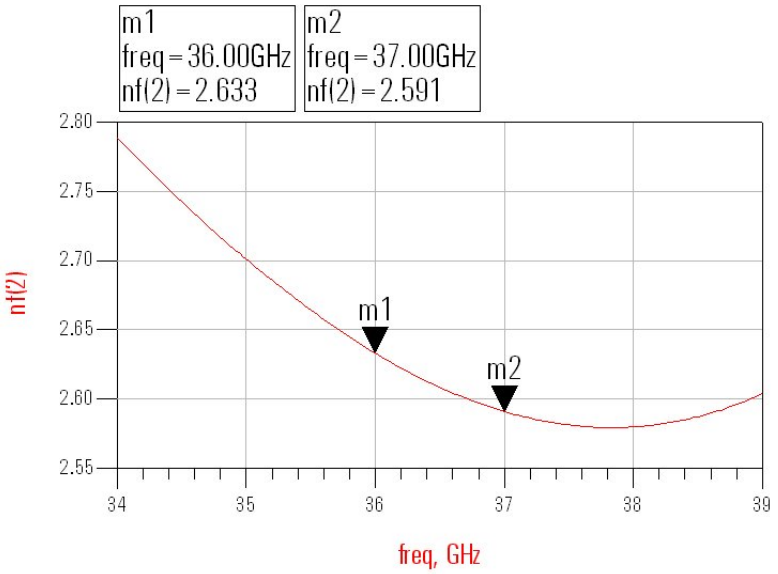

Figure 4.14: Noise figure of switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

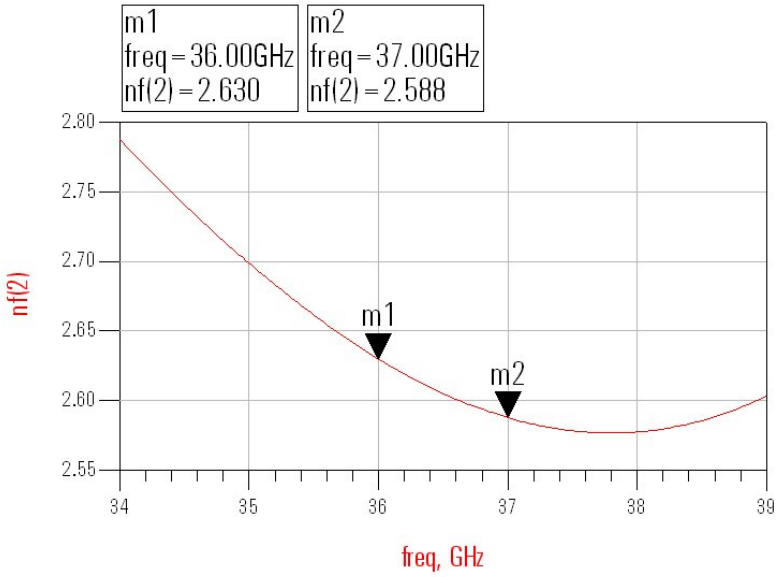

Figure 4.15: Noise figure of switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

As can been from plots 4.10 though 4.14 both possible switch inputs produce a nearly identical response, the variation between the switch arms is on the order of thousandths of a dB. For the full design, taking into account all transmission line discontinuities and process degradation, the gain of the combined switch-LNA circuit is approximately 7.84 dB, with an input return loss greater than 10 dB and output return loss of greater than 20 dB, while the noise figure is about 2.6 dB. The isolation of the switch combined with the LNA was around 25 dB. A summary of the simulated results is shown in table 4.2.

Table 4.2: Simulated results for the switch-LNA

	Gain		Isolation	
	36 GHz	37 GHz	36 GHz	37 GHz
	dB			
Straight Arm	7.840	7.620	-25.207	-25.569
90 Deg Arm	7.843	7.617	-25.182	-25.550

4.3.2 Switch – LNA Layout

The layout of the switch-LNA is shown in figure 4.8. The size of the chip is roughly 1.1 mm by 2.4 mm. The RF pads were designed to have a 150 micron pitch to match the available GGB probes available.

CHAPTER 5

EVALUATION AND RESULTS

This chapter describes the S-parameter and noise figure measurements of the SPDT switch and the SPDT switch-LNA combination. All measurements were performed in LAMMDA lab using the probe station, 8510C network analyzer and noise figure analyzer. Chapter 5.1 describes the measurement methodology and set up, chapter 5.2 describes the measurements performed on the SPDT switch, chapter 5.3 describes the measurements performed on the switch-LNA combination, chapter 5.4 describes the temperature measurements performed. Discrepancies with simulated results are discussed within each subchapter.

5.1: Measurement Methodology and Setup

Once the MMIC chips were fabricated they were inspected and characterized. Raytheon provided two different dies, one was of the single SPDT switch and the other was of the SPDT-LNA combination. Due to an error there were no breakaway pieces that could have assisted in determining the cause of discrepancies between measurements and simulations. In addition, each individual die consisted of two circuits. This caused some problems involving the length of the wire bond required to bias the circuit which in effect made measuring one of the circuits nearly impossible. Figure 5.1 shows the die of the SPST switch. As can be seen two circuits w ere not scribed properly creating a die with two identical circuits.

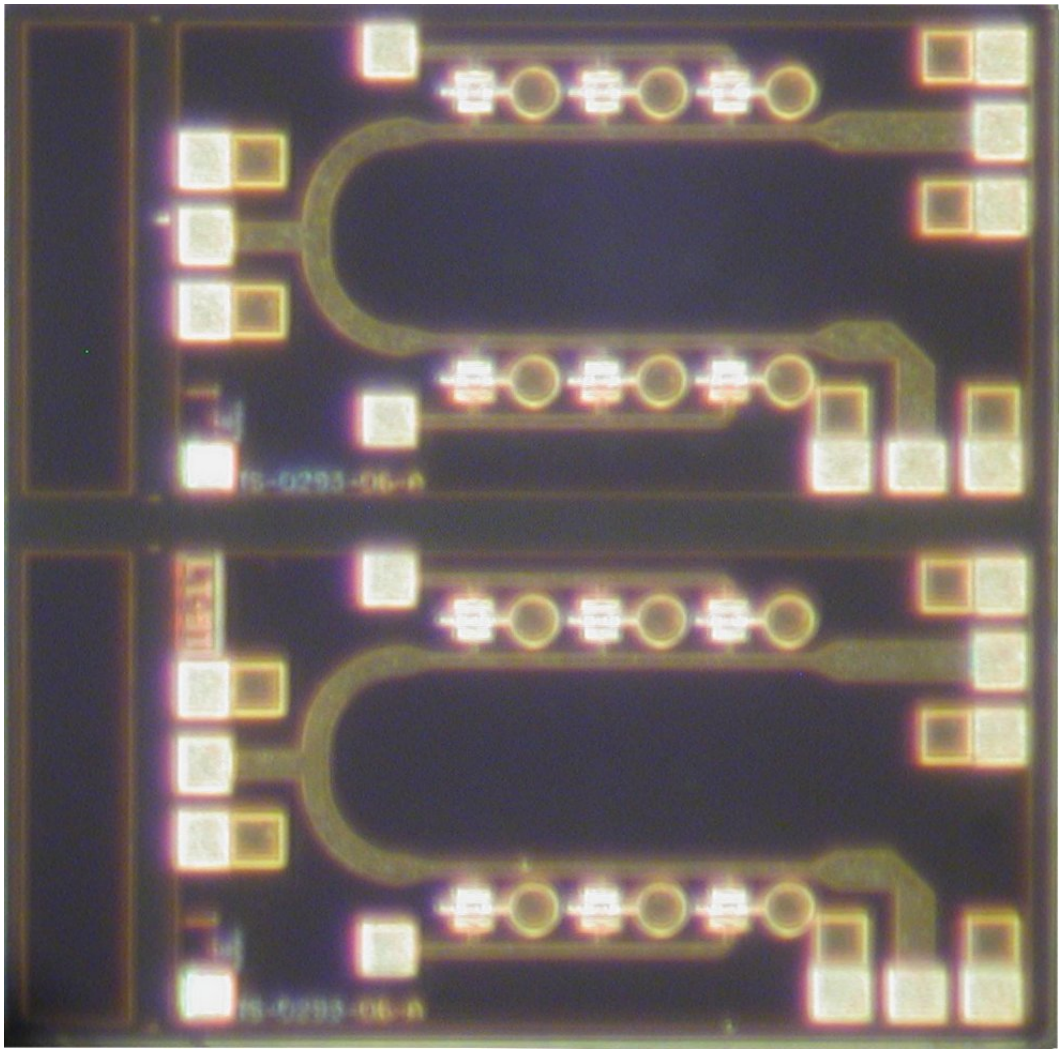

Figure 5.1: Fabricated MMIC chips

Before the MMIC chips could be measured they were mounted on a fixture. Although the measurements that were performed were on-chip, because the circuits required off chip bias capacitors and resistors the MMIC chips needed to be mounted on a test fixture. The chips were mounted using conductive epoxy, part number H20E from Epoxy Technologies; conductive epoxy is used to create a good ground plane. The chips were epoxied on a small copper board which served as the basic test fixture. A ground

reference for the bias voltages was provided with a simple piece of wire that was soldered on to the copper board. All additional off-chip bias components such as resistors, capacitors and jumpers were also epoxied on the test fixture. The probes utilized for the RF measurement were GGB-150C probes from GGB Industries. Biasing to the chips was provided with bias tips that were connected to the power supplies. In some cases biasing traces were etched on the copper board, more detail on this is provided in the following chapters, where appropriate.

5.2: SPDT Switch Measurements

As described in chapter 3, the switch is controlled with the use of two voltages, one that isolates the arm by turning the FETs "on," and another voltage that turns the FETs "off" which allows the signal to pass from the input the output. These voltages were supplied to the MMIC chip via a large, $2\,\mathrm{k}\Omega$, thin film resistor from mini-systems. One pad of the resistor was wire bonded to the bias pad of the switch arm using gold wire bond, and the other pad of the resistor was contacted with the bias probe or wire bond to the jumper that corresponded to the switch bias trace, this was necessary when the switch-LNA combination was measured and is explained further in the chapter. The SPDT switch test setup is shown in figure 5.2. A picture of the SPDT MMIC is shown in figure 5.1

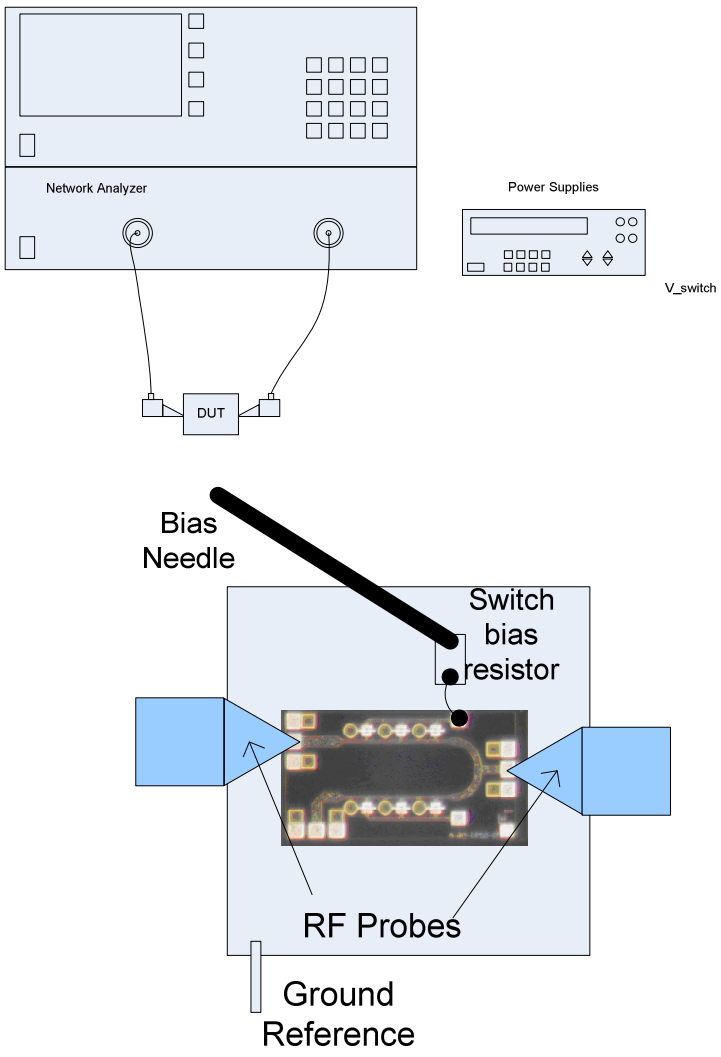

Figure 5.2: SPDT switch test setup and DUT test fixture detail

During the ADS simulations the arm of the switch that was not being probed was terminated with a 50 Ω port impedance which can be represented as a 50 Ω resistor. Accordingly, a 50 Ω thin film resistor was originally going to be epoxied onto the test fixture. However, since the 50 Ω terminated arm is not probed during measurements and is biased such that the FETs are turned "on" thus isolating the output of the arm from the rest of the switch, it does not matter what impedance the arm is

terminated with, provided the circuit has adequate isolation. For that reason and to simplify other needed measurements the arm was left “open” when not being measured.

A SOLT calibration was performed on the GGB RF probes before any measurements were carried out, the calibration was performed using a GGB Calibration substrate CS-5. For the straight arm transmission the simple straight calibration structures were used. However, when the 90 degree arm calibration was needed an RF probe arm was placed 90 degrees relative to the input and output and calibrated with the 90 degree bend calibration structures.

The first step in the measurement process was to appropriately bias the switch; biasing one switch arm on, and the other arm off. The RF probes were then contacted to the input and output RF pads. The measured and simulated results are shown in figures 5.3-5.8. Figures 5.3 and 5.5 display the measured insertion loss, and figures 5.4 and 5.6 display the measured input/output return loss of each switch arm. Figures 5.7 and 5.8 display the measured isolation of each switch arm. In the figures below, the measured results were simulating with port 4 being the input of the switch and port 5 being the output of the switch, additionally port 3 represents the 90 degree input port.

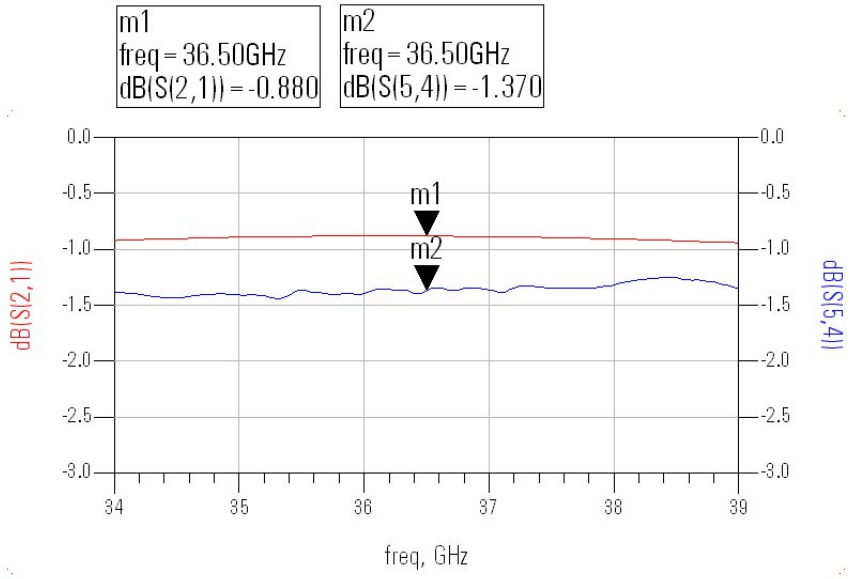

Figure 5.3: Measured and Simulated Insertion loss simulation of SPDT switch when the straight arm is biased off, and the 90 Deg bend arm is biased on

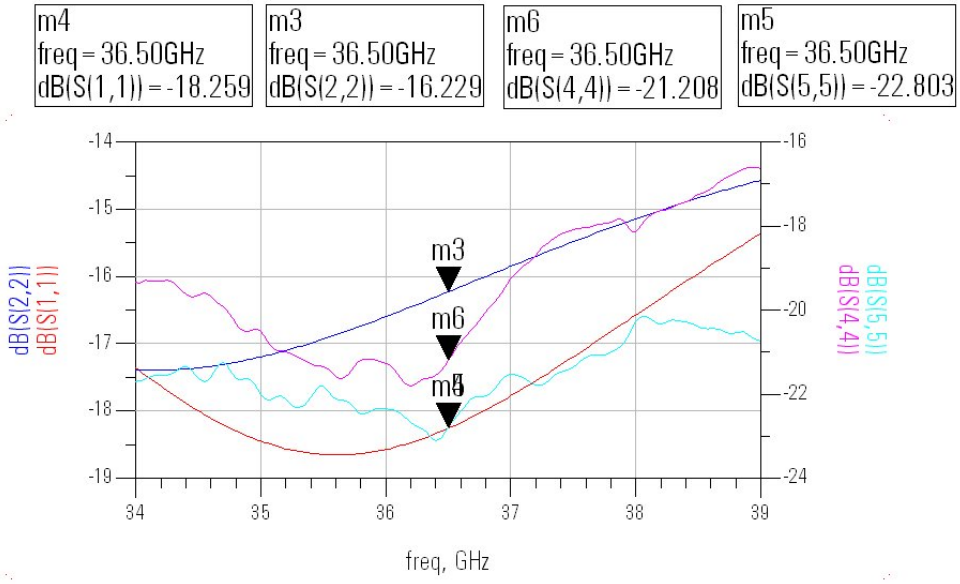

Figure 5.4: Measured and Simulated Input and Output return loss of SPDT switch when the straight arm is biased off, and the 90 Deg bend arm is biased on

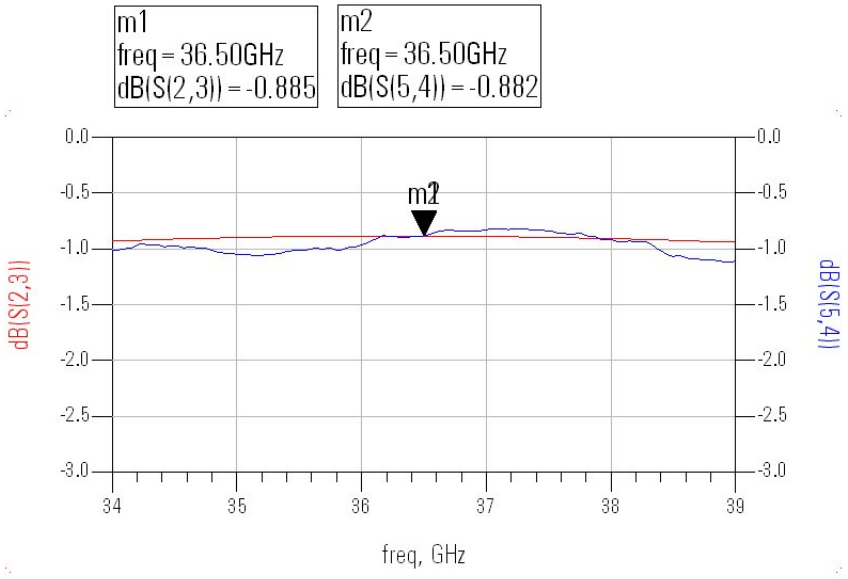

Figure 5.5: Measured and Simulated Insertion loss simulation of SPDT switch when the 90 Deg bend arm is biased off, and the straight arm is biased on

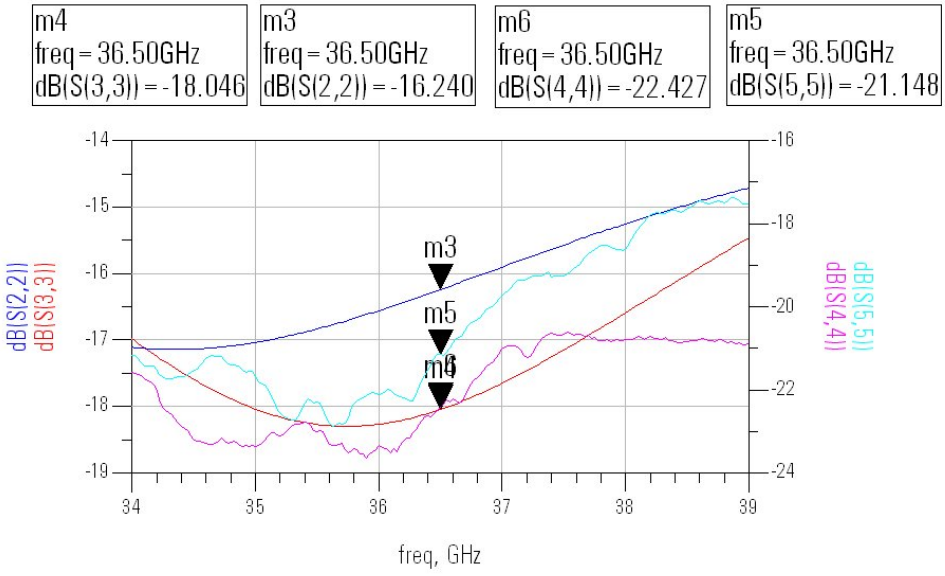

Figure 5.6: Measured and Simulated Input and Output return loss of SPDT switch when the 90 Deg bend arm is biased off, and the straight arm is biased on

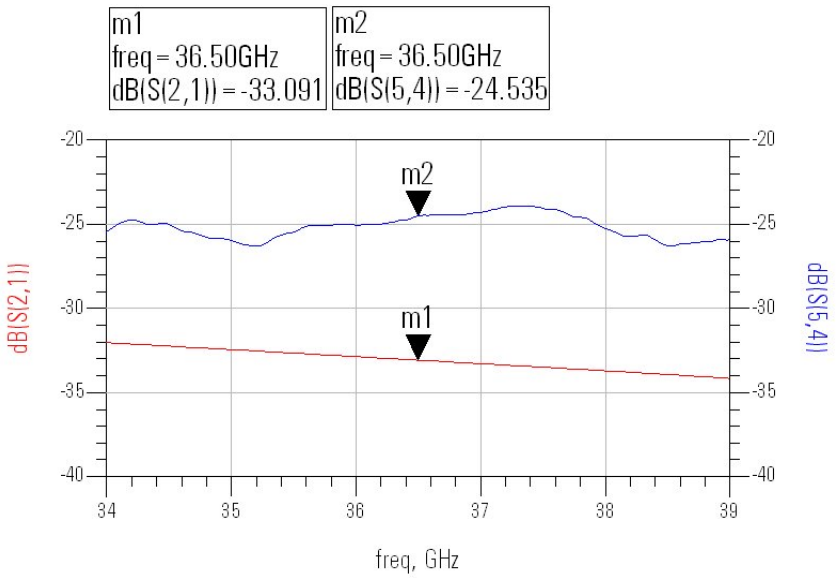

Figure 5.7: Measured and Simulated Isolation simulation of SPDT switch when the straight arm is biased on, and the 90 Deg bend arm is biased off

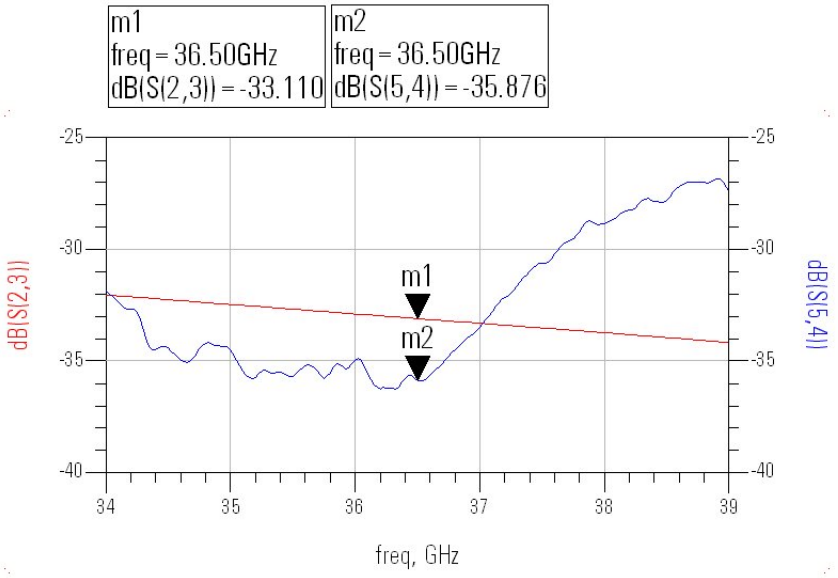

Figure 5.8: Measured and Simulated Isolation simulation of SPDT switch when 90 Deg bend arm is biased on, and the straight arm is biased off

As can be seen from figure 5.3-5.8, the insertion loss of the straight and 90 degree arms are 1.3 dB and 0.88 dB and the isolation is 25 dB for the straight arm and 36 dB for the 90 degree arm. Both inputs have an input and output return loss of -19 or better in the desired 36-37 GHz bandwidth.

The measured data shown in the previous plots only represent one measured result. Several other measurements were also performed and that data was used to create error bar plots for the insertion loss of the switch. These plots are shown in figures 5.9 and 5.10. The error bar plots take into consideration 6 additional measurements performed on the straight input arm of the switch, and 4 for the 90 degree input arm of the switch, respectively. The s-parameter measurements shown in the previous plots represent the most typical response seen and were not selected to match better with the simulated results.

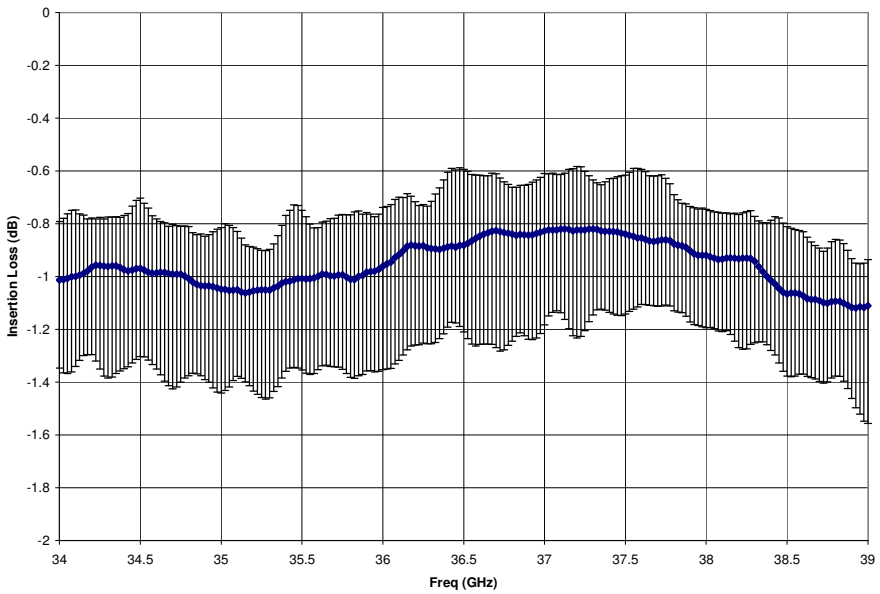

Figure 5.9: Error bar plot for the switch with straight input arm active

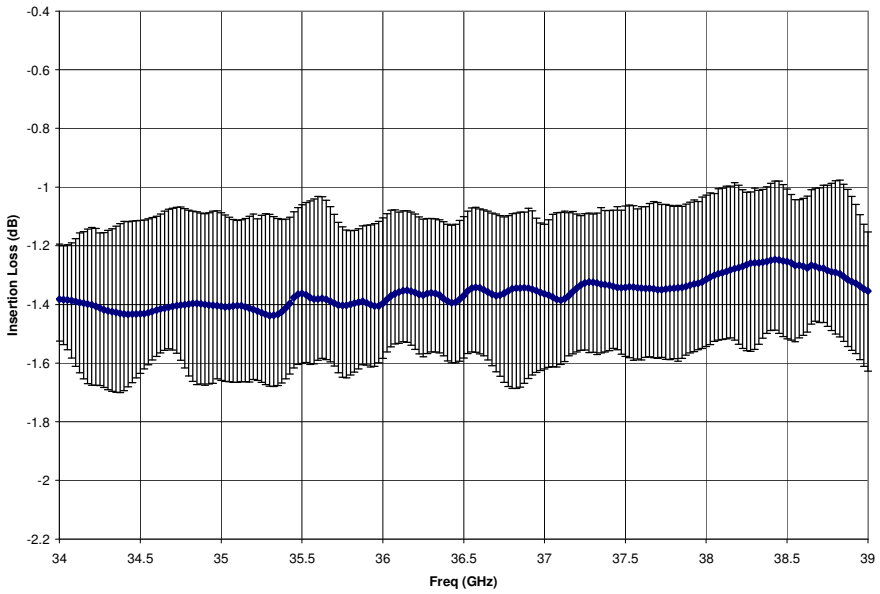

Figure 5.10: Error bar plot for the switch with straight input arm active

The measured s-parameters for the switch are within range of the simulated s-parameters. The difference in measured insertion loss between the 90 and straight arm is around 0.6 dB. This difference is likely due to the difference in input impedance between them, the value of the input insertion loss for the 90 degree bend arm is around 1.3 dB better than that of the straight input arm, mainly due to the fact that, as can be seen in figure 5.1, the arms are not identical. Both inputs had higher input and output return loss.

The difference between measured and simulated insertion loss of the straight input arm is around 0.5 dB, while the difference in the 90 degree arm the difference is minimal. The 0.5 dB difference in insertion loss in the straight arm of the switch is likely due to the way the biasing was distributed to the switch FETs. As seen in figure 5.1, each individual chip consists of two circuits, this occurred because it was laid out in the mask next to larger circuits and it would have been more expensive to sub-scribe down the level of these circuits.

Consequently since the biasing into the switch was performed via an off chip resistor the distance from bias pads in the MMIC and the off chip resistor was not the same for both switch arms, in fact the bond wire length required was considerably longer for one of the bond pads. Since the mHEMT FETs are typically biased “on” if they are not biased off completely the model would not be valid for the switch and additional loss would occur in the transmit path. The isolation path would not be affected since the FETs are by default on.

5.3: Switch-LNA Measurements

Unlike the SPDT-Switch MMIC chip, which required only two power supplies, the switch-LNA chip needed four different power supplies to bias it. The chip required two supplies to bias the switch and then two other supplies to bias the drain and gate of the LNA. This created a problem because although there were plenty of power supplies, only three bias probes were available. A possible solution to this problem was to only bias one of the switch arms. This would continue to provide an accurate measurement because mHEMT transistors are inherently on which means that the transistors are turned on with no bias applied and require a negative voltage to be biased "off". Therefore, providing biasing to only one switch arm and also biasing the drain and gate of the LNA could be sufficient for these measurements. Since it is not possible to verify this with measurements, given the available bias probes, this was simulated using ADS. Figure 5.11 displays the delta of S21 seen in each arm, where delta is defined as the value of S21 when the opposite arm of the circuit is biased "on" subtracted from S21 when the opposite arm is not biased at all.

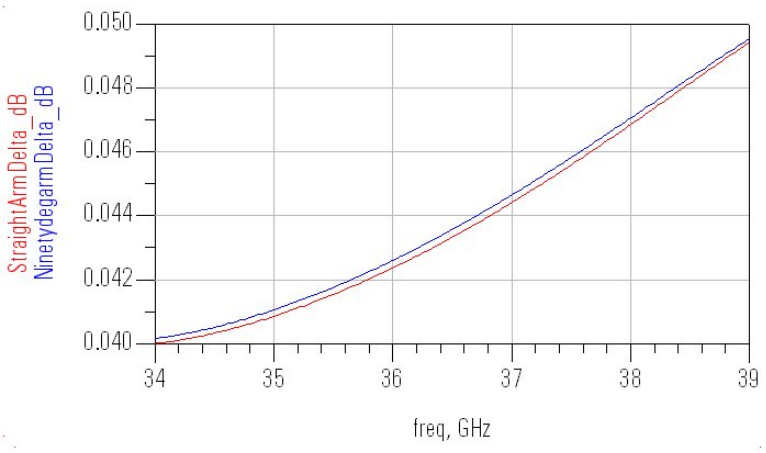

Figure 5.11: Delta of the magnitude of S21 in the SW-LNA when not biased and when it is biased "on"

In figure 5.11 the *StraightArmDelta* corresponds to the straight input switch, and *NinetydedarmDelta* refers to the difference, in dB, with the switch and the switch-LNA combination is minimal when there is no voltage applied at the gates of the mHEMT transistors compared to when they are biased fully on. Therefore, it is valid to rationalize that using only three bias probes will provide adequate results.

Due to the position of the 90 degree input of one of the switch arms and the fact that the biasing pads were placed on the chip to agree with the bias positions of the design currently used by another student, the gate and drain bias and the switch biasing were located on opposite sides of the chip. This biasing scheme was a problem when performing on chip measurements because the RF probes and the bias probes were colliding given the small space of the chip. The solution to this problem was to create an external routing for the biasing. This could be accomplished on the copper board itself using a milling machine to create the routing traces. The picture of the external

routing is shown in figure 5.12, from AutoCAD. The test setup for the Switch-LNA circuit is also shown in figure 5.12.

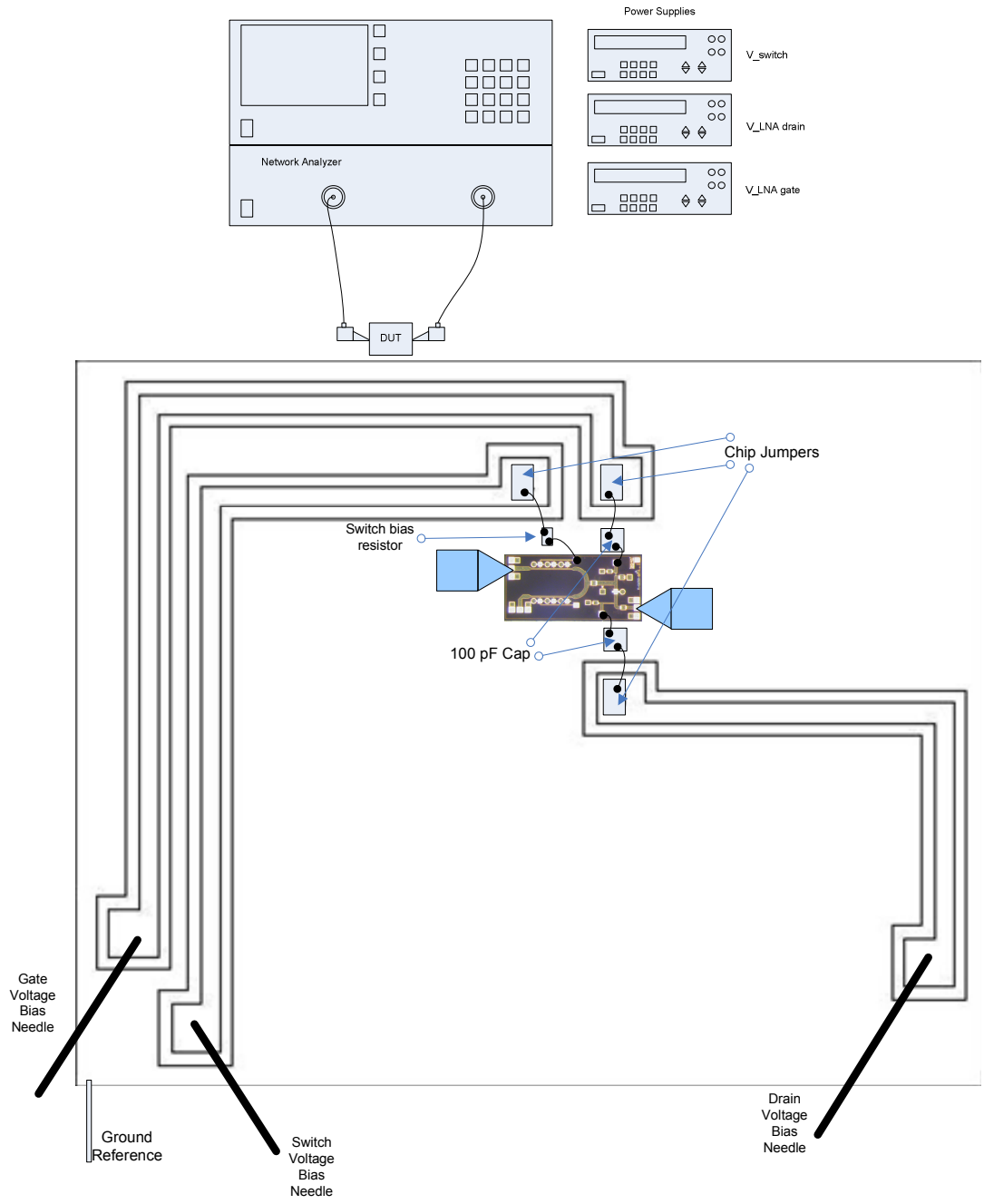

Figure 5.12: Switch-LNA test set up and DUT test fixture detail

In order to create contact the MMIC chips and the bias traces a thin film jumper was used to jump from one of the thin film resistor pads, in the case of the switch, and the thin film capacitors in the case of the LNA. The thin film chip jumper is a zero ohm resistance component that can be used as a bonding island, or in this case make a connection between copper and the MMIC more reliable and easy to implement. The bias probes made direct contact with the copper trace.

The biasing of the gate and drain of the LNA where provided through bias capacitors. The capacitors were 100 pF from mini-systems, these capacitors function to further protect the LNA from possible oscillations at low frequencies. The biasing procedure was to initially bias the gate with a -1 V, and the drain with a 0 V. The gate supply was then increased a few tenths of a volt, the drain voltage was then biased to the desired voltage. The gate voltage was then increased until the designed i_D was measured. This biasing scheme is typical of amplifiers because if the drain is biased before the gate it could cause the LNA to oscillate. Conversely, when the amplifier is biased off the reverse scheme is followed: the drain is turned off first and then the gate. The picture of the MMIC is shown in figure 5.13.

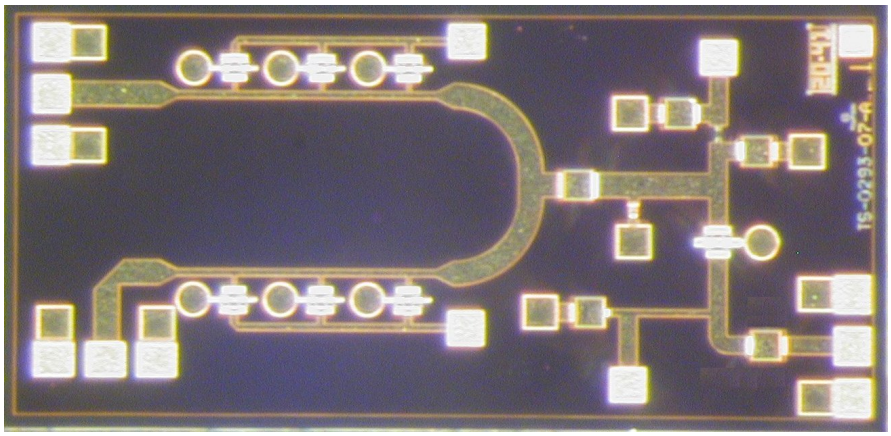

Figure 5.13: Switch-LNA MMIC

The measured and simulated results of the Switch-LNA are shown in figures 5.14 thru 5.19. Figures 5.14 and 5.15 displays the measured gain and the input and output return loss of the switch-LNA when the straight arm is biased off, and figures 5.16 and 5.17 displays the measured gain and the input and output return loss of the switch-LNA when the 90 degree arm is biased off,. While figures 5.18 and 5.19 display the measured isolation of both switch arm inputs. As with the switch results in the figures below the measured results were simulating with port 4 being the input of the switch and port 5 being the output of the switch, additionally port 3 represents the 90 degree input port.

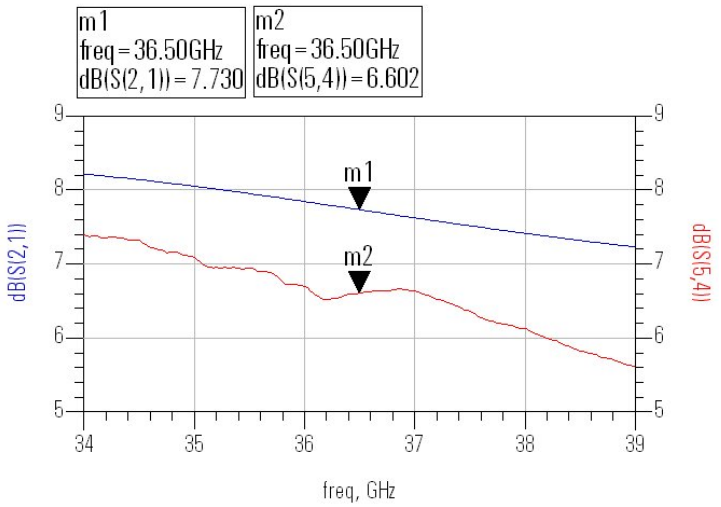

Figure 5.14: Measured and Simulated Gain of the switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

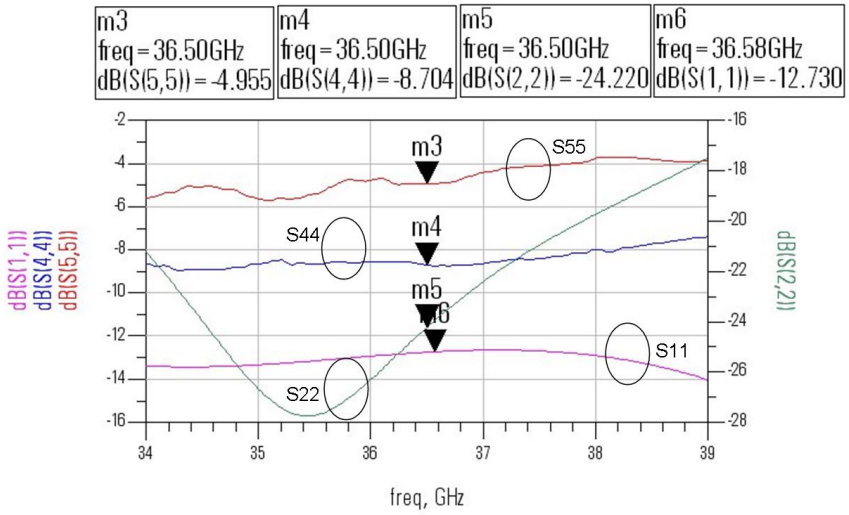

Figure 5.15: Measured and Simulated input and output return loss of the switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

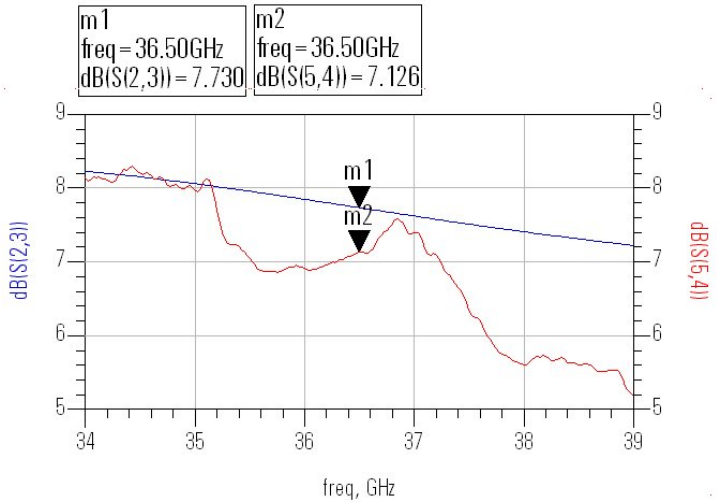

Figure 5.16: Measured and Simulated Gain of the switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

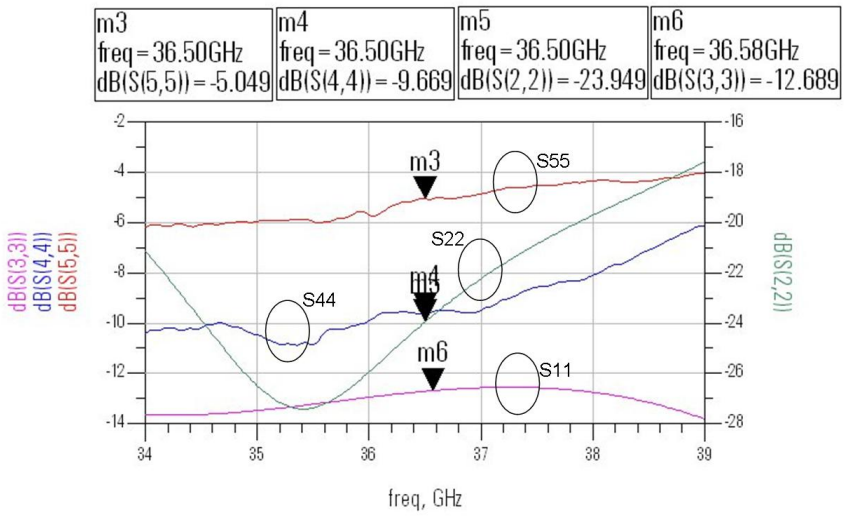

Figure 5.17: Measured and Simulated input and output return loss of the switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

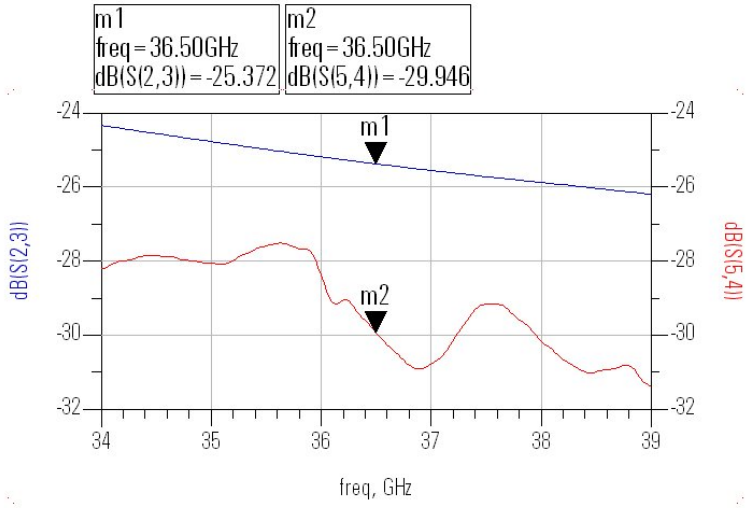

Figure 5.18: Measured and Simulated Isolation of the switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

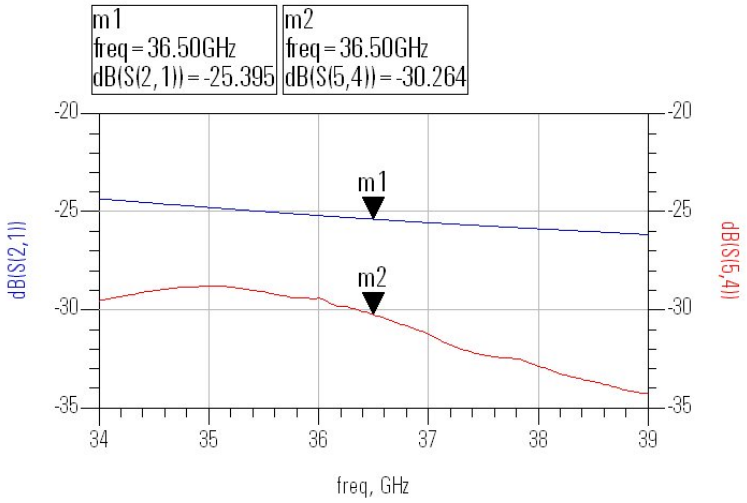

Figure 5.19: Measured and Simulated Isolation of the switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

As can be seen from figure 5.14 and 5.16 the measured gain of the switch LNA is around 6.6 dB for the straight arm input and 7.1 for the 90 degree input, respectively. The difference between the arms correlates well with the difference in insertion loss that was measured in the switch alone. The measured difference in insertion loss between the switch arms was around 0.5 dB, with the 90 degree input having the lower insertion loss and thus correlating with the better gain. The dip in gain seen in the 90 degree switch arm is caused by the input impedance presented at the 90 degree input since there is no significant dip in gain when measuring from the input of the straight input arm. Then the impedance presented to the LNA must cause it to have a different gain curve in that frequency range. As shown in figures 5.3 and 5.5 there is no insertion loss dip when then switch measured alone, so the effect is due to the characteristics of the LNA and with no individual breakouts it is not possible to measure the input match characteristics of the physical LNA.

As with the switch measured data plots the measured data for the switch-LNA shown in the previous plots only represent one measured result. Several other measurements were performed and that data was used to obtain error bar plots for the gain of the switch-LNA. The error bar plots take into consideration 5 additional measurements performed on the straight input arm of the switch-LNA and 6 additional measurements for the 90 degree input arm of the switch-LNA, respectfully. These plots are shown in figures 5.20 and 5.21.

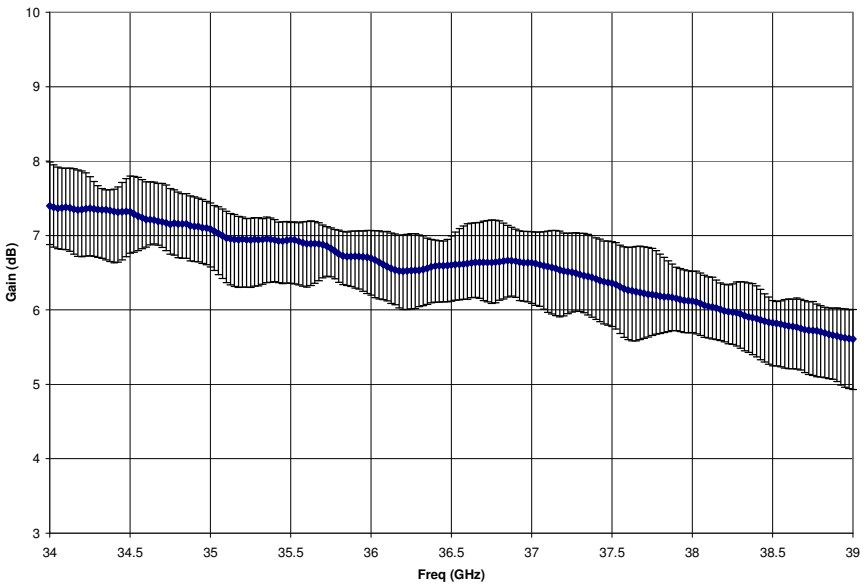

Figure 5.20: Error bar plot for the gain of the switch-LNA when the straight arm is biased off, and the 90 degree arm is biased on

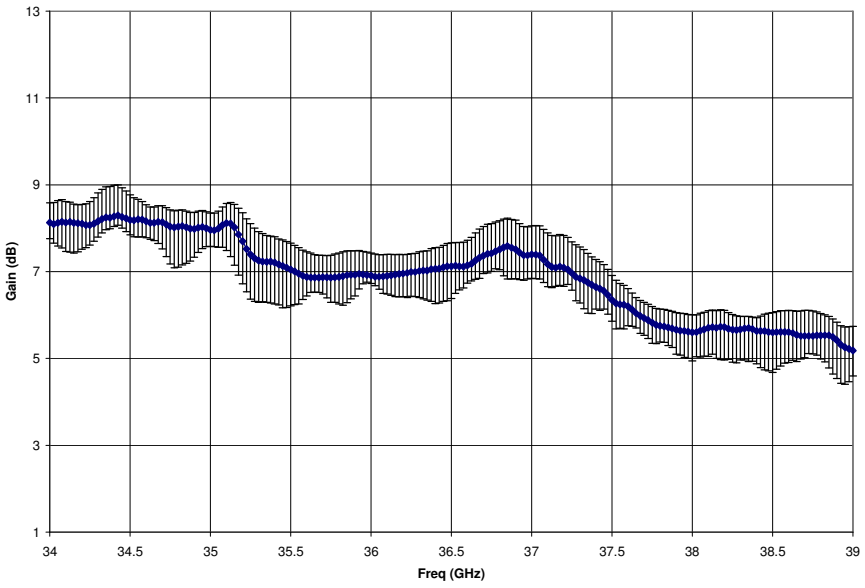

Figure 5.21: Error bar plot for the gain of the switch-LNA when the straight arm is biased on, and the 90 degree arm is biased off

The isolation in both arms was around 30 dB, although the isolation was higher for the 90 degree input than the straight arm when the switch was measured alone. The isolation actually increased for the straight arm, while the isolation at the 90 degree arm decreased around 5 dB. Overall the measured gain and isolation results were not far off the predicted values.

However, the difference between the measured and simulated output return loss is significant and causes a considerable degradation in the circuit performance. The measured output return loss was around 5 to 6 dB while the simulated results predicted lower than 20 dB. Several chips were measured to verify that this was not a process issue; however, all measurements were around 5 to 6 dB.

The first step in determining the cause for the large difference in output return loss was to analyze the output matching network. The values were verified and the output matching network was simulated to verify that the Γ_{out} and Γ_L were as designed and really provided the needed matching. Once this was determined to not be the cause the physical layout of the output matching network was considered. Using the process guide from Raytheon, the dimensions of the components used in the output matching networks were verified to match the correct desired values of the component. One of the first errors found was the RF pad contact that forms part of the GSG output. The Pad was not modeled with the correct length and width; this was due to a typing error when it was inputted where the length was entered as the width and the width was entered as the length.

Additionally, the transmission line lengths were also verified. An error was finally found in one of the transmission lines. The series transmission line that follows the FET was shorter in length than desired, by approximately 100 um. At this high frequency that is a critical length, especially since the transmission line was a critical component in the matching network. The circuit was re-simulated to display the affect of the shorter transmission line and the RF pad was modeled appropriately and the results of the differences with the measured results are shown in figure 5.22.

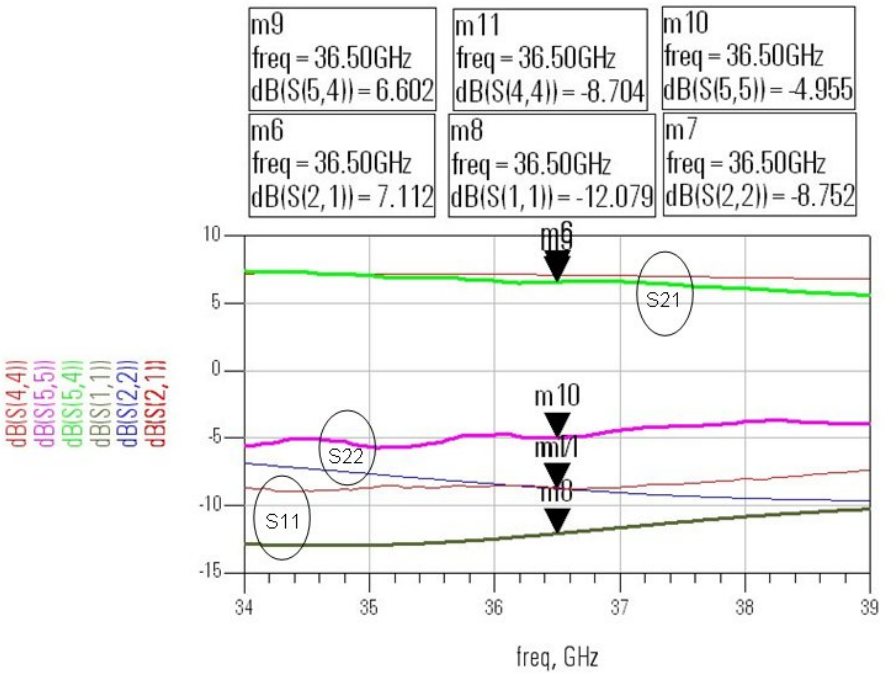

Figure 5.22: S-Parameter comparison between re-simulated and measured switch-LNA

With the corrected transmission line lengths and RF contact the gain drops a few tenths of a dB to 7.1 dB. The input return loss remained essentially the same at around

12 dB, however, as predicted the simulated output return loss drops by more than 10 dB, the new output return loss is 9 dB. The majority of the degradation is caused by the transmission line length error (~10 dB). The remaining error is caused by the error at the RF output pad. However, this error is more difficult to quantify due to the involvement of the probe. Due to it being the last part of the RF path within the MMIC a larger error is possible since the calibration of the output probe is dependent on a certain pitch, due to the different width of the RF path, though slight, does change the distance between the RF path from the via pads that from the grounds in the GSG probe.

5.3.1: Noise Figure Measurements

Next, the noise figure was measured; this measurement was performed in LAMMDA lab. The noise figure was measured using a noise figure analyzer (NFA) that can measure the noise figure directly without having to do any calculations. The NFA works by first calibrating it with the output of a noise source connected to the NFA. Next, the DUT was placed between the noise source and the NFA to obtain a NF measurement. The noise source available in LAMMDA was a waveguide Ka band noise source. Since the GGB probes available had a K connector input, a K-connector to Ka waveguide transition was required.

- **Noise Figure Measurement Set-up**

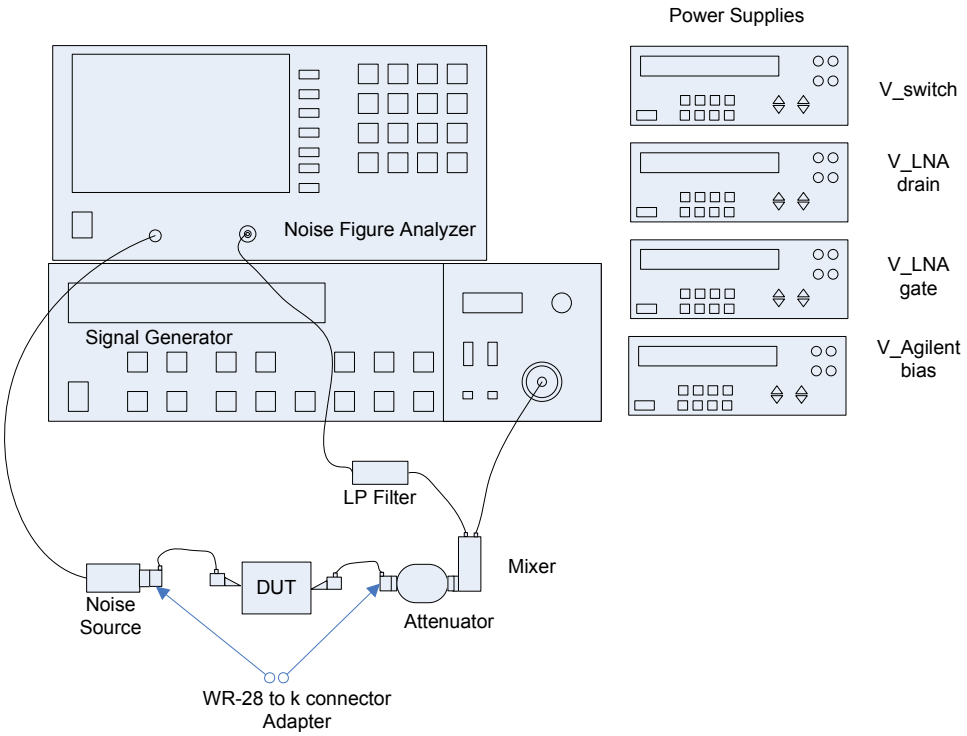

Figure 5.23: Noise Figure measurement setup

Since there were no noise figure analyzers that could measure the noise figure up to Ka band available and since the operating frequency of the available noise figure analyzer was from DC to 3 GHz, the output of the MMIC chip had to be down converted to the NFA frequency range. Additionally two other low noise amplifiers, Agilent AMMC 6241, were needed to overcome the large conversion loss of the mixer. The mixer had a conversion loss of 25 dB at 36.5 GHz. The mixer used was an Agilent waveguide harmonic mixer (11970A) that was available in LAMMDA lab. Figure 5.23 illustrates the measurement system set up for the evaluating the device.

The measurements were performed with the NFA by connecting the noise source to a WR-28 / 2.9 mm adapter. A 2.9 mm cable was then used to connect to the

input probe. During Calibration, the GGB probe would touch down to the input pads of the Agilent MMIC amplifier, which is a low noise amplifier that has a gain of 20 dB and operates from 26 to 43 GHz, a picture of the chip is shown in figure 5.24.

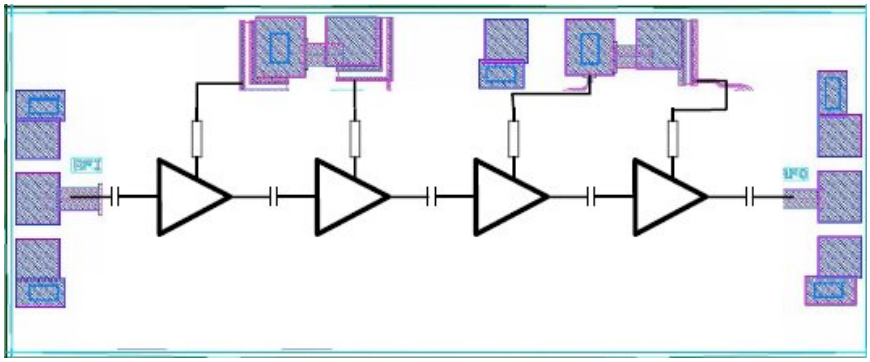

Figure 5.24: Photograph of Agilent LNA MMIC chip [32]

The output GGB probe was placed at the output of Agilent amplifier and its 2.9mm-connector cable was connected via a WR-28 / 2.9 mm adapter which fed into a WR-28 waveguide attenuator. The attenuator was an Agilent variable waveguide attenuator, R382A, which was obtained from LAMMDA lab. The attenuator was placed between the output of the Agilent amplifier and the input of the mixer to further guarantee that both the input of the mixer and the output of the Agilent amplifier both saw a 50 Ω impedance; the attenuation was set to 1 dB. The output of the attenuator was then connected to the WR-28 waveguide input of the mixer; since both components had WR-28 ports no adapter was necessary.

This mixer had a Ka- band (WR-28) waveguide RF input, and an SMA connector LO and IF output. The mixer's RF operating frequency was 26.5 GHz to 40

GHz. Since the mixer was a harmonic mixer it did not require a high frequency signal source to serve as the LO. The mixer was designed to have an LO in the range 3 GHz to 6.1 GHz, this range of LO produced an IF range of DC to 1300 MHz. The LO was provided with a low noise synthesizer, the IF output of the mixer was then connected to a low pass filter and the output of the filter was then connected to the input of the NFA. The low pass filter was to filter all signals above the measured bandwidth.

The NFA was originally set up to provide noise figure measurements at a 1 GHz bandwidth. However, after the calibration it was found that it was not stable at a large bandwidth. That is the NF was not at a stable 0 dB after calibration, it would vary up to 5 dB, this can typically be a problem when measuring large bandwidths. For that reason the noise figure measurements were performed over a 200 MHz bandwidth centered at 36.5 GHz. Additional 200 MHz, noise measurements were originally planned; however, this would have required the wirebond at the input of the Agilent amplifier to be removed and reapplied at least five times. When this was attempted wire bonding significantly wore the input RF pad of the Agilent amplifier which made the calibration dangerous for the RF probe since significant wire bond debris remained, for this reason no further noise figure measurements were possible.

- **Device Under Test**

Once the calibration of the noise figure meter was performed, the DUT was inserted between the noise source and the components following it in the calibration

loop. The addition of the Agilent amplifier required an additional off chip capacitor for biasing which meant that the test fixture used to measure the switch-LNA is chapter 5.2 had to be redesigned, the new test fixture is shown in figure 5.25, the numbers 1-4 correspond to the assigned bias traces, 1 corresponds to switch bias, 2 corresponds to the LNA gate bias, 3 corresponds to the Agilent LNA bias, and finally 4 corresponds to the LNA drain bias. The MMIC cascade depicted in the figure is shown in detail in figure 5.26.

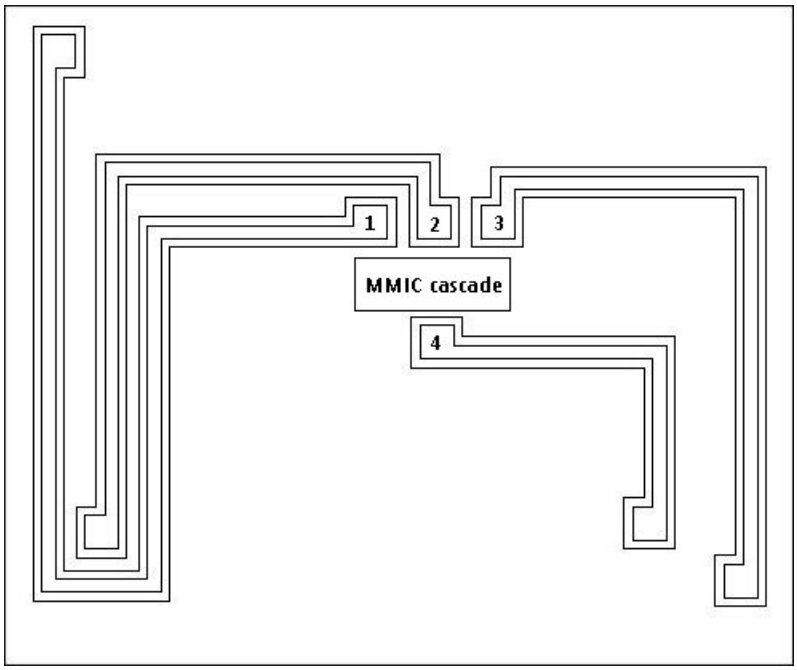

Figure 5.25: AutoCAD picture of the noise figure measurements test fixture

As mentioned before there were only three bias tips, so a new solution was developed to accommodate the new biasing needs for the Agilent LNA. The switch bias voltage, trace number one, was provided by creating a bias path that led to a metal lead soldered to it with an alligator clip, instead of a bias pin, used to provide the voltage. A

biasing trace was created to feed the Agilent LNA, however, the MMIC chips are only a few millimeters long so it would require large wire bonds if the chips were epoxied close to each other. For that reason a small, separate substrate, thin film 50 Ω transmission line was placed between the output of the switch-LNA and the Agilent LNA. For clarity a figure of the MMIC cascade is shown in figure 5.26. As can be seen it consists of the switch-LNA, an attenuator, a transmission line and the two Agilent amplifiers.

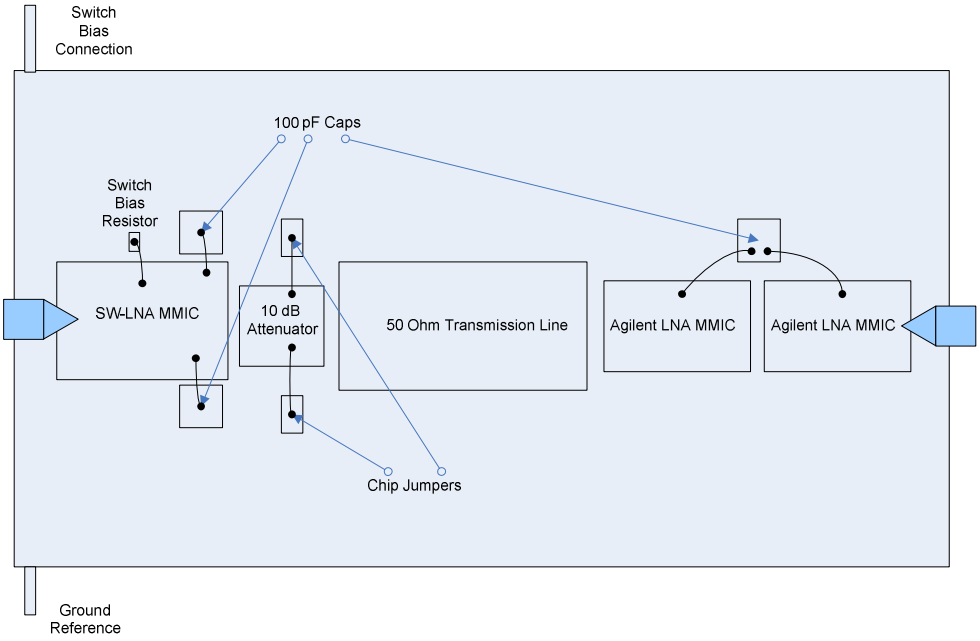

Figure 5.26: Noise Figure measurement MMIC Chips

As mentioned in the chapter 5.3 the output return loss of the switch-LNA was around 5 dB, this meant that the output impedance of the MMIC was not 50 Ω as designed. Since the noise calibration occurs when the probes touch down on the Agilent MMIC input, which are approximated to be 50 Ω, the gain and the noise figure of the

Agilent LNA would no longer be the same if the output of the switch-LNA MMIC was wirebonded to the input of the Agilent LNA. Since the impedance the Agilent LNA "sees" would no longer be 50 Ω and it would no longer have the same gain and noise figure as it did during the calibration. A solution to that mismatch problem was to place an attenuator that was capable of presenting a 50Ω impedance to both the output of the switch-LNA MMIC and the input of the Agilent amplifier MMIC. The attenuator was a 10 dB high frequency attenuator from skyworks, part number ATN3580-10. Due to the large attenuation within the DUT another Agilent amplifier was placed after the transmission line but before the other identical Agilent amplifier. The thin film attenuator was wire bonded between the output of the Switch-LNA MMIC and a transmission line used to connect to the Agilent amplifier. The switch-LNA, the attenuator, the transmission line, and the first Agilent amplifier would now be the DUT.

The noise figure measurements were then performed as previously described with the new DUT. The switch-LNA MMIC was biased appropriately and the measured noise and gain provided by the NFA were obtained. However, since other components were also part of the DUT the measured noise figure was larger than just the noise figure of the switch-LNA MMIC which had to be calculated from the total measured noise figure. The measured total noise figure of the DUT is plotted in figure 5.27 for both switch inputs.

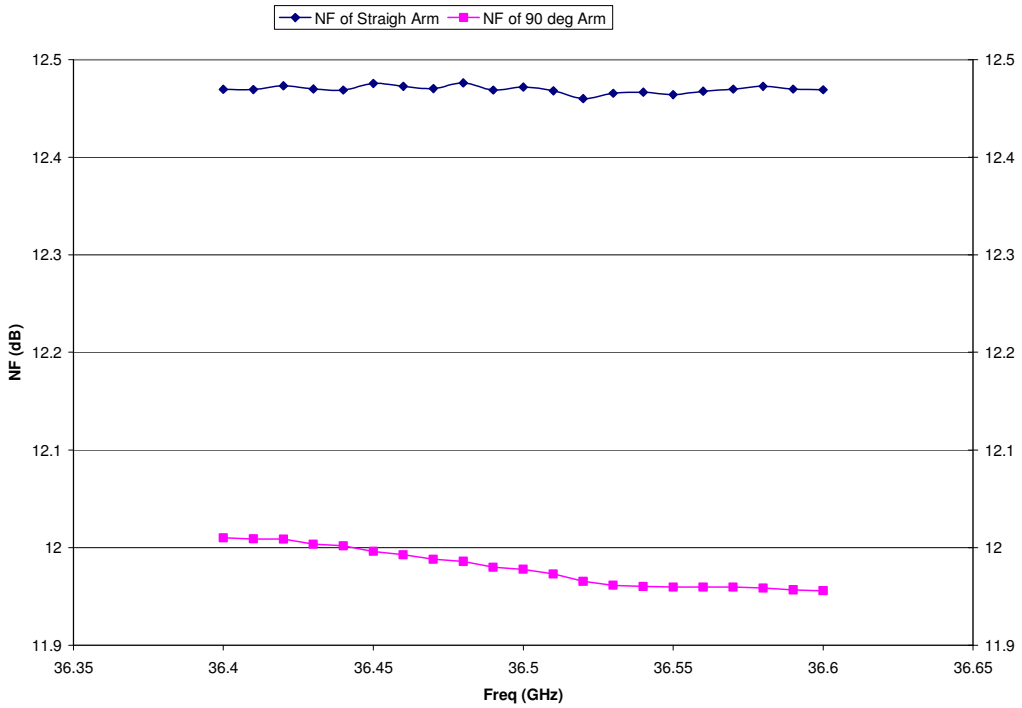

Figure 5.27: The measured noise figure of the DUT for both switch arm inputs

- **De-embedding of the Switch LNA from DUT**

Once the noise figure was measured for the DUT, the noise figure of only the switch LNA was calculated. A first step is to remove the mixer's sideband affects from the DUT noise figure. Since the mixer converts all frequencies presented to it, it is typical to include a bandpass filter at the mixer RF input around the center frequency to filter out unwanted signals. Of special importance is the image frequency which directly affects the gain and noise figure of the DUT. If this frequency is not filtered out then it will also downconvert to the IF frequency thereby increasing the measured value of the

gain and noise figure by approximately 3 dB. Since no filter was available at this frequency, DSB measurements were performed.

Once the noise figure of the full DUT is measured the actual noise figure of the switch-LNA must be extracted from this number. Due to the low loss of the transmission line, in the order tenths of a dB, its contribution to the noise figure and gain of the DUT will be ignored. Using Friis' formula the total noise figure of the DUT can be written as shown in equation 5.1.

$$F_{DUT} = F_{swlna} + \frac{F_{atten} - 1}{G_{swlna}} + \frac{F_{lna} - 1}{G_{swlna} G_{atten}} \tag{5.1}$$

Where F_{DUT} is the measured noise figure, F_{swlna} is the noise figure of the switch-LNA, F_{atten} is the noise figure of the attenuator, G_{atten} is the gain of the attenuator and G_{swlna} is the gain of the switch-LNA. Then solving for the noise figure of the switch LNA in equation 5.1 the noise figure of interest can be written as equation 5.2.

$$F_{swlna} = F_{DUT} - \left(\frac{F_{atten} - 1}{G_{swlna}} + \frac{F_{lna} - 1}{G_{swlna} G_{atten}} \right) \tag{5.2}$$

The next step is to solve for all the unknowns in the equation. This was performed with further measurements; the gain of the switch-LNA was measured for both switch arm inputs. The s parameters of the actual attenuator in the noise figure measurements were

not performed because it was not possible to safely remove it from the test fixture. Additionally, a direct probe measurement of the attenuator was not possible because of the difference in probe pitch between the attenuator and the available probes. Therefore, a different but identical attenuator was measured with the use of J-probe substrates. These substrates were epoxied on both sides of the attenuator. The J-probe substrates contain 150 um pitch RF contacts with a 50 Ω transmission line, the RF contacts are then wire-bonded to the input and output of the attenuator. Before measurement, a (thru-reflect-line) TRL calibration was performed, a TRL calibration was needed because the reference plane needed to be moved toward the input and output of the actual attenuator chip, and not at the tips of the RF probes. Once the calibration was performed the s parameters were measured and are shown in figure 5.28.

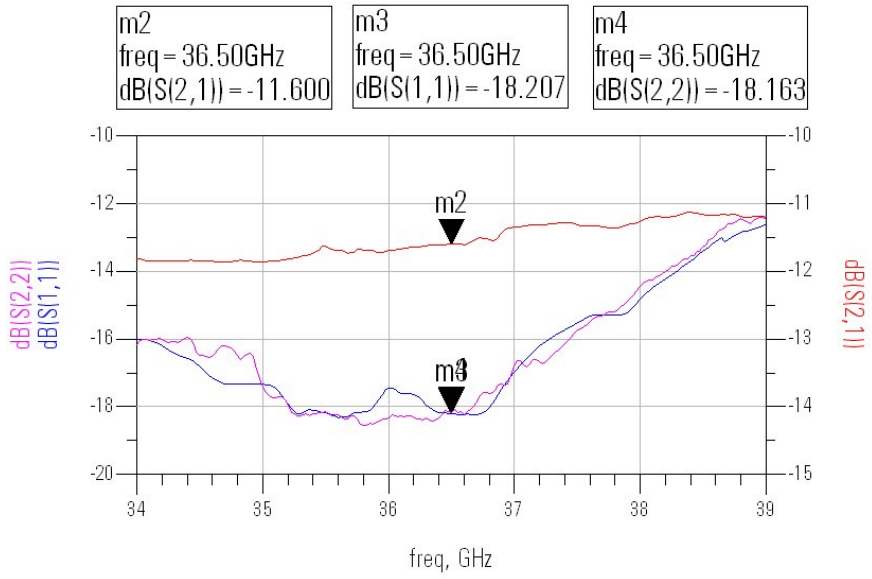

Figure 5.28: Measured attenuator loss and input and output return loss

Since the attenuator is a passive device the noise figure of the attenuator is equal to its loss. The last unknown was the noise figure of the Agilent LNA. No noise calibration was needed since the Agilent amplifier is the last component in the DUT it simply needed to be disconnected from the connecting transmission line and probes could touch down at the input to obtain the noise figure. This was the last measurement because it required the destruction of the transmission line in order for there to be physical room for the probes to touch down on the Agilent amplifier, since they were epoxied close to limit the size of the connecting wirebond. The measured noise figure of the Agilent LNA is shown in figure 5.29.

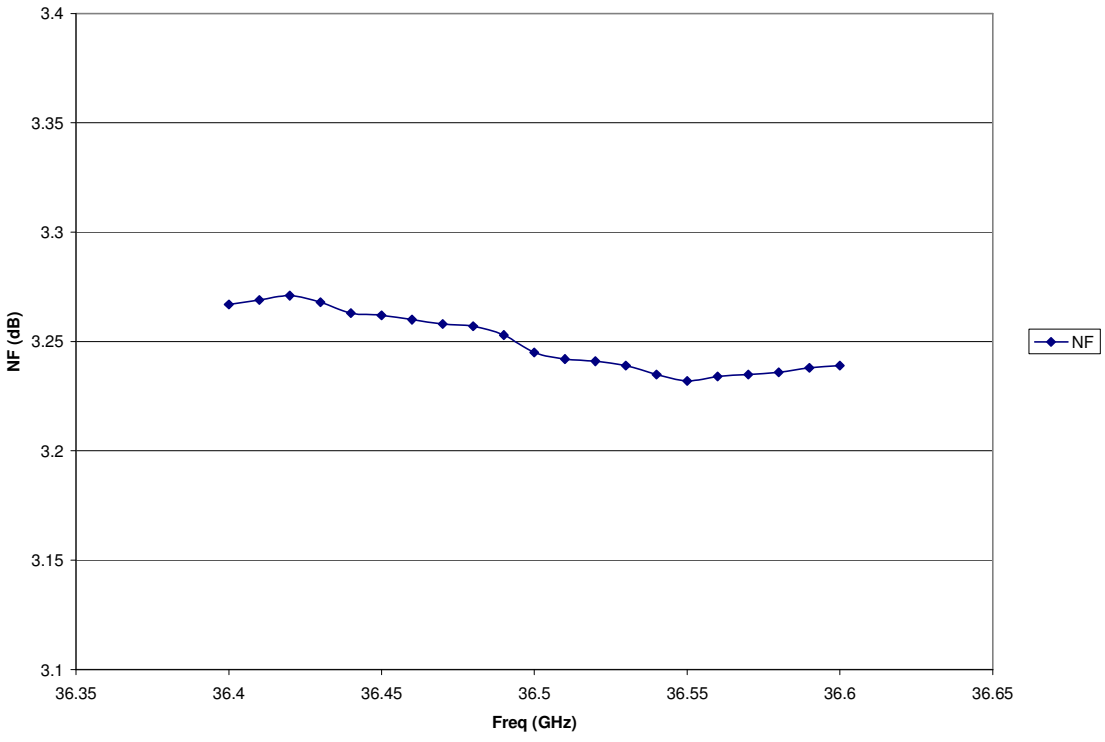

Figure 5.29: Measured noise figure of the Agilent amplifier

As can be seen in figure 5.29 the measured noise figure was around 3.25 dB, which is within the spec sheet noise figure of the amplifier. Now that all the unknowns in the noise figure equation have been determined, the noise figure of the switch LNA was obtained by solving equation 5.2 at all values where the noise figure was measured. An example is shown below at 36.5 GHz when the straight arm of the switch is biased off.

$$F_{swlna} = F_{DUT} - \left(\frac{F_{atten} - 1}{G_{swlna}} + \frac{F_{lna} - 1}{G_{swlna} G_{atten}} \right)$$

$$F_{swlna} = 8.854 - \left(\frac{14.454 - 1}{4.572} + \frac{2.111 - 1}{(4.572)(0.069)} \right)$$

$$F_{swlna}(\mathrm{dB}) = 10 \cdot \log(2.4) = 3.8\,\mathrm{dB}$$

The plots of the calculated noise figure for both the straight and 90 degree switch arms are shown in figures 5.30 and 5.31, along with the predicted simulated noise figure.

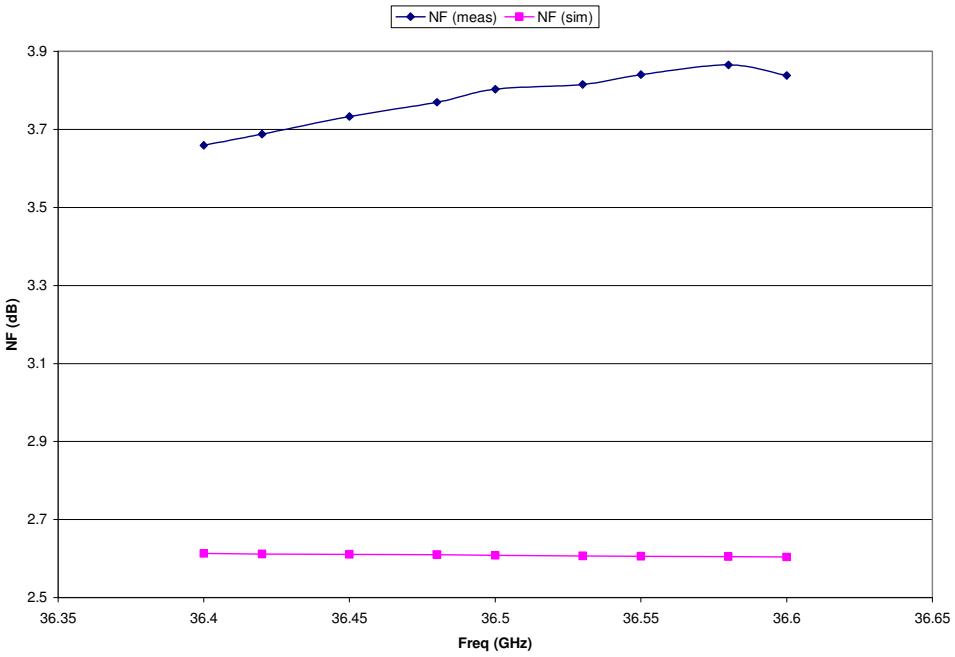

Figure 5.30: Calculated and simulated noise figure based on measured results of the switch-LNA with the straight arm biased off

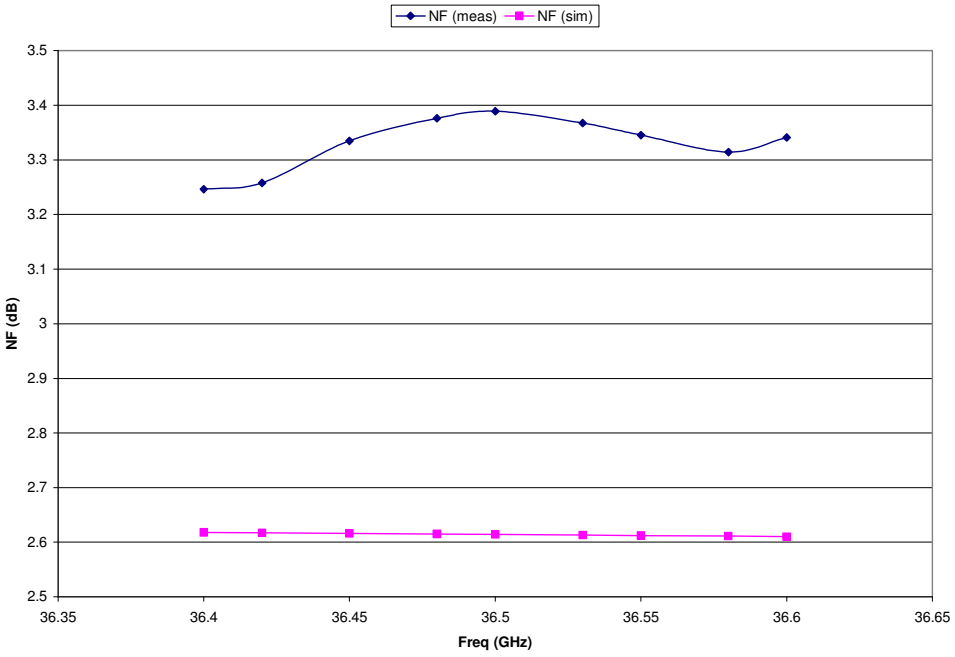

Figure 5.31: Calculated and simulated noise figure based on measured results of the switch-LNA with the 90 degree arm biased off

As can be seen in figures 5.30 and 5.31 the noise figure of the switch LNA is approximately 3.8 dB for the straight arm, and 3.3 dB for the 90 degree input switch arm. This difference is noise figure approximately follows the previous relationship seen between both switch arms. From previous chapters the insertion loss of the switch alone and the gain difference between both input switch arms were both around 0.5 dB.

- **Discussion of NF results**

The calculated noise figure based on measurements is approximately 1 dB higher than what was simulated. This discrepancy can be explained by several reasons. As expected, the mismatch at the output of the LNA did not significantly affect the noise figure since the noise figure is mainly determined by the input matching network. Since the noise source was a waveguide output, ideally the input of the DUT should have had a waveguide input. Although it is only a passive device using a waveguide to 2.9mm adapter at the noise source introduces error that can in effect invalidate the noise source calibration codes, since the ENR values listed for a noise source are given at the output connection plate, in this case at the waveguide output.

More importantly, the need of an attenuator as the second component in the DUT causes problems in the accuracy of the calculation due to the large attenuation. For example, if the attenuator had a variation of 0.5 dB, the calculated noise figure of the LNA could vary from 1.736 dB to 4.944 dB at 36.5 GHz. Since the attenuator is

specified to have a variation of +/- 1 dB at ka band it is possible then that the noise figure is higher due to the differences between the attenuator used in the noise figure measurement and the one characterized, since as described before a measurement of the actual attenuator used in the measurement was not possible. The variation of the attenuator and its affect on the noise figure is shown below in figure 5.32 for the straight arm and in figure 5.33 for the 90 degree arm, respectively.

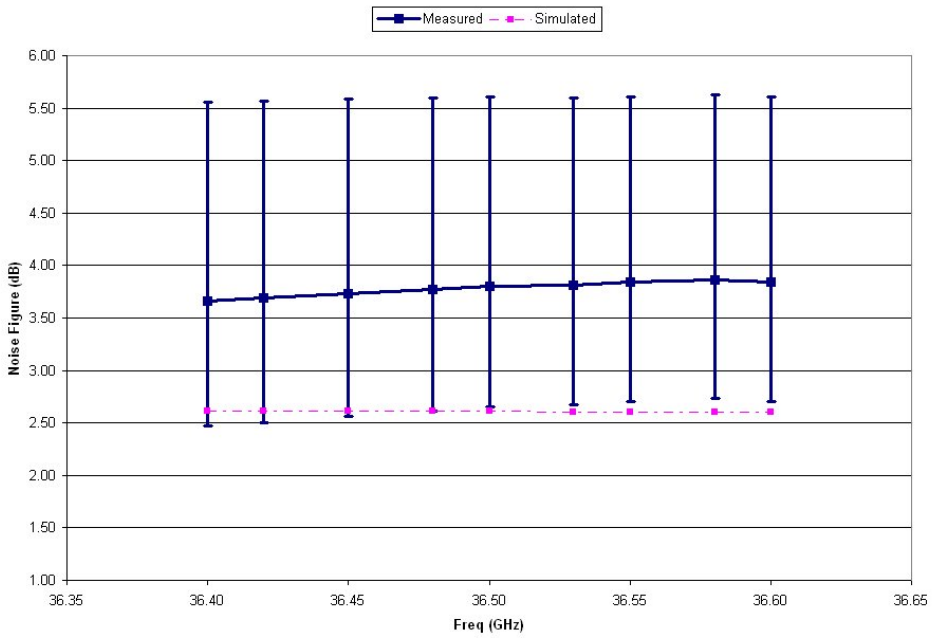

Figure 5.32: Error-bar plot of the measured noise figure for the straight arm

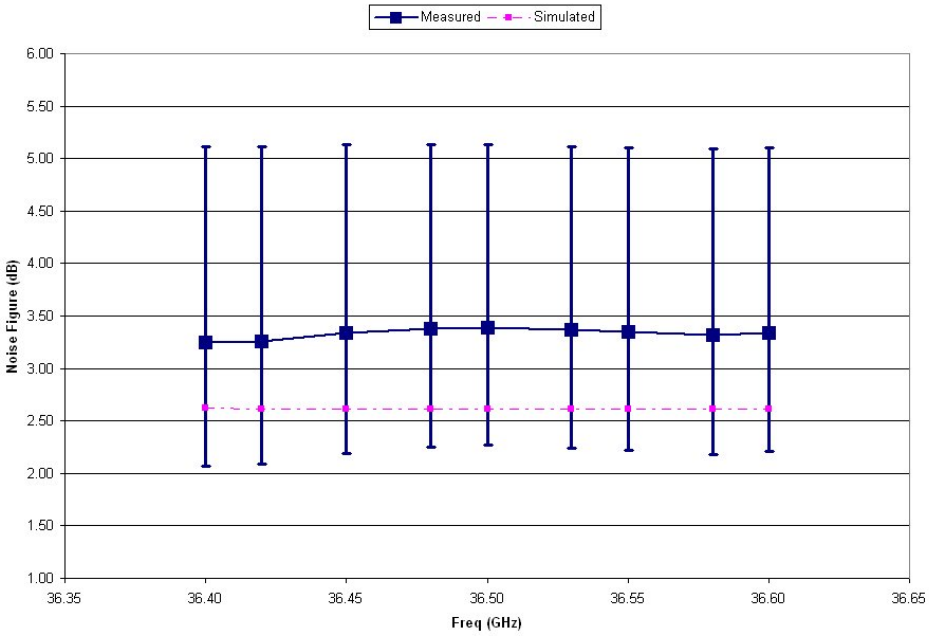

Figure 5.33: Error-bar plot of the measured noise figure for the 90 degree arm

As can be seen in figures 5.32 and 5.33, the error bar plots show the affect the attenuator variation has on the noise figure measurement. The average variation shown is around 1.5 dB. For the straight arm, the lower point of the variations allows the measured noise figure to come within a fraction of a dB of the simulated noise figure, on the other hand, due to the lower loss that occurs when the 90 degree arm is selected the simulated noise figure is within the variation of the noise figure measurements. These variations in the noise figure measurement are significant because of the large attenuation. Had an attenuator with a lower attenuation value been available, a 3 dB attenuator for example, the variations would have been in order of tenths of a dB. Additionally, if the output of the MMIC was properly matched and no attenuator been needed the variations would have been due only to the measurement variations of the

MMIC which would be in the order of +/- 0.4-0.6 dB as previously shown in the error bar plot switch-LNA measurements.

However, the errors that are caused by the variation of the attenuator are minimal compared to the effect the large attenuation has on the calibration. The problem that arises from using a large attenuation is that the output noise figure becomes independent of the noise source and all the noise power is dominated by the attenuator. This in effect invalidates the calibration performed and thus the accuracy of the measurements.

5.3.2: Temperature Measurements

In order to determine the variation of the circuit due to temperature a way to vary the temperature was required. Originally the temperature was going to be varied by using a hot plate, however, this proved to be difficult due to the size of hotplates available and the space available within the probe station. The solution was to use a large resistor that could increase the temperature of the copper board, when a large voltage was placed at the resistor's terminals. The resistor that was mounted onto the board had a value of 10 $k\Omega$. In order to attach the large resistor to the copper board two holes were drilled on to the copper board, and another opening was drilled to allow the thermocouple to be fixed onto the copper board. The location of the large resistor and thermocouple can be seen in figure 5.34.

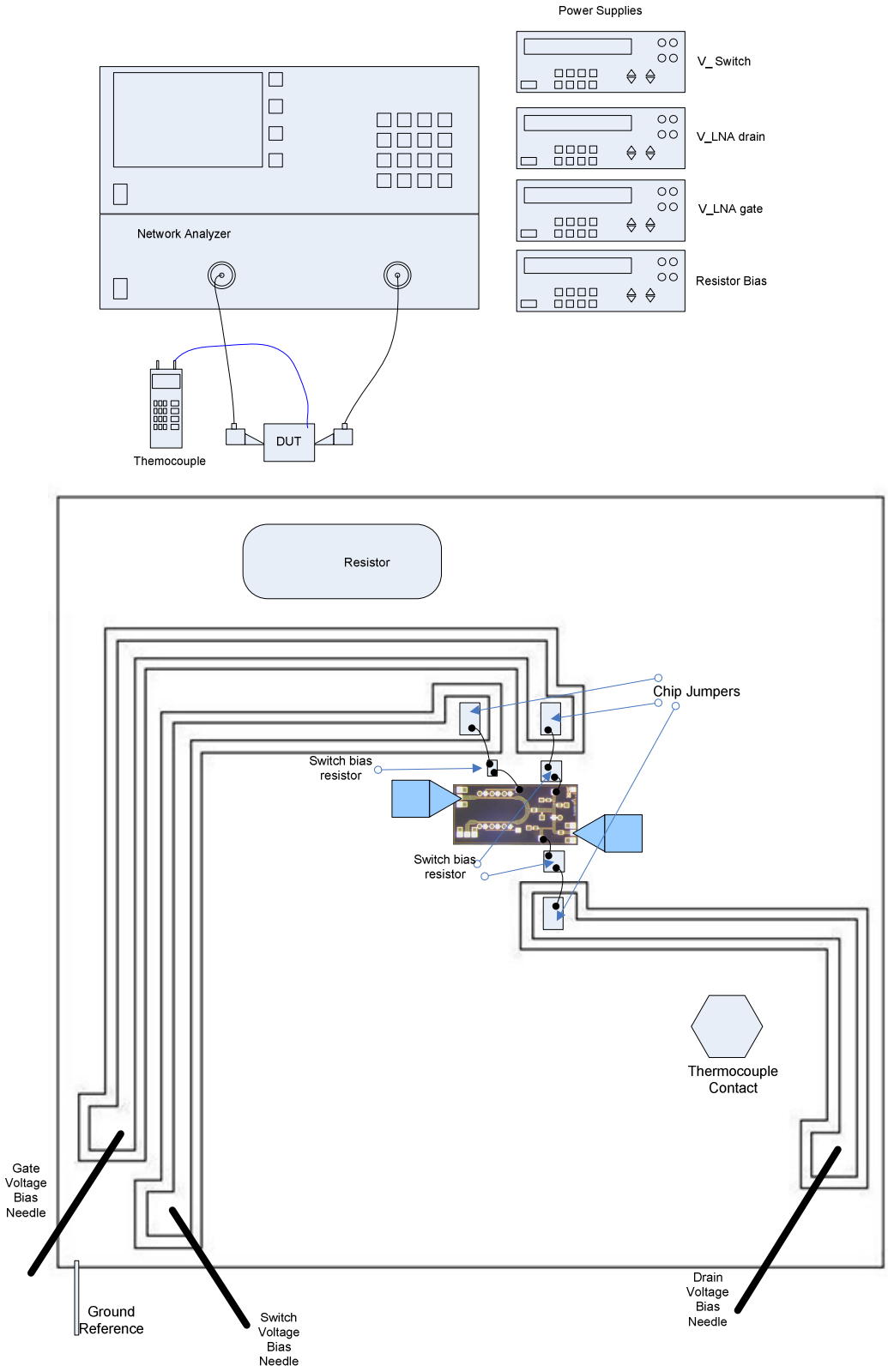

Figure 5.34: Temperature Measurements Set up

During temperature measurements adequate time was given so the temperature could stabilize before any measurement or calibration was made. Additionally, probe calibration was required after each temperature change because not doing so would create errors and invalidate the calibration and therefore the measurements.

Since the “room temperature” is not always constant in a physical room, the initial temperature measured was 24.5 C. The initial temperature change was provided by applying a small voltage across the large resistor; in the event that the initial ambient room temperature was high a fan was used to bring the temperature to 24.5 C. Several tests were performed to determine the voltages that would cause the needed temperature changes. The temperatures at which measurements were made were 24.5 C, 30.5 and 35.5 C, respectively.

The calibration substrate was placed on top of the copper board to allow it to heat to the needed temperature. Once the desired temperature was measured with the thermocouple a probe calibration is performed. The calibration substrate is then removed from the copper board and the bias and probes contact the MMIC. Once the s-parameters were measured for this temperature the probes and bias contacts were removed and the calibration substrate was again placed on the copper board. The RF probes were lifted during temperature changes as a precaution because the MMIC might expand and cause probe skating which can damage the probe. The voltage across the large resistor was then increased to the next temperature, and the identical procedure

was repeated. This was performed for the three different temperatures measured for both arms of the switch-LNA circuit. The measured gain at the three different temperatures for the straight switch arm is shown in figure 5.35, and in figure 5.36 for the 90 degree switch arm.

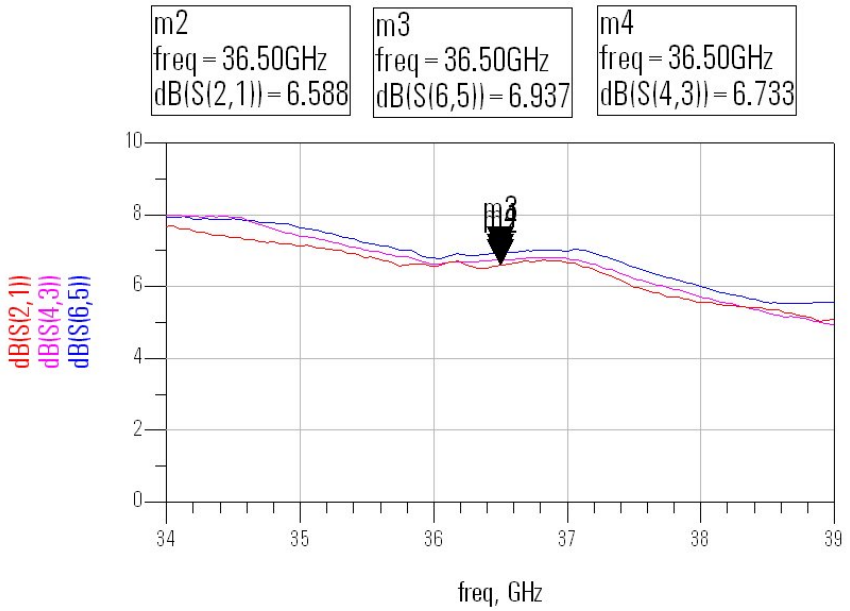

Figure 5.35: Gain variation at three different temperatures for the switch-LNA when the straight arm is biased off

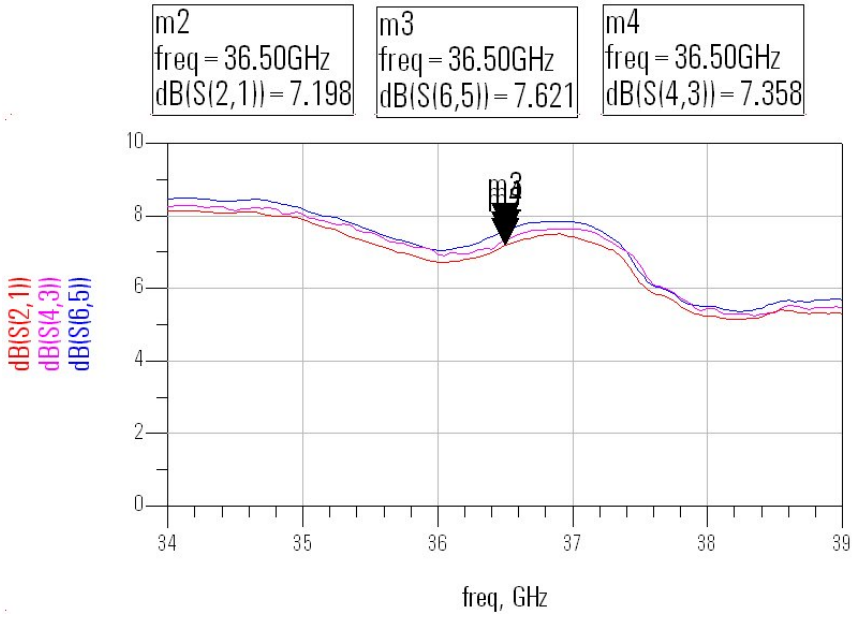

Figure 5.36: Gain variation at three different temperatures for the switch-LNA when the 90 degree arm is biased off

The important characterization, however, is the gain difference between the straight arm and the 90 degree arm and how their variation tracks with temperature. Figure 5.37 displays the difference in gain between the straight and 90 degree arm at each temperature.

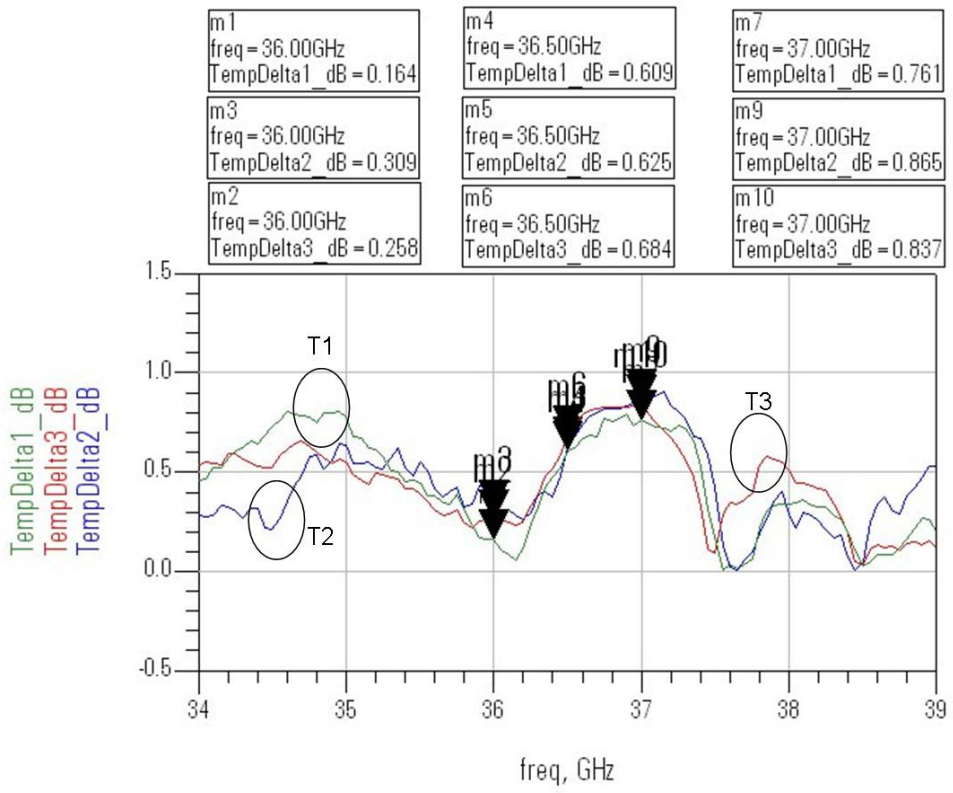

Figure 5.37: Gain difference between straight and 90 degree arm and its variation with temperature

In figure 5.37 TempDelta1 is defined as the gain of the 90 degree bend input minus the gain of the straight arm in dB at all frequencies for the first temperature, 24.5 C, similarly TempDelta 2 and 3 correspond to the gain difference in dB at 30.5 and 35.5 C, respectively. The variation of at each temperature at the low, mid and high end of the frequency range is summarized in table 5.1.

Table 5.1: Summary of the measured temperature variation for the switch-lna

	36 GHz	36.5 GHz	37 GHz
	dB		
TempDelta1	0.164	0.609	0.761
TempDelta2	0.309	0.625	0.865
TempDelta3	0.258	0.684	0.837
STDV	0.0736	0.0395	0.0538

The results shown in table 5.1 show that the MMIC design tracks well with temperature, the average standard deviation is 0.056 dB. Based on these temperature measurements the calibration accuracy of the radiometer can be calculated to be roughly 0.03 dB/K. This value represents the variation that can occur during a radiometer calibration due to temperature changes and not random atmosphere fluctuations.

CHAPTER 6

CONCLUSION

This chapter summarizes the work accomplished in this thesis. Also, future work that could further improve this area of research is mentioned.

6.1: Summary

In this thesis the design and characterization of a mHEMT switch and LNA MMIC at 36.5 GHz was accomplished. Temperature simulations were performed on the circuit and measured. The Switch LNA was designed to have a gain of around 7.7 dB and a noise figure of 2.6 dB. The goal was also to test the temperature dependence of the mHEMT process and to observe the difference due to temperature tracked when considering both switch inputs.

Chapters 1 and 2 provided the background for this thesis and explained the reasoning for the design decisions made in this thesis. Chapters 3 and 4 explained the methodology in the way the design was implemented. Finally, chapter 5 described the test methods followed and presented the results.

Although a layout error caused the output matching network to fail, the overall performance of the design was satisfactory. The measured gain was lower than expected, around 1 dB, due to the mismatch that was occurring at the output. The

measured noise figure of the switch LNA was about 1 dB above the simulated value of 2.7 dB, but due to the large attenuation used during measurement, the noise figure measurements have larger errors than would have been the case if the attenuator had not been necessary. The tracking of both input switch arms is also evaluated and the measured variation was 0.273 K, while the simulations showed a variation of 0.1 K.

Compared to commercially available components the size and performance of this design would be advantageous had the output matching not been degraded. In a current MMIC based radiometer design the switch was around 1.8 mm by 1.8 mm and had an insertion loss of around 2 dB, while the LNA used was 2mm by 1mm and had a gain of 18 dB and 2 to 2.5 dB noise figure, respectively [1]. However, the switch was implemented with p-i-n diodes, and the LNA was a three stage a LNA. In terms of size the combined switch and LNA would take up around 2 mm x 2 mm area, while the design implemented within 2.4 mm to 1.1 mm.

However, due to the low gain of the circuit designed, an additional amplifier would need to be used following the current design. Assuming the chosen amplifier used is the commercially available Agilent amplifier, then the gain at the end of the chain would be 27.1 dB, with a noise figure of 3 dB, while the PIN switch and amplifier would have a gain of 18 dB and a noise figure of 4.5 dB. If two additional gain stages were added within the IC design presented in this thesis the approximate increase in size would be about 1mm in either the vertical or horizontal direction. As mentioned previously the layout of FETs were heavily influenced by the design layout rule that the

gates in the FET cannot be perpendicular to each other. If the current layout is maintained the chip increase would happen in the vertical direction thus making the total size of the chip around 2 mm by 2.4 mm. Another option would be to rotate all the FETs 90 degrees, and add the two consecutive stages horizontally following the current LNA FET. The problem with implementing it in this fashion is that the switch FETS would now require a curved TL between the main signal line of the switch and the drain of the FET, which could negatively impact the switch performance.

6.2: Future Work

The heart of the issue in this topic is the decrease in size of a radiometer while maintaining the current performance or improving it. Following the same theory as system on chip, a good place for future work is to design the majority of the RF subsection on a MMIC, given the performance of the mHEMT process.

.

In terms of the temperature variation issues, a good idea for future work should be to concentrate on designing temperature compensation within the MMIC as done in [33], where a gain temperature variation of 0.02 dB/ K was observed. On chip temperature compensation should keep instrument temperature constant, or at the very least reduce the temperature variation observed.

REFERENCES

[1] Flavio Iturbide-Sanchez, "Private Communication," 2006-2007

[2] Ulaby, F., Moore, R., and Fung, A., *Microwave Remote Sensing: Active and Passive vol.1,* Artech House Publishers, 1981.

[3] Pozar, D.M., *Microwave Engineering, Third Edition*, John Wiley & Sons, 2005.

[4] Ali, F., *HEMTs and HBTs: Devices, Fabrication, and Circuits*, Artech House Publishers, 1991.

[5] Mimura, T., Hiyamizu, S., Fujii, T., Nanbu, K., "A New Field-Effect Transistor with Selectively Doped GaAs/n-As Heterojunctions," *Jpn. J. of Appl. Phys.*, vol. 19, pp. L225-L227, May 1980.

[6] Yngvesson, K.S., *Microwave Semiconductor Devices*, Kluwer Academic Publishers, 1991.

[7] Schwierz F., and J. J. Liou, *Modern Microwave Transistors*, Wiley Interscience, 2003.

[8] Smith, P., Dugas, D., Chu, K., Nichols, K., Duh, K.G., Fisher, J., Mt Pleasant, L., Xu, D., Gunter, L., Vera, A., Lender, R., and Meharry, D., "Progress in GaAs Metamorphic HEMT Technology for Microwave Applications," *IEEE GaAs IC Symposium*, pp. 21-24. Nov 2003.

[9] Pobanz, C., Matloubian, M., Nguyen, L., Case, M., Hu, M., Lui, M., Hooper, C., and Janke, P., "A High Gain, Low Power MMIC LNA for Ka-Band Using InP HEMTs," *IEEE RFIC Symposium Digest*, pp. 149-152, 1999.

[10] Hoke, W.E., Whelan, C.S., Marsh, P.F., Lemonias, P., Lardizabal, S., Leoni, R., Kazior, P.E., Torabi, A., Jang, J.H., Dumka, D.C., Adesida, I., Chang, K.L., and Hsieh, K.C., "Progress in GaAs-Based Metamorphic Technology," *Conf. Dig. GaAs Manufacturing Technology*, pp. 225-229, 2001.

[11] Lardizabal, S., Advances in Microwave FET Technology: A Presentation to EEL 6936: MMIC, *USF Class Notes*, Fall 1999.

[12] Whelan, C.S., Marsh, P.F., Hoke, W.E., McTaggart, R.A., Lyman, P., Lemonias, P., Lardizabal, S., Leoni, R., Lichwala, S., and Kazior, T.E., "Millimeter-Wave Low-Noise and High-Power Metamorphic HEMT Amplifiers and Devices on GaAs Substrates," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 9, pp. 1307-1311, September 2000.

[13] Takasu, H., Sasaki, F., Kawasaki, H., Tokuda, H., and Kamihashi, S., "W-Band SPST Transistor Switches," *IEEE Microwave and guided wave letters*, vol. 5, pp. 315-316, Sep. 1996.

[14] Madihian, M., Desclos, L., Maruhashi, K., Onda, K., and Kuzuhara, M., "A sub-nanosecond resonant-type monolithic T/R switch for millimeter-wave systems applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 1016–1019, July 1998.

[15] Ingram, D., Cha, K., Hubbard, K., and Lai, R., "Q-Band High Isolation GaAs HEMT Switches," *GaAs IC Symposium*, pp.289-292, 1996.

[16] Mizutani, H., and Takayama, Y., "DC-110-GHz MMIC Traveling-Wave Switch," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, May 2000.

[17] Schiendler, M., and Morris, A., "DC-40 GHz and 20-40 GHz MMIC SPDT Switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. mtt-35, Dec. 1987.

[18] Lin, K., Wang, Y., Niu, D., and Wang, H., "Millimeter- Wave MMIC Single-Pole-Double-Throw Passive HEMT Switches Using Impedance-Transformation Networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 1076-1085, Apr. 2003.

[19] Lin, K., Wang, Y., Tu, W., Chen, P., Chang, H., Wang, H., and Wu, R., "Millimeter-Wave MMIC Passive HEMT Switches Using Traveling-Wave Concept," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, Aug. 2004.

[20] Mizutani, H., Funabashi, N., Kuzuhara, M., and Takayama, Y., "Compact DC–60 GHz HJFET MMIC switches using OHMIC electrode-sharing technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 1597–1603, Nov. 1998.

[21] Bermkopf, P., Schindler, M., and Bertrand, A., "A High Power K/Ka-band Monolithic T/R switch," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, pp. 15–18, June 91.

[22] Matloubian, M., "Advances in Millimeter-Wave FET MMIC Technology," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 141-144, 1999.

[23] Whelan, C.S., Marsh, P.F., Hoke, W.E., McTaggart, R.A., McCarroll, C.P., and Kazior, T.E "GaAs metamorphic HEMT (MHEMT): An Attractive Alternative to InP HEMTs for High Performance Low Noise and Power Applications," *InP and Related Materials Conf. Proceedings*, pp. 337-340, 2000.

[24] Henkes, D., "LNA Design Uses Series Feedback to Achieve Simultaneous Low Input VSWR and Low Noise," *Applied Microwave & Wireless*, pp. 26-32, Oct. 1998.

[25] Winson, P., Lardizabal, S., and Dunleavy, L., "A Table Based Bias and Temperature Dependent Small Signal and Noise Equivalent Circuit Model," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 623-626, 1995.

[26] Nosal, Z., "Temperature Dependent Functional Small-Signal and Noise Model of GaAs FET," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1339-1342, 1995.

[27] Lardizabal, S., Dunleavy, L., and Boudiaf, A. "New Aspects Concerning the Bias and Temperature Dependence of Intrinsic Noise Generators in Extracted FET Models," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1325-1328, 1996.

[28] Munoz, S., Sebastian, J., and Gallego, J., "Modeling the Bias and Temperature Dependence of a C-Class MESFET Amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 527-533, Apr. 1997.

[29] Aniel, F., Zerounian, N., Almeyda, A., Danelon, V., Vernet, G., Crozat, P., Adde, R., Harmand, J., and Ladner, C., "High Frequency Analysis of InP Transistors versus Temperature," *Solid-State Device Research Conference*, pp. 708-711, 1997.

[30 Jackson, R.W, "Active Microwave Circuits," ECE 683 Class Notes, Spring 2004.

[31] Lardizabal, S., Dunleavy, L., Yau, W., and Bar, S., "Experimental Investigation of the Temperature Dependence of PHEMT Noise Parameters," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 845-848, 1994.

[32] Agilent Technologies, "AMMC-6241: 26-43 GHz Low Noise Amplifier Datasheet."

[33] Long, A., Holmes, S., and Wallis, R., "Wideband HEMT MMIC low-noise amplifier with temperature compensation," *IEEE Electronic Letters*, vol. 30, pp. 422-423, Mar. 1994.