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Si Based Mis Devices with Ferroelectric Polymer Films for Non-Volatile Memory Applications

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Si BASED MIS DEVICES WITH FERROELECTRIC POLYMER FILMS FOR NON-VOLATILE MEMORY APPLICATIONS

A Thesis Presented

by

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And lastly and most importantly, I would like to say that I am short of words to express my thankfulness to my very important friends during my Masters who provided me the emotional and moral support which helped me struggle through the challenges of graduate student life.

SAI SWAROOP NERELLA

ABSTRACT

Si BASED MIS DEVICES WITH FERROELECTRIC POLYMER FILMS FOR NON-VOLATILE MEMORY APPLICATIONS

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Ferroelectric non-volatile memories have gained momentous importance in the recent years. Significant research is being done on different device structures with several ferroelectric films for better data retention, lower power dissipation and higher density of integration. Metal - ferroelectric insulator – semiconductor (MIS) capacitor structures with Poly Vinylidene Fluoride(80%) - trifluoroethylene (20%) (PVDF – TrFE) copolymer are observed to demonstrate consistent dielectric properties and retainable memory action under selected operating conditions. Prior research was done on devices with MFeOS structure with an oxide buffer layer. The presence of a buffer oxide reduces the field acting on the film for memory state switching, which in effect requires the devices to be operated at higher voltages. In this work, MFeS devices with lower ferroelectric film thickness; with, and without a very thin buffer oxide have been studied. The dielectric behavior of PVDF thin film, when deposited directly on Si, is observed to exhibit reliable memory properties without significant charge injection under certain operating conditions. Electrical characteristics such as capacitance-voltage(C-V) and polarization-electric field (P-E) hysteresis with the direction of measurement and

conduction properties through the junction have been comprehensively studied to establish the behavior of the MIS device for possible use in MIS FETs for high density ferroelectric memories.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

High density and low power memories are crucial in almost all electronic gadgets used in the modern world. DRAM, SRAM and other semiconductor memories used for high speed storage in computers are volatile since they lose the information when powered off. Magnetic disks which are non-volatile, on the contrary, suffer from serious drawbacks of being large, mechanically fragile, slower and discouraging in power consumption. The present day EEPROMS and Flash memories are being widely used for non-volatile purposes that store data as electrical charges in floating gate electrodes. These are still being worked on, to improve their writing times and usage life of the memory. [1, 2]

Semiconductor devices like MOS capacitors and MOSFETs are the building blocks of most of the memory cells. Different materials and device structures are researched for these memory cells according to the requirements, which is a major research area in semiconductors.

Non volatile memories based on ferroelectric materials integrated with semiconductor devices are called FRAMs. These devices have potential uses in military applications which require low power consumption. The ability to hold stable states designated as 0 and 1 under zero bias conditions by proper electrical polarization and reverse polarization, enables us to use it for storage purposes, maintaining the nonvolatile characteristics and high speed read-write frequency. Ferroelectric films are integrated

with MOS and MOSFET devices to exploit their ferroelectric action for switching action and hence data storage. Basic memory cells of such kind which are one transistor-one capacitor (1T-1C) memory cells are found to have a serious drawback of destructive read out or data loss while reading. Memories with Non-Destructive read out capabilities are currently researched which employ single transistor memory cells with integrated ferroelectric materials. This research is aimed at studying in detail the dielectric and ferroelectric properties of Polyvinylidene Fluoride (PVDF) polymer; and suggest its use as a gate dielectric for such transistors cells.

1.2 Ferroelectric Memories

FRAMS would competitively stand in the line of non-volatile memories to avoid the short comings of the types of memories described above, but they do provide challenges which have to be attended to in their material selection and processing procedures.

1.2.1 Reliability of Ferroelectrics

Leakage current and dielectric breakdown can decide the reliability of ferroelectric memories. Data in ferroelectric memories is usually stored as a polarization state of the polarization domains in the material. Since devices can undergo gradual depolarization with time, it could be a serious concern in long term shelf life. Electrical integrity of ferroelectric thin films is dependent on the specific ferroelectric material, processing techniques, thickness and temperatures of processing. Choice of proper material and process techniques can yield high reliability levels with ferroelectric memories.

1.2.1.1 Fatigue

Repetitive switching of the polarization state of a ferroelectric capacitor reduces the ability to read or write data over time. This loss of switchable polarization is called fatigue, which determines the number of read-write cycles a ferroelectric device can withstand. In case of FRAMs data writing is not just necessary for writing but also for reading, and hence ideally the read/write should be operated at as low voltage as possible.

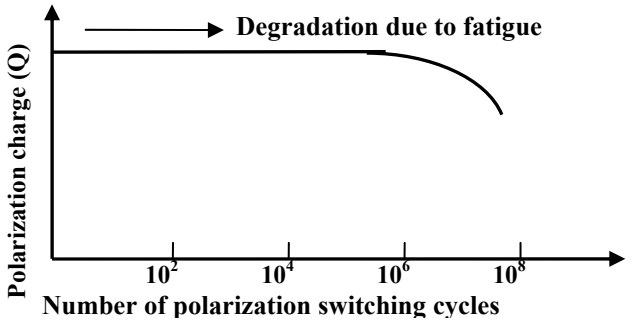


Figure 1.1 Degradation of polarization charge due to Fatigue.

Figure 1.1 describes the fatigue characteristics showing the tendency for polarization charge decrease with the number of polarization reversal cycles.

1.2.1.2 Data retention characteristics

As the time elapses, the polarization charge (Q) decreases, which determines the data retention capabilities or shelf life of the ferroelectric memories. This behavior greatly varies from material to material. This can be noted in Figure 1.2. [1] Appropriate material selection is crucial for good data retention abilities of the memories.

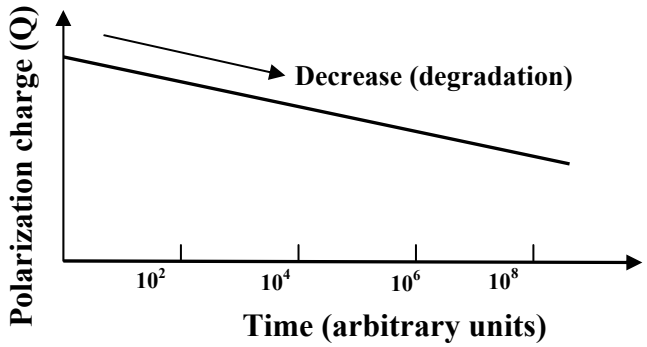


Figure 1.2 Decrease in polarization charge (Q) with time elapsed.

1.2.1.3 Imprint

If the storage element in the ferroelectric memory is repeatedly polarized to the same state, which is not very unlikely sometimes in memories, the state may become a preferred or reinforced state. Switching the polarization of the device to the other state may be rather feeble or suppressed.

1.3 Ferroelectricity

The hysteresis in the polarization of ferroelectric materials makes possible their use in electrically switchable nonvolatile data storage elements. The more commonly implemented ferroelectric data storage element is a capacitor consisting of a thin ferroelectric film sandwiched between two conductive electrodes.

Ability to switch between two stable polarization states of opposite sign constitutes a permanent electric memory of non-volatile nature. The earliest ferroelectric materials used for such studies were ferroelectric ceramic thin films e.g., BST, PZT etc., which require a few tens to hundreds of volts to switch the state, which makes them not suitable for use in the modern semiconductor industry operating at 5V(Si-CMOS), 3V (GaAs) or 2.5V (ultra high density Si). [3] Direct integration of ferroelectric thin films with

Si would enable switching at very low electric fields which are suitable for the semiconductor devices today.

Most ferroelectric materials used for FRAM devices are expressed as a perovskite crystal with the chemical structure ABO_3 shown in Figure 1.3

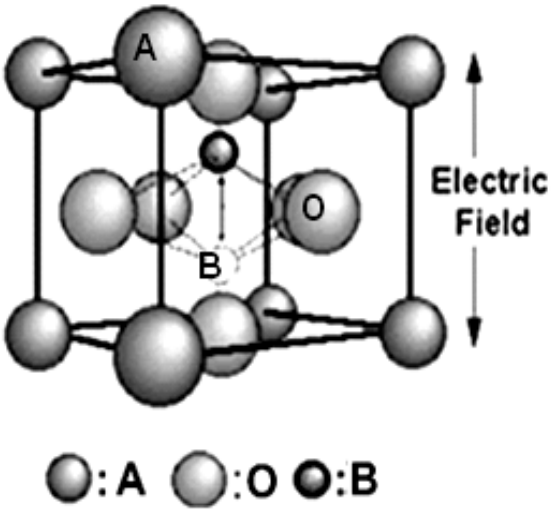


Figure 1.3 Perovskite crystal structure.

Below a temperature called the Curie temperature, the B ion has two stable states; where in the shift of the charged ions by the applied electric field produces electrostatic polarization. These B ions are controlled by the applied electric field in the devices with the ferroelectric material as the dielectric. [3]

The Figure 1.4 demonstrates the non-volatile nature of the ferroelectric memory describing a polarization hysteresis curve. In the absence of any applied voltage to the ferroelectric capacitor, both voltage and dipole moment will remain at 0, 0. If a positive electric field greater than the coercive field (E_c) is applied to the capacitor, the dipoles are polarized in the positive field direction with a polarization value of P_s. When the voltage is removed from the capacitor, then polarization doesn't return to zero, but still holds some polarization called as remanant polarization (P_r).

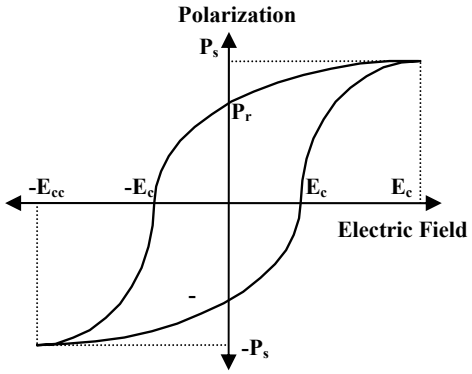


Figure 1.4 Demonstration of the Ferroelectric Property and the Hysteresis curve

If a negative field is applied slowly, then the polarization doesn't turn to the negative direction untill a voltage –Vc called as negative coercive voltage. A maximum reverse polarization of $-P_s$ is recorded only at $-E_{CC}$, and similarly removal of the negative field doesn't remove the polarization, but relaxes the polarization to a value $-P_r$. This represents a bistable operation. The remanant polarization states, P_r and $-P_r$ correspond to the stored data, 0 and 1 respectively. [2]

1.4 Memory Cells

A Typical example of a circuit configuration using a transistor and a ferroelectric capacitor for FRAM applications is shown Figure 1.5.

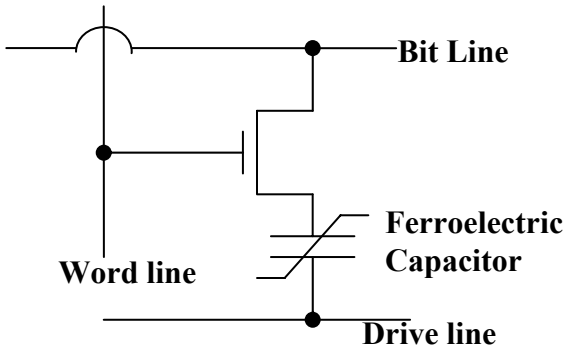
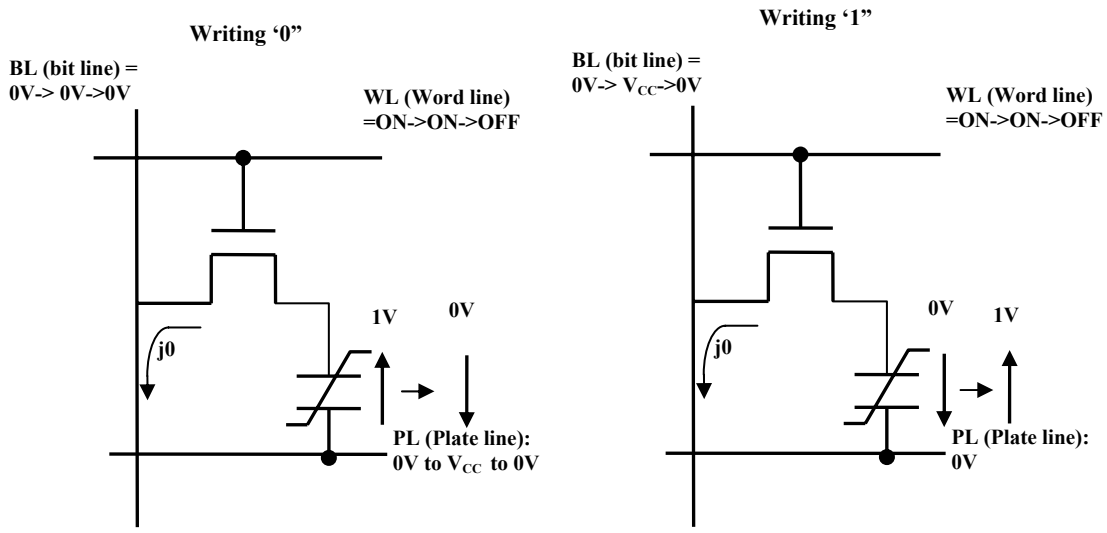


Figure 1.5 A typical memory cell for FRAMs

1.4.1 Memory Cells with Destructive Read Out (DRO)

Memory function in the basic cell described above is implemented by electrical switching of the ferroelectric capacitor device between two states that involves a destructive read out. A voltage of V_{CC} or $-V_{CC}$ needs to be applied to both electrodes of the ferroelectric capacitor in order to write a "1" or "0" to the data cell. Using the Figure 1.6 to understand the writing operation, the word line (WL) is selected to turn the transistor ON and V_{cc} or - V_{cc} is applied between the bit line (BL) and the plate line (PL).



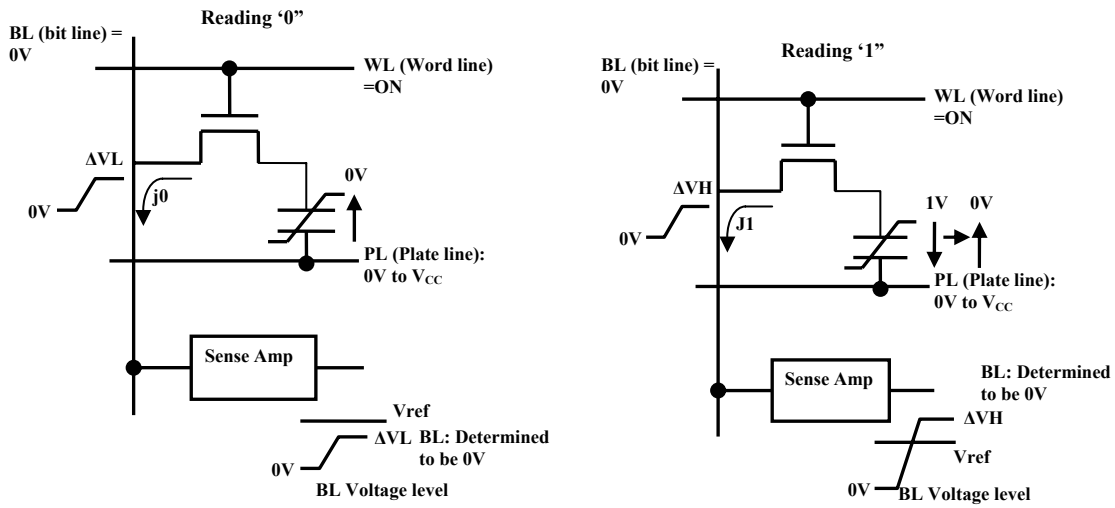
(a) Writing a '0' (b) Writing a '1'

Figure 1.6 Memory cell write operation

Writing "0" data is accomplished by making BL=0 V and PL= V_{cc} and a "1" is written by making BL = VCC and PL = 0V. The data is retained even when the WL line is unselected and the transistor is in the OFF state. This explains the non-volatility of the memory cell. [1, 4]

Before reading the data from the cell, the BL needs to be precharged to 0V, and WL is selected for the cell and V_{CC} is applied to PL. If the cell holds a value "0", the polarization is not reversed, causing a slight movement of electric charge (j0) and this

charges the BL up by ΔVL. On the other hand if the cell holds logic "1", the polarization in the capacitor is reversed and a large displacement current (j1) flows through the BL charging it up by ΔVH. The sense amplifier holding the reference voltage (Vref) decided to be some value between ΔVL and ΔVH detects the signal, so that any voltage level less than Vref is further reduced to 0 and the voltage levels over Vref are raised further to V_{CC}. This is demonstrated in Figure 1.7



(a) Reading a '0' (b) Reading a '1'

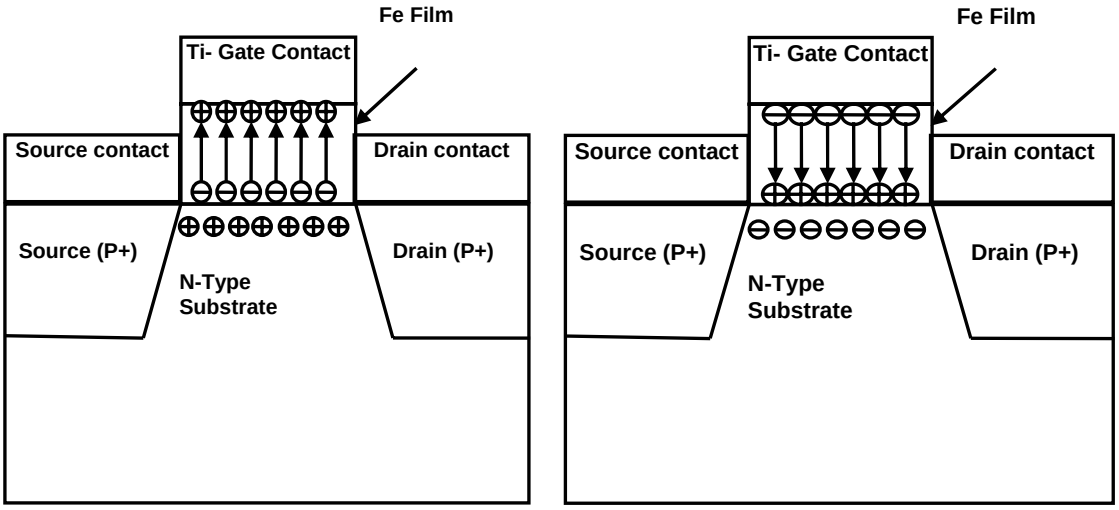
Figure 1.7 Memory Cell read operation

The data is lost during the reading a "1" due to polarization reversal. This loss of written data at one of the polarization states in the read out operation requires a restoration procedure, prior to re-read by a rewriting cycle there by increasing the access time, limiting operation life and enhanced area of memory cell to accommodate additional circuitry. If reading data is "0", the data is not destroyed since no reversal of polarization occurs.

1.4.2 FET Cells for NDRO (Non destructive read out) Capability

For nonvolatile memory with NDRO capability, ferroelectric thin films should be stacked with the gate dielectric in the FET structures. These Ferroelectric FET devices help eliminate the additional circuitry required for data restoration and significantly reduce the area requirements and render high density integration.

Memory operation in such devices is performed by controlling the channel conduction in the transistor by dipole polarization in the ferroelectric film. The polarization state of the ferroelectric material over the gate is set for the desired action which accordingly controls the conductance of the channel over the Si surface behaving like two logic states ON or OFF. [4] One such device structure capable of memory applications is shown in Figure 1.8.



(a) Conduction ON (b) Conduction OFF

Figure 1.8 MFeS FET structure demonstrating an NDRO memory element which stores bit data as the conduction state between the source and the drain of the device.

Ferroelectric gate FETs used for these operations are usually of many different structures and they function like a 1-Transistor (1-T) memory cell without any additional

circuitry required for memory storage and restoration. One of them is the MFS FET which has a layer of ferroelectric material directly interfaced with Si at the gate. Severe charge injection [5, 6, 7]between the ferroelectric materials employed and Si, have largely discouraged working on these devices. Hence buffer layers such as oxides are employed to provide a good interface with Si. Such devices are called MFeOS FETs. But the presence of a buffer layer increases the voltage of operation of the devices due to the field sharing between the two layers. Significant research is being done on these two structures involving various materials to come up with devices with both better switching capabilities and lower voltage of operation.

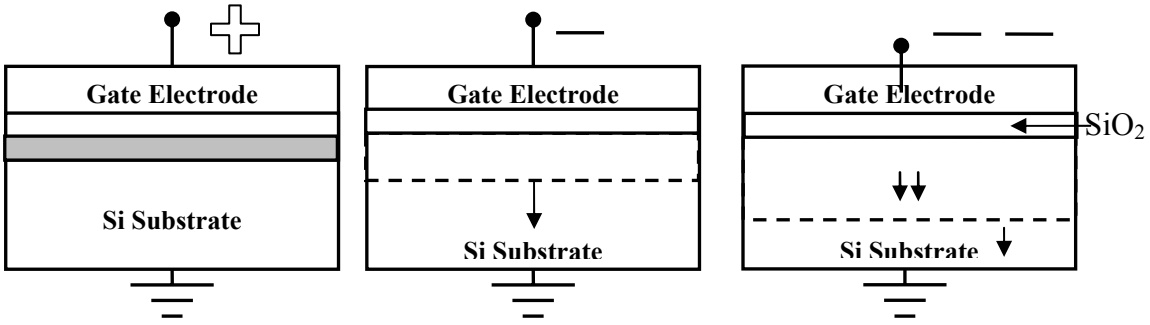
CHAPTER 2

BACKGROUND STUDIES

2.1 MOS Capacitor

The study of the properties of FRAM devices such as MFS, MFeOS Capacitors and FETs employing these capacitor structures in their gates, requires a profound understanding of the underlying physics of a MOS capacitor and its characteristics. The figures 2.1 (a)-(c) show the cross section of a basic MOS capacitor under various conditions. A MOS capacitor has a conducting gate electrode on top of a thin layer of an insulator like silicon dioxide grown usually on a silicon substrate.

The high frequency capacitance – voltage (C-V) measurements of a MOS capacitor show three distinct behaviors, under three different regions of operation. They are called the accumulation, depletion and inversion phases depicted in the three pictures of Figure 2.1



(a) Accumulation (b) Depletion (c) Inversion.

Figure 2.1 Accumulation, depletion and Inversion behaviors of a MOS Capacitor

Considering a capacitor with n-type substrate, a positive voltage +Vg applied to the gate would attract the majority carrier electrons to accumulate at the SiO_2 – Si interface. Since there is no depletion, the device acts as a resistance in series with a

capacitor and the capacitance measured would simply be the capacitance of the oxide, C_{OX}.

If the applied voltage is slowly reduced till it turns negative, the electron accumulation slowly decreases and the electrons are eventually depleted from the interface forming a depletion region. Flat band capacitance, C_{FB} which is a characteristic of capacitance of a MOS structure can be computed by,

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_D} = \frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_0 \varepsilon_{si}}$$

where L_D is the Debye length defined as $L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{si} kT}{q^2 N_D}}$. Charge balancing by a positive charge in the substrate is necessary to account for any negative charge on the gate for charge neutrality. [8, 9, 10]

$$|Q_G| = |Q_D| = N_D L_D$$

where Q_G and Q_D are the units of number of charges / cm^2, and N_D is the doping concentration in the substrate. The total capacitance is C_{OX} in series with the varying C_D, the depletion capacitance.

If the negative bias at the gate is further increased, the Si surface will be inverted from n-type to p-type. The negative voltage on the gate attracts the minority carriers (holes) into the interface. The gate voltage at which this occurs is called threshold voltage V_{TH}.

In all the regions the charge at the gate is opposed by an equal charge in the substrate. Hence,

$$|Q_G| = N_D L_D + |Q_I|,$$

where Q_I is the charge density in the inversion layer. Q_D being lower during depletion, the additional gate charge during inversion is balanced by Q_I. W_D reaches a maximum value yielding the least capacitance. This is given by

$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \frac{1}{C_{D\min}} = \frac{1}{C_{ox}} + \sqrt{\frac{4kT\ln(\frac{N_d}{n_i})}{\varepsilon_0 \varepsilon_{si} q^2 N_d}}$$

where ε_o is the permittivity (F/cm^2) of free space; ε_{si} is the permittivity of Si, which is 11.7; T (K) is the ambient temperature; k is the Boltzmann's constant, and q the electronic charge.

2.2 Polymers for Ferroelectrics

The chemical inertness of polymers to Si enables them to be easily processed as thin films by solution techniques at relatively low temperatures, which is controllable and stable for device fabrication. The low dielectric constants of polymers as compared to ferroelectric ceramics account for their high voltage sensitivity. [11, 12] The polymer synthesis and processing technology today can produce very reliable high purity films with excellent switchability and data retention properties. This study is devoted to a copolymer of poly-vinylidene fluoride known as PVDF (80%) and trifluoroethylene (20%) (PVDF - TrFE). The use of TrFE suppresses the temperatute of the paraelectric phase transition which provides more spontaneous polarization with the switching field applied. [13]

2.3 Poly vinylidene fluoride (PVDF)

Polyvinylidene fluoride has its applications in the chemical-process industry, various electrical and electronic devices, as a weather resistant binder for architectural

finishes, and other areas requiring high performance thermoplastic and fluoroplastic attributes. The polymer can be easily processed by traditional solvent techniques, and it is highly inert to severe chemical, thermal, ultraviolet, weathering and oxidation environments which makes it ideal for semiconductor processing. Mechanically it is very similar to the tough thermoplastics used in high temperature environments. It has high mechanical integrity at the temperatures ranging from -60 to 150^{o} C and it has high heat deflection temperature. Well oriented PVDF films and fibers have high resistance to elastic deformation under load which makes them very ideal for flexible/plastic memories in the future. [14]

PVDF has a large dipole moment of 2.1D associated with the electropositive carbon and the electronegative fluorine in the perpendicular direction to the chain axis. [15] The chemical tructure of PVDF can be seen in Figure 2.2 Since the dipoles are rigidly attached to the main chain carbons, their orientation is responsible for the ferroelectricity of the material. A relatively lower dielectric constant of the PVDF (~10-15) as compared to ferroelectric ceramic materials, permits the use of native SiO_2 as buffer layer staying within the limits of the depolarization fields. Added to that, PVDF has high remanant polarization value and fast dipole switching properties.

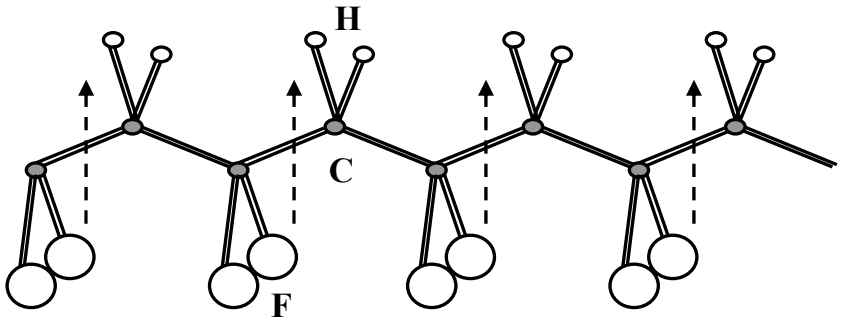


Figure 2.2 Dipole moment in PVDF

PVDF can be crystallized in the orthorhombic β-phase with low temperature processing in the range of 80^{o} C - 140^{o} C. The quasi-hexagonal polar packing of PVDF by crystallization is depicted in Figure 2.3. [13]

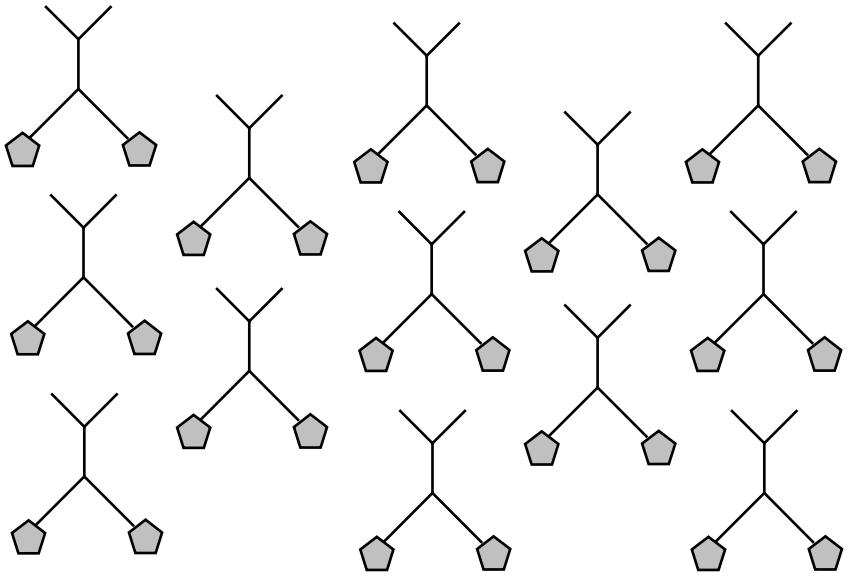


Figure 2.3 Alternating quasihexagonal β-phase crystallization of PVDF

CHAPTER 3

GOALS AND CONTRIBUTIONS

The goal of the research involved in this thesis is to study the behavior of PVDF - TrFE copolymer as a gate dielectric for ferroelectric memory devices with non-destructive read out capability and explore the electrical properties of the ferroelectric polymer-Si MFeS structure with both n and p-type substrates of different resistivities. We have observed that PVDF exhibits MOS behavior which helps us to use it as both, a ferroelectric material and a gate dielectric. A very thin layer of the copolymer film needs to be studied for low power operation of devices. It would also be required to study the film in conjunction with a thin (150nm) buffer layer of SiO_2 to comparatively study the suppression of charge injection in the presence of a buffer oxide.

This thesis involves studying the properties of PVDF as ultra thin (50-120nm) films as opposed to the high thickness(450nm) studies explored earlier, and analyze its behavior as an MFeS capacitor with, and without a buffer oxide layer, which could be listed as

a. Standardizing the process for the most promising film deposition at low temperature.
b. Fabrication of the different MFeS and MFeOS devices required.
c. Measurements for analytic and quantitative study of the electrical characteristics of the PVDF/ Si in MFeS type devices; and film/oxide and oxide/Si interfaces in the presence of a buffer oxide layer in MFeOS type devices.
d. Investigate the rewards and shortcomings in using the PVDF copolymer as a gate dielectric.

CHAPTER 4

PLAN OF STUDIES

Significant work was done employing different ferroelectric ceramics in series with the gate dielectric in the MFeOS structure. Most recent work was done on the electrical characteristics of the PVDF-TrFE integrated gate, MFEOS structure [16, 17] with the thickness of the ferroelectric film as high as 4500A°. These devices operated in a bias range of ~35V and above. A significant fraction of this applied voltage is shared by the SiO_2 buffer layer. It was observed for the first time, that the PVDF film exhibits MOS action in itself in addition to its ferroelectricity. This would suggest an opportunity to eliminate the buffer oxide in the ferroelectric memory devices and study the MFeS structure which could operate at much lower voltages, significantly reducing the power consumption.

The summarized studies involved in this thesis are

a) Fabrication of (metal-ferroelectric-metal-Si) MFeM, MFeS and MFEOS device structures with ferroelectric polymer thin film using the solvent spinning technique and demonstration of low temperature device processing.
b) Study of the C-V characteristics of PVDF film in MFeM and MFeS device structures and establishment of its MOS behavior for its use as a dielectric in ferroelectric FETs.
c) Study of the shift in the C-V characteristics under different poling conditions of the molecular dipoles in the ferroelectric film to demonstrate the ferroelectric behavior.

d) Recording the bidirectional C-V measurements for C-V hysteresis to demonstrate its bistable operation and quantitatively study the memory window by recording the shift in flat band voltage.

e) Study of the C-V characteristics of PVDF deposited on a thin oxide in MFeOS structure and comparative analysis of the behavior of MFeOS and MFeS devices. This includes the study of capacitive properties, hysteresis effect, flat band analysis, and the theoretical analysis of the field distribution under different bias.

f) Study of the polarization hysteresis (P-E) characteristics of the PVDF in the three different devices and interpretation of these behaviors, particularly the asymmetry recorded in the remanant polarizations and coercive voltages, with both thick and thin SiO_2 buffer oxide layers.

g) Study of the junction properties in MFeS devices made on p-type Si instead of n-type Si and also the effects of employing higher resistivity Si wafers.

h) Examination of the charge injection possibilities and effects of space charge on the polarization of the film, by performing the necessary I-V measurements to analyze the conduction through the film.

A detailed description of the experimental work involved in this research is summarized in Chapter 5.

CHAPTER 5

EXPERIMENTS

This chapter details the device fabrication and experiments required for the study.

5.1 Device Structure Fabrication

5.1.1 MFeM structure

It was required to fabricate devices with MFeM structure as shown in Figure 5.1 to study the behavior of the ferroelectric copolymer (PVDF-TrFE) as a very thin film (~120 nm).

Well polished n-type Si wafers with a resistivity of ~1.0 ohm-cm were cleaned using a summa cleaning solution at 45^{o}C and a 150 nm thick Ti-metal film was deposited using thermal evaporation at high vacuum. This was followed by a deposition of a 120 nm thick PVDF film.

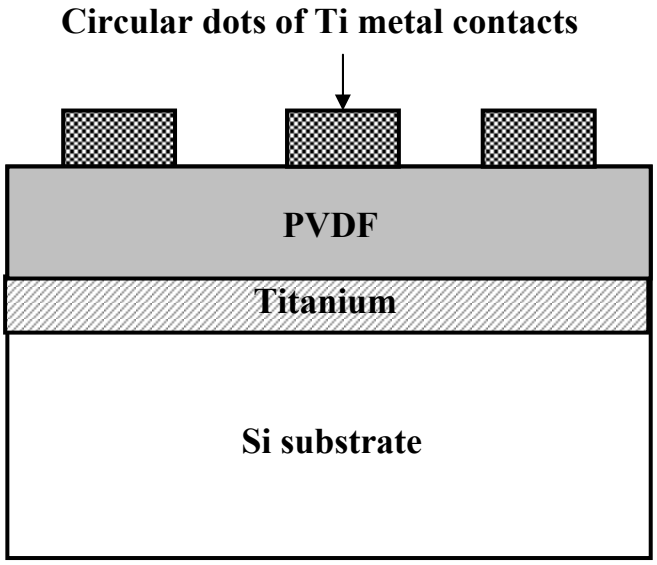


Figure 5.1 Structure of an MFeM device

The PVDF Film was deposited by spin coating the sample with a dilute solution of 1.5wt% of pure PVDF-TrFE in diethyl carbonate (DEC) under isothermal conditions. The spinning was performed at a rate of 2000 rpm at 80^{o}C under a N_2 ambient and repeated to form a three layer deposition for consistency of deposition and for a desired thickness of 120 nm. Each spin coat was followed by a bake process for 15 minutes at 145^{o}C. Thermal processing and spinning conditions determine the crystal structure and morphology of the film after deposition. This was followed by rapid thermal annealing of the sample at 140^{o}C for 45 minutes. This is essential to form the orthorhombic β-phase of the crystal structure. A better annealed and crystallized sample yields better polarization and improved fatigue handling capabilities. [5, 16, 17, 18]

An array of circular top contacts of area ~3 X 10^{-4} cm^2 was deposited through a shadow mask by thermal evaporation of Ti in a high vacuum system operating at 1 X 10^{-8} Torr vacuum. Adequate precaution such as thermal protection is taken to prevent the damage of the co-polymer film surface.

5.1.2 MFeS structure

To study the properties of PVDF as a gate dielectric with ferroelectric switching properties, devices were fabricated with an MFeS structure as described in Figure 5.2. Ferroelectric thin films of P(VDF-TrFE) were deposited on two different <111> oriented n-Si wafers with resistivities of 0.02-1 ohm.cm and 5-15 ohm.cm respectively. These devices were fabricated in order to understand the effect of the resistivity of free Si on the device properties. Identical samples were also prepared on a <111> oriented p-type Si substrate of resistivity ~1-5 ohm.cm to analyze the device behavior with a p-type

substrate. All the devices are completed with the deposition of an array of circular dots of Ti on top and aluminum on the back, to create the metal contacts.

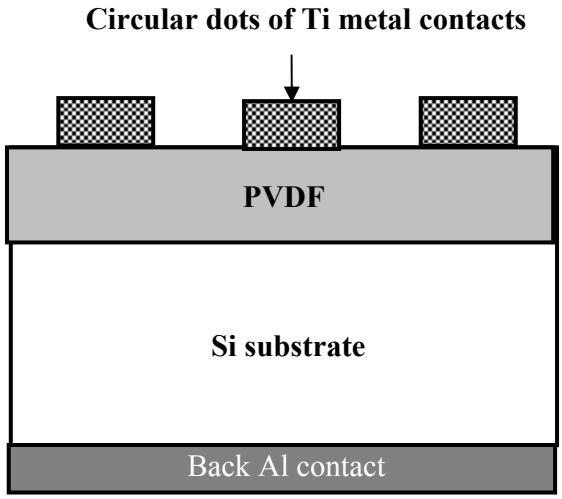


Figure 5.2 Structure of an MFeS device.

5.1.3 MFeOS Structure

Devices with very thin buffer oxide were fabricated to form an MFeOS structure, to examine charge injection behaviors with and without a buffer oxide. The structure of these devices is shown in the Figure 5.3. The presence of an oxide layer which could share the applied field can increase the combined operating voltage of the devices; hence a very thin (15 nm) layer of SiO_2 is employed for the studies.

These devices were made on a <111> oriented n-Si wafer. A 150A^o thick SiO_2 layer was grown by thermal oxidation at 1100^{o}C. This was surfaced with a deposition of the ferroelectric thin film in an identical procedure described above; followed by forming an array of circular top Ti metal contacts. The back obmic contact to the MFeOS device structure was formed by depositing a thick aluminum film on the back side of the sample.

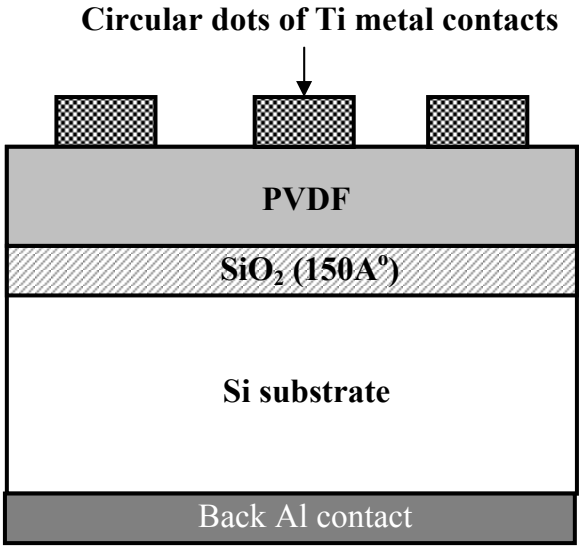


Figure 5.3 Structure of an MFEOS device

5.2 Data Acquisition

The polarization-hysteresis (P-E)) characteristics were recorded in the computer-controlled ferroelectric tester Precision Pro with Vision-Pro software from Radiant Technology Inc. Polarization-electric field hysteresis curves were obtained by the hysteresis function in the Vision Pro software. Hysteresis curves were generated with a standard bipolar profile with parameters of 0 offset and pre-loop delay of 100 ms.

The capacitance-voltage (C-V) measurements performed in this study were at a high (500 KHz) frequency, usually in a sweep direction from the inversion region towards the accumulation region. This frequency was selected after a series of experiments with different frequencies, to choose a right compromise between the dipole response times and the noise in the recordings. For higher accuracy, the data was measured with 200points. The program sweeps the voltage through a set of discrete values from 0V to the voltage assigned $\pm V_{max}$ then back to 0, and starts a second cycle towards $\mp V_{max}$, and then back to 0V. Two sets of such CV measurements are required

with this program to obtain the information for the CV Hysteresis which is shown in Figure 5.4. The data which was considered is shown in bold line and the discarded data is shown in dotted lines. The data corresponding to the dark line is used to plot C-V hysteresis curves.

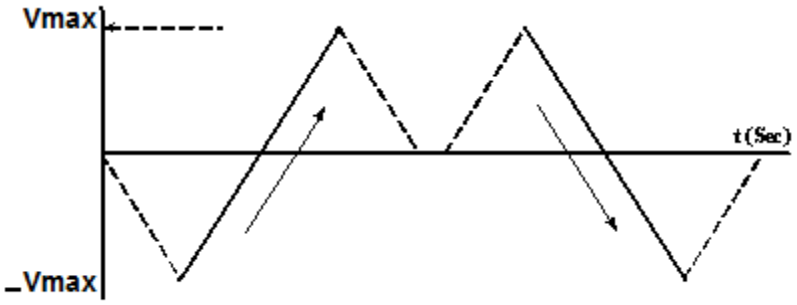


Figure 5.4 C-V Data acquisition showing redundant data in dotted lines

I-V characteristics of the devices were recorded to investigate charge injection effects. These were recorded using a computer controlled Keithley 2400 source meter with a software application developed for the RS-232 interface by programming in Visual Basic. This required the use of a commercial Active – X control object provided by Active Experts Inc. This interface takes small programs of SCPI commands as inputs through the RS-232 serial port and programs the meter to take measurements on the device. It then acquires the output data from the source meter and sorts the data based on the measurements taken and exports them to an external spreadsheet application like Microsoft Excel. The interface provides facility to control the parameters for the RS-232 communication like baud rate, parity and transmission settings. A log file is also generated to keep log of the activities in the application. A screenshot of this application is shown in Figure 5.5.

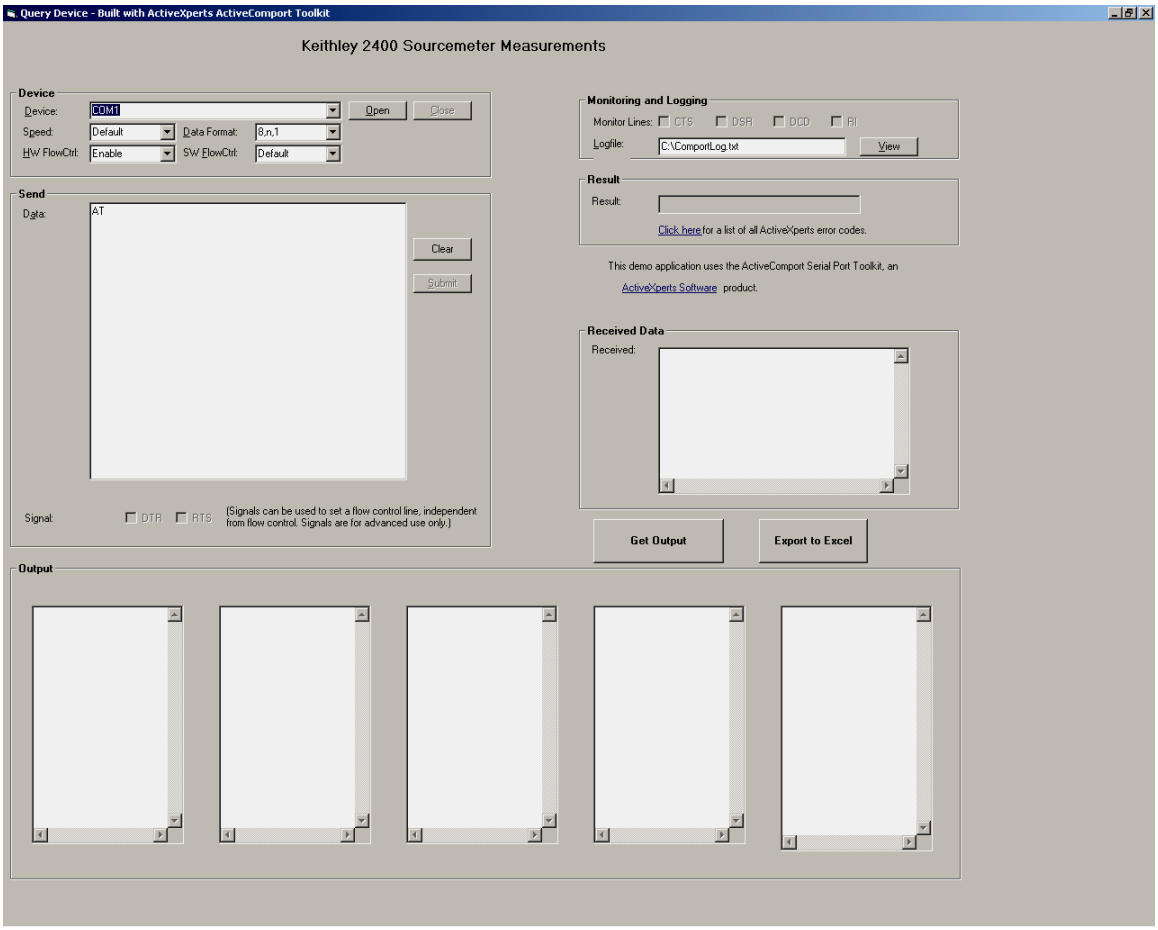


Figure 5.5 RS-232 Interface for I-V measurements developed in Visual Basic 6.0

CHAPTER 6

RESULTS AND ANALYSIS

6.1 Electrical properties

6.1.1 Dielectric action of PVDF

MOS Action in the PVDF/Si interface was demonstrated for the first time by the C-V characteristics of PVDF in the MFeS device structure as shown in Figure 6.2. Experiments were conducted to evaluate the ferroelectric behavior of the PVDF film in a capacitor structure between two metal electrodes in the devices with MFeM structure. C-V characteristics of such a device in Figure 6.1 shows both the -25V to +25V and the +25V to -25V directions of sweep. This characteristic, also known as butterfly dielectric characteristic establishes the ferroelectric nature of the PVDF copolymer film. This C-V behavior of PVDF is significant in analyzing the C-V curves of MFeS and MFeOS devices which will be described later.

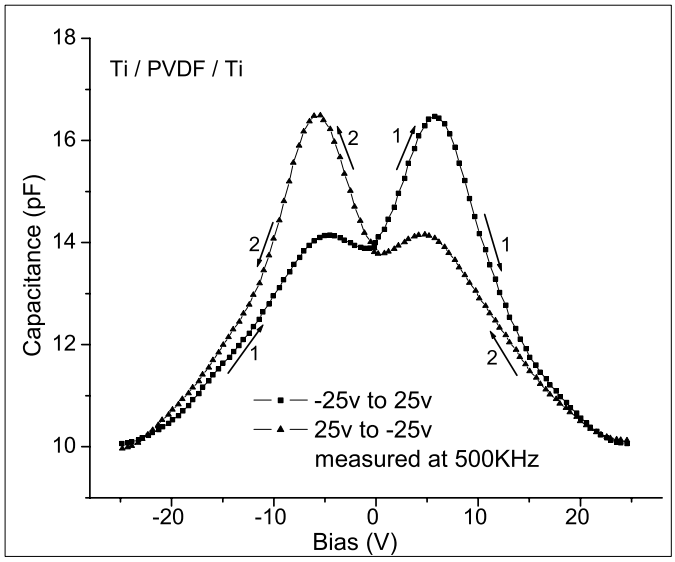


Figure 6.1 C-V measurements of PVDF Copolymer film in the MFeM Device

Figure 6.2 shows that PVDF can act as a good gate dielectric in Si based devices substituting gate oxides. The three regions of MOS action showing accumulation, depletion and inversion behaviors are clearly seen in MFeS devices at the PVDF-Si interface. The threshold voltage V_{TH} which marks the onset of deep inversion is observed at ~6.48V for the sample under study. Flat band voltage (V_{FB}) shift was measured as 1.52V from the theoretical value indicating the presence of fixed charges. The magnitude of these charges can be computed by $Q_i = -C_{Acc}.\Delta V_{FB}/qA$ which was calculated to be 8 x 10^{10} cm^{-2}. A decrease in the accumulation capacitance noticed at higher voltages could be due the low non-linear capacitance value of PVDF at those voltages (Figure 6.1) in series with the capacitance of the accumulation layer. The effective capacitance C_{eff} is given by,

$$\frac{1}{C_{eff}} = \frac{1}{C_{Si}} + \frac{1}{C_{Fe}}$$

Where C_{Si}, C_{Fe} are the capacitances of the Si surface charge layour and the ferroelectric film respectively.

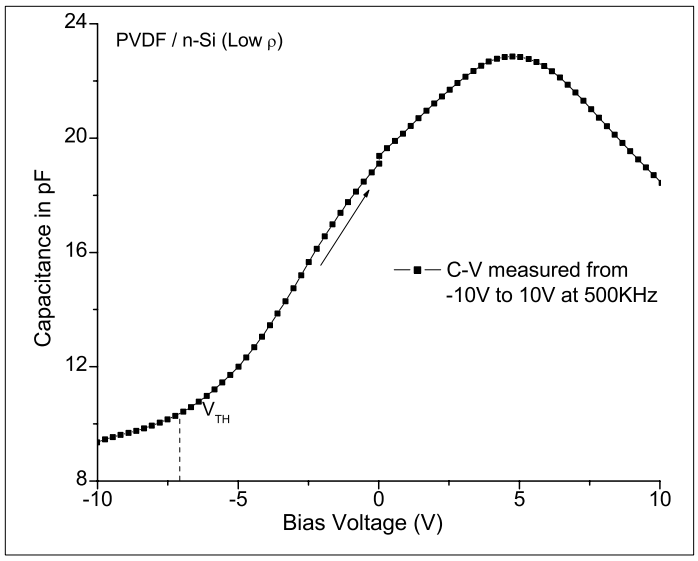


Figure 6.2 C-V characteristic of PVDF on Si in MFeS device showing MOS action.

6.1.2 Conduction properties

To understand the conduction properties through the film, various current transport mechanisms were examined on the devices and I-V measurements were performed which are presented in Figure 6.3.

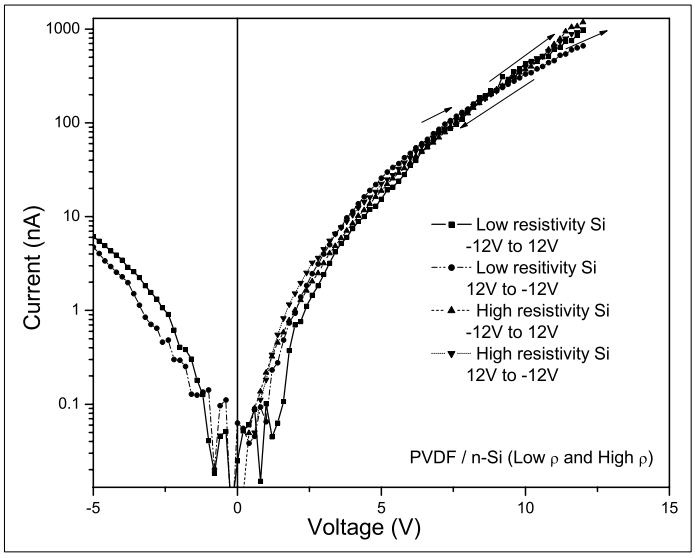


Figure 6.3 I-V measurements on MFeS devices showing non-linear increase in leakage current at gate voltages above 4V.

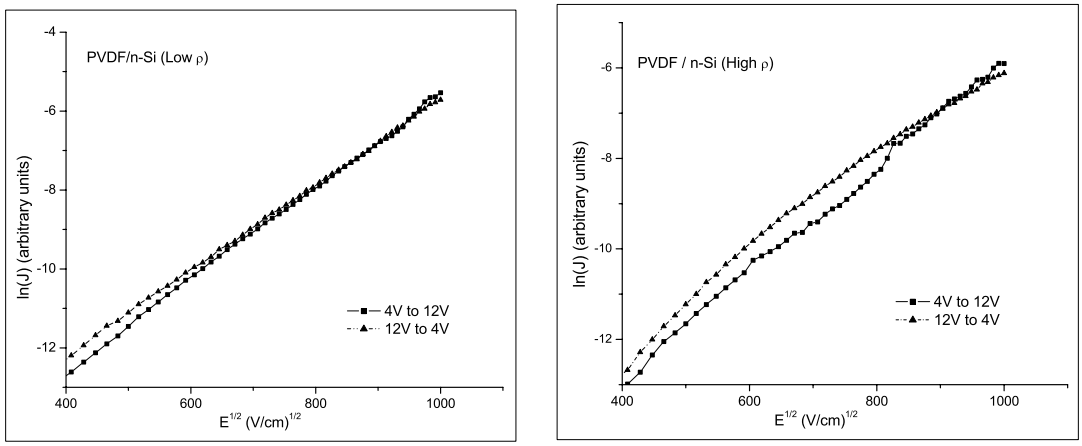
The leakage current was found to increase non-linearly at positive gate voltages beyond 4V. Hence detailed studies were done to study the conduction when the gate voltage is positive. The current non-linearly increases in the range of 4V to 12V, which implies that charge injection is most likely of the electrons injected from the n-type substrate in forward bias at negative voltages. The type of conduction that occurs is not completely understood. Nevertheless, among the different modes of current transport, it was found that the I-V measurements best fit the Schottky emission characteristics. The Schottky emission can be electrically characterized as, [19, 20, 21]

$$J = A^* T^2 \exp\left(\frac{\beta_s E^{1/2} - \phi_s}{k_B T}\right)$$

where $\beta_S = \left(\frac{e^3}{4\pi\varepsilon_0 \varepsilon} \right)^{1/2}$ where e is electronic charge, ε_0 is the dielectric constant of free space, ε is the dielectric constant, A^* is the effective Richardson constant, T is the absolute temperature, ϕ_s is the contact potential barrier, E the applied electric field and k_B, the Boltzmann constant.

A^* is the effective Richardson constant, given by $A^*/A=m^*/m_0$, where A is the Richardson Constant ~120A/cm^2/K^2 and, m^* and m_0 are the effective mass and free-electron mass, respectively for the substrate under study. The value of m^*/m_0 for n-type Si <111> is about 2.2 and for p-type it is about 0.66.

The Theoretical value of β_s can be computed using an assumed value for the dielectric constant of PVDF ~8-12. This is found to yield values of β_s in the range of 3.53x10^{-23} J cm$^{1/2}$/V$^{1/2}$ to 4.32x10^{-23} J cm$^{1/2}$/V$^{1/2}$.



(a) Low Resistivity (ρ) Sample (b) High Resistivity (ρ) Sample

Figure 6.4 Plots of $\ln(J)$ with $\sqrt{E}$ for the MFeS devices with both low resistivity and high resistivity

Rearranging the previous equation, and computing the natural logarithm on both sides, the expression reduces to,

$$\ln(J) = \frac{\beta_S}{k_B T}\sqrt{E} + \ln(AT^2) - \frac{\phi_S}{k_B T}$$

The plots of $\ln(J)$ with $\sqrt{E}$ for the MFeS devices with both low resistivity and high resistivity substrates are presented in Figure 6.4. Based on the above expression, the slope of the plot of $\ln(J)$ with $\sqrt{E}$ yields an experimental value of β_s. This was found to be ~3.66 x 10-^{23} J cm$^{1/2}$/V$^{1/2}$ to 4.32 x 10-^{23} J cm$^{1/2}$/V$^{1/2}$ for the different I-V curves measured on different devices. This is in agreement with the theoretical value computed for β_s demonstrating that Schottky emission is the dominant current transport mechanism through the PVDF/n-Si interface. The Schottky barrier height ϕ_s as computed from the plots was found to be ~0.83- 0.86eV.

A detailed analysis of charge injection and its effect on the other device properties is presented in Section 7.4 on Charge injection.

6.2 Ferroelectric Behavior

6.2.1 Polarization Properties of PVDF Film

Polarization – Electric field (PE) hysteresis measurements were recorded on the devices with PVDF film to ascertain relevant parameters such as remanant polarization (P_r), coercive voltage (V_c), maximum polarization P_s which indicate the strength and response parameters of the ferroelectric film.

To establish the properties of the film under identical thickness and processing conditions , the P-E properties of PVDF were first studied in a device with MFeM structure with the ferroelectric polymer film between two Ti metal electrodes. Figure 6.5

shows the polarization hysteresis (P-E) characteristics of a Ti-P(VDF+TrFE)-Ti-Si, MFEM structure using a 120 nm thick PVDF copolymer film.

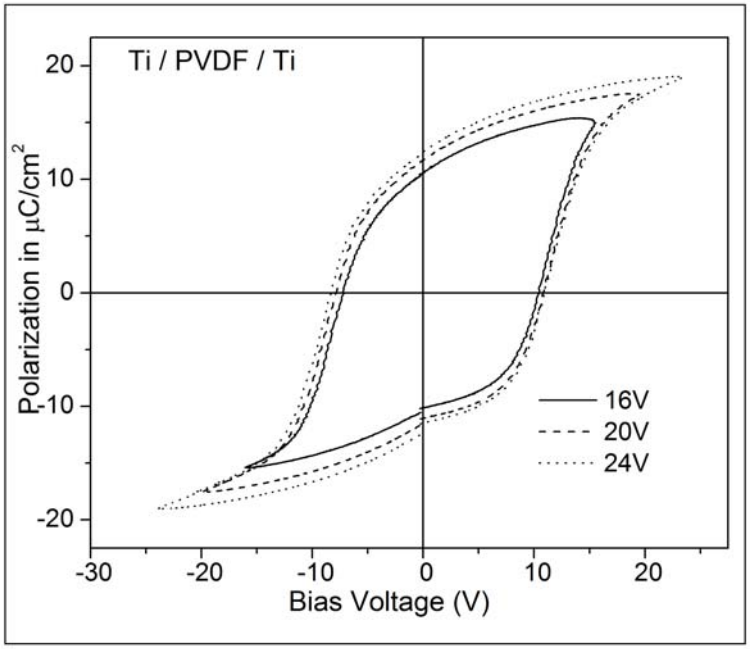


Figure 6.5 P-E hysteresis curves of ferroelectric PVDF copolymer film in MFEM structure showing dipole switching and saturation polarization.

Repetitively applying small voltage pulses and switching between positive and negative gate voltages; and step by step enhancement of this applied voltage while observing the device behavior would sweep the free ionic charges towards the interfaces which increases the switchability of the dipoles and hence increases the remanant polarization P_r. Total switchable polarization and coercive voltage increase during this training process and tend to saturate when a majority of the dipoles are free for spontaneous switching. This was observed at measurements above 20V corresponding to a field of ~1600kV/cm Saturation coercive voltage recorded was ~10V and total switchable polarization $2P_r$ is also found to record a maximum of 24.8μC/cm^2.

PE characteristics of the MFeS structure with PVDF on n-type Si substrate are shown in Figure 6.6. Due to the presence of Si between the film and one of the

electrodes, only a part of the applied field acts on the PVDF film for dipole switching. It was observed to be relatively difficult to attain clear saturation polarization behavior in these devices and that $2P_r$ increases relatively slowly with step increase in peak gate bias. It should be noted that the PE loops are not symmetrical about the axes. The values of $+P_r$ and $-P_r$ and $+V_C$ and $-V_C$ were unequal between the voltage range of 4V to 16V. Ideally PE hysteresis is supposed to exhibit a positive value for $+V_C$ and negative value for $-V_C$ which is demonstrated by the MFeM device. But the MFeS devices under study happened to record both values positive under certain operating conditions. It should be noted that this region corresponds to the region of non-linear current conduction through the film as observed from Figure 6.3. This is a result of charge injection from Si into PVDF at the Si/PVDF interface. [22, 23] The detailed analysis of this asymmetry due to charge injection is presented in the section on charge injection in section 7.4

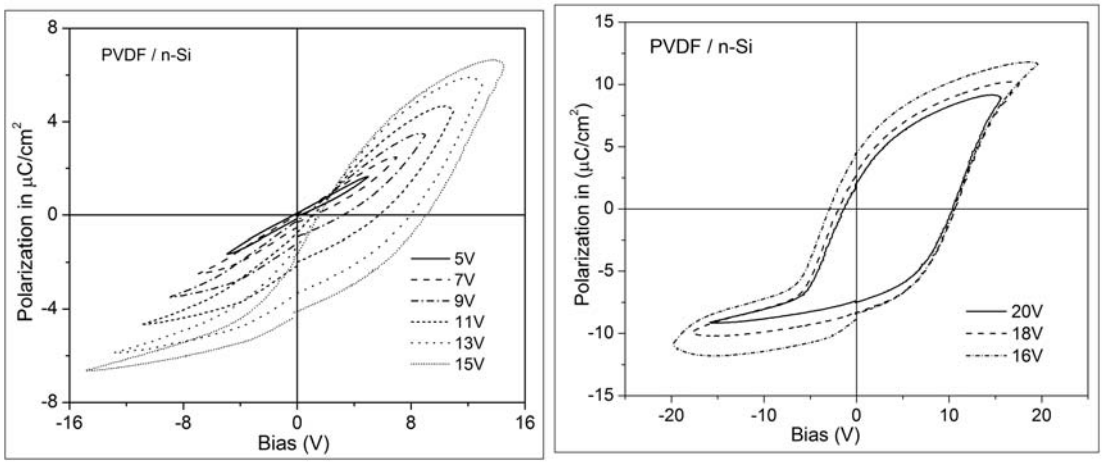
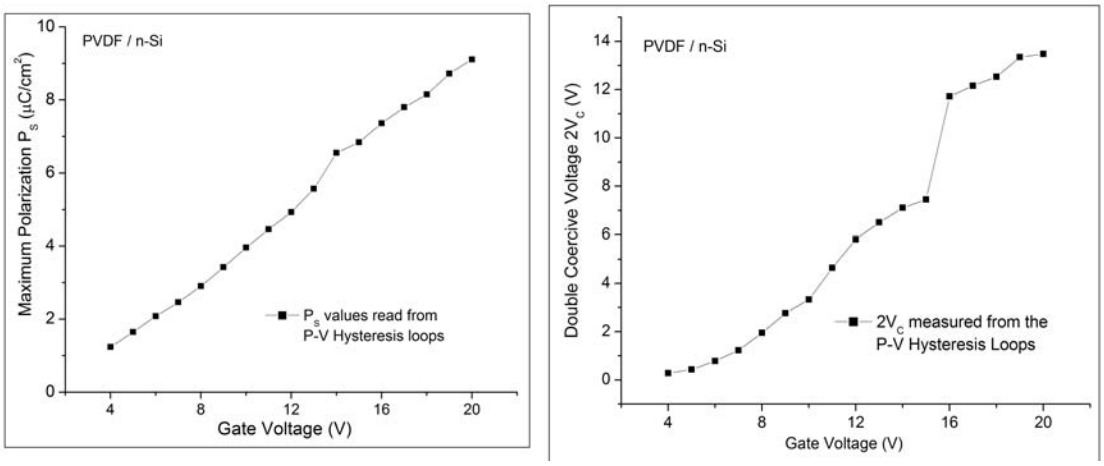


Figure 6.6 P-E hysteresis curves of ferroelectric PVDF film in MFS structure on n-type low resistivity Si at low and high voltage ranges.

Repetitive recordings over the same device revealed a sudden change of properties beyond 16V. The PE loops recorded beyond 16V were identical to those of the MFeM devices. This is explained based on charge trapping at very high voltages which

restores the ferroelectric behavior of the polarization domains. However under such circumstances, saturated hysteresis was observed only at voltages over 16V and the remanant polarization $2P_r$ recorded saturates at ~13.3V. The coercive voltage which was initially found to increase with voltage is also observed to saturate at a value of 10.5V. When the device was driven from accumulation to depletion and inversion, the depletion layer established dramatically reduces the field acting on the dipoles for switching. At very high voltages, this reduction in the field and heavy charge injection results in partial polarization compensation. Hence the switching is not sharp but rather gradual in the negative voltages resulting in loop rounding as seen in the figure at very high voltages.

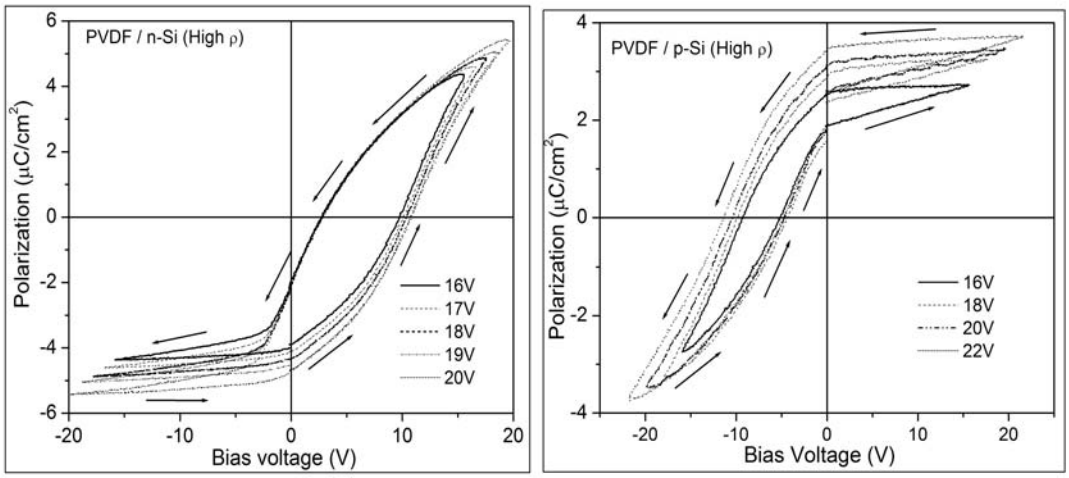


(a) Plot of P_S vs. V_G (b) Plot of ΔV_C vs. V_G

Figure 6.7 Maximum Polarization and Double coercive voltage read from P-V hysteresis curves, plotted against Gate voltage

The Figures 6.7 (a) and (b) demonstrate the increase in the values of maximum polarization (P_S) and double coercive voltage ($2V_C$= ($+V_C$)-($-V_C$)). It can be seen that the value of 2VC increases rather quickly at the lower voltages, and slowly attains a saturation value at higher voltages.

PE hysteresis was also studied on samples with very high substrate resistivity ~5-15 Ω-cm. Figure 6.8 (a) and (b) show the PE hysteresis recorded on devices with PVDF copolymer film deposited on high resistivity n and p-type Si substrates respectively.



(a) High Resistivity n-Type substrate (b) High Resistivity p-Type substrate

Figure 6.8 PE Hysteresis recordings on MFeS devices employing high resistivity substrates indicating the absence of the loops under depletion conditions.

The loops were found to be completely suppressed at voltages corresponding to deep inversion of the substrate. This is due to the very high thickness of the depletion layer formed. This is detailed in Section 7.3. The devices still exhibited a noticeable double coercive voltage and total switchable polarization values of 8.05V and 5.38μC/cm^2 in the n-type device and 16.52V and 3.638μC/cm^2 in the p-type device, respectively, necessary for ferroelectric action. High resistivity accounts for higher charge layer widths and hence greater voltage drop across Si which restrains the switchability of the dipoles.

6.2.2 Polarization Effects on MOS Capacitance.

The oriented dipoles in PVDF can influence the MOS capacitance and hence the C-V curves measured on the devices. Experiments were conducted by recording the C-V curves on the devices under different poling conditions. Poling is a slow process of orienting the molecular dipoles in PVDF film under the influence of applied external dc field. The dipoles in the film were released by a series of positive and negative voltage sweeps and slow increase in the voltage of sweep. C-V measurements were initially recorded in the pristine conditions where the device is not subjected to any poling voltages and when the dipoles are assumed to have a random distribution. The devices were then subjected to prolonged DC voltages beyond their coercive voltages to align them in the direction of the applied dc field. C-V measurements taken on the devices so poled were found to be shifted relative to the pristine measurements. Measurements were always taken with a voltage sweep from inversion to accumulation, which means negative to positive voltages for the devices with n-type Si substrate under study. These observations can be noticed in Fig. 6.9 and Fig. 6.10. The poling voltages and magnitude of voltage sweep used for C-V measurements is chosen to be within the tolerable voltage range of the film which can be estimated from the PE measurements.

The device in Figure 6.9 is subjected to positive DC voltages of 4V and 6V at the gate for 200 sec, and the C-V measurements were taken for a sweep from -8V to +8V. The C-V curves are clearly shifted negatively. These are quantitatively identified by the shift in flat band voltages of -0.64V and -1.69V relative to the flat band voltage under pristine measurement conditions. The onset of inversion for pristine condition is analyzed

at ~-5.5V and the same for measurements after poling with DC 4V and 6V are observed to give flat band voltages as -6.8V and 7.7V respectively.

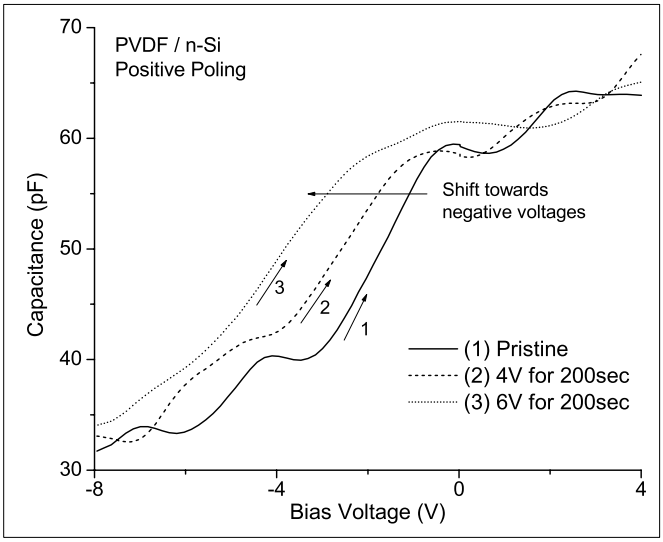


Figure 6.9 C-V curves recorded with a voltage sweep of -8V to 8V on MFeS devices after poling with Positive voltages of 4V and 6V demonstrating a shift towards negative voltages.

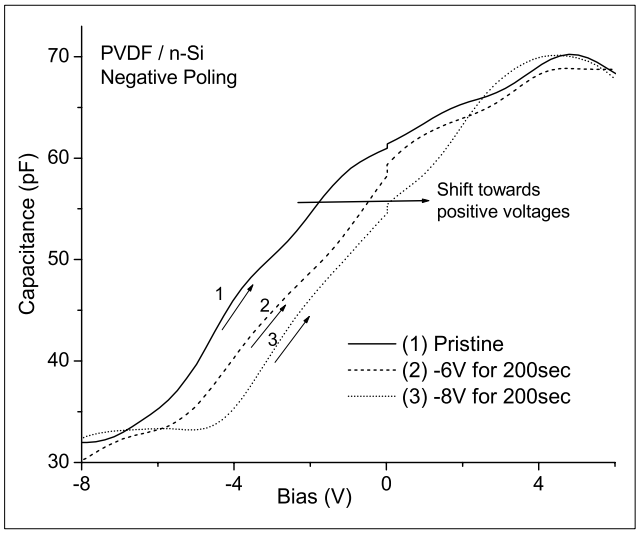


Figure 6.10 C-V curves recorded with a voltage sweep of -10V to 10V on MFeS devices after poling with Negative voltages of -6V and -8V demonstrating a shift towards positive voltages.

The device in Figure 6.10 shows the recordings taken after DC poling with negative voltages of -6V and -8V for 200 sec. The voltage at the gate is swept from -10V

to 10V for each measurement. The shifts in flat band voltage recorded relative to the pristine measurement are 1.04V and 2.04V respectively for -6V and -8V poling voltages. The threshold voltage which marks the deep inversion is observed at -6.55V for the pristine measurement and -5.37 and -4.05V with measurements after -6V and -8V poling respectively.

This noticeable shift of -2.2V under positive poling and +2.5V under negative poling relative to the pristine measurements would be due to the coercive field contribution from the dipoles.

C-V measurements for poling were measured at voltages in the range of 8V to 12V due to the observation of rounding and asymmetry of PE loops recorded at higher voltages. At very high voltages, the possible charge injection could alter the effects of poling these devices. This range of operation of the devices is chosen to keep the charge injection levels low.

6.3 Memory action

6.3.1 Hysteresis in C-V

Polarization influence on the C-V curves was also observed with the direction of the sweep of measurements, which validates that the shifts are predominantly due to the influence of dipoles and not free charges. When the device is traced from inversion to accumulation and then back to inversion, the C-V curves recorded in both directions are found to be shifted, exhibiting hysteresis. This proves for bistable operation of the device, since the onward path is well separated from the return path. This observation can be

noticed in Figure 6.11, which shows the C-V recordings on an MFeS device with n-type substrate, when the voltage on the device is traced from -15V to 15V and then back to -15V.

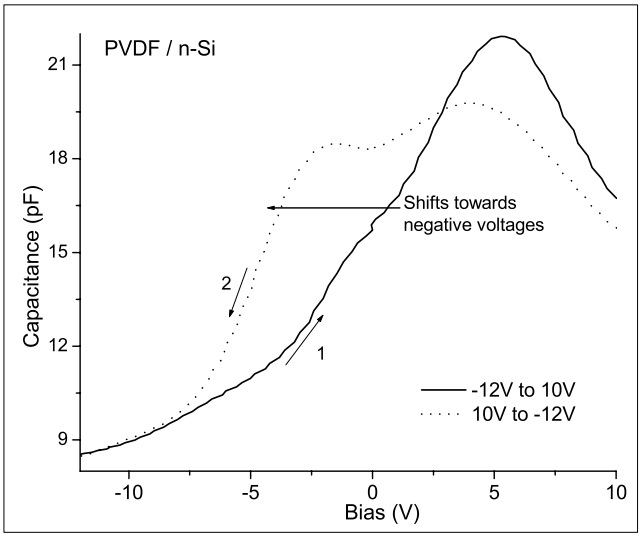


Figure 6.11 C-V Hysteresis recorded on MFeS devices with low resistivity n-Si substrate

The voltage sweep in the negative direction shifted the curves towards negative voltages. This shift can be quantified by the difference in flat band voltage measured in each direction. This is known as the memory window $MW=\Delta V_{FB}=V_{FB+}-V_{FB-}$,[15] where V_{FB+} is the flat band voltage measured when the voltage is swept in the positive direction and V_{FB-} is the flat band voltage calculated when the voltage is swept in the negative direction. A clear shift of 4.8V is recorded which indicates a significant memory window for bistable memory operations. It is noted that the C-V hysteresis is observed at voltages as low as 10V in case of MFeS devices. The highest capacitance of about ~22 pF is recorded for the positive voltages and the lowest capacitance of about 7pF is observed when the device is in deep inversion.

Identical recordings were also taken on devices with p-type substrate. Figure 6.12 shows the C-V hysteresis recording on an MFeS device with p-type substrate for voltage sweeps from 20V to -20V and 20V to -20V. A very similar shift of the magnitude ~4.2V towards positive voltages is noticed in these recordings. When the device is traced from accumulation to inversion, the remanant polarization of the dipoles oriented towards the gate provide a retarding field to the external voltage of measurements. Hence the same capacitances are recorded at higher voltages in the reverse sweep.

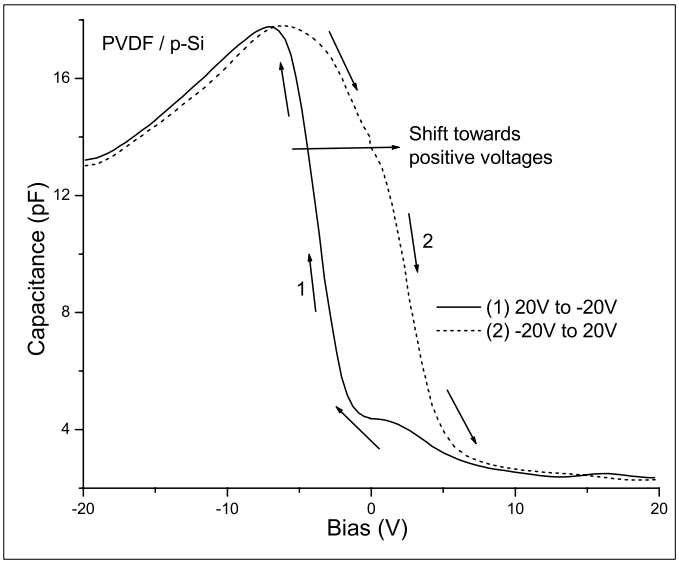


Figure 6.12 C-V Hysteresis recorded on MFeS devices with a p-type Si substrate indicating a shift towards positive voltages in the reverse sweep from accumulation to inversion.

6.4 Presence of a Buffer Oxide

Devices for ferroelectric memories were studied in MFeOS structure in the past with a layer of SiO_2 in conjunction with the film. [24, 25]But the prior studies were done on devices with a very high thickness of Fe film (4500 nm) and very thick (80nm) oxide. Comparative experiments were performed to study the same but with a lower thickness of

oxide (15 nm) and film (120 nm) in the current studies in an effort to pull down the operating voltage of these devices.

6.4.1 P-E Hysteresis

The Polarization – Voltage (P-V) curves for the MFeOS device with a very thin (150A) SiO_2 buffer layer are shown in Figure 6.13.

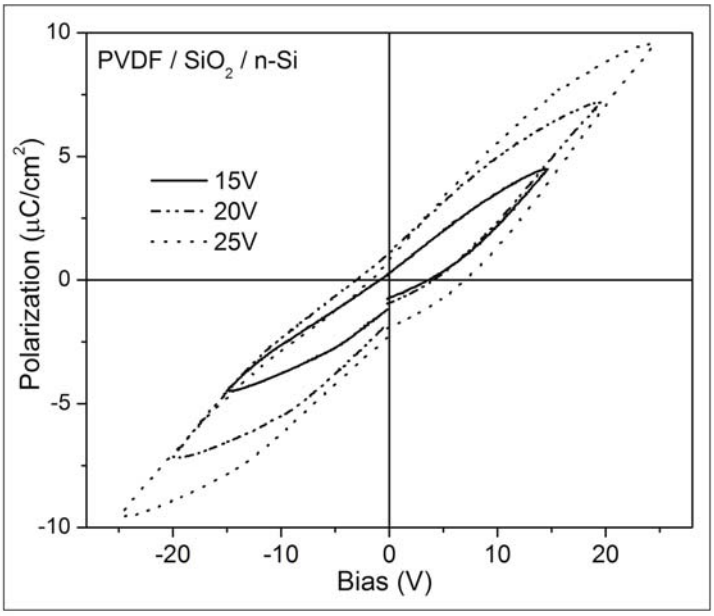


Figure 6.13 P-E hysteresis of devices with MFeOS structure indicating higher voltage of operation and relatively symmetric PE loops with positive $+V_C$ and negative $-V_C$ values.

These curves also demonstrated unequal values for $+P_r$ and $-P_r$ and $+V_C$ being much higher in magnitude than $-V_C$. Again here, the inversion charge layer formed during the negative voltage measurements would prevent the switching of the dipoles. Hence in the sweep from negative to positive voltages, a higher voltage is required to perform dipole switching. This results in a $+V_C$ value much higher in magnitude than $-V_C$. However, the device did record a positive value for $+V_C$ and negative value for $-V_C$. Complete saturation of the hysteresis loops was not observed even at very high voltages,

but the coercive voltages increased rather slowly beyond 25V with a value recorded around 6.5V. Highest recorded switchable polarization ($2P_r$) value was ~5.18 $\mu C/cm^2$, which is significantly lower than the value for the MFeS device which is attributed to the field sharing by the oxide layer in these devices. Loops with a noticeable double coercive voltage (2Vc) and saturation polarization could only be recorded at measurement voltages above 20V.

6.4.2 C-V Hysteresis

It would be necessary to note the C-V behavior of a pure MOS sample with identical oxide thickness before studying the behavior of the ferroelectric film stacked on the buffer oxide in MFeOS structure. The C-V behavior of regular MOS structure with a thermally grown oxide layer of identical 150A^o thickness was recorded at 500 KHz and it is shown in Figure 6.14.

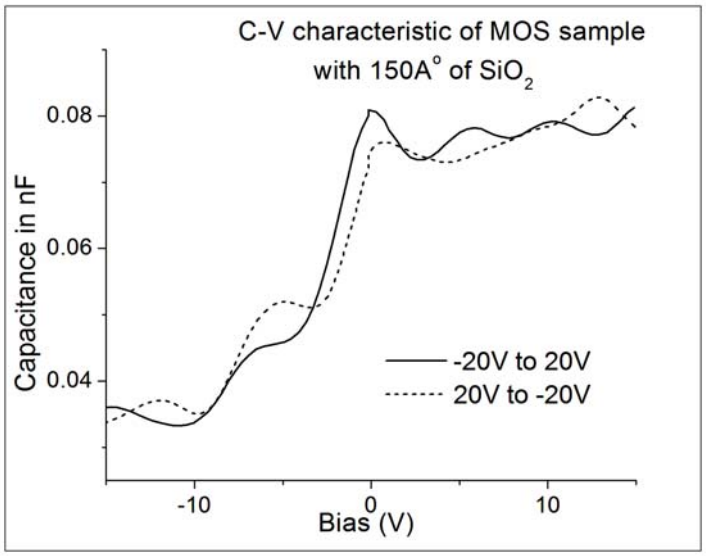


Figure 6.14 C-V recordings of MOS device with 150A^o of SiO_2 on n-Si

The C-V characteristics measured on an MFeOS device are shown in Figure 6.15 The presence of ferroelectric material on SiO_2 still exhibits a notable memory window in

the C-V hysteresis. A low thickness oxide is employed in our study in an effort to pull down the operating voltage of devices, and the devices are still found to exhibit a noteworthy shift of -8.2V in the flat band voltage. Thus the fixed oxide charges in SiO_2 are of positive polarity whose concentration is calculated by the equation $Q_i = -C_{acc}.\Delta V_{fb} /qA \sim 7 \times 10^{11} cm^{-2}$. The two peaks observed in each of the C-V traces could be explained as corresponding to the peaks observed in the C-V characteristic of the MFeM sample due to the non-linear dielectric C-V curve of PVDF noticed in Figure 6.1.

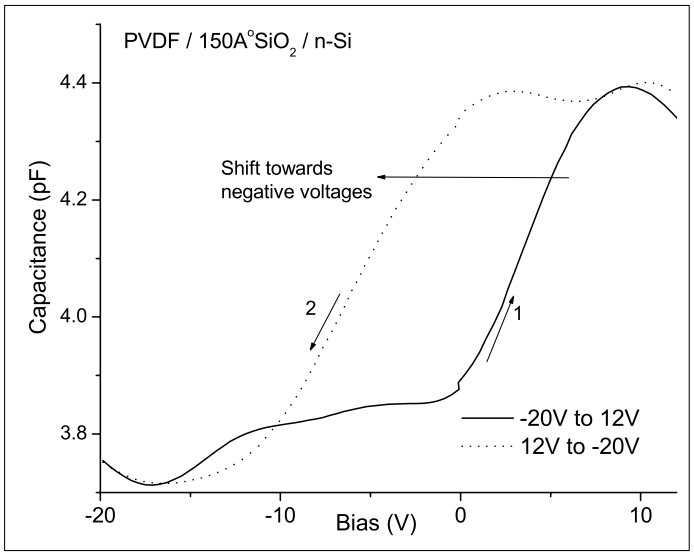


Figure 6.15 C-V Hysteresis recorded on MFeOS device with 150A° of SiO_2 between PVDF and n-Si substrate

PE and C-V Hysteresis were observed only at voltages beyond 20V in these devices. The asymmetry and loop rounding in PE measurements is reduced due to the suppression of charge injection by the buffer oxide layer. But MFeS devices were observed to exhibit a clear memory window even at very low voltages, which proves that inclusion of oxide in the device would just increase the gate voltage V_G for device operation.

At positive gate voltages, since the charge layer in the Si surface is in accumulation, the maximum capacitance corresponds to the stacked capacitance of the bilayer dielectric composed of the 15nm thick SiO_2 layer and the 120nm thick PVDF-TrFE copolymer film. At negative voltages, the minimum capacitance corresponds to the stacked capacitance of the depletion charge layer, oxide and the FE film. The ratio of these two capacitances is given by

$$\frac{C_{\max}}{C_{\min}} = \left[1 + \left(\frac{\varepsilon_{eff}}{\varepsilon_{si}} \right) \left(\frac{4\varepsilon_{si} kT \ln(N_d / ni)}{q^2 N_d} \right)^{1/2} \right]$$

where N_d, n_i and ε_{si} are donor concentration, intrinsic concentration, and dielectric constant of Si respectively, and ε_{eff} is the effective dielectric constant given by

$$\varepsilon_{eff} = \frac{\varepsilon \ \varepsilon_{FE} \left(t_i + t_{FE} \right)}{\varepsilon_i t_{FE} + \varepsilon_{FE} t_i}$$

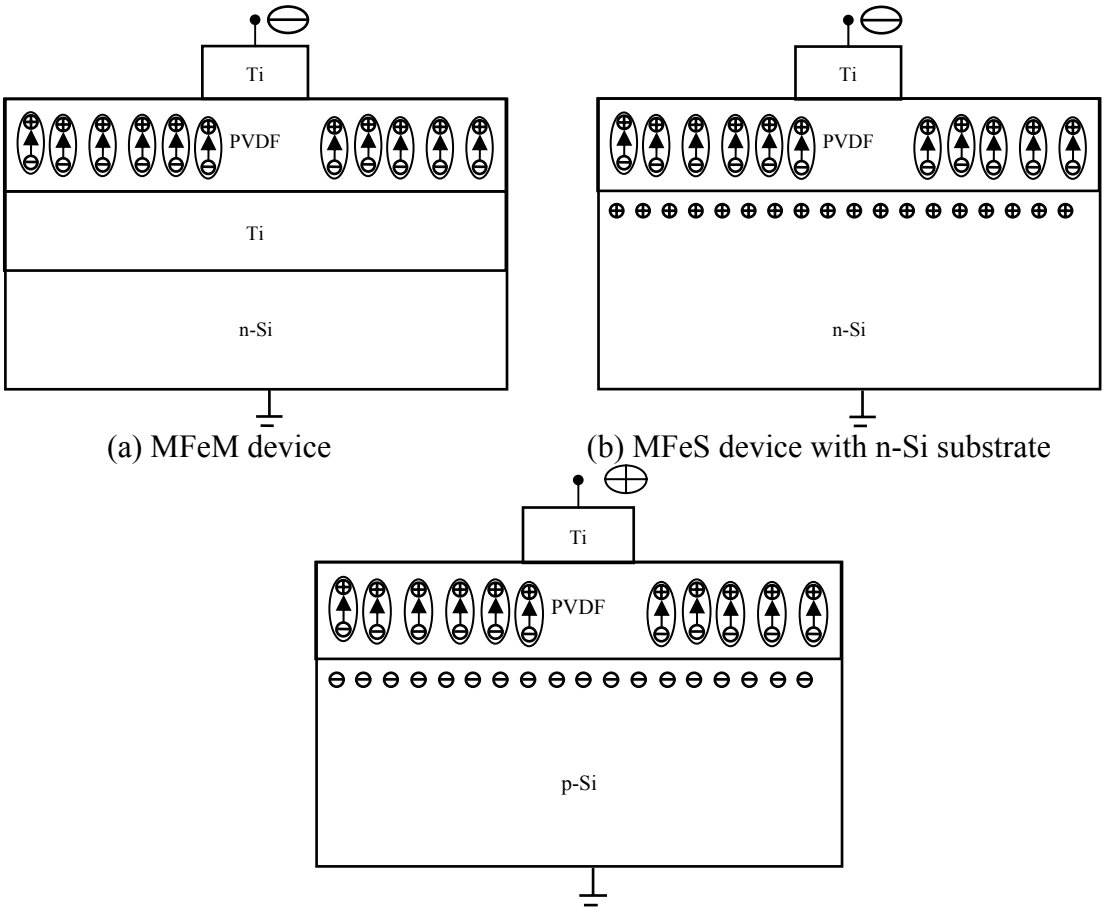
where ε stands for dielectric constant and t stands for thickness, and subscripts FE and i stand for the ferroelectric film layer and the SiO_2 oxide layer respectively. [26]

CHAPTER 7

DISCUSSION

7.1 Analysis of PE curves

A detailed observation of the PE curves in MFeS devices reveals a quenching of the PE hysteresis curve in the negative half cycle, more so clearly seen in the sweep from positive to negative voltages. This quenching of PE loops is not observed in MFeM devices. This can be explained by the formation of the inversion charge layer at the Si surface in the MFeS devices. This is demonstrated by the Figures 7.1 (a), (b) and (c).



(a) MFeM device

(b) MFeS device with n-Si substrate

(c) MFeS device with p-Si substrate

Figure 7.1 Demonstration of the effect of Si surface inversion charge layer on the Polarization characteristics of the devices.

When the voltage at the gate is negative, the Si surface is set to inversion and the minority carrier holes at the Si surface, in close proximity with the dipoles, swtich the dipoles even before the applied external field is reduced below the negative coercive field. Hence the polarization changes its direction sooner for the negative voltages, resulting in a very low $-V_C$ value. The presence of this inversion charge also results in neutralization of the dipole field. Hence a lower value of $|+P_r|$ is recorded. In the sweep from negative voltages to positive voltages at the gate, this depletion charge layer reduces the field acting across the film, and hence higher voltages are required to switch the polarization resulting in a greater value for $+V_C$ and $|-P_r|$.

In devices with high –resistivity Si substrate (5-15 Ω-cm) in Figure 6.8 (a), the absence of a loop at the negative voltages is due to the high thickness of the depletion layer formed. High resistivity accounts for high thickness of the depletion layer (W), and hence low inversion capacitance. This reduces the field acting across the PVDF film. This is explained in Section 7.3 on voltage sharing between PVDF and Si under inversion conditions.

Identically in the MFeS devices with p-type substrate, the loop is absent in the positive half cycle as can be noticed from figure 6.8 (b), due to the high resistivity (ρ) of the Si substrate (5-15 Ω-cm) employed for the studies. Quenching of the loop occurs in these devices in the positive voltages. This is due to the polarization compensation by the inversion charge layer during the sweep from negative voltages to positive voltages. For a p-type substrate, when the voltage at the gate is positive, the p-Si surface near the PVDF film is in inversion. The inversion charge layer here is comprised of electrons which tend to neutralize the dipole field which is oriented towards the substrate. Hence in

this case when the voltage at the gate is swept from positive bias towards negative bias, this quenching is absent at V_C. This behavior is explained in Figure 7.1 (c).

7.2 Interplay of dipoles and surface charges during poling

When the device is poled to different DC voltages, the dipoles are oriented creating an internal field which aids or retards the applied external field during C-V measurements. Since switching of dipoles is only possible at voltages beyond the coercive voltage of the film, the poling voltage is chosen according to the coercive voltage read from the PE measurements. The initial pristine measurements are taken when the dipoles are just released from the binding ionic charges and are free for switching. The dipoles have random alignment and create no internal field Figure 7.2.

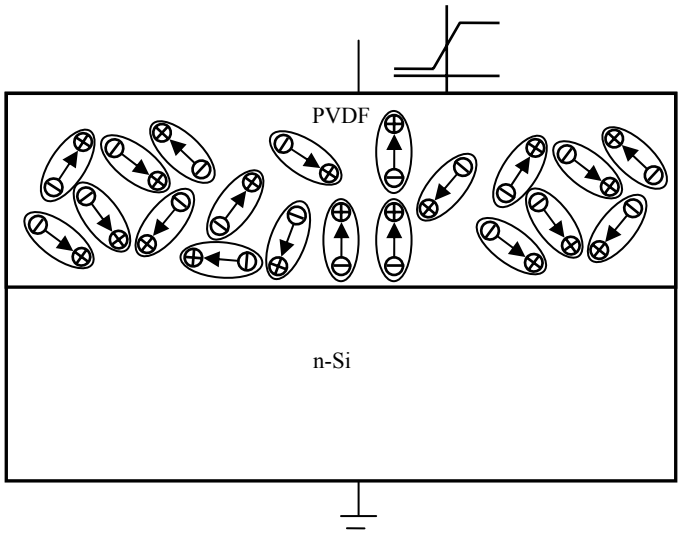
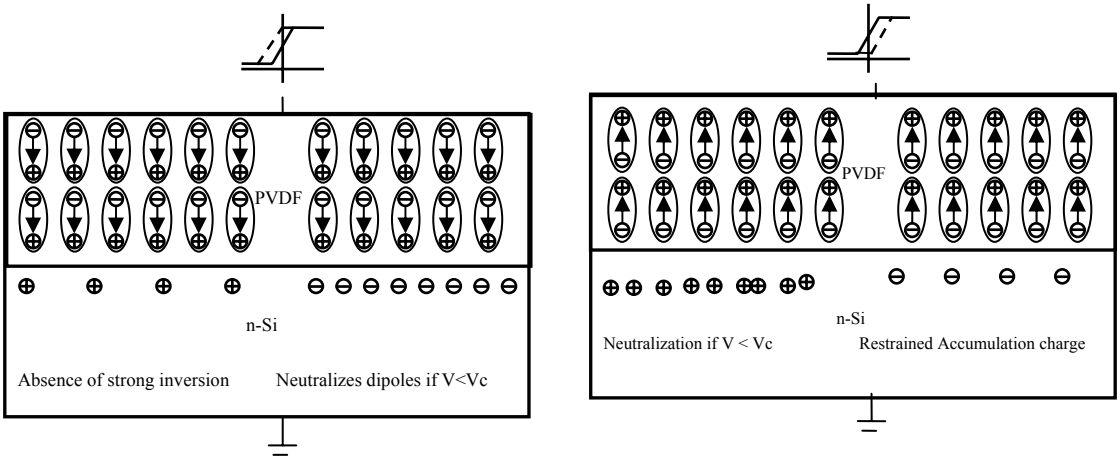


Figure 7.2 Demonstration of Pristine condition for measurement of C-V before studying poling effects.

The device is then subjected to a DC voltage of +4V and +6V at the gate for 200 s. This results in a slow orientation of the dipoles towards the Si surface, creating in a net internal field towards the Si surface which aids the external field for C-V measurements.

Hence the same capacitances are recorded at earlier voltages, resulting in the shift of C-V curves towards negative voltages as in Figure 7.3 (a) and its inset. When the device is poled with DC voltages of -6V and -8V at the gate, the dipoles are oriented away from the surface. This results in a retarding field for the applied external sweep voltage. This implies that higher voltages are required for recording the same capacitance values as the pristine curve, resulting in a shift of C-V curves towards positive voltages.



(a) Positive Poling (b) Negative Poling

Figure 7.3 Illustration of Poling effects on C-V.

A detailed observation of the shifted curves in Figure 6.10 reveals that the C-V curves are parallel shifted in the measurements with negative poling. But the curves seem to converge in the positive half cycle in measurements after positive poling in Figure 6.9. Also a clear inversion is not seen in the C-V curves measured with positive poling conditions. This will be explained below. Under positive poling conditions, the dipoles and their field are oriented towards the Si surface; hence the presence of the positive charges of the dipoles near the Si surface prevents the inversion charges to accumulate at the Si surface. Hence a clear inversion is not observed in these curves. However the orientation of the dipoles still aids the external bias for C-V measurements. Hence the

curves are shifted towards negative voltages. But, as the voltage at the gate is slowly traced towards positive voltages, the Si surface is slowly driven to accumulation. The accumulation charges, which are the majority carrier electrons compensate a part of the dipolar charges resulting in a reduction of that contributing field. Hence, a near pristine C-V behavior is observed for the positive voltages which results in conversion of the curves towards the pristine curve.

Similarly in the C-V curves taken during negative poling (Figure 6.10), it is observed that the onset of accumulation is not sharp but rather gradual. When the PVDF film is poled to a negative voltage, the dipoles orient themselves away from the Si substrate. Hence the negative charges of the dipoles in close proximity with the Si surface tend to prevent the accumulation of electrons. Hence the accumulation is rather gradual than abrupt in these curves.

The shift can be quantitatively measured by noting the magnitude of the shift in the flat band voltage and the threshold voltage. The shifts in the threshold voltage V_{TH} are 1.39V and 2.26V respectively which are much higher than the shifts in the flat band voltage V_{FB} which are 0.64V and 1.69V. These shifts in the threshold voltage are in accordance with the V_C values of 1.6V and 2.9V read from the PE curves before taking the C-V measurements.

7.3 C-V Voltage Sharing

As demonstrated, the C-V curves of PVDF-TrFe film when deposited directly on Si shows clear MOS action. A general expression for the stacked capacitance of the device is given by [2]

$$\frac{1}{C_{Stack}} = \frac{1}{C_{Si}} + \frac{t_{Fe}}{\varepsilon_{Fe}}$$

where t_{Fe} and ε_{Fe} are the thickness and the dielectric constant of the ferroelectric layer, C_{si} is the capacitance of the surface layer on Si whose properties depend on the region of operation and the magnitude of the gate voltage.

In the device with n-type substrate, the highest capacitance ~21 pF is recorded at positive voltages when the majority carrier electrons accumulate at the PVDF-Si junction forming a conducting layer. C_{Si} has a higher value in the accumulation mode when the thickness W_A of the layer of accumulation charge is negligible compared to the thickness of the PVDF film. Using the value of C_{Stack} from the Fig. 2, and ignoring the term $1/C_{Si}$ in the above equation under accumulation conditions, the dielectric constant of PVDF is calculated to be ~10.31 which is in agreement with the commonly assumed value for the PVDF polymer film.

It was explained in section 6.2.1 that the absence of the loop under depletion and inversion conditions in the high resistivity samples is due to the high thickness of the depletion layer width formed. An expression can be computed and simulated to study the division of voltage between the PVDF film and the charge layer on the Si surface. For the devices made on well cleaned Si substrate, ideally the total voltage applied at the gate of the device is shared between the PVDF copolymer film and the charge layer at the surface of Si.

$$V_G = V_{Si} + V_{Fe}$$

Where V_G is the applied external gate voltage, V_{Si} is the voltage drop across the charge layer in Si at the PVDF – Si interface, and V_{Fe} is the voltage drop across the ferroelectric film. An expression for calculating the effective voltage acting across the ferroelectric layer has been determined as. [23]

$$V_{Fe} = \left(\frac{\varepsilon_{Si} t_{Fe}}{\varepsilon_{Si} t_{Fe} + \varepsilon_{Fe} W_d} \right) V_G$$

where the ε and t stand for the dielectric constant and thickness respectively, and the subscripts 'Fe', 'Si' and 'd' stand for the ferroelectric layer, charge layer in Si . The depletion layer width, W_D for a Si substrate assuming an abrupt junction and thermal equilibrium is about $8L_D$, where L_D is the debye length, a characteristic of semiconductors given by, [27]

$$L_D = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_D}}$$

which is calculated to be 1.29 nm, giving W_d as 10.37 nm for n-type Si with low resistivity. Employing a higher resistivity substrate would effect the width of the depletion layer and hence the depletion capacitance. The samples employed for studies with higher resistivity were n-Si with resistivity σ about 10 Ω-cm and p-Si with σ about 15 Ω-cm. The doping densities N_D and N_A corresponding to these resistivities are 10^{15} cm^{-3} and 5 $x10^{14}$ cm^{-3}. [28]This would yield a value for W_D of about 180 nm and 300 nm, which are significantly higher than the thickness of the FE film employed. Hence the voltage drop across the depletion layer is also very high. Figure 7.4 shows the variation of the voltage acting across the ferroelectric film as a fraction of applied voltage with varying substrate resistivity / doping concentration. The doping concentrations

corresponding to the high resistivity n and p-type samples employed in the studies fall in the range of 10^{14} to 10^{15} where just about 0.1% of the applied gate voltage acts on the film to provide for polarization switching. [4,5]

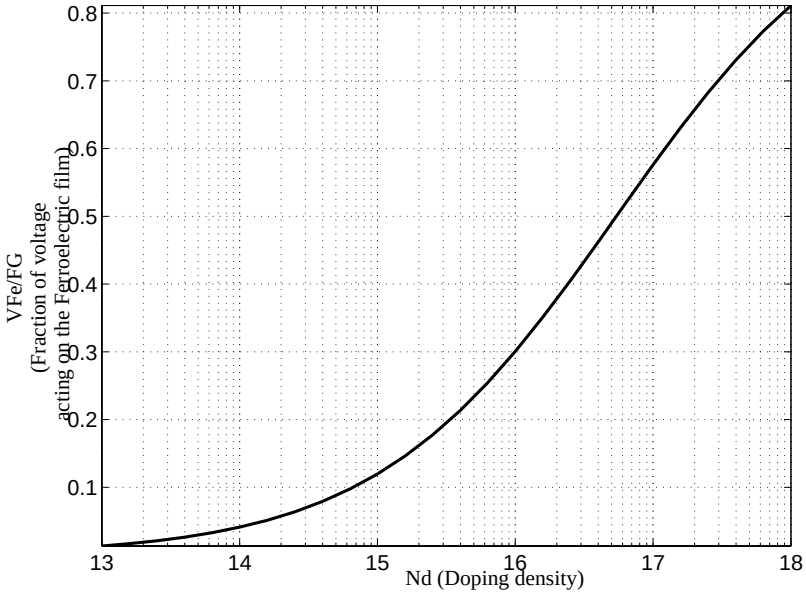


Figure 7.4 Simulation of the Fraction of the gate voltage acting across the PVDF film as a function of Doping density.

7.4 Charge injection

The experiments on P-E and C-V measurements in the MFeS devices demonstrated clear charge injection effects at voltages over 8V. The events of charge injection are illustrated in Figure 7.5 (a) and (b).

A detailed observation of the I-V characteristics in Figure 6.3 reveals that the leakage current non-linearly increases due to charge injection between 4V to 16V. Under the same conditions it can also be observed from the PE Hysteresis loops of Figure 6.6 (a) that the value of –Vc also increases. When the voltage at the gate is above 4V, the voltage at the Si substrate being negative, the absence of a buffer oxide would trigger electron injection into the FE film. [7, 29, 30, 31] The electrons so injected at the PVDF-Si

interface move through the ferroelectric domains in thePVDF. This accumulation of the injected charges is likely to increase with the increase in the positive field at the gate which is shown in Fig. 7.5 (a)

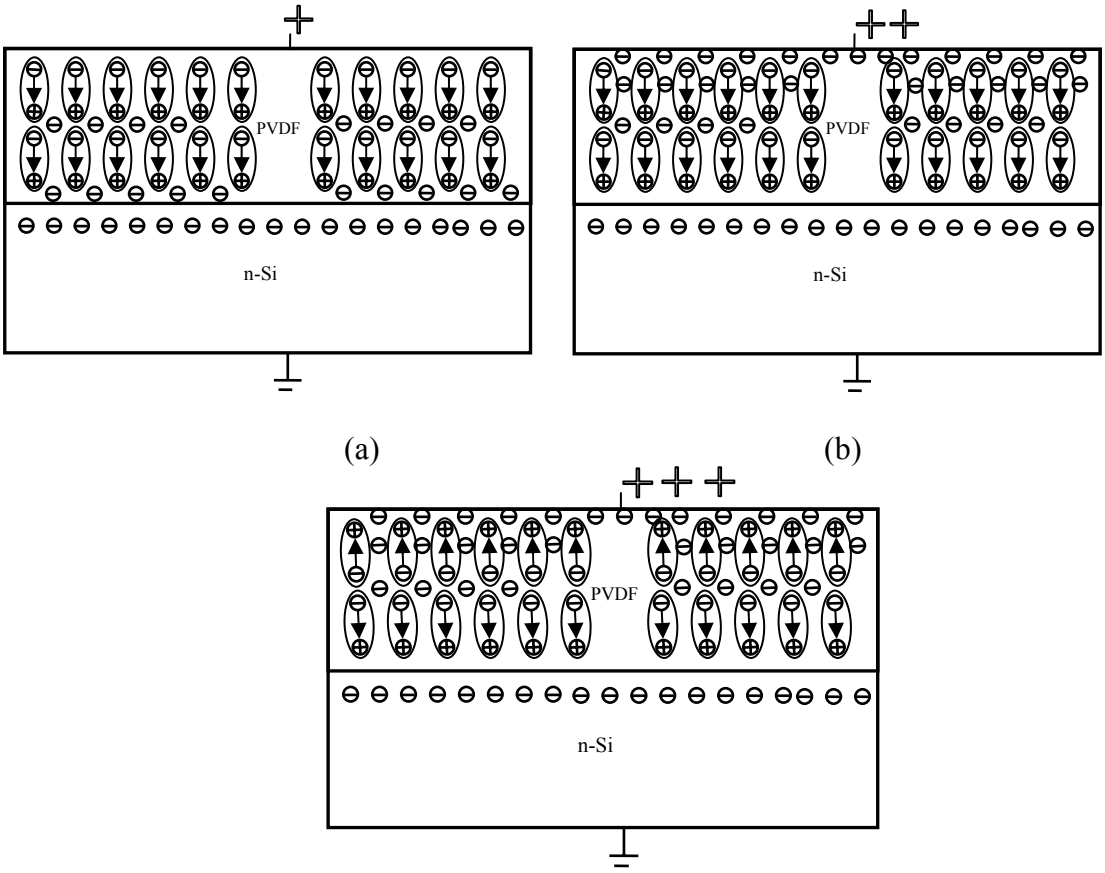


Figure 7.5 Illustration of Charge Injection from Si into PVDF film
(a) Injected charges move freely through the polarization domains
(b) Injected Charges move towards the Gate at very High voltages.
(c) Polarization switching under the influence of injected charges.

The charge injection increases and the injected charges move freely through the polarization domains and accumulate at the gate due to the positive voltage at the gate. During the sweep from positive to negative voltages, these negative charges aid the early switching of dipoles. Hence the value of $|-V_C|$ is observed to increase with the increasing measurement voltages. This accumulation of injected electrons at the gate is shown in Figure 7.5 (b).

At further higher voltages (>8V), the charge injection increases so as to completely compensate the dipolar field and also switch the domains even before the applied field is reduced below zero. Hence $-V_C$ records positive values between 8V to 16V. These changes in $-V_C$ can be noted from Figure 7.6. The increasing value of $|-V_C|$ between 4V to 8V and zero crossing at 8V when $-V_C$ turns positive can be noted in the same figure.

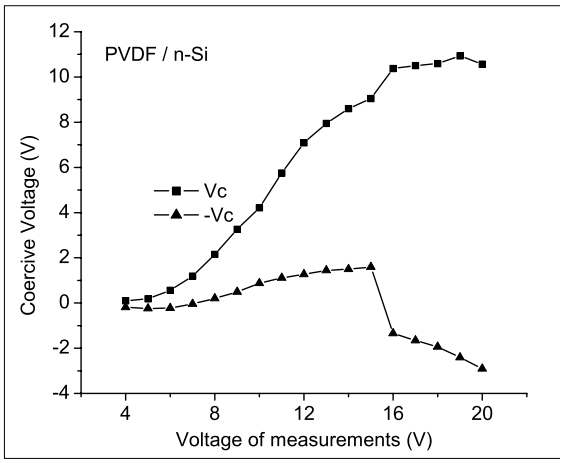
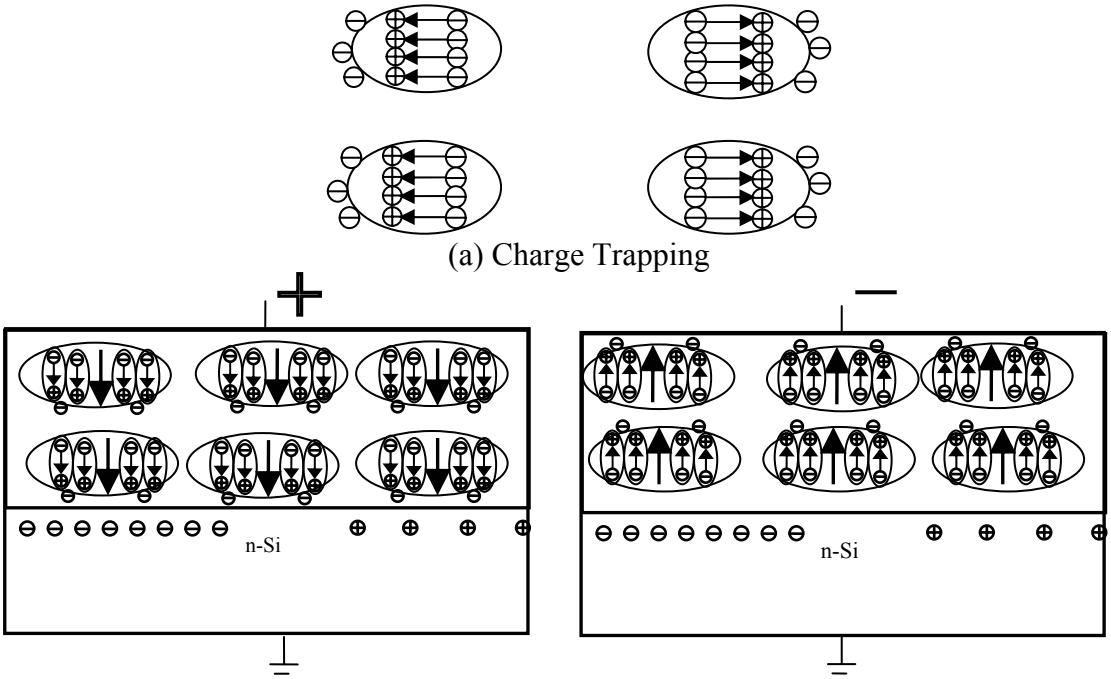


Figure 7.6 Changes in the values of $+V_C$ due to charge injection and charge trapping.

Repetitive experiments performed to record the P-E hysteresis under these voltage ranges have consistently demonstrated this behavior, but when the device under study, is subjected to continuous switching from negative to positive, and positive to negative voltages in this region, the charge injection changes its behavior. The injected charges are most likely to get trapped in the domains and get locked-in with the dipoles, which prevent their free movement further between the gate and the Si interface. The trapped electronic charges compensate a part of the dipolar charges, but the domains in the film still have net dipole moment and exhibits spontaneous polarization. Hence hysteresis is

again observed, but with reduced sensitivity [7-9]. This behavior of charge trapping is illustrated in Figure 7.7.



(a) Charge Trapping

(b) Polarization switching with gate voltages

Figure 7.7 Polarization Restoration after charge trapping and domain formation at voltages >16V.

The device under such conditions would exhibit a dramatic change in the PE characteristics. The absence of the injected charge layer results in $-V_C$ recording negative values, and its negative value increases with increasing voltage, which results in relatively symmetric PE curves. This is because the dipoles along with the trapped charges switch with the applied external field and behave like a ferroelectric material again, just like a pure PVDF sample which can be seen in Figure 7.7 (a) and (b). Figure 7.6 depicts the V_C variations before and after charge trapping at voltages before and after 16V. The illustration shows the sudden change in $-V_C$.

Charge injection also shows its effect on the C-V measurements. The memory window measured from the C-V hysteresis plots is found to increase initially up to ~14V

in the MFeS devices under study. However the C-V measurements performed with voltage traces beyond this voltage are found to exhibit a decrease in the memory window. Table 1 and Figure 7.8 shows the different values of ΔV_{FB} measured at different voltage traces.

Table 7.1 Variation in Flat band voltages with Sweep voltage at the gate

Voltage of measurement	8	10	14	20	24
Vfb+	0.22	1.78	2.93	2.13	0.11
Vfb-	-2.007	-3.04	-2.758	-1.42	-1.19
ΔVfb	2.227	4.82	5.688	3.55	1.3

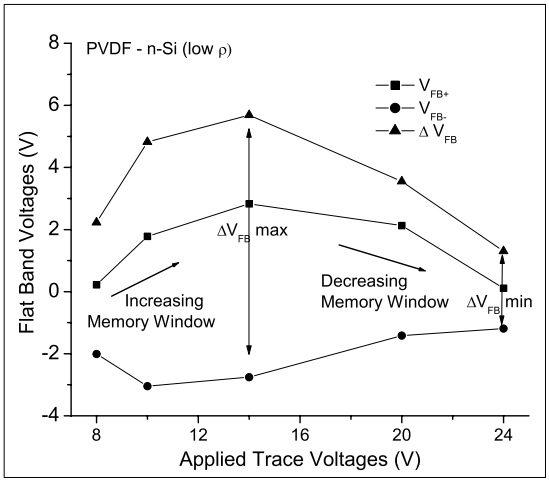
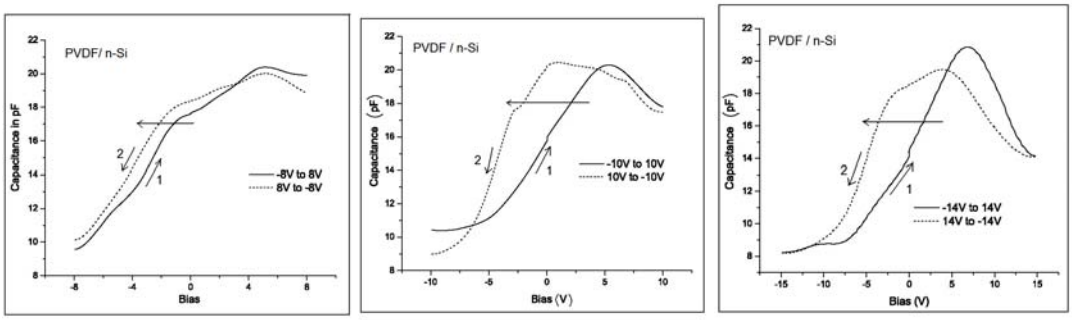


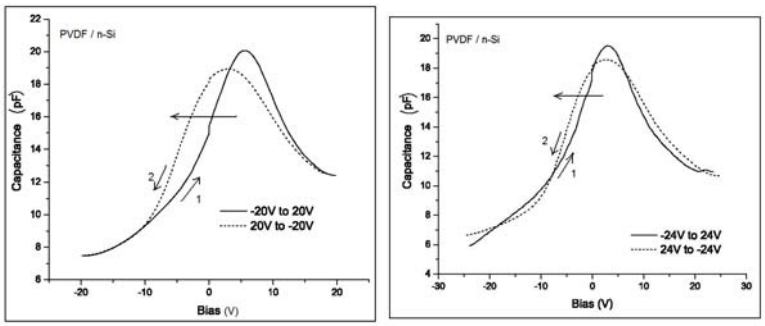
Figure 7.8 Changes of Memory window with Charge injection.

It can be seen that the maximum memory window of 5.688V was recorded when the voltage is swept from -14V to +14V and back to -14V. The C-V hysteresis plots corresponding to these readings are also illustrated in Figure 7.9. In the presence of a very thin oxide in MFeOS devices studied, no noticeable decrease in memory window was noticed even at voltage sweeps as high as 35V. However it is clearly understood that the presence of a buffer oxide does suppress charge injection, but it comes with the price

of higher operating voltage. Under well chosen operating voltages (10V-16V) it is observed that MFeS devices can be operated without significant charge injection effects.



(a) 8V voltage sweep (b) 10V voltage sweep (c) 14V voltage sweep



(d) 20V voltage sweep (e) 24V voltage sweep

Figure 7.9 C-V Hysteresis plots measured on MFeS device with n-Si substrate at different voltage sweeps demonstrating the changes in memory window.

CHAPTER 8

CONCLUSIONS

In summary, we have demonstrated MOS action of PVDF film in stack with Si and it recorded a clear shift in flat band voltage of magnitude ~3.5V to ~ 4.8V under operating voltages as low as 10V to 15V. Its high remanant polarization values and low coercive voltages when deposited directly on Si suggest the possibility of its use without the buffer oxide.

Charge injection into the ferroelectric film is observed in detail by analyzing the conduction process through the junction. The behaviors of P-E and C-V measurements under charge injection have been explained. It was proved that C-V and P-E hysteresis can still be recorded under the required low voltage operation of the devices as opposed to higher voltages studied before. Selected operation of these devices at low voltages can prevent heavy charge injections and exhibit significant bistable behavior necessary for memory applications. Even under higher voltages of operation, charge trapping can be adopted to restore the ferroelectric behavior.

Studies on MFeOS devices with low thickness oxide have proved that presence of oxide can reduce the charge injection and provide a larger memory window in the C-V measurements. But this comes with a price of high voltage of operation and further possibilities of oxide trapped charge. The absence of a buffer layer also improves the data retention time. [18]The elimination of the gate oxide which shares a significant fraction of the applied field could drastically pull down the operating voltages of the devices, from 20V-25V to 8V-15V which is a primary concern for current day low power gadgets.

APPENDIX

PHYSICAL CONSTANTS

Table A1 Useful physical constants.

Description	**Symbol**	**Value and unit**
Electronic charge	q	1.6×10^{-19}C
Boltzmann's Constant	K	1.38×10^{-23} J/K
Vacuum permittivity	ε_o	8.85×10^{-14} F/cm
Silicon permittivity	ε_{si}	1.04×10^{-12} F/cm
Oxide permittivity	ε_{ox}	3.45×10^{-13} F/cm
Planks constant	h	6.63×10^{-34} J-s
Temparature of measurements	T	300K
Thermal voltage	kT/q	0.0259V
Nanometer	nm	10^{-7} cm
Micron (micrometer)	μm	10^{-10}cm
Electron-volt	eV	$1eV = 1.6 \times 10^{-19}$ J
Intrinsic concentration (assumed)	ni	1.45×10^{10} /cm

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