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Integration of HfO₂ on Si/SiC heterojunctions for the gate architecture of SiC power devices

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1, 2, 3, 4, a)

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In this paper we present a method for integrating HfO₂ into the SiC gate architecture, through the use of a thin wafer bonded Si heterojunction layer. Capacitors consisting of HfO₂ on Si, SiC, Si/SiC and SiO₂/SiC have been fabricated and electrically tested. The HfO₂/Si/SiC capacitors minimise leakage, with a breakdown electric field of 3.5 MV/cm through the introduction of a narrow bandgap semiconductor between the two wide bandgap materials. The Si/SiC heterojunction was analysed using transmission electron microscopy, energy dispersive X-ray, and Raman analysis, proving that the interface is free of contaminants and that the Si layer remains unstressed.

The physical and electrical properties of silicon carbide (SiC), including its wide band gap (3.26 eV), high critical electric field (3 MV/cm) and thermal conductivity (3.7 W/cmK), make it an attractive material for high frequency, high power devices. Twenty years of material development has seen many of the processing techniques mature and the quality of the substrates improve significantly, to a point where the substrates supplied today achieve a defect density low enough to fabricate electronic devices. Commercial SiC Schottky barrier diodes and junction gate field-effect transistors¹ are now available though the development of a SiC metal-oxide-semiconductor field-effect transistor (MOSFET) is hindered by the material cost and quality, and due to problems with the SiC-oxide interface that has prevented SiC being used to its full potential.

Often seen as one of the materials key benefits, SiC has a native oxide in silicon dioxide (SiO₂), which can easily be formed through thermal oxidation of the surface. Furthermore, with SiO₂ having a very wide bandgap, the leakage that occurs through a SiC/SiO₂ interface at moderate electric fields is very low. Recent studies^{2,3} suggested that SiC/SiO₂ MOS capacitors are capable of supporting an electric field of 3.9 MV/cm for a lifetime of 100 years at 375 °C. However, with a low dielectric constant of 3.9, Gauss' law ($\nabla \cdot \epsilon \epsilon_0 \vec{E}$) states that the SiO₂ must be capable of withstanding 7 MV/cm to match the potential of SiC. Furthermore, the build up of a SiO_xC_y transition layer at the interface between the two materials causes scattering in the channel, lowering the mobility of this region⁶. Post deposition anneals in nitric oxide (NO) have been shown to shrink this region, increasing the channel mobility three-fold⁷. The threshold-voltage instability effect, which has been observed in both

SiC lateral MOSFET test structures and fully-processed SiC power double diffused MOSFETs, is consistent with direct tunneling into and out of near-interfacial oxide traps^{8,9}.

The use of oxides with large dielectric constants (High-K) have been investigated as an alternative to SiO₂. Popular studies have included Al₂O₃ and HfO₂ deposited onto SiC^{10,11}. Results have shown a reduction in interface trap density compared to SiO₂/SiC interfaces¹⁰, however large leakage currents tend to occur due to the inverse relationship between dielectric constant and band gap¹². The use of a thin SiO₂ interlayer^{13–15} reduced this leakage and achieved a reported¹³ channel mobility of 300 cm²/(Vs). However, the reintroduction of SiO₂ lowers the total dielectric constant value and reintroduces the SiO_xC_y transition layer.

In this letter, we present a method of integrating HfO₂ on SiC as a potential architecture for the gate stacks of SiC power devices. By depositing the high-K dielectric on wafer bonded Si/SiC heterojunction structures, we aim to overcome the poor reliability (and high interface trap density) of thermal oxides, and the high leakage currents of high-K dielectrics formed directly on SiC. Studies of HfO₂ on Si have shown it to be a reliable oxide with a low interface trap density compared to SiO₂/SiC interfaces, and low leakage currents. To demonstrate the feasibility of integrating this solution on SiC, Si is wafer bonded to on-axis SiC, previous work¹⁶ having proven the quality of this interface. Practical devices would be fabricated on mechanically polished off-axis 4H-SiC wafers. The Si/SiC interface is one that we have characterised extensively, the Si having been formed both by Molecular Beam Epitaxy (MBE)^{17,18} and wafer bonding (WB)^{19,20}, whilst we have also discussed the inhomogeneous interfacial properties of similar structures²¹.

HfO₂/Si/SiC structures were formed alongside three other structures for comparison. These comprised of a

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HfO₂/Si, a HfO₂/SiC and a HfO₂/SiO₂/SiC structure. The thickness of the HfO₂ was 40 nm in each case, whilst the SiO₂ was 12-15 nm thick. In forming the Si/SiC heterostructure, wafer bonding was performed using commercial 3 in. on-axis 4H-SiC substrates from Cree Inc., USA. Epitaxial layers of on-axis 4H-SiC were grown on the substrates, highly n-type doped at $N_D = 1 \times 10^{18} \text{ cm}^{-3}$. The Smartcut process transferred 400 nm of p-type Si doped at $N_A = 1 \times 10^{17} \text{ cm}^{-3}$ onto the SiC surface using a hydrogen-ion implant, room-temperature wafer bonding, and subsequent heat-treatment for wafer splitting. Before wafer bonding was performed, the Si wafer was implanted with H₂⁺ ions with an energy of approximately 200 keV and a fluence in the range of 10^{16} - 10^{17} cm^{-2} . Both wafers were then cleaned using standard RCA1, RCA2 and piranha cleans. Rinsing and drying of the wafers was performed before bonding. The wafers were bonded in a vacuum at room temperature followed by a 150 °C anneal in order to achieve a sufficient bond strength for cleaving. They were then cleaved at a temperature of 300 °C followed by a 1100 °C anneal for 2 h to strengthen the chemical bonds. Further details regarding the results of this process can be found elsewhere²⁰.

The formation of the SiO₂/SiC structures was achieved by using the aforementioned cleans on an identical SiC wafer. Thermal oxidation of the surface was carried out through a standard wet oxidation process lasting 2 hours at 1100 °C, resulting in an oxide 12-15 nm thick. The 40 nm of HfO₂ was deposited onto the samples using a Savannah-200 ALD system from Cambridge NanoTech Incorporated. The ALD system is based on precursor wave propagation and is carried out in a small profile chamber at a controlled temperature and vacuum. The system is provided with deionized H₂O or O₃ as oxygen precursors together with Tetrakis(Dimethylamido)-Hafnium for HfO₂ deposition. N₂ was the carrier/purging gas.

A thorough physical analysis of the Si layer was undertaken to assess its state after wafer bonding, which ideally should be crystalline, free of stress, and free of contaminants or unwanted oxides at the interfaces. Figure 1 shows the XRD and Raman spectroscopy results. Both techniques compare the Si/SiC structure prior to oxide deposition, with substrates of Si and SiC. The XRD results of image a) shows that the heterojunction structure displays only the Si and SiC peaks that one would expect from substrates of these materials. Hence, the Si layer comprises of a single crystal. The Raman results of images b) and c) indicate that no phase shift has taken place after the wafer bonding process. This means that no stress has been induced into the Si layer. Both these results mean that electron transport within the Si layer is uninhibited, and the resistance of the layer should be as low as in a regular Si wafer of the same doping.

Figure 2 shows three TEM images of the layers. Image a) gives a view of all the layers of the HfO₂/Si/SiC structure. A discoloured interface region exists at the Si/SiC boundary marked α and a higher resolution image of this

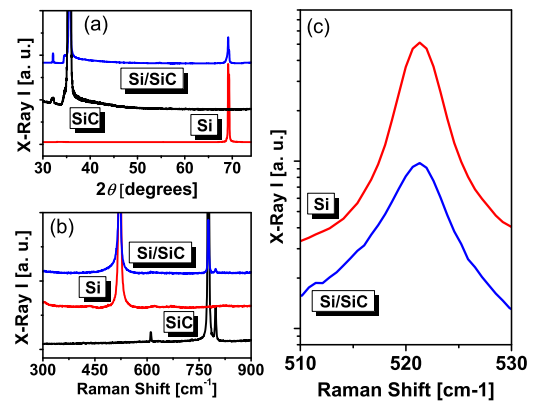


FIG. 1. (a) XRD theta-2theta of the Si substrate, 4H-SiC substrate and of wafer bonded Si/SiC structure. (b) Raman spectra of the Si substrate, 4H-SiC substrate and of wafer bonded Si/SiC structure. (c) Detail of the Si peak of the spectra at 521.3 cm^{-1} .

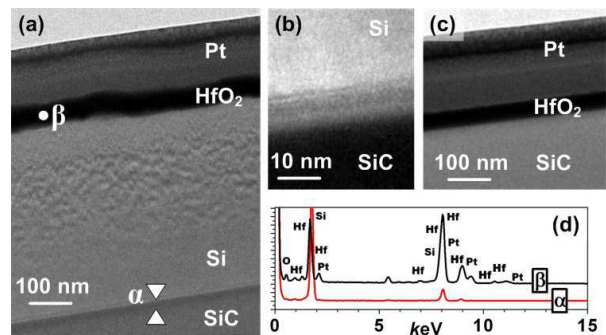


FIG. 2. (a) TEM cross-section of SiC/Si/HfO₂. (b) Detailed picture of the Si/SiC interface. (c) TEM cross-section of SiC/HfO₂. (d) EDX measurement of the interfacial region (α) and of the HfO₂ layer (β).

boundary is shown in image b). Any SiO₂ build up at this interface would limit current transport between the semiconductors. Plot d) shows the EDX spectrum of area α . The EDX spectrum appears to be free of oxygen, with the only prominent peaks attributable to Si. The presence of parasitic peaks of Pt is a common effect that occurs because some electrons diffuse up to the platinum top layer emitting from there. Plot d) also shows the spectrum for point β , the HfO₂ layer. The many peaks here represent the hafnium and oxygen present, whilst there are also some platinum peaks. The size of the EDX spot within the TEM is in the range of 10-100 nm, which is small enough to separate regions α and β . Image c) shows the TEM image of a HfO₂/SiC structure. Noticeable in this image, is the uniformity of the HfO₂ layer compared to the layer on the Si/SiC structure. This is due to the rough finish of the Si layer.

High frequency (100 kHz) C-V analysis was carried out on the four fabricated samples and the resulting

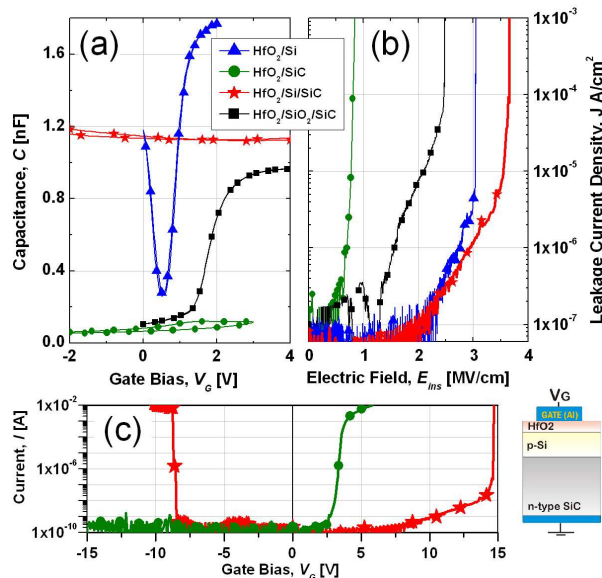


FIG. 3. (a) C-V results from the High-K MOS structures. (b) Leakage and breakdown characteristic taken using I-V analysis. (c) The forward and reverse breakdown of the SiC/Si/HfO₂ structure compared to the SiC/HfO₂ structure.

curves are presented in Fig. 3a. The development of HfO₂/SiC capacitors has been hindered by the inadequate conduction band offset of approximately 0.7 eV between the materials²². The leakage current that results is the most likely cause for the immeasurable accumulation signal seen for this structure in Figure 3. To counteract the leakage, a thermal oxide was reintroduced forming a HfO₂/SiO₂/SiC capacitor and, with its wide bandgap preventing the large leakage current, the structures can be seen to produce adequate C-V inversion-accumulation characteristics in Fig. 3a. However, reintroducing a SiO₂ interlayer also reintroduces its associated problems, decreasing the effective dielectric constant, and leaving carbon-based traps in the channel. The HfO₂/Si layer, with a conduction band offset¹² of approximately 1.5 eV, can be observed transitioning from depletion to inversion, as one would expect. The HfO₂/Si/SiC structures however appear to show little variation in the capacitance. This unusual response may be explained by the inclusion of the heterojunction layer. With only 400 nm of moderately doped Si sandwiched between the oxide layer and the highly doped SiC, it seems quite likely that the spread of the depletion layer may be limited, with little chance of the MOS device being able to enter deep depletion. Also, the Si/SiC p-n heterojunction itself has a built-in potential that must be overcome. Hence, the C-V signal may be the result of the MOS capacitance coupled with the heterojunction capacitance.

The blocking characteristics of the structures are displayed in Figure 3b. The HfO₂/SiC capacitor quickly broke down at less than 1 MV/cm due to

the small band-offset between the materials, whilst for the HfO₂/SiO₂/SiC capacitor it was approximately 2.5 MV/cm, consistent with other studies^{14,23}. However, with its large band offset, the wafer bonded HfO₂/Si/SiC capacitor exceeded both of these at 3.5 MV/cm, with a leakage current consistent with the other structures. In Figure 3c, this result is further compared with the HfO₂/SiC structure. As the SiC is n-type, the HfO₂/SiC capacitor breaks down only with the application of a positive (accumulation) voltage. The HfO₂/Si/SiC capacitor suffers breakdown in both directions most likely due to the p-n heterojunction beneath the oxide. In the forward direction, the p-n heterojunction is forward biased, and there should be no obstruction to electron flow. Hence, the voltage is entirely dropped over the oxide, now effectively a Si/HfO₂ structure, perhaps explaining their very similar breakdown values. In the reverse direction, the bands of the p-n junction bend the other way and a large depletion region is formed. This is then effectively two capacitors in series, reducing the overall capacitance of the structure. This acts as a potential divider for the total voltage dropped over the structure and may also explain the reduced breakdown voltage in the reverse direction.

A method of reducing leakage current in a high-K - SiC MOS capacitor has been presented, using a wafer bonding technique to form a Si/SiC heterojunction substrate. A range of physical analysis tools including TEM and raman spectroscopy, proved that the wafer bonding of the substrates introduced no stress and was free of contaminants at the interface. I-V results showed that the structures could withstand 3.5 MV/cm, exceeding values attained for HfO₂/SiO₂/SiC and HfO₂/SiC capacitors. C-V analysis of HfO₂/Si, HfO₂/SiC, HfO₂/SiO₂/SiC and HfO₂/Si/SiC was presented and the impact of reduced band-offsets and interfacial engineering of the effective capacitance was discussed.

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