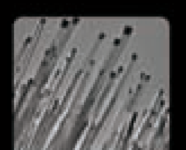
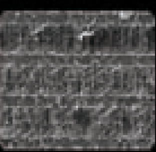
Monolithic integration of VLS silicon nanowires into planar thermoelectric generators

Diana Dávila Pineda





Monolithic integration of VLS silicon nanowires into planar thermoelectric microgenerators

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under the supervision of:

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El Dr. Luis Fonseca Chácharo, investigador científico del Instituto de Microelectrónica de Barcelona (IMB-CNM,CSIC), y el Dr. Albert Tarancón Rubio, investigador del Institut de Recerca en Energia de Catalunya (IREC),

CERTIFICAN:

Que la memoria titulada **"Monolithic integration of VLS silicon nanowires into planar thermoelectric microgenerators"** presentada por Diana Dávila Pineda para optar al grado de Doctora en Ingeniería Electrónica por la Universitat Autònoma de Barcelona ha sido realizada bajo su direccin en el Instituto de Microelectrónica de Barcelona del Consejo Superior de Investigaciones Científicas.

Barcelona, Diciembre 2011

Dr. Luis Fonseca Chácharo　　　　Dr. Albert Tarancón Rubio

“Es ist nicht genug, zu wissen,
man muss auch anwenden.
Es ist nicht genug, zu wollen,
man muss auch tun.”

Johann Wolfgang von Goethe

Abstract

The increasing demand for portable power required by miniaturized systems is driving the development of new technologies and materials to achieve efficient energy generation at the microscale. Apart from removing heat from electronic devices, thermoelectric microgenerators offer an attractive opportunity to harvest waste heat converting it into power. The low thermoelectric conversion efficiency of current bulk microelectronics semiconductor materials has limited their implementation for energy harvesting purposes. However, recent studies have proven, at single nanowire level, that nanostructuring of silicon into nanowires greatly enhances the thermoelectric properties of this material, opening up the opportunity for the integration of thermoelectric generators into silicon microtechnology.

In this thesis, dense and well-ordered arrays of silicon nanowires (Si NWs) have been monolithically integrated into a silicon micromachined device. The VLS-CVD technique has been used for the controlled lateral growth of nanowires. The microstructure has been appropriately designed to adapt the tridimensional growth of the Si NWs arrays to a planar architecture, and to assure electrical accessibility to the nanowires. Additionally, the device allows an internal in-plane temperature gradient to be established when placed in contact with a heat source, giving rise to a complete thermoelectric microgenerator in which the Si NWs act as the nanostructured thermoelectric material.

This thesis is intended to bring new background in thermoelectric materials integration, characterization techniques and fabrication technologies to the IMB-CNM (CSIC), paving the way for the development of future generations of thermoelectric microgenerators.

The work presented in this thesis is divided into four chapters. The first chapter introduces thermoelectricity and its underlying physics, reviewing the state-of-the-art of thermoelectric materials and devices. The

second chapter focuses on the experimental and technological tools employed along this study. The third chapter describes the process followed for the design, simulation and fabrication of the building block of the proposed planar thermoelectric microgenerators based on a single Si NWs array. Finally, chapter four studies the enhanced performance of thermoelectric microgenerator structures by means of transversally linked Si NWs arrays, further adapting and exploiting the 3D lateral growth of VLS Si NWs.

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Scope of the thesis

This thesis is dedicated to *explore* the feasibility of using silicon nanowires as an efficient thermoelectric material in an energy microgenerator device. The work developed along this thesis intends, first, to take advantage of the relative abundance of silicon in the Earth's crust compared to that of the elements typically employed in thermoelectric materials (e.g. Bi, Te). Second, to exploit the good thermoelectric properties that have been recently reported for single silicon nanowires (Si NWs). Finally, to use a silicon wafer-based microfabrication technology to develop thermoelectric microgenerators with high throughput processing and scalability (Figure 1).

For this purpose, the microtechnology expertise of the working group and the available knowledge to synthesize silicon nanowires in large numbers will be used in order to fabricate silicon microplatforms compatible with the VLS silicon nanowire growth method leading to monolithically integrated microgenerators.

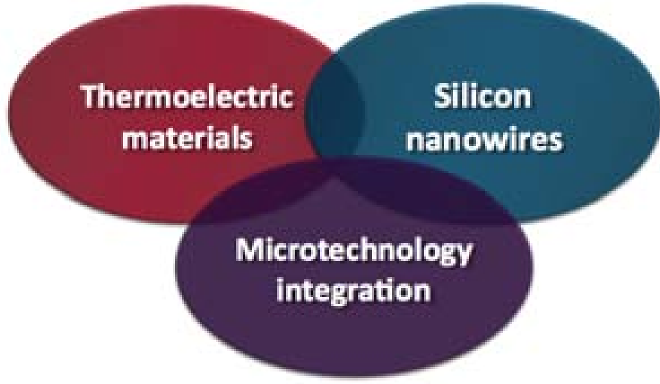


Figure 1: Scope of the thesis

In addition, it is hoped that this thesis will bring new background in thermoelectric materials, characterization techniques and fabrication technologies to the working group in order to pave the way for the development of future generations of thermoelectric microgenerators. It is also important to mention that the "Thermoelectrics group" at the IMB-CNM started with this thesis only three years.

This thesis is organized as follows,

- A brief introduction to thermoelectric generation and fundamentals of thermoelectricity is given in **Chapter 1**. The state-of-the-art of both thermoelectric materials and devices is reviewed as well.
- **Chapter 2** is focused on the experimental and technological aspects. The microfabrication processes used along this thesis, the synthesis of silicon nanowires and the characterization techniques employed together with the experimental set-ups that were developed and tailored for this purpose are described.
- The fabrication of microplatforms and the integration of silicon nanowires for the development of a thermoelectric microgenerator is discussed in **Chapter 3**. The process flow followed for the fabrication of the device is described, i.e. design, simulation, microfabrication and proof-of-concept characterization.
- **Chapter 4** deals with the optimization of thermoelectric microgenerator structures based on transversally linked Si NWs arrays, adapting and exploiting the capability of 3D lateral growth of VLS Si NWs.

Five appendixes were added to the manuscript. **Appendix A** describes the experimental procedure followed in order to find a metal able to withstand the aggressive conditions to which the devices were subjected during silicon nanowire growth, i.e. strongly reducing atmospheres, high temperatures and rapid heating/cooling rates. In **Appendix B** the efforts to ensure the orientation of the (110) Silicon-On-Insulator (SOI) wafers used along this thesis are described. **Appendix C** presents the narrow technological window of the silicon nanowire growth mechanism employed along this thesis, describing the most sensitive parameters to consider. **Appendix D** details the methodology followed for the estimation of the density of arrays of silicon nanowires. Finally, **Appendix E** describes the labor invested in the development of thermally isolated structures for future thermal characterization of silicon nanowires.

1

Introduction

Fossil fuels have been our main source of energy since the Industrial Revolution. Due to its own nature, the fossil fuel stock can only be depleted, and this is what it has been doing at an alarming pace because of the impressive increase of energy demands in the last decade of globalization, leading to an unsustainable energy availability situation. This situation is doubly alarming due to the environmental side effects (climate change/global warming) associated to the irrational use of fossil fuels. Political considerations over the security of energy supply and the environmental concerns are expected to move the world's energy consumption away from fossil fuels. Reducing carbon emissions and ensuring energy availability are closely linked and a challenge to society on a global scale [1, 2]. While political measures may show a short-term impact, technology offers a realistic hope for a long-term solution.

About 90% of the power generated worldwide is based on the use of fossil fuels in heat engines. Since a heat engine has an effective efficiency of around 30-40%,

it is estimated that around 15 TW of power are lost as waste heat not used during the energy conversion process [3]. Besides the ones derived from the use of fossil fuels, there are a lot of non-exploited heat sources like the human body, the interior of houses which are thermally conditioned, flight decks or computer processors, among others. The direct use of this residual heat for other processes is difficult to achieve due to the characteristics of the sources that generate it (dispersion and small scale, wide range of temperatures, instability and variability of temperature, low energy density per unit volume and weight...) and therefore, new strategies for the conversion of this heat into another type of energy like electricity, more useful and convenient for most of the processes, are desirable.

Energy harvesting has been around for centuries in the form of windmills, watermills and passive solar power systems. In recent decades, technologies such as wind turbines, hydro-electric generators and solar panels have turned harvesting into a small but growing contributor to the world energy needs. These are several macro-scale harvesting technologies able to add kilowatts or megawatts to power distribution systems. However, they are not an option for miniaturized systems where long-lasting operation without cords or even batteries is desired. Energy harvesting microsystems are the answer. The growing demand for portable power required by these miniaturized systems is driving the development of new technologies and materials to achieve efficient energy generation at a microscale. Although batteries are a well-established technology for portable applications, they cannot be considered the final stage for attaining fully autonomous systems since periodical human intervention is required. Alternative power sources based on energy harvesting are promising candidates to substitute batteries due to their ability to extract unlimited power from the environment or secondary processes, having little or no adverse environmental effects. Energy harvesting's new frontier is an array of micro-scale technologies that scavenge milliwatts from solar, vibrational, thermal and biological sources.

Due to the large amount of residual heat yielding from the current energy generation technology based on fossil fuels, or other naturally occurring thermal gradients, macro thermoelectric energy harvesters have received special attention in recent years [4]. Thermoelectric generators (TEGs) are used in a wide variety of applications all over the world as well as in space missions. TEGs consist of three parts: ***a heat source, a heat sink and a thermopile***. The heat source and heat sink provide the energy to the system by creating a temperature gradient across the

thermopile. The thermopile connects the heat source and heat sink, and serves to convert some of the thermal energy contained in the thermal reservoirs into electrical energy [5]. Due to their high reliability, small size, and relatively low cost, thermoelectric devices can be utilized in a myriad of applications, from energy recovery of the thermal waste of modern jet engines [6, 7] to the cooling of relatively small volumes such as in portable coolers [8].

In the following sections, the basics of thermoelectricity (thermoelectric effects and main material properties involved in) as well as its state-of-the-art in terms of materials, heat transport phenomena and devices will be reviewed. Special attention to the few thermoelectric microgenerators already available is payed in order to set up the framework of the experimental work done in this thesis along the lines exposed in the scope section.

1.1 The thermoelectric effect

The thermoelectric effect describes the interaction of heat and electricity in metals and semiconductors in which charge carriers are free to move much like gas molecules, while carrying charge as well as heat. When a temperature gradient (ΔT) is applied to a thermoelectric couple, the mobile charge carriers at the hot end tend to diffuse to the cold end. The build-up of charge carriers results in a net charge at the cold end, producing an electrostatic potential (ΔV). Thus an equilibrium is reached between the chemical potential for diffusion and the electrostatic repulsion due to the build-up of charge. This property, known as the Seebeck effect, is the basis of thermoelectric power generation. Conversely, when a voltage is applied to a thermoelectric couple, the carriers attempt to return to the equilibrium that existed before the current was applied by absorbing energy at one connector of the thermocouple and releasing it at the other, this effect is known as the Peltier effect [4, 9].

While developing new materials and models is crucial to improve and understand the operation of thermoelectric devices, this will be considered beyond the scope of this work. Instead, this thesis will be focused on understanding the phenomenological characteristics of thermoelectric devices to develop a new technology.

- **The Seebeck effect**

Thermoelectric energy conversion was discovered by Thomas Seebeck in 1821. When two dissimilar conductors, A and B (referred to in thermoelectrics as thermocouple legs, arms, thermoelements or pellets), which are connected electrically in series but thermally in parallel, are maintained at different temperatures (T_1 and T_2, $T_1 > T_2$) a voltage is developed between the hot and cold ends (Figure 1.1) defined by

$$V = \Delta S \times \Delta T \tag{1.1}$$

where ΔS is the differential Seebeck coefficient between the materials A and B and ΔT is the temperature difference. The Seebeck coefficients depend on the conductor's absolute temperature, material and molecular structure. Any electrically conductive material with a finite S and subjected to a temperature gradient develops a voltage difference between points of different temperatures.

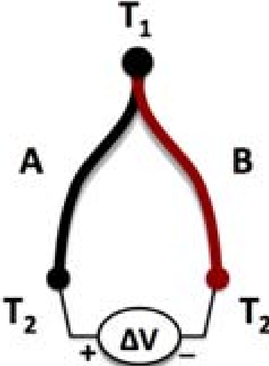


Figure 1.1: Schematic of a basic thermocouple - The voltage difference, ΔV, produced across the terminals of an open circuit made from a pair of dissimilar conductors, *Material A* and *Material B*, whose two junctions are held at different temperatures, is directly proportional to the difference between the hot (T_1) and cold (T_2) junction temperatures.

- **The Peltier effect**

In 1834, Jean Peltier discovered that when current flows between two dissimilar materials held at a constant temperature, heat is often absorbed or released at the interface. This phenomenon is known as the Peltier effect.

This effect occurs when an electric current passes through a junction between two materials having different S.

If a current I is forced to flow through the junction made by two materials held at a constant temperature, a rate of heating (q) will occur at the interface while a rate of cooling -q will occur if the direction of the current is reversed (the direction of the heat flow is also reversed). The heat is directly proportional to the magnitude of the current flowing across the junction and can be decomposed into a contribution from each material. The ratio of heat to current for each material defines the Peltier coefficient (π), which has units of Watts per Ampere or Volts:

$$\pi = \frac{q}{I} \tag{1.2}$$

where I is the electric current magnitude and q is the heat flux at the interface of the two materials. π is the product of T at the interface and the difference in S between the two materials that compose the interface.

- **The Thomson effect**

The Thomson effect relates to the rate of generation of reversible heat q which results from the flow of a current along a portion of a single conductor along which there is a temperature difference ΔT. Providing that the temperature difference is small,

$$q = \beta I \Delta T \tag{1.3}$$

where β is the Thomson coefficient. The units of β are the same as those of the Seebeck coefficient V/K. β is given as

$$\beta = \frac{dS}{dT} \tag{1.4}$$

While the Seebeck and Peltier effects are the main thermoelectric effects, the Thomson effect is not of primary importance in thermoelectric devices but it should not be neglected in detailed calculations. The Joule effect (the heat generated when a voltage is applied across a resistive material), although not a reversible thermoelectric effect and not generally termed a thermoelectric effect, is an important non-ideality of any thermoelectric device.

1.2 Thermoelectric materials properties

Thermoelectric devices are normally made from alternating n-type (electron-charge carrier) and p-type (hole-charge carrier) semiconductor elements joined by metallic connectors (Figure 1.2). Because two dissimilar materials have different Seebeck coefficients, charge carriers flow through the n-type element, cross a metallic interconnect, and pass into the p-type element. When a heat source is provided, the thermoelectric device functions as a power generator. The temperature difference provides the voltage from the Seebeck effect while the heat flow drives the electrical current, which therefore determines the power output (Figure 1.3).

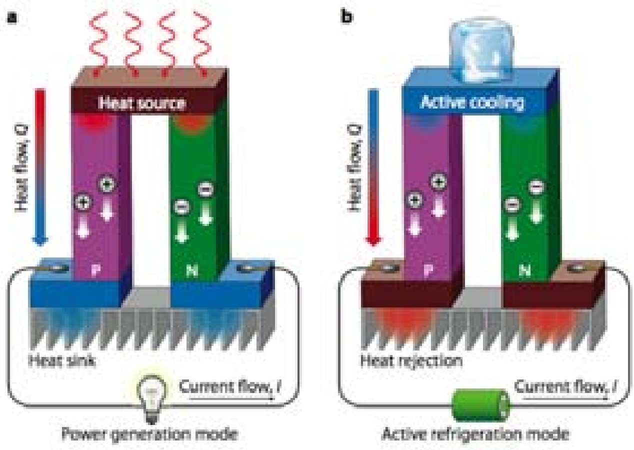


Figure 1.2: Schematic illustrations of a thermoelectric module for (a) power generation (Seebeck effect) and (b) active refrigeration (Peltier effect). - (a) An applied temperature difference causes charge carriers in the material (electrons or holes) to diffuse from the hot side to the cold side, resulting in a current flow through the circuit. (b) Heat evolves at the upper junction and is absorbed at the lower junction when a current is made to flow through the circuit, taken from [10].

A thermoelectric generator contains several thermocouples wired electrically in series and thermally in parallel to convert heat (temperature gradients) into electrical energy. The heat flow across a temperature gradient is used to power an external circuit. Conversely, a heat flux can be forced in a similar structure by applying a voltage, providing a way of cooling. The maximum efficiency of a thermoelectric material for both power generation and cooling is determined by its dimensionless

thermoelectric figure of merit ZT [4] given by:

$$ZT = \frac{S^2 \sigma T}{\kappa} \tag{1.5}$$

where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the temperature. The term $S^2\sigma$ is referred as to the *thermoelectric power factor* —the only "electronic" component that is comprised in the efficiency of a thermoelectric device.

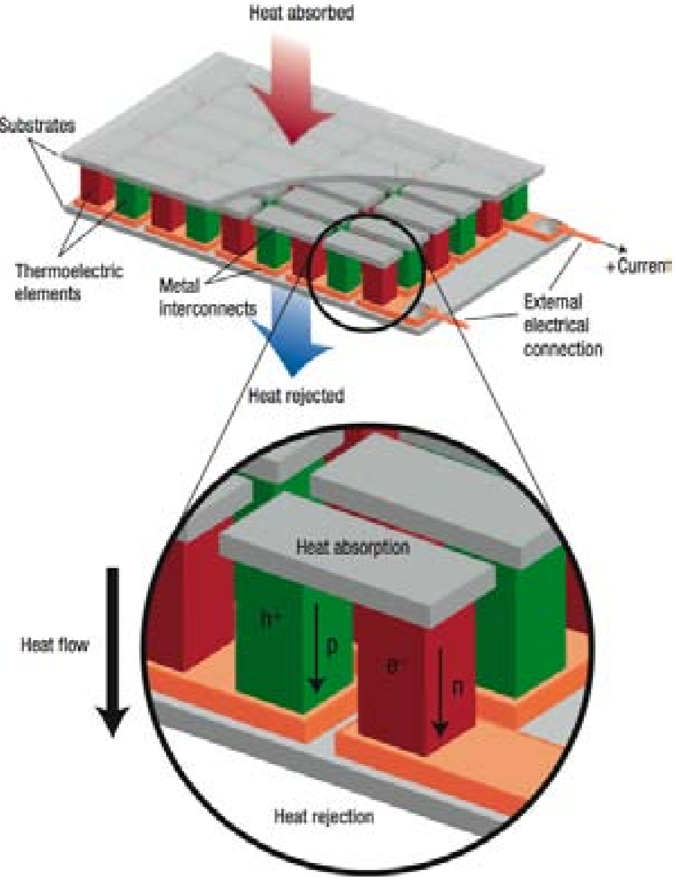


Figure 1.3: Schematic of a thermoelectric module - The image shows the direction of charge flow on both cooling and power generation, taken from [11].

1.2.1 Seebeck coefficient

The Seebeck coefficient (S) of a material is defined as the voltage developed between two points in the material per unit temperature difference between these points. The units of S are typically expressed in μV·K^{-1}.

1.2.2 Electrical conductivity

Electrical conductivity is a measure of the ability of a material to conduct an electric charge. The electrical conductivity (σ) of a material is a product of the number of available charge carriers per unit volume, the amount of charge transported by each carrier, and the ease at which the carriers move in the material in response to an electric field. It is defined as

$$\sigma = en\mu \tag{1.6}$$

where e is the unit charge of an electron or hole, n is the concentration of available charge carriers, and μ is the drift mobility of the charge carriers. The units of σ are typically expressed in Ω^{-1}·cm^{-1}.

1.2.3 Thermal conductivity

The thermal conductivity (κ) quantifies the ability in which thermal energy propagates in a material. The κ of a material has two components: a component due to lattice vibrations (phonons propagation through the lattice, κ_L) and a component due to the random kinetic energy transported by electrons (κ_e). The effective κ of a material is therefore a sum of the lattice and electronic contributions. The lattice contribution to the thermal conductivity is a material-dependent parameter and can be modulated by naturally occurring or engineered scattering centers (alloys, inclusions...) that difficult the propagation of phonons of a wide range of wavelengths. The units of κ are typically expressed in W·m^{-1}K^{-1}.

The thermoelectric effect described above comprises the mechanisms by which thermal energy is transferred to electrical energy. Improving the ZT of a material relies in the optimization of each of the three material parameters S, σ, κ for a given operating temperature range while considering practical tradeoffs. Moreover, in real thermoelectric devices, apart from the fundamental material losses, there are additional parasitic losses that affect the device performance. The thermal conduction of the assembly materials and insulation as well as the contact and wiring

resistances introduce significant non-idealities (imperfect impedance matching and non-zero thermal contact resistance) that have to be considered for final designs.

1.3 State-of-the-art in thermoelectric generation

As it has been previously described, the figure of merit (Eq. 1.5) is a function of three transport coefficients: the electrical conductivity, the Seebeck coefficient and the total thermal conductivity. The thermoelectric performance of a material can be improved through the independent adjustment of these parameters. According to the definition of the figure of merit, a material with good thermoelectric properties shows a high power factor while keeping a low thermal conductivity. However, as shown in Figure 1.4, all these parameters are, at the same time, functions of the carrier concentration leading to a significant trade-off relationship between them. First, the Seebeck coefficient of the material decreases with increasing σ. Therefore, in order to increase the power factor ($S^2\sigma$), the carrier concentration (n) cannot simply be increased to saturation: a peak of ($S^2\sigma$) occurs prior to the saturation of n. Second, as the carrier concentration in the material increases, the electronic contribution to the thermal conductivity κ_e also increases. Interestingly, this coupling of the electrical conductivity with the Seebeck coefficient and the thermal conductivity make semiconductors the best candidates for use as thermoelectric materials. However, only those materials with a ZT>0.5 are usually regarded as good thermoelectric materials [4].

1.3.1 Thermoelectric materials

The field of thermoelectrics advanced rapidly in the 1950s when the basic science of thermoelectric materials became well established. The important role of heavily doped semiconductors as good thermoelectric materials became accepted, the thermoelectric material bismuth telluride (Bi_2Te_3) was discovered and developed for commercialization, and the thermoelectric industry was launched [12]. It was at that time when it was stablished that the efficiency of thermoelectric materials could be described in terms of the dimensionless thermoelectric figure of merit, ZT. During the next three decades, only few advances were made in increasing ZT and up to about 1990, three material families dominated thermoelectrics: Bi_2Te_3-based materials for applications around room temperature (up to 450K), PbTe-based materials for use in an intermediate temperature range (up to 850K) and SiGe for use

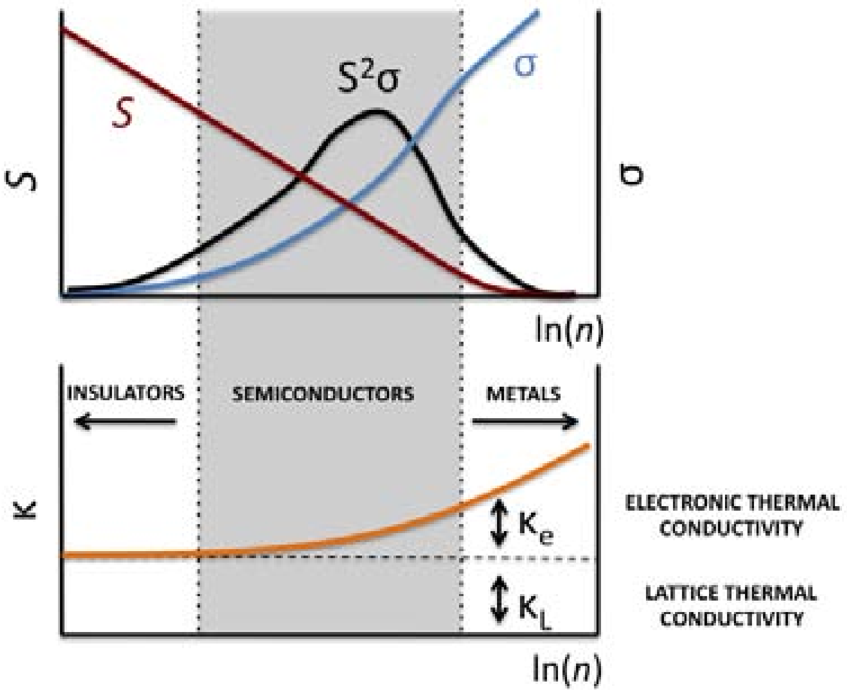


Figure 1.4: Dependence of *ZT* components on carrier concentration - Schematic dependence of electrical conductivity, Seebeck coefficient, power factor, and thermal conductivity on concentration of free carriers (n).

at the highest temperatures (up to 1350K), primarily in Radioisotope Thermoelectric Generators (RTGs) used to power spacecrafts [13]. Even though these classical materials still remain the cornerstone for current commercial applications in thermoelectric generation and refrigeration [4], there have been important advances since the 1990s regarding the synthesis of new materials and the fabrication of material structures with improved thermoelectric performance (Figure 1.5).

It was at the beginning of the 1990s, when the *1st National Thermogenic Cooler Conference* took place, that thermoelectrics caught the eye of the US Department of Defense. From then on, funding agencies like the Defense Advanced Research Projects Agency (DARPA) or the Office of Naval Research (ONR) became interested in the potential of thermoelectrics, encouraging the research community to re-examine research opportunities in this field [12]. This yielded to the development of two different research lines: one focused on synthesizing new materials with

complex crystalline structures and other focused on smart structuring of traditional ones to achieve low dimensional materials systems. This second one being of great interest for silicon based thermoelectricity.

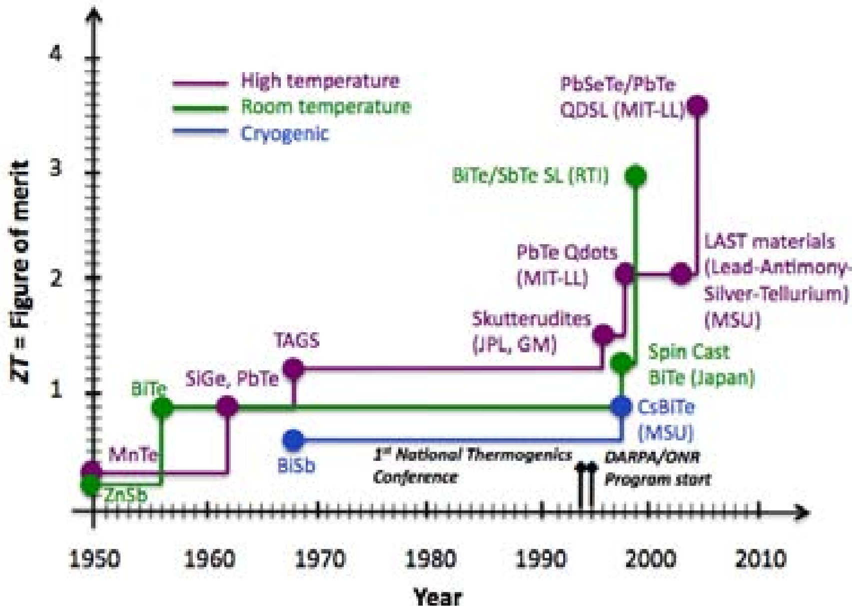


Figure 1.5: History of the thermoelectric figure of merit, selected results - As a direct consequence of the studies performed since the beginning of the 1990s, Harman *et al.* (MIT Lincoln Labs) [14] have demonstrated impressive ZT gains in PbTeSe quantum-dot superlattices (QDSL), reaching ZT values of 3.5-3.6, which is the highest credible report of ZT in the literature, adapted from [13].

The search for new materials has led to the development of a huge number of compound families (Figure 1.6) and is mainly motivated by the suggestion made by Slack and Tsoukala [15] based on the search for the so-called 'phonon glass-electron crystal' (PGEC), which implies that an optimum thermoelectric material should have a low lattice thermal conductivity as in a glass, and a high electrical conductivity as in a crystal. In this type of new materials, such as skutterudites [16, 17] and clathrates [18], the 'rattling' motion of loosely bonded atoms within a large cage generates strong scattering against lattice phonon propagation, but has less of an impact on the transport of electrons. As a consequence, the thermal conductivity of these compounds can be reduced greatly while maintaining the electrical conductivity at a high level [10]. Table 1.1 summarizes the effects produced on phonons

by engineering different thermoelectric material structures [19, 20], e.g. fabrication of complex nanostructures, introduction of vacancies or impurities, grain mixtures, etc.

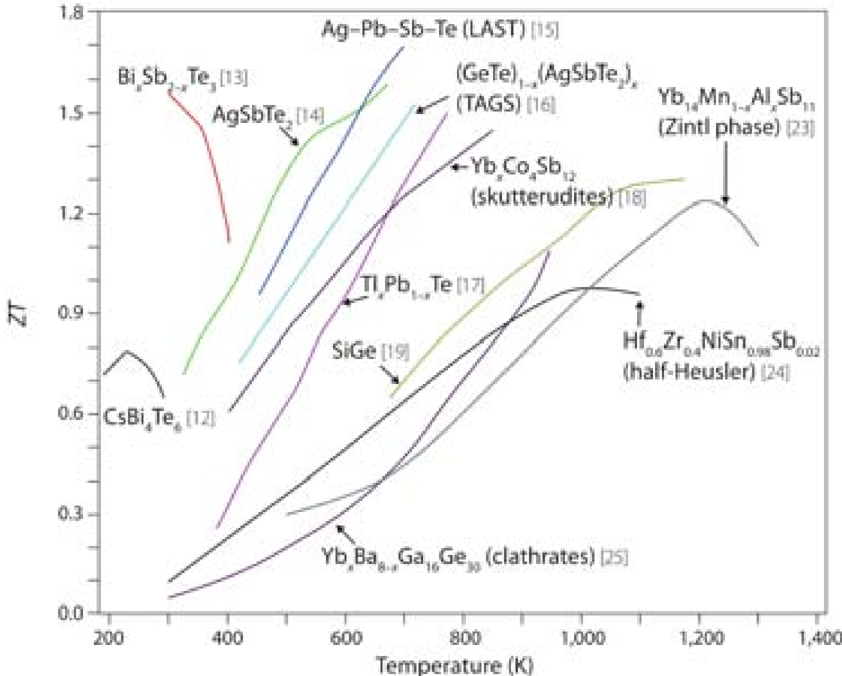


Figure 1.6: State-of-the-art of thermoelectric materials - Figure of merit (ZT) of recent high-performance bulk thermoelectric materials as a function of applied temperature. The high performance of most of these materials, which are complex alloys with dopants, is related to nanostructure engineering, taken from [10].

The research on low-dimensional material systems began in 1993, when Hicks and Dresselhaus discovered their potential working on two theoretical papers that predicted the enhanced thermoelectric properties of quantum wells [21] and quantum wires [22]. These low-dimensional structures such as quantum wells (materials which are so thin as to be essentially of two dimensions, 2D), quantum wires (extremely small cross-section and considered to be of one dimension, 1D, and referred to as nanowires), quantum dots (which are quantum confined in all directions) and superlattices (a multiple layered structure of quantum wells) provide a route for achieving significantly improved thermoelectric figures-of-merit [23]. Possible explanations of such enhancement are an enlarged Seebeck coefficient due to a modified density of

Material structure	Effect on phonons	Recent materials
Complex structure	Increase the number of optical phonon modes	**Clathrate** Chevrel **Intermetallic $Yb_{14}MnSb_{11}$** **Skutterudite** Misfit oxides
Weakly bound atoms (or out of the site positions)-PGEC	Increase disorder (rattling mode)	**Skutterudite** **Clathrate** Penta-telluride
Vacancies	Increase disorder & mass fluctuations	**Skutterudite** **half Heusler**
Solid solutions	Increase mass fluctuations	**half Heusler-Mg_2(Sn,Si)**
Impurities, inclusions	Increase diffusion	New Bi_2Te_3+Te+CuBr **PbTe-TAGS**
Grain boundaries	Reduce the mean free path of phonons	**$AgPb_mSbTe_{2+m}$** Nanocomposites

Table 1.1: Thermoelectric bulk-materials with impact in phonons - Effects produced on phonons by engineering different thermoelectric material structures.

states when quantum confinement takes place and/or a reduction in lattice thermal conductivity due to phonon scattering.

The illustrations shown in Figure 1.7, attempt to categorize the morphological improvement of nanocomposites in thermoelectric materials in terms of several parameters, including dimension reduction, grain refinement and size reduction of a second phase. Single crystals usually present the best electrical conductivity because of the absence of grain boundaries that scatter charge carriers, but the ZT values of such materials can be optimized only by adjusting the carrier concentration through elemental doping. Reducing the dimensions instead, as shown in Figure 1.7(a–d), offers a new possibility to individually tune the thermoelectric parameters (through quantum confinement and scattering of phonons as it will be explained in section 1.5). Apart from surface scattering, the thermal conductivity can be reduced significantly by introducing grain boundaries or interfaces, as shown in Figure 1.7(e–h). Yet, nanostructured thermoelectrics are not limited to single-phase materials. Much interest is emerging concerning nanocomposite materials which combine multiple phases of nanometer-scale dimensions [24]. Figure 1.7(i–l) shows the size reduction of isolated distinct phases or atoms in a composite, including sphere-,

plate- and wire-shaped dispersed phases.

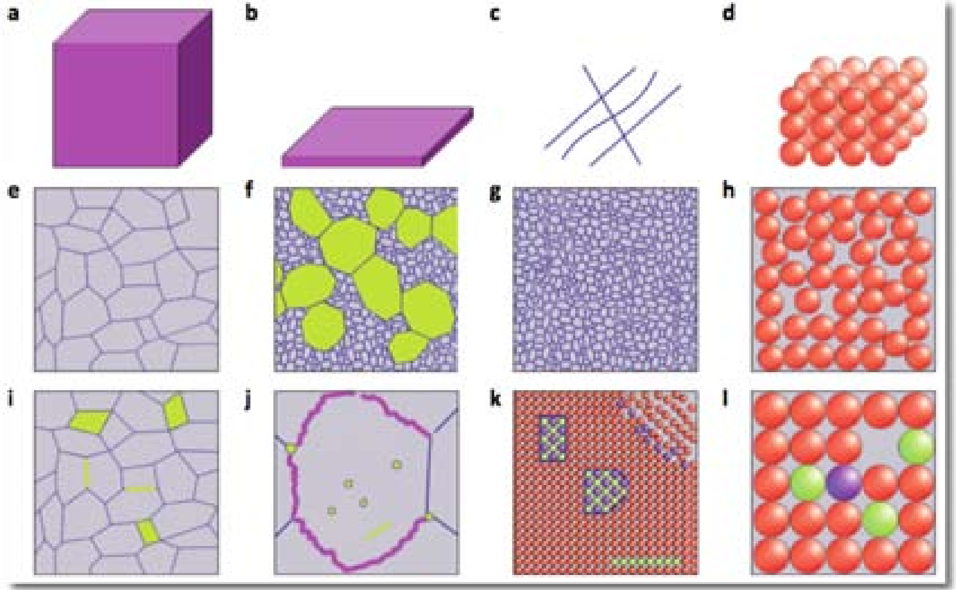


Figure 1.7: Summary of thermoelectric material structures from macro- to nanoscale - (a–d) Change in dimensionality: (a) bulk, (b) thin-film, (c) nanowire, (d) atomic cluster. (e–h) Grain mixtures from micro- to nanoscale: (e) normal micro-grained bulk, (f) mixture of coarse and finee grains, (g) nano-grained bulk, (h) amorphous. (i–l) Size evolution of isolated distinct phases or atoms in the composite: (i) normal composite, (j) nano-dispersions located inside grains or at grain boundaries, (k) nano-inclusions or nanodots, boundary modification, (l) atomic doping or alloying, and vacancies, taken from [10].

Although low-dimensional structures will eventually find application in microelectronics, at present the technology is expensive and applying it to bulk devices problematic. In some aspects nanowires appear as a more attractive proposition for thermoelectric applications than quantum well superlattices because the fabrication process is more compatible with integrated technology [4].

Type	Material	Price in $/kg (metals)
V-VI	Bi_2Te_3	140
IV-VI	PbTe	99
Zn_4Sb_3	Zn_4Sb_3	4
Silicides	p–MnSi1.73	24
	n–$Mg_2Si_{0.4}Sn_{0.6}$	18
	$Si_{0.80}Ge_{0.20}$	660
	$Si_{0.94}Ge_{0.06}$	270
Skutterudites	$CoSb_3$	11
Half-Heusler	TiNiSn	55
n/p–Clathrate	$Ba_8Ga_{16}Ge_{30}$	1000 without Ba
Oxides	p–$NaCo_2O_4$	17 without Na, O
Zintl Phase	p–$Yb_{14}MnSb_{11}$	92
Th_3P_4	$La_{3-x}Te_4$	160

Table 1.2: Raw materials cost per kg of current and known potential thermoelectric materials - Current cost and toxicity of thermoelectrics are incompatible with large-scale use. Affordable materials and structures lack of a high-ZT performance and therefore produce low energy yields or require high volumes, taken from [20].

Current niche-market devices are based on Te-containing compounds. As the ninth least abundant element (1 ppb by weight in the earth's crust) [25], Te is too scarce to support usage. Moreover, the costs of raw materials (Table 1.2) leave little margin for production and fabrication of commercial modules based on Bi_2Te_3, or on the current material of choice for power generation, PbTe [26]. Consideration of both sustainability and cost issues leads to the conclusion that development of high-performance thermoelectric materials, free of tellurium and lead, that incorporate more abundant elements is essential to provide a sustainable basis for wide-scale implementation of thermoelectric technology.

1.3.2 Thermoelectric Devices

Thermoelectric devices are solid-state devices used to convert thermal energy from a temperature gradient into electrical energy (power generation -Seebeck effect) or to convert electrical energy into a temperature gradient (cooling -Peltier effect) as described in section 1.1. The first application is used most notably in spacecraft power generation systems (for example, in *Voyager I* and *II*) and in thermocouples for temperature measurement, while the second application is commonly used in specialized cooling applications like consumer electronics refrigeration [8].

Although thermoelectrics received little attention from the research community after the 1950s when the basis of this field were established, the thermoelectrics industry grew slowly but steadily by finding niche applications for space missions, laboratory equipment, and medical applications, where cost and efficiency were not as important as energy availability, reliability, and predictability [12]. A key development for the thermoelectric 'industry' was the introduction of the first significant consumer product in the early 1990s: a thermoelectric picnic basket cooler [13].

Possibly the most significant commercial development in recent years has been the success of Amerigon (US) in placing thermoelectric coolers/heaters in automobile passenger seats. Amerigon shipped 940,000 units in 2007 [27] and has placed over 3 million of its Climate Control Seat (CCS) options (Figure 1.8) in 20 vehicle models sold worldwide. Just as importantly, Amerigon revenues have grown substantially, the company achieved a world market of almost US$1 billion in 2008 [28]. Moreover, the automobile industry is actively pursuing the capture of waste heat from exhaust to provide additional power to a car.

Since 1992 China has emerged as a major supplier of low cost cooling modules, which are assembled manually. These modules are fabricated by connecting a large number of thermocouples or pellets electrically in series and thermally in parallel and sandwiching them between two high thermal conductivity but low electrical conductivity ceramic plates to form a module (Figure 1.9). Until relatively recently, commercial thermoelectric modules were designed for operation in the refrigeration (Peltier) mode. It is only in the last 5 to 10 years or so that thermoelectric power generating modules have become commercially available with their thermoelement geometry and material composition tailored for this application [4]. This achievement has been driven by the worldwide concern about the harmful effect of global warming and the recognition that thermoelectric technology offers an environmentally friendly method of converting waste heat into electrical power.

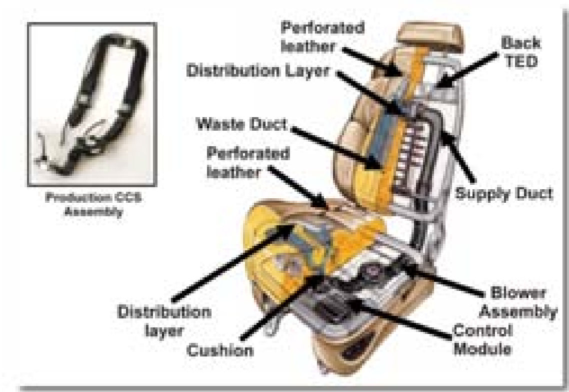


Figure 1.8: Amerigon Climate Control Seat (CCS) for cooling and heating car seats - Amerigons CCS system has led the way for the use of thermoelectrics in the automotive industry, and interest continues to grow. The system, which mounts in the seat frame, adds to perceived performance of the vehicles HVAC system, while reducing the power load required for the overall system, taken from [29].

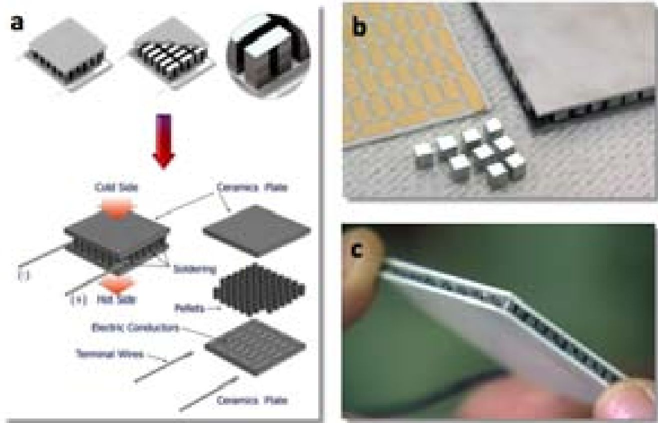


Figure 1.9: A commercial thermoelectric module: (a) configuration, (b) manual assembly and (c) final device - (a) A thermoelectric module is a device composed of thermoelectric couples (n- and p-type semiconductor legs) that are connected electrically in series, thermally in parallel and, fixed by soldering, sandwiched between two ceramic plates [30]. The latter form the hot and cold thermoelectric sides. (b) Commercially available thermoelectric modules are assembled manually. (c) Image of a typical thermoelectric module.

A typical thermoelectric module measures 30 mm x 30 mm x 3.6 mm [31]. Their geometric footprints are small as they vary from 2 x 2 mm to 62 x 62 mm and light in weight. A design engineer should consider using thermoelectrics when the system design criteria includes such factors as precise temperature control, high reliability, compact geometry constraints, low weight, quietness, vibration and shock resistance, fire safety, resistance to dynamic and static overloads, no consumable materials and environmental requirements. Among the advantages of these solid-state devices is important to mention that they do not comprise moving parts, which reduces their maintenance to a minimum and makes them more reliable and long-lasting; and it is easy to switch from cooling to heating mode, which makes them very adaptable depending on the application required. Therefore, thermoelectrics are ideal for many of the consumer, food & beverage, medical, telecom, photonics and industrial applications requiring thermal management. For example, thermoelectrics could substitute conventional compressor-based cooling systems for tight geometric space or low weight applications, or they could be used as power generators converting waste heat into energy in remote locations [31]. The cost and functionality of energy harvesters are important factors for their acceptance by industry and for moving them into mass production. Reduction of the cost can be achieved by using micro and nanotechnologies for high throughput processing [32].

Although the principles and theory of thermoelectrics have been rigorously developed for nearly two hundred years, a widely spread usage in commercial power conversion applications has not been reached until today due to the low conversion efficiencies. While the most metallic configurations are not suitable because of their low Seebeck coefficients, the introduction of semiconductors as thermoelectric materials enabled maximum conversion efficiencies in the range of 5–10% [33, 34], whereby theoretically maximum values are predicted in the range of 20% [35, 36, 37]. The efficiencies are still very low in absolute terms, but it enables a limited economical usage of thermoelectric generators to niche applications, where their outstanding reliability outweighs the low conversion efficiencies.

1.4 Thermoelectric microgenerators

The demand for portable power generation required by miniaturized systems with long-lasting operation is large and expanding. In order to fulfill this demand, high-energy density storage and generation devices are required. Currently available technologies include batteries and micro fuel cells. However, true energy autonomy would eventually be better enabled by energy harvesting devices.

In the last decade a lot of effort has been invested in the development of thermoelectric microgenerators. Most of these attempts, which will be shortly reviewed, have tried to follow the approach of scaling down the typical architecture of a macro thermoelectric generator, i.e. the "out-of-the-plane" leg configuration, which better adapts the naturally occurring thermal gradients. From the materials point of view, microgenerators move from macrostructures like pellets to nanostructures like thin films or superlattices. Although scaling down reduces the output power per device, automation and mass production are enabled if standard microtechnologies are involved.

Regarding the "out-of-the-plane" (vertical) architecture, such geometry is difficult to replicate using microelectronics technology. The reason for this is strictly process-related since microelectronic processes have historically been developed to make lateral structures on silicon wafers. In this planar configuration, the thermocouple legs are patterned on a substrate and the interconnections between them are fabricated on the same surface level, making the fabrication process simpler than the vertical approximation, but consuming more area. This horizontal or "in-the-plane" architecture is typically used in the fabrication of thermopiles for most commercial temperature sensors. If a traditional vertical or "out-of-the-plane" configuration should be replicated, the legs of the thermocouple have to be implemented through the substrate material or structured on it, and some type of suspended interconnections are then needed. This kind of 3D arrangement is hard to achieve monolithically at the microscale in a single substrate. Some alternatives to overcome this issue involve attaching two complementary dies face to face.

The thermoelectric microgenerators developed until now have mainly been based on thin films of the state-of-the-art V-VI semiconductors, e. g. Bi_2Te_3 [4, 38]. Even though these semiconductors have good thermoelectric properties, the microtechnology associated (e.g. patterning) is barely developed and therefore their integration is far from what can be achieved with Si or SiGe. An example of this limitation can be found in the device fabricated by DTS [39] based on V-VI semiconductors where

an area of 64 mm^2 is required to integrate 2250 thermocouples and generate 1.6 μW (ΔT=5K). On the contrary, Infineon Technologies has developed thermoelectric devices based on doped poly-Si and poly-SiGe for wearable electronics applications (Figure 1.10), with a thermoelectric microgenerator formed by 16000 vertical thermocouples in an area of 7 mm^2 to generate 0.112 μW (ΔT=10K) [40].

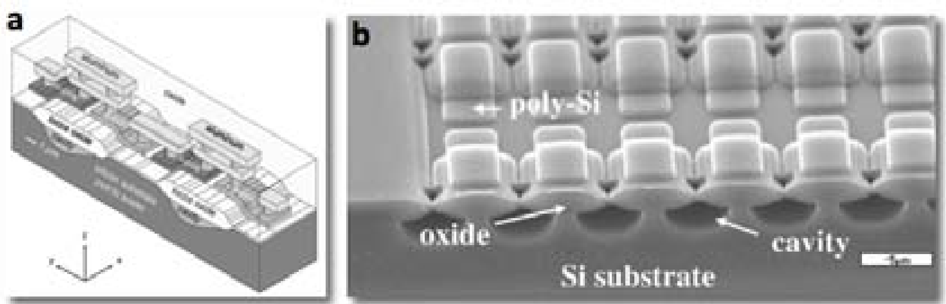


Figure 1.10: Miniaturized thermoelectric generators based on poly-Si and Poly-SiGe surface micromachining developed by Infineon Technologies - (a) Schematic view of two thermoelectric couples of a BiCMOS realization using standard materials. (b) SEM micrograph showing the cavities etched into a Si-substrate in order to optimize the vertical heat flux direction within the microgenerator, taken from [40]

Startups like Micropelt (a spin-off from Infineon Technologies) or Nextreme are pursuing thin-film technologies to produce the next generation of thermoelectric devices. Both companies are developing devices based on a vertical architecture. Micropelt has developed a sputtering method based on Bi_2Te_3 materials to produce wafers and thermoelectric devices compatible with modern semiconductor industry mass-production methods, its TEG MPG-D751 high voltage thin-film thermogenerator (Figure 1.11) is commercially available and capable of delivering 0.14 V/K [41, 42]. Nextreme technology is based on the Bi_2Te_3-Sb_2Te_3 superlattice developed by Venkatasubramanian [38], its eTEG HV56 high voltage thermoelectric generator (Figure 1.12) has demonstrated output power levels of 1.5mW and an open circuit voltage of 0.25V at a ΔT of 10K (0.025V/K) [43]. These companies offer prototypes of their products and have achieved general production providing benefits like size, speed and heat pumping capacity (Watts/cm^2) [13]. Table 1.3 summarizes and compares some of the development achieved in thermoelectric microgenerators.

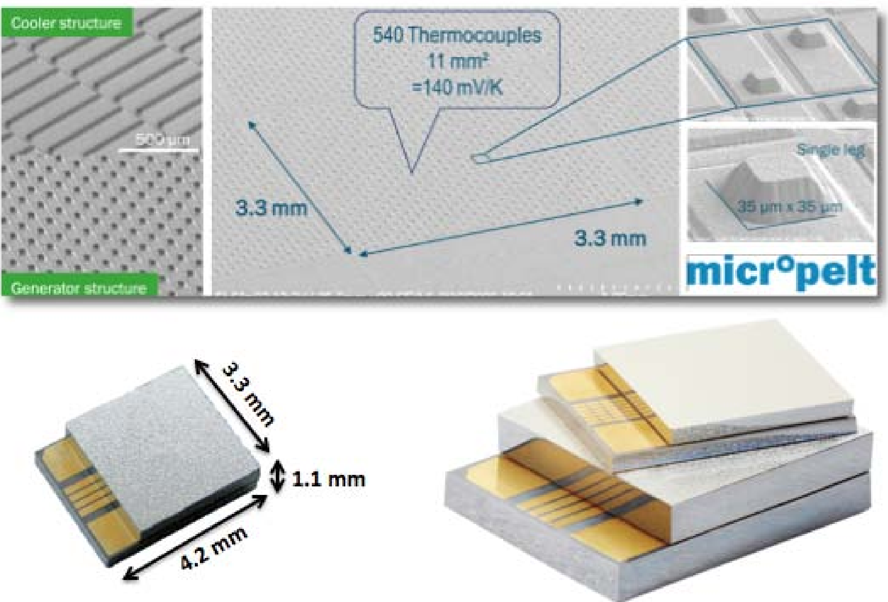


Figure 1.11: High voltage thin-film thermogenerator developed by Micropelt - With the Micropelt technology more than 50 vertical leg pairs are possible on a square millimeter, taken from Micropelt.

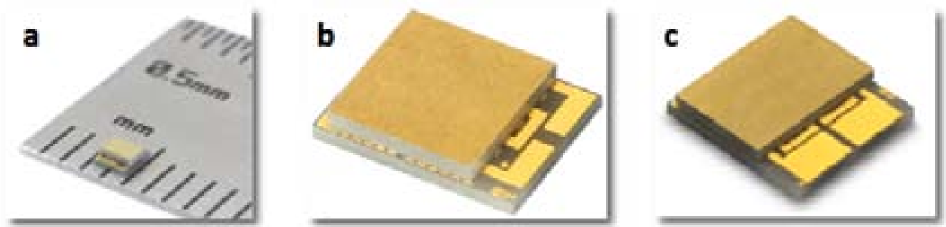


Figure 1.12: Nextreme's thermoelectric generators (TEG) - (a) The eTEG HV14 provides microscale power generation capabilities. (b) The eTEG HV37 is intended for battery charging, medical implants or combined into large arrays for high power applications. (c) The eTEG HV56 high-voltage thermoelectric power generator delivers steady-state clean energy at very low temperature diffeentials, taken from Nextreme.

It is also important to mention the work developed at the IMEC research facilities, which is a world-leading center in nanoelectronics and has an important thermoelectrics group led by Prof. Vladimir Leonov. Their work is based on the

Company	Thermoelectric material	Area (mm^2)	Units	Power (μW)	ΔT (K)
DTS	$(Bi_{0.25}Sb_{0.75})Te_3/Bi_2(Te_{0.9}Se_{0.1})_3$	63.65	2250	1.6 [a]	5
JPL-NASA	$(Bi_{1-x}Sb_x)_2Te_3/Bi_2Te_3$	2.89	63	1	1.25
Micropelt	Bi_2Te_3	1.12	12	0.67 [b]	5
Micropelt	Bi_2Te_3	11	540	400 [c]	5
Nextreme	Bi_2Te_3-Sb_2Te_3	10.23	N/A	1500	10
Infineon	Poly-Silicon	7	16000	0.112	10
HSG-IMIT and Kundo	Si/Al	16.5	1000	1.5 [d]	10
NUS	Top-down Si NWs	162	25	0.0015 [e]	0.12

Table 1.3: Commercially available thermoelectric microgenerators - Comparison of thermoelectric microgenerators developed by different companies. [a]Taken from [44]. [b]Taken from [45, 46]. [c]Simulated results. [d]Taken from [47]. [e]Not a commercially available product.

development of micromachined thermoelectric energy harvesters for applications focused on wearable wireless medical devices using thermal energy, like an electrocardiogram (ECG) in a shirt, a solar/thermal-hybrid powered electro-encephalogram (EEG) with hybrid energy scavenger or wrist thermoelectric generators to power different types of wireless sensors [48]. Their activity mainly comprises the fabrication of both planar and vertical micromachined modules using poly-SiGe thermocouples (Figure 1.13) [49, 50].

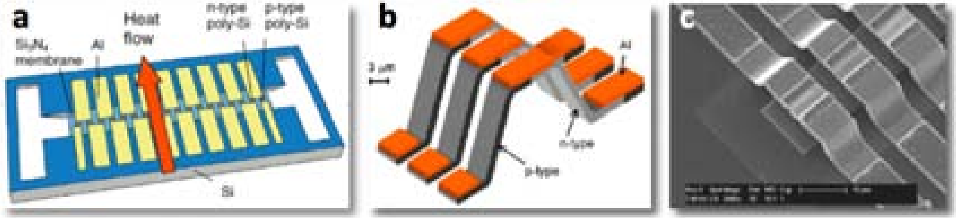


Figure 1.13: Micromachined thermoelectric energy harvesters developed at the IMEC research center - (a) Schematic layout of membrane-less in-plane bulk-micromachined thermopiles for energy harvesting, shown with supporting membrane. (b) Schematic of the design of the thermocouple employed in a thermoelectric energy harvester fabricated by stepper. (c) SEM image of the released thermocouples of the design in (b), taken from [32, 48, 49, 50].

Moreover, although not an energy generation application, it is worth to mention the work developed by Jondetech, where thermopile structures for ultra-thin flexible IR sensors using thermoelectric nanowires have been developed. The thermopile structure proposed by this company features up to 224 vertically-arranged thermocouple legs deposited in a specially prepared polyimide material [51, 52]. The thermopile is optimized for infrared thermal radiation detection and its fabricated using flexible printed circuit board-like (flex PCB-like) processing. One of the main features, and the reason why Jondetech is mentioned here, is the use of bundles of metal nanowires as thermocouple legs. The nanowires are built from antimony and nickel, which are electrodeposited in a polyimide grid in order to form the nanowires. The starting submicron porous polyimide template is obtained using ion track techniques: the polyimide foil is irradiated with swift heavy ions, at an accelerator facility, that produces latent ion tracks (continuous paths of modified material, afterwards chemically revealed) all through the foil thickness (up to 125 μm). Figure 1.14 shows an image of the nanowire-based thermocouples developed by this company, in which the polyimide matrix was removed by plasma etching exposing the thermocouple legs for illustration purposes. The device developed by Jondetech, shows a clever thermoelectric application for nanowires, however, this technology is limited by the metals that can be electrodeposited, and the modest Seebeck coefficient of metals in general.

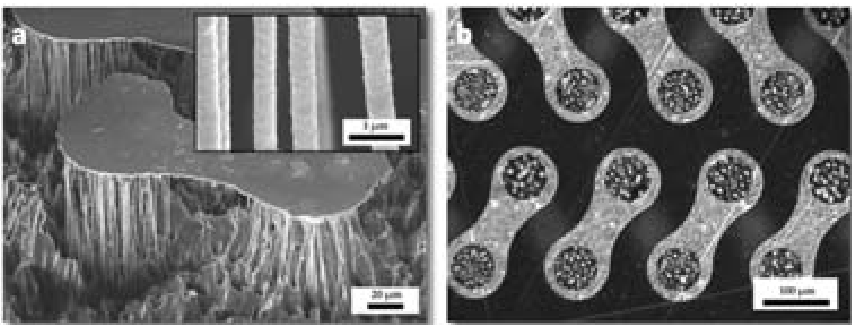


Figure 1.14: Thermoelectric nanowires for ultra-thin flexible IR sensors developed by Jondetech - (a) SEM image showing the bundles of sub-micron strands of a thermocouple with its surface interconnections. The close-up inset view presents the miniature building blocks of this structure. (b) Microscope close-up view showing the surface interconnections (‘dog-bone’ structures) and their coupling to thermoelectric junctions, taken from [52].

Following the vertical configuration for nanowire-based devices, Li *et al.* [53], from the National University of Singapore (NUS), have developed a high-density silicon-nanowire (Si NW)-based thermoelectric generator prepared by a top-down CMOS-compatible technique (Figure 1.15). The 5 x 5 mm TEG is comprised by densely packed alternating *n*- and *p*-type Si NW bundles with each wire having a diameter of 80 nm and a height of 1 μm (each bundle serving as an individual thermoelectric element having 540 x 540 wires). The fabricated TEG has demonstrated thermoelectric power generation with an open circuit voltage of 1.5 mV and a short circuit current of 3.79 μA with an estimated temperature gradient across the device of 0.12 K. The work developed by Li *et al.* represents the first attempt to develop a Si NW-based TEG using a top-down approximation for the nanowire growth. Nevertheless, the complexity of this "out-of-plane" configuration added to a thermal gradient restricted by the nanowire height limit the maximum power output attainable to 1.5 nW.

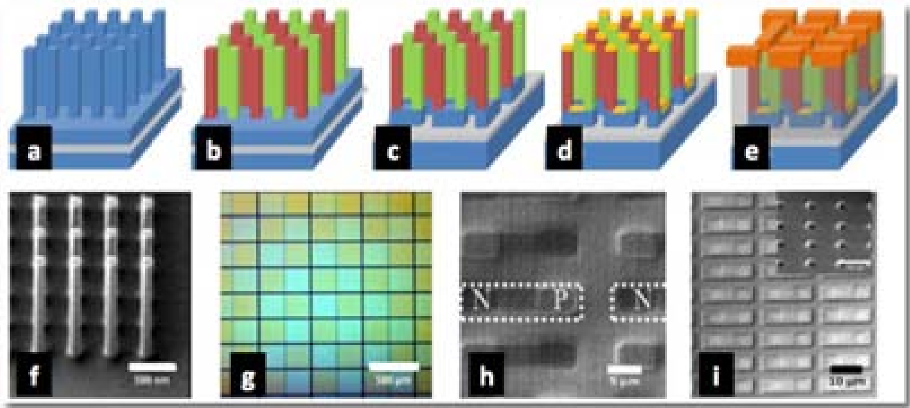


Figure 1.15: Chip-Level TEG based on high-density Si NWs array prepared with top-down CMOS Technology - Schematic of fabrication. (a) Si NW formation by dry etch. (b) Ion implantation and P/N element definition with each element consisting of hundreds of Si NW. (c) P/N couples formed by dry etch. (d) Si NW top and bottom silicidation while protecting the sidewall. (e) Dielectric deposition and etch back to expose only the tip of the Si NW and top metallization. (f) SEM images of pillar formation. (g) N and P implants can be seen clearly under microscope with a different shade. (h) SEM image of Si NW after N/P implant. (i) Metallization etch showing individual N/P couples. Inset shows the tips of the Si NW exposed after oxide etch which confirms the structure of the TEG. (h) and (i) are images of the test structures; the actual design is too large to be shown in SEM image. Taken from [53].

Summarizing, thermoelectric generators might be particularly interesting for portable devices although their implementation in microelectronics is not straightforward. Good thermoelectric materials cannot be easily integrated monolithically in microelectronics processes, and common microelectronics materials result unattractive due to their poor thermoelectric properties. It is clear that the challenge to widespread commercial applications with thermoelectric devices is highly related to the improvement of the thermoelectric figure of merit of the material, ZT, where current fundamental research in nanoscience is actually trying to push the limits. With companies like Micropelt and Nextreme pursuing thin-film thermoelectric devices, like Infineon proving the feasibility of integrating thermoelectrics with microtechnology and research centers like IMEC developing new applications, it seems reasonable to expect further size and cost reductions through mass production and utilization of modern semiconductor manufacturing technologies for introducing new products in the market.

As it has been reviewed along this section, most of the research on thermoelectric microgenerators has been focused on developing microdevices based on the typical vertical architecture (e.g. Infineon, Micropelt, Nextreme, IMEC, etc.) while the horizontal configuration is only used in the design of thermopiles (e.g. IMEC). Moreover, the use of specific materials in the form of thin-films persists and only Jondetech and a research group in Singapore have nanostructured metals and silicon respectively to fabricate vertically aligned bundles of nanowires to form thermoelectric legs. In this thesis, as a step forward, bottom-up silicon nanowires are proposed to increase the figure of merit of bulk silicon [54, 55] using a technique that makes their integration compatible with planar microgenerators. The planar architecture design proposed in this work allows to overcome the limitations of the thermal gradients attainable observed in the work developed by Li *et al.* [53].

In summary, the aim of this thesis is to overcome the difficult implementation of thermoelectric generators with microelectronics materials and microelectronics processes. A good combination of the thermoelectric properties shown by silicon nanowires and their suitable integration into microelectronics could yield a major breakthrough in the fabrication and application of this type of devices.

1.5 Heat transport in low-dimensional materials

As explained in section 1.3, thermoelectric performance is described in terms of a figure of merit, ZT, which is proportional to the operating temperature, the electrical conductivity and the square of the Seebeck coefficient, and inversely proportional to the thermal conductivity. However, due to the intrinsic properties of thermoelectric materials, it can be difficult to increase the electrical conductivity or Seebeck coefficient without also increasing the thermal conductivity.

From equation 1.5, it can be observed that the increase in ZT can be achieved by two means: (1) increasing power factor ($S^2\sigma$) by increasing the Seebeck coefficient of the material or (2) by decreasing the thermal conductivity while maintaining the power factor sufficiently high. However, simultaneous increase of the terms contained in the power factor (Seebeck coefficient and electrical conductivity) is challenging. There is a tradeoff between S and σ since the S of the material decreases with increasing σ (Figure 1.4). The theoretical study of Hicks and Dresselhaus [22] first predicted that thermoelectric efficiency could be greatly enhanced by increasing the Seebeck coefficient, S, over that of the bulk, through quantum confinement of the electron charge carriers. When the dimensionality of the system is decreased from 3D crystalline solids to 2D (quantum wells) to 1D (quantum wires) and finally to 0D (quantum dots) and approaches a scale comparable to the feature length of electron behavior (*e.g.* mean free path, wavelength) in any direction, the density of electronic states (DOS) is increased significantly due to quantum confinement potentially leading to sharp changes in DOS (Figure 1.16). The electron energy bands in quantum-confined structures are progressively narrower as the confinement increases and the dimensionality decreases. These narrow bands should produce high effective masses (electrons behave like free particles with an effective mass that is different from the free electron mass in vacuum) and therefore enhanced Seebeck coefficients. Since S is related to the derivative of the DOS, at the Fermi level, through the Mott relation [56], this affords a means of increasing S and hence ZT [26, 57, 58]. Although theoretical calculations predict the potential to improve $S^2\sigma$ by quantum confinement in low-dimensional structures such as quantum wells [59], nanowires [21], and nanodots, there is no convincing experimental evidence to validate such predictions [60].

Meanwhile, as the dimensionality of a material is decreased, the thermal conductivity is also reduced because the surface/interface strongly scatters the propagation of phonons (as any dimension is smaller than the average free path of phonons).

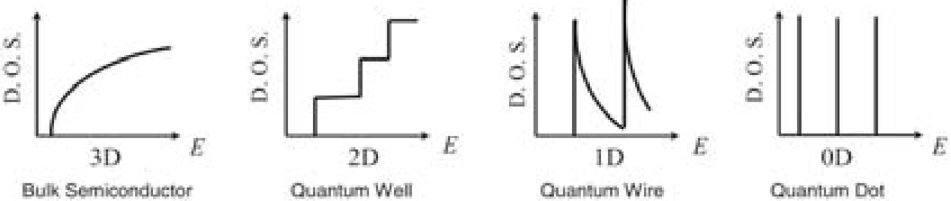


Figure 1.16: Schematic representation of the electronic density of states - Electronic density of states for (a) a bulk 3D crystalline semiconductor, (b) a 2D quantum well, (c) a 1D nanowire or nanotube, and (d) a 0D quantum dot, taken from [57].

As the size of a material decreases, its surface area to volume ratio increases. This reduced dimensionality of the structures may result in confinement of the charge carriers and phonons, thereby affecting transport characteristics, and consequently leading to an enhanced thermoelectric figure of merit [21, 61, 62, 63]. For instance, if we take a cube of a solid of side a, its surface S and volume V, are given by $6a^2$ and a^3, respectively. By plotting the behaviour of the volume and surface as a function of a (Figure 1.17), there is one point where the surface of the solid equals the volume. Below this point phonon scattering effects at surfaces or interfaces become more important than volume effects [64].

In principle, the thermal conductivity κ and the electrical conductivity σ may be independently optimized in semiconducting nanostructures because different length scales are associated with phonons (which carry heat) and electric charges (which carry current). Phonons have mean free paths of hundreds of nanometres, compared with about 10 nm or less for electrons. This means that it is possible to restrict the movement of phonons without hindering the electron mobility. Phonons are scattered at surfaces and interfaces, so κ generally decreases as the surface-to-volume ratio increases. In contrast, σ is less sensitive to a decrease in nanostructure size, although at sufficiently small sizes it will degrade through the scattering of charge carriers at interfaces. For example the directional thermal transport of nanowires can be used to create easy pathways to electrons and restrict the flow of phonons by scattering [65] as shown in Figure 1.18.

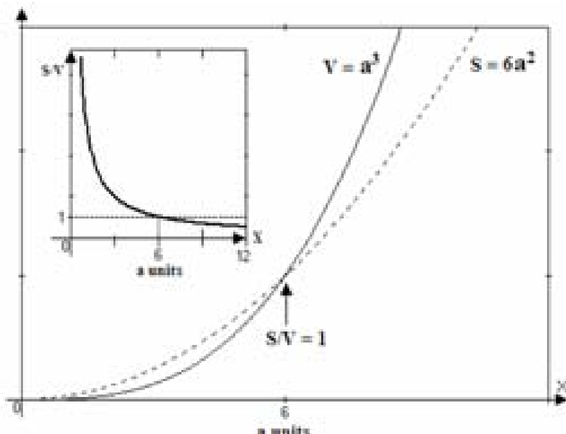


Figure 1.17: Surface to volume ratio for a cubic solid cell of material. Boundary scattering becomes important below S/V=1 - The inset shows the plot of the ratio S/V for the cube of side a. When the side is six length arbitrary units, the ratio is one; if $a>6$ then $S/V<1$ and volume scattering effects take place; conversely if $a<6$ then $S/V>1$ and surface scattering effects become predominant, taken from [64].

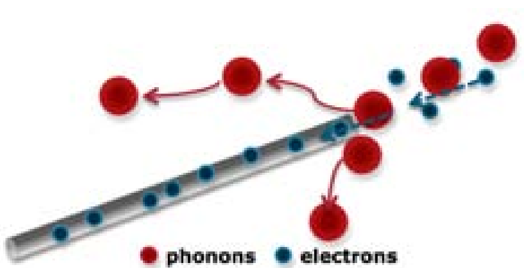


Figure 1.18: Sketch of phonon scattering & electron filtering - Phonon-boundary scattering is responsible for a large reduction in the thermal conductivity of a silicon nanowire where the thickness of the nanowire is comparable to or smaller than the phonon mean free path.

1.5.1 Silicon nanowires as a low-dimensional thermoelectric material

As previously mentioned, despite the fact that thermopower generators are particularly interesting for portable devices, they have not been successfully integrated because the poor thermoelectric properties of the materials traditionally used in microelectronics (e.g. silicon with $ZT \approx 0.01$) and the poor integrability of good thermoelectric materials in mainstream microelectronics. Nevertheless, quantum confinement and phonon scattering effects studied in low-dimension structures offer a promising approach to enhance the thermoelectric properties of semiconductors [57]. For instance, by greatly reducing the thermal conductivity without much affecting the Seebeck coefficient and electrical resistivity, Si nanowire arrays show to be a promising high-performance thermoelectric material, paving the way for thermoelectric devices monolithically integrated in silicon.

Independent works of Boukai *et al.* [54] and Hochbaum *et al.* [55] showed an astonishing enhancement of the thermoelectric properties for the particular case of single silicon nanowires (Si NWs) related to the low dimensionality of the material (Figure 1.19). The work performed by Boukai *et al.* [54] showed that by varying the nanowire size and impurity doping levels, ZT values representing an approximately 100-fold improvement over bulk Si could be achieved over a broad temperature range, including $ZT \approx 1$ at 200 K. Moreover, Hochbaum *et al.* [55] demonstrated that it is possible to achieve $ZT=0.6$ at room temperature in rough Si nanowires of $\sim$50 nm diameter, attributing this ZT enhancement to efficient scattering throughout the phonon spectrum by the introduction of nanostructures at different length scales (diameter, roughness and point defects). However, while the thermal conductivity of silicon nanowires has been shown to decrease from its bulk value for a wide range of nanowire diameters [54, 55, 66, 67, 68], there is only evidence of the enhancement of the Seebeck coefficient for the smallest diameters ($\sim$20 nm) [54]. In addition, this dimensional reduction has an insignificant effect on the electrical conductivity of the material which is close to the bulk value.

Although when synthesized silicon nanowires are usually obtained in large numbers, their enhanced thermoelectric properties have only been measured in *ad hoc* single nanowire test structures. To the author's knowledge, no arrays of bottom-up silicon nanowires have been put to a test in a planar thermoelectric microgenerator, as thermocouple themselves or as a nanostructured form of thermoelectric thin-film material.

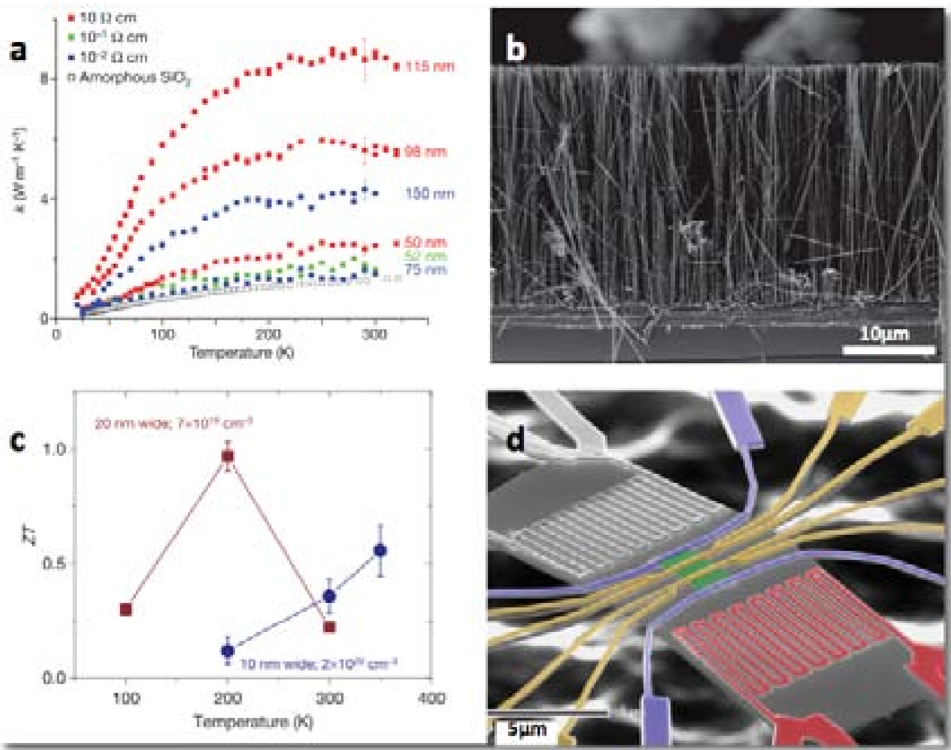


Figure 1.19: Silicon nanowires as efficient thermoelectric materials - (a) Thermal conductivity values of Si nanowires measured by Hochbaum *et al.*, nanowires were fabricated from wafers of different resistivities: 10 Ω·cm (red squares), 10^{-1} Ω·cm (green squares), and 10^{-2} Ω·cm (blue squares). (b) Cross-sectional SEM image of a Si nanowire array fabricated by Hochbaum *et al.*, taken from [55]. (c) Temperature dependence of ZT for two different groups of nanowires and (d) SEM image of the device used by Boukai *et al.* to measure the thermopower and electrical and thermal conductivity of Si nanowire arrays, taken from [54].

2

Experimental methods

2.1 Overview

In this chapter the experimental techniques and technological aspects for both the fabrication and characterization of the devices designed throughout this thesis are described. The most important microfabrication processes used and the optimization of some of them is reviewed. The basic theory for the synthesis of silicon nanowires and the galvanic displacement method employed for this purpose are explained. The characterization techniques used together with the experimental set-ups that were built for this purpose are detailed.

It is important to mention that one of the characterization techniques used in this thesis, the thermoereflectance imaging technique, was learned as part of a 4-months research stay at the Quantum Electronics Group (QEG) in the University of California, Santa Cruz (UCSC), under the supervision of Prof. Ali Shakouri. The QEG studies the mutual interaction of heat, light and electricity in nano and

microscale materials and devices; and has a long experience in the thermoelectrics field, being a pioneer group in the use of the thermoreflectance imaging technique. Moreover, as part of a further collaboration, a thermoreflectance imaging system was acquired and installed at the IMB-CNM through *Microsanj* —a small startup founded by the QEG group.

2.2 Micro & Nanofabrication techniques

The main fabrication techniques employed along this work will be described through this section. It is important to mention that all the micro and nanofabrication processes have been performed at the clean room facilities of the Instituto de Microelectrónica de Barcelona (IMB-CNM) with the help and collaboration of the clean room staff. The silicon nanowire growth has been achieved thanks to a collaboration with Dr. Alvaro San Paulo, Marta Fernández Regúlez and Marc Sansa.

2.2.1 Growth of silicon nanowires

This work is based on the horizontal growth of silicon nanowires originally reported by Islam *et al.* [69] and He *et al.* [70] for single nanowires, and then followed by San Paulo *et al.* for well-ordered nanowire arrays [71]. As a brief description of the method, a catalyst particle deposited in a vertical sidewall of a prefabricated silicon trench promotes the horizontal growth of Si nanowires, which grow from one sidewall and end up bridging the opposing sidewall to form mechanically rigid and electrically continuous double clamped nanobeams (Figure 2.1). Direct integration of nanowire growth into the fabrication of predetermined device architectures simplifies the overall microfabrication procedure. Silicon nanowires have been grown laterally in microtrenches that were defined on Silicon-On-Insulator (SOI) wafers, demonstrating that nanowire growth and device fabrication can be achieved monolithically.

2.2.1.1 The Vapour-Liquid-Solid (VLS) mechanism

Homogeneous, uniformly dense, well-oriented and size controlled silicon nanowires were grown between (111)-oriented silicon sidewalls by CVD using the vapor-liquid-solid (VLS) synthesis mechanism. The VLS mechanism was first proposed by Wagner and Ellis [72] in the mid-1960s and has derived in one of the most important techniques for silicon-wire growth. When catalytic nanoparticles, Au for example,

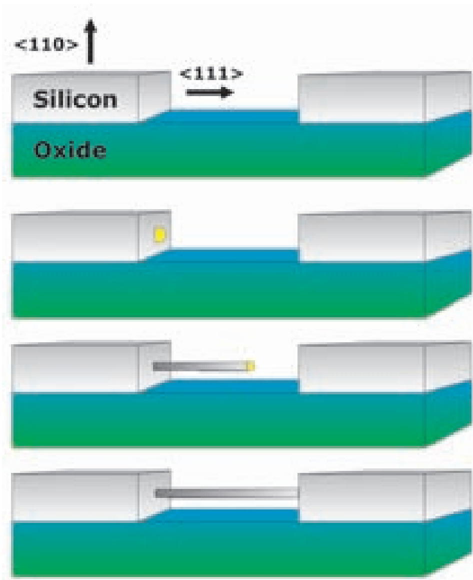


Figure 2.1: Overall process for growth of silicon nanowire bridges in microfabricated trenches - Schematic illustration of the fabrication of the Si nanowire bridge between two vertical Si {111} surfaces on (110)-oriented SOI wafers.

are deposited on a silicon substrate and heated to temperatures above the eutectic point of the Au–Si alloy, i.e. T=363°C, liquid Au–Si alloy nanodroplets will form on the substrate surface. When exposing the substrate to a gaseous silicon precursor, such as silicon tetrachloride, $SiCl_4$, or silane, SiH_4, precursor molecules will crack on the surface of the Au–Si alloy droplets, whereupon Si is incorporated into the droplet. The silicon supply from the gas phase causes the droplet to become supersaturated with Si until silicon precipitates at the silicon/droplet interface. The continuation of this process then leads to the growth of a wire with the alloy droplet riding atop the growing wire (Figure 2.2). The name of the VLS mechanism refers to the fact that silicon from the vapor passes through a liquid droplet and finally ends up as a solid [73].

Like other methods, a chemical vapor deposition (CVD) derives its name from the way the material to be deposited is provided (in this case the silicon required for wire growth). In a CVD process, a volatile gaseous silicon precursor, such as SiH_4 or $SiCl_4$, serves as the silicon source. The precursor is transported in gas phase to the deposition surface at which it reacts. The CVD mechanism allows epitaxial growth

of silicon wires, with the growth velocity varying from about 10^{-2} to 10^{+3} nm/min [74, 75], depending on the temperature and the type of Si precursor used. By using this growth method, a crystallographic contact between the silicon nanowires and two opposing (111) sidewalls is achieved, bridging the sidewalls either though a single nanowire (Figure 2.3a) or arrays of nanowires (Figure 2.3b).

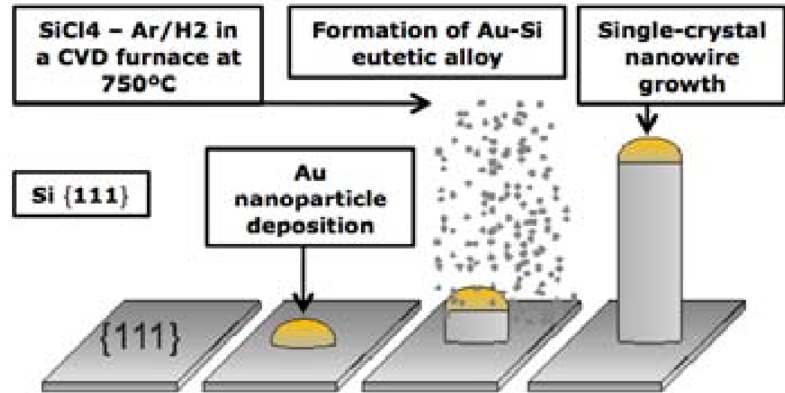


Figure 2.2: Schematic of the VLS growth mechanism - Schematic illustration of a Si nanowire growth from the reaction of $SiCl_4$ and Ar/H_2 vapor phases. This reaction is catalyzed by a gold-silicon droplet deposited on the wafer surface prior to the nanowire growth.

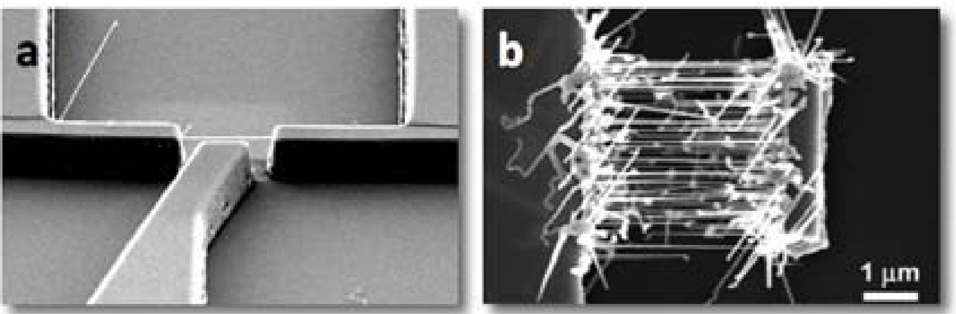


Figure 2.3: SEM images of nanowire array structures - (a) Single nanowire structure and (b) top view of a 3 μm wide single suspended array structure composed of 3 μm long nanowires with 50 nm diameter, taken from [70, 71].

The CVD furnace used in this thesis is shown in Figure 2.4 and is located at the clean room facilities of the IMB-CNM. In this CVD chamber, $SiCl_4$ and BBr_3 are used as the growth precursor and doping gases respectively. In our case, $SiCl_4$ was chosen instead of SiH_4 to ensure epitaxial growth since gaseous HCl, which is a byproduct of the $SiCl_4$ decomposition inside the reaction furnace, etched the oxide layer on the Si surface, presenting a clean Si crystal surface for precipitating Si from the binary liquid droplet and ensuring good contact. In this way, growth direction alignment of the nanowire with the crystal face of the Si wafer is induced by epitaxial deposition of Si at this interface. Such alignment is not possible using SiH_4, without separately adding HCl gas [76, 77] or taking special precautions to remove the oxide layer before SiNW synthesis [78].

The VLS growth mechanism is a temperature-sensitive method. The temperature of growth employed in this work ranged between 745 and 800 °C at atmospheric pressure. Since the set-up used for nanowire growth is experimental, the size of the tube furnace allowed to grow nanowires on substrates with a maximum size of only 2 x 3 cm.

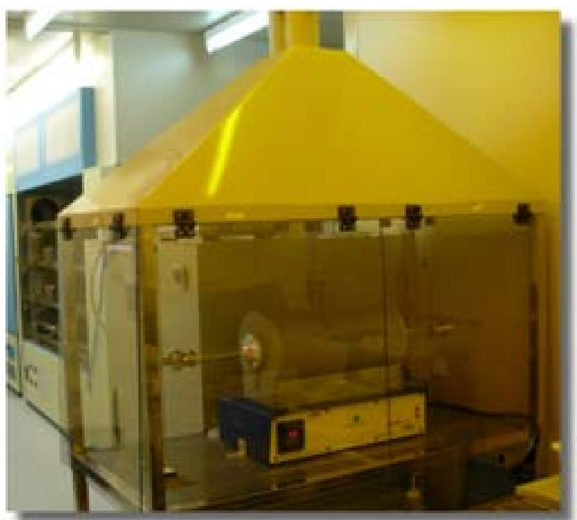


Figure 2.4: CVD furnace used in this thesis for the growth of silicon nanowires - $SiCl_4$ is used as the precursor in an atmospheric pressure CVD (APCVD) and in-situ *p*-type doping is achieved by using a BBr_3 precursor.

2.2.1.2 The galvanic displacement method

Since the early publications of Wagner and Ellis [72], Au has been the catalyst material of choice for growing Si-wires. However, in recent years, a renewed interest focused on the search of catalysts compatible with complementary metal-oxide-semiconductor (CMOS) technology has arisen. In this search, other catalyst have been successfully tested for Si-wire synthesis, such as Ag [72, 75, 79, 80, 81, 82], Al [80, 83, 84, 85, 86], Bi [87], Cd [81], Co [88], Cu [72, 75, 79, 81, 82], Dy [89], Fe [88, 90, 91], Ga [80, 86, 92, 93], Gd [81], In [80, 84, 87, 93], Mg [81], Mn [81], Ni [72, 75, 79, 80, 81, 82, 88, 94], Os [81], Pb [87], Pd [72, 80, 81, 82, 94], Pt [72, 75, 79, 94, 95], Te [87], Ti [96, 97, 98] and Zn [80, 87, 99, 100]; but without doubt, Au is still the most frequently used catalyst since is non-toxic, is chemically inert and easily available, it possesses an eutectic point at a low temperature but high Si solubility, it has a low vapor pressure at elevated temperatures and the Au-Si liquid alloy that forms has a high-enough surface tension [73]. Moreover, it is important to mention the influence of the catalyst employed on growth direction, which is not limited to <111> [100, 101, 102, 103, 104]. The growth direction has been found to be catalyst dependent [86, 95, 105] and, in the synthesis using Au as catalyst, diameter depend [106, 107]. For instance, when silicon nanowires below 20 nm in diameter are synthesized, the growth is produced in the <110> whereas for diameters larger than 30 nm the <111> direction becomes dominant (the transition between these two orientations takes place at a crossover diameter of ∼20 nm around which also the <112> orientation is present) [108]. If another metal such as Pt is used as the catalyst, growth will occur in the <110> for diameter ranges where <111> growth is obtained when using Au [95, 105].

There are several methods employed for the controlled deposition of the catalyst material used for nanowire growth which depend on the size and density desired (e.g. e-beam lithography, colloidal deposition, etc.).

In this work, the galvanic displacement method has been employed to deposit the Au catalyst nanoparticles needed for the VLS synthesis allowing the growth of uniformly dense arrays of silicon nanowires. The key advantage of this method is that the metal deposition occurs selectively on Si surfaces and not on other surfaces such as silicon dioxide and silicon nitride (materials commonly used as masks in microfabrication).

In a galvanic displacement process, gold is deposited on Si through a redox mechanism, in which the Si surfaces themselves act as a reducing agent for gold ions

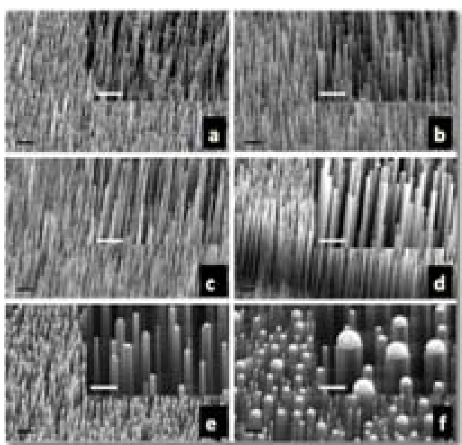


Figure 2.5: SEM images showing how the galvanic displacement method is use to control the size of silicon nanowires - SEM images (with insets of close-up images) of vertically aligned Si nanowire arrays grown from Au clusters deposited on Si (111) substrates. The R parameter of the microemulsion used in the galvanic displacement process is 16 (a), 25 (b), 50 (c), 100 (d), and 200 (e), respectively. Au clusters are deposited from water-based solution in (f). The scale bar is 300 nm, taken from [109].

in the solution. The Au nanoparticles are deposited by immersion of the substrates in a reversed micelle microemulsion that is prepared by mixing a water-based plating solution with n-heptane and a surfactant as it will be further explained in section 3.2.4.

The size of the micelle is known to be a function of the microemulsion parameter R, defined as the ratio of the molar concentrations of water and the surfactant:

$$R = [Water]/[Surfactant] \tag{2.1}$$

The size of the deposited metal clusters in the galvanic displacement process has been found to be determined by the nominal micelle size over a wide range of the microemulsion parameter, R (Figure 2.5) [109]. This fact is employed to control the size of the Au catalyst and, hence, the size of the nanowires synthesized by the VLS method ranging from wires several hundreds of micrometers thick [79] down to nanowires of just a few nanometers in diameter. This large range of sizes is one of the most remarkable features of the VLS mechanism. Using this approach, vertically and laterally aligned nanowire arrays with controlled nanowire size have been demonstrated.

2.2.2 Microfabrication technologies

Silicon microtechnology combines adding layers of a material over a silicon wafer with etching (selectively removing material) precise patterns in these layers or in the underlying substrate, in the iterative sequence needed to fabricate a given device in large numbers per wafer. As shown in Figure 2.6, there is a broad portfolio of fabrication processes, including material deposition, patterning, and etching techniques [110]. The aim of this section is not to describe silicon microtechnology thoroughly, but to briefly explain those microfabrication methods employed in this thesis for the sake of readers non familiar with those technologies.

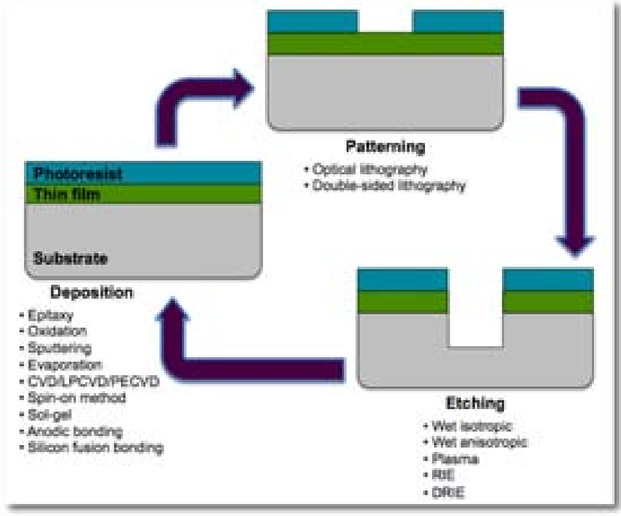


Figure 2.6: Illustration of the basic process flow in micromachining - Layers are deposited, photoresist is lithographically patterned and then used as a mask to etch the underlying materials. The process is repeated until completion of the microstructure, adapted from [110].

2.2.2.1 Deposition techniques

- **Sputter deposition**

  In sputter deposition, a target made of a material to be deposited is physically bombarded by a flux of inert-gas ions (usually argon) in a vacuum chamber at a pressure of 0.1–10 Pa. Atoms or molecules from the target are ejected and deposited onto the substrate. Sputtering is a commonly employed method

by the MEMS community for the low-temperature deposition (<150°C) of thin metal films such as aluminum, titanium, chromium, platinum, palladium, tungsten, Al/Si and Ti/W alloys, amorphous silicon, insulators including glass, and piezoelec-tric ceramics. A thin (5 to 25 nm) adhesion layer, which bonds the underlying material and the metal over it, is often used for inert metals that normally peel off immediately after deposition or during later handling. The most common adhesion layers are Cr, Ti, and Ti/W alloy. The inert metal must be deposited on the adhesion layer without breaking the vacuum, as oxygen in the air would immediately oxidize the adhesion layer, rendering it useless. Thin films of Ti/Pt, Cr/Pt, W/Pt, Ti/Pt/Ti, Ti/W/Pt, Cr/Pt/Cr, Cr/W/Pt, Cr/W/Pt/Cr, Pt, W, Ti/W, TiW, TiW/W, Ta/Pt were deposited by sputter for this thesis with the aim of finding a suitable metal that could withstand the high temperature and aggressive atmosphere conditions of the silicon nanowire growth. The experiments performed are detailed in Appendix A.

- **Chemical-Vapor Deposition**

  Chemical-vapor deposition (CVD) works on the principle of initiating a surface chemical reaction in a controlled atmosphere, resulting in the deposition of a species on a heated substrate. In contrast to sputtering (a high energy process, out-of-equilibrium), CVD is a high-temperature process (near-to-equilibrium), usually performed above 300°C. The field of CVD has grown substantially, driven by the demand within the semiconductor industry for high-quality, thin dielectric and conductive films for multilayer electrical interconnects. The deposition of polysilicon, silicon oxides, and nitrides is a routine within the MEMS industry. Chemical vapor deposition processes are categorized as atmospheric-pressure (referred to as APCVD), low-pressure (LPCVD), or plasma-enhanced (PECVD), which also encompasses high-density plasma (HDP-CVD). APCVD and LPCVD methods operate at rather elevated temperatures (400°-800°C). In PECVD and HDP-CVD, the substrate temperature is typically near 300°C since a plasma is used to deliver additional energy to the reaction.

  In this thesis, APCVD, LPCVD and PECVD depositions were used. As it has been previously described, the APCVD was used for Si nanowire growth. In general, for all the devices fabricated along this work, LPCVD silicon nitride (Si_3N_4) was used as an isolation layer, while PECVD silicon nitride and silicon

oxide (SiO_2) were used as a passivation layer either individually or combined, the purpose of this passivation layer was to selectively grow silicon nanowires only at Si-exposed areas and to prevent exposing the metal contacts of the device inside the CVD furnace in order to avoid irregular nanowire growth as is further explained in section 3.2.4.

Silicon Dioxide was deposited at 380 °C by reacting silane (SiH_4), nitrous oxide (N_2O) and oxygen in a PECVD reactor. Due to the low temperature compared to thermally grown oxide, this is known as low-temperature oxide (LTO). In this thesis, thermal oxide has also been used for electrical isolation (instead of silicon nitride) by exposing the silicon substrate itself (which is therefore partially consumed) to the action of oxidizing agents such as O_2 or H_2O at atmospheric pressure and elevated temperatures (800-1100 °C).

Silicon Nitride was deposited throughout this work by reacting dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) at 800 °C for LPCVD deposition while PECVD deposition was performed at 380 °C by reacting silane (SiH_4), ammonia (NH_3) and N_2 at 650 mtorr. Si_3N_4 is common in the semiconductor industry for the passivation of electronic devices because it forms an excellent protective barrier against the diffusion of water and sodium ions. In microtechnology, LPCVD silicon nitride films are effective as masks for the selective etching of silicon in alkaline solutions, such as potassium hydroxide (KOH) and are also used as a structural material for the fabrication of self-standing thin membranes.

2.2.2.2 Lithography

Lithography plays a significant role in the delineation of accurate and precise patterns in microtechnology. This technique involves three sequential steps: (1) application of photoresist (a photosensitive emulsion layer) on a substrate; (2) optical exposure to print an image of the mask onto the resist; (3) immersion in an aqueous developer solution to dissolve the exposed resist and render visible the latent image.

- **Photolithography**

  A photolithography process uses light to transfer a geometric pattern from a photo mask to a light-sensitive chemical photoresist on the substrate. Afterwords, a series of chemical treatments either engraves the exposure pattern

into the material underneath the photoresist or enables deposition of a new material with the desired pattern. The mask itself consists of a patterned opaque chromium (the most common), emulsion, or iron oxide layer on a transparent fused-quartz or soda-lime glass substrate, all the masks used in this thesis were fabricated on soda-lime glass. A complete microfabrication process normally involves several lithographic operations with different masks, in this work, the maximum amount of masks used in a microfabrication process flow was 4. A positive photoresist is an organic resin material containing a sensitizer. It is spin-coated on the wafer with typical thickness between 0.5 μm and 10 μm. The sensitizer prevents the dissolution of unexposed resist during immersion in the developer solution. Exposure to light in the 200 to 450 nm range (ultraviolet to blue) breaks down the sensitizer, causing exposed regions to immediately dissolve in developer solution (Figure 2.7). The exact opposite process happens in negative resists —exposed areas remain and unexposed areas dissolve in the developer [110].

For this thesis, contact photolithography using an HIPR6512 positive photoresist was employed in the photolithography steps of all the fabricated devices, in this process the mask touches the wafer during optical exposure. The maximum resolution achievable through this method at the IMB-CNM is of approximately 2-3 μm.

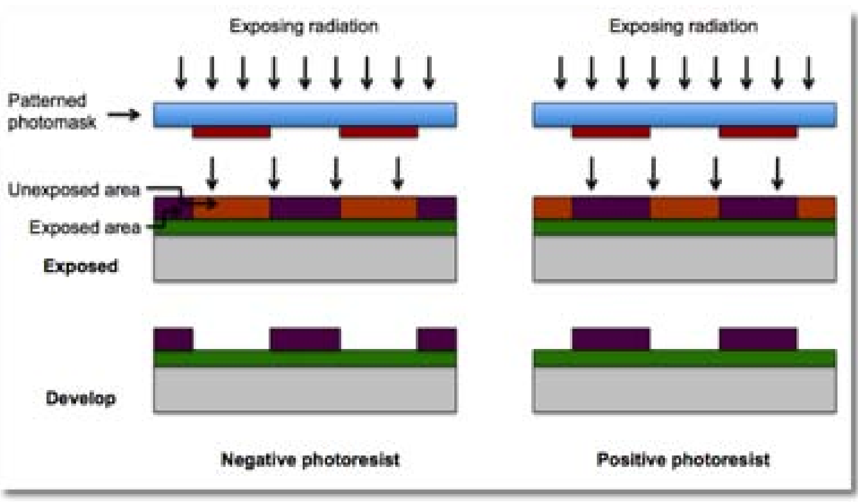


Figure 2.7: Photolithography - Negative and positive photoresist process.

- **Direct Laser Writing**

  This type of lithography is a maskless process where the radiation that is used to expose the photoresist is not projected from, or transmitted through, a photomask. Instead, this method relies on a multi-photon absorption process in a material that is transparent at the wavelength of the laser used for creating the pattern. By scanning and properly modulating the laser, a chemical change (usually polymerization) occurs at the focal spot of the laser and can be controlled to create an arbitrary three-dimensional periodic or non-periodic pattern. Two-photon absorption is utilized to induce a dramatic change in the solubility of the resist for appropriate developers [111]. This method is a very popular form of optical maskless lithography, which offers flexibility, ease of use, and cost effectiveness achieving small features (down to 1 micron) without the use of complex optical systems or photomasks, but it is a rather slow process when the whole surface of a wafer has to be patterned.

  This process was used in this thesis in the fabrication of test structures for the characterization of the thermal properties of silicon nanowires (Appendix E). Due to the nanoscale dimensions of the material, the size of the designed structures has to be small enough in order to be able to measure the response of the nanowires. In the designed devices, a minimum size pattern of 1 μm was used for defining heaters and metal strips on narrow silicon nitride arms, which limited the minimum distance between strips. Several tests were performed in order to achieve a good resolution by laser lithography. Figure 2.8 shows the results obtained by using this technique followed by a lift-off process. The distance between strips was varied from 1 to 3 μm. However, as it can be observed in the images, dimensions were not as accurate as expected. Metal strips got wider during the lithography process, probably due to overexposure of the photoresist employed for this process since this is not a standard resist and exposition parameters are difficult to tune. Moreover, laser lithography is a recently implemented procedure at the clean room facilities of the IMB-CNM and, therefore, this process is not completely optimized. From the results obtained, the distance between strips was determined to be of 2 μm with metal strips of 1 μm-width in desing but with real dimensions of strips 2 μm-width and a distance of about 1 μm between them. This test allowed us to determined not only the patterns that could be achieved through laser lithography but also the limitations of the lift-off process that followed this

lithography step, since both small (∼2 μm) and big (400 μm) dimensions were patterned at the same time with this technique.

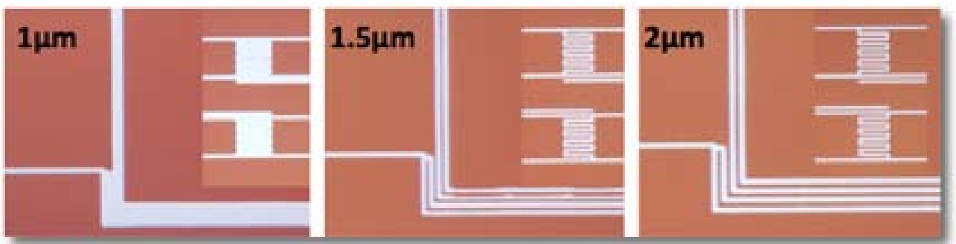


Figure 2.8: Direct laser writing lithography tests - Tests performed to determine the best combination between the width of metal strips and the distance between them with the best resolution achievable through laser lithography for the fabrication of test structures. The images indicate the distance between strips in each case. Only the results for a strip 1μm-width and a variation in distance up to 2 μm are shown.

- **Stepper photolithography**

  A stepper is a photolithography machine used to expose a pattern on a wafer by shining light through a reticle (a glass plate with a pattern etched in chrome, or other photolithographic mask) containing the magnified design of a single-chip. In a stepper, a reduction lens is used to image the pattern of a single chip onto the resist-coated wafer, exposing the wafer one chip at a time and using a precise stage to move the wafer between exposures until the entire wafer is exposed. This repetitive process led to the "step-and-repeat" designation for this tool, "stepper" for short. The key advantage of a stepper relies on the reduction of the minimal pattern size achievable with photolithography due to the reduction of the size of the design from the reticle to the wafer (a design with the size of a mask is transfered to the wafer but with the size of a chip). This reduction makes possible to combine small and large patterns in the same mask without the need of employing more complex techniques like e-beam. Moreover, a finer alignment between different lithography processes can be achieved since the alignment takes place at a chip level instead of at a wafer level making this process less sensitive to the effects caused by the undesired curvatures of the wafer.

  In this thesis, a 5x reduction stepper was used with a reticle size of 6 inches, a usable chip area of 22 by 22 mm and a maximum resolution of 0.35 μm. After

several attempts to fabricate test structures for the thermal characterization of silicon nanowires, a fabrication process using 3 stepper lithography steps was chosen to pattern these microstructures (Appendix E). The highest resolution employed for this purpose was 0.5 μm.

2.2.2.3 Etching

The etching process allows to selectively remove material using imaged photoresist as a masking template. The selected pattern can be either directly etched into the silicon substrate or into a thin film, which may in turn be used as a mask for subsequent etches. For a successful etch, there must be sufficient selectivity (etch-rate ratio) between the material being etched and the masking material. When those etching processes allow adding 2D+1/2 or 3D geometries by obtaining self standing structures or thin-film diaphragms then we speak about micromachining. It usually involves severe lateral undercutting of underneath sacrificial layers (surface micromachining) or the formation of very deep trenches in the substrate (bulk micromachining). Figure 2.9 shows the resulting profile from four different types of etch methods.

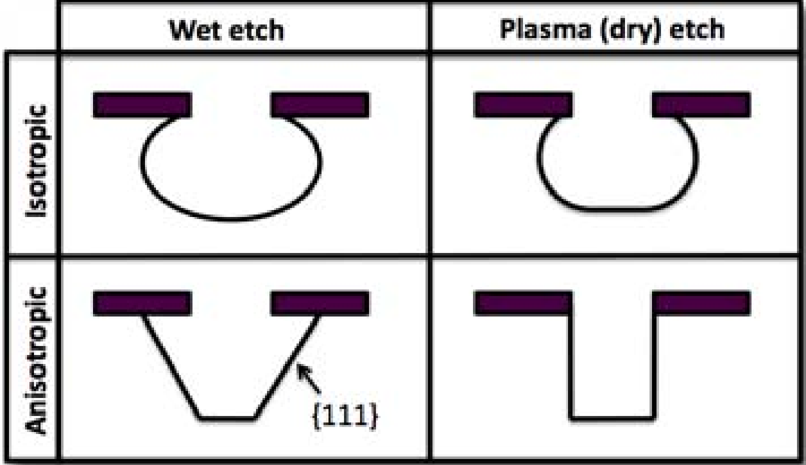


Figure 2.9: Profiles for different etch methods - Schematic illustration of cross-sectional trench profiles resulting from four different types of etch methods.

- **Isotropic wet etching**

  The most common group of silicon isotropic wet etchants is *HNA* (hydrofluoric acid-nitric acid-acetic acid), also known as *iso etch* and *poly etch* because of its use in the early days of the integrated circuit industry as an etchant for polysilicon. It is a mixture of hydrofluoric (HF), nitric (HNO_3), and acetic (CH_3COOH) acids. In the chemical reaction, the nitric acid oxidizes silicon, which is then etched by the hydrofluoric acid.

- **Anisotropic wet etching**

  Anisotropic wet etchants are also known as orientation-dependent etchants (ODEs) because their etch rates depend on the crystallographic direction. There is a large list of anisotropic wet etchants that can be used, however, KOH is by far the most common ODE. Etch rates are typically given in the [100] direction, corresponding to the etch front being the {100} plane. The {110} planes are etched in KOH about twice as rapidly as {100} planes, while {111} planes are etched at a rate about 100 times slower than for {100} planes. LPCVD silicon nitride is an excellent masking material against etching in KOH. Silicon dioxide etches at about 10 nm/min and can be used as a masking layer for very short etches. Photoresist is rapidly etched in hot alkaline solutions and is therefore not suitable for masking these etchants.

  This type of etching was a key process in the development of test structures for the thermal characterization of silicon nanowires. In this structures, narrow silicon nitride arms had to be suspended by etching the silicon device layer of the SOI wafer underneath the nitride layer. The structures were designed with silicon walls oriented in the {111} direction for nanowire growth while the arms were oriented in the {110} planes. In this way, the silicon underneath the nitride arms could be etched faster without affecting the silicon sidewalls where the nanowires were to be grown obtaining in this way free standing silicon structures hold by nitride arms. This procedure is further explained in Appendix E.

- **Plasma etching**

  Plasma (or dry) etching is a key process in the semiconductor industry. It involves the generation of chemically reactive neutrals (e.g., F,Cl), and ions (e.g., ${SF_x}^+$) that are accelerated under the effect of an electric field toward a target substrate. The reactive species (neutrals and ions) are formed by

the collision of molecules in a reactant gas (e.g., SF_6, CF_4, Cl_2, $CClF_3$, NF_3) with a cloud of energetic electrons excited by an RF electric field. When the etch process is purely chemical, powered by the spontaneous reaction of neutrals with silicon, it is colloquially referred to as plasma etching. But if ion bombardment of the silicon surface plays a synergistic role in the chemical etch reaction, the process is then referred to as reactive ion etching (RIE). In RIE, ion (e.g., SF_x^+) motion toward the substrate is nearly vertical, which gives RIE vertical anisotropy.

This process was mainly used in this work to define the structures of the dielectric layers deposited on top of the device layer of the SOI wafers.

- **Deep Reactive Ion Etching (DRIE)**

  DRIE is an etching process capable of vertically define high-aspect-ratio trenches at rates substantially larger than the 0.1 to 0.5 μm/min typical of traditional plasma and RIE etchers by combining cycles of etching and passivation sequentially. The etch part of the cycle, typically lasting about 7 s in a standard process at the IMB-CNM, uses SF_6, which supplies highly reactive fluorine radicals, to etch silicon. The etch step has both vertical and isotropic character, resulting in a slight mask undercut (Figure 2.10). In the passivation step, a fluorocarbon polymer (made of a chain of CF_2 groups similar in composition to Teflon), about 10 nm thick, is plasma-deposited using C_4F_8 as the source gas, this step typically lasts 3 s in a standard process. In the following etch step, the vertically oriented ions (SF_x^+) enhance the effect of fluorine radicals in removing the protective polymer at the bottom of the trench, while the film remains relatively intact along the sidewalls. The repetitive alternation of the etch and passivation steps results in a very directional etch at rates from 1 to over 15 μm/min, depending on the recipe and machine. The degree of scalloping —the sidewall texture due to the isotropic component of the etch— varies with the recipe. For instance, if a small degree of scalloping is desired, i.e. for "nano" conditions, the etching step is changed to a 2 s cycle with a passivation step of 1 s.

  In this thesis, this process was used to etch the device layer of the SOI wafers to define the main structures and to etch the backside of the devices fabricated. Since the profile of the silicon sidewalls of the device layer of the structures had to be perpendicular to the wafer surface in order to grow horizontal nanowires

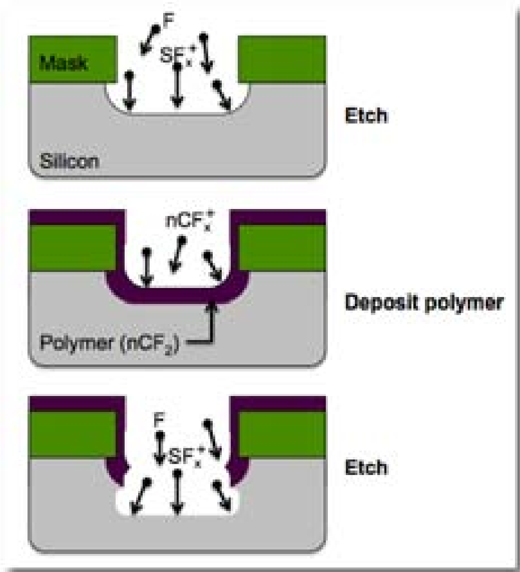


Figure 2.10: Profile of a DRIE trench - The process cycles between an etch step using SF_6 gas and a polymer deposition step using C_4F_8. The polymer protects the sidewalls from etching by the reactive fluorine radicals.

between these trenches, anisotropic dry etching had to be used. Moreover, the devices were designed to open trenches in the <111> orientation (for nanowire growth) and therefore, any wet etching process would had exposed undesired silicon planes yielding to irregular nanowire growth as it will be further explained in section 3.2.2. DRIE was one of the the key processes employed in this work not only to define the device layer but to release all the device structures fabricated. In this matter, it was used to etch the handle wafer of the SOI wafers, which in all cases was about 500 μm thick. As it will be explain in section 3.2.3, SOI wafers with a 2 μm-thick device layer, a 2 μm-thick buried oxide layer and a 500 μm-thick were initially used however, when performing the DRIE process to release the large membrane structures of the devices, the intrinsic stress of the thermal oxide and silicon device layers tended to break the membranes. Therefore, the thicknesses of the SOI wafers were varied until the membranes in the devices were successfully suspended.

2.2.2.4 Lift-off

In semiconductor wafer fabrication, the term "lift-off" refers to the process of creating patterns on the wafer surface through an additive process, as opposed to the more familiar patterning techniques that involve subtractive processes, such as

etching. Lift-off is most commonly employed in patterning metal films for interconnections. In this process a sacrificial material, such as photoresist, is first deposited and patterned on the substrate. The material of interest is then deposited on top and the sacrificial material is subsequently removed, leaving behind only the material deposited directly on the substrate. These processes are useful for patterning unreactive materials and those that cannot be etched without affecting underlying materials on the substrate. In this thesis, the lift-off process was used to pattern the metal layer for electrical contact and to define heaters in the devices. Commonly employed metals for this purpose are Au or Al, which could not be used in our devices due to the low eutectic alloy temperatures that this metals form with silicon. Instead, a Ti/Pt layer was initially chosen as the metal layer, but since Pt can not be patterned using wet etching processes a lift-off process was required for this. Figure 2.11 shows the standard steps of this process.

Moreover, as part of the drawbacks encountered during the compatibility between the fabrication of the devices and the growth of silicon nanowires, several tests were performed in order to improve the lift-off process.

The key for a successful lift-off process is the ability to ensure the existence of a distinct break between the material layer deposited and the sacrificial layer on the substrate. Such separation allows the dissolving liquid to reach and attack the sacrificial layer. When this separation is not enough, the material deposited is not successfully patterned and unwanted parts of the material layer will remain on the wafer or, sometimes, "ears" can be formed, which are made of the material along the sidewall of the sacrificial layer standing upwards from the surface.

In this thesis, the metal "ears" standing upwards represented a problem when silicon nanowires were growth since the passivation layer was not enough to cover them and therefore, the metal was exposed during the nanowire growth altering the process. To solve this issue, different sacrificial layer thicknesses were employed to increase the separation between the metal layer deposited and the substrate. A fabrication process including 5 wafers and different photolithography conditions was performed. Figure 2.12a shows the results obtained by using an annealed 2 μm-thick photoresist with an extra Aluminum layer, whereas Figure 2.12b shows the same results but with a non-annealed photoresist layer. As it can be observed, the best lift-off results were obtained by using a non-annealed 2 μm-thick photoresist combined with a 4500 Å-thick sacrificial Aluminum layer.

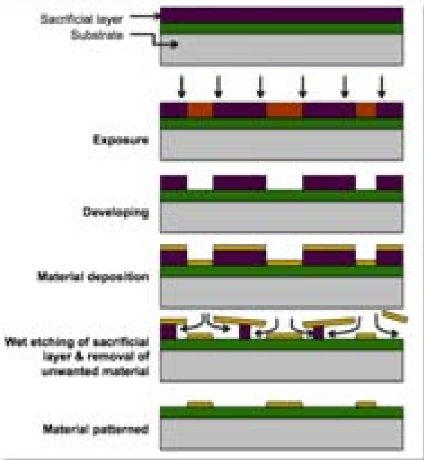


Figure 2.11: Sketch of a lift-off process - The figure shows the lift-off process for the production of thin-films structures using a sacrificial layer. The procedure is used in the semiconductor and microsystem technology, for example to produce metallic interconnections.

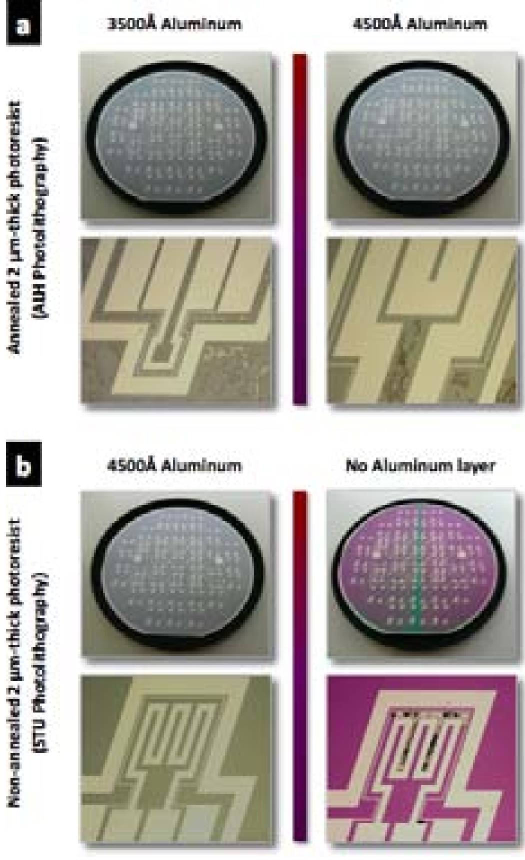


Figure 2.12: Tests performed to improve the lift-off process - (a) Using an annealed 2 μm-thick photoresist and (b) using the same sacrificial layer but non-annealed.

2.3 Structural characterization techniques

2.3.1 Scanning electron microscopy

A scanning electron microscope (SEM) is a type of electron microscope that uses a focused high-energy beam of electrons in a scan pattern to generate a variety of signals at the surface of the solid specimens. Accelerated electrons in a SEM carry significant amounts of kinetic energy, which is dissipated as different signals produced by electron-sample interactions when the incident electrons are decelerated in the solid sample. These signals include secondary electrons (that produce SEM images), backscattered electrons, diffracted backscattered electrons (that are used to determine crystal structures and orientations of minerals), photons (characteristic X-rays that are used for elemental analysis and continuum X-rays), visible light (cathodoluminescence–CL), and heat. Secondary electrons and backscattered electrons are commonly used for imaging samples: secondary electrons are most valuable for showing morphology and topography on samples and backscattered electrons are most valuable for illustrating contrasts in composition in multiphase samples (i.e. for rapid phase discrimination).

SEM images, using both backscattered and secondary electrons, were taken throughout this thesis to observe the results of different processes, i.e. silicon nanowire growth or microstructures fabrication, and to follow the different topography of the metal and passivation layers of the devices after silicon nanowire growth.

2.3.2 Energy-dispersive X-ray spectroscopy

After several issues encountered during the development of this work regarding the growth of silicon nanowires, as it will be explained is Appendix C, energy-dispersive X-ray spectroscopy (EDX) was used to qualitatively and semi-quantitatively analyze the chemical composition of samples to determine possible contaminations before and after nanowire growth. This technique relies in the analysis of X-rays emitted by a material in response to being hit with charged particles. Its characterization capabilities are due in large part to the fundamental principle that each element has a unique atomic structure allowing X-rays that are characteristic of an element atomic structure to be spectrally identified uniquely from one another. This SEM analysis is considered to be “non-destructive”; that is, X-rays generated by electron interactions do not lead to volume loss of the sample, so it is possible to analyze the same materials repeatedly.

2.3.3 Transmission electron microscopy

In a Transmission Electron Microscope (TEM) a high-energy electron beam is transmitted through an ultra-thin sample, interacting with the sample as it passes through and forming an image from this interaction. The image is then magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor such as a CCD camera. In a TEM, the associated wavelength of electrons accelerated at high voltage (100-1000 kV) to a velocity approaching the speed of light is five orders of magnitude smaller than the light wavelength (0.04-0.008 Å). However, the magnetic lens aberrations of the microscope limit the convergence angle of the electron beam and reduce the TEM resolution to the Å order. This resolution enables material imaging and structure determination at the atomic level, allowing image resolutions that are on the order of 1 - 2 Å. Compared to SEM, TEM has better spatial resolution and is capable of additional analytical measurements (crystallographic phase, crystallographic orientation, etc.) but requires significantly more sample preparation since very thin samples (around 100 nm-thick or less) are required.

In this thesis, a TEM was used to observe the crystallographic orientation of silicon nanowires in order to ensure crystallographic growth in the <111> orientation.

2.3.4 Micro X-ray diffraction

Micro X-ray diffraction (μXRD) allows to reveal the crystalline structure of small samples or areas. Like conventional XRD instrumentation, it is based on the elastic scattering of X-rays from the electron clouds of the individual atoms in the system to obtain information about the structure of crystalline materials. μXRD uses X-ray optics to focus the excitation beam to a small spot (tens of micrometers) on the sample surface so that small features on the sample can be analyzed.

The μXRD technique was used in this work to analyze the composition of samples where inhomogeneous nanowire growth was observed. Initially, this inhomogeneity was regarded as contamination of samples or metal exposition before the nanowire growth process. However, by using the EDX technique combined with μXRD and after several attempts to solve these issues, which are further described in Appendix C, this possibility was rejected.

2.4 Thermal & electrical characterization: methodology & experimental set-ups

Once device fabrication is completed, it is necessary to experimentally evaluate the properties of the functional materials employed, in this case silicon nanowire arrays, as well as the performance of the fabricated devices. In this section, the different methods and experimental set-ups employed for the characterization of the microstructures described in Chapters 3 and 4 will be detailed. Current, voltage and power generated by the microstructures were measured when subjected to temperature differences generated by a natural heat source or by employing an integrated heater.

Figure 2.13 shows the process flow followed after device fabrication at a wafer level. First of all, wafers were cut into chips to grow silicon nanowires (as it will explained in section 3.2.3). Djeevices were then inspected by SEM imaging followed by the removal of remaining oxide layers. At this point, a preliminary characterization was performed through a probing system and devices showing both good performance and no fabrication defects were encapsulated and wire bonded. To electrically measure the temperature in the device, the metal interconnections and heaters patterned on it were employed as thermometers in some of the experiments performed. For this purpose, the temperature coefficient of resistance (TCR) of the metals was measured prior to the characterization of the devices. The thermal gradients to which the devices were subjected for its characterization were generated by two different methods: i) by means of an integrated heater (*testing operation mode*); ii) by means of a natural heat source simulated through an external hot plate (*harvesting operation mode*). Additionally, the temperature distribution on the surface of devices was also measured by means of the thermoreflectance imaging technique when possible.

Due to the nanoscale dimensions of the thermoelectric materials employed in this work (silicon nanowires) and the conditions under which the devices were tested, e.g. high temperatures and vacuum, typical characterization techniques and methods presented several singularities that made them difficult to apply.

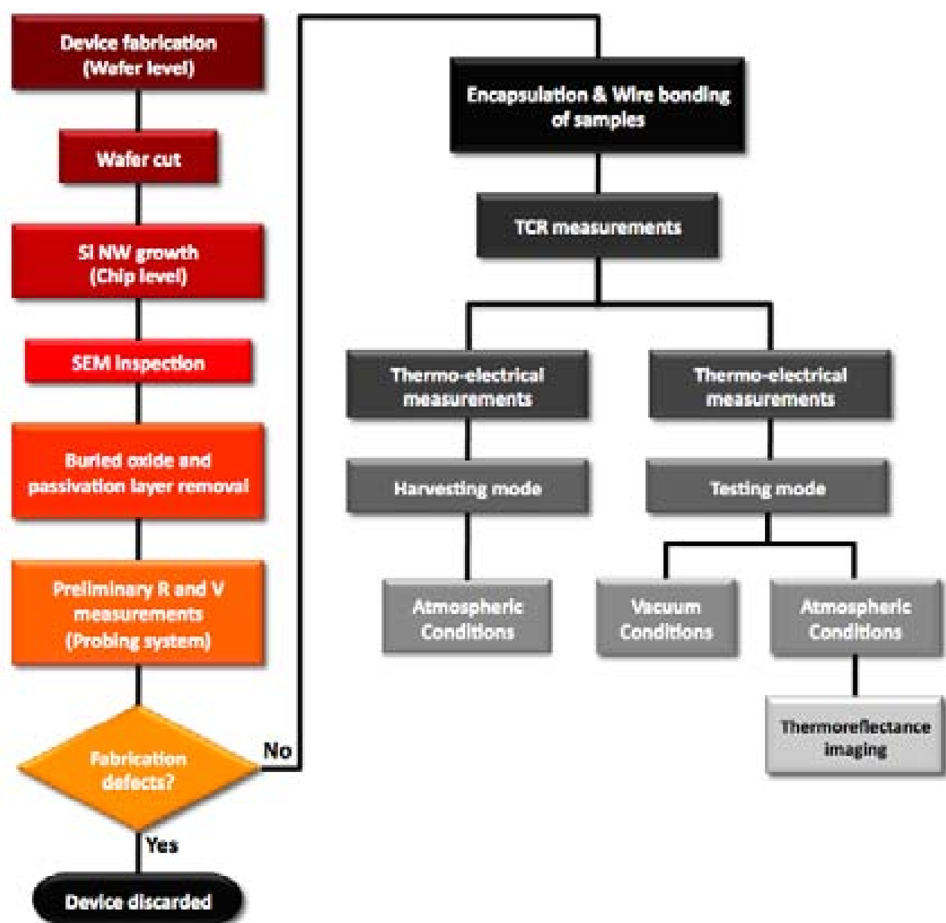


Figure 2.13: Process flow followed for the characterization of devices - Schematic representation of the process followed step-by-step from device fabrication to the final characterization of devices.

2.4.1 Preliminary characterization: Electrical conductivity & Seebeck voltage experimental set-up

This section is aimed to briefly describe the preliminary measurements, i.e. before encapsulation, carried out in order to estimate the performance of the fabricated devices and to determine whether these devices had fabrication defects or not. For these preliminary characterization, as well as for the rest of the characterization process, two-probe and four-probe sensing methods were combined.

- ***Two & Four-point probe electrical characterization***

  The *four-point probe* configuration is an electrical measuring technique commonly used to measure the resistivity of semiconductors. It uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements than traditional two-point probe sensing by removing the contribution of the contacts. The two-probe method is easier to implement, because only two contacts are needed, but parasitic impedances are convoluted into the measurement [112]. If a two-point probe arrangement as the one shown in Figure 2.14c is considered, each contact will serve as a current *and* as a voltage probe and the total resistance of the device under test (DUT) will be given by

$$R_T = \frac{V}{I} = 2R_W + 2R_C + R_{DUT} \tag{2.2}$$

  where R_W is the wire or probe resistance, R_C is the contact resistance at the interface between the probe tip and the semiconductor, and R_{DUT} the resistance of the device under test. From the equation 2.2 we can see that it is clearly impossible to determine R_{DUT} with this measurement configuration. A possible solution is the four-probe arrangement as shown in Figure 2.14b. Two probes carry the current and the other two probes sense the voltage. Each probe has a probe resistance R_P, a probe contact resistance R_{CP} at the interface between the probe tip and the semiconductor and a spreading resistance R_{SP} associated with it which is generated when current flows from the small tip into the semiconductor and spreads out in the semiconductor (Figure 2.14a). However, these parasitic resistances can be neglected for the two voltage probes because the voltage is measured with a high impedance voltmeter, which draws very little current. Thus the voltage drops across these

parasitic resistances are negligible and the voltage reading from the voltmeter is approximately equal to the voltage drop across the semiconductor sheet resistance.

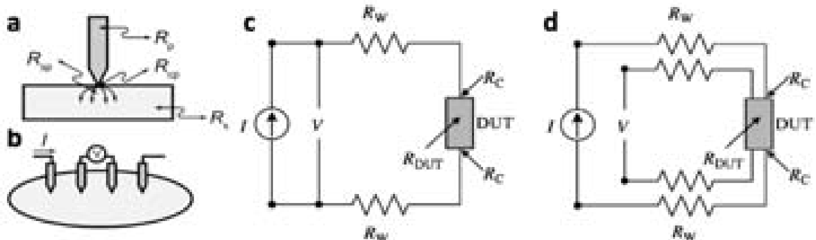


Figure 2.14: Two-probe and four-probe resistance measurement arrangements - (a) Several resistances need to be considered. (b) Four-probe measurement configuration. (c) Two-probe and (d) four-probe equivalent circuits.

The preliminary characterization performed to the devices consisted on resistance and voltage measurements at room temperature under atmospheric conditions. These measurements were made, under a 4-probe configuration, with a HP4155 semiconductor parameter analyzer by performing automated I-V measurements applying a DC current sweep to integrated heaters (*testing mode*) and measuring the resistance and voltage at the ends of the silicon nanowire arrays. Samples were probe through a Karlsuss PA200 semiautomatic probe system (Figure 2.15). These measurements were performed to verify a good ohmic contact between the silicon nanowire arrays and the opposing (111) silicon sidewalls and to observe the thermogenerated voltage response of the devices.

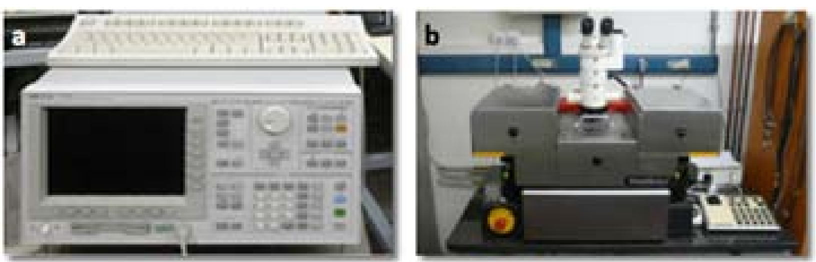


Figure 2.15: Electrical set-up used to performed four-probe measurements - (a) Semiconductor analyzer equipment used for resistance and voltage measurements. (b) System used to probe samples.

2.4.2 Encapsulation & wire bonding of devices

Prior to the characterization of the devices and after selecting samples without fabrication defects, i.e. good nanowire growth and contact, samples were encapsulated and wire-bonded. These two processes were key steps in the development of the different measurements.

Encapsulation was performed using a ceramic quad flat package (CQFP) from Kyocera (drawing number PB-F90462-A). Packages had to be very thin since the chamber used for characterization allowed only about 2.5 mm-thick packages. These packages contained 48 flat leads and were ordered in this way since high-temperature measurements (up to 350 °C) needed to be performed and therefore, no solder could be used to contact the package or its leads (commonly used alloys melt between 180 and 190°C). Instead, small mechanical double clamps were used to contact the package leads and wires. Devices were bonded to the Kyocera packages using a thermal conductive silver paste.

Samples were wire-bonded using an Ultrasonic Wire bonder 4526 from Kuliche & Soffa and employing a 25 μm-thick aluminum wire. This procedure required an accurate optimization since it was difficult to find a wire bonder equipment that, combined with the precise setting parameters, worked for our samples. Four wire bonders under different conditions were tested for this purpose. Moreover, since the silicon nanowire growth is an aggressive procedure, obtaining samples with the adequate metal conditions was a challenge not only at a fabrication level but also for wire bonding purposes, i.e. metal in the samples got detached and the roughness of the metal layer complicated the wire bonding process.

Moreover, for TCR measurements, cables had to be adapted as well. In this procedure, samples, packages and cables were exposed inside a furnace with temperatures ranging from room temperature up to 250°C for a time period of about 1.5 days. Apart from avoiding any kind of soldering and using mechanical clamps, cables had to be adapted and isolated using Kapton® film to avoid any short circuits since conventional plastic covers melted at this temperature.

2.4.3 Electrical characterization of devices

In this work, electrical characterization of devices consisted on monitoring the intrinsic resistance of the silicon nanowire arrays, the Seebeck voltage generated by this material and the I-V characterization and power curves for different experiment conditions under which the devices were tested. The resistance of the heaters patterned on the devices was also monitored when employed.

2.4.3.1 Contact resistance

As mentioned in the previous chapter, the contact resistance is a key parameter for the final performance of thermoelectric devices. In this work, the contact resistance between the metal layer employed and the silicon device layer was measured using a *transmission line model* (TLM) configuration.

The TLM method allows to accurately measure the contact resistance. These type of structures consists in depositing a metal grid pattern of unequal spacing L_i between the contacts, which leads to a scaled planar resistor structure. Each resistor changes only by its distance L_i between two adjacent contacts, as shown in Figure 2.16a and it can be expressed by

$$R_i = \frac{\rho_s L_i}{W} + 2R_c \tag{2.3}$$

Then, by plotting the measured resistances as a function of the contacts spacing L_i, and according to Eq. 2.3, the layer sheet resistivity ρ_s and the contact resistance R_c can be deduced from the slope and from the intercept at L_i=0 respectively, as shown in Figure 2.16b:

$$Slope = \frac{\rho_s}{W}; \quad R_i(intercept) = 2R_c \tag{2.4}$$

2.4.3.2 Temperature Coefficient of Resistance (TCR)

The TCR of a material indicates how much its electrical resistance variates as its temperature changes. It is usually expressed in ppm/°C (parts per million per degree Centigrade) units. The TCR may be either positive (the resistance increases with temperature) or negative (the resistance decreases with temperature). The TCR is generally not constant with temperature and may even change polarities over the operating temperature range of the material.

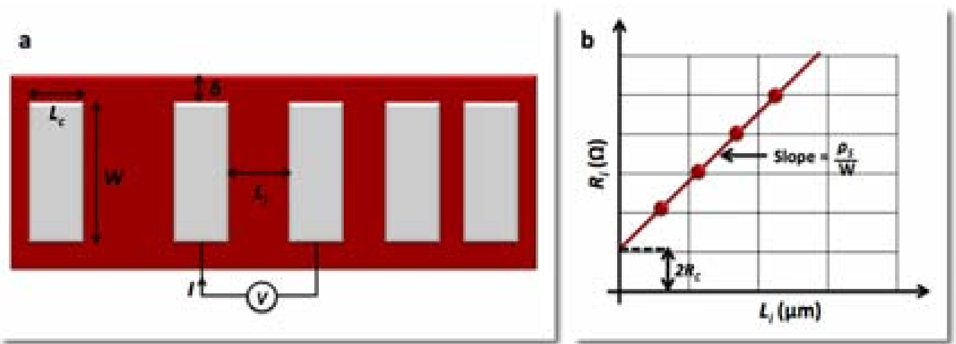


Figure 2.16: Transmission line model test structure - (a) Structure configuration and (b) characterization of the contact resistance using a TLM test structure.

In this thesis, several experiments were performed in order to determine the temperature coefficient of resistance (TCR) of the metals used. Samples were prepared in the four-point measurement configuration and placed into a suitable oven together with a thermocouple meter. The thermocouple was used for temperature measurement in order to achieve accurate measurements and was placed as close to the sample as possible and held in place but without affecting the sample so the system could respond to temperature changes inside the furnace. Figure 2.17 shows an image of the set-up implemented.

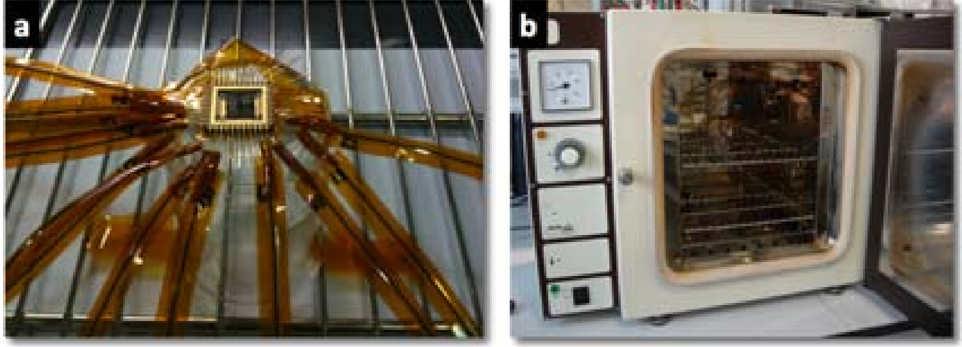


Figure 2.17: Set-up used to performed TCR measurements - TCR measurements were performed using an oven to heat the sample up to 250°C and letting it cool down while measuring the changes in the resistance of the materials under test. (a) Shows the sample set-up and (b) the oven were it was heated.

Once samples were mounted inside the oven, the oven was switched on and the temperature increased to a maximum temperature value of 250°C. A maximum of four resistances were measured at the same time which, together with the corresponding temperature, were recorded until the maximum temperature was reached. After reaching this temperature the power to the oven was switched off and the same measurements were done while letting the oven cool down. Since this process happens much more slowly than heating, the thermal equilibrium inside of the oven between the thermocouple and the actual temperature in the sample is better and therefore provides sufficiently accurate results. The data was recorded using a multimeter data acquisition unit (Keithley® 2700) and a system scanning thermometer (Keithley® 740) connected to a personal computer. Data were collected using an automated program (Figure 2.18) developed with LabVIEW 10.0 software (National Instruments).

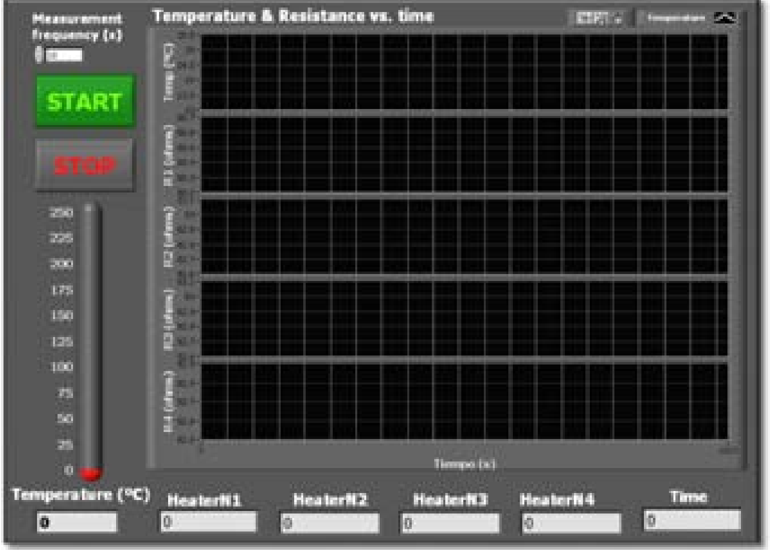


Figure 2.18: Screen shot of the program developed for TCR measurements - Main window of the developed program using LabVIEW software.

In order to evaluate the obtained results, it was first verified that the resistance vs. temperature graph was nearly a straight line. The TCR was then obtained from the following formula from the line of best (least squares) fit to the data.

$$TCR = \frac{1}{R_0} \cdot \frac{\Delta R}{\Delta T} \tag{2.5}$$

Figure 2.19: Linkam vacuum stage - This small chamber allows to heat and cool samples in a temperature range from -196°C up to 350°C and to perform vacuum testing at the same time.

were R_0 is the resistance of the material at room temperature, ΔR the difference between the resistance at the maximum temperature and at room temperature and ΔT the difference between these temperature values.

2.4.3.3 I-V & power characteristic curves

In order to characterize the performance of the devices fabricated throughout this thesis, different set-ups were used depending on the characterization mode employed (*harvesting or testing*) and the conditions under which the devices were tested, i.e. atmospheric conditions or vacuum.

For this purpose, an Examina vacuum stage (THMS350EV) with 8 electrical connectors was acquired from Linkam Scientific Instruments Ltd. (Figure 2.19). This small chamber allows to heat or cool samples through a small stage (sample area of 22mm of diameter) with a temperature control range from -196°C up to 350°C at a vacuum of 10^{-3}mbar using a simple E2M 1.5L rotary vacuum pump. With this chamber, samples can be heated using a TMS94V temperature controller that can be programmed through the RS232 serial interface to heat the chamber stage. Moreover, to cool samples from ambient down to -196°C a LNP95 liquid nitrogen cooling system is included, however, this feature was not used in this thesis.

- ***Harvesting mode***

  In this characterization mode, the temperature gradient built up in the microstructures is produced by the temperature difference between an external hot-plate in contact with the base of the microdevice and a membrane thermally isolated from this base. For this characterization mode, samples were mounted on the thermal chuck of the Linkam chamber –connected to a temperature controller– using an Omegatherm® "201" high temperature and high thermal conductivity paste.

  In order to measure the I-V and power characteristic curves, a multimeter data acquisition unit (Keithley® 2700) and a source meter unit (Keithley® 2400) were connected to a personal computer together with the temperature controller of the chamber (Figure 2.20). Data were collected through an automated program developed with LabVIEW 10.0 software. The temperature controller was used to fix the temperature of the hot-plate stage of the chamber. Initially, the minimum and maximum temperatures, the heating rate, the holding time at each temperature and the temperature step were set through the interface window of the developed program (Figure 2.21), which included also the option to make the temperature ramp to go up or down.

  The Seebeck voltage, the device resistance and the I-V curves were measured at each temperature value set in the hot-plate. The Seebeck voltage signal and the resistance of the device were first measured using a multimeter unit. For current-voltage analysis, the I-V characteristic curves were measured by using a source meter unit as a dummy load, i.e. as a current sink. The I-V measurements started at I = 0 A, the dummy load was then increased stepwise and controlled by the source meter stopping when the maximum current value that could be delivered by the device was reached –this maximum value was obtained from the open circuit voltage value and the resistance of the device. This procedure was performed for each temperature set point, i.e. the Seebeck voltage, the device resistance and its I-V curve were measured at the minimum temperature set, the temperature was then increased a "temperature step" value and measurements were performed again after the "holding time" had passed, which allowed the system to stabilized at the set temperature before performing any measurement. The power curves were computed from this data for each temperature value.

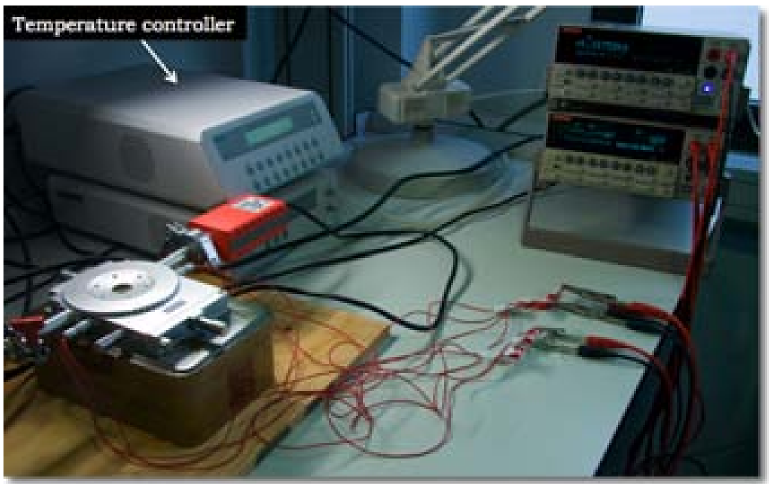


Figure 2.20: Set-up used for the harvesting characterization mode - I-V curves and power curves were measured using a multimeter, source meter unit and a temperature controller to fix the temperature in the hot-plate stage of the Linkam chamber.

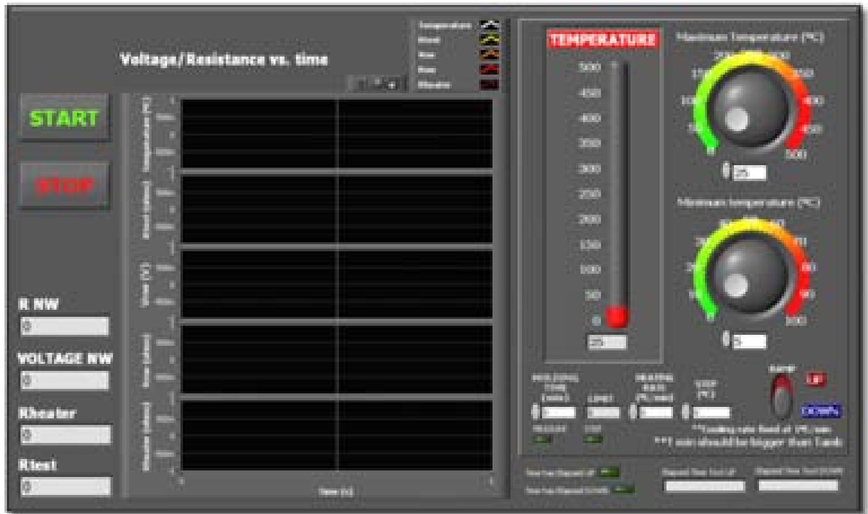


Figure 2.21: Screen shot of the program developed for I-V measurements for the *harvesting mode* - Interface of the program developed using LabVIEW software.

- ***Testing mode***

  In this characterization mode, the temperature gradient built up in the microstructures is produced by means of heaters integrated in the microdevices. For this characterization mode, samples were mounted in the Linkam chamber since the samples were already wire bonded and the chamber made easier the characterization allowing 8 electrical contacts at the same time avoiding the need of probing. On this mode, samples were glued to the chamber stage with thermal paste using the hot-plate of the stage as a heat-sink while monitoring the temperature increment at the base of the device with the temperature controller (hot-plate temperature).

  A multimeter and two source meter units connected to a PC together with a program developed in LabVIEW (Figure 2.22) for automated measurements were used. In this case, one of the two source meter units was used to apply an specific DC current to the heater to achieve a certain temperature given its TCR value while the other unit was employed for measuring the I-V characteristic curves of the device, which consisted of 20 points. Meanwhile, the multimeter recorded the Seebeck voltage and resistance of the device at each temperature step. In summary, the current-voltage analysis and the Seebeck voltage and resistance measurements were performed in the same way as the *harvesting mode* but under different operation conditions, i.e. in the *testing mode* the temperature gradient across the devices was increased by exciting the heater with the source meter unit controlled by the PC instead of using the Linkam hot plate as it was the case for the *harvesting mode*.

- ***Vacuum conditions***

  Both *harvesting* and *testing* measurements were performed in atmospheric conditions, but the *testing mode* was also carried out under vacuum conditions. For the measurements performed under atmospheric conditions, the Linkam chamber was used with the lid on (measurements without the lid were also performed giving the same results but with more noise). The vacuum mode was employed in the *testing mode* to achieve higher thermal gradients avoiding heat loses by convection. For this purpose, samples were placed inside the Linkam chamber, which was then connected to a rotary vacuum pump. The vacuum level was monitored using an active pirani gauge with a gauge-controller lead connected to the PC and controlled through the software

provided with the vacuum system. After about 1.5 hours, once a maximum vacuum level of 10^{-3} mbar was achieved, the characterization of the devices was performed as previously mentioned. Figure 2.23 shows the system set-up employed for this mode.

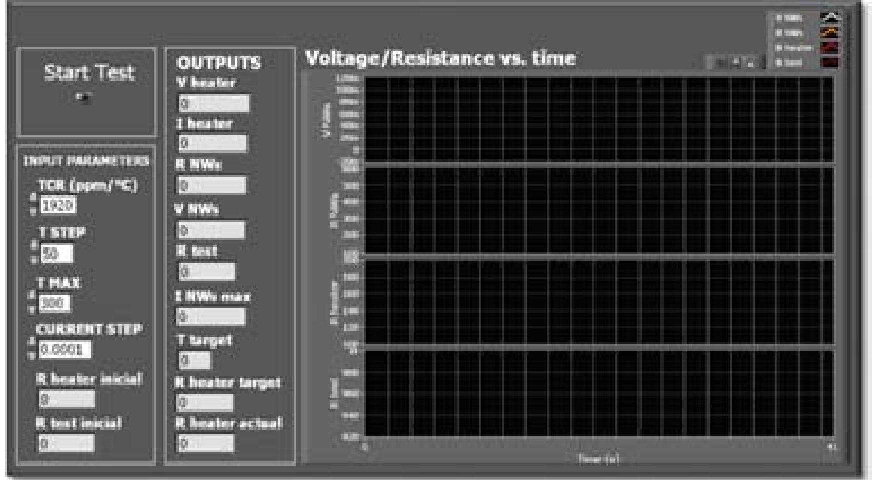


Figure 2.22: Program developed for I-V measurements under a *testing mode* - The program developed using LabVIEW software served to control a multimeter and two source meter units connected to a PC for automated measuremnts.

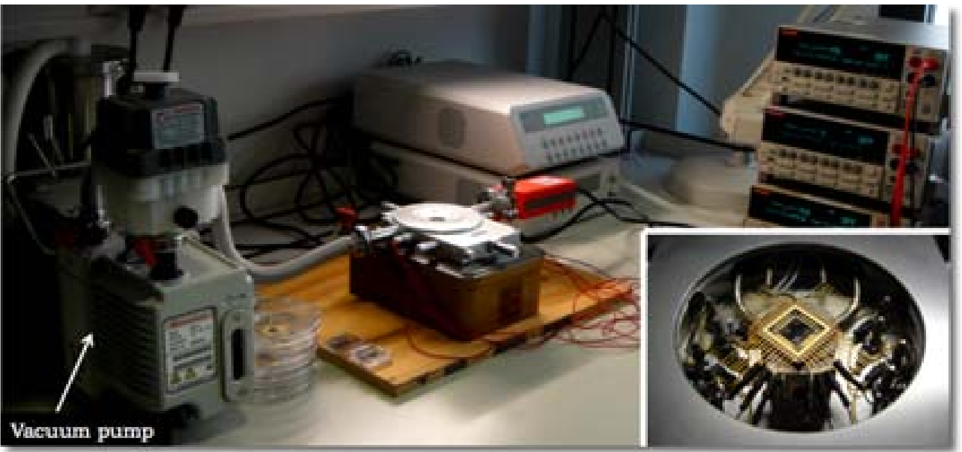


Figure 2.23: Set-up used for vacuum measurements - A rotatory vacuum pump with an active pirani gauge allowed to achieve vacuum levels of 10^{-3}mbar.

2.4.4 Thermal characterization of devices

In this thesis, two methods were used to determine the thermal properties of silicon nanowires when used as thermoelectric material in a power microgenerator. The first one was a differential approach to calculate the thermal conductivity of silicon nanowires by comparing the thermal losses in devices with and without nanowires. The second method consisted in an optical characterization using the thermoreflectance imaging technique to measure the thermal gradients in the surface of the devices that were attained when operated under *testing mode*

2.4.4.1 Thermal conductivity of silicon nanowires

In order to obtain an estimation of the thermal conductivity of silicon nanowires, a differential approximation was employed. This method was performed under the *testing mode*, which means that the heater was used to generate a ΔT in the device.

As previously explained, once devices were fabricated, silicon nanowires were grown in the microstructures. If two devices are analyzed: one with nanowires (A) and one without them (B), the presence of nanowires in the device A makes neccesary to dissipate more power with the heater to achieve a certain temperature difference than in device B. This can be proved by comparing how the temperature (through the resistance of the heater) evolves with the dissipated power in both devices (Figure 2.24a). For this purpose, the TCR of the materials is first measured as described in section 2.4.3.2 and the values obtained are used to estimate the temperature in the device.

If the power dissipated is plotted as a function of the temperature difference (Figure 2.24b), it can be observed –as expected– that the device with silicon nanowires needs a higher power to reach a given temperature difference value because of the presence of the additional thermal losses trough the silicon nanowires ensemble.

To quantitatively estimate the thermal conductivity of silicon nanowires, the increment of power needed to achieve a certain temperature difference in the microstructure with nanowires was calculated. This increment is defined as the thermal conductance (G) of the material. For this, the power dissipated to achieve a certain temperature difference in both devices is plotted and, adjusting the curves to their polynomial fits, the power increment needed for each ΔT value is defined as the difference of these two polynomial fits (Figure 2.24b).

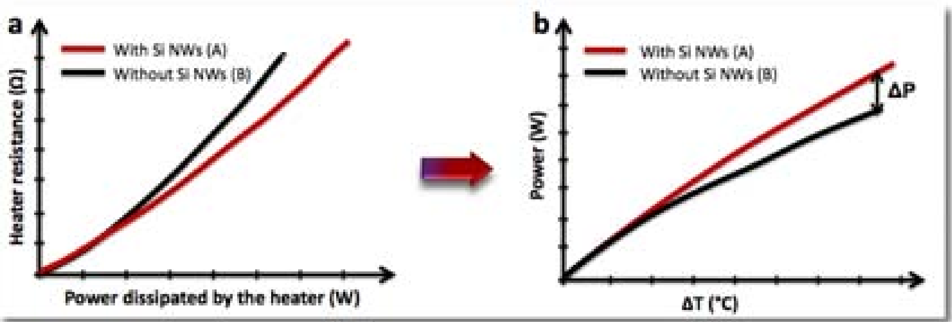


Figure 2.24: Method employed to estimate the thermal conductivity of silicon nanowires - In this differential method two devices are employed, one where silicon nanowires have been grown (A) and one without nanowires (B). (a) The graph shows the evolution of the resistance of the heater as a function of the dissipated power in the two different devices (A and B). (b) Dissipated power in the isolated suspended platform as a function of the temperature difference for the two cases.

The thermal conductivity κ of the equivalent material can be estimated from the thermal conductance by considering the geometry of the trench (longitude and equivalent area). Since the thermal conductance is given by

$$G = \frac{\kappa A}{L} \tag{2.6}$$

The thermal conductivity κ will be given by GL/A. Therefore, the κ of Si NWs can be estimated.

2.4.4.2 Thermoreflectance imaging tecnique

Optical characterization of thermoelectric devices can be useful to determine how the devices behave thermally in the micrometer-scale regime due to the spatial resolution that can be achieved using optical techniques. The spatial resolution achieved optically is far superior to what can be achieved by physical probing of the devices with the exception of scanning thermal microscopy (SThM), which uses an AFM with a thermocouple or a Pt termistor tip achieving a spatial resolution of about 50 nm. The most popular method of thermal imaging is based on the use of an infrared (IR) sensitive camera. However, the spatial resolution of the IR image is given by the diffraction limit of the wavelength used with the most sensitive IR cameras working at the 3 micron wavelength [113].

Thermoreflectance microscopy is an imaging technique frequently applied to measure the surface temperature distribution of active semiconductor devices with sub-micron spatial (∼200 nm) and good temperature (∼0.2°C) resolutions. As it has been previously mentioned, this technique was learned as part of a research stay at the University of California, Santa Cruz (UCSC) in the QEG group and it was used in this thesis to measure the surface temperature of devices in order to evaluate the thermal conductivity of silicon nanowire arrays.

Thermoreflectance thermal imaging relies on the linear change of the reflection coefficient of any material with temperature. This technique utilizes the finite temperature dependence of the surface reflectivity of materials to determine the surface temperature. By measuring the intensity change of illumination reflected from the surface due to a temperature change, a thermal image can be obtained. To capture the thermoreflectance signal with reasonable signal-to-noise ratio (SNR), the device under test is thermally cycled at a known frequency and a lock-in technique is used. Images are detected by a special high frame rate CCD camera. Figure 2.25 is a diagram of a typical thermoreflectance experiment found in the laboratory. The sample to be studied is typically mounted on a *xyz* translation stage for positioning and focusing on the region of interest. Because the reflection characteristics of a material are wavelength dependent, the spectrum of the illumination source is chosen to maximize the experimental thermoreflectance coefficient (C_{th}) as well as to minimize the total reflectivity provided that sufficient intensity of reflected illumination at steady state is achieved.

The thermoreflectance coefficient describes the normalized change in the reflection coefficient with temperature, being on the order of 10^{-4} - 10^{-5} per degree Kelvin for most materials in the visible spectrum. This coefficient is wavelength, material, and sometimes surface texture dependent, and in-situ calibration is necessary. Calibration of the C_{th} is accomplished in an experimental arrangement that is similar to the actual thermoreflectance temperature measurement experiment with the difference that the temperature of the device whose surface requires calibration is modulated externally and therefore, since the device under study is not excited it remains as a passive element. In addition, an independent device to monitor temperature, such as a microthermocouple, is placed on the surface of the device that is being calibrated.

In thermoreflectance experiments, the ΔT across the thermoelectric device is modulated using a sinusoidal voltage source. In this work, this sinusoidal voltage

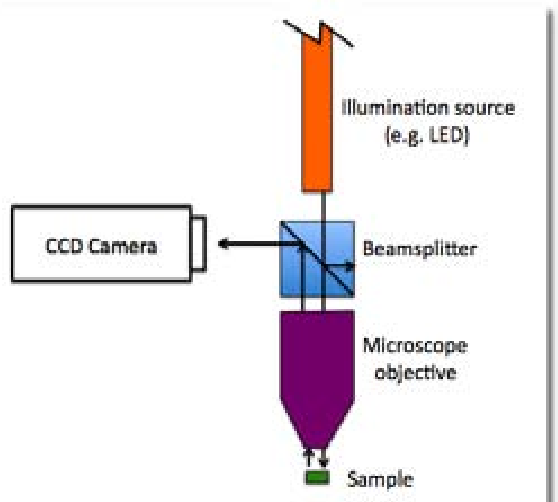


Figure 2.25: Diagram of a typical laboratory thermoreflectance experiment - The thermoreectance imaging technique is used to observe the heat transfer distribution along a device. The images are used to determine the temperature difference achieved across the sample. Measurements are performed using an optical microscope and a light-emitting diode (LED) as the illumination source. A charged-couple device (CCD) camera is used to obtain the two-dimensional thermal images, adapted from [60].

was applied to small thermoelectric devices for external temperature modulation in the case of C_{th} calibration or to the heater pattern on the suspended platform of the devices in the case of thermoreflectance measurement. Since the heater was used for ΔT modulation across the devices, this technique was used only under the *testing mode*. Moreover, the external modulation voltage is chosen to be sinusoidal to reduce the demands on the frequency response of the modulation temperature, as opposed to square-wave modulation that requires fast temperature rise and fall times.

For calibration measurements, the modulation frequency is chosen as the maximum value that permits the signal output from the temperature sensing thermocouple placed on the surface of the sample to be identical to the voltage waveform at the input of the thermoelectric device used for external modulation. This comparison can simply be made on an oscilloscope. The thermoreflectance signal from the surface of the externally modulated sample and the ΔT measured using the calibration thermocouple are recorded simultaneously. The measurement time should permit sufficient averaging for good SNR in the thermoreflectance signal. Thermoreflectance imaging of the devices is performed very similar to the calibration experiment but without modulating the external thermoelectric stage and instead directly modulating the device under study.

The thermoreflectance imaging technique can be used to capture steady state thermal signals but can be also adapted to provide information about the thermal

transient response with a millisecond and microsecond time resolution. The transient technique relies on the precise adjustment of the phase between the pulsed thermal excitation of the device and the illumination pulse used to measure the thermoreflectance change in the device [114]. Since fast CCD cameras are limited to ~500Hz sampling, in the transient technique, the shutter of the camera is leaved always open and only the excitation signal and the illumination source are triggered. In contrast to the steady state technique, where the illumination source is always on and the camera and excitation signals are triggered. Both the steady state and the transient techniques were employed at UCSC during the research stay at the QEG group. During this period, these techniques were learned by helping the group through different projects which mainly comprised the analysis of superlattice samples. Figure 2.26 shows a block diagram of the thermal imaging system employed at UCSC. This set-up consists of a CCD Microscopy head, which includes the microscope (1), the CCD camera (2) and the LED (3). A function generator (4) is used for biasing the samples and, in the case of the transient imaging system, a high speed signal generator (5) and a transient imaging module (6) are added. Figure 2.27 shows the set-up of the system.

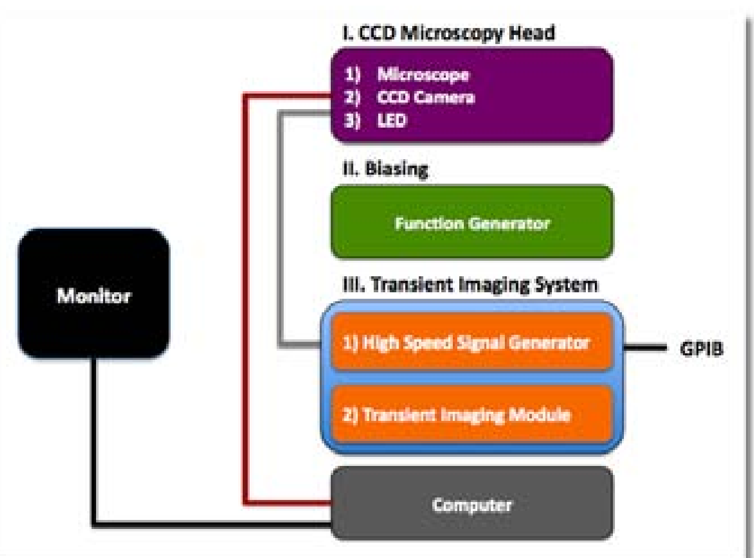


Figure 2.26: Block diagram of Thermal Imaging Analyzer - The diagram shows the parts comprised in a thermal imaging system. A steady state system includes blocks I and II while a transient response system includes all shown blocks.

Although the research stay at UCSC served as a first contact with the QEG and to learn thermal characterization techniques, measurements with the devices fabricated in this thesis were barely performed due to several issues encountered along the fabrication process. Nevertheless, despite these issues, some results were obtained and published [115]. As a further collaboration, and once the device fabrication issues were overcome, a short stay at the QEG group helped to observe the results that could be achieved with an improved thermal imaging system developed by the *Microsanj* startup founded by the QEG group. The new system included the ThermoVIEW software that eases the acquisition and analysis of the thermal images. Figure 2.28 shows the system employed. Finally, as a result from these collaborations, a steady state system (Figure 2.29) was acquired from *Microsanj* by the IMB-CNM. This system helped to characterize not only the devices fabricated throughout this thesis, but to characterize some other devices developed at the working group, e.g. thermopiles, IR emitters, etc.

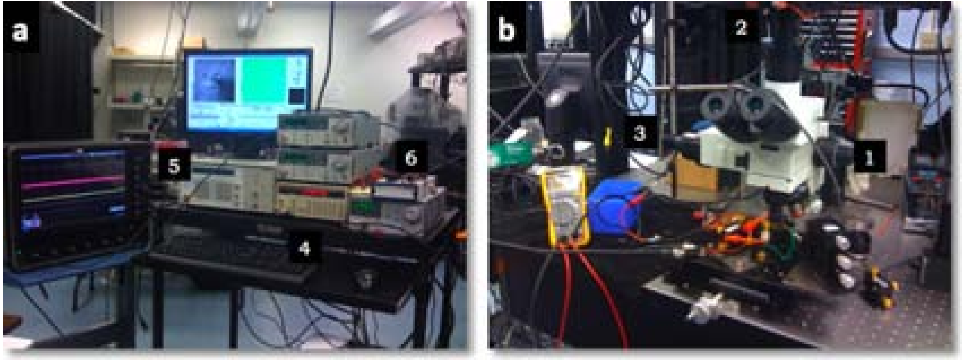


Figure 2.27: UCSC thermoreflectance imaging set-up employed - (a) Biasing and transient thermal response equipment. (b) CCD Microscopy head and sample stage with probing system.

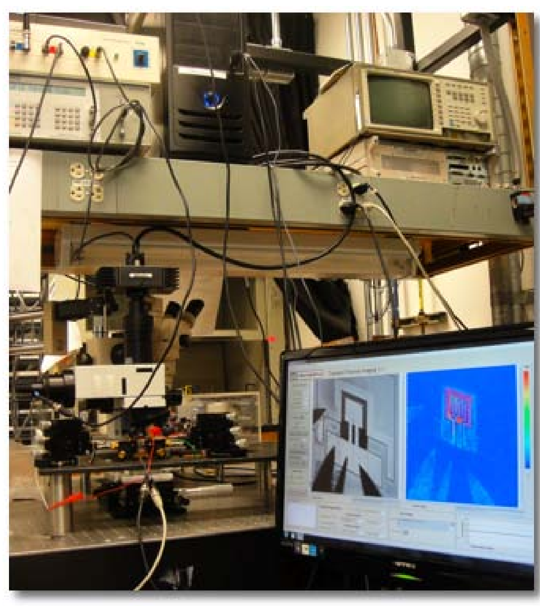


Figure 2.28: Microsanj thermoreflectance imaging set-up employed - The system was improved by making it more compact and adding the ThermoVIEW software. A typical thermoreflectance image can be observed in the screen of the PC.

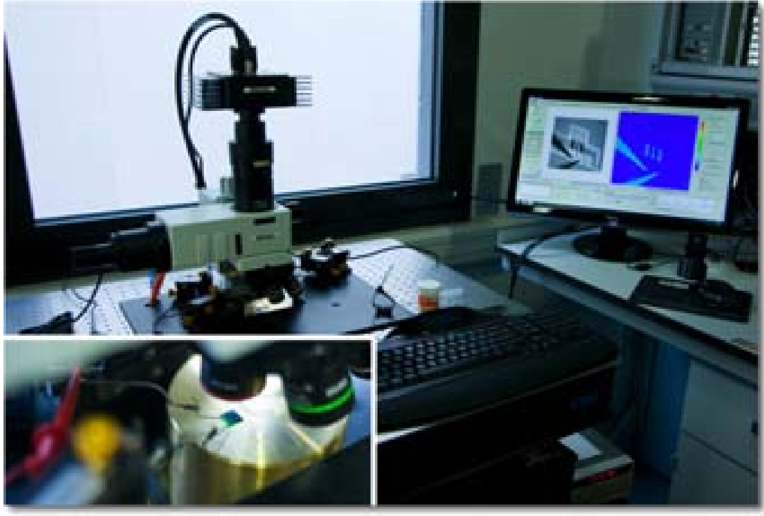


Figure 2.29: IMB-CNM thermoreflectance imaging set-up acquired - A thermoreflectance steady state imaging system was acquired for the thermal characterization of the devices developed throughout this thesis.

3

Silicon nanowires-based thermoelectric microgenerator

3.1 Overview

In this thesis, arrays of silicon nanowires (Si NWs) have been implemented, for the first time, into microfabricated structures to develop *uni-leg* thermoelectric microgenerators (μTEGs) with the aim of converting into electric energy the heat flow originated by the presence of thermal gradients in the environment. This development has yielded a patent [116] and two national grants [117, 118].

In this particular *uni-leg* architecture configuration, the system consists of a thermocouple formed by a *p*-type silicon nanowire array, which acts as the thermoelectric material, and a metal strip. The patented design follows the concept

sketched in Figure 3.1 consisting of a suspended silicon platform (*S1*) connected to a silicon mass (*S2*) through a Si NWs array. The temperature difference is generated across the structure by defining thermally isolated platforms (*S1*) through silicon micromachining techniques. This single thermocouple structure can be replicated and connected in series or parallel, depending on the magnitude to control (voltage or current), to form a complete microgenerator.

In this chapter, the design, simulation and fabrication process of microstructures for the development of planar thermoelectric microgenerators is discussed. The process for obtaining silicon nanowire structures is described as well as the implementation of arrays of this one-dimensional material into the microfabricated structures. In contrast with the work developed by Li *et al.* [53] where a superficial arrangement of top-down defined Si NWs is used, in our case, a bottom-up Si NWs growth has been integrated to allow the dense nanowires arrays to cover the whole volume between the two different temperature zones of the microgenerator device.

Finally, this chapter focuses on the proof-of-concept demonstration of the device by means of electrical and thermal characterization.

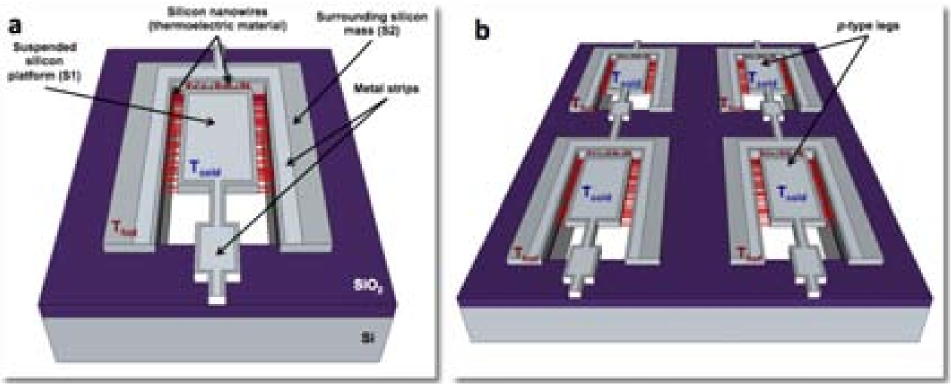


Figure 3.1: Sketch of the patented silicon-based single thermocouple - (a) The designed device consists of a suspended silicon platform connected to a silicon mass through arrays of silicon nanowires, which act as the thermoelectric material for power generation. (b) Uni-leg thermoelectric module consisting of several *p*-type legs connected electrically in series and thermally in parallel.

3.1.1 Uni-leg thermoelectric generators

The work presented in this thesis is based on the so-called *uni-leg* device architecture where a single thermoelectric material is employed together with a metal to form a thermocouple. This type of device has been previously shown to work as a thermopile-based IR detector [119] as well as a thermoelectric generator at a macroscale [120, 121]. The disadvantages of the uni-leg architecture are the reduction of the conversion efficiency due to the lack of a second active semiconductor material and the increment of the thermalization between the hot and cold regions (Figure 3.2) through the metal legs (good thermal conductors). Despite this, the *uni-leg* architecture has been previously used due to its economical advantages for thermopiles fabrication in CMOS technology, or due to technological constraints in thermoelectric modules; for instance, having a single material overcomes the thermal expansion problems at high temperature applications of the modules containing *p*- and *n*-type materials [120]. In this thesis, this architecture was chosen for the device to simplify the overall fabrication process since only one type of silicon nanowire has to be defined from a single bottom up growth/doping step and to partially overcome the thermalization issues by design.

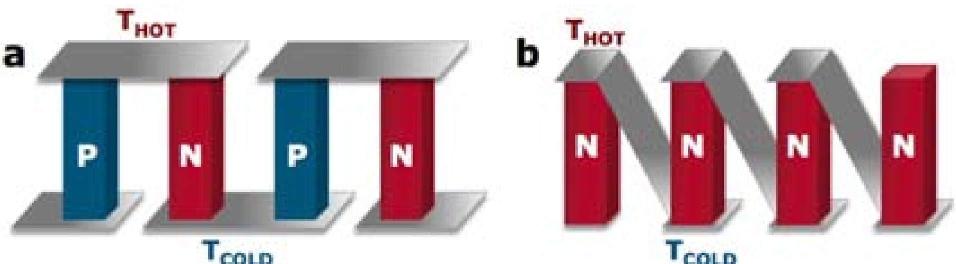


Figure 3.2: (a) Conventional thermoelectric module and (b) *uni-leg* module used in this work - Thermalization of the electrical contacts between the hot and cold regions in the *p*-type *uni-leg* module reduces its efficiency when compared to the *two-leg* architecture (*p*-type/*n*-type materials).

3.2 Silicon nanowires-based thermoelectric microgenerator fabrication

As previously mentioned, the design concept of the device fabricated in this thesis consists of a suspended silicon platform (*S1*) connected to a silicon mass (*S2*) through arrays of silicon nanowires (Figure 3.1). This design allows the natural generation of thermal gradients between the suspended platform and the bulk, which can be achieved by placing the bulk in contact with a heat source (*harvesting mode*). An intermediate proof-of-concept structure that included an additional heater on top of the suspended platform (Figure 3.3) was also developed to make the device characterization easier (*testing mode*) —the heater was used as a thermometer as well.

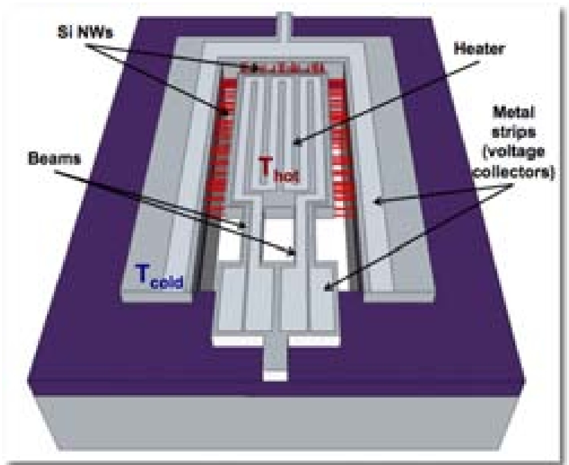


Figure 3.3: Sketch of the complete *uni-leg* design fabricated in this work including a heater for characterization purposes - The integrated heater was employed to establish thermal gradients across the structure. Two beams were incorporated in the design to electrically access the suspended platform as well as to provide mechanical stability to it.

3.2.1 Design & simulation

Accurate device models that allow the evaluation of the system behaviour prior to the fabrication is of key importance in Microsystems development. For the μTEG developed in this project, the influence of the geometry on the device performance

was investigated by simulation. In this section, the thermal distribution of the proof-of-concept devices for different geometries was modeled. The models allowed to determine the optimal geometry for the thermal device characterization at high temperatures, feasible driving voltages, appropiate power ranges and non-destructive currents.

Due to the difficulties for the simulation of devices working under *harvesting mode* (highly dependent on real operation conditions), devices working under *testing mode* were preferred. Therefore, test structures in which the suspended platform (*S1*) acts as the hot silicon mass while the bulk silicon (*S2*) was kept at room temperature were simulated. In addition, a heater was included on top of the suspended platform, which also needed to be designed according to the volume to be heated and the temperatures to be reached as it will be explained further in this section.

3.2.1.1 Suspended platforms

In order to optimize the thermal isolation of (*S1*) and therefore maximize the ΔT between (*S1*) and (*S2*), different thermal simulations were carried out. Simulations were performed modeling structures by means of the finite element method (FEM) using ANSYS Multiphysics 11.0 software to determine the geometry of the suspended and isolated square microplatform of the device. The aim of these simulations, besides defining the geometries of the structures and supporting beams, was to evaluate the maximum temperature and homogeneity that could be reached at the perimeter of the suspended platforms (*S1*), where the nanowires are attached, for each of the different geometries, while applying a certain power in all cases.

Table 3.1 summarizes the parameters that were defined for the simulations. Initially, square suspended microplatforms of 500, 1000 and 2000 μm, with an air trench of 10 μm-width (fixed Si NWs length), were defined and simulated in order to observe the temperature distribution for the different device geometries. The square platform designed for the devices was held by two beams with the aim of providing electrical access to the suspended platform through the heater and electrical connections (for applying current to the heater while measuring the thermoelectric voltage) and as a way to provide mechanical stability. These supporting beams had to be carefully designed to minimize the thermal conduction losses (and therefore undesired thermalization between the hot and cold parts) while maintaining a rigid support to the membrane. Due to the symmetry of the design, the FEM model

reproduced only half of the platform marked by the dotted line in Figure 3.4a. The solid volumes used for the thermal model are shown in Figure 3.4b. Two different widths of beams (100 and 200 μm), which also depended on the width of the heater strips and metallic interconnections, were simulated for each of the three sizes of platform with three different lengths (100, 200 and 400 μm). The thickness of the suspended platform and the buried oxide layer of the SOI wafer were both fixed to 2 μm while the bulk thickness was fixed to 500 μm (Figure 3.5a). Heat was applied to the suspended platforms in the form of a dissipated power density, which was calculated by diving a fixed power of 100mW by the volume of the platform for each case. Structures were simulated with a 500 μm-thick air volume above them and a temperature of 25°C fixed at the base of the bulk silicon as shown in Figure 3.5a.

Parameter	**Value (μm)**
Suspended platform	500
	1000
	2000
Beam width	100
	200
Beam length	100
	200
	400
Si NW length (air)	10
Silicon device layer thickness	2
Buried oxide layer thickness	2
Bulk silicon	500

Table 3.1: Geometrical parameters employed in the simulations - Different sizes of suspended platforms, beam widths and beam lengths were simulated.

Figure 3.6 shows the temperature distribution for platforms with a 100 μm-width beam and different lengths. As it can be observed, the temperature distribution in the small platforms (500 μm) is similar to a cantilever structure while in the larger platforms (2000 μm) it resembles more to the typical distribution across a membrane. Temperature profiles were taken along the perimeter of the platforms as indicated by the dotted arrow in Figure 3.5b in order to observe the temperature homogeneity for each geometry (Figure 3.7).

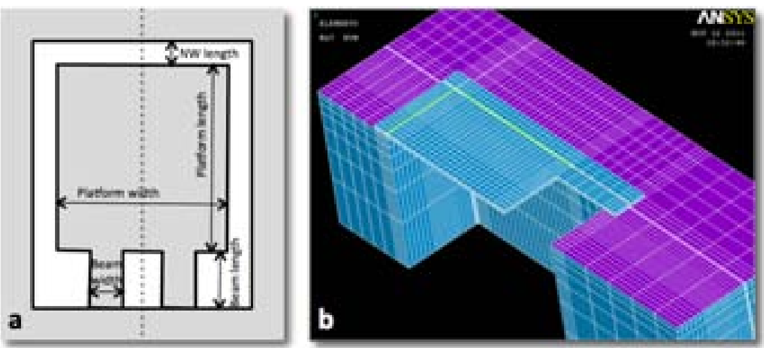


Figure 3.4: Simulated device structure - (a) Sketch of the simulated structure showing the studied parameters. (b) Volumes of the FEM model, the colors allow to differentiate between the silicon and oxide zones.

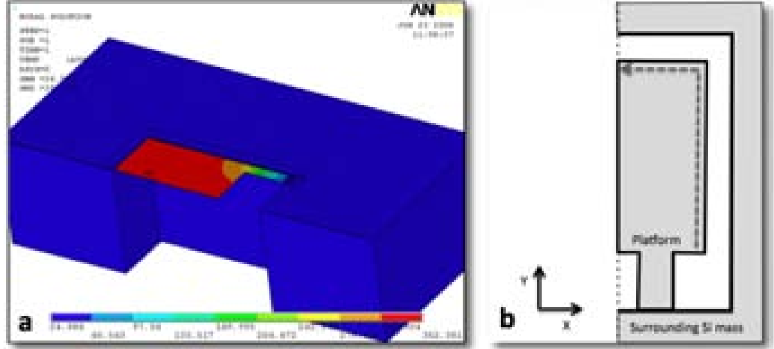


Figure 3.5: Simulation of temperature distribution over the suspended platform - (a) A temperature of 25°C was fixed at the bottom of the bulk Si of the devices while the suspended platform was heated by applying a power density to it. (b) Profile taken all along the perimeter of the platform as shown by the dotted arrow.

Simulations were used to estimate the relation between the dimension of the platforms, the supporting beams and the uniformity of temperature across the suspended platform. The thermal losses were characterized by the highest achievable temperature for the different beam dimensions of each platform size at a constant heating power. From the simulations, it was observed that the bigger the length of the beams and the narrower these were, the better the thermal isolation, i.e. higher temperatures were attained at the edges of the platform. Nevertheless, the beam dimensions are, at the same time, technology-dependent, i.e. if the length of the beam is too large, a bending momentum is caused by the intrinsic stress of the

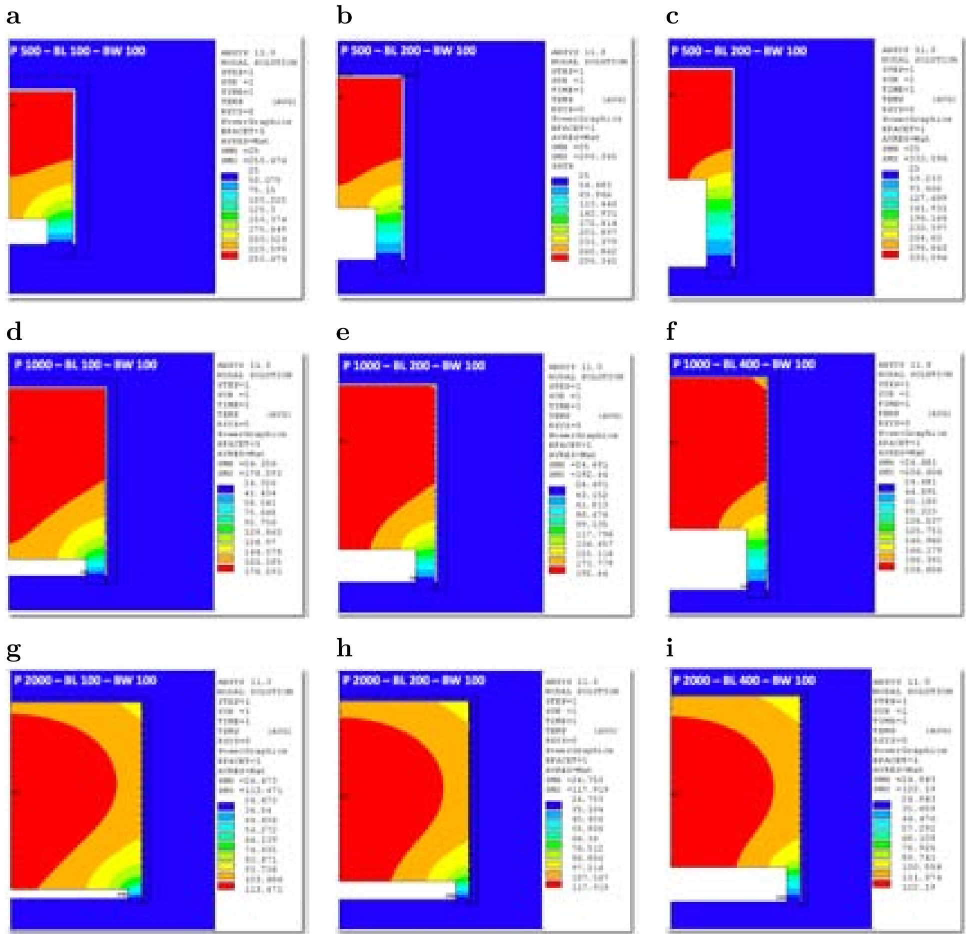


Figure 3.6: Simulations of suspended platforms with 100 μm-width beams - Simulations performed to observe the heat distribution in suspended square platforms of different sizes: (a–c) 500 μm, (d–f) 1000 μm and (g–i) 2000 μm. Three different beam lengths were modeled: (a, g, d) 100 μm, (b, e, h) 200 μm and (c, f, i) 400 μm. Notation: P (platform size), BL (Beam length), BW (Beam width).

lateral load (suspended platform). Furthermore, the bigger the platform, the more homogeneous the temperature reached at its perimeter. This can be observed in Figure 3.7, which represents the temperature profiles of the suspended platforms for 100 μm-width beams showing the temperature homogeneity along the perimeter of the platforms for different beam lengths. Figure 3.8 shows the mean temperature

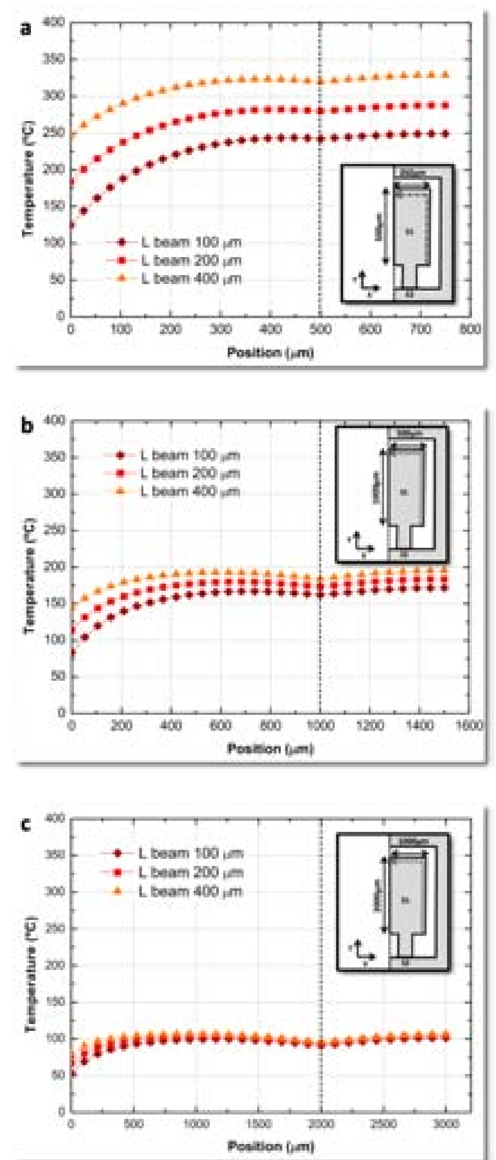


Figure 3.7: Temperature profiles of simulated platforms with 100 μm-width beams - Profiles were taken along the edge of the suspended platforms as indicated in the insets for 500 μm (a), 1000 μm (b) and 2000 μm (c) square platforms. The dotted line indicates the left/top corner edge of the platforms.

of the temperature profiles for the different platform geometries and beam widths as a function of the beam length. It can be observed that higher temperatures are attained with the 500 μm platform with a beam length of 400 μm and a width of 100 μm. As it was discussed in Chapter 1, the Seebeck voltage generated by a thermocouple is directly proportional to the temperature difference developed across it, therefore the maximum temperature achievable was desired through the design of the structures. However, a trade-off exists between the maximum temperatures achieved, the temperature homogeneity desired and the technological constraints that the structure dimensions might entailed.

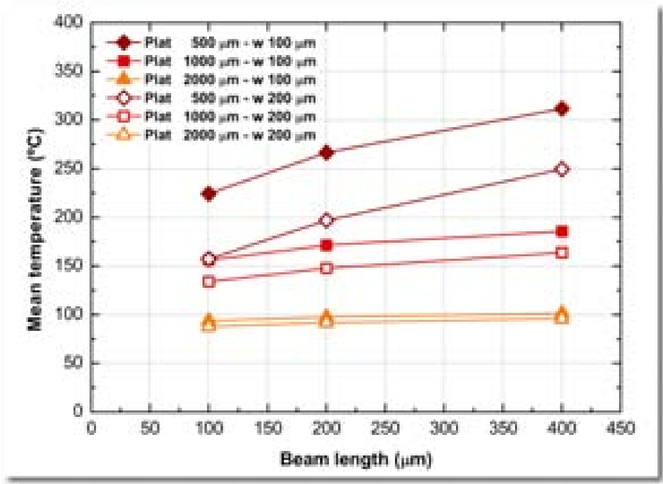


Figure 3.8: Simulated maximum temperature per power density applied on the platforms vs. the length of supporting beams - The graph shows the influence of the beam dimensions on the maximum mean temperature achieved per power density at the edge of the platform for the different geometries. The open symbols correspond to a beam width of 200 μm.

Apart from the geometrical parameters used in the simulations, different lengths of nanowires were initially expected to be grown. Even though this length depends on the growth time employed, as it was explained in section 2.2.1.1, nanowires larger than a couple microns had not been grown at our research facilities yet. As part of the fabrication challenge, and in order to increase the trench between the suspended mass (*S1*) and the surrounding silicon mass (*S2*), nanowire lengths of 10, 20, 30 and 50 μm were initially considered.

3.2.1.2 Heaters & Electrical contacts

Once the design and the geometry of the devices were established, the optimum design of the characterization heaters patterned on top of the suspended platforms was determined. The design of the heaters depends on their dimensions and the resistivity of the material employed in their fabrication. Usually, microheaters are designed by tuning their resistance while fixing the maximum current density that is going to be applied. Therefore, it is necessary to play with the meandering layout of the heater to obtain an optimum resistance that allows dissipating a certain power without encountering accelerated electro-migration degradation or destructive melting problems in the process. When metallic heaters are heated up electrically, their resistivity is influenced by both annealing effects[1] and electro-migration[2] [122]. As the structure size in electronics decreases, the practical significance of the electro-migration effect increases due to a higher current density. The typical current density at which this effect occurs in metal interconnects is 10^5 - 10^7 A/cm^2 [123]. This current density limit was employed as a design criteria when defining the heater configuration. In order to be able to fix this current density, the sheet resistance of the conductive metal has to be known. In a regular three-dimensional conductor, the resistance can be expressed as:

$$R = \rho \frac{L}{A} = \rho \frac{L}{Wt} \tag{3.1}$$

where ρ is the resistivity of the conductor, L is the length of the conducting line, and A is the cross-sectional area, which can be split into the width W and the layer thickness t. By grouping the resistivity with the thickness, the resistance can then be written as:

$$R = \frac{\rho}{t} \frac{L}{W} = R_s \frac{L}{W} \tag{3.2}$$

where R_s is then the sheet resistance. For a square, L=W, so R_s=R which is also referred to as the square resistance ($R_\square$), expressed in $\Omega/\square$. The $R_\square$ is the

[1] Annealing occurs by the diffusion of atoms so that a material progresses towards equilibrium. The heat increases the rate of diffusion in the material by providing the energy needed to break bonds causing the movement of atoms, which affects the grain size, grain distribution and density of dislocations.

[2] Electro-migration is caused by the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor, i.e. the momentum transfer between conducting electrons and diffusing metal atoms results in material transport.

resistance between two opposite sides of a square and is independent of the size of the square or its dimensional units [124].

The $R_\square$ was used to determine the current density and voltage required to achieve the desired power dissipated by the heater. Initially, Pt was the choice for heater fabrication since this metal is commonly used in the fabrication of heaters by the working group. The required nominal power, in the range of 100mW, limit the current density to a reasonable value of 1 mA/μm^2 [125]. A $R_\square$ value of ~1.1 $\Omega/\square$ was assumed for Pt [126], but in a second stage we moved into W because of stability reasons (see section 3.2.4.1).

By using the resistance provided by the number of squares of the designed heaters multiplied by the $R_\square$ of the corresponding material, the voltage needed to achieve 100 mW was obtained from the following expression

$$P = \frac{V^2}{R} \tag{3.3}$$

The current was extracted from this voltage and resistance values and, by dividing this current by the cross section area of the strip, the current density was obtained. Different heater configurations with different meandering combinations were designed to achieve the highest number of strip squares and, in this way, increase the strip resistance in order to lower the current density. These calculations were performed considering different strip widths. Table 3.2 summarizes the results obtained for each size of platform. Strip widths of 50, 100, 200 and 400 μm were used for the different platform designs according to the beam width of each geometry. As it can be observed from the table, some designs required current densities higher than 1 mA/μm^2 still considered reasonable. These current density issues could have been solved by increasing the width of the beams of the platforms, and therefore the width of the strip, but this solution was rejected since it involved additional thermal losses that reduced the total ΔT across the device. In the final device, a balance was achieved by keeping reasonable current densities while avoiding extra thermal losses.

Finally, another important aspect was considered in the design of the structures: metal strips needed to be added in order to have a complete *uni-leg* structure as well as to make electrical contact for the characterization of their thermoelectric output. These strips (of the same material than the heaters) were added to the final design of the device at both ends of the thermoelectric material (silicon nanowires).

Platform (μm)	Strip width (μm)	Max No. squares	Current density (mA/μm^2)	Voltage (V)
500	50	65	2.99	2.67
	75	53	2.21	2.41
	100	23	2.51	1.59
1000	100	71	1.43	2.79
		82	1.33	3.00
	50	50	1.14	2.35
	200	40	0.95	2.10
2000	200	158	0.48	4.17
	300	120	0.37	3.63
	400	79	0.34	2.95

Table 3.2: Results obtained from the calculations made for the design of Pt heaters - Different heater configurations were considered for the design of heaters, a maximum amount of strip squares was desired to limit the current density to 1 mA/μm^2 and the dissipated power to 100 mW.

3.2.1.3 Design of choice

Table 3.3 summarizes the geometries considered from the results obtained after simulations and the amount of chips assigned for each geometry in a first mask set. A 4" wafer with an effective area of 64 cm^2 (active area of 8 x 8 cm), considering a device size of 0.6 x 0.6 cm (~0.4 cm^2), allowed to have 160 devices by wafer: 60 with a 500 μm platform, 50 with a 1000 μm platform and 50 with a 2000 μm platform. Devices were grouped in 1.2 x 1.2 chips, each containing 4 devices of the same nanowire length. As commented previously, some critical dimensions of the design are heater dependent. Without this characterization heater, smaller thermocouples could be possible and a higher integration could be achieved, if advantageous from a thermal point of view.

Despite the variety of devices shown in Table 3.3, it must be outlined that, after fabrication, not all of these designs were technologically viable. First of all, devices for nanowire lengths larger than 10 μm were discarded due to technological constraints. Nanowire length, which is merely time-dependent in principle, is limited by the tapering phenomena. Moreover, in order to grow different nanowire lengths, different growth processes needed to be optimized for each length (nanowires in devices designed for different lengths could not be grown at the same time) and, after

Platform (μm)	NW length (μm)	Total devices	Quantity	Beam width (μm)	Beam length (μm)	Technological viability	No viability reason*
500	10	25	10	50	200	Yes	N/A
			15	100	200	Yes	N/A
	20	25	10	50	200	No	1
			15	100	200	No	1
	30	5	5	100	200	No	1
	50	5	5	100	200	No	1
1000	10	22	22	100	200	Yes	N/A
	20	18	18	100	200	No	1
	30	5	5	200	200	No	1
	50	5	5	200	200	No	1
2000	10	22	17	200	200	No	2
			5	400	400	No	2
	20	18	13	200	200	No	1 & 2
			5	400	400	No	1 & 2
	30	5	5	200	200	No	1 & 2
	50	5	5	200	200	No	1 & 2

Table 3.3: Geometries defined for the design of the devices - Distribution of the devices fabricated according to the geometry results obtained from the simulations performed with ANSYS. *No viability reasons: (1) Tapering of silicon nanowires, (2) Mechanical instability of suspended platforms.

performing several attempts, it was observed that the longer this process became the more difficult to optimize and the less stable, i.e. nanowires became thinner at the tip as the growth progressed altering the growth velocities. To solve this problem and in order to increase the trench between the *S1* and *S2* silicon masses, a second generation of devices was designed in which several 10 μm-long nanowire arrays were bridged through silicon microspacers as it will be explained in Chapter 4, in this way, only one growth process needed to be optimized. Moreover, structures with 2000 μm suspended platforms were mechanically non-stable and broke during manipulation of samples. Bending was observed in this size of platforms probably caused by the the stress applied to the beams by the lateral load (suspended platform) and the stress of the layers patterned on top of it, also the compressive stress of the buried oxide layer of the SOI wafer below the platform might have influenced these deflections. This bending led to misalignment of structures preventing nanowires to bridge the two silicon masses. In summary, only 500 μm and 1000 μm platform sizes with a 10 μm trench were used, which limited the amount of useful devices to about a third of the total amount of the chips fabricated per wafer. These issues, as it will be explained in Chapter 4, were solved in the layout design of the second generation of devices.

3.2.2 Device orientation required for silicon nanowire growth

Another important parameter that had to be defined, prior to the fabrication of masks and devices, was the orientation of the wafers and surface geometry of the devices. As it was explained in section 2.2.1, silicon nanowires grow along the <111> direction when gold nanoparticles are used as the catalyst and nanowires with diameters above 30 nm are synthesized. For this purpose, the {111} silicon surfaces of the devices where the nanowires were to be grown had to be exposed between the suspended platform (*S1*) and the surrounding silicon mass (*S2*). From the previous experience in the growth of silicon nanowires, Silicon-On-Insulator (SOI) wafers with a (110) silicon device layer were chosen as the substrate for the devices since <111> planes perpendicular to the surface are presented in such wafers. Knowing the spatial distribution of these planes allowed us to define the shape of the devices according to the growth directions (for perpendicular nanowire growth) and to define also whether anisotropic wet etching could be used or not during the fabrication process.

In order to identify which the intersections of the {111} family with a (110)-surface wafer are, the orientations of the typical silicon planes are illustrated in Figure 3.9a. In this image, the (110) plane is defined by the gray area, while the four possible orientations corresponding to the <111> family are colored. It can also be observed that the green (-111) and blue (1-11) planes are the ones which are perpendicular to the (110) plane. In the same way, it is shown that the yellow (111) and red (-1-11) planes are tilted 35.3° with respect to the gray (110) plane. The angle formed between these planes and the (110) plane is the reason why wet etching was not used in the fabrication of the devices since any dimension vertically defined in the (110) plane would be reduced by these planes as the etching would had progressed. Figure 3.9b shows the intersection lines of the different {111} planes with a (110) wafer having its primary flat in the <100> family. Colors have been kept the same as in Figure 3.9a for an easier identification of each line with its corresponding plane.

SOI wafers with a (110) surface orientation device layer and one primary flat in the <111> were acquired from Ultrasil. These SOI wafers are obtained by bonding (110) wafers onto oxidized 'handle' (100) silicon wafers, and thinning down the upper wafer to the desired device layer thickness. As explained before, it was desired to have a perpendicular growth of silicon nanowires in the whole area delimited by the perimeter of the suspended platform (*S1*). Therefore, these perimeter walls had to

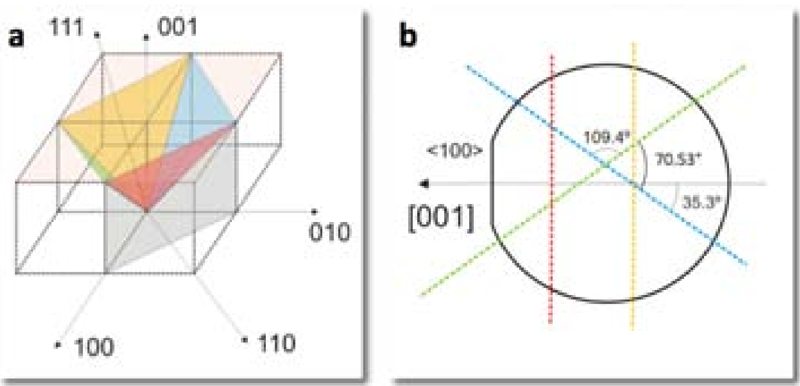


Figure 3.9: Intersection of the <111> planes with respect to a (110) wafer - (a) Orientation of the different silicon planes involved in the fabrication of the devices of this thesis. (b) Intersections lines of the <111> planes with a (110) wafer.

be either parallel to the <111> flat or had to form an angle of 70.53° with respect to the flat as shown in Figure 3.10, and they should be as vertically defined as possible. For this reason, the shape of the real structures is that of a skewed square rather than the orthogonal square that has been presented in the device sketches so far. There are two possible situations regarding the surface distribution of <111> walls depending on which face of the (110) wafer is bonded to the handle wafer. In this work, SOI wafers were ordered according to the orientation shown in Figure 3.10a and device designs were drawn following this orientation. Figure 3.11 shows the mask set design used for the fabrication of devices.

It is certainly important that the starting wafers had the (110) layer consistently bonded in the same way so that the <111> planes matched the orientation given to the designed devices. Even though SOI wafers were specifically ordered to have a determined direction, after several fabrication processes, it was observed that, unfortunately, not all of the wafers ordered were bonded accordingly with this specification. Therefore, in order to determine the wafer orientation, a specific mask was fabricated to produce small trenches in the periphery of the wafers to verify the planes orientations in each of them in order to ensure a correct orientation prior to the fabrication of devices. This procedure is further described in Appendix B.

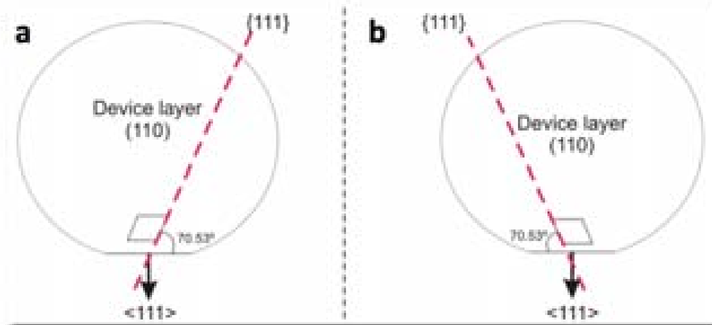


Figure 3.10: SOI wafer orientation employed in this work - Two possible wafer orientations could be used in this work, wafers were ordered to be bonded according to (a).

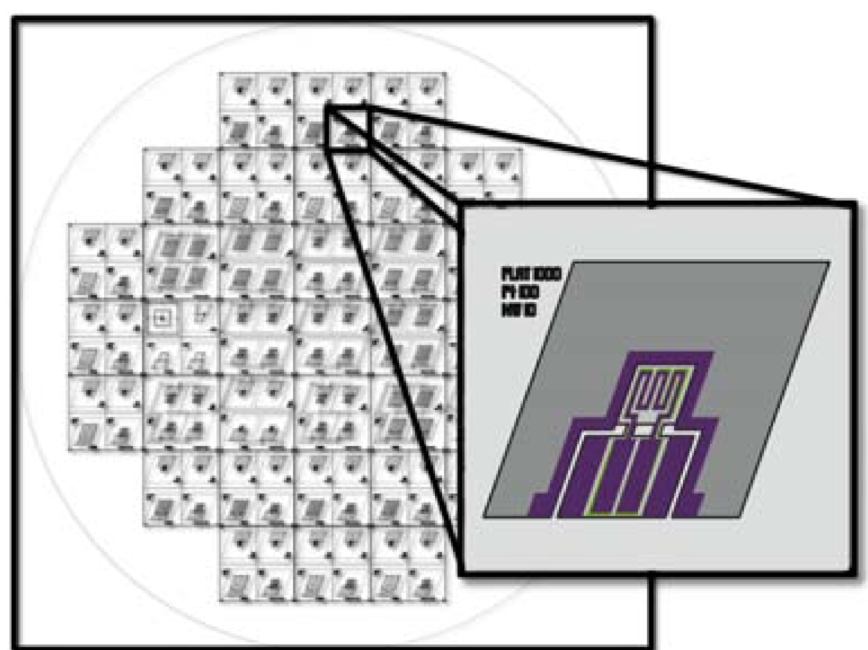


Figure 3.11: Mask set designed for the fabrication of the devices - Devices were drawn with the edges either parallel to the wafer flat or with an angle of 70.53° with respect to it.

3.2.3 Fabrication process

As mentioned in section 2.2, all the fabrication processes presented in this work were performed at the clean room facilities of the IMB-CNM. The main fabrication process followed in this thesis for the development of thermoelectric microgenerators is summarized in Figure 3.12.

Single crystal SOI *p*-type wafers with a 2 μm-thick Si (110) device layer and a 2 μm-thick buried silicon oxide layer over a 500 μm-thick (100) silicon handle wafer were initially used. However, after encountering some issues in the fabrication process, as it will be explained in section 3.2.4.1, the thicknesses of the SOI wafers were changed to a 15 μm-thick Si device layer with a 0.5 μm-thick buried SiO_2 layer and then finally, to a 15 μm-thick Si device layer with a 1 μm-thick buried SiO_2 layer.

As a first step, a 1175 Å low-pressure CVD (LPCVD) nitride layer was deposited and etched to isolate the heater from the suspended platform. A 250/2500 Å-thick Ti/Pt layer was then deposited by sputtering, this layer was initially used as the metal layer to define the heater strips and the electrical contacts and was patterned through a lift-off process. In order to avoid metal exposure during the silicon nanowire growth process, which could change the atmosphere conditions inside the CVD furnace yielding to amorphous silicon nanowire growth (see Appendix C), a PECVD SiO_2/Si_3N_4 layer (3000/2000 Å) was deposited to temporarily passivate the metal.

As a next step, the passivation layer (SiO_2/Si_3N_4) and the silicon device layer were dry-etched simultaneously with a tailored deep reactive ion etching (DRIE) process using the conditions described in section 2.2.2.3 to define the suspended platform and to open the trenches with (111)-oriented sidewalls for silicon nanowire growth using the buried oxide as an etch-stop layer. Finally, an additional standard DRIE process to etch the back side silicon was performed in order to suspend and isolate the platform (*S1*) using, once again, the buried oxide layer to stop the etching process and leaving this layer to give mechanical strength to the suspended platforms for the further silicon nanowire growth process. This last DRIE step represented a fabrication challenge since, as explained in section 2.2.2.3, the suspended membranes of the devices tended to break during this etching stage. In SOI wafers, the presence of a SiO_2 layer in contact with Si introduces stresses in the SOI structure due to a large difference in the thermal expansion coefficient (TEC) of Si (2.5 x 10^{-6}/K @ 25°C) and SiO_2 (4.5 x 10^{-5}/K @ 25°C), which makes the silicon substrate to

Step	Description
	SOI wafer 110 *p*-doped Silicon device layer (15 µm) Buried oxide layer (1 µm)
	1175 Å LPCVD Si_3N_4 deposition on SOI wafer
	Si_3N_4 etching for heater insulation
	250 Å Ti + 2500 Å Pt deposition (metal contacts and heater) + lift-off process
	3000 Å PECVD SiO_2 + 2000 Å PECVD Si_3N_4 deposition (passivation layer)
	Si + passivation layer etching Aluminum deposition on backside (mask for DRIE)
	Aluminum etching + DRIE of bulk Si
	Aluminum removal + Si nanowire growth
	Etching buried thermal SiO_2 + passivation layer

Silicon; LPCVD Si_3N_4; PECVD Si_3N_4; Aluminum; Buried SiO_2; Ti/Pt; PECVD SiO_2; Silicon NWs

Figure 3.12: Main steps of the microfabrication process flow of thermoelectric microgenerators - SOI wafers with a 15 μm-thick Si (110) device layer and a 1 μm-thick buried thermal SiO_2 layer were selected.

shrink more than the oxide layer during cooling resulting in a compressive thermal stress in the oxide layer. In addition to thermal stress, compressive stress due to volume expansion, commonly referred as intrinsic stress, is also developed in the oxide layer during oxidation process. These stresses lead to bending of the SOI wafer and therefore to significant yield loss during device fabrication [127]. In order to solve this problem, SOI wafers with a thicker silicon device layer and a thinner oxide layer were acquired giving rise to a much higher wafer yield.

After these fabrication steps, wafers were cut into 1.2 x 1.2 cm chips, each containing 4 devices with the same nanowire length design. This dicing was needed since, as previously mentioned, the CVD furnace used for NW growth allows up to 2 x 2 cm squared samples. Figure 3.13 shows a SEM image of the as-fabricated microdevice before nanowire growth. The following step, the growth of silicon nanowires, will be explained in detail in the following section. After nanowire growth, devices were released from the buried oxide layer using a SiO-etch solution, etching at the same time the passivation layer (SiO_2/Si_3N_4) and exposing the metal pads. After this process, devices were dried using the critical point drying (CPD) technique, which achieves a phase change from liquid carbon dioxide to dry gas without the effects of surface tension and is therefore suitable to dry fragile structures. For this process, substrates were first immersed in acetone (to wash away all water in the samples) and then transferred into a critical point dryer (Tousimis Automegasamdri®-915B, Series C). The acetone was then washed away with high pressure liquid carbon dioxide, which was then heated beyond its critical point. At this point the pressure was gradually released, allowing the gas to escape and leaving the substrates dried. With this technique, nanowires were successfully suspended avoiding the possibility of nanowires to stick together or collapse.

3.2.4 Implementation of silicon nanowires into microfabricated structures

As described in section 2.2.1, a chemical vapor deposition (CVD) growth based on the vapor-liquid-solid (VLS) mechanism has been employed for growing arrays of Si NWs by means of the galvanic displacement method used for the selective deposition of Au nanoparticles onto silicon surfaces (Figure 3.14).

The diameters of the nanowires synthesized by the VLS method are mainly determined by the size of the metal nanoclusters that serve as the nucleation sites during the initial phase of the nanowire growth. In this work, Au nanoparticles

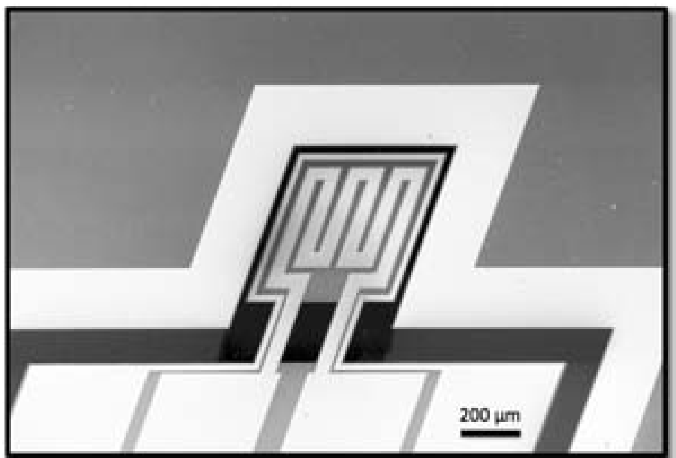


Figure 3.13: Scanning electron microscopy image of the microfabricated structure for the development of thermoelectric microgenerators - The image shows a device before silicon nanowire growth. The device consists of a 500 μm platform with 100 μm-width and 200 μm-long beams and a trench width of 50 μm for silicon nanowire growth, this trench size was chosen for this figure for illustration purposes. An homogeneous and well-defined metal layer for both heater and electrical contacts can be observed.

were deposited by immersion of the substrates in a reversed micelle microemulsion that was prepared by mixing a water-based plating solution with n-heptane and a surfactant, sodium bis(2-ethylhexyl) sulfosuccinate (AOT, $C_20H_37O_7SNa$). The water-based solution consists of 0.2 M HF and 0.01 M $KAuCl_4$. The AOT/heptane solution is made by dissolving 0.33 M AOT in n-heptane. The two solutions were mixed to make microemulsions with different water-to-surfactant molar ratios, R (Eq. 2.1). The reversed micelles that are formed in the microemulsions contain the water-based solution and have a radius R_m that has been found to depend on R according to the empiric law [128]:

$$R_{micelle} = 0.175R + 1.5 \tag{3.4}$$

It has been demonstrated that the diameter of the resulting Au nanoclusters is directly proportional to the diameter of the micelles, providing a way of controlling the diameter of the Au catalyst and consequently the diameter of the nanowires [71, 109]. In our case, we used a molar ratio R=20 to obtain nanowires with a 50–100 nm average diameter and a density of approximately 20 NWs/μm^2 (see Appendix D).

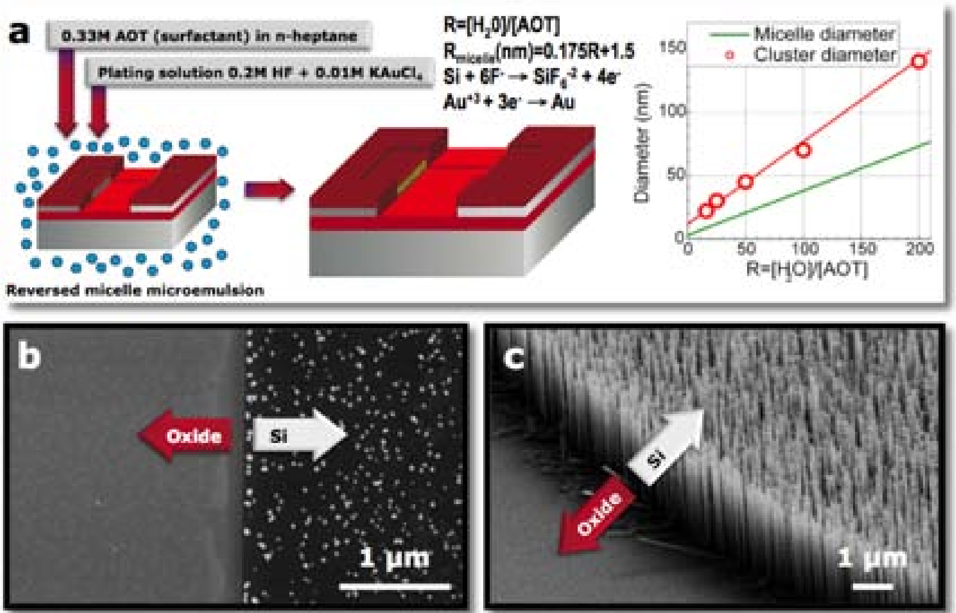


Figure 3.14: Galvanic displacement method employed - (a) Composition of the micelle solution employed for this work. (b) SEM image showing the selectivity of this method, gold nanoparticles are deposited only at Si-exposed areas. (c) SEM image of Si nanowires growth on gold patterned Si surfaces.

In order to implement the silicon nanowires in the microfabricated structures, substrates were first cleaned and the native oxide layer removed using a SiO-etch solution. Substrates were then immersed in the micelle microemulsion for 30 seconds, rinsed in deionized water and dried. In-situ doped silicon nanowires 10 μm-long were then grown in a chemical vapor deposition tube furnace at 755 °C and atmospheric pressure with 10% H_2/Ar as both the diluent and carrier gas. The carrier gas was passed through liquid $SiCl_4$ (growth precursor) and BBr_3 (for in situ *p*-doping) bubblers kept at 0 °C in order to maintain a constant vapour pressure. Flow rates of 270 (diluent), 40 ($SiCl_4$ carrier) and 1 s.c.c.m. (BBr_3) were used.

Once the substrates are placed inside the CVD furnace, the silicon from the source ($SiCl_4$) enters the Au nanoclusters (formed in the galvanic displacement method) and begins to saturate them. Once supersaturation is reached, the silicon solidifies and grows outward from the nanocluster forming the nanowire as shown in Figure (2.2). The final product's length is adjusted by simply turning off the source.

The time used to grow silicon nanowires 10 μm-long was tuned according to the conditions employed but in average a 20 minute-growth period was used, which was enough to achieve both the desired length and the bouncing of nanowires ensuring in this way an epitaxial contact with the opposite sidewall. The tilted SEM image of Figure 3.15a shows horizontal nanowire growth in an exposed silicon sidewall, which demonstrates that the galvanic displacement also takes place correctly at vertical silicon exposed areas and that growth occurs all along the silicon wall, from top to bottom, of the opened trenches. A top view of the same freestanding array can be observed in Figure 3.15b.

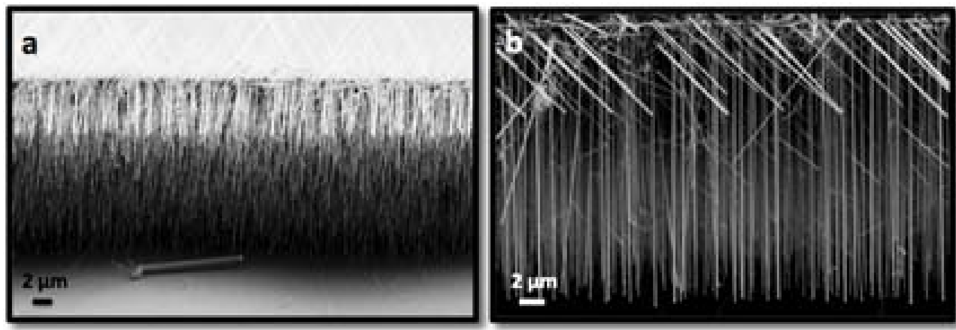


Figure 3.15: SEM images showing horizontal nanowire growth in a silicon sidewall - (a) Nanowire growth occurs all along the silicon sidewall. (b) Top view of the freestanding array of silicon nanowires.

In order to ensure crystalline growth of silicon nanowires, a TEM analysis was performed. Samples were obtained by breaking devices with Si NWs into small pieces and selecting regions where the nanowires were freestanding (without bridging silicon walls). Some of these pieces were directly placed on carbon-coated grids for TEM inspection while some other pieces were embedded in epoxy resin and, using a ultramicrotome (Leica EM UC7) equipped with a diamond knife, very thin cross sections (80-100 nm) of silicon nanowires were cut. Figure 3.16 shows different TEM images of Si NWs. A typical bright field TEM image of the Si NWs forest is presented in Figure 3.16a. Single crystal Si wires with gold nanoparticles on the top are clearly observed. The high resolution TEM image of Figure 3.16b shows an amorphous external layer of ~5nm corresponding to SiO_2 native layer. Figure 3.16c corresponds to cross sections of Si NWs, the hexagonal shape of the section confirms the <111> direction of growth. High resolution images of the cross sections presented in Figures 3.16c and 3.16d confirm the existence of small residues along the

NWs. Selected Area Electron Diffraction (SAED) of these residues suggests they are nanodroplets of gold spread during the VLS growth process. The reduction in the amount of gold during the growth process leads to the so-called tapering phenomena. Due to the progressive reduction in the amount of available catalyst, the NW diameter decreases with length leading to a sharpening mechanism that limits the maximum length of VLS growth NWs. In our particular case, this limitation means a maximum value of ΔT achievable between the *S1* and *S2* silicon masses. Chapter 4 will be focused on designing structures to overcome this major drawback.

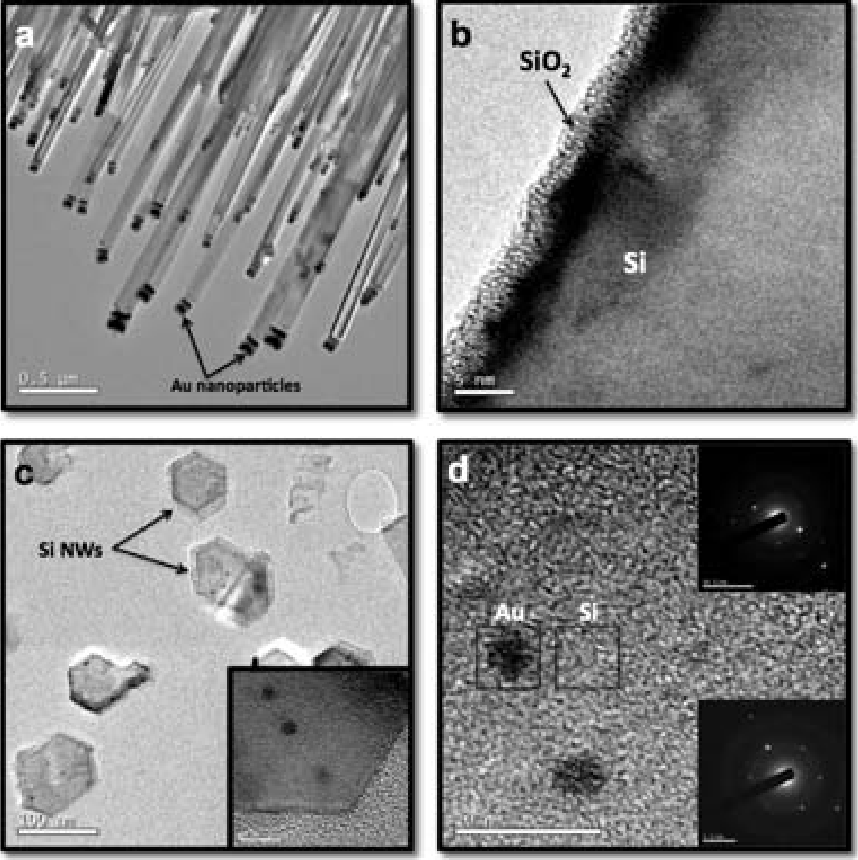


Figure 3.16: TEM images of silicon nanowire arrays - (a) Silicon nanowire arrays showing gold nanoparticles in the tip. (b) Single crystal Si NW with an amorphous external layer of SiO_2 native layer. (c) Cross section of silicon nanowires showing an hexagonal shape. (d) Small gold nanodroplets can be observed along the Si NWs.

Figure 3.17 shows an example of a device after silicon nanowire growth. The inset shows the region were the silicon nanowires bridge the suspended platform (*S1*) and the surrounding silicon mass (*S2*). The image also shows the damaged condition of the metal areas of the devices after this process, which do not longer exhibit the homogeneous and good appearance that was characteristic of the devices before the nanowires growth (Figure 3.13). This degraded aspect, more severe for the heater (metal seating on Si_3N_4 isolating layer) than current collectors (metal seating on Si layer), was observed for the whole batch of devices. The compatibility problems betweeen conventional microfabrication technologies and the Si NW growth that arose during the development of this work will be explained in the following section.

Even though complete microgenerators were rough in appearance and presented several integration problems, some of these devices were still operative and could be characterized as it will be explained later. As a first achievement, silicon nanowires were selectively grown in the regions of the devices designed for this.

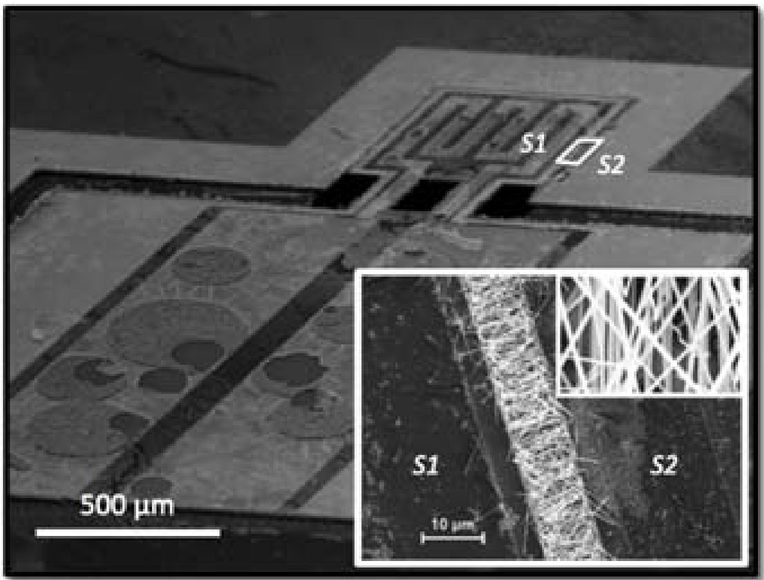


Figure 3.17: SEM images of microfabricated thermoelectric generator after silicon nanowire growth - The image shows the damage caused by the nanowire growth process. The inset is a detail of the silicon nanowire region delimited by the white square connecting the suspended silicon mass (*S1*) with the surrounding silicon mass (*S2*).

3.2.4.1 Compatibility of VLS-CVD silicon nanowires growth with standard microfabrication techniques

Although the VLS method was discovered over 50 years ago and a wide range of nanowire materials, properties, devices, and potential applications have been investigated in the last decade, a great challenge still remains in its integration to form functional systems [129, 130].

Once nanowires have been grown they must be connected to eventually become part of a device or an electronic circuit. Defining contacts in nanowire-based devices is a big challenge. For the characterization of individual nanowires, the most widely used method to define contacts is to remove the nanowires from the growth substrate and transfer them on a second substrate with patterned contacts. The common methods employed for this purpose are the deposition of colloidal suspensions of NWs or the direct micromanipulation of simple NWs [131]. The first method requires the inspection under an electron microscope to reveal promising candidates (among the total amount of NWs transferred) making it a random process, while the second method is an almost "artesanal" process that requires the use of microtools. Finally, the transferred silicon nanowires have to be "properly" anchored to those patterned contacts by selective deposition of Pt through a focus ion beam (FIB) [55, 67, 132]. For nanowire-based devices, where several nanowires have to be embedded, electrical contact is usually made either by directly wire-bonding "silicon electrodes" or by post-patterning of contacts [133, 134, 135].

Basically, the main difficulty in large-scale integration of Si NW-based devices is the compatibility between the 3D growth mode of Si NWs and the 2D planar device architecture, which needs an extra rearrangement or manipulation step to integrate vertical Si NWs into a 2D layout. From this point of view, using silicon micromachining and an appropriate geometry for our thermal device, and the VLS technique as a well-controlled lateral growth of Si NWs, the connection of the nanowires to predesigned electrodes have been achieved. Nevertheless, a metallization scheme compatible with the VLS method is needed to provide an ultimate solution to a planar-architecture-compatible Si NWs-based device integration. The purpose of this section is to summarize the different experiments performed to define a well suited metal for any device involving silicon nanowires growth using the VLS synthesis method. The challenge of this procedure relies in the use of a metal able to withstand the high temperatures as well as the aggressive conditions (highly corrosive atmosphere) typical of the silicon nanowire growth mechanism.

In this work, a metal was required to integrate a heater for thermal characterization purposes and to define contacts for electrical measurements as it was explained in section 3.2.1. Therefore, an optimum metal to achieve this integration should have a good adhesion to silicon for electrical measurements and nitride for thermal measurements. Moreover, the CVD reactor used for the silicon nanowire growth in this study allows working only with 2 x 2 cm-samples, which limits the fabrication process of the device forcing the silicon nanowire growth to be one of the lasts steps after wafer cut. Any metal deposition either for thermal or electrical characterization must be performed before the silicon nanowire growth at a wafer-level process or after the growth at a chip-level process, this last one being a difficult and time-consuming process since the device consists of fragile suspended membranes. Moreover, a chip-level process is hard to overcome due to the surface topology of the samples (i.e., the spin coating step to apply the photoresist on samples for any etching or lift-off process is difficult to achieve)[1]. Furthermore, as explained before, the VLS synthesis requires metal nanoparticles as the catalysts for the nanowire growth process. Therefore, the passivation layer on top of the metal already present in the device plays a key role for avoiding any interference inside the CVD reactor atmosphere.

In microtechnology, commonly employed metals for electrical contacts are Au or Al. However, since the silicon nanowire growth mechanism used in this work requires temperatures between 750 and 800 °C, these metals could not be used in our devices due to the low temperatures at which these metals form an eutectic alloy with silicon, i.e. 359 °C and 577 °C respectively. Instead, a Ti/Pt layer was initially chosen as the metal layer since the eutectic between Pt–Si is formed at 979 °C and below this temperature it is thermodynamically unfavorable to precipitate pure Si [95, 136]. Pt is one commonly used metal in the design of thin-film resistance thermometers [137] and a known material for the fabrication of heaters in our working group. However, the disadvantages of using Pt is that it can not be patterned using direct etching processes and therefore requires a lift-off step, and that it has a poor adhesion to silicon surfaces requiring the use of an adhesion layer, e.g. Ti. Figure 3.13 shows the as-fabricated microdevice before the nanowires growth. Homogeneous, well-defined and well-passivated electrical Ti/Pt pads for both heater (on nitride isolating layer) and current collectors (on silicon layer) were observed for the whole batch of devices.

[1] In order to overcome the problems related chip-level samples, a collaboration with the IREC (Catalonian Institute for Energy Research) for the growth of Si NWs at a wafer-level is ongoing.

Figure 3.18 shows the compatibility issues encountered with this metal after silicon nanowire growth. Delamination of the passivation layer on top of the heater occurred during the silicon nanowire growth process due to the thermal mismatch forced between the SiO_2/Si_3N_4 and Ti/Pt layers during the high temperature treatment. This delamination produced unwanted exposed metal areas that induced changes in the concentration of precursors in the atmosphere inside the CVD tube furnace and therefore irregular silicon NW growth (see Appendix C). In addition, the formation of hillocks and delamination of the Ti/Pt strip itself was observed. This is likely due to the reaction with the passivation layer and the oxidation/reoxidation cycles taking place during the nanowire fabrication process. According to Puigcorbé *et al.* [138], Ti from the adhesion layer and N from the Si_3N_4 passivation layer probably migrate into the Pt film reaching the Pt surface and modifying the heater electrical resistivity. Additionally, the intrinsic and thermal stresses of the Ti/Pt layer led to hillocks formation on the heater surface, which has been previously observed for annealing temperatures above 650°C [139]. These problems caused heaters and current collectors more resistive than anticipated but, in some cases, still operative. In the following paragraphs of this section, a brief explanation on the procedure followed to solve the encountered compatibility problems is given, however, the results of this comprehensive study are discussed further in detail in Appendix A.

Different tests were performed in order to overcome the above mentioned issues of metal stability under nanowire growth conditions. These tests involved a stress analysis of each of the layers comprised in the device, variations on the thicknesses of the layers, changes in the metal adhesion layer and exploring other possibilities for the metal and the passivation layers. After this study, it was decided to replace the Ti/Pt layer for another metal layer and the composition of the passivation layer was also changed from a SiO_2/Si_3N_4 (3000/2000 Å) layer to a 5000 Å oxide layer in order to simplify the process since it was observed that the SiO_2 worked perfectly for the same purpose and had a better adherence to the tested metal layers.

In order to replace the Ti/Pt layer for a more adequate metal layer, a batch of experiments considering different metals (Ta_2Si/Pt, W, Ti/W, TiW, TiW/W and Ta/Pt) as the electrically conducting layer under several deposition conditions was carried out to find a well suited metal that could withstand the silicon NWs growth process when deposited both on silicon and nitride. Once samples were fabricated and exposed to the growth conditions, optical inspection was performed showing

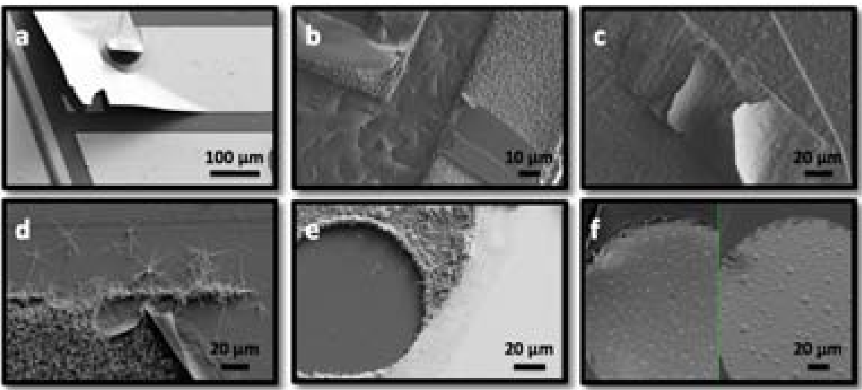


Figure 3.18: SEM images showing delamination of layers and hillocks formation in devices after Si NWs growth - (a) Delamination of metal layer. (b–c) The delamination of the passivation layer produced unwanted metal exposition during Si NWs growth causing irregular nanowire growth as observed in (d). (e–f) Hillocks formation caused heaters and electrical contacts more resistive than expected. Topography of hillocks and delamination of layers was analized by means of secondary electron imaging.

that the samples that were able to withstand the growth procedure were the ones involving W as single layer, Ti and W as an alloy or the combination of these two layers (W and TiW) as it can be observed in Figure 3.19.

Before proceeding to the fabrication of new devices, the sheet resistance, contact resistance and TCR of the chosen metal layers (W, TiW and TiW/W), when deposited on silicon, were measured in order to compare them to the original Ti/Pt layer. In this way, it was expected to characterize the electrical performance of these materials and to determine whether this one would be similar to the Ti/Pt layer or not, since heaters and electrical contacts for the devices had already been designed considering the properties of Pt for it. From the results obtained, it was decided to use W as the metal layer.

Stable metallic pads with a low contact resistance were obtained using 1500 Å-thick tungsten layers. Tungsten showed to have a good adhesion to both silicon (electrical contacts) and nitride (heater isolation) surfaces while good stability, due to the passivation layer, at the high temperatures and corrosive atmosphere inside the CVD reactor during Si NWs growth. Moreover, this metal has been successfully used before for on-chip deposition of carbon nanotubes using microhotplates working at 750 °C by Haque *et al.* [140], which reinforces the results obtained.

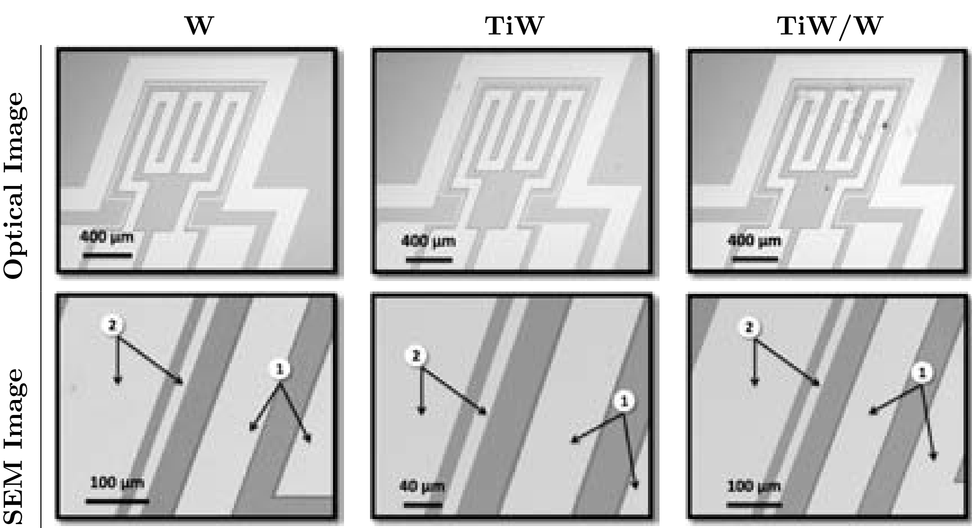


Figure 3.19: Optical and SEM images of device samples with different metal layers - Results obtained after exposing the samples to a silicon nanowire growth process using the VLS synthesis mechanism. The numbers in the SEM images refer to the area on which the layer is deposited: (1) for layers on silicon and (2) for layers on Si_3N_4.

Figure 3.20 shows a device after nanowire growth with W as the metal layer. The inset shows the desired region where homogeneous Si NWs were selectively grown and a detail of the nanowires good aspect.

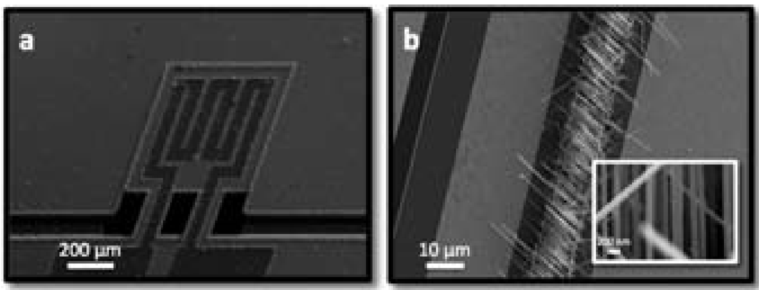


Figure 3.20: SEM images of devices obtained after Si NW growth and after replacing the Ti/Pt layer for a W layer - (a) Image of a device before etching the buried oxide and the passivation layers, neither hillocks or delamination are observed. (b) Detail of the region where the Si NWs were selectively grown, the inset shows the homogeneity, density and uniformity of the nanowire array.

3.3 Silicon nanowires-based thermoelectric microgenerator characterization

After showing the fabrication feasibility of the proposed design, a proof-of-concept characterization was performed. The aim was to verify:

- Good electrical contact between $S1$ and $S2$ through the silicon nanowire arrays.
- Enough thermal isolation to ensure a ΔT between the hot and cold parts of the device.
- Generation of a Seebeck voltage.

This was carried out by using the techniques and experimental set-ups described in section 2.4.1. Although initially devices with a Ti/Pt metal layer presented hillocks formation and delamination problems, devices that were still working, i.e. with operative heaters and metal strips, were characterized. It must be noticed that the observed problems were related mainly to the heater fabrication, which is a test component only useful in the device development phase (*testing mode*). These problems will not necessarily compromise the intrinsic operation of the device as a thermal harvester, since the final device will not need to feature any heater. Therefore, a proof-of-concept characterization was performed while the encountered issues were solved, which served not only to evaluate the response of devices when submitted to a thermal gradient, but to begin the design of the characterization protocol to be followed later on.

3.3.1 Electrical contact through Si NWs arrays

Initially, the fabricated proof-of-concept device, before overcoming compatibility issues, was used to perform electrical measurements to evaluate the conductivity of the Si nanowire arrays, i.e. 4-probe measurements to obtain the Si NWs resistance (R_{NW}), and the Seebeck voltage (V_S) generated when subjected to a thermal gradient. These electrical measurements were made through the platinum strips patterned on the silicon at the edges of the silicon nanowires both in the perimeter of the suspended platform and the surrounding structure as shown in Figure 3.21.

The first proof-of-concept characterization was performed in the device shown in Figure 3.17, consisting of a 500 μm platform structure with Ti/Pt electrical contacts and heater. Resistance along the silicon nanowire array was measured to be 300

Ω, which indicated that the silicon nanowires were electrically connecting both the suspended platform and the surrounding silicon mass [115].

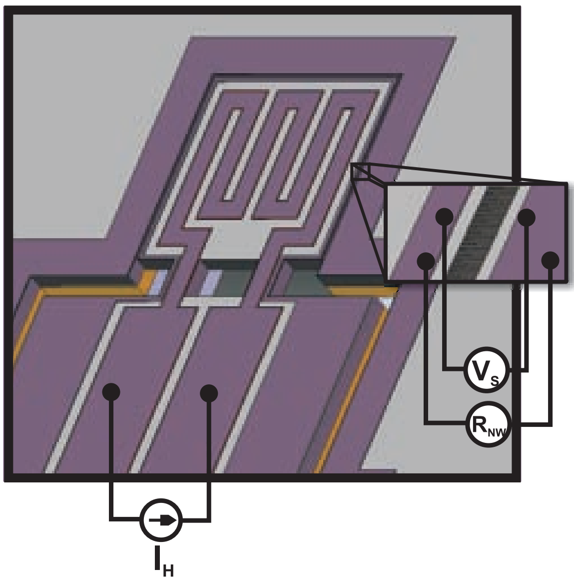


Figure 3.21: Electrical connections for device characterization - Planar view scheme of the device showing electrical connections (the inset shows a zoom of the grown silicon nanowires).

3.3.2 Verification of the thermal isolation

The thermoreflectance imaging technique was used to observe the temperature distribution along the device by means of the integrated heater (*testing mode*). The images were used to determine the temperature difference achieved across the thermoelectric elements (Si NWs) due to an applied electric current to the heater (I_H) on the suspended silicon platform. Measurements were performed using a 50x, NA = 0.5 microscope objective and a white light-emitting diode (LED) as the illumination source. A 30Hz charged-couple device (CCD) camera was used to obtain two-dimensional thermal images. The heater excitation was a 10Vpp and 3.75Hz sinusoidal voltage driving a current of 35 mA through the heater. Calibration of the thermoreflectance coefficient (C_{th}) was performed for silicon and platinum; however, a precise C_{th} for each material was difficult to accomplish due to the roughness of the surface device. These proof-of-concept thermoreflectance measurements were

performed as part of a research stay at UCSC and, at this point of the thesis, the compatibility issues encountered had not been solved.

A thermal image of the device shown in Figure 3.17 when heated up using the platinum heater is shown in Figure 3.22b. A temperature contrast between the suspended hot platform and the cold silicon bulk through the Si NW array is observed. The image confirms that even though silicon nanowires electrically connect the suspended platform to the surrounding silicon mass the thermal transport across them is poor pointing to a promising thermoelectric behavior. Figure 3.22c shows a thermal profile of the device, the arrows in Figure 3.22a indicate the region where the profiles of Figure 3.22c (100 lines) were measured and averaged. A temperature gradient of 20 °C across the silicon nanowires was measured for a 10 Vpp sinusoidal signal applied to the heater.

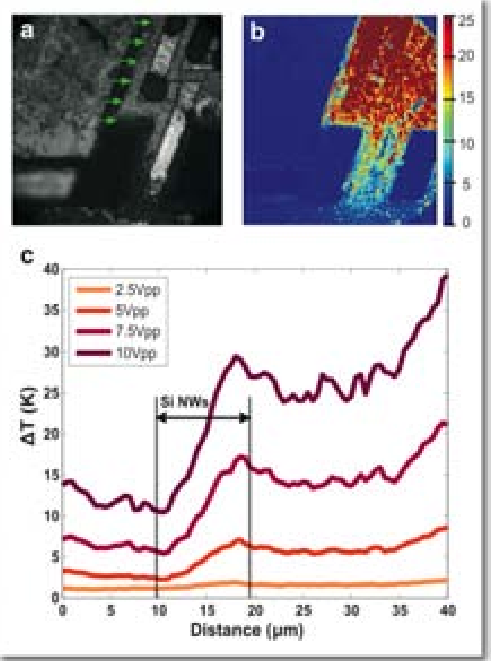


Figure 3.22: Temperature profile across Si nanowires - (a) Optical image and (b) thermal image of the device in ΔT. (c) Thermal profile along the arrows in (a), 100 lines were measured and averaged. The dotted lines of the thermal profile correspond to the silicon nanowires region.

3.3.3 Seebeck voltage measurements

Once the previously described compatibility issues were solved and devices with operative heaters and electrical contacts were obtained, measurements were performed with a probing system as explained in section 2.4.1 heating the suspended platform (*S1*) by means of the integrated heater. The device of Figure 3.20, with a 1000 μm suspended platform, was characterized [141].

In this case, when measuring the electrical contact between the components of the thermocouple: the thermoelectric material (*p*-type Si NWs array) and the metal strips connecting the two silicon volumes, a thermocouple resistance of 198 Ω was obtained with a four-probe configuration, which indicated that the Si NWs were electrically connecting the *S1* and *S2* silicon masses. In this device, the Seebeck voltage of the thermocouple was measured by applying a DC current sweep to the heater. A polynomial fit to four of these current sweeps is presented in Figure 3.23a. To make an estimation of the temperature produced by the heater in the suspended platform from its resistance, a measured TCR of 1920 ppm/K was used for tungsten.

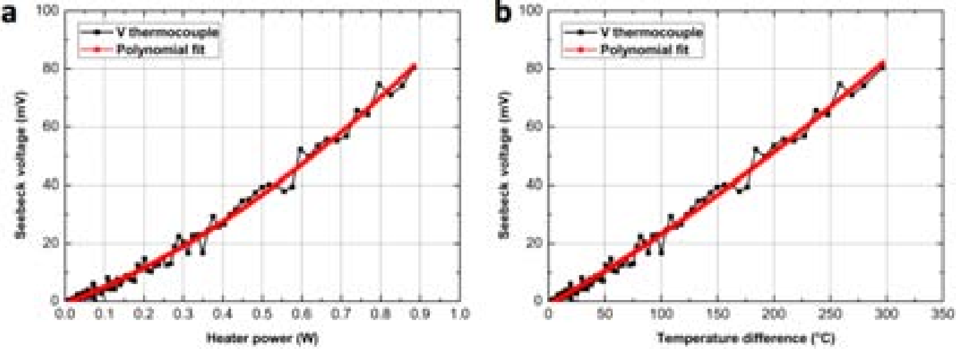


Figure 3.23: Characterization results of a device by means of the integrated heater (*testing mode*) - (a) Seebeck voltage of the Si NWs measured while applying a DC current sweep to the heater. (b) Seebeck voltage as a function of the calculated temperature difference.

As indicated by the previous results, where the thermoreflectance imaging technique was used to measure the temperature profile along the silicon nanowires while applying different sinusoidal voltages to the heater, it was observed that the temperature in the silicon mass *S2* increased only a few degrees under similar operation conditions for different imposed thermal gradients. Assuming that the silicon mass *S2* remained at room temperature, a temperature difference of 300°C across the

thermocouple was obtained when a maximum DC current of 100 mA was applied to the heater (resulting in a power dissipation of 950 mW), which led to a generated voltage of 80 mV (Figure 3.23b). From these results a Seebeck coefficient of approximately 270 μV/K was calculated for a temperature difference of 300°C. This value which corresponds to typical values for bulk silicon (100–1000 μV/K –depending on dopant levels) [142].

Alternatively, the nanowire array's resistance and the Seebeck voltage were also measured by heating the base of the device with a hot plate (*harvesting mode*) but in this case, since the set-ups described in section 2.4.3.3 were under construction, a simpler Linkam chamber that allowed only 2-probe measurements was used. This thermal characterization approach is clearly closer to the harvesting operation mode of a real device since it allows controlling the temperature of the hot source but not the temperature difference increment across the thermocouple. Experimental data and polynomial fits of these measurements are presented in Figure 3.24.

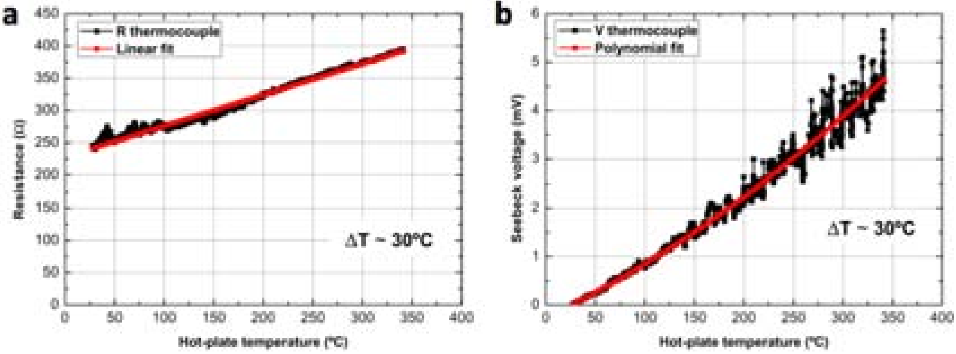


Figure 3.24: Characterization of a device under a *harvesting mode* - (a) Resistance and (b) Seebeck voltage measured at the edges of the Si NWs while heating the base of the device (the x-axis indicates the temperature of the hot plate).

As shown in Figure 3.24a, a nanowire array resistance of 240 Ω at room temperature was measured, this resistance is slightly larger than the previously measured due to the additional contribution of the two-probe configuration of the harvesting set-up used. The thermocouple resistance increases linearly with the hot plate temperature, with a TCR around 2000 ppm/K, which is similar to that of doped bulk silicon. Regarding the Seebeck voltage, a maximum value of 4.5 mV was obtained at a hot plate temperature of 340 °C (Figure 3.24b). According to the results presented in Figure 3.23, this Seebeck voltage value corresponds to a temperature

difference (between the suspended platform *S1* and the surrounding bulk silicon *S2*) of approximately 30°C.

3.4 Discussion & summary

A proof-of-concept novel design of a planar *uni-leg* thermoelectric microgenerator based on Si NWs has been presented and its basic thermocouple element has been fabricated and characterized under both forced thermal gradient and harvesting operation conditions. Si NWs arrays grown by the VLS technique have been integrated in a thermoelectric microdevice combining, for the first time, bottom-up nanotechnologies and top-down silicon microtechnologies in a thermoelectric generator. Reliable tungsten patterning in such devices has been demonstrated, i.e. a stable metallization at the high temperatures and corrosive atmosphere required for Si NWs growth has been shown. The fabrication route proposed allows not only the compatible, but the monolithical integration of VLS nanowires with silicon technology and assures their electrical accessibility with predefined electrodes, which is the great challenge to overcome in order to fully exploit the promising properties of semiconductor nanowires.

The mechanically robust Si NWs array has shown to be a good thermal barrier and high electrical conductivity path between the hot and cold silicon parts of the device, having an effective thermal conductivity low enough to let a temperature difference to build-up across the microdevice and generate a Seebeck voltage when submitted to a thermal gradient. A temperature difference of several hundred of degrees was attained across the Si NWs when using the in-built heater, while tens of degrees were achieved across the device when it was placed on a hot plate at 300°C.

Additionally, the thermoreflectance imaging technique was used to observe the local temperature distribution along the active part of the device.

Although some processing fine-tuning, better thermoreflectance coefficients calibration and more versatile characterization set-ups were still needed, this proof-of-concept characterization pointed to the promising practical application of the improved thermoelectric behavior of single Si NWs anticipated in the literature.

4

Optimization of silicon NWs-based thermoelectric microgenerator

4.1 Overview

In Chapter 3, different low-thermal mass suspended structures were designed and microfabricated on Silicon-On-Insulator substrates to passively generate thermal gradients and operate as microgenerators using Si NWs arrays as thermoelectric material. Such arrays were achieved by horizontally synthesizing silicon nanowires between the opposing (111)-oriented sidewalls of microfabricated thermally-isolated silicon platforms. This design allows passive generation of thermal gradients between those low thermal structures and the surrounding silicon bulk, which is in contact with a heat source. Nevertheless, the temperature difference attainable in such

devices is limited by the short length of VLS Si NWs, which in this work was optimized for 10 μm. In order to obtain suspended Si NWs arrays of lengths bigger than the ones normally achieved by the VLS technique, structures composed by multiple ordered arrays consecutively linked by transversal microspacers (Si bars and pillars) were fabricated. This increases the thermal gradient generated across the device. Figure 4.1 shows a sketch of this second generation of devices.

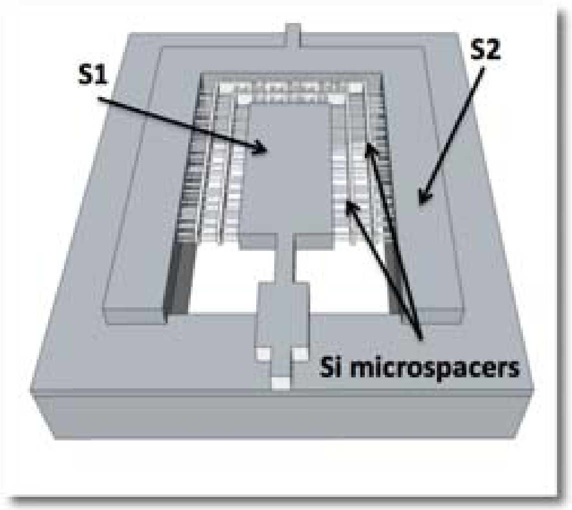


Figure 4.1: Sketch of the basic concept of the second generation of devices - Several silicon nanowires arrays are linked by transversal silicon microspacers (Si bars) widening in this way the trench between the two silicon masses (*S1* and *S2*).

4.2 Design & fabrication

For the design of this second generation of *uni-leg* structures, several constraints observed in the previous structures were taken into account. First of all, it was decided to modify the size of the surrounding silicon mass and therefore, the size of the chip, which decreased from 1.2 x 1.2 cm to 0.7 x 0.7 cm obtaining a total of 116 chips, each consisting of 4 devices giving rise to a total of 464 devices per wafer (about four times more than with the previous designs). In this new layout design, only 500 and 1000 μm platform structures were included, dismissing the 2000 μm platforms due to their mechanical instability and the difficulties encountered during their manipulation. Figure 4.2 shows the final mask set layout with an inset

of a single chip, it can be observed that besides the devices, TLM-like structures for contact resistance measurements are included. This measurements are further explained in Appendix A (section A.3).

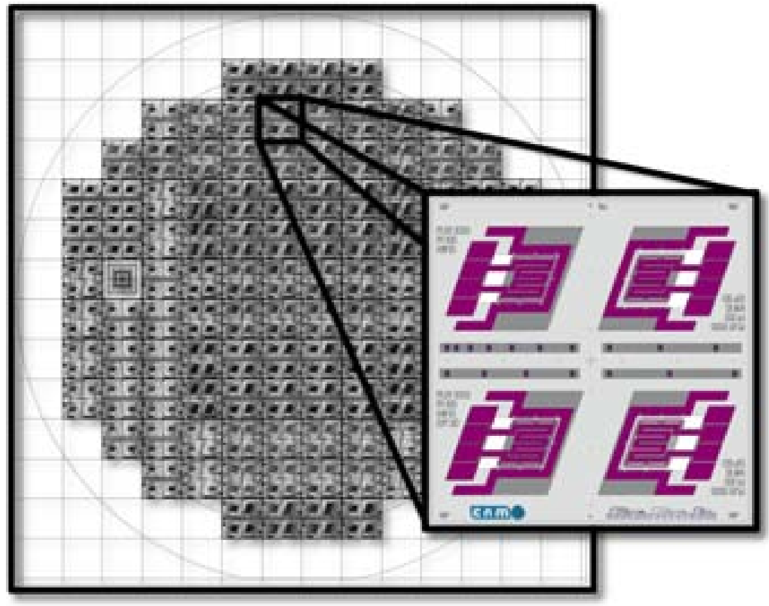


Figure 4.2: Mask set layout of the second generation of devices - Devices were grouped in 4 and TLM structures were included for contact resistance measurements. The structures were rotated and drawn with two sides parallel to the flat with only one side having an angle of 70.53° with respect to it.

Moreover, bending was sometimes observed in the platforms, preventing the nanowires from bridging the two silicon structures of the design as shown in Figure 4.3a. In order to overcome this bending issues, small Si supports (3 μm-width) were added at the corners of the squared platforms as highlighted by the black squares in Figure 4.3b. Initially, bending of structures represented a technological limitation and hence, the maximum length of the beams that held the suspended platform of the device was fixed to 200 μm but, since the mechanical strength of the structures was increased by the additional supports mentioned, this length was increased to 400 μm in order to decrease the thermal losses through the beams and therefore achieve higher thermal gradients.

Furthermore, in the thermal characterization described in section 3.3.1, it was observed that, while performing thermoreflectance measurements, bigger silicon areas

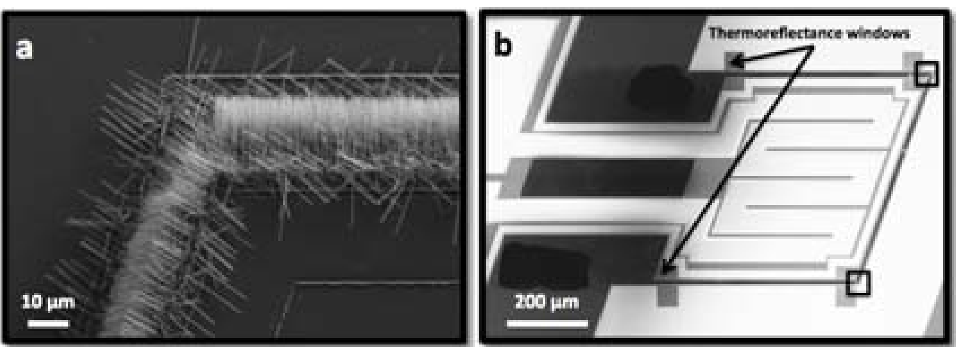


Figure 4.3: Bending problems observed in the first generation of devices - (a) Misalignment of structures prevented silicon nanowires from bridging the two silicon masses. (b) Bending issues were solved in a further design by including two narrow Si supports (highlighted by the black squares) at the corners of the platforms bridging the two masses to give the suspended membrane more stability.

were needed at the edges of the silicon nanowires in order to compare the temperature at the hot and cold areas of the devices. Initially, these thermoreflectance measurements were not taken into account while designing the devices and only small silicon zones remained for this purpose. Therefore, small “windows” were added in the design of the metal patterned at the contour of the suspended platform and the surrounding silicon mass as shown by the arrows in Figure 4.3b in order to ensure zones with smooth silicon surfaces where the thermoreflectance measurements could be performed.

As an additional improvement in this second generation of devices, the structures were oriented in such a way that two sides of the platforms were parallel to the <111> flat of the wafer while only one side formed an angle of 70.53° with respect to it, in contrast to the previous designs where two sides were oriented with this angle (Figure 4.2). The rotation in the design of the structures was intended to ensure the perpendicularity of the horizontal growth in at least two walls of the structures for the cases where the desired bonding of the ordered SOI wafers failed.

Nevertheless, the main feature added to this second generation of devices consisted in widening the trench were silicon nanowires were grown in order to increase the thermal gradient generated across the device. This was performed by adding transversal microspacers that consecutively bridged several 10 μm-long nanowire arrays. These microspacers consisted in small 3 μm-width silicon bars or pillars, which had to be aligned with the (111)-oriented silicon sidewalls where the nanowires would

preferentially grow. Therefore, special attention had to be taken into account when designing these structures with the specific orientation such that the bridging of nanowires arrays could be achieved. In this respect, as it will be explained later, structures including pillars to form nanowire meshes represented a design and fabrication challenge. Four devices with different trench sizes were embedded in a same chip allowing, through the silicon microspacers, to obtain different nanowire “lengths” in a single growth process. The four devices contained in a chip corresponded to a 10, 30, 60 and 90 μm trench width with the corresponding amount of microspacers needed to bridge arrays of silicon nanowires 10μm-long. Devices in each chip were named after the nanowire length as N1, N2, N3 and N4 corresponding to the 10, 30, 60 and 90 μm trench respectively.

The fabrication process of the second generation of devices followed the same design flow described in section 3.2.3. Figure 4.4 shows the final aspect of the fabricated devices.

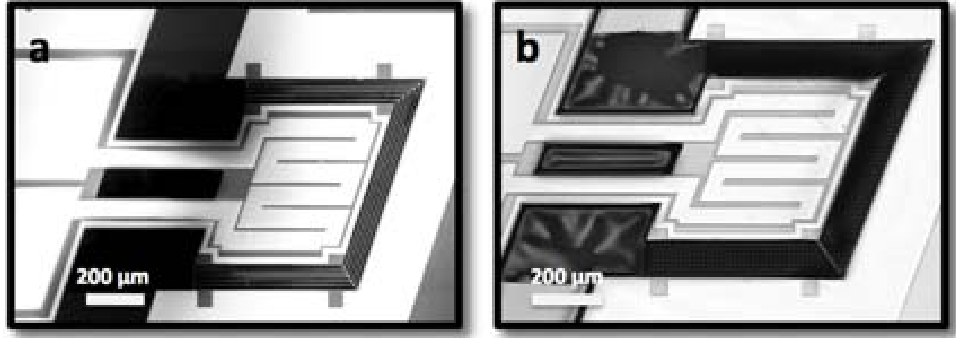


Figure 4.4: Second generation of devices - Square structures with transversal microspacers were fabricated. Silicon bars (a) and pillars (b) were embedded in trenches of different widths.

SOI wafers with a 15 μm-thick Si (110) device layer and a 1 μm-thick buried thermal silicon oxide layer were selected this time. The fabrication process started with a LPCVD nitride layer deposition, which was used to electrically isolate the heater and, in this second generation of devices, also the electrical contacts of the metal collectors strips. In order to overcome the compatibility problems discussed in the previous chapter, the metal of choice on this occasion was W, and a single 5000Å-thick PECVD oxide layer was used as the passivation layer. Both, the silicon device layer and the passivation layer, were consecutively etched until reaching the buried

oxide of the SOI wafer. This step was crucial for the new designs since it defined, at the same time, the main structure of the devices and the silicon bars and pillars for obtaining longer nanowires. The bars and pillars dimensions (3 μm-width), which were close to the photolithography limit (2-3 μm), were difficult to achieve and special care had to be put both in the photolithography and DRIE processes. Figure 4.5 shows a detail of the pillars and bars patterned in the structures. As a last wafer-level step, a Deep Reactive Ion Etching (DRIE) process was performed to etch the backside of the wafer in selected areas in order to form the suspended squared silicon platforms (*S1*) and microspacers using again the buried oxide layer of the SOI wafer as an etch stop. After this process, silicon bars and pillars were held only by the 1 μm-thick buried oxide layer membrane making these structures fragile during any further manipulation process, i.e. wafer dicing, silicon nanowire growth and oxide removal. However, careful handling has permitted the completion of the devices with very good yield.

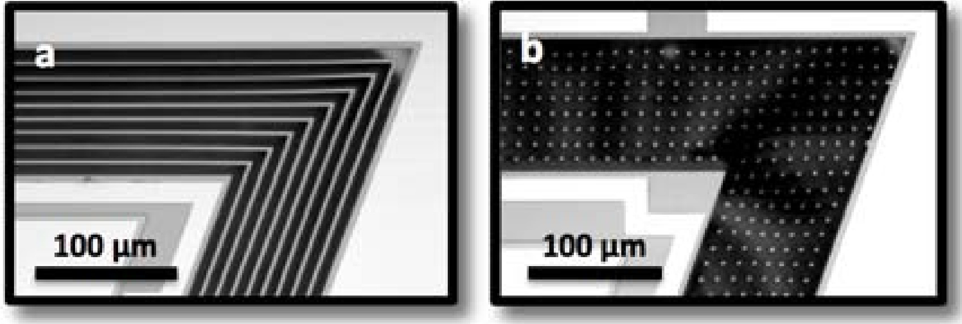


Figure 4.5: Detail of silicon bars and pillars - Several silicon bars (a) and pillars (b) were patterned in order to obtain suspended Si NWs arrays of longitudes bigger than the ones normally achieved by the VLS technique.

The fabrication process of this second generation of devices also entailed some drawbacks. First of all, misalignment of the microspacers (Si bars and pillars) was caused by the intrinsic and compressive stress of the buried oxide layer, which presented an irregular and rough topography, making these fragile silicon structures to tilt and displace from its original place. This misalignment can be observed in Figure 4.5b. It was also observed that, when the DRIE process for etching the device layer was not properly adjusted, the interface between the buried oxide layer and the silicon pillars or bars suffered, causing these structures to detach from the oxide layer. Moreover, the design of the silicon pillars represented a challenge since the

four walls of the pillars had to be aligned and their (111)-oriented silicon sidewalls, where the nanowires would grow, clearly defined, otherwise, after nanowire growth and oxide removal, these structures would simply disappear since nothing would link them (Figure 4.6a). This was observed after growing nanowires in the first batch of fabricated devices where the silicon sidewalls of pillars forming a 70.53° with respect to the flat were misaligned in the lay-out and therefore, silicon nanowires did not bridge, while nanowire growth in the sidewalls parallel to the flat were perfectly linked (Figure 4.6d). Additionally, as it was explained previously, pillars dimensions were in the photolithography limit, which altered their morphology causing more misalignment. In the other hand, microspacers consisting of silicon bars did not represent an orientation problem but, in this case, some lateral misalignment and tilting prevented intermediate Si bars to link adjacent nanowire arrays. Figure 4.7 shows structures with silicon bars after nanowire growth.

Figure 4.8 shows the different issues observed in devices after nanowire growth. The fragile pillars structures that were patterned on, and held only by, the buried oxide layer tended to move out of place. Also, misalignment of bars caused discontinuities in the "total" nanowire array. Nevertheless, these same issues allowed to observe that silicon nanowires were growing all along the vertical dimension of pillars and bars walls and that these structures were mechanically bridged.

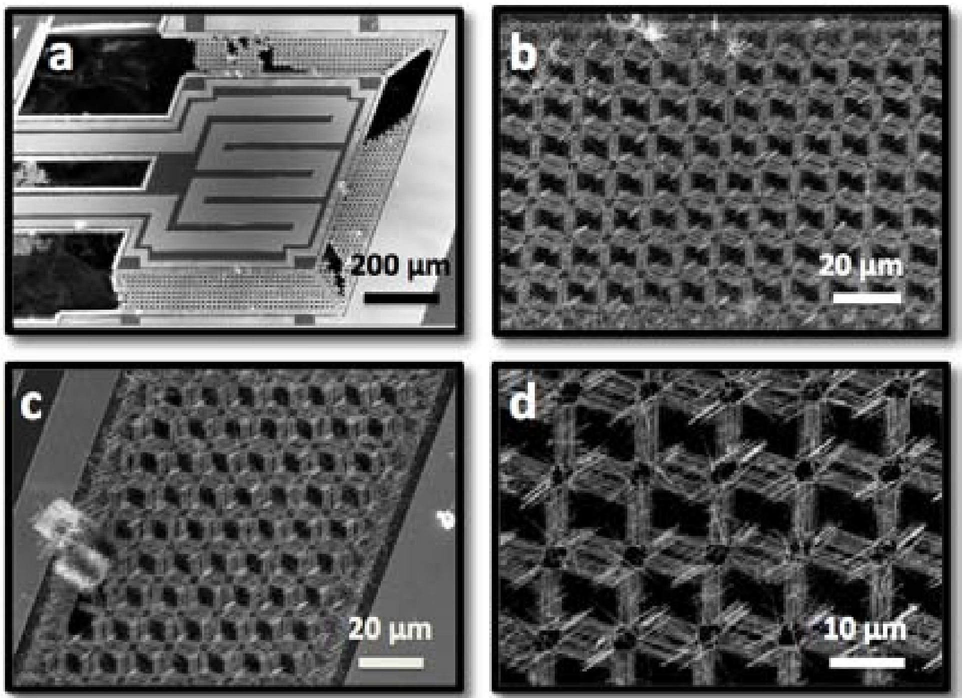


Figure 4.6: Multiple ordered arrays of silicon nanowires linked by silicon pillars - (a) SEM image of a square platform design with pillars bridging nine 10 μm-long arrays of Si NWs forming a nanowire mesh. Details of nanowires bridging pillars arranged in line with the flat of the wafer (b & d) and pillars arranged with a 70.53° respect to it (c).

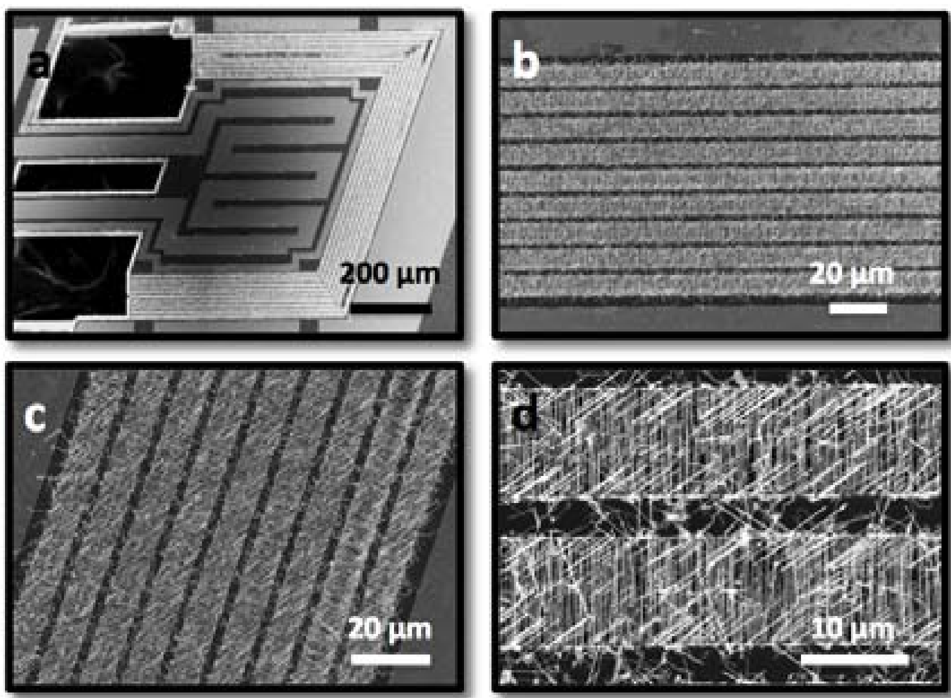


Figure 4.7: Multiple ordered arrays of silicon nanowires linked by silicon bars - (a) SEM image of a device with silicon bars linking nine 10 μm-long nanowire arrays. Nanowire arrays connecting silicon bars parallel to the wafer flat (b & d) and bars forming a 70.53° respect to it (c).

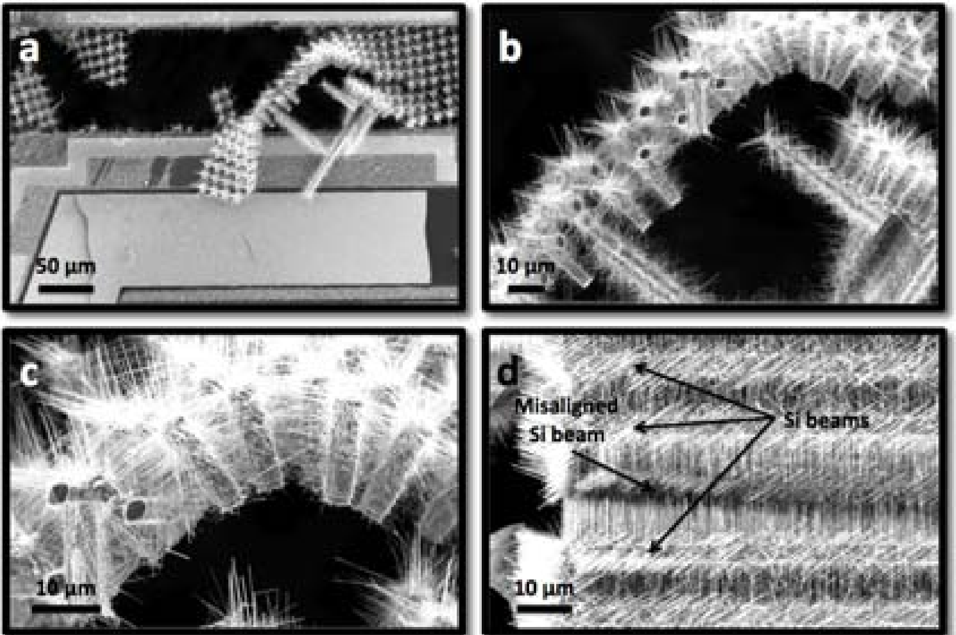


Figure 4.8: Issues observed for the second generation of devices after nanowire growth - (a), (b) and (c) show devices with pillars detached from the buried oxide layer after nanowire growth due to misalignment problems. Silicon nanowire growth can be observed all along the pillar's walls. (d) Lateral misalignment of silicon bars prevented nanowire arrays from bridging properly.

4.3 Characterization

After all the fabrication processes performed to obtain reliable and homogeneous devices, electrical characterization to evaluate the electrical conductivity of the nanowire arrays as well as the capability of the structures to generate a voltage when subjected to thermal gradients was performed. At this point, the characterization process described in section 2.4 was carried out in the experimental set-ups developed for it.

4.3.1 Verification and validation test

Although devices with silicon bars and pillars were fabricated, the last ones were not characterized due to the technological constrains encountered related to the misalignment of the designed patterns in the mask layout. The characterized devices are shown in the SEM images of Figure 4.9 and consisted of square platform designs (500 μm) with arrays of silicon nanowires bridged by silicon bars.

Following the characterization procedure described in Figure 2.13, once SEM inspection was performed, the buried oxide and passivation layers of samples were removed at the same time. Then, an electrical characterization of the internal resistance of the devices before encapsulation (in air and at room temperature) was performed using a probing system as described in section in 2.4.1. The thermocouple resistance (the *p*-type Si NWs array and the metal strips connecting *S1* and *S2*) was measured, under a two-point configuration, to be 62, 60, 74 and 60 Ω for the 10 (N1), 30 (N2), 60 (N3) and 90 (N4) μm-trench devices of Figure 4.9 respectively. This similitude between the resistances of devices bridging different nanowire arrays could be due to a very low resistance of the arrays which did not represented a significant contribution when compared to the resistances of the metal strips, contacts and portions of bulk silicon between the SiNWs and those metal strips, which were similar in all devices. For an instance, when the resistance of similar devices without Si NWs was measured, i.e. the resistance of the silicon supports, the values obtained were 332, 737, 1357 and 2043 Ω for the N1, N2, N3 and N4 devices respectively.

After good electrical contact in the four devices comprised in a single chip was verified and no defects were observed, the chip was encapsulated and wire bonded. The following step performed was the measurement of the TCR of each of the heaters contained in the chip as well as of the silicon structures added for contact resistance evaluation. Figure 4.10 shows the TCR measured for each heater, it can be observed

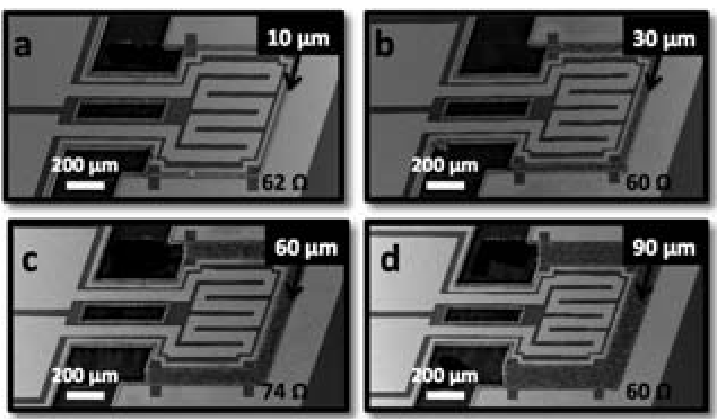


Figure 4.9: SEM images of four devices contained within a single chip - Silicon bars are used to increase the nanowire "length" from 10 μm (a) to 30 (b), 60 (c) and 90 (d) μm in a single growth process by bridging several 10 μm-long nanowire arrays. Images were taken before buried oxide removal.

that the resistance value of the heater of the device with a 90 μm nanowire length (N4) is higher than the others, nevertheless, the slope of the graphs is similar for all the heaters, showing constant TCR values for tungsten. This might be due to a bad bonding effect which made the N4 resistance to oscillate at high temperatures. For practical purposes, and given the similarity between the measured values, an average of the N1, N2 and N3 TCR values was used for the N4 device, i.e. 1921 ppm/°C.

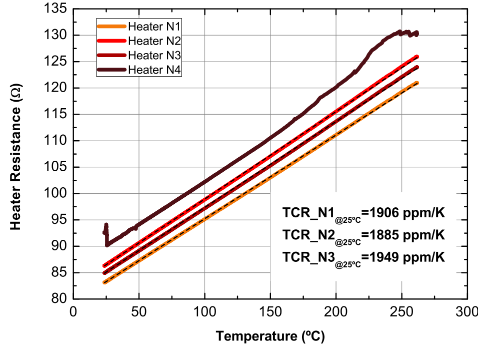


Figure 4.10: TCR values measured for the different heaters of the devices shown in Figure 4.9 - The similar slope in the 4 heaters indicates a constant TCR value for W. The dotted lines correspond to the linear fit curves for each case.

4.3.2 Estimation of the thermal conductivity of arrays of Si NWs

In order to assess the thermal barrier behavior of the Si NWs arrays, the differential approximation described in section 2.4.4.1 was employed using the heater to generate a thermal gradient in the device. This estimation was performed by comparing the dissipated power in the heater necessary to obtain the same average platform temperature (calculated from the heater resistance and its TCR value) in a device with and without nanowires. In a first order analysis, the power differences observed were roughly attributed to an equivalent thermal conductivity of the Si NWs array disregarding any thermal contact resistances.

The graph of Figure 4.11 shows the evolution of the heater resistance (R_{heater}) with the dissipated power for a device with a single nanowire array (N1) and for an analogous device without Si NWs, both measured under air and vacuum conditions. The devices considered have platforms with a side of 500 μm.

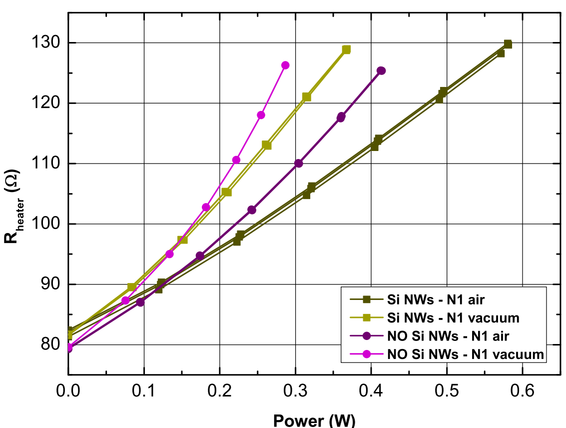


Figure 4.11: Heater's resistance vs. dissipated power for two types of devices: with Si NWs and without Si NWs - Evolution of the resistance of the heater with the dissipated power for the two devices measured in air and vacuum.

Figure 4.12 shows the mean temperature in the suspended platform (derived from R_{heater} by using the previously calibrated TCR value for each device) as a function of the dissipated power. As expected, the device exhibiting the bigger losses is the one with Si NWs operating in air, while the one with smaller losses is

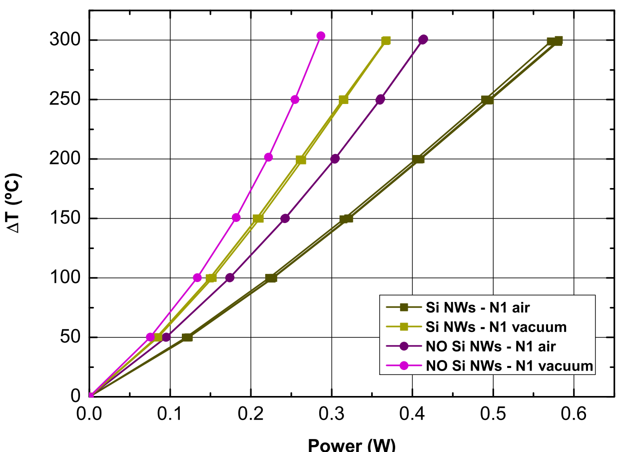


Figure 4.12: Temperature differences generated in two types of devices: with Si NWs and without Si NWs - Temperatures were calculated by using measured TCR values.

the one without Si NWs operating in vacuum (those loses are the ones associated to the platform silicon beams). A first qualitatively indication that the low equivalent conductivity of the Si NW arrays is that the device with Si NWs operating in vacuum present less losses than the device without Si NWs operating in air, thus meaning that the losses associated to the nanowires are lower than the associated to air conduction and convention. In any case, it was confirmed that, both under air and vacuum conditions, the structures containing nanowires need higher power values to attain a given working temperature due the increment in the losses produced by the thermal conduction through the additional thermal path established by the NWs filling the trench between the two silicon masses.

In order to quantitatively estimate the equivalent thermal conductivity associated with the thermoelectric material (Si NWs array), the extra power needed to attain a certain temperature difference in the device with nanowires with respect to its analogous without nanowires was calculated. This was identified as the thermal conductance G of the thermoelectric material, which was determined from the difference in the polynomial fits of the dissipated power as a function of the temperature difference attained in the two devices illustrated in the graph of Figure 4.13.

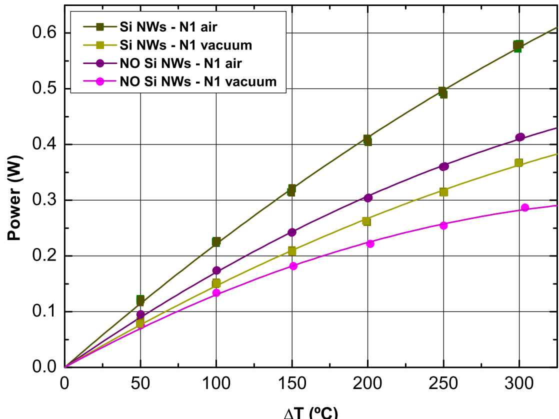


Figure 4.13: Polynomial fits of the dissipated power in the heater as a function of the temperature difference - The values obtained allowed to estimate the power needed to achieve a certain temperature difference value in a device with Si NWs and in one without them.

The obtained result is linear for the measurement in air, which allows interpreting its slope as the ratio between the heat that flows through the NWs array and the temperature difference between its ends. The resulting thermal conductance of the nanowires ensemble is 535 μW/K. On the other hand, the result obtained from the measurements under vacuum conditions is clearly no linear, and the thermal conductance assigned to the NWs array is practically the half, i.e. 253 μW/K (Figure 4.14).

According to equation 2.6, the thermal conductivity κ will be equal to GL/A. An equivalent thermal conductivity of the material filling the trench can be estimated by considering the trench geometry, with a length L of 10 μm, a height of 15 μm (Si device layer thickness) and a total width of 1500 μm given by the platform perimeter (section A: 2.25x10^{-8} m^2). In this way, two equivalent thermal conductivity values related to the Si NWs array were obtained, i.e. in air and in vacuum (Figure 4.15). The results obtained under vacuum conditions would be linked to the inherent thermal properties of the nanowire arrays while the ones obtained in air conditions would reflect better the equivalent thermal behavior under harvesting operation.

In summary, the equivalent thermal conductivity κ of the Si NWs array at room temperature can be estimated as 0.21 W/mK in air, and 0.05 W/mK in vacuum. It

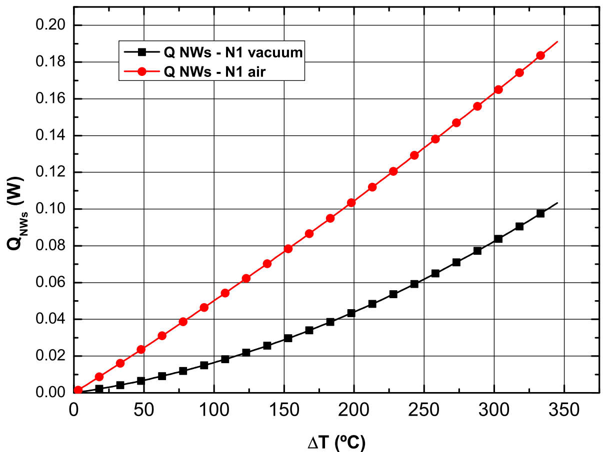


Figure 4.14: Heat flow through devices with and without Si NWs - The slope of the graphs gives an estimation of the ratio between the heat that flows through the Si NWs ensemble and the temperature difference between its ends.

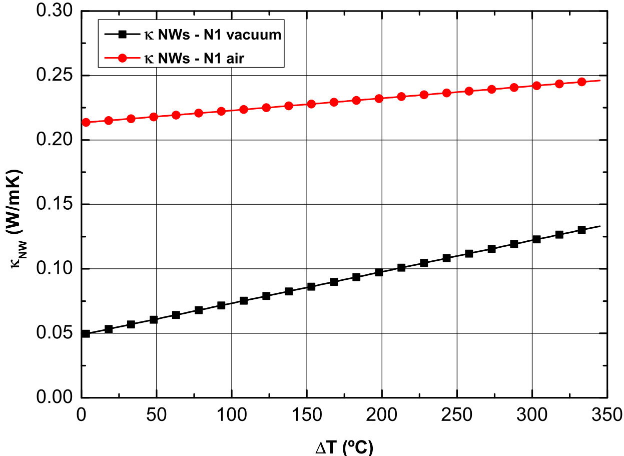


Figure 4.15: Thermal conductivity of Si NWs measured in air and vacuum conditions - By using the geometry of the thermoelectric material and the calculated thermal conductance, the κ of Si NWs was estimated.

can be noticed the "anomalous behavior" that implies the increment of the thermal conductivity with temperature, which is opposite to the bulk material. Nevertheless, the obtained result for the equivalent conductivity of the Si NWs array is higher than the one of air (0.025 W/mK) and much lower than the one of bulk silicon (150 W/mK).

From these results, we can either calculate the occupancy factor of the nanowires by comparing the measured values with the ones reported in the literature for similar nanowires, or calculate the thermal conductivity of the Si NWs fabricated in this work from an independent measurement of the occupancy factor of the NWs array.

The occupancy factor can be calculated from the average diameter of the silicon nanowires and the average nanowire density obtained in the growth. If an occupancy factor is considered and the rest of the volume is filled by air, the effective thermal conductivity can be estimated as

$$\kappa_T = \frac{\kappa_1 A_1 + \kappa_2 A_2}{A_{TOTAL}} \tag{4.1}$$

where κ_1 and κ_2 are the thermal conductivities of the silicon nanowires and air respectively and A_1 and A_2 their respective occupancy areas. In this way, by considering the equivalent material to have a silicon occupancy factor of 2/5 (see AppendixD), a higher equivalent thermal conductivity (0.5 W/mK in air, 0.12 W/mK in vacuum) is obtained.

This value is still lower than the one for bulk silicon. If the same procedure is followed employing a 2/5 occupancy factor for bulk Silicon (κ_1 = 150 W/mK), an effective thermal conductivity of 60 W/mK is obtained, indicating that the additional reduction in the thermal conductivity is due to the nanostructuration of the material.

Besides the already described microgenerator structures, devices with trenches partially filled with bulk silicon simulating different occupancy factors were fabricated. Figure 4.16 shows the power dissipated by the heater patterned in a device with a 1/5 trench area filled by bulk silicon and similar ones with and without silicon nanowires measured under vacuum conditions. Even though the occupancy factor of the silicon bulk structures is only half of the one estimated for silicon nanowire arrays, a much larger heater power is needed to bring the former to the same temperature, thus indicating that silicon nanowires act as an efficient thermal barrier due to the nanostructuration of the material.

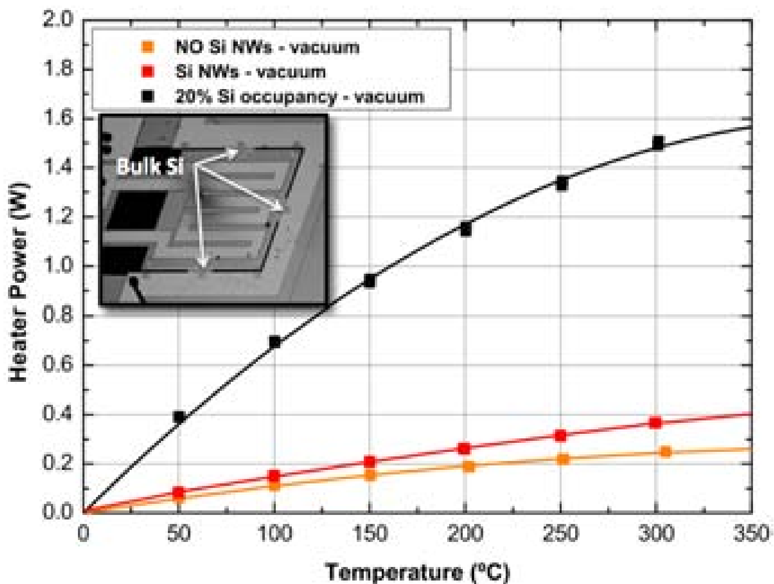


Figure 4.16: Comparison between the power dissipated by the heater on a device with a 20% trench area filled with bulk silicon and similar ones with and without Si NWs - The difference between the dissipated powers demonstrate the effect of nanostructuring silicon. The inset shows an optical image of the device.

In addition, the equivalent Si NWs thermal conductivity obtained is one order magnitude lower than the values previously reported for single nanowires. By using a κ_1 of 40 W/mK [55] and a 2/5 occupancy factor (3/5 filled by air), an equivalent thermal conductivity of 16 W/mk would be estimated instead of the 0.5 W/mK obtained in our case. This discrepancy points to the effect of additional thermal contact resistances present at the interfaces between silicon nanowires and bulk silicon, which in this differential approximation will lead to an underestimation of the calculated thermal conductivity values of the Si nanowires themselves. Regarding these thermal contact resistances, the quasi-epitaxial growth of the Si NWs would lead to the lowest thermal contact resistance possible, from the material perspective, but we cannot assure a zero value for it. Additionally, the effect of the physical constriction of going from 3D to 1D silicon on the heat flow might behave as an additional contribution to the overall thermal contact resistance.

The same procedure for estimating the thermal conductivity was followed for different platform sizes (500 and 1000 μm) and for the different devices contained in each chip, i.e. different nanowire "lengths" (10, 30, 60 and 90 μm). The results ob-

tained are shown in Figure 4.17. In all cases, the equivalent conductivities obtained are comparable (0.05 - 0.25 W/mK).

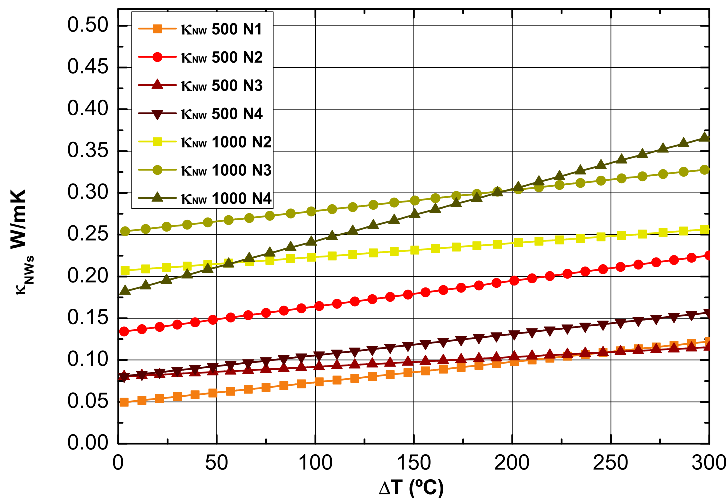


Figure 4.17: Thermal conductivity of Si NWs estimated for different device sizes and nanowire "lengths" - The results shown were determined from the measurements performed in vacuum conditions.

In general, the values estimated are higher for the bigger platforms (1000 μm). An increment of the conductivity with temperature can be observed in all the different cases, and with similar slopes in all cases but a couple of them. Even though the conductivities were not the same for different nanowire effective lengths, no clear dependence of these values with this parameter was observed.

The thermal conductivity of the silicon beams supporting the platform, and the additional supports of the Si NWs arrays,can also be estimated from the power-temperature curves. The calculated values were in consonance with the expected thermal conductivity of bulk silicon (150 W/mK). Reproducing this result for the different devices (Figure 4.18) took only small adjustments on the equivalent width of the platform supporting beams to account for the contribution of the additional supports for the Si NWs.

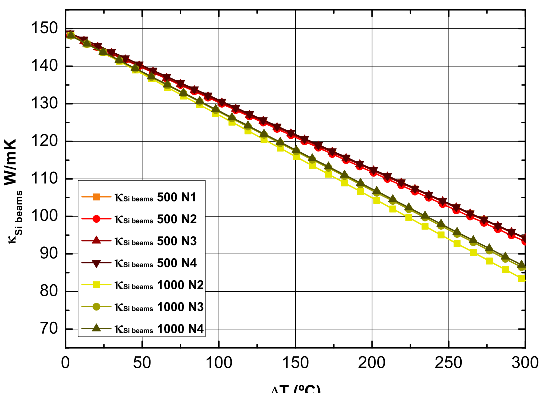


Figure 4.18: Thermal conductivity of bulk Si estimated for different device sizes with different nanowire "lengths" - The thermal conductivity of bulk Si was estimated for the Si supports added to the suspended platforms.

4.3.3 Operation tests

As mentioned in Chapter 2, the thermal gradients, for the characterization of devices, were generated by two different methods: i) heating the suspended platform (*S1*) by means of the integrated heater (*testing mode operation*); ii) heating the silicon bulk (*S2*) with an external hot plate (*harvesting mode operation*).

4.3.3.1 Testing mode operation

After the devices were encapsulated, wire bonded and all needed TCRs values were measured, they were characterized under a *testing mode operation*. In this characterization mode, the heater integrated in the devices was employed to achieve temperature differences across them in order to test their performance. By following the procedure described in section 2.4.3.3 for this operation mode, the previously measured TCR values were employed to compute the target resistance of the heaters in order to force a given temperature value in the suspended platforms (T_{S1}). In this characterization, measurements started at T_{S1} = 50°C and ended at T_{S1} = 300°C with a temperature step of 50°C.

As an initial procedure, the resistance of the heater of the device under test was measured at room temperature and, given its TCR value, the target resistance to achieve T_{S1} = 50°C in the suspended platform was calculated. A DC current,

increasing in 0.1mA steps, was then applied to the heater until its resistance reached the desired value. Once the first target temperature value was reached, the sample was allowed to attain thermal equilibrium by holding this temperature during 5 minutes. After this time period had passed, the generated Seebeck voltage (open circuit voltage), the nanowire array resistance and the I-V characterization curve of the device under study were measured. The I-V characterization curve was measured starting at zero current and ending at the maximum current that could be generated by the device, which was computed using the Seebeck voltage and the internal resistance of the device measured for the temperature set point (see section 2.4). Once the I-V curve measurement ended, the following target temperature was set and the required heater resistance value to achieve it was calculated starting over the characterization procedure at the new temperature value. This procedure was repeated for each temperature step until reaching a maximum value of 300°C.

- ***Determining the temperature gradient***

In order to estimate the temperature gradients attainable during the characterization of the devices, it is necessary to determine the temperatures both in the suspended platforms (T_{S1}) and the surrounding silicon structures (T_{S2}). In this characterization mode, T_{S1} was obtained by means of the integrated heater (by previously measuring its TCR) while T_{S2} was measured through the TLM-like structures added in the devices for contact resistance measurements. Moreover, in this characterization mode, the hot-plate of the Linkam chamber was used as the heat-sink and as a way to monitor the temperature variation at the base of the encapsulated devices. It was observed that this temperature increased 2-3°C for the maximum temperature attained with the heater (300°C).

In previously performed thermoreflectance measurements (see Figure 3.22) it was observed that, by operating the devices under a *testing mode*, the temperature of the surrounding silicon mass (T_{S2}) increased only a few degrees for different imposed thermal gradients. Nevertheless, the thermal gradients achievable with this system were limited to the maximum voltages that could be applied to the heater through the function generator of the system, which allowed dissipating 200°C in the suspended platform at the most.

To verify that the temperature increment in the silicon mass *S2*, i.e. the cold element of the device, remained within a small range for the all the operating temperatures, the resistance of the TLM-like silicon structure was monitored and, by

measuring its TCR value, the temperature increments of the silicon mass *S2* could be estimated. In this way, the temperature of *S2*, through the TLM silicon structures, and the temperature of the platform *S1*, through the heater, could be evaluated. After measuring these structures for different devices it was found that, the temperature increment in *S2* (surrounding silicon) was about 4°C per each 100°C increment in *S1* (suspended platform) as shown in Figure 4.19.

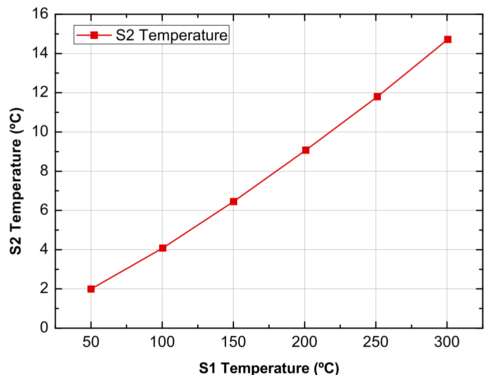


Figure 4.19: Temperature increment in *S2* as a function of the temperature increment in *S1* - A temperature increment in *S2* of around 4°C per every 100°C in *S2* was observed.

Additionally, the thermoreflectance imaging technique was employed to verify the previously measured temperature differences in *S1* and *S2*. As explained in section 2.4.4.2, this technique could only be used to verify those thermal gradients generated across the devices when operated under a *testing mode*. For these measurements, the set-up of Figure 2.29, was employed. A sinusoidal voltage was used to externally modulate the temperature in the heater of the devices through a function generator, employing an oscilloscope to monitor the peak-to-peak voltage values.

Measurements were performed using a 20x and a 50x, NA = 0.5 microscope objectives and a green LED (570 nm) as the illumination source. A 30Hz charged-couple device (CCD) camera was used to obtain the thermal images using a calibrated thermoreflectance coefficient (C_{th}) of $1.1\text{x}10^{-4}$ for silicon. The 2-dimensional images acquired were analyzed using the ThermoVIEW software, which allowed to obtain the mean temperature of selected areas. Figure 4.20 shows the temperature

distribution observed in the suspended platform of the N4 device (90 μm-width trench) with Si NWs and a similar device without Si NWs for different temperatures generated through the heater. The mean temperatures of the small square regions highlighted in the 0°C image for the two types of devices are shown in Figure 4.21. A zoom of the right-bottom corner of the device for the two cases with its corresponding mean temperatures of the hot and cold parts (selected regions) are shown in Figures 4.22 and 4.23 respectively.

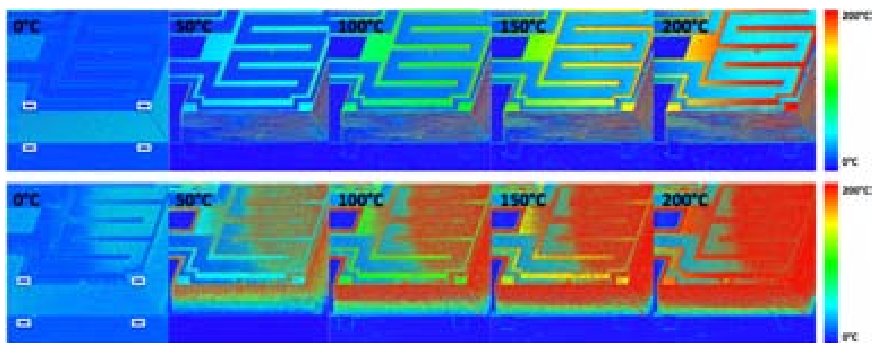


Figure 4.20: Thermoreflectance images of a N4 device without (top line) and with (bottom line) Si NWs - Two-dimensional thermal images were acquired to observe the temperature distribution corresponding to different temperatures attained in the suspended platform (*testing mode*). The areas highlighted by the white squares show the region where the mean temperatures of Figure 4.21 were measured in both cases.

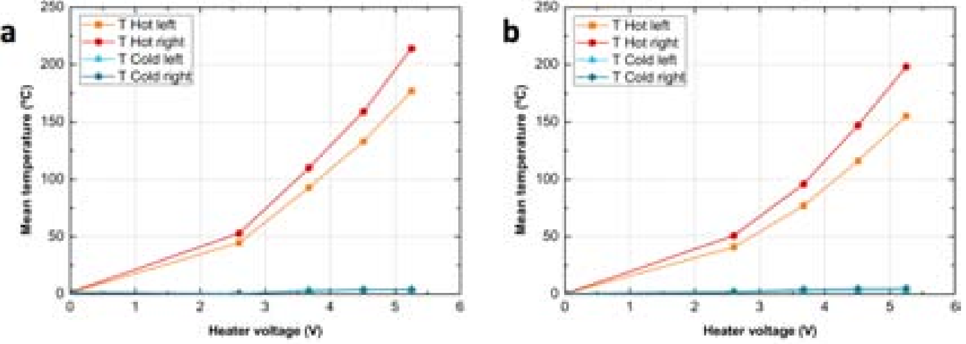


Figure 4.21: Mean temperatures of the regions highlighted in Figure 4.20 - Temperatures measured in a N4 device without (a) and with (b) Si NWs in the highlighted areas of Figure 4.20.

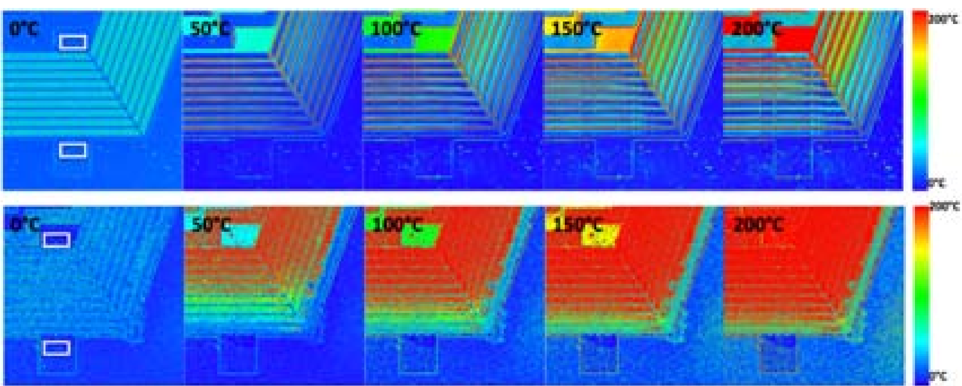


Figure 4.22: Thermoreflectance images of the right-bottom corner of a N4 device without (top line) and with (bottom line) Si NWs - Thermal images for different dissipated powers in the suspended platform corresponding to different average *S1* temperature increments: 0, 50, 100, 150, 200°C.

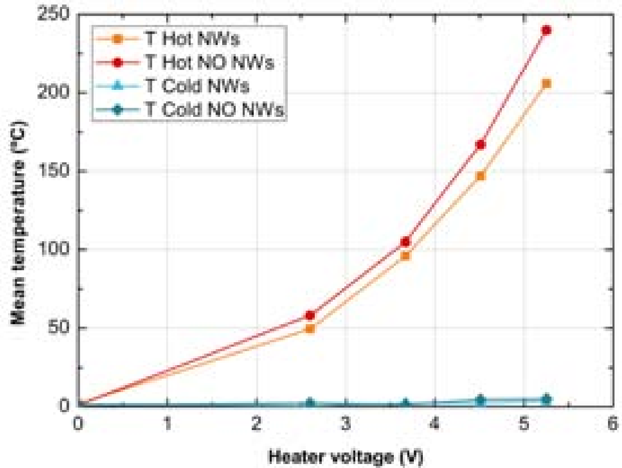


Figure 4.23: Mean temperatures of the regions highlighted by the white squares in Figure 4.22 for devices with and without Si NWs - The cold regions of the devices show a small temperature increment as the temperature in *S1* increases.

Clearly, the cold parts for both types of devices, i.e. with and without silicon nanowires, remained almost at room temperature, with an increment of ∼4°C for the highest platform temperature in the N4 device (200°C). This increment was lower when compared to the temperature dependence of the electrical resistance of the TLM-like structures shown in Figure 4.19 for the N1 device, which demonstrated

a temperature increment of 9°C for a 200°C temperature in the suspended platform of devices with Si NWs. These measurements additionally confirm that a higher ΔT is achieved in the N4 devices due to a design improvement, i.e. devices consisting of several Si NWs arrays transversally linked by silicon microspacers. For simplification purposes, the worst case isolation scenario, i.e. a N1 device, will be taken to define a 5% error in the estimation of the ΔTs presented in this thesis.

In summary, the thermoreflectance technique was useful not only to observe the temperature distribution in structures with and without silicon nanowires, but to confirm once again that the nanowire ensemble served as a good thermal barrier between the hot and cold parts of the devices.

- ***Atmospheric conditions measurements***

As mentioned in section 2.4.3.3, two different environments were considered for the characterization of devices: atmospheric and vacuum conditions. The aim was to measure the device performance in air and to compare it with the case when no thermal losses, through convection, affected this performance.

The first characterization process under the testing mode was performed in atmospheric conditions. The resistance of the devices was measured again to check that the electrical contact was good after encapsulation. In this case, a better contact resistance was achieved through the wire bonding of samples since the resistance values were lowered to 45, 52, 56 and 44 Ω for the N1, N2, N3 and N4 devices respectively (vs 62, 60, 74 and 60 Ω before encapsulation).

As mentioned before, the current applied to the heaters was chosen in such a way that, by using the respective TCR values, temperature difference steps of 50°C were achieved. Figure 4.24 shows the estimation of the power dissipated by each of the heaters to achieve a certain temperature in the suspended platform of the devices. Three consecutive measurements were performed in each device. As derived from the simulations, the more isolated the suspended platforms were, i.e. the longer the effective length of the Si NWs, the lower the power needed to achieve a given temperature in the suspended platform.

The Seebeck voltage generated by the devices at each temperature difference is shown in Figure 4.25. In this case, the temperature increment in the platform is used as a good approximation for the temperature difference across the nanowires. The data of Figure 4.19 shows that this assumption is only overestimating that temperature difference by 5% at most. Therefore, for the following measurements

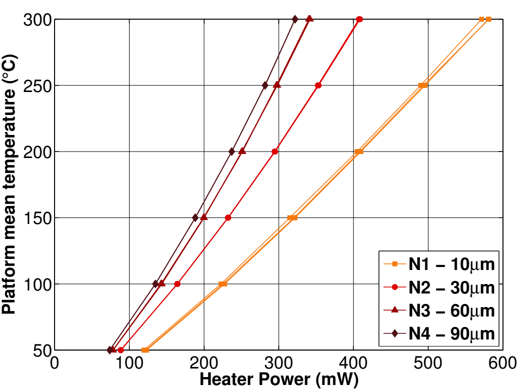


Figure 4.24: Suspended platform mean temperature (above room temperature) vs dissipated power in the heater of the four devices shown in Figure 4.9 - Three consecutive measurements are displayed for each device

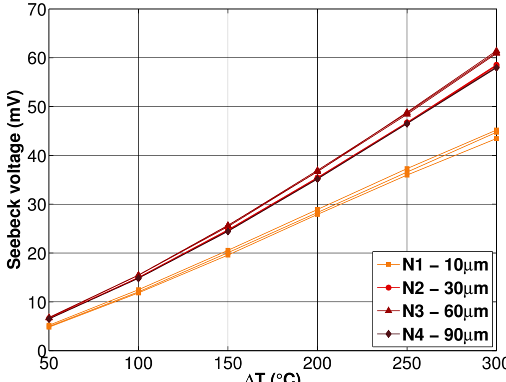


Figure 4.25: Seebeck voltage vs ΔT (above room temperature) measured in the four devices shown in Figure 4.9 - The results obtained were similar for the N2, N3 and N4 devices. Three consecutive measurements are shown for each device.

performed under the *testing mode*, the mean temperature reached in the suspended platform will be considered as the achieved ΔT. These Seebeck voltage values, were expected to be similar in the four devices for a given temperature difference. This was the case for the N2, N3 and N4 devices. It can be observed that the voltages measured for the N1 case deviate from these values, this reason is still under study and it will be considered for the development of future work.

Figure 4.26 shows the different curves measured in each device for the different ΔT. By plotting together the thermoelectric power curves obtained, from measuring the I-V characteristic curve for each device (Figure 4.27), it can be observed that the bigger the effective nanowire length the higher the power generated by the thermocouple, which indicates that adding microspacers to bridge several nanowire arrays in order to increase the thermal gradient effectively enhances the performance of the devices as a power microgenerator thermocouple.

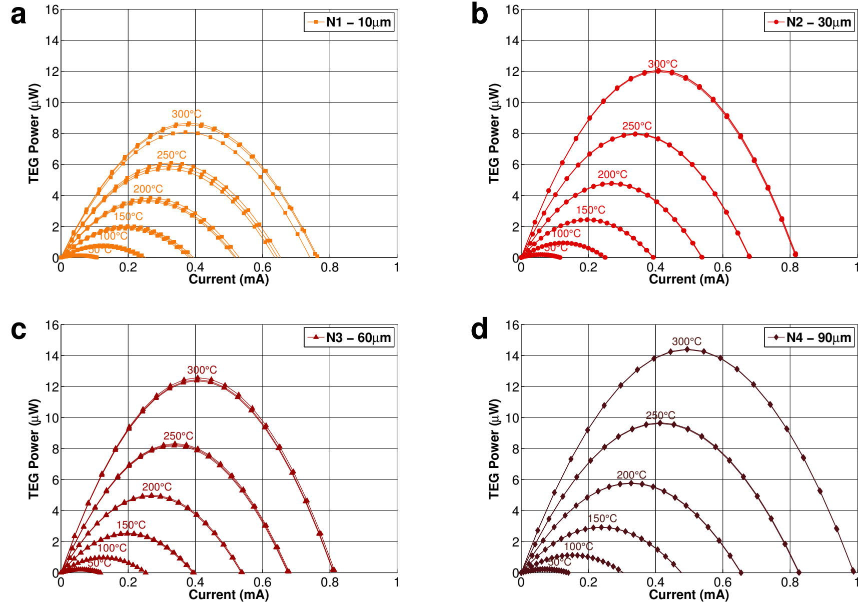


Figure 4.26: Thermoelectric power curves measured for the N1 (a), N2 (b), N3 (c) and N4 (d) devices for different temperatures set in the suspended platform - Three measurements were performed in each device at the temperature differences labeled in the graphs.

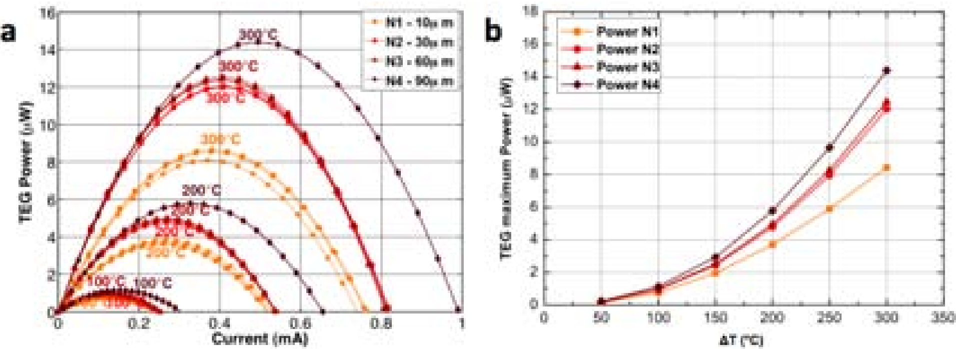


Figure 4.27: Thermoelectric power curves for different temperature set points - (a) Generated powers were measured for several temperature differences set points. Only three temperature set points (100, 200 and 300°C) are shown for illustration purposes. (b) Evolution of the maximum generated power with the temperature difference for the N1, N2, N3 and N4 devices.

- ***Vacuum measurements***

Ideally, high temperature measurements of thermoelectric devices are conducted in a vacuum environment to minimize thermal contributions in the materials and devices due to convective heat transfer. Although the devices presented in this work were characterized in the low temperature regime, the characterization process was repeated in vacuum since thermal management of the system is easier in a vacuum environment where heat conduction and convection from the hot-temperature region to the ambient can be substantially reduced. The reduction of any parasitic heat losses in the system reduces the power requirements necessary to achieve and maintain a given temperature difference.

The experiments previously described were repeated under vacuum conditions. Once the heat losses due to air were eliminated, lower power values were required to attain the different temperature set points in the suspended platform, whereas the obtained Seebeck voltages remained within the same range than before (Figure 4.28). Accordingly, the thermoelectric power values achieved in the different devices were similar to the ones attained under atmospheric conditions for the same temperature differences across the Si NWs (Figures 4.30 and 4.29). A comparison between the results obtained for each condition are shown in Figures 4.31 and 4.32.

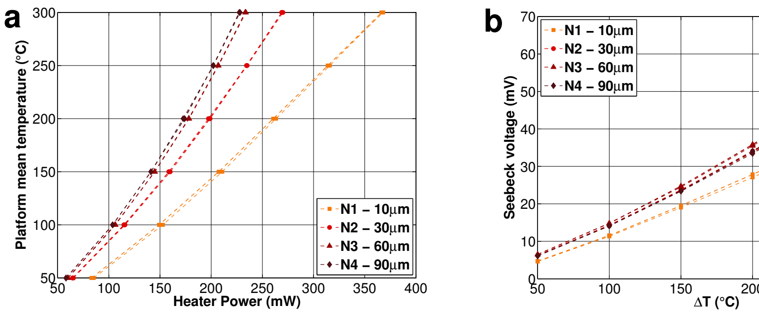


Figure 4.28: (a) Temperature at the platform as a function of the power dissipated by the heater and (b) Seebeck voltage vs the ΔT measured under vacuum conditions - Three measurements are plotted for each case.

Once the previously described characterization process under a *testing mode* was accomplished and in order to ensure that the heaters had not suffered any deterioration, TCR measurements were performed before proceeding with any further

characterization. As expected, the resistance of all heaters and their corresponding TCR values remained almost constant after the performed tests.

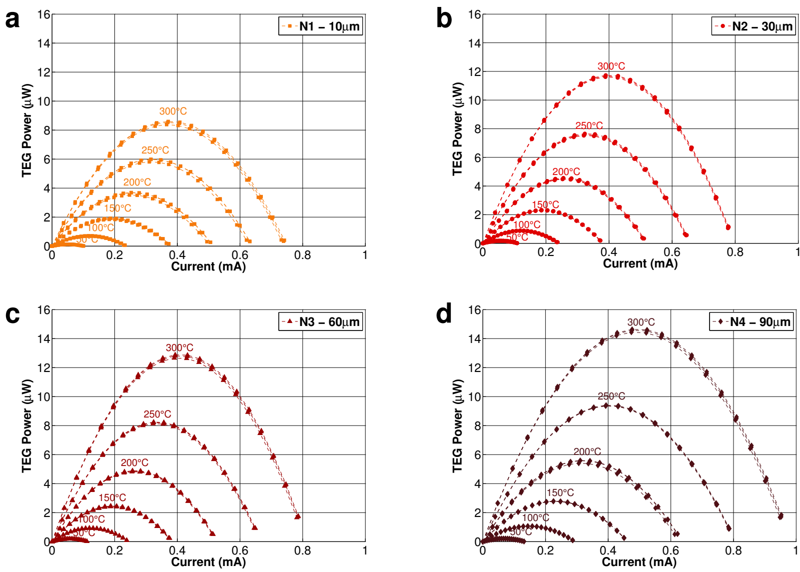


Figure 4.29: TEG power curves measured for the N1 (a), N2 (b), N3 (c) and N4 (d) devices as a function of the temperatures set in the suspended platform under vacuum conditions - Three measurements are presented for each device.

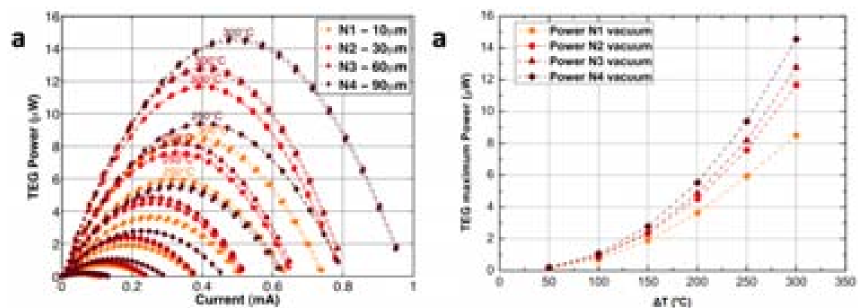


Figure 4.30: Thermoelectric power curves measured for each device under vacuum condtions - The results obtained were similar to the ones presented in Figure 4.27 for the atmospheric conditions results.

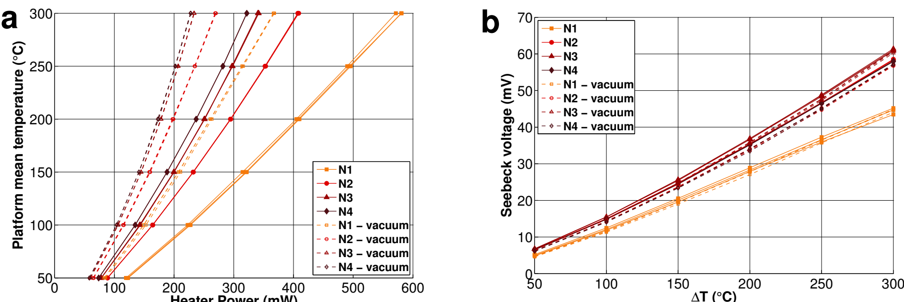


Figure 4.31: Comparison of the platform mean temperature vs the power dissipated (a) and the Seebeck voltage vs ΔT (b) - Measurements were performed under atmospheric conditions (continuos lines) and vacuum (dashed lines).

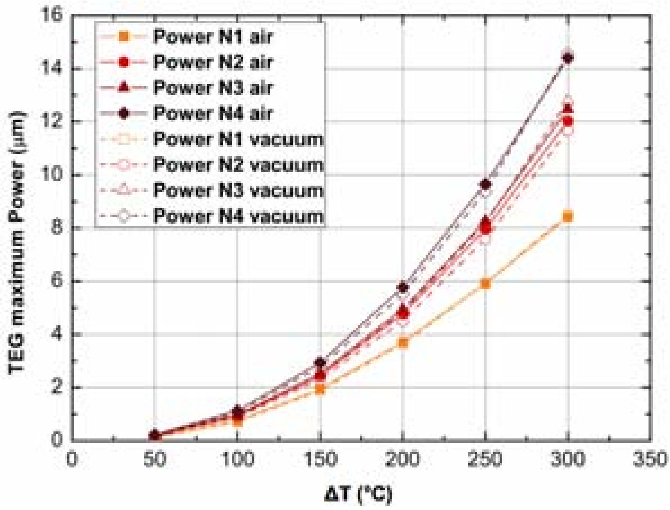


Figure 4.32: Comparison of the maximum TEG powers obtained under atmospheric (air) and vacuum conditions - Evolution of the TEG power as a function of the ΔT.

4.3.3.2 Harvesting mode operation

In order to characterize the performance of the devices as energy harvesters, a *harvesting mode operation* was employed. For this purpose, the procedure described in section 2.4.3.3, with its corresponding set-up, was followed. The encapsulated chip containing the four devices that were previously measured under a testing mode, was mounted on the hot-plate (HP) of the Linkam chamber using a high thermal conductivity paste. In this method, the hot and cold elements of the devices are switched when compared to the testing mode, i.e. the base of the device and therefore the surrounding silicon mass *S2* corresponds the hot part of the device (heated through the hot-plate) while the suspended platform *S1* corresponds to the cold part. In order to increase the thermal gradient across the device and reproduce real harvesting conditions, an air flow on top the suspended platform *S1* was used to cool it down[1].

The measurements performed started at a hot-plate temperature (T_{HP}) of 30°C and ended at T_{HP} = 350°C with a temperature step of 20°C. The Seebeck voltage, the resistance of the device and the I-V curves were measured at each temperature value set in the hot-plate, i.e. at the base of the encapsulated device. Figure 4.33 shows the Seebeck voltages delivered by the devices as a function of T_{HP}.

In summary, also under the *harvesting mode*, the structures with longer effective nanowire length exhibited bigger temperature differences across them for the same excitation input (the temperature hot-plate in this case). A maximum Seebeck voltage of 3.5mV and a generated power of 43 nW for a hot plate temperature of 350°C was achieved with the N4 device.

It should be noted that the *harvesting mode operation* did not allow an estimation of the achieved ΔT in the devices. The measured resistance values of the heater and TLM silicon structures presented a lot of noise due to the forced air flow. Moreover, the thermoreflectance imaging technique could not be employed since, in this system, the heat source should be controlled through the function generator and for this purpose the hot-plate of the Linkam chamber could not simply be used. Ongoing work entails a modification of the thermoreflectance set-up. Furthermore, when comparing the values obtained under the *harvesting mode operation* with the power output results of Figure 4.27 obtained for devices under a *testing mode operation*, it can be noted that a ΔT lower than 50°C should be expected. As a

[1] A real forced convection in the device should include an air flow on top and below the device.

future work, the design of the devices as energy harvesters should be improved to achieve a higher ΔT through a tailored structure for forced convection.

Figure 4.34 shows the detail of each power curve measured. The evolution of the thermoelectric power generated by the four devices as the temperature in the hot-plate increases can be observed in Figure 4.35. Polynomial fits of the thermoelectric power curves generated by the devices are given since the original curves, also shown, did not present a perfect parabolic shape. This was due to the forced convection on top of the device, which interfered with the temperature stabilization control of the hot-plate.

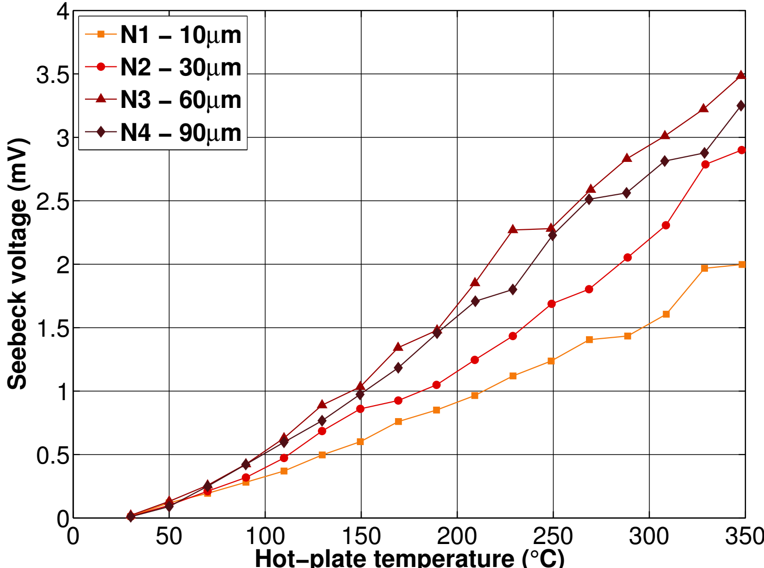


Figure 4.33: Seebeck voltage vs hot-plate temperature measured in the four devices shown in Figure 4.9 - The results obtained were similar for the N2, N3 and N4 devices.

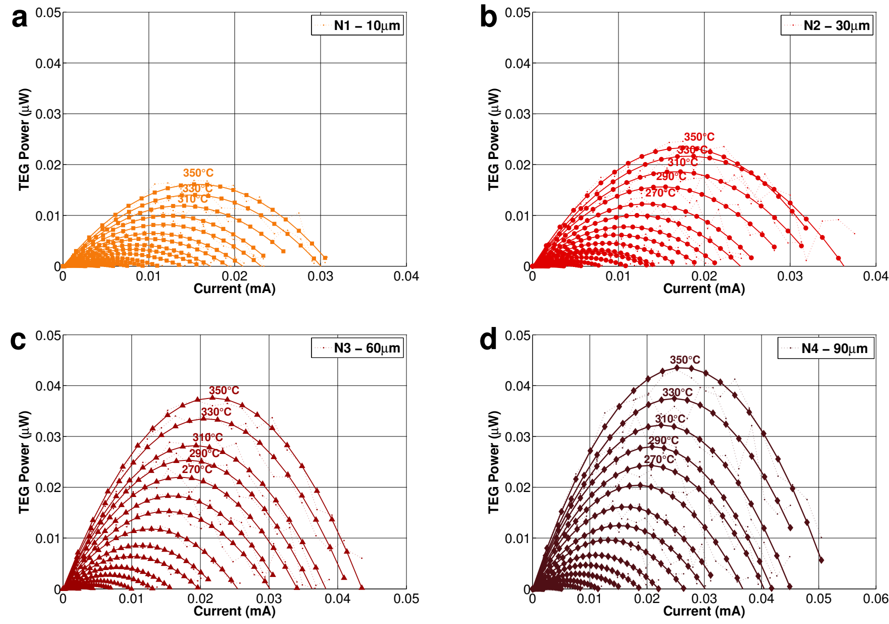


Figure 4.34: Thermoelectric power curves measured for the N1 (a), N2 (b), N3 (c) and N4 (d) devices for the different temperatures set in the hot-plate - Only 5 temperatures are labeled in the graphs for illustration purposes.

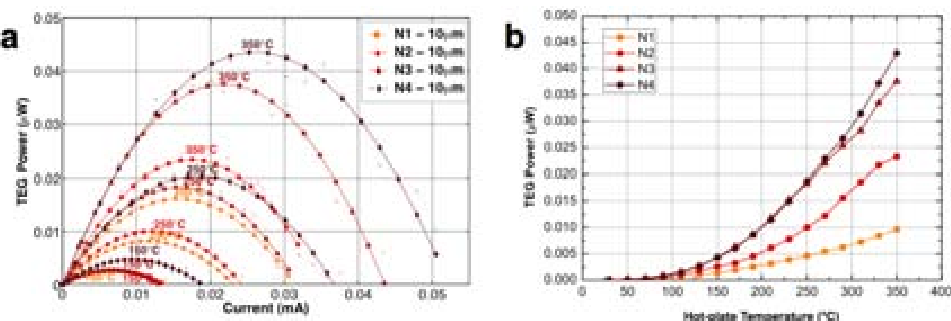


Figure 4.35: Evolution of the thermoelectric power generated by the N1, N2, N3 and N4 devices employing a *harvesting mode* for different hot-plate temperature set points - (a) Generated voltages were measured as a function of current for different temperatures set at the hot-plate of the linkam chamber. Only three T_{HP} set points (150, 250 and 350°C) are shown for illustration purposes. (b) A maximum generated power of 43 nW for a hot plate temperature of 350°C was achieved with the N4 device

4.4 Discussion & summary

The enhanced performance of thermoelectric microgenerator structures by means of transversally linked Si NWs arrays has been presented. This new design further exploits the 3D lateral growth of VLS-CVD Si NWs while preserving their electrical connectivity. Consecutively bridging multiple ordered Si NWs arrays has been shown to be a design solution that overcomes the limitation of the maximum temperature difference attainable across the microgenerator. In the traditional vertical thermocouple configuration this limitation is much harder to overcome since it is a packaging and a technologically-limited parameter.

In this second generation of μTEGs, Seebeck voltage and power output values of up to 60 mV and 14.4 μW respectively were measured for a single thermocouple at a temperature difference of 300K. Moreover, it was observed that increasing the nanowire "length" did not compromise the intrinsic resistance of the thermocouple, which remained constant for the different bridged arrays of Si NWs.

The thermoreflectance technique was used to verify the temperature distribution in the structures and, specifically, to ensure that the increment in the temperature of the cold part remained small (2% variation) when compared with the dissipated temperatures in the hot part of the device under a *testing mode* operation.

In addition, a differential method was employed to roughly estimate a fairly low thermal conductivity for Si NWs arrays (κ = 0.21W/mK). Although an increment of the thermal conductivity with temperature was observed, the results obtained were coherent when compared with the thermal conductivity of bulk silicon and air. Nevertheless, the thermal contact resistances which could be present at the different interfaces between bulk silicon and Si NWs arrays might have caused an underestimation of the intrinsic thermal conductivity of silicon nanowires. From the material perspective, the quasi-epitaxial growth of the Si NWs would lead to the lowest thermal contact resistance possible, but we cannot assure a zero value for it. Also we have not considered the effect on heat flow of the physical constriction of going from 3D to 1D silicon, which might behave as an additional thermal contact resistance. It must be said that, although the thermal contact resistance issue undermines the intrinsic thermal conductivity estimation for silicon nanowires, the presence of this resistance is positive for minimizing the thermal transport between the hot and cold regions of the device.

A comparison between the device developed throughout this work and the state-of-the-art thermoelectric microgenerators is difficult to accomplish since the microstructures presented in this thesis correspond to a single thermoelement (not to a complete microgenerator consisting of several units) and the integration of several thermoelements is still pending. In this direction, vertical stack of units, smaller thermoelements (after removing the heater included for the *testing mode*) and size optimization will lead to higher integration.

Despite this, table 4.1 shows a comparison between the commercially available thermoelectric microgenerators described in Chapter 1 and the thermoelements developed in this work. Power densities were calculated by dividing the output power values by the area of the device in each case (1 mm^2 for the thermoelement developed in this work).

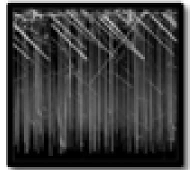
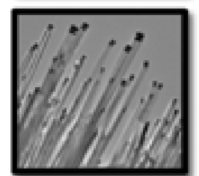
Company	**Thermoelectric material**	**Units**	**Power (μW/mm^2)**	**ΔT (K)**
DTS	$(Bi_{0.25}Sb_{0.75})Te_3/Bi_2(Te_{0.9}Se_{0.1})_3$	2250	0.025	5
JPL-NASA	$(Bi_{1-x}Sb_x)_2Te_3/Bi_2Te_3$	63	0.346	1.25
Micropelt	Bi_2Te_3	12	0.6	5
Micropelt	Bi_2Te_3	540	36.3[a]	5
Nextreme	Bi_2Te_3-Sb_2Te_3	N/A	146.6[b]	10
Infineon	Poly-Silicon	16000	0.016	10
HSG-IMIT and Kundo	Si/Al	1000	0.09	10
NUS	Top-down Si NWs	162	0.00006[c]	0.12
Dávila *et al.*	**Bottom-up Si NWs**	**1**	**0.23**	**50**
Dávila *et al.*	**Bottom-up Si NWs**	**1**	**14.4**	**300**

Table 4.1: Comparison of the results obtained in this work with existing thermoelectric microgenerators - Thermoelectric microgenerators developed by different companies and research groups. [a]Simulated power output. [b]Taken from a preliminary data sheet. [c]Not a commercially available product.

The generated output power of devices based on V-VI semiconductor compounds is clearly higher than those generated for Si-based μTEGs (including the one developed for this work). However, the thermoelement fabricated in this thesis is well positioned when compared to other Si-based devices. Additionally, the optimization of the design and of the nanowire growth employed could lead to the improvement of the power output generated by the thermoelements through higher densities, smaller diameters and rougher nanowires. This optimization, added to the possibility of overcoming the thermal constrains observed in vertical μTEG configurations (limited ΔT), due to a planar device architecture, opens excellent perspectives for the successive generations of the device. Moreover, compared to μTEGs based on

V-VI semiconductors, the device developed in this work is compatible with standard microtechnology processes and employs nanostructured silicon as the thermoelectric material, which is clearly advantageous from an environmental-friendly and economic point of view (silicon is the second most common element in the Earth's crust).

Conclusions

The work developed in this thesis presents, for the first time, a proof-of-concept novel design, monolithically integrated in silicon, of a planar *uni-leg* thermoelectric microgenerator based on the implementation of dense arrays of silicon nanowires as the thermoelectric material. A basic thermocouple element has been fabricated using traditional microtechnology techniques and taking advantage of the promising thermoelectric properties of silicon nanowires previously reported in the literature.

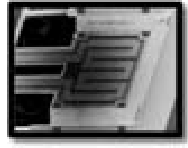
Large-scale integration of Si NW-based devices still remained a challenge to date due to the compatibility difficulties between the 3D growth of nanowires and the typical 2D planar architecture of microdevices, making the electrically accessibility to Si NWs a critical parameter. In this study, by using top-down silicon micromachining, an appropriate device geometry, and the VLS-CVD technique for the controlled lateral growth of nanowires, well-ordered bottom-up Si NWs have been monolithically integrated overcoming spatial constraints in electrically accessible structures.

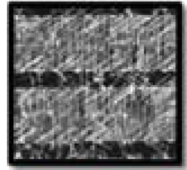
Silicon nanowires dense arrays (20 NWs/μm^2) were successfully implemented in thermoelectric microstructures by using the VLS-CVD growth method. The growth arrays consisted of nanowires with diameters of 50–100 nm and lengths of 10 μm giving rise to thermocouples with an internal electrical resistance of 60 Ω and an estimated thermal conductivity of $\kappa = 0.21$ W/mK in air and at room temperature.

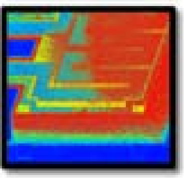
The novel thermoreflectance technique was used along this study to measure the temperature distribution in the structures. This technique served as a tool to verify the temperature increments in the hot and cold parts of the devices and to

compare the mean temperatures of selected regions, validating in this way that the nanowire ensemble served as a good thermal barrier. A thermoreflectance set-up was implemented at the IMB-CNM improving the facilities and know-how of the institute.

A first generation of microgenerators served as proof-of-concept devices. The fabricated thermocouple elements were characterized under both forced thermal gradients and harvesting operation conditions. The mechanically robust Si NWs ensemble showed to be a good thermal barrier and high electrical conductivity path between the hot and cold silicon parts of the device, having an effective thermal conductivity low enough to let a temperature difference to build-up across the microdevice and generate a Seebeck voltage when submitted to a thermal gradient. Limitations in performance were found due to the finite size length achievable by silicon nanowires, which limited the ΔT, and compatibility problems associated to the aggressive conditions of the silicon nanowire growth method.







The compatibility issues were successfully overcome by controlling the metal and passivations layers comprised in the device. A comprehensive study on this optimization is presented.

A second generation of microgenerators with enhanced performance reached by transversally linking several Si NWs arrays has been demonstrated. In order to increase the thermal gradient attainable across the device and therefore its performance, limited by the nanowires length, microstructures composed by multiple ordered arrays consecutively bridged by transversal microspacers have been fabricated, adapting and exploiting the 3D lateral growth of VLS Si NWs. This new set of devices yielded a maximum power density of 14.4 μW/mm^2 for a single thermoelement at a ΔT of 300K with a Seebeck voltage of 60 mV.

In summary, the study presented throughout this thesis lays the technological foundation for the development of efficient thermoelectric microgenerators fully integrated in silicon and based on nanostructured materials, in this case silicon nanowires. From the author's point of view, this thesis represents not only a significant advance in thermoelectric microgeneration but in the integration of silicon nanowires towards the development of nanowire-based devices that exploit the outstanding properties given by the nanoscale dimension.

Ongoing & Future work

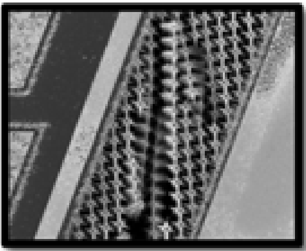
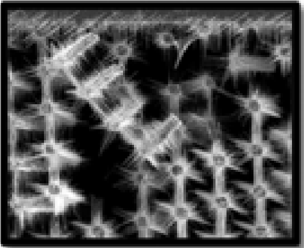
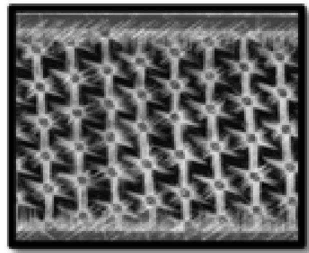
Following the investigation described in this thesis, a number of experimental procedures (still ongoing) and parallel projects have been initiated. This section highlights some of the most important from the author's point of view.

The most important aspect to cover in the near future is the optimization of the silicon nanowire growth method at a wafer-level. This will show the scalability of this technology and its feasibility for industrial implementation. This will be done in collaboration with IREC (Catalonian Institute for Energy Research) that recently acquired a CVD equipment for large-area silicon nanowires growth (4" wafers).

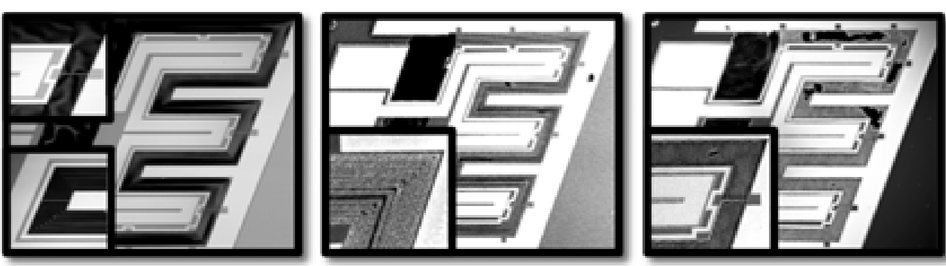
Another important issue to cover is the probe of the capability of connecting the microgenerators in series or parallel. This will open a new avenue for covering a wide range of applications.

In addition, a list of **technological enhancements** focused on solving drawbacks encountered during this thesis are in progress. The most important being:

a) Pillars misalignment. In order to solve the misalignment of pillars in devices containing microspacers to enhance the thermoelectric power output, structures have to be redesigned and characterized. For this purpose, a new mask layout is being designed according to the dimensions of the observed misalignments.

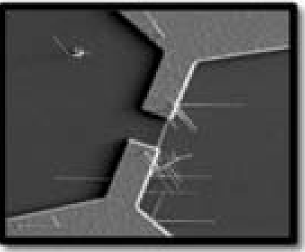
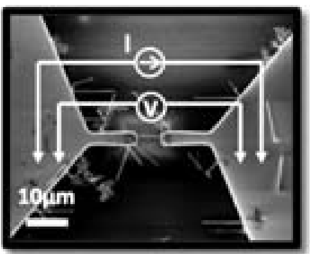




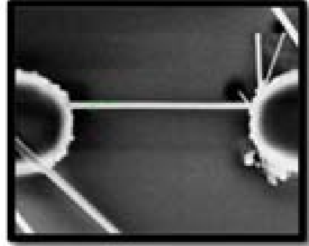
b) Interdigitated structures. Interdigitated silicon suspended structures have been also designed to maximize the contact area of the thermoelectric material and improve the power output obtainable for a given temperature difference. These designs also contained wider trenches with several microspacers as described in Chapter 4. Nevertheless, even though arrays of silicon nanowires have been grown in these structures, the characterization of these devices has not been concluded due to doping issues encountered during the last batches of nanowire growth processes.



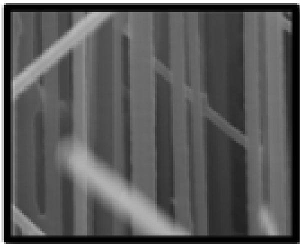
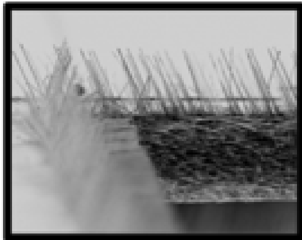
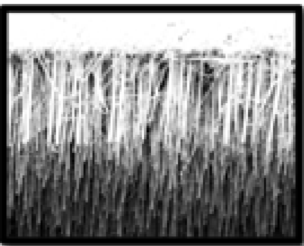
Finally, there are different aspects to cover in future work related to a more accurate **characterization of the fundamental properties** of nanowire arrays:

a) Contact resistance. For this purpose, electrical test structures have been designed and fabricated. The aim is to measure the contact resistance between the silicon nanowire and the silicon sidewalls of the structures by means of the TLM method. Test structures bridged by individual silicon nanowires with different lengths have been fabricated. The growth of individual silicon nanowires has been achieved through a colloidal deposition method. By using a thin polyelectrolyte layer, gold colloids can be electrostatically attracted to and immobilized on the substrate to act as seeds for Si nanowires grown by the VLS synthesis [143]. Sparser and somewhat thinner nanowires can be obtained with this method since colloid nanoparticles (in this case Au) are commercially available with diameters ranging from 2 to 250nm [73]. However, simultaneous control over the size, position, and epitaxial growth is more difficult to achieve. Although the growth of individual silicon nanowires of different lengths, with a uniform diameter and grown under exactly equal conditions entails a technological challenge, a first batch of structures has been designed and fabricated. Like in the interdigitated structures, doping issues are postponing their final characterization.

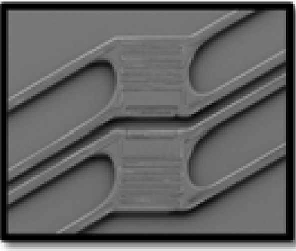
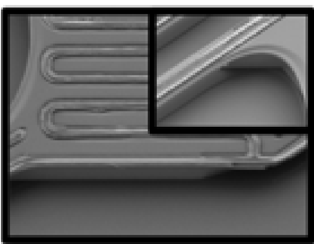
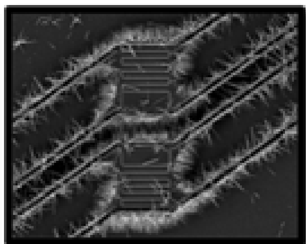





b) Nanowires morphology. Thinner and rougher nanowires than the ones used in this study are expected to exhibit better thermolectric properties. A fine-tunning of the galvanic displacement method employed in combination with sacrificial oxidation of the silicon nanowires and oxide etching in HF could reduce the nanowire dimensions. Strong doping is expected to provide rougher NWs surfaces.

c) Thermal properties. The characterization of the thermal properties of the silicon nanowires synthesized at the IMB-CNM facilities is still an ongoing project. Specific thermally isolated structures have been fabricated and silicon nanowires have been grown as it is explained in Appendix E. Nevertheless, the optimization of the growth of silicon nanowires in these type of structures is currently underway.

Scientific contributions

Publications

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, M. Salleras, C. Calaza, A.San Paulo, L. Fonseca, *Silicon nanowire arrays as thermoelectric material for a power microgenerator*, Journal of Micromechanics and Microengineering, 21 (2011), pp 104007.

- D. Dávila, A. Tarancón, D. Kendig, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, C. Cané, I. Gràcia, E. Figueras, J. Santander, A.San Paulo, A. Shakouri, L. Fonseca, *Planar thermoelectric microgenerators based on silicon nanowires*, Journal of Electronic Materials, 40 (2011), pp 851-855.

Conferences

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, L. Fonseca. *Development of an energy harvesting microdevice using silicon nanowire arrays as thermoelectric material.* EMRS Spring Meeting. Nice, France (May 2011). *Poster presentation*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, L. Fonseca. *Thermoelectric power microgenerator based on silicon nanowires dense arrangments as thermoelectric material.* MRS Spring Meeting. San Francisco, CA, USA (April 2011). *Oral presentation*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, L. Fonseca. *Integration of silicon nanowire arrays*

as thermoelectric material into thermoelectric energy harvesting microdevices. Smart Systems Integration. Dresden, Germany (March 2011). *Oral presentation*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, L. Fonseca. *Thermoelectricity generation using silicon nanowires arrays: harvesting energy from the environment.* Conference on Electron Devices. Palma de Mallorca, Spain (February 2011). *Oral presentation (Invited talk)*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, D. Kendig, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, A. Shakouri, L. Fonseca. *Silicon nanowire arrays as thermoelectric material for a power microgenerator.* PowerMEMS. Leuven, Belgium (December 2010). *Oral presentation*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, D. Kendig, N. Sabaté, M. Salleras, C. Calaza, A. San Paulo, A. Shakouri, L. Fonseca. *Planar thermoelectric microgenerators based on silicon nanowires.* International Congress on Thermoelectrics. Shanghai, China (May 2010). *Poster presentation*

- D. Dávila, A. Tarancón, M. Fernández-Regúlez, M. Sansa, N. Sabaté, A. San Paulo, I. Gràcia, C. Cané, L.Fonseca. *Implemetation of silicon nanowire arrays in microfabricated devices for thermoelectric power generation.* MRS Spring Meeting. San Francisco, CA, USA (April 2010). *Poster presentation*

Patents

- *Dispositivo de generación termoeléctrica, generador termoeléctrico y método de fabricación de dicho dispositivo de generación termoeléctrica.*

  Inventors: A. Tarancón, D. Dávila, N. Sabaté, A. San Paulo, M. Fernández-Regúlez, L. Fonseca.

  Patent ref: PCT/ES2011/07021.

Projects

- μ**GENTERM**: Thermoelectric energy harvesters based on micro/nano technologies for autonomous system development.

  Granted by: Spanish Ministry of Science and Innovation (TEC-2010-20844-E).

- **EXPLORA**: Estudio de la viabilidad de microgeneradores termoélectricos basados en nanohilos de silicio.

  Granted by: Spanish Ministry of Science and Innovation (TEC-2008-03255-E).

Appendix A

Compatibility of silicon nanowire growth with multilayer configuration of the designed microgenerators

As it was described in Chapter 2, several compatibility issues between the multilayer configuration of the device and the growth process of silicon nanowires arose during the development of this work. The aim of this appendix is to describe the comprehensive study performed in order to overcome these issues.

A.1 Stress analysis of the as-deposited device layers

As a first attempt to solve the delamination problems encountered in the devices after Si NW growth (see section 3.2.4.1), a stress analysis of all the layers comprised in the device was performed. Layers were analyzed both individually and combined in multilayers. The study involved depositing the different layers employed for the fabrication of the device (Si_3N_4, SiO_2, Ti/Pt, Ti/W/Pt) on standard 4" wafers and performing a stress analysis of the thin films using the bending plate method [144, 145] and a Dektak® Stylus profiler.

The measurement technique consists in measuring the curvature of the substrate

prior to deposition and then, once the layers were deposited, measuring the substrate curvature along the same trace. This stress analysis allows to calculate stress in a deposited thin film layer, based upon the change in curvature and material properties of the film and substrate (the key parameter is the substrate radius of curvature before and after deposition). If the height of the substrate is expressed as a continuos function of distance along the substrate, $y = f(x)$, then the radius of curvature at any point may be calculated as:

$$R(x) = \frac{(1 + y'^2)^{\frac{3}{2}}}{y''} \tag{A.1}$$

where $y' = dy/dx$, and $y'' = d^2y/dx^2$. Assuming an initially flat substrate, the stress in the film can then be calculated as:

$$\sigma = \frac{1}{6}\left(\frac{1}{R_{post}} - \frac{1}{R_{pre}}\right)\frac{E}{(1-\upsilon)}\frac{t_s^2}{t_f} \tag{A.2}$$

where σ is the stress in the film (after deposition), R_{pre} is the substrate radius of curvature before deposition, R_{pos} is the substrate radius of curvature after deposition, E is the Young's modulus, υ is the Poisson's ratio, t_s is the substrate thickness and t_f is the film thickness. Each scan is fit with a 5th order polynomial by the method of least squares. The fit to each scan is then differentiated to produce the function $y'(x)$ and again to produce $y''(x)$. These functions are substituted into equation A.1 to calculate the radius of curvature as a function of scan position before and after deposition. The two radii are substituted into equation A.2 to calculate pre-deposition and post-deposition stress. The difference between these values is the film induced stress. Negative values of stress are compressive (convex surface); positive values are tensile (concave surface).

Two stress measurements were performed at 90° angles to achieve a more complete image of the substrates distortion. Table A.1 lists the cases of study. Wafers 1 to 7 were measured all along the wafer but, since the profiler allowed only 5 cm-long traces, measurements were performed in two parts, the rest of the wafers were measured with a single 5 cm-centered trace. In wafers 8 to 13, the first two layers, the pedestal oxide layer and the LPCVD Si_3N_4 layer, were deposited to simulate a protective and isolation layer (for the heater) respectively. A W layer was added

as an intermediate barrier metal between the adhesion layer and the metal layer in wafers 3, 7, 10, 11 and 13.

A list with all the data collected along the stress analysis carried out is presented to set a precedent in case stress-related issues are confronted in a future work. Moreover, the results of this study helped to better understand the stress of such a complicated multilayer devices as the ones fabricated for this thesis. In addition, the results obtained are now part of the know-how of the IMB-CNM.

Wafer	**Layer**	**Layer thickness (Å)**	**Stress 0° (MPa)****	**Stress 90° (MPa)****
1	Ti/Pt [1]	250/2500	C - 440	C - 552
	Ti/Pt [2]	250/2500	C - 505	C - 486
2	Ti/Pt[1]	250/2500	C - 498	C - 526
	Ti/Pt[2]	250/2500	C - 548	C - 464
2	$Ti/Pt/SiO_2/Si_3N_4$[1]	250/2500/3000/2000	C - 15	C - 20
	$Ti/Pt/SiO_2/Si_3N_4$[2]	250/2500/3000/2000	C - 8	C - 36
3	Ti/W/Pt[1]	250/500/2500	C - 524	C - 909
	Ti/W/Pt[2]	250/500/2500	C - 931	C - 899
4	SiO_2[1]	3000	C - 368	C - 423
	SiO_2[2]	3000	C - 356	C - 437
5	Si_3N_4[1]	2000	T - 335	T - 235
	Si_3N_4[2]	2000	T - 331	T - 243
6	SiO_2/Si_3N_4[1]	3000/2000	C - 112	C - 153
	SiO_2/Si_3N_4[2]	3000/2000	C - 101	C - 156
7	Ti/W/Pt[1]	250/500/2500	C - 895	C - 887
	Ti/W/Pt[2]	250/500/2500	C - 914	C - 878
7	$Ti/W/Pt/SiO_2/Si_3N_4$[1]	250/500/2500/3000/2000	C - 255	C - 274
	$Ti/W/Pt/SiO_2/Si_3N_4$[2]	250/500/2500/3000/2000	C - 266	C - 275
8	*$SiO_2/Si_3N_4/Ti/Pt$	200/1175/250/2500	C - 101	C - 63
9	*$SiO_2/Si_3N_4/Ti/Pt$	200/1175/250/2500	C - 27	C - 6
	*$SiO_2/Si_3N_4/Ti/Pt/SiO_2/Si_3N_4$	200/1175/250/2500/3000/2000	T - 115	T - 111
10	*$SiO_2/Si_3N_4/Ti/W/Pt$	200/1175/250/500/2500	C - 450	C - 428
11	*$SiO_2/Si_3N_4/Ti/W/Pt$	200/1175/250/500/2500	C - 455	C - 418
	*$SiO_2/Si_3N_4/Ti/W/Pt/SiO_2/Si_3N_4$	200/1175/250/500/2500/3000/2000	C - 77	C - 131
12	*$SiO_2/Si_3N_4/Ti/Pt$	200/1175/100/2500	C - 142	C - 100
13	*$SiO_2/Si_3N_4/Ti/W/Pt$	200/1175/100/500/2500	C - 497	C - 457
14	Ti/Pt	100/2500	C - 489	C - 442
15	Ti/W/Pt	100/500/2500	C - 1013	C - 981

Table A.1: Stress analysis of the different layers comprised in the first generation of devices - Wafers 1 to 7 were measured in two parts: [1] from top to the center of the wafer and [2] from the center to the bottom of the wafer. *Wafers with a pedestal oxide layer and a LPCVD Si_3N_4 layer. ** C=Compresive stress and T=Tensile stress.

A.2 Stress analysis of the device layers after high temperature annealing

After the stress analysis, wafers were subjected to an annealing process similar to the one used for the growth of VLS silicon nanowires. The heat treatment under a reducing atmosphere started at 350°C, wafers were then heated up to 700°C (5°C/min ramp rate) keeping this temperature for one hour to finally cool the wafers down to 350°C. Figure A.1 shows optical images of the results for wafers 2, 7, 9 and 11 (all including a passivation layer of SiO_2/Si_3N_4 over the metal layer); the rest of the wafers presented no delamination or defects.

After observing the bad adherence of the passivation layer, the adhesion layer was varied from Ti to Cr. These adhesion layers were also deposited on both sides of the Pt layer, i.e. adhesion layer/platinum/adhesion layer, to improve the adhesion of the passivation layer. In addition, it was decided to test the possibility of using only a single 5000 Å-thick SiO_2 layer as the passivation layer instead of the SiO_2/Si_3N_4 bilayer (wafer 7). Table A.2 shows the results obtained for this batch of wafers after subjecting them to the annealing process described before. Once again, the metal layer in wafers without passivation had a good adhesion, while in the rest of the wafers the passivation detached (Figure A.2). This indicated that adding an extra adhesion layer after the Pt did not help to solve the delamination process. However, it was observed that wafer 7 had a good aspect in general, indicating that SiO_2 as a single passivation layer worked better.

Wafer	Layer	Layer thickness (Å)	Adhesion
1	Cr/Pt	250/2500	Good
2	$Cr/Pt/SiO_2/Si_3N_4$	250/2500/3000/2000	Bad
3	Cr/Pt/Cr	250/2500/250	Good
4	$Cr/Pt/Cr/SiO_2/Si_3N_4$	250/2500/250/3000/2000	Bad
5	Ti/Pt/Ti	250/2500/250	Good
6	$Ti/Pt/Ti/SiO_2/Si_3N_4$	250/2500/250/3000/2000	Bad
7	$Ti/Pt/SiO_2$	250/2500/5000	Good

Table A.2: Wafers fabricated to improve the adhesion of the passivation layer - Bad performance was observed in wafers including a SiO_2/Si_3N_4 passivation layer.

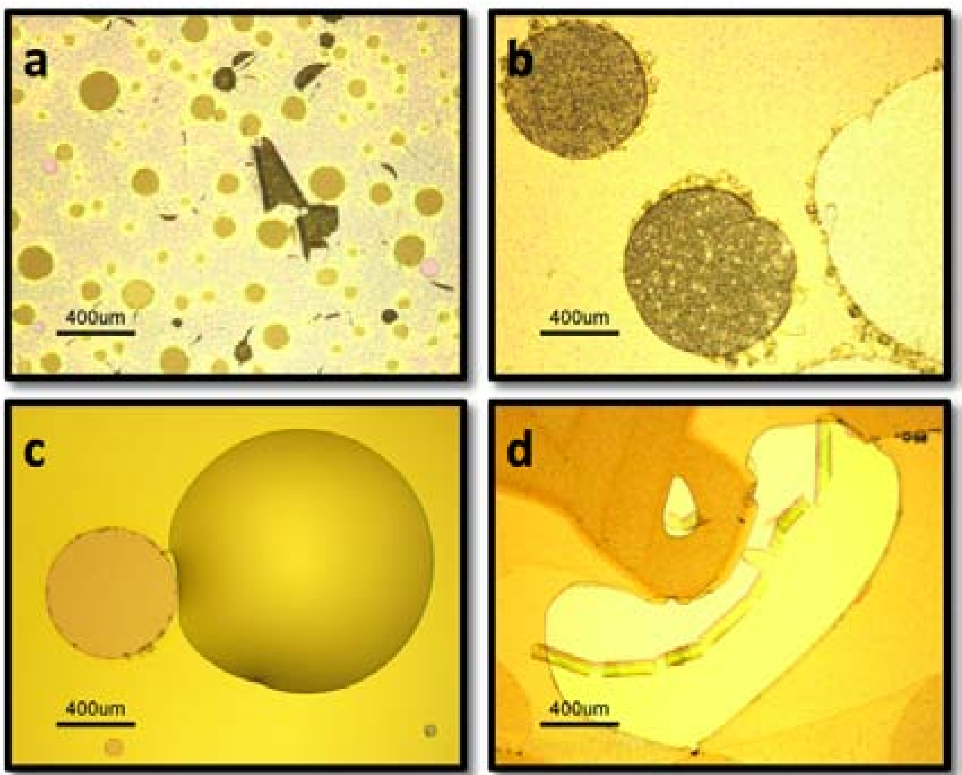


Figure A.1: Optical images of wafers 2, 7, 9 and 11 of Table A.1 after an annealing process at 700°C - The images show the bad adherence of the passivation layer whereas in the rest of the wafers of Table A.1 homogeneous layers were observed after the annealing process.

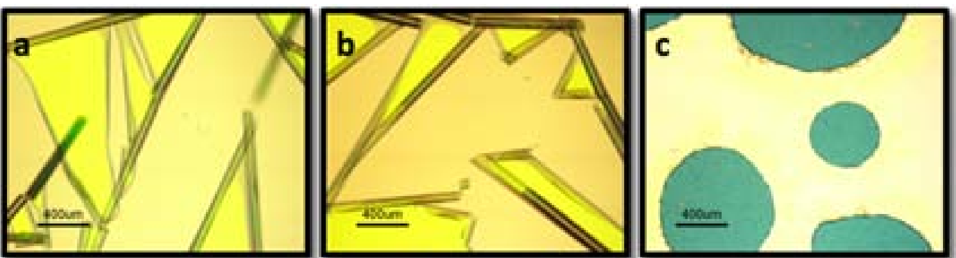


Figure A.2: Optical images of wafers 2, 4, and 6 of Table A.2 after an annealing process at 700°C - The images show the delamination of the passivation layer.

A.3 Stress analysis of the device layers after annealing under nanowire growth conditions

Although in tests performed in sections A.1 and A.2 no delamination was observed for the metal layers without passivation, adhesion problems of this layer were observed in real devices when subjected to nanowire growth conditions. In order to determine the role of the patterning on the delamination of layers, samples with patterned heaters and metal strips both on Si and Si_3N_4 and with a single SiO_2 passivation layer were fabricated. These wafers were cut in chips to be subjected to the conditions employed for nanowire growth inside the CVD reactor.

After confirming strong delamination problems, it was decided to replace the Ti/Pt metal layer. Ta_2Si/Pt, W, Ti/W, TiW, TiW/W and Ta/Pt were considered as an alternative. The TiW alloy was formed by 10% Ti and a 90% W. Table A.3 summarizes the results obtained from this set of experiments. Ta/Pt samples were difficult to fabricate due to the stress mismatch between the metal layer and the oxide passivation layer, which did not adhere properly and detached from some zones of the sample. The rest of the samples (Ta_2Si/Pt, W, Ti/W, TiW, TiW/W) were subjected to the conditions used for the growth of VLS silicon nanowires.

Metal	**Thickness (Å)**	**Deposition process**	**Patterning process**	**Adhesion to Si***	**Adhesion to Si_3N_4***
Ta_2Si/Pt	150/2500	Sputtering	Lift-off	Bad	Good
W	1500	Sputtering	Lift/off & wet etching	Good	Good
Ti/W	300/2000	Sputtering	Lift-off & wet etching	Bad	Good
TiW	1500	Sputtering	Lift-off & wet etching	Good	Good
TiW/W	300/2000	Sputtering	Lift-off & wet etching	Good	Good
Ta/Pt	250/2500	Evaporation	Lift-off	**	**

Table A.3: Metal optimization for high temperature applications using silicon nanowires - Metals tested at 755 °C under silicon nanowire growth conditions using the VLS synthesis mechanism.
*Adhesion observed after Si NW growth process.
**Bad adhesion even before the Si NW growth process.

Samples containing metals that could be patterned either with a lift-off or a wet etching process were fabricated using both. The results obtained were the same for both processes, which means that the patterning process does not affect the adhesion or performance of the metals.

As it can be noted from the images in Figure A.3, the Ta_2Si/Pt and Ti/W layers showed a bad adherence to silicon after being exposed to the conditions of the silicon nanowire growth process, whereas the rest of the samples had a good appearance in all zones. Since the W, TiW and TiW/W samples did not present any problem during fabrication and had a good performance after the growth process, these three metal layers were chosen to replace the Ti/Pt layer originally used for the device. Moreover, another advantage of considering W or its alloys as the conducting layer is that this layers can be patterned using either a lift-off process or a hydrogen peroxide wet etching process, which makes the fabrication process of the device more flexible.

In addition, the sheet resistance, contact resistance and TCR of the metal layers that showed the best performance (W, TiW and TiW/W) were measured in order to compare them to the original Ti/Pt layer, since heaters and electrical contacts for the devices had already been designed considering Pt for it.

Table A.4 shows a comparison of the results obtained for the three metal layers. The sheet resistance and contact resistance were measured in samples as-fabricated whereas the TCR was measured in samples subjected to the conditions of the Si NW growth process. In order to have an estimation of the contact resistance between each of these material layers and silicon, test samples were prepared. Metal contacts were patterned on silicon by using a PDMS shadow mask trying to follow the TLM architecture. The values obtained were used to decide which metal layer would be employed for the following generation of devices. TCR values were measured following the method explained in section 2.4.3.2 using the samples shown in Figure 3.19 for the W, TiW and TiW/W metal layers.

Metal	**Thickness (Å)**	**Sheet resistance* (Ω/□)**	**Contact resistance* (Ω)**	**TCR** (ppm/°C)**
Ti/Pt	250/2500	1.09	649	1390
W	1500	1.02	71	1305
TiW	1500	3.13	55	386
TiW/W	300/2000	0.90	490	1029

Table A.4: Sheet, contact resistance of metals studied in this work -
(*) Resistances measured in as-fabricated samples.
(**) TCR values obtained in samples exposed to the conditions of the Si NW growth process at 755 °C.

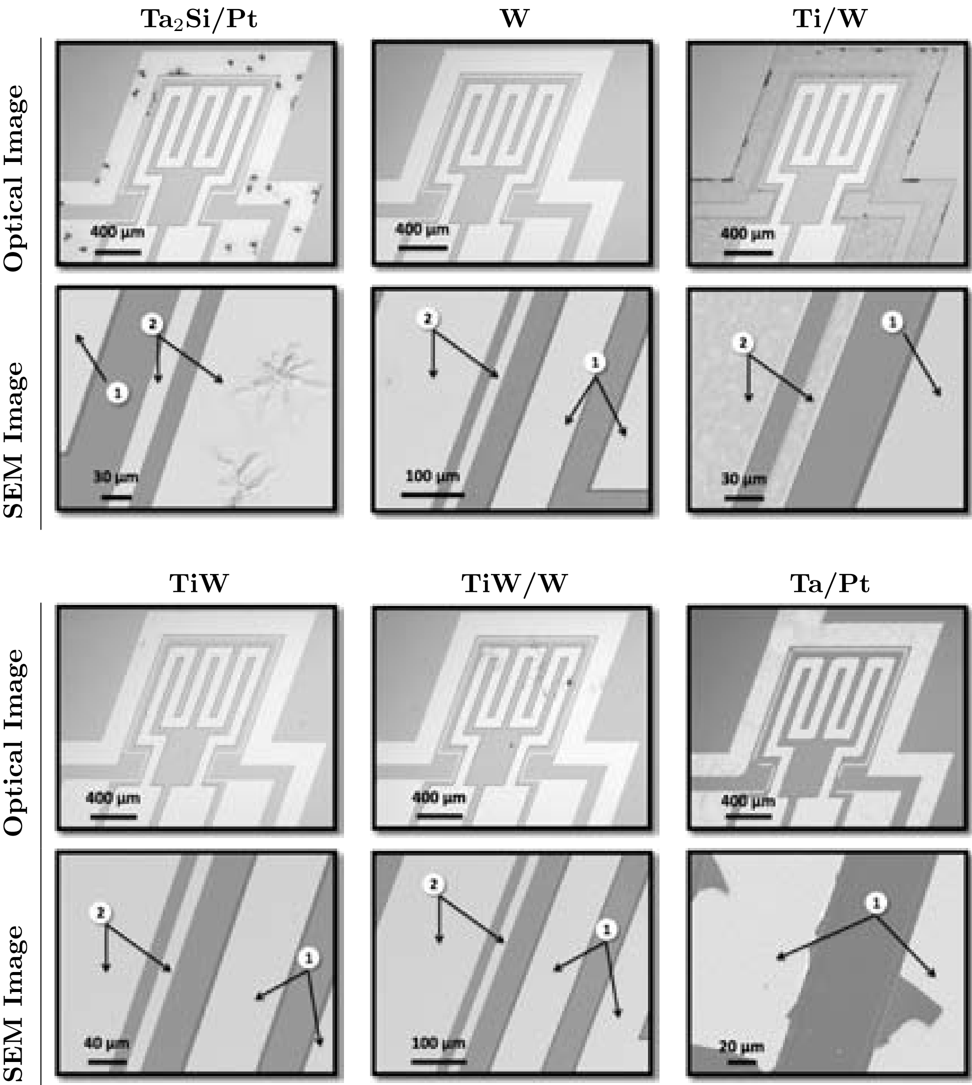


Figure A.3: Optical and SEM images of device samples with different metal layers - Results obtained after exposing the samples to a silicon nanowire growth process using the VLS synthesis mechanism. The numbers in the SEM images refer to the area on which the layer is deposited: (1) for layers on silicon and (2) for layers on Si_3N_4.

As it can be observed from Table A.4, TiW/W and W showed to have a sheet resistance very similar to Ti/Pt while in the TiW layer this value triplicates. The contact resistance varies from metal to metal, showing low values for the W or TiW layers. For simplification, W was preferred over Ti/W. Tungsten showed a TCR and sheet resistance very similar to Ti/Pt without compromising the contact resistance (an important parameter for this work since this resistance is connected in series with the thermoelectric material). Moreover, after selecting W as the metal layer, it was necessary to measure the contact resistance in accurate test structures to ensure low values. For this purpose, the following generation of devices included TLM test structures in all samples, which allowed to accurately measure the contact resistance in each sample if necessary. Also, the contact resistance and TCR values for W after the Si NW growth process were once again measured to observe whether subjecting samples to a complete growth process could alter the adhesion of the layer. A contact resistance of 4.87 Ω and a TCR of 2000 ppm/°C were obtained. Since a remarkable deviation from the results obtained in table A.4 was observed, it was decided to measure the TCR of W in each characterized sample in order to improve the accuracy.

Appendix B

Orientation issues of (110) Silicon-On-Insulator (SOI) wafers

Throughout this thesis, several issues related to the orientation of the SOI wafers employed were solved. This Appendix presents the work performed for this purpose during the development of microgenerator structures and microplatforms for the thermal characterization of Si NWs. For the case of the microgenerator structures, SOI wafers had to be carefully selected to ensure the orientation defined in the mask layout. For the case of microstructures for thermal characterization, apart from verifying the orientation of the wafers, the orientation dependent wet-etching of the {110} and {111} planes was exploited to achieve free standing silicon microplatforms held by nitride arms.

B.1 Microgenerator structures

In Chapter 3, the importance of the orientation of the SOI wafers employed in this thesis was described. Since microgenerator devices were designed with a certain orientation in order to have a perpendicular growth of nanowires in defined (111) trenches, the starting SOI wafers had to be consistent with this requirement. However, it was observed, after several fabrication processes, that not all the acquired wafers had the desired orientation. Depending on which side of the (110) wafer is flipped down onto the oxidized (100) handle wafer during the SOI wafer bonding

process, the intersecting (111) planes will form the expected angle (70.53°) or its complementary.

To check the actual plane distribution of the acquired wafers before the fabrication of the devices, they were subjected to a short sacrificial wet etching using a mask that defined small tilted (70.53°) rectangular patterns at the edge of the wafers with the two possible orientations shown in Figure 3.10. A 1175 Åthick LPCVD Si_3N_4 layer was used as the mask for the selective etching of 3 μm of the device silicon layer of the SOI wafers. For this step, an anisotropic Tetramethylammonium hydroxide (TMAH) wet etching process was used. Figure B.1 shows the patterns etched on the wafers. It can be noticed how the patterns in Figure B.1a follow the desired orientation with which the devices along this work were designed since vertical walls are observed, whereas in Figure B.1b, the same orientation shows undesired intersecting planes.

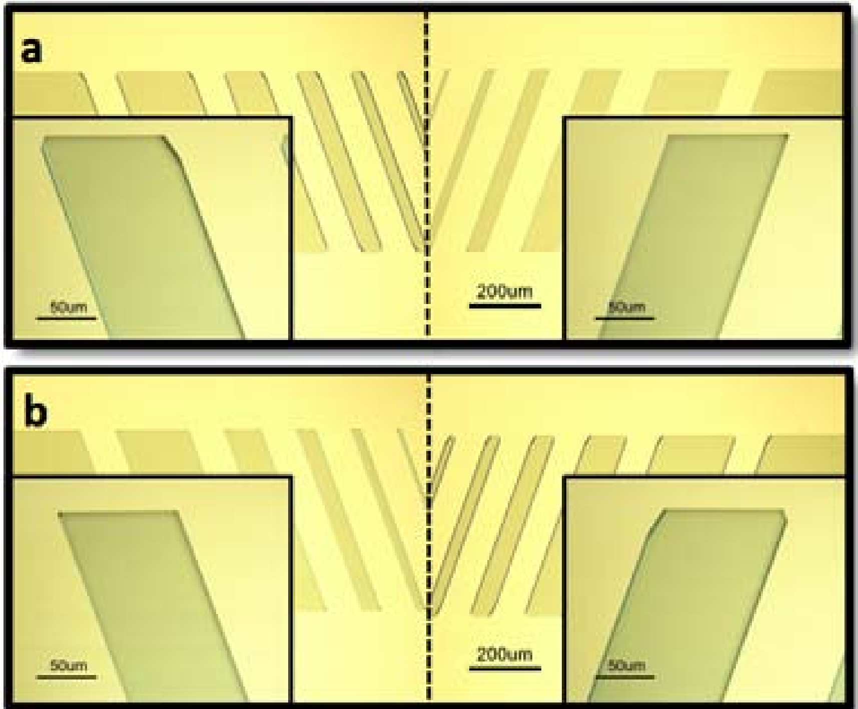


Figure B.1: Optical image of rectangles patterned in SOI wafers to observe the wafer orientation - (a) SOI wafer with the desired orientation and (b) wafer of the same batch but with the opposite direction.

B.2 Microstructures for thermal characterization

The orientation of the (110) SOI wafers employed and the different anisotropic etch rate of {110} and {111} planes played a key role in the development of microplatforms for the thermal characterization of Si NWs. The aim here was to observe how, if the defined structures were properly oriented, the {110} Si planes could be etched without affecting the {111} planes where perpendicular nanowire growth was desired. In this way, suspended silicon masses held by nitride arms were obtained (see Appendix E). Simulations were performed using a mask layout for the fabrication of free standing isolated structures in which, a silicon mass held by silicon beams was wet-etched to remove the silicon arms. For this purpose, the anisotropic crystalline etching simulation (ACES) software was employed to simulate the different sequences of silicon etching of a (110) wafer.

Figure B.2a shows the initial mask design of the simulated structure, which was tailored to observe the desired planes. The removal of the {110} planes as the etching progresses can be observed in Figures B.2 b–c. It is important to note that the simulations performed were only used to observe the etch fronts of the {110} planes and how the {111} planes are defined as the etching process progresses. The times employed for the simulations as well as the defined etching parameters differed from those finally employed for the fabrication of the structures.

Figure B.2 d shows the as fabricated device before being subjected to a 7-minute TMAH etching process at a chip-level (Figure B.2e) and at a wafer-level (Figure B.2f). The qualitative good agreement of the simulations with the results can be appreciated by comparing Figures B.2c and B.2e. The images of Figures B.2e and B.2f demonstrate how the wet etching conditions are altered by the size of the sample, and that over-etching must be carefully avoided.

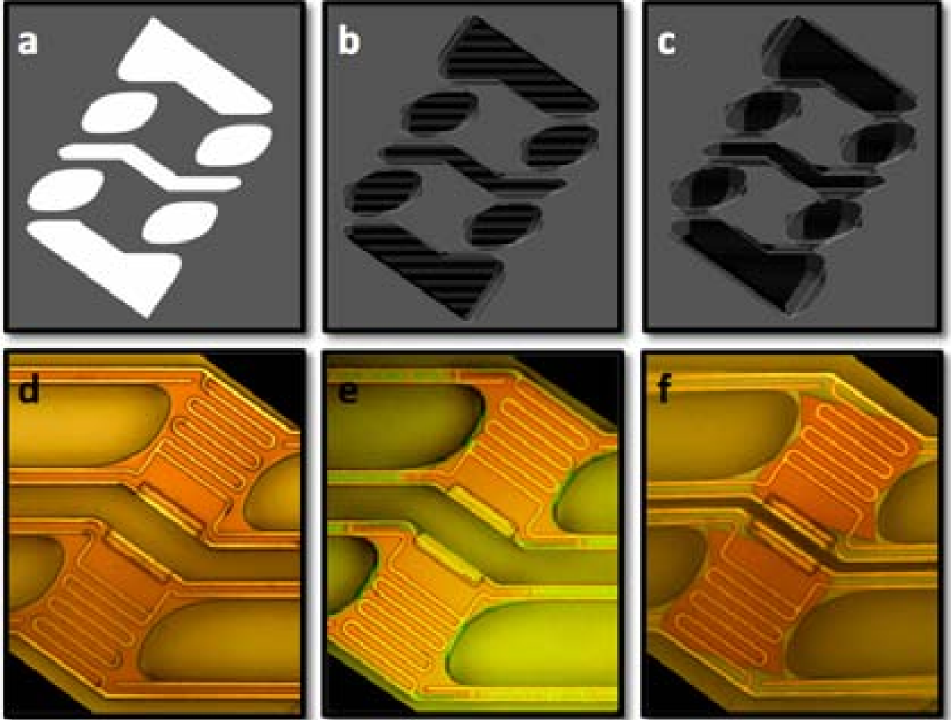


Figure B.2: Anisotropic crystalline etching simulation (ACES) & experimental results of (110)-oriented silicon beams of a suspended microstructure - (a–c) Simulations performed to observed the etch front of the {110} and {111} silicon planes of the structure. (d) Optical image of the as-fabricated structure. (e) Structure subjected to a 7-minute TMAH etching process at a chip-level. (f) Results obtained with a similar structure subjected to a 7-minute TMAH etching process at a wafer-level, which resulted over-etched.

Appendix C

Technological window for silicon nanowire growth

The integration of epitaxially grown silicon nanowires into a pre-existing device architecture demands a high level of control over the nanowire growth process. The nanowire length, diameter and growth direction should be controlled in order to achieve a well-defined nanowire morphology. The interdependency of these parameters, i.e. the growth velocity –nanowire length– and the crystallographic growth direction are diameter-dependet [73, 105, 106, 108]), together with the narrow technological window of the silicon nanowire growth process, make this method extremely sensitive to experimental conditions.

In this thesis, temperature of growth and undesired metal exposure were found to be critical parameters.

C.1 Temperature sensitivity

Figure C.1 shows an example of the narrow temperature growth window for the synthesis of well-oriented silicon nanowires. In this case, by following a defined galvanic displacement procedure, three different growth temperatures, 745°C, 755°C and 765°C, were tested while keeping the other growth conditions constant. It can be observed how, by shifting the temperature of growth by 10°C, perfectly unidirectional nanowires (Figure C.1 a–c), multi-directional nanowires (Figure C.1 d–f) or whiskers can be grown (Figure C.1 g–i).

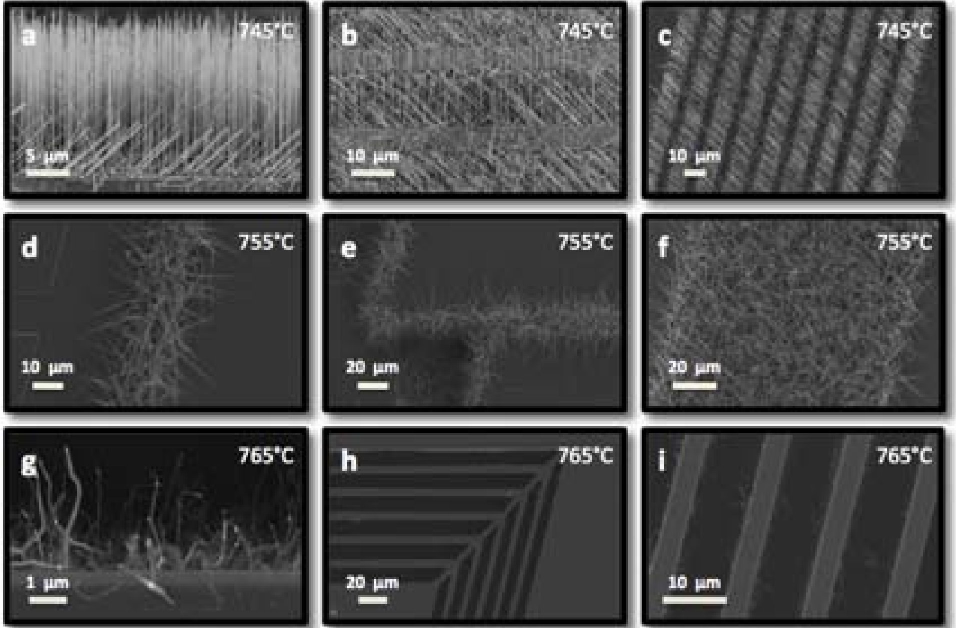


Figure C.1: Temperature sensitivity observed in the synthesis of silicon nanowires - Analysis of the influence of the temperature on the growth of silicon nanowires. Three different temperatures were tested, i.e. 745, 755 and 765°C, obtaining defined and well-oriented Si NWs (a–c), multi-directional Si NWs (d–f) and Si whiskers (g–i) for each temperature respectively.

C.2 Undesired metal exposure

Metal exposure in samples during silicon nanowire growth lead to amorphous growth of silicon nanowires in unwanted areas due to changes in the growth atmosphere. Examples of how this metal exposure, caused by a bad adhesion of the layers comprised in the fabricated devices, affected the synthesis of silicon nanowires promoting irregular growth are shown in Figure C.2.

Additionally, it was decided to perform an EDX analysis to discard the possibility of other metal sources coming from the experimental CVD set-up. Figure C.2a shows an example of a sample in which, without performing the galvanic displacement method, i.e. no Au nanoparticles are deposited, amorphous nanowire growth is observed. The EDX technique was used in this case to qualitatively and semi-quantitatively analyze the chemical composition of the sample. However, no chemical components other than those expected were found, as is shown in the

spectrum of Figure C.3.

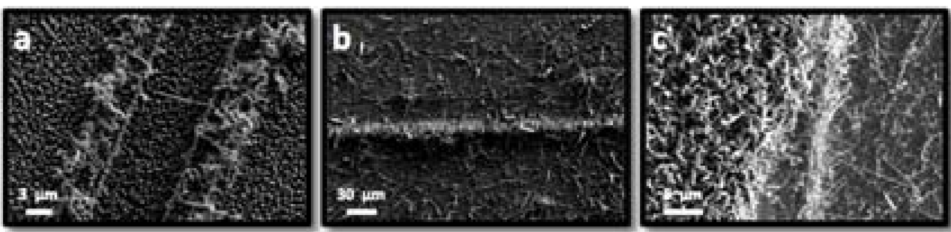


Figure C.2: Irregular nanowire growth observed derived from undesired metal exposure - Samples exposed to the nanowire growth procedure without (a) and with (b-c) Au nanoparticles yielded irregular nanowire growth in all the surface of samples.

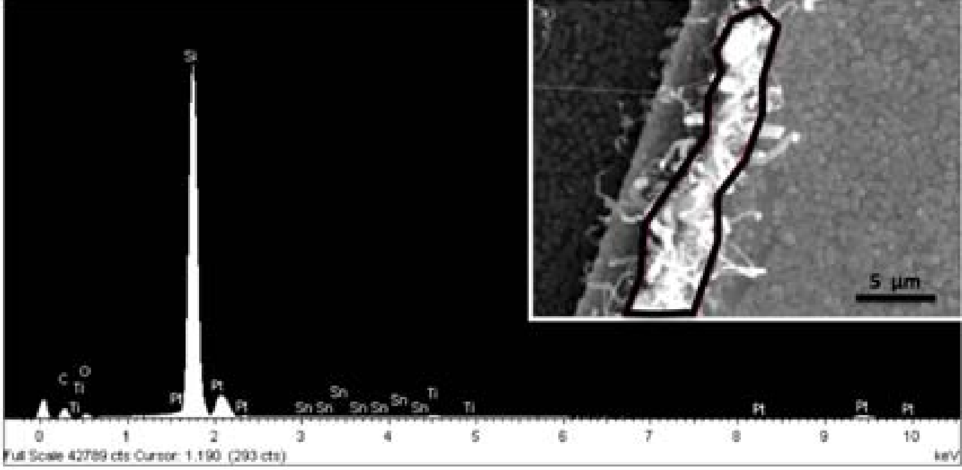


Figure C.3: EDX spectrum of the sample shown in Figure C.2a - Irregular nanowire growth was observed in a sample in which no galvanic displacement was performed. This indicates that undesired exposed metal was present before the device fabrication was optimized. The inset in the spectrum shows the analyzed region. No unexpected chemical components peaks were observed.

Moreover, as a consequence of an excess of undesired metal exposure, silicon deposition was observed even in the sample holder used for the growth of silicon nanowires. In this case, since the quantity of the material present in the holder was relatively small, μXRD was employed to ensure the absence of any external chemical component by using the grazing-incidence technique. The μXRD spectra obtained

for the silica sample holder is shown in Figure C.4. A thin film of crystalline silicon was observed, but there was no evidence of unexpected components.

Finally, after dismissing the possibility of contaminated samples, an optimization of the metal layers comprised in the device was performed following the procedure described in Appendix A. Once, this drawback was overcome, the growth conditions were optimized in order to achieve homogeneous and regular nanowire growth.

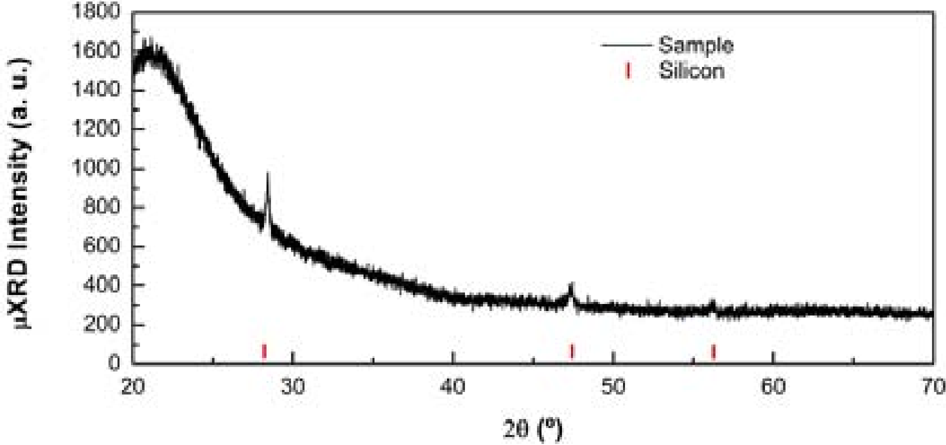


Figure C.4: μXRD spectra of sample holder after nanowire growth - Crystalline silicon layer was deposited on the sample holder after a nanowire growth process probably due to an excess of undesired metal exposed altering the growth conditions.

Appendix D

Estimation of the Si NWs array density

In this work, the occupancy factor of silicon nanowires arrays was estimated through image analysis using Matlab software. In order to obtain an estimation of the density of the Si NWs growth, a SEM image of the gold nanoparticles deposited by means of the galvanic displacement method was employed (Figure D.1a). The image was treated with Adobe Photoshop® to enhanced its contrast (Figure D.1b).

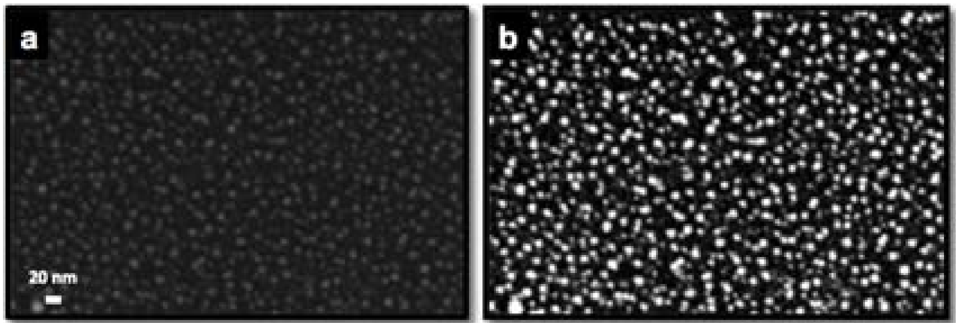


Figure D.1: Original SEM image employed for the estimation of the Si NWs array density - (a) SEM image of gold nanoparticles deposited by means of the galvanic displacement method. (b) Enhanced SEM image using Adobe Photoshop®

The nanoparticles shape was then detected by means of different algorithms (Zero-crossing, Sobel, Dewitt and Canny) obtaining Figure D.2a. Aftwerwards, since some of the nanoparticles appear to have an "open" shape, the image was

treated to connect the borders and “close” the shapes, followed by the filling of all the “hollow” nanoparticles and obtaining the image of Figure D.2b. Then, the remaining shapes were eliminated (Figure D.3a). The image of Figure D.3b shows the overlapping of the original SEM image and the processed image. As it can be observed, some nanoparticles are lost and, in some other cases, nanoparticles being close together are overlapped.

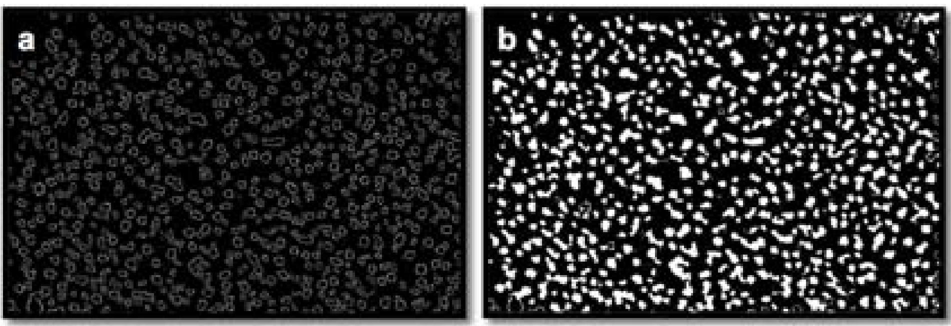


Figure D.2: Detection of the nanoparticles outline by means of digital image processing - (a) Nanoparticles shape detection. (b) Filling of hollow shapes.

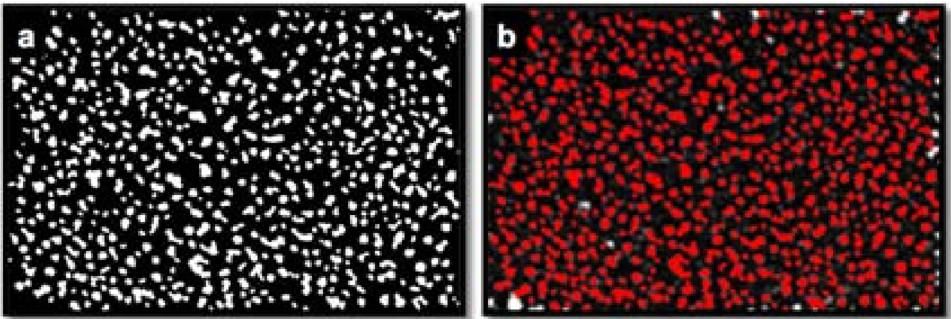


Figure D.3: Processed image showing clearly-defined nanoparticle shapes - (a) Image showing filled shapes after the removal of undefined shapes. (b) Overlapped original SEM image and processed image

The area occupied by these nanoparticles (calculated from the ratio between the pixels count and the total amount of pixels in the image) and therefore the occupancy factor, was estimated to be 21%. By using this occupancy factor and varying the nanowire radius, the density of silicon nanowires as a function of the radius can be obtained (Figure D.4). If nanowires with an average diameter of

100 nm are considered (radius of 50 nm), a nanowire density of 20 NWs/μm^2 can be calculated. Nevertheless, since the device structures fabricated throughout this work contained trenches, nanowire growth from both silicon walls can be expected, doubling in this way the calculated occupancy factor for a best case scenario, i.e. 41.72%.

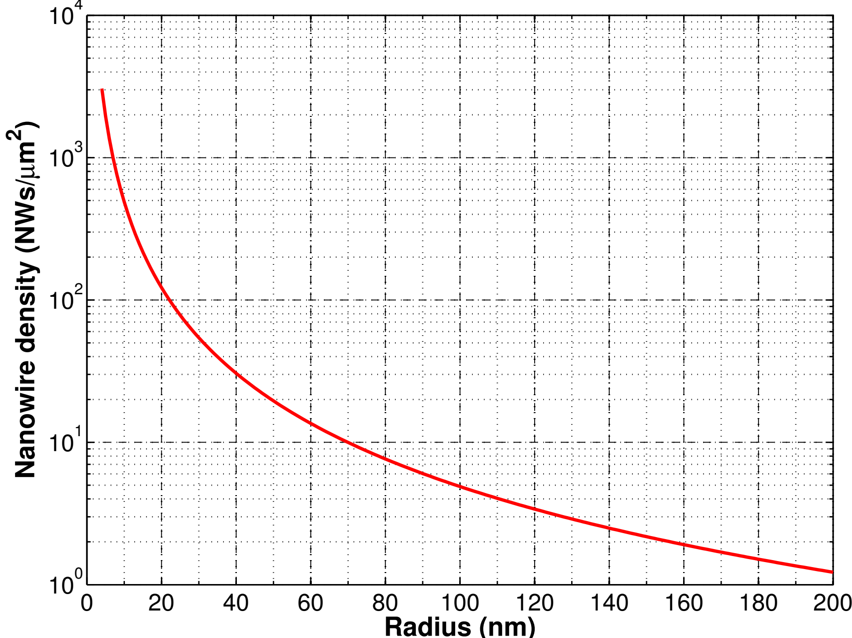


Figure D.4: Nanowire density as a function of the nanowire radius for an occupancy factor of 20% - By varying the nanowire radius, given the occupancy factor of Si NWs in a determined area, the nanowire density can be obtained.

Appendix E

Microplatforms for the thermal characterization of Si NWs arrays

One-dimensional (1D) nanostructures have unique thermophysical properties different from those of their bulk counter parts. In general, as these materials are confined in dimensions with a size comparable to the phonon scattering mean free paths, the thermal conductivity is often reduced due to increased boundary scattering and modified phonon dispersion [132, 146, 147].

Nevertheless, measuring the thermal properties of one-dimensional structures has been a challenge to the research community. This is because conventional techniques for thin-film thermal conductivity measurements, such as the 3ω method, cannot be used readily for these nanostructures due to the small sample size.

In this Appendix, we report the effort invested in the development of thermally isolated structures for the characterization of silicon nanowires. This work, still ongoing, has entailed novel microfabrication techniques and the required optimization of new equipments and processes at the clean room facilities at the IMB-CNM, such as direct laser writing and stepper photolithography and their corresponding intermediate processes.

As it has been previously reported in the literature [54, 55, 64, 132, 148], thermally isolated platforms consisting of two adjacent symmetric silicon nitride membranes suspended by long silicon nitride beams are the state-of-the-art microstructures for measuring the thermophysical properties of one-dimensional nanostruc-

tures (nanotubes or nanowires). In this type of devices (Figure 1.19d), a membrane can be heated to cause heat conduction through the sample to the other membrane while measuring the electrical conductivity, the thermal conductivity and the Seebeck coefficient of the sample. This Appendix attempts to explain all the efforts performed along this thesis in order to fabricate suitable structures for the characterization of these properties.

E.1 Thermal test structures designed by stepper

Test structures to characterize the thermal properties of silicon nanowires arrays were designed, simulated and fabricated throughout this thesis. Nevertheless, several drawbacks (not detailed here) related to different technological constrains encountered during the fabrication of these devices guided the design and fabrication process towards the development of the microstructure that will be described in this section.

As the final approach for the fabrication of adequate devices, stepper lithography was employed trying to simplify, at the same time, the fabrication process to overcome the drawbacks observed in previous studies. The aim was to devised a technological alternative to avoid topography-related problems that afflicted previous designs.

As it was described in Appendix B, by taking advantage of the orientation of the (110) SOI wafer planes, free standing isolated structures could be achieved if properly oriented. The reticle layout designed for this purpose and the design of the structures are shown in Figure E.1.

In summary, the fabrication process started with (110) SOI wafers (*p*-doped) with a 3 μm device layer and a 2 μm buried oxide (BOX) layer. A 3000 Å Si_3N_4 layer was used as the electrical isolation layer followed by an etching step to define small squares to electrically access the suspended Si platforms. A lift-off process was employed to define the heaters strips and the electrical contacts using a 1500 Å tungsten layer. Finally, a DRIE process was employed to etch, at the same time, the Si_3N_4 and Si device layers in order to define the main structures (platforms) and holding beams.

Once the wafer-level fabrication process concluded, wafers were diced in chips of 0.8 x 0.8 cm. Since the beams of the devices were defined along the (110) orientation (with a 35.26° angle with respect to the flat), by using TMAH anisotropic wet etching process (at a chip level) as described in section 2.2.2.3, the silicon beams

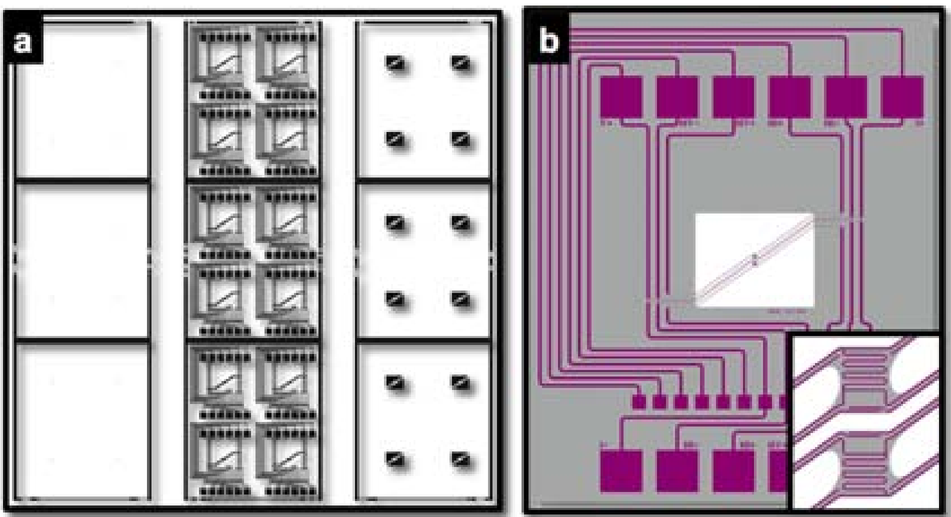


Figure E.1: Reticle layout employed for the fabrication of thermal test structures - (a) The reticle was divided in three sections taking advantage of the flexibility of the stepper lithography to achieve three mask levels in a same layout. (b) Design of the final device showing beams oriented with a 35.26°.

(110-oriented) were selectively removed slightly etching at the same time the main silicon {111} planes of the platforms (where Si NWs would be grown). Nevertheless, since the etch rate of the {110} Si planes is faster than the {111} Si planes[1], the etch of the (111) walls was negligible. By following this procedure, silicon platforms held only by free standing silicon nitride beams were obtained (Figure E.2). At this point, with the silicon platforms still lying on the BOX layer, Si NWs were grown between those suspended silicon masses employing the VLS-CVD mechanism.

As a final step to accomplish a completely isolated free standing structure, the BOX layer beneath the silicon platforms had to be etched. For this purpose, structures without Si NWs were employed to performed different tests. The BOX layer was initially etched in 49% HF for 11 minutes to laterally remove ∼15 μm of SiO_2 (the silicon platforms were 30 μm-width). Nevertheless, the SiO_2 etching process caused the narrower tungsten strips (1 μm-width) to detach. Therefore, the wet

[1]The (110) plane is the fastest etching primary surface with an etching rate of two orders of magnitude higher than that of the (111) plane. The ideal (110) surface has a more corrugated atomic structure than the (100) and (111) primary surfaces. The (111) plane is an extremely slow etching plane that is tightly packed, has a single dangling-bond per atom, and is overall atomically flat. [149]

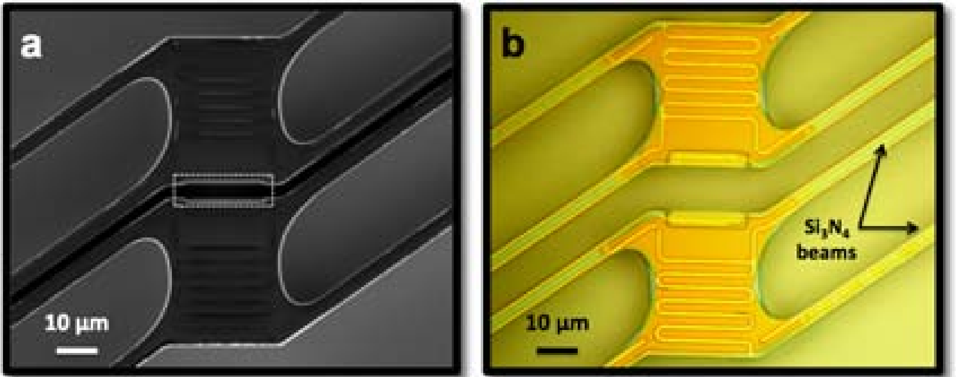


Figure E.2: Fabricated structures for the thermal characterization of Si NWs - (a) SEM image of a as-fabricated device before Si NWs growth and BOX layer removal. The highlighted area shows the trench defined for Si NW growth (2 μm-long). (b) Optical image of a similar device (with a 10 μm-trench), the orientation-dependency of the etched Si walls can be clearly observed through the Si_3N_4 layer and free standing beams, which are distinctly bright.

etching agent was substituted by a Sioetch® solution with an etching process lasting 2.6 hours. Samples were then dried using a CPD to avoid bending of the silicon microplatforms and nitride beams which otherwise would be caused by surface tension forces. Although the structures could be defined and the sacrificial etching of silicon and buried oxide was performed without affecting the metal and nitride layers, the optimization of CPD conditions represented a challenge to achieve free standing isolated structures.

In order to check the correct release of the structures, the thermoreflectance imaging technique was employed to observe the temperature distribution of the platforms which, in case of not being completely etched or in case of collapse, would not heat up as observed in Figure E.3. Confocal microscopy was also helpful to observe the topography of the samples for the cases where the Si platforms were not completely released and the nitride beams bended (Figure E.4a), or for the cases where the structures were released but one of the two structures bended (Figure E.4b).

In summary, the release of the designed structures represented a fabrication challenge and the CPD operation conditions became critical for the fragile structures. After fine-tuning the critical processes involved in the fabrication of these structures, suspended isolated silicon masses connected through silicon nanowires

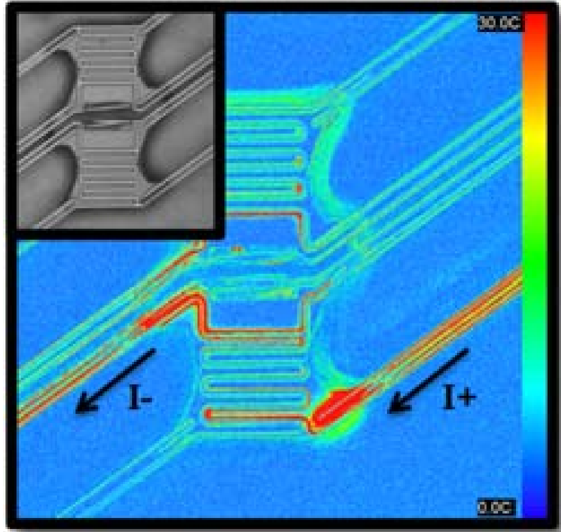


Figure E.3: Thermoreflectance image of a thermal test structure with remaining oxide underneath it - Electrical current was applied to the structure to heat up the silicon platform and observe the temperature distribution. A temperature increment was observed in the Si_3N_4 beams, but no temperature change whatsoever was observed in the Si platform (bottom) to which it was applied.

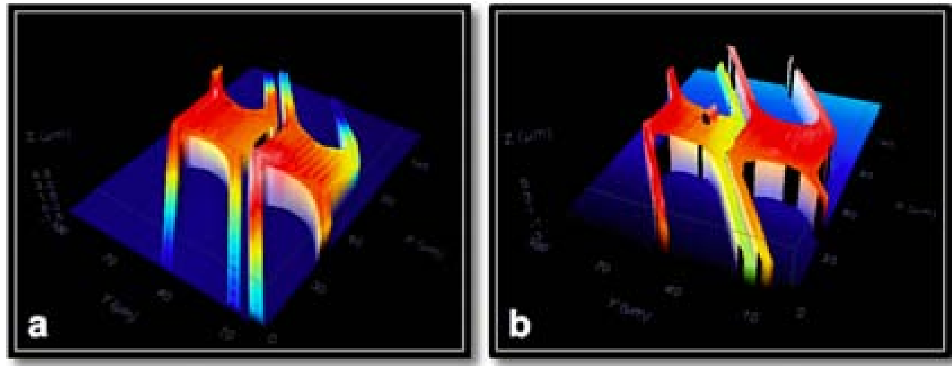


Figure E.4: Confocal images of thermal test structures after BOX layer removal - (a) Topography of structures showing unsuccessful removal of the BOX layer. The profile indicates a $\sim$5 μm step whereas bending of the Si_3N_4 beams is observed. (b) Topography of a structure showing bending (left) and its perfectly free standing counterpart (right).

and held by nitride arms were achieved (Figure E.5). Nevertheless, silicon nanowire growth was observed along the suspended nitride beams, which affected the electrical measurements probably due to a short circuit between the patterned metal strips. The optimization of the growth of silicon nanowires in these structures is currently underway.

Achieving perfectly aligned free standing microstructures compatible with a good Si NWs growth and with well-defined heaters and electrical contacts has proved to be quite technologically challenging. We are still struggling to overcome the different technological constraints.

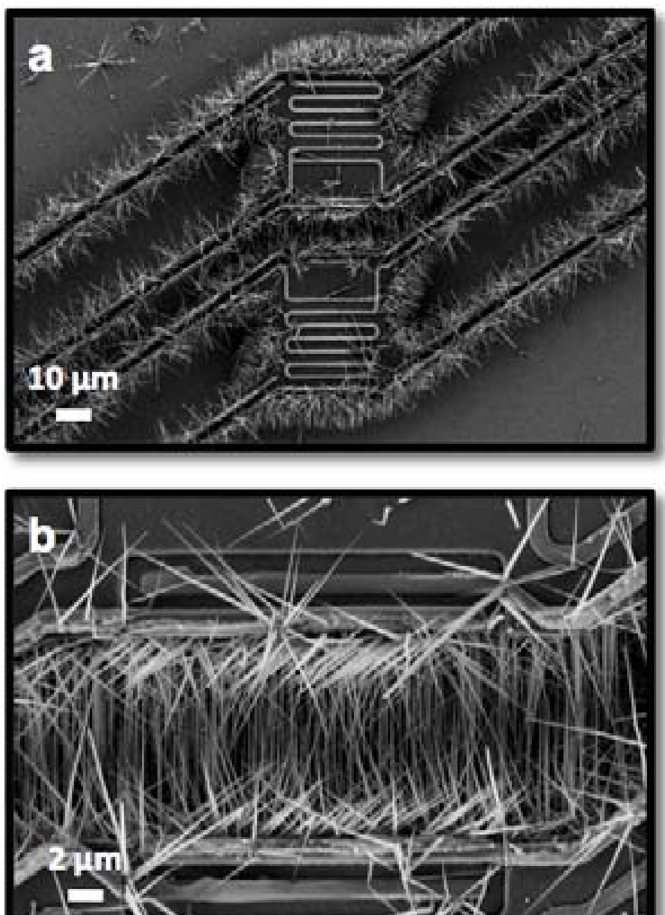


Figure E.5: SEM images of free standing isolated test structures with grown silicon nanowires - (a) Due to the fragility of the structures, samples could not be properly rinsed during the galvanic displacement process, causing nanowire growth not only at Si-exposed areas but also in the nitride beams. (b) Inset of the region were 10 μm-long Si NWs have been grown.

Glossary

ACES *Anisotropic Crystalline Etching Simulation* A first PC-based 3-D etch simulator. The program can simulate silicon etching with different front-surface orientations in different etchants.

AFM *Atomic Force Microscopy.* A very high-resolution type of scanning probe microscopy (SPM). One of the foremost tools for imaging, measuring, and manipulating matter at the nanoscale.

ANSYS An engineering simulation software (computer-aided engineering, or CAE). ANSYS Multiphysics software is a general-purpose finite element modeling package for numerical solving thermal, structural, CFD, electromagnetics, and acoustics problems.

AOT *Dioctyl sodium sulfosuccinate.* An anionic surfactant, a substance that lowers the surface tension of water. It is the most widely used surfactant in reverse micelle encapsulation studies.

APCVD *Atmospheric Pressure CVD.* Atmospheric pressure equals 760 Torr at sea level at 0°C. The APCVD process is controlled by temperature and process gas flow rate.

BOX *Buried silicon OXide.* An oxide layer present in SOI substrates extending across the entire wafer, just below a surface layer of device-quality single-crystal silicon.

CCD *Charge-Coupled Device.* A light-sensitive integrated circuit that stores and displays the data for an image in such a way that each pixel (picture element) in the image is converted into an electical charge the intensity of which is related to a color in the color spectrum.

CMOS *Complementary Metal-Oxide-Semiconductor.* A particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (IC).

CVD *Chemical Vapor Deposition.* A technique whereby gaseous reactants can be deposited onto a substrate used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films.

DOS *Density Of States.* The number of states per interval of energy at each energy level that are available to be occupied by electrons.

DRIE *Deep Reactive-Ion Etching.* A highly anisotropic etch process that prevents lateral etching of the wafers/substrates used to create deep penetration, steep-sided holes and trenches, typically with high aspect ratios.

DUT *Device Under Test.* A packaged part or electronic assembly undergoing testing.

EDX *Energy-Dispersive X-ray spectroscopy.* An analytical technique used for the elemental microanalysis or chemical characterization of a sample by SEM.

FEM *Finite Element Method.* A numerical technique for solving models by finding approximate solutions of partial differential equations.

FIB *Focus Ion Beam.* A system that uses a Ga + ion beam to raster over the surface of a sample in a similar way as

the electron beam in a SEM. The generated secondary electrons (or ions) are collected to form an image of the surface of the sample. The ion beam allows the milling of small patterns in the sample at well localized sites, so that cross-sectional images of the structure can be obtained or that modifications in the structures can be made.

IR *InfraRed.* Electromagnetic radiation with a wavelength longer than that of visible light, measured from the nominal edge of visible red light at 0.74 μm, and extending conventionally to 300 μm, including most of the thermal radiation emitted by objects near room temperature.

KOH *Potassium hydroxide.* One the most commonly used anisotropic silicon ODE chemistry for micromachining silicon wafers.

LED *Light-Emitting Diode.* A semiconductor diode that emits visible light when electricity is applied (via electroluminescence).

LPCVD *Low Pressure CVD.* A CVD deposition process is performed in a reactor at temperatures up to $\sim$900°C. The deposited film is a product of a chemical reaction between the source gases supplied to the reactor. The process is typically performed on both sides of the substrate at the same time.

MEMS *MicroElectroMechanical Systems.* A technology that in its most general form can be defined as miniaturized mechanical and electro-mechanical elements (i.e., devices and structures) that are made using the techniques of microfabrication. The critical physical dimensions of MEMS devices can vary from well below one micron on the lower end of the dimensional spectrum, all the way to several millimeters.

NW *NanoWire.* A one-dimensional (1D) structure or wire that have a lateral size constrained to tens of nanometers or less and an unconstrained longitudinal size.

ODE *Orientation-Dependent Etchant.* A wet etchant that etches crystalline materials at very different rates depending upon which crystal face is exposed.

PCB *Printed Circuit Board.* Used to mechanically support and electrically connect electronic components using conductive pathways, tracks or signal traces etched from copper sheets laminated onto a non-conductive substrate.

PECVD *Plasma-Enhanced CVD.* A CVD process that uses plasma to enhance the chemical reaction rates of the precursors to deposit thin films from a gas state (vapor) to a solid state on a substrate. It allows deposition at relatively low temperatures, which is often critical in the manufacture of semiconductors.

PGEC *Phonon Glass-Electron Crystal.* A material that would possess electronic properties normally associated with a good semiconductor single crystal but have thermal properties akin to that of an amorphous material.

QDSL *Quantum-Dot SuperLattice.* A structure composed by multiple arrays of quantum dots with a delta-function distribution of density of states and discrete energy levels due to three-dimensional quantum confinement. These structures have a potentially more favorable carrier scattering mechanism and a much lower lattice thermal conductivity providing a potential for better thermoelectric devices.

RIE *Reactive Ion Etching.* A dry etching technology that uses chemically reactive plasma (generated under low pressure by an electromagnetic field) to remove material deposited on wafers. High-energy ions from the plasma at-

tack the wafer surface and react with it.

RTG *Radioisotope Thermoelectric Generator.* An electrical generator that obtains its power from the heat released by the decay of a suitable radioactive material.

SAED *Selected Area Electron Diffraction.* A crystallographic experimental technique that can be performed inside a TEM to selectively choose a part of the specimen from which a diffraction pattern is obtained.

SEM *Scanning Electron Microscopy.* A type of electron microscope that images a sample by scanning it with a high-energy beam of electrons in a raster scan pattern.

SNR *Signal-to-Noise Ration.* A measure used in science and engineering that compares the level of a desired signal to the level of background noise. It is defined as the ratio of signal power to the noise power.

SOI *Silicon-On-Insulator.* A technology that refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing.

SThM *Scanning Thermal Microscopy.* An advanced scanning probe microscopy (SPM) mode intended for simultaneous obtaining nanoscale thermal and topography images. This technique allows to visualize temperature and thermal conductivity distribution at the sample surface.

TCR *Temperature Coefficient of Resistance.* An indicator of the change in the electrical resistance of a material as its temperature changes, typically measured in ppm/K.

TEG *ThermoElectric Generator.* A device able to convert temperature differences into electrical energy by means of the Seebeck effect.

TEM *Transmission Electron Microscopy.* A microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through to form an image.

TLM *Transmission Line Model.* A method used to accurately measure the contact resistance. It consists of a structure composed by a set of contacts, separated by a variable distance L, that allows measuring the resistance between them.

TMAH *TetraMethylAmmonium Hydroxide.* An anisotropic ODE (similar to KOH etching) used for fast removal and silicon micromachining.

VLS *Vapor-Liquid-Solid.* A mechanism for the growth of one-dimensional structures, such as nanowires, from chemical vapor deposition.

XRD *X-Ray Diffraction.* An analytical technique used to reveal information about the crystallographic structure, chemical composition, and physical properties of materials and thin films.

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The increasing demand for portable power required by miniaturized systems is driving the development of new technologies and materials to achieve efficient energy generation at the microscale. Apart from removing heat from electronic devices, thermoelectric microgenerators offer an attractive opportunity to harvest waste heat converting it into power. The low thermoelectric conversion efficiency of current bulk microelectronics semiconductor materials has limited their implementation for energy harvesting purposes. However, recent studies have proven, at single nanowire level, that nanostructuring of silicon into nanowires greatly enhances the thermoelectric properties of this material, opening up the opportunity for the integration of thermoelectric generators into silicon microtechnology.

In this thesis, dense and well-ordered arrays of silicon nanowires (Si NWs) have been monolithically integrated into a silicon micromachined device. The VLS-CVD technique has been used for the controlled lateral growth of nanowires. The microstructure has been appropriately designed to adapt the tridimensional growth of the Si NWs arrays to a planar architecture, and to assure electrical accessibility to the nanowires. Additionally, the device allows an internal in-plane temperature gradient to be established when placed in contact with a heat source, giving rise to a complete thermoelectric microgenerator in which the Si NWs act as the nanostructured thermoelectric material.