

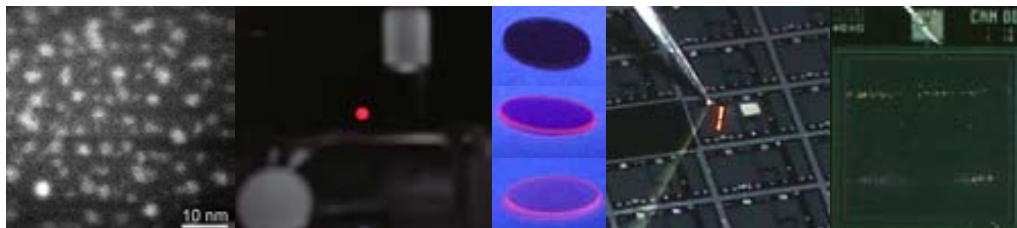


**Universitat Autònoma
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**Correlation between optical and electrical
properties of materials containing nanoparticles**

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Ph.D. Thesis

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Barcelona, Spain
September 2008

La presente tesis doctoral titulada: “Correlation between optical and electrical properties of materials containing nanoparticles” ha sido realizada por Alfredo Morales Sánchez como Trabajo de Investigación dentro del programa de Tercer Ciclo de Física bajo la dirección de Carlos Domínguez Horna, Profesor de Investigación del Instituto de Microelectrónica de Barcelona (IMB–CNM, CSIC) y Mariano Aceves Mijares, Investigador Titular del Departamento de Electrónica perteneciente al Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE) de México y actuando de tutor el Dr. Javier Rodríguez Viejo, Profesor Titular del Departamento de Física de la Universidad Autónoma de Barcelona.

Bellaterra, Barcelona. Septiembre 2008

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Acknowledgments

At first place, I want to thank Consejo Nacional de Ciencia y Tecnología (CONACyT) and Fundación Carolina for the grant received.

My deepest thanks to Dr. Carlos Domínguez Horna for giving me the opportunity of working under his direction and for his support and help during my stage in Barcelona, Spain.

I would like to thank to Dr. Mariano Aceves Mijares for co-direct this work and for his support and help.

Thanks to:

Dr. Javier Rodríguez Viejo for being my tutor at the Universidad Autónoma de Barcelona.

Dr. Blas Garrido's research group from the Universidad de Barcelona, Physics department.

All the staff of the Instituto de Microelectrónica de Barcelona (IMB-CNM), especially to the chemical transducers group (GTQ).

Instituto Nacional de Astrofísica, Óptica y Electrónica.

To projects:

MILES: "Monolithic integration of light emitters and optochemical transducers with silicon technology". TEC2006-13907-C04-01/MIC.

Optimization of silicon radiation sensors with high efficiency in the UV range. CSIC, P2005MX03. Bilateral cooperation program CSIC-CONACYT.

NANOMAGO: Fabrication and characterization of thin magneto-optical layers in metal-dielectric nanostructures: Implementation as modulators in integrated optics technology. D.G.I. S.E.P.C. y T., MAT2002-04484-C03-01.

Finally, thanks to my family and my wife, Edith.

Abstract

It is known that bulk silicon is the dominant semiconductor material in microelectronics. However, its use in reliable and low cost integrated circuits (IC) fabrication which carry out opto-electronic functions has not been appropriate due to the fact that silicon is an indirect band gap material.

Observation of luminescence in porous silicon seemed to solve the physical inability of the silicon (Si) to act as light emitter; however its poor chemical stability, weak robustness and luminescence degradation made it unsuitable for such applications. Other Si-based materials such as hydrogenated silicon rich oxynitride, Si/SiO₂ multilayers, and silicon rich oxide (SiO_x, x<2) films have been reported to solve the physical incapacity of silicon to act as light emitter. The key for the excellent light emission properties of these materials are the embedded silicon nanoparticles (Si-nps). With this approximation the quantum confinement of carriers is maximized, the probability of radiative recombination is improved, and the emission wavelength is shifted to the visible range and controlled with the Si-np's size. These nanometre-sized silicon particles either embedded in a SiO₂ or Si₃N₄ matrix have shown a strong and stable luminescence seeming as a better alternative for light emitting devices (LED's) fabrication.

In this thesis, silicon rich oxide [SRO, (SiO_x, x<2)] films with different silicon excesses were deposited by low pressure chemical vapor deposition (LPVCD). Besides, Si implanted SRO (SI-SRO) films were also fabricated. Si-nps in these films were created after a thermal annealing at high temperature (1100 and 1250° C). The composition, microstructure and optical properties of these SRO and SI-SRO films were analyzed as a function of the different technological parameters, such as silicon excess, Si ion implantation dose, and thermal annealing temperature.

Once the microstructure, composition as well as the optical properties of these materials is known, SRO films which exhibited the best photoluminescent (strongest PL) properties were chosen in order to analyze their electrical and electro-optical properties.

Simple Metal–Oxide–Semiconductor (MOS) structures using the SRO films as the dielectric layer were fabricated for these studies. SRO films with Si-excess of ~ 4.0 and ~ 2.2 at.% and thickness ranging from 24 to 80 nm were deposited. The conduction mechanism in these films is analyzed by making use of trap assisted tunnelling (TAT) in low electric field as well as Fowler–Nordheim (FN) tunnelling in high electric fields.

The electrical measurements exhibited important results, such as a reduction in capacitance and current during the sweep or after applying a constant bias. These effects are ascribed to the annihilation of conduction paths created by silicon clusters (Si-cl) inside the SRO films.

A part from that, some devices exhibited current fluctuations in the form of spike-like peaks and a clear staircase at room temperature. These effects were related to Coulomb blockade (CB) effects in the silicon nanoparticles embedded in the SRO films. And from the current plateaus, the size of the Si-nps (about 1 nm) was calculated.

Field effect luminescence of these SRO films was studied by alternating negative (positive) to positive (negative) voltages (pulsed excitation). Moreover, it is demonstrated that these SRO films show EL emission in continuous current voltage, observed at naked eye. Multiple shining spots of several colours are seen on the MOS-like structure surface when reversely biased.

These devices display a broad electroluminescent emission spectrum which goes from 400 nm up to 900 nm. Finally, a correlation between the structural, electrical and luminescent (PL and EL) properties is discussed.

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List of Symbols

A	Area
C	Capacitance
C_{cl}	Si-cluster capacitance
C_{FB}	Flat-band capacitance
C_{MAX}	Maximum capacitance
C_{MIN}	Minimum capacitance
C_{np-np}	Capacitance between nanoparticles
C_{ox}	Oxide capacitance
C_S	Silicon surface capacitance
C_{np}	Si-np capacitance
C_{SiO_2}	Silicon dioxide capacitance
C_{SRO}	SRO capacitance
C_T	Total capacitance
d	Si-np size
δ_i	Stairwidth current
E	Electric field
E_c	Coulomb charging energy
E_C	Conduction band energy
E_F	Fermi energy
E_g	Band gap energy
E_i	Intrinsic energy
E_{ox}	Electric field in the silicon dioxide
E_V	Valence band energy
f	Frequency
I_{drop}	Current drop
J	Current density
K_{SRO}	Dielectric constant of SRO
m_e^*	Effective mass of electron
m_h^*	Effective mass of hole
N_a	Density of acceptors
N_{eff}	Silicon/silicon rich oxide interface charge density

q	Elementary charge
R	Resistance
R_{cl}	Resistance of Si-cls
R_{np}	Resistance of Si-nps
R_s	Resistance of Si-substrate
R_{SiO_2}	Resistance of oxide
t	Time
t_{ox}	SiO ₂ thickness
t_{SRO}	SRO thickness
t_{np-np}	Distance between Si-nps
V_{drop}	Voltage where current drop happens
V_{FB}	Flat-band voltage
V_G	Gate voltage
V_{stair}	Stair voltage width
V_{TH}	Threshold voltage
ϵ_0	Permittivity of SiO ₂
ϵ_{Si}	Dielectric constant of bulk crystalline silicon
ϵ_{SRO}	Permittivity of SRO
λ_{exc}	Excitation wavelength
τ	Mean lifetime

Abbreviations

A	Ampere
Al	Aluminium
at.%	Atomic percent
C-f	Capacitance – Frequency
C-V	Capacitance – Voltage
CMOS	Complementary metal oxide semiconductor
CB	Coulomb blockade
CBG	Coulomb blockade gap
Cd	Cadmium
CL	Catholuminescence
cm	Centimetre
Cu	Copper
CVD	Chemical vapor deposition
DT	Direct Tunneling
EFTEM	Energy Filtered Transmission Electron Microscopy
EL	Electroluminescence
eV	Electron Volt
F	Farad
FB	Forward bias
FN	Fowler Nordheim
FTIR	Fourier Transform Infrared Spectroscopy
FWHM	Full width at half maximum
GaAs	Gallium arsenide
GHz	Giga Hertz
H	Hydrogen
h	Hour
He	Helium
IC	Integrated circuit
I-t	Current – time
I-V	Current – Voltage
kHz	Kilo Hertz

LC	Luminescent center
LED	Light emitter devices
LO	Longitudinal optical vibrational mode
LPCVD	Low pressure Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
ms	Millisecond
MV	Mega Volt
N	Nitrogen
N ₂ O	Nitrous oxide
NBOHC	Non-bridging oxygen hole center
NDC	Negative differential conductance
NDR	Negative differential resistance
nm	Nanometer
NOV	Neutral oxygen vacancy
O	Oxygen
P	Pressure
pF	Pico farads
PF	Poole-Frenkel tunnelling
PECVD	Plasma Enhanced Chemical Vapor Deposition
PL	Photoluminescence
PLD	Pulsed laser deposition
PLE	Photoluminescence excitation
QCE	Quantum confinement effects
RB	Reverse bias
RBM	Random bonding model
RF	Radio Frequency
RMM	Random mixtures model
Ro	Flow ratio
SCC	Stationary charge configuration
SED	Single electron devices
Si	Silicon
Si-cl	Silicon cluster
SiH ₄	Silane
Si ₃ N ₄	Silicon nitride

SiO ₂	Silicon dioxide
Si-nc	Silicon nanocrystal
Si-np	Silicon nanoparticle
SI-SRO	Silicon-implanted silicon rich oxide
SRO	Silicon Rich Oxide
SRIM	Stopping and Range of Ions in Matter
TO	Transverse optical vibrational mode
TAT	Trap-assisted tunnelling
UV	Ultraviolet
V	Voltage
WOB	Weak oxygen bonds
XPS	X-ray Photoemission Spectroscopy
μs	Microsecond

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Chapter 1

Introduction

The high integration levels reached by the Si microelectronics industry have permitted high speed performance and unprecedented interconnection levels. However, interconnect propagation delays, overheating, and information latency between single devices are produced by this interconnection degree. To overcome these phenomena, photonic materials in which light can be generated, modulated, amplified and detected as well as integrated with standard electronic circuits are needed. Although the detector and optical component integration has been demonstrated, the main limitation of the silicon (Si) photonics is the lack of suitable light emitters.

In this sense, currently one of the most ambitious scientific and technologic goals is the development and realization of light emitters compatible to the complementary metal oxide semiconductor (CMOS) technology.

1.1. Bulk Silicon

It is an undeniable fact that silicon is the leading semiconductor in the microelectronic industry; however, it is an indirect band-gap material, that is, the bottom of the conduction band and the top of the valence band are not aligned in the k space as depicted in figure 1.1(a). This implies that for the electron-hole (e-h) radiative

recombination occurs the assistance of a further process (usually a phonon) is necessary to conserve the momentum. Such a three particle process is quit inefficient if compared with the recombination in direct band-gap, where the bottom of the conduction band and the top of the valence band are aligned as shown in figure 1.1(b). In this kind of materials the recombination does not need the participation of a third process. Besides, the radiative lifetime in Si is very long, in the milliseconds range, meanwhile in direct band-gap semiconductors the radiative lifetime is significantly slower, in the nanoseconds range.

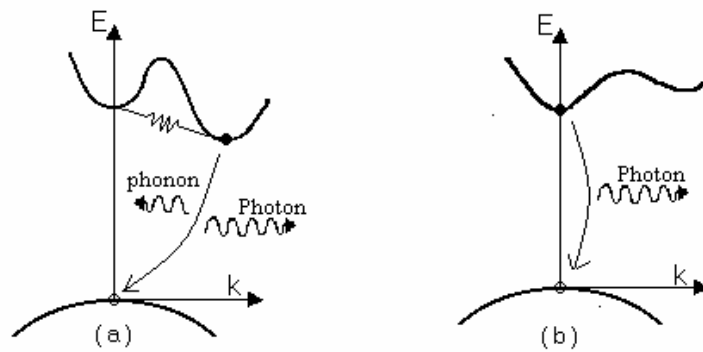


Figure 1.1. Recombination process in (a) indirect and (b) direct band-gap materials in the k space.

The presence of defects or impurities in the crystal produces new levels into the band-gap, where the excited carriers can relax or being trapped, and then the recombination in these levels can dominate. In addition to the radiative recombination processes, the non-radiative recombination processes can contribute to the annihilation of electrons and holes. In these processes, the energy is released as phonons in most of cases. Then, there exist a competition between the non-radiative recombination and the radiative recombination. This competition is strongly dominated by the non-radiative phenomena in Si causing very low luminescence efficiency. Therefore, the absence of linear electro-optic effects makes the Si a poor light emitter and unsuitable for optoelectronic applications.

1.2. Nanoparticles

Observation of visible luminescence in porous silicon by Canham in 1990 [1] seemed to solve the physical inability of silicon to act as light emitter. This novel characteristic was

the result of the dramatic two-dimensional quantum size effects which can produce emission far above the band gap of bulk crystalline Si.

This discovery attracted a new effective way of obtaining light emission in Si-based materials. However, it was found that the porous silicon suffers from poor mechanical and chemical stability [2, 3]. Since then, many strategies have been researched to overcome this limitation as well as to understand and optimize the light emission phenomena with more stable materials.

One of the approaches was nanometre-sized silicon (Si) and germanium (Ge) crystallites (nanoparticles) embedded in a dielectric matrix. Both Si-nanoparticles (Si-nps) and Ge-nanoparticles (Ge-nps) have shown a strong and stable luminescence at room temperature seeming a better alternative for light emitting devices fabrication [4-9].

Another approach is impurity-mediated luminescence from the addition of rare earth ions [such as erbium (Er)] into a silicon rich oxide film in order to change their luminescence properties [10, 11]. With this approach, the wavelength emission is shifted toward $\sim 1.5 \mu\text{m}$, which is a common wavelength for telecommunication applications.

1.3. Quantum confinement

The visible light emission in nanoparticles has been related to quantum confinement phenomena. Quantum confinement is obtained when electrons and holes in a semiconductor are confined by a potential well with size d , as illustrated in figure 1.2. This quantum phenomena can be observed in either in two-dimensional (2D, quantum well), one-dimensional (1D, quantum wires), or zero-dimensional (0D, quantum dots) and it occurs when one or more of the dimensions of a particle are made very small so that it approaches the size of the Bohr exciton radius ($\sim 5 \text{ nm}$).

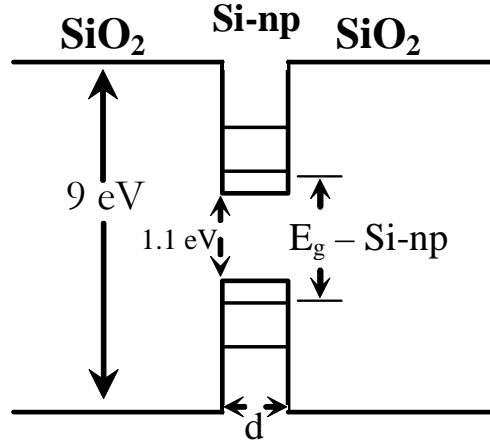


Figure 1.2. Band-gap increasing of a Si-np with size d ($< 5\text{nm}$) due to quantum confinement.

Confinement raises the energy of the ground state, tends to create a discrete density of states at low energies, and introduces uncertainty into the momentum of the particle. The last of these effects can also be understood by considering only the uncertainty principle, to the extent that the potential well localizes the particle in a small volume.

An analytic model based on the effective mass approximation predicts that this size-dependent effective band-gap varies according to [12]:

$$E_{Si-np} = E_g + \left(\frac{1}{L_x^2} + \frac{1}{L_y^2} + \frac{1}{L_z^2} \right) \left(\frac{1}{m_e^*} + \frac{1}{m_h^*} \right) \frac{\hbar^2 \pi^2}{2} \quad (1.1)$$

Where m_e^* and m_h^* are the effective masses for electron and hole, respectively, L_x , L_y and L_z are the linear dimensions of the Si-np, and $E_g = 1.1\text{ eV}$ is the bulk band-gap. It is clear that this model neglects any surface/interface related defects and relies heavily on the effective mass approximation. Some experimental results have demonstrated that there is no correlation with theoretical studies. This fact has been attributed to the existence of some radiative recombination centres at the Si-np/SiO₂ interface [13, 14]. Some of these centres have been related to the presence of double bonds Si=O [15, 16] and excitons confined on the spherical shell, which is an interfacial layer between the Si-np core and the a-SiO₂ surface layer [17]. Moreover, a SiO_x shell at the surface of Si-nps has been observed and therefore it is expected to have some kinds of defects inside and therefore affecting the luminescence emission [17, 18].

1.4. Contents of this thesis

The aim of this thesis is to investigate the structural, optical and electrical properties of silicon rich oxide films in order to obtain a Si-based light emitter device. Chapters are organized as follows:

Chapter 2 is focused on the luminescence nanomaterials such as silicon porous and silicon nanoparticles as well as the main preparation processes. Techniques focused on the materials characterization, such as ellipsometry, Fourier transform infrared spectroscopy (FTIR), X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM) and photoluminescence are also presented in this chapter.

In chapter 3, the composition, microstructure and optical properties of SRO and SI-SRO films are analyzed as a function of the different technological parameters as silicon excess, Si ion implantation dose, and thermal annealing temperature.

In chapter 4, the fabrication of Metal–Oxide–Semiconductor (MOS) structures using the SRO films as the dielectric layer is reported. Their electrical properties are presented as C-f, C-V and I-V curves. The conduction mechanism in these films is analyzed by making use of trap assisted tunnelling (TAT) in low electric fields as well as Fowler–Nordheim (F–N) tunnelling in high electric fields. Field effect luminescence and continuous electroluminescence results measured from these MOS-like structures are reported. Furthermore, images of EL which is observed at naked eye are shown.

In chapter 5, the structural, electrical and luminescent (PL and EL) properties are discussed. A possible mechanism for the film composition that clarifies the origin of all properties is proposed. Finally, conclusions of the work done as well as the further studies are discussed in chapter 6.

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Chapter 2

Luminescence in nanostructures

Since the observation of light emission in porous silicon by Canham in 1990, Si-based nanostructures embedded in a dielectric matrix have been the most studied materials for the fabrication of light emitting silicon devices. The interest in these Si-nanostructures is due to their novel quantum phenomena that results when their diameter is less than the size of the Bohr radius (~ 5 nm).

2.1. Porous silicon (PS)

Porous silicon was discovered by A. Uhlir at the Bell laboratories (US) in 1956 [1]. Despite of this discovery, the scientific community was not interested in PS until the late 80's, when Canham proposed that porous silicon could display quantum confinement effects [2]. In his published experimental results, strong light emission from silicon was obtained after subject the Si-wafers to an electrochemical and chemical dissolution. Different PL peaks were observed depending on the porosity of the layer, as observed in figure 2.1. These novel results stimulated the interest of the scientific community in the non-linear optical and electrical properties of silicon, especially due to its potential applications.

Despite of the strong room temperature luminescence observed in PS, it was found that it suffers from poor mechanical and chemical stability producing degradation in the PL properties [3, 4].

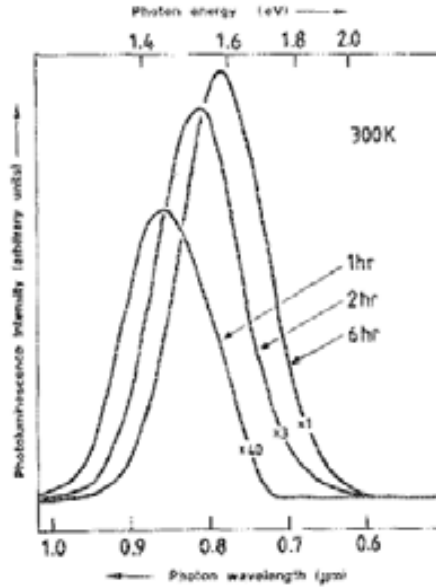


Figure 2.1. Photoluminescent spectra from anodized p wafer after immersion in 40 % aqueous HF for different times. After [2].

2.2. Silicon nanoparticles (Si-nps)

Si nanoparticles inside a dielectric matrix have shown a strong and stable luminescence seeming a better alternative for light emitting devices fabrication. Si-nps can be obtained from a gas phase or indirectly by recrystallization within a matrix.

The most popular approach is to produce Si-nps in a silica matrix to exploit the stability of the SiO₂/Si interface and the improvement emission properties of quantum confined Si. Si-nps are obtained when the corresponding dielectric layers super enriched with silicon are subjected to thermal annealing in high temperature. Here, the technological parameters such as the duration of the thermal treatment, the annealing temperature, and the Si excess content all determine the final size of the cluster, the size dispersion, as well as their nature (amorphous or crystalline).

2.3. Fabrication techniques

Different techniques have been reported in order to obtain silicon nanoparticles (Si-nps). However, since compatible techniques with complementary metal oxide semiconductor (CMOS) technology are required, the most employed techniques to obtain Si-nps are silicon ion implantation into silicon-based dielectrics, plasma enhanced chemical vapor deposition (PECVD), and low pressure chemical vapor deposition (LPCVD). However, techniques based in CVD method allow obtaining thick SRO layers which are more stable as well as containing uniform silicon excess.

Ion implantation

It is a process by which ions of a material can be implanted into another solid, changing its physical properties, as shown in figure 2.2(a). Ion implantation is a common technique used in semiconductor device fabrication. With this technique, both chemical and structural change are introduced by the implanted ions. To activate the implanted ions and restore the damage produced, a thermal annealing is necessary.

In the case of Si ions implanted into silicon dioxide matrix, a silicon agglomeration in the form of Si-nps is obtained after the thermal annealing process.

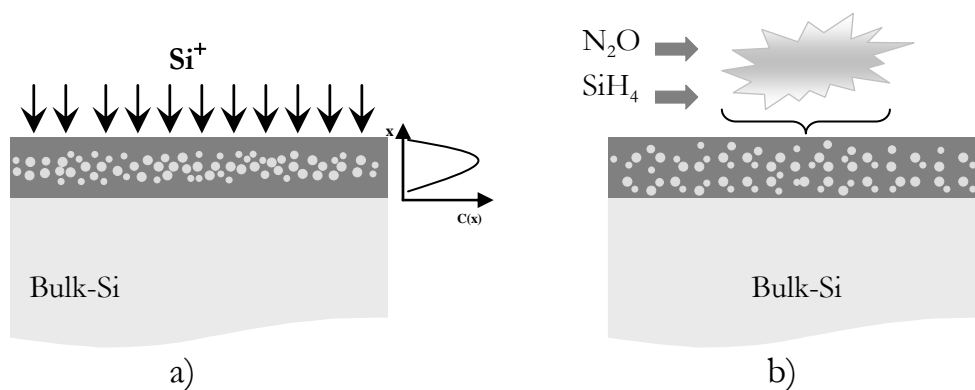


Figure 2.2. a) Si-ion implantation into SiO₂ and b) SRO films deposited using CVD by the reaction of N₂O and SiH₄ reactant gasses.

Chemical vapour deposition (CVD)

CVD is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer or substrate is exposed to one or more volatile precursors, which react and/or decompose on or near the substrate surface to produce the desired deposit (see figure 2.2(b)). Frequently, volatile byproducts are obtained, but they are removed by the gas flow through the reaction chamber.

Types of CVD processes

There are a great number of forms of CVD. These processes differ in the means by which chemical reactions are initiated (e.g., activation process) and process conditions. The main CVD techniques used for Si-nps fabrication are LPCVD and PECVD.

Low-pressure CVD (LPCVD) is CVD processes at sub-atmospheric pressures. Reduced pressures tend to reduce unwanted gas-phase reactions and improve film uniformity across the wafer.

Plasma-enhanced CVD (PECVD) is CVD processes that utilize a RF discharge to enhance chemical reaction rates of the precursors. PECVD processing allows deposition at lower temperatures, which is often critical in the manufacture of semiconductors.

Silicon rich oxide (SRO) films are easily deposited by PECVD and LPCVD techniques using oxidant species (like nitrous oxide, N_2O) and silicon compounds (i.e. silane, SiH_4) as reactant gasses. After SRO films are thermally annealed at high temperature, a phase separation between Si and SiO_2 occurs creating Si-nps. The Si-nps size depends on the silicon excess inside of the deposited films, as well as of the time and the temperature of thermal annealing.

2.4. Characterization techniques [5]

The study of composition and microstructure of SRO films before and after apply a thermal annealing play an important role in order to understand the luminescence properties of nanostructures. Several techniques such as null ellipsometry, Fourier transform infra-red spectroscopy (FTIR), x-ray photoelectron spectroscopy (XPS), energy filtered transmission electron microscopy (EFTEM) and photoluminescence (PL) are of great interest to get such characteristics.

Ellipsometry

Ellipsometry is a true contact less, non-invasive technique measuring changes in the polarization state of light reflected from a surface. It is used predominantly to determine the thickness of thin dielectric films on highly absorbing substrates, but can also be used to determine optical constants of films or substrates.

Consider plane-polarized light incident on a plane surface as illustrated in figure 2.3. The incident polarized light can be resolved into a component p, parallel to the plane of incidence and a component s, perpendicular to the plane of incidence.

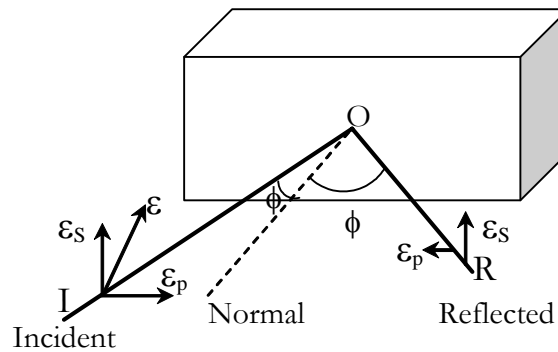


Figure 2.3. Schematic of polarize light reflection form a plane surface. Lines I-O and O-R define the plane of incidence and ϕ is the angle of incidence.

If the material that reflects the waves has zero absorption, then only the amplitude of the reflected wave is affected. Linearly polarized light is reflected as linearly polarized light. However, the two components experience different amplitudes and phase shifts

upon reflection for absorbing materials and for multiple reflections in a thin layer between air and the substrate. The parallel component reflectance is always less than the vertical component for angles of incidence other than 0° and 90°. The two are equal at those two angles. The phase shift difference introduces an additional component polarized 90° to the incident beam, rendering the reflected light elliptically polarized. Projected onto a plane perpendicular to the reflected beam, the resultant electric field vector of the elliptically polarized light depicts an ellipse. The key property of polarized light for ellipsometry is the change of plane-polarized light into elliptically polarized light or elliptically polarized light into a plane-polarized light upon reflection.

Light propagates as a fluctuation in electric and magnetic fields at right angles to the direction of propagation. The total electric field is made of the parallel component ε_p and the vertical component ε_s . The reflection coefficients:

$$R_p = \frac{\varepsilon_p(\text{reflected})}{\varepsilon_p(\text{incident})}; R_s = \frac{\varepsilon_s(\text{reflected})}{\varepsilon_s(\text{incident})} \quad (2.1)$$

are not separately measurable. However, the complex reflection ratio ρ , defined in terms of the reflection coefficients R_p and R_s or the ellipsometric angles Ψ and Δ is measurable. It is given by:

$$\rho = \frac{R_p}{R_s} = \tan(\Psi)e^{j\Delta} \quad (2.2)$$

where $j=(-1)^{1/2}$. Since ρ is the ratio of reflection coefficients, that is, the ratio of the intensities and the relative phase difference, it is not necessary to make absolute intensity and phase measurements.

The ellipsometric angles Ψ ($0^\circ \leq \Psi \leq 90^\circ$) and Δ ($0^\circ \leq \Delta \leq 360^\circ$) are the most commonly used variables in ellipsometry and are defined as

$$\Psi = \tan^{-1}|\rho|; \Delta = \text{differential phase change} = \Delta_p - \Delta_s.$$

The angles Ψ and Δ determine the differential changes in amplitude and phase, respectively, experienced upon reflection by the component vibrations of the electric field vectors parallel and perpendicular to the plane of incidence. From these parameters, the refractive index and the thickness of a film can be calculated using the equations:

$$\tan \Psi * e^{i\Delta} = \left(\frac{r_{1p} - r_{2p} e^{-2i\delta}}{1 - r_{1p} r_{2p} e^{-2i\delta}} \right) \left(\frac{1 - r_{1s} r_{2s} e^{-2i\delta}}{r_{1s} - r_{2s} e^{-2i\delta}} \right) \quad (2.3)$$

$$\delta = d \frac{2\pi}{\lambda} \sqrt{n^2 - \text{sen}^2 \phi} \quad (2.4)$$

where λ is the wavelength of the incident light, ϕ the incidence angle; r_{1p} , r_{1s} , r_{2p} , and r_{2s} the Fresnel's coefficients for the reflection components at the air-film and film-substrate interfaces, respectively.

Null ellipsometry

A common ellipsometer schematic is shown in figure 2.4; its principle of operation is as follows: a collimated beam of unpolarized monochromatic light, typically from a laser, is linearly polarized by the polarizer. When the unpolarized light is incident on such a polarizer, total internal reflections allows only linearly polarized light to exit.

The compensator changes the linearly polarized light to elliptically polarized light. The compensator contains a fast and a slow optical axis perpendicular to the direction of transmission. The component of incident polarized light whose electric field is parallel to the slow axis is retarded in phase relative to the component parallel to the fast axis as the light passes through the compensator. When the relative retardation is $\pi/2$, the compensator is called a quarter-wave retarder or quarter-wave plate. Linear quarter-wave retarders, made out of birefringent mica or quartz, are most common used in ellipsometers.

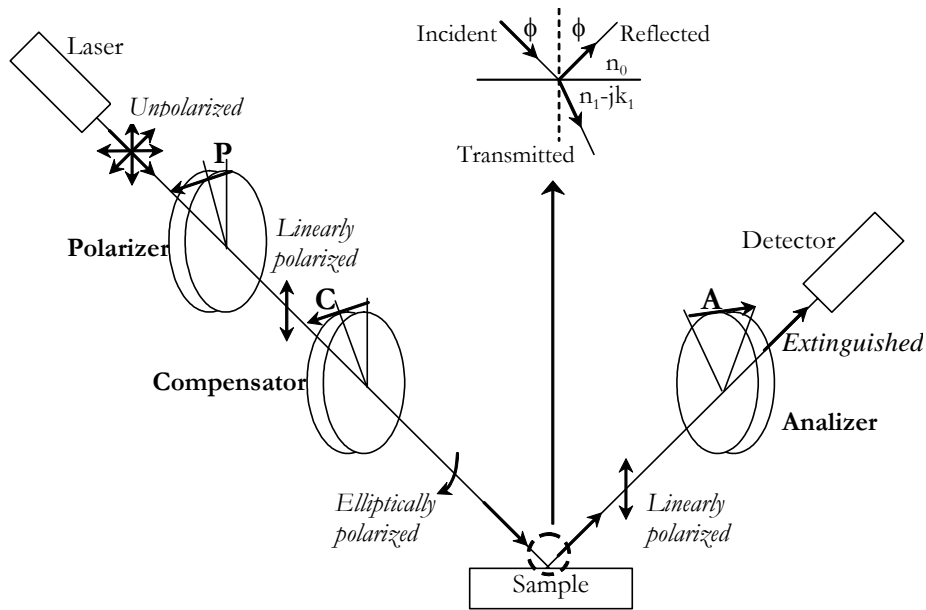


Figure 2.4. Ellipsometer schematic.

The angles of P and C of the polarizer and the compensator can be adjusted to any state of polarization ranging from linear to circular. The aim of an ellipsometry measurement is a null at the photodetector. This is attained by choosing P and C to give light of elliptical polarization which, when reflected from the sample, becomes linearly polarized to be extinguished by the analyzer. The linearly polarized light is passed through the analyzer, which is similar to the polarizer, and the angle A is adjusted for minimum photodetector output.

Fourier transform infrared spectroscopy (FTIR)

The basic optical component of Fourier transform spectrometers is the Michelson interferometer shown in a simplified form in figure 2.5. Light from an infrared source is collimated and directed on a beam splitter. In one path the beam is reflected back to the beam splitter by a fixed-position mirror, where it is partially transmitted to the source and partially reflected to the detector.

In the other arm of the interferometer, the beam is reflected by the movable mirror that is translated back and forth while maintained parallel to itself. The beam from the movable mirror is also returned to the beam splitter where it, too, is partially reflected back to the source and partially transmitted to the detector. Although the light from the

source is incoherent, when it is split into two components by the beam splitter, the components are coherent and can produce interference phenomena when the beams are combined.

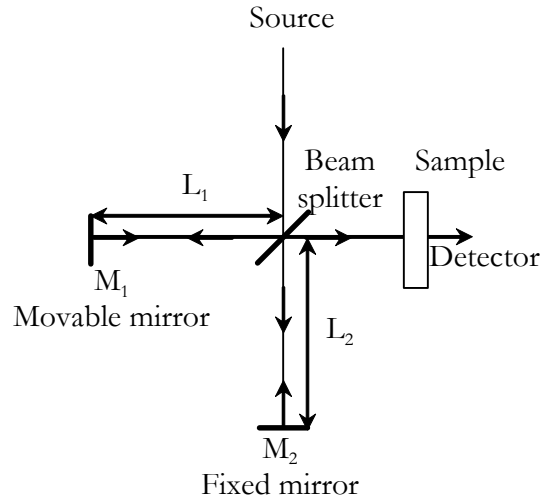


Figure 2.5. FTIR schematic.

The light intensity reaching the detector is the sum of the two beams, which are in phase and reinforce each other when $L_1 = L_2$. When M_1 is moved, the optical path lengths are unequal and an optical path difference δ is introduced. If M_1 is moved a distance x , the retardation is $\delta = 2x$ since the light has to travel an additional distance x to reach the mirror and the same additional distance to reach the beam splitter.

Consider the output signal from the detector when the source emits a single frequency or wavelength. For $L_1 = L_2$ the two beams reinforce each other because they are in phase, $\delta = 0$, and the detector output is a maximum. If M_1 is moved by $x = \lambda/4$, the retardation becomes $\delta = 2x = \lambda/2$. The two wavefronts reach the detector 180° out of phase, resulting in destructive interference or zero output. For an additional $\lambda/4$ movement by M_1 , $\delta = \lambda$ and the constructive interference results again. The detector output – the interferogram – consist of a series of maxima and minima that can be described by the equation:

$$I(x) = B(f)[1 + \cos(2\pi xf)] \quad (2.6)$$

where $B(f)$ is the source intensity modified by the sample. $B(f)$ and $I(x)$ are shown in figure 2.6(a) for this simple case. When the source emits more than one frequency, then:

$$I(x) = \int_0^f B(f)[1 + \cos(2\pi xf)]df \quad (2.7)$$

If consider a source spectral distribution, $B(f) = A$ for $0 \leq f \leq f_1$ in figure 2.6(b). The interferogram is obtained by eliminating the unmodulated term from last equation:

$$I(x) = \int_0^{f_1} A \cos(2\pi xf) df = Af_1 \frac{\sin(2\pi xf_1)}{2\pi xf_1} \quad (2.8)$$

shown in figure 2.6(b). The interferogram becomes narrower as f_1 is increased by including more frequencies.

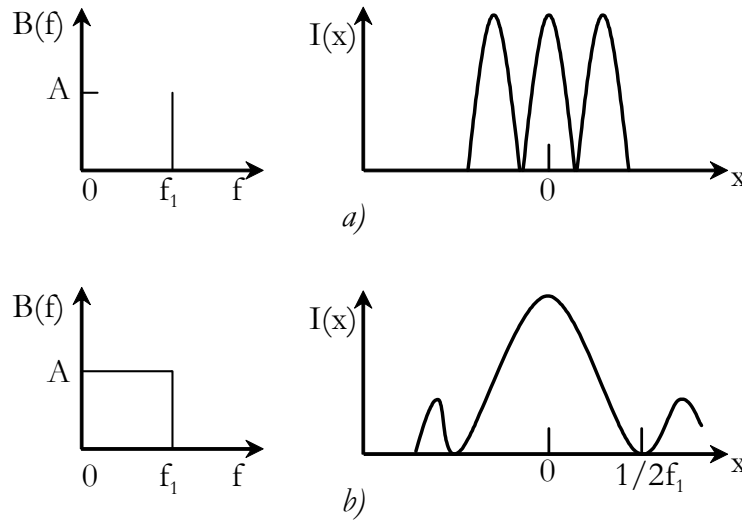


Figure 2.6. Spectrum and interferogram for a) cosine wave and b) band-limited signal.

FTIR measures the interferogram containing not only the spectral information of the source but also the transmittance characteristics of the sample. The spectral response is calculated from the interferogram using the Fourier transformation:

$$B(f) = \int_{-\omega}^{\omega} I(x) \cos(2\pi xf) dx \quad (2.9)$$

In this equation, $B(f)$ contains the spectral content of the source, the sample and the ambient in the path of the measurement. H_2O and CO_2 absorption lines are reduced by purging the apparatus with dry nitrogen. The effect of the sample is eliminated by making one measurement without the sample (background) and one with the sample. Storing the two interferograms in a computer allows the ratio of the two to be calculated, thereby eliminating the background.

X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is also known as electron spectroscopy for chemical analysis (ESCA). It is mainly used for identifying chemical species at the sample surface, allowing all elements except hydrogen and helium to be detected.

The method is illustrated with the energy band diagram in figure 2.7(a) and schematized in figure 2.7(b).

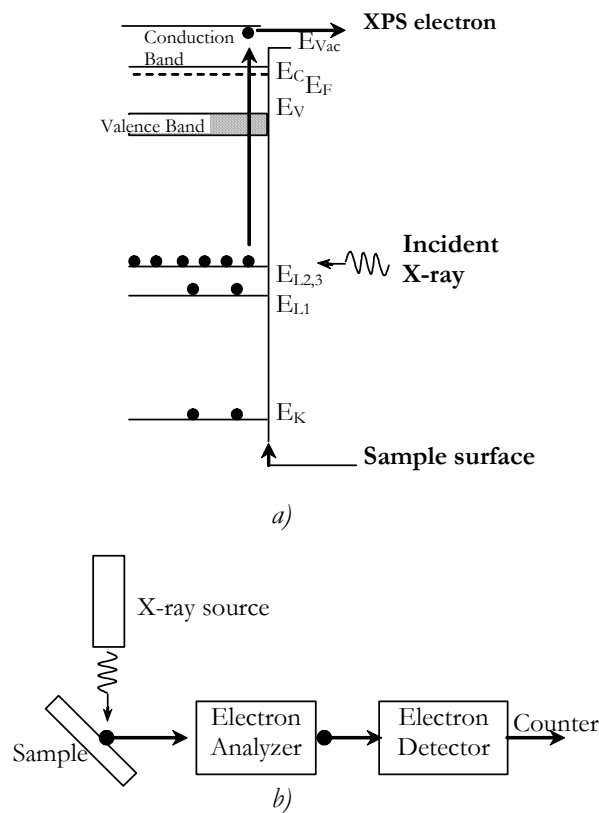


Figure 2.7. a) Electronic processes and b) schematic of an X-ray photoelectron spectroscopy.

Primary X-rays of 1 to 2 keV energy eject photoelectrons from the sample. The measured energy of the ejected electron at the spectrometer E_{sp} is related to the binding energy E_b , referenced to the Fermi energy E_F , by:

$$E_b = h\nu - E_{sp} - q\phi_{sp} \quad (2.10)$$

where $h\nu$ is the energy of the primary X-rays and ϕ_{sp} the work function of the spectrometer (3-4 eV). The spectrometer and the sample are connected forcing their Fermi levels to line up.

The electron binding energy is influenced by its chemical surroundings making E_b suitable for determining chemical states. This leads to a major strength of XPS; it allows chemical, not only elemental, identification. Although, XPS is a surface-sensitive method (despite the deeper penetration of the primary X-rays compared to a primary electron beam), depth profiling is possible by ion beam sputtering. The major use of XPS is for identification of compounds using energy shifts due to changes in the chemical structure of the sample atoms.

Transmission electron microscopy (TEM)

Transmission electron microscope is similar to optical microscopes; both contain a series of lenses to magnify the sample. The main strength of TEM lies in its extremely high resolution, approaching to 0.15 nm.

A schematic presentation of the microscope is shown in figure 2.8. With an electron gun, an electron beam is formed, which is accelerated by an electric field formed by a voltage difference of, typically, 200 kV. By condenser lenses, the electron beam is focused to a spot of the order of 1 mm on the thin film to be investigated. The first image, which is formed by the objective lens, is magnified typically $\times 25$, and the following lenses give a final magnification of the image of more than $\times 10^6$. In addition to thin-sample images, electron diffraction patterns can also be formed on the final image screen. The electron rays corresponding to *bright field imaging* and (*selected area diffraction*) are shown in the left and right drawings of figure 2.8, respectively. In *bright field*

imaging, the image of a thin sample is formed by the electrons that pass the film without diffraction, the diffracted electrons being stopped by a diaphragm. In the corresponding *dark field imaging* mode, a diffracted beam is used for imaging.

The microstructure, e.g. the grain size, and lattice defects are studied by use of the image mode, while the crystalline structure is studied by the diffraction mode. In addition, the chemical composition of small volumes, for example grain boundaries, can be obtained by detection of x-rays emitted from the film.

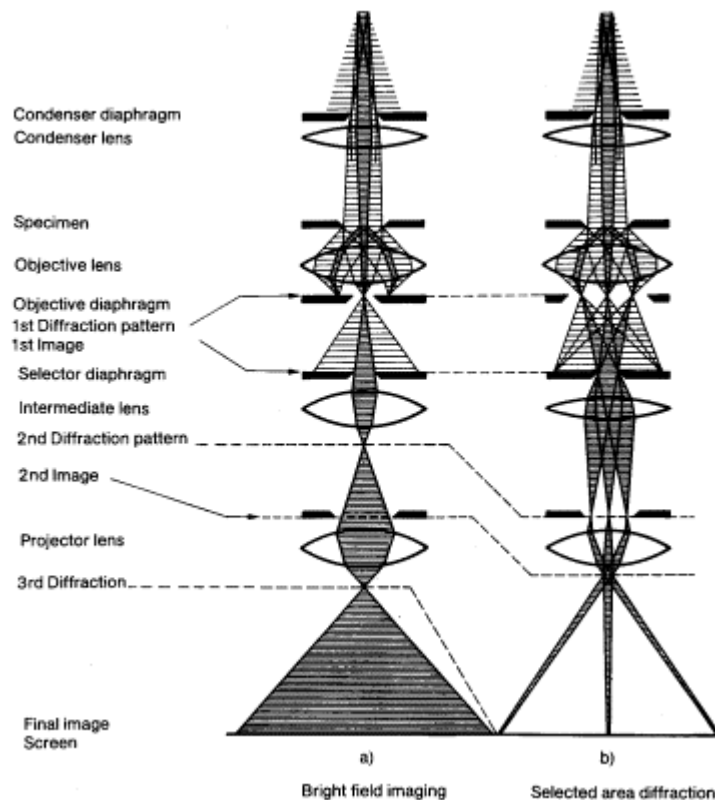


Figure 2.8 .Schematic presentation of a transmission electron microscope

Samples for electron microscopy in form of films mounted on fine-meshed grids are required to be very thin. In case near-atomic resolution is required film thicknesses have to be limited to a few tens of Å. Therefore, the quality of the electron microscopy work is sometimes limited by the thinning-down procedure as structural changes may occur during the thinning.

Energy-filtered transmission electron microscopy (EFTEM) is a technique used in Transmission electron microscopy, in which only electrons of particular kinetic energies

are used to form the image or diffraction pattern. The technique can be used to aid chemical analysis of the sample in conjunction with complementary techniques such as electron crystallography.

If a very thin sample is illuminated with a beam of high-energy electrons, then a majority of the electrons will pass through the sample but some will interact with the sample, being scattered elastically or inelastically (phonon scattering, plasmon scattering or inner shell ionisation). Inelastic scattering results in both a loss of energy and a change in momentum, which in the case of inner shell ionisation is characteristic of the element in the sample.

If the electron beam emerging from the sample is passed through a magnetic prism, then the flight path of the electrons will vary depending on their energy. This technique is used to form spectra in Electron Energy Loss Spectroscopy (EELS), but it is also possible to place an adjustable slit to allow only electrons with a certain range of energies through, and reform an image using these electrons on a detector.

The energy slit can be adjusted so as to only allow electrons which have not lost energy to pass through to form the image. This prevents inelastic scattering from contributing to the image, and hence produces an enhanced contrast image.

Adjusting the slit to only allow electrons which have lost a specific amount of energy can be used to obtain elementally sensitive images. As the ionisation signal is often significantly smaller than the background signal, it is normally necessary to obtain more than one image at varying energies to remove the background effect. The simplest method is known as the jump ratio technique, where an image recorded using electrons at the energy of the maximum of the absorption peak caused by a particular inner shell ionisation is divided by an image recorded just before the ionisation energy. It is often necessary to cross-correlate the images to compensate for relative drift of the sample between the two images.

Improved elemental maps can be obtained by taking a series of images, allowing quantitative analysis and improved accuracy of mapping where more than one element

is involved. By taking a series of images, it is also possible to extract the EELS profile from particular features.

Photoluminescence

Photoluminescence (PL) is the emission of photons generated by a material which is under an optical excitation. In this technique, the light is directed on the sample, where it is absorbed and producing an energy excess inside of the material in a process called photo-excitation. This energy excess can be released by the sample through the light emission (luminescence).

The photo-excitation produces that the electrons inside the material to move into permitted excited states. When these electrons come back to their equilibrium states, the energy excess is released, producing the light emission (radiative process). The energy of the emitted light (PL) is related to the difference between the energy levels from the electronic states involved in the transition, that is, the excited and the equilibrium state, respectively.

A typical PL set-up is shown in figure 2.9. The sample is excited with an optical source typically a laser with energy $h\nu > E_g$, generating electron-hole pairs which recombines emitting photons. The emitted light from the sample can be analyzed by a grating monochromator and detected by a photodetector.

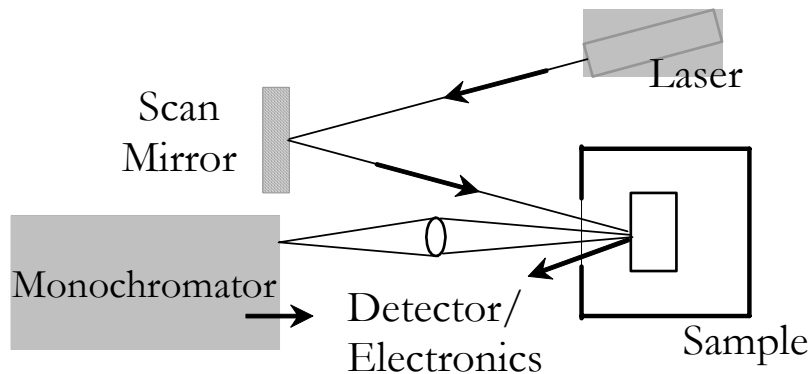


Figure 2.9. Schematic photoluminescence arrangement.

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Chapter 3

Deposition and characterization of SRO and SI-SRO films

In this chapter, the deposition process and characterization of SRO and Si implanted SRO (SI-SRO) films is reported. Moreover, the composition, microstructure and optical properties of SRO and SI-SRO films are analyzed as a function of the different technological parameters as silicon excess, Si ion implantation, and thermal annealing temperature.

3.1. Material fabrication

Several different preparation techniques of silicon sub-oxide (SiO_x , $x < 2$) films have been reported including ion implantation of Si into thermal silicon oxide [1, 2], Pulsed Laser Deposition (PLD) [3], thermal evaporation [4, 5], SiO/SiO₂ multilayers [6], Plasma Enhanced Chemical Vapor Deposition (PECVD) [3, 7-10] as well as Low Pressure Chemical Vapor Deposition (LPCVD) [11, 12]. Silicon rich oxide (SRO) films produced by techniques based on CVD method have the advantage of being more stable and compatible with standard MOS technology.

In this work, SRO films were deposited by LPCVD using pure nitrous oxide (N_2O) and 5%-nitrogen (N_2) diluted silane (SiH_4) as the reactant gasses. LPCVD is a simple

technique and commonly used in microelectronics, therefore compatible with that complementary metal oxide semiconductor (CMOS) technology. LPCVD equipment used for SRO deposition is shown in figure 3.1.



Figure 3.1. LPCVD system used for the deposition of SRO films from this work.

Deposition of SRO films was carried out on 2 in. and N type Si wafers ((100)-oriented) at temperature of 720 °C. Si excess in the deposited films is controlled by a parameter R_o defined by the equation 3.1, the ratio of partial pressure of the reactant gases of N_2O and SiH_4 . SRO films with R_o values of 10, 20, 30, and 40 were deposited with the parameters of table 3.1 and depicted in figure 3.2(a). The expected thickness of the films was about 550 nm.

$$R_o = \frac{P(N_2O)}{P(SiH_4)} \quad (3.1)$$

Ro = N ₂ O / SiH ₄	Pressure of gases (Torr)		Time (min)
	N ₂ O	SiH ₄	
10	0.600	0.600	75
20	1.060	0.053	120
30	1.400	0.047	140
40	1.400	0.035	115

Table 3.1. Parameters of deposited SRO – LPCVD films, T= 720° C.

The effect of additional silicon excess obtained by silicon ion implantation into SRO films on the microstructure and photoluminescent properties was also studied. Then, Si ions were implanted into a set of SRO (SI-SRO) samples with energy of 150 keV and a dose of $5 \times 10^{15} / \text{cm}^2$, as shown in figure 3.2(b). The projected range as calculated by TRIM simulations is about 250 nm [13].

After deposition and Si ion implantation, both sets of SRO and SI-SRO films were thermally annealed at 1100 and 1250° C for 60 minutes in a N₂ atmosphere in order to induce a Si and SiO₂ phase separation and therefore the formation of silicon nanoparticles embedded in a SiO₂ matrix, as exhibited in figure 3.2(c).

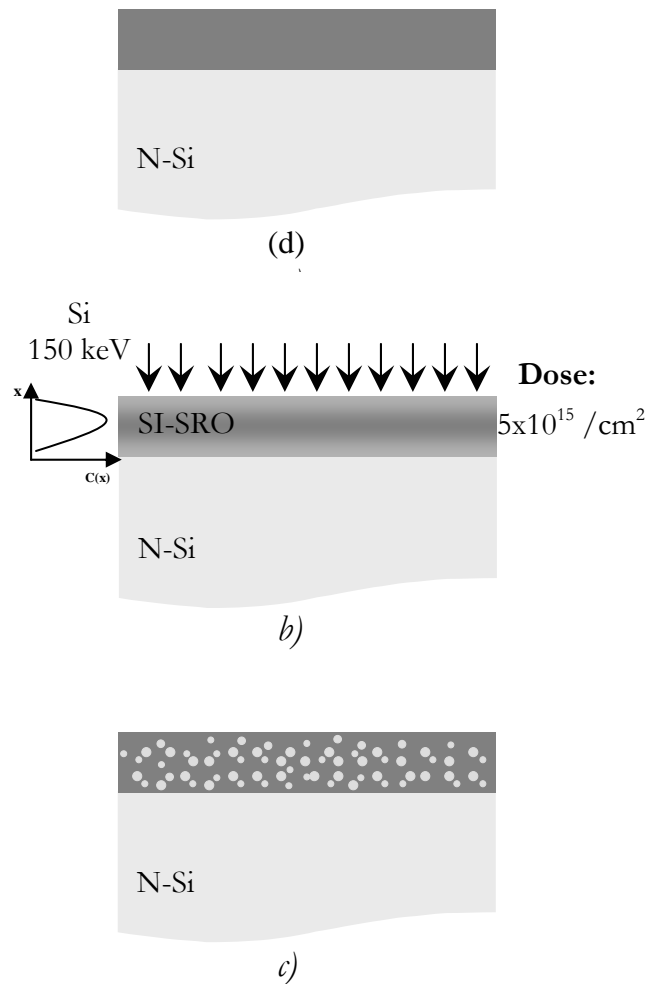


Figure 3.2. a) Deposited, b) implanted with Si ions, and c) thermally annealed SRO films.

The study of composition and microstructure of SRO films before and after applying a thermal annealing play an important role in order to understand their luminescence properties. In this sense, several techniques such as null ellipsometry, Fourier transform

infra-red spectroscopy (FTIR), x-ray photoelectron spectroscopy (XPS) and energy filtered transmission electron microscopy (EFTEM) have been used.

3.2. Characterization of the material

3.2.1. Ellipsometry

An easy way to verify the presence of Si excess in SRO films is measuring their refractive index (n). The refractive index of SiO_2 and Si is about 1.46 and 3.8 (for the real part), respectively. It is well known that n values between 1.46 and 3.8 are due to silicon excess into the film, if no other element or impurity is in the SRO films.

The thickness and refractive index of the fabricated SRO films were measured using a Gärtner L117 ellipsometer with incident laser wavelength of 632.8 nm. A mapping with 30 ellipsometry measurements was done for each SRO film. Table 3.2–3.4 show the thickness and refractive index of as-deposited SRO and thermally annealed SRO and SI-SRO films, respectively.

From table 3.2, on one hand when R_o is small (≤ 30) the refractive index is higher than 1.46 indicating the presence of silicon excess into the films. On the other hand, as R_o become higher, the refractive index tends to the SiO_2 value, as expected by the lower value of SiH_4 pressure listed in table 3.1. Thickness was higher than expected and it was different for each R_o value. Measurements on SRO films after Si implantation were not done because of the damage produced (by the implantation) to the film makes it difficult to extract the real thickness and refractive index values.

SRO $R_o = \text{N}_2\text{O}/\text{SiH}_4$	Refractive index	Thickness (nm)	
		Theoretical	Ellipsometry
10	1.99 ± 0.0900		772.8 ± 33.3
20	1.64 ± 0.0700		726.1 ± 71.8
30	1.48 ± 0.0007	550	717.0 ± 18.4
40	1.47 ± 0.0040		508.7 ± 8.8

Table 3.2. Thickness and refractive index from as deposited SRO-LPCVD films.

As shown in table 3.3 and 3.4, the thickness of SRO and SI-SRO films was reduced, if compared to the as-deposited films, after thermal annealing (1100 and 1250° C), which is due mainly to a microstructural re-ordering and densification of the material. By the contrary, the refractive index was increased, being more evident for samples with higher silicon excess.

SRO Ro =N ₂ O/SiH ₄	Thickness (nm)		Refractive index	
	1100° C	1250° C	1100° C	1250° C
10	619.0 ± 28.5	658.8 ± 19.0	2.11 ± 0.090	1.99 ± 0.060
20	655.0 ± 0.9	636.0 ± 25.3	1.77 ± 0.003	1.67 ± 0.059
30	696.6 ± 12.0	714.0 ± 14.3	1.48 ± 0.001	1.48 ± 0.002
40	492.3 ± 9.9	482.2 ± 7.8	1.47 ± 0.001	1.47 ± 0.002

Table 3.3. Thickness and refractive index from SRO-LPCVD films after thermal annealing.

SI-SRO Ro =N ₂ O/SiH ₄	Thickness (nm)		Refractive index	
	1 100 °C	1 250 °C	1 100 °C	1 250 °C
10	698.1 ± 8.2	621.4 ± 3.2	2.09 ± 0.019	2.11 ± 0.010
20	746.2 ± 24.3	732.4 ± 79.5	1.62 ± 0.02	1.85 ± 0.070
30	687.6 ± 9.3	690.8 ± 11.8	1.48 ± 0.001	1.48 ± 0.002
40	507.2 ± 4.7	480.5 ± 3.1	1.45 ± 0.004	1.46 ± 0.001

Table 3.4. Thickness and refractive index from SI-SRO-LPCVD films after thermal annealing.

3.2.2. Fourier Transform Infra-red Spectroscopy (FTIR)

Since FTIR is a non-destructive technique, a FTIR BRUCKER Vector 22 spectrometer was employed to study the composition and structure of the SRO and SI-SRO films. The scanned range was between 350 cm⁻¹ and 3500 cm⁻¹ with 2.5 cm⁻¹ of resolution.

Figures 3.3 and 3.4 show the IR absorbance spectra obtained from SRO and SI-SRO films before and after annealing, respectively. It has been reported that SRO films deposited by the mixture of N₂O and SiH₄ display absorption bands associated with SiN, NH, SiH and OH vibrations in addition to the three characteristic bands related to

the Si-O-Si bonding arrangement [14]. However, the presence of some nitrogen and hydrogen characteristic peak was not observed in the IR spectra of the films. Only three vibration bands related to Si-O-Si rocking (TO_1), Si-O-Si bending (TO_2) and Si-O-Si stretching (TO_3) appeared [8, 14], as observed in figures 3.3 and 3.4.

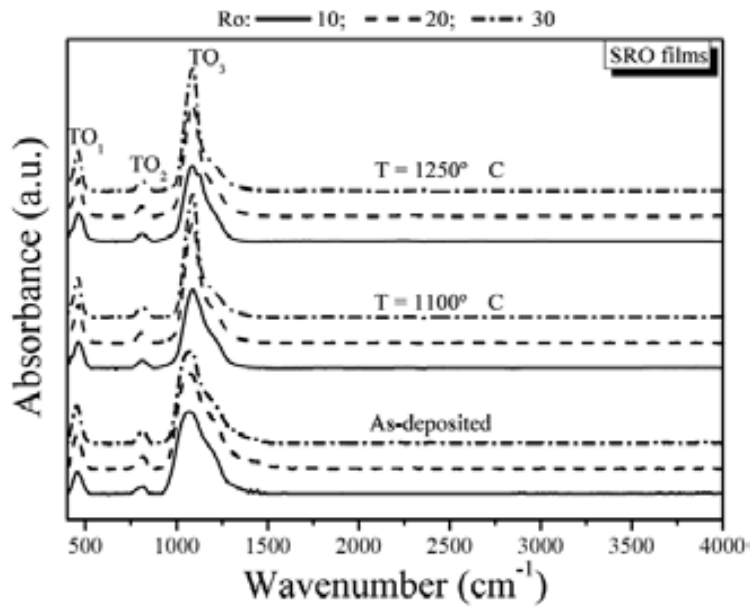


Figure 3.3. Infrared absorption spectra of SRO films before and after thermal annealing.

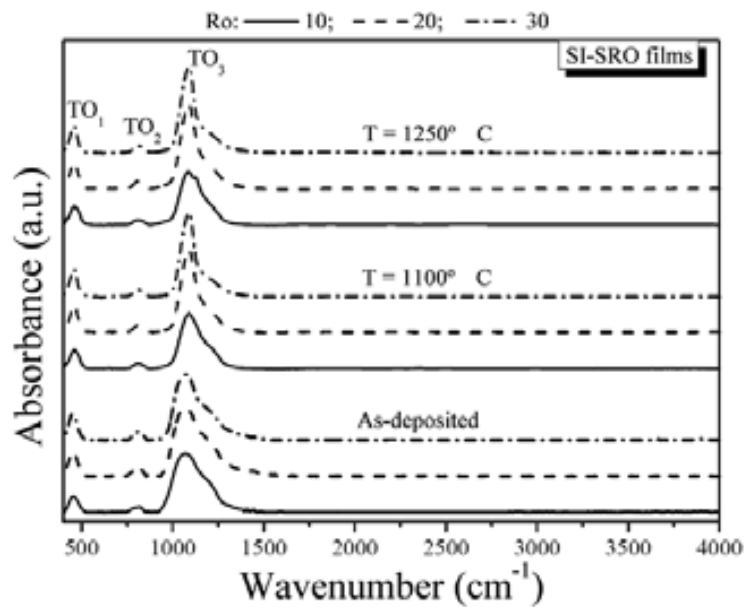


Figure 3.4. Infrared absorption spectra of SI-SRO films after thermal annealing. IR from SRO as deposited films is shown for comparison.

The dominant feature in the IR spectrum is associated to the stretching motion of the oxygen atoms (TO_3). A shifting in the frequency of the TO_3 mode is associated with the presence of silicon excess and with a change in the microstructure of the material [8, 15]. It has been reported that the peak position of the TO_3 mode shifts with the film thickness. For a thermally grown 400 nm thick SiO_2 film, the TO_3 mode and its full width at half maximum (FWHM) are about 1088 and 85 cm^{-1} , respectively [16].

For as-deposited SRO films and with the highest silicon excess ($Ro = 10$), the TO_1 , TO_2 and TO_3 vibration bands were placed at 458, 818 and 1069 cm^{-1} , respectively as enlisted in table 3.5. The TO_1 , TO_2 modes remains almost at the same frequency for all SRO films with different silicon excess. However, the TO_3 band slightly shifted toward higher frequencies and its FWHM was reduced as Ro was changed from 10 to 40 corresponding to a larger oxygen concentration and to the presence of different bonding arrangement (microstructural disorder), respectively [8, 14, 15]. This effect is directly related to the decrease in the refractive index (n) of the as-deposited SRO films where n tends to the SiO_2 value as Ro is varied from 10 to 40.

Ro = N ₂ O/SiH ₄	Vibration mode (cm^{-1})			FWHM (cm^{-1})
	<i>TO₁</i> (Si – O Rocking)	<i>TO₂</i> (Si – O Bending)	<i>TO₃</i> (Si–O Stretching)	
10	458.1	818.8	1069.5	210.6
20	452.5	817.9	1072.3	207.8
30	451.6	817.9	1073.2	178.9
40	454.4	819.8	1072.3	125.8

Table 3.5. IR Vibration bands of SRO as deposited films.

Another shift and width (FWHM) reduction of the TO_3 vibration band was obtained when the SRO and SI-SRO films were subjected to a thermal annealing at both temperatures of 1100 or 1250° C. On the one hand, the TO_3 vibration band was placed at about 1088 cm^{-1} for all films, independently of the flow ratio (Ro) and silicon implantation, as indicated in tables 3.6 and 3.7. On the other hand, the FWHM was reduced after thermal annealing indicating a strong arrangement on the microstructure of the films. In addition, the FWHM decreases as Ro increases (lower silicon excess).

Due to the silicon excess inside these films, these changes are ascribed to a phase separation of Si and SiO₂ in the SRO films.

Ro	Annealing (N ₂), t = 60 min.						FWHM	
	1 100°C			1 250°C			(cm ⁻¹)	
	Vibration Bands (cm ⁻¹)						1 100°C	1 250°C
	TO ₁	TO ₂	TO ₃	TO ₁	TO ₂	TO ₃		
10	461.4	811.5	1088.9	461.4	811.5	1086.7	134.31	143.12
20	461.4	811.5	1088.9	461.4	811.5	1088.9	99.08	99.08
30	459.4	811.5	1088.9	461.4	811.5	1088.9	83.66	83.66
40	459.4	811.5	1088.9	459.2	809.3	1086.7	81.46	81.46

Table 3.6. IR vibration bands of SRO films thermally annealed at 1100 and 1250°C for 60 minutes.

Ro	Annealing (N ₂), t = 60 min.						FWHM	
	1 100°C			1 250°C			(cm ⁻¹)	
	Vibration Bands (cm ⁻¹)						1 100°C	1 250°C
	TO ₁	TO ₂	TO ₃	TO ₁	TO ₂	TO ₃		
10	461.4	811.5	1088.9	461.4	811.5	1086.7	136.50	143.12
20	461.4	811.5	1088.9	461.4	811.5	1088.9	99.08	101.28
30	459.2	811.5	1088.9	461.4	811.5	1088.9	83.66	83.66
40	459.2	811.5	1086.7	459.2	809.3	1086.7	79.26	81.46

Table 3.7. IR vibration bands of SI-SRO films thermally annealed at 1100 and 1250°C for 60 minutes.

An important feature is observed in the IR-TO₃ mode for SRO and SI-SRO films with Ro = 10. Figure 3.5 shows the evolution of the TO₃ mode at different temperatures of anneals. For as-deposited film, a broad peak is observed with a maximum at 1069 cm⁻¹. However, as mentioned before, the FWHM reduces after thermal annealing and the maximum peak shifts towards higher wavenumber. Both, microstructural arrangement and high silicon excess in the SRO film produced that the TO₃ mode splits into two peaks when the temperature of anneal was 1250° C. The first one placed at ~1088 cm⁻¹ and the second one at ~1124 cm⁻¹, as shown in figure 3.5.

It has been reported that the shoulder located on the high wave-numbers side of the TO_3 mode is the result of the overlapping of higher frequency bands attributed to three symmetric stretching modes: two longitudinal optical (LO_2 and LO_1) modes at 1150 and 1250 cm^{-1} and one transverse optical TO_4 mode at 1200 cm^{-1} [15]. Then, the absorption peak at 1124 cm^{-1} could be a result of larger phase separation between Si and SiO_2 .

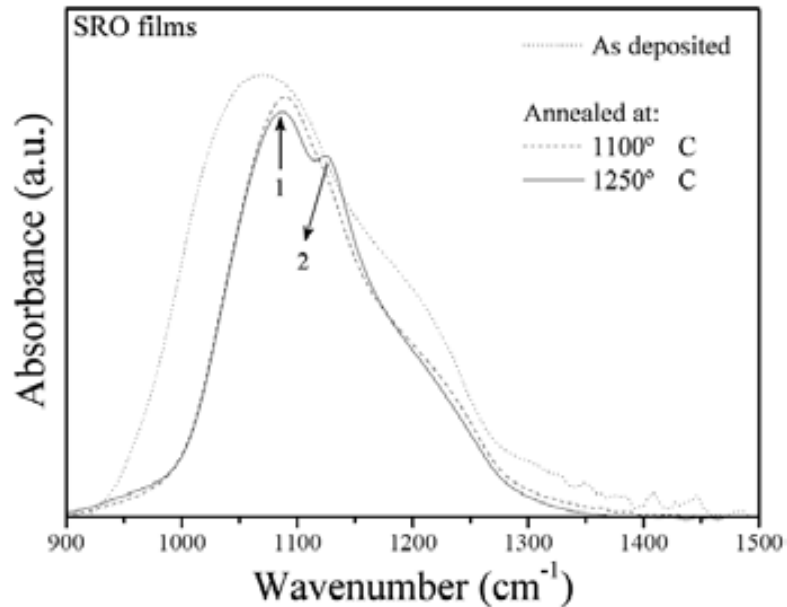


Figure 3.5. FTIR absorption spectra of SRO films with $R_o = 10$ before and after thermal annealing in the 900 to 1500 cm^{-1} range.

3.2.3. X-ray Photoelectron Spectroscopy (XPS)

XPS is a technique used for surface chemical analysis which allows obtaining the atomic percent of different elements of an analyzed sample, besides of information about the chemical states from each element.

The silicon excess in SRO and SI-SRO films was measured with a PHI ESCA-5500 X-ray photoelectron spectrometer using a monochromatic Al radiation source with energy 1486 eV. Depth composition profiles inside the films were obtained measuring by XPS in the surface, then etching and measuring again. XPS analysis was done on thermally annealed samples.

The silicon (Si) and oxygen (O) concentration in SRO films as measured by XPS are depicted in figure 3.6(a) and 3.6(b), respectively for different Ro values. As it was expected, the silicon excess varies depending on the flow ratio (Ro). For SRO films with Ro = 40, the silicon profile stays about 35.5 at.% and it increases until 46 at.% as Ro value reduces to 10. A thin silicon dioxide layer is formed at the SRO surface for low Ro values; which can be explained by the silicon excess oxidation with air.

A nitrogen profile was also observed, however is very low (around 0.8 at.%) as compared to other works reported for SRO-PECVD films where the N incorporation is about 10 at.% [10]. Table 3.8 summarizes the silicon excess in the SRO films. It is observed that Si concentration ranging between 35.5 and 46 at.%.

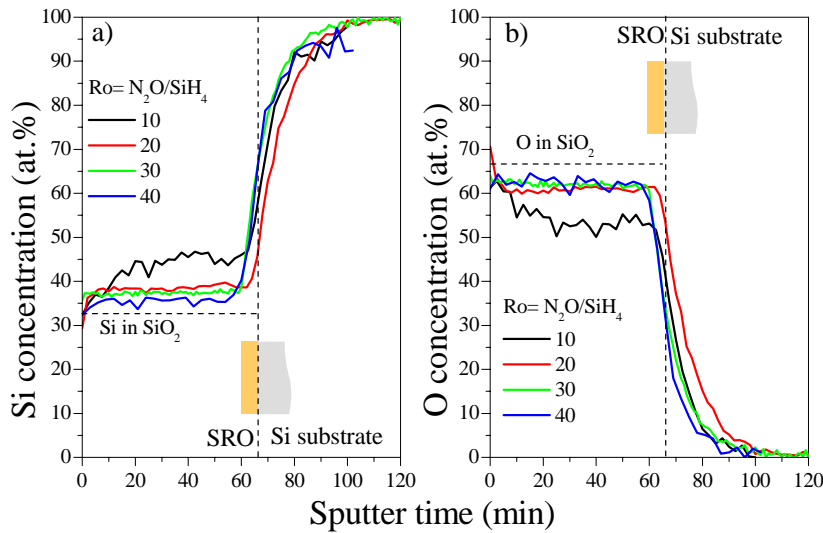


Figure 3.6. a) Silicon and b) Oxygen concentration in SRO films with different flow ratio (Ro) values as measured by XPS.

Ro = N ₂ O/SiH ₄	Si excess (at.%)	Concentración (%)			x = O / Si
		O	Si	N	
10	12.7	54.00	46.00	0.00	1.17
20	5.1	60.81	38.46	1.00	1.58
30	4.0	62.01	37.35	0.62	1.66
40	2.2	64.50	35.50	0.00	1.81

Table 3.8. Silicon excess of thermally annealed SRO films obtained by XPS.

Figure 3.7 indicates the composition of the thermally annealed SRO and SI-SRO films with flow ratio, $Ro = 30$. For the SRO film, the results indicate a uniform silicon and oxygen profile. The Si and O profiles in the SI-SRO film oscillates around the corresponding Si and O profiles of non-implanted SRO film. These oscillations were a feature of all the SI-SRO films. This behaviour could be the result of Si implantation, because Si and O atoms are displaced from their position. Using SRIM [13] simulation, the expected silicon excess by implantation is estimated to be ~ 0.4 at.%. Although XPS measurements showed a silicon excess similar to that SRO films, the SI-SRO films should have a 0.4 at.% of silicon excess above of the non-implanted SRO films reported in table 3.8. This effect could be due to the resolution of the XPS equipment.

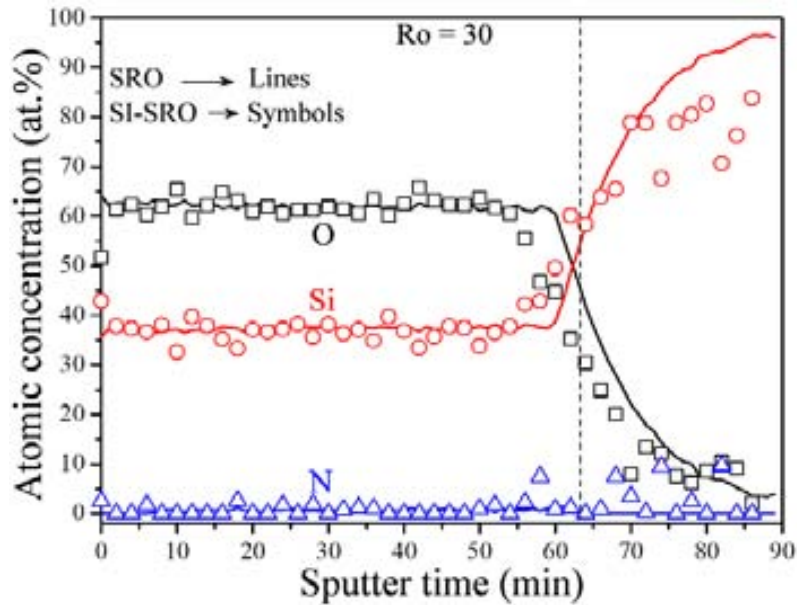


Figure 3.7. XPS composition profile of thermally annealed SRO and SI-SRO films with $Ro = 30$.

Analysis of Si2p-XPS peak

The Si2p peaks obtained from XPS spectra of the SRO films were also analyzed. There are two models describing the microstructure of SiO_x ($x < 2$) films. First the random bonding model (RBM) [3, 9, 12, 17], in which the silicon environment can be distinguished between five different tetrahedral units, $Si-(Si_{4-n}-O_n)$ with $n = 0-4$, corresponding to five possible oxidation states of silicon (Si^0 , Si^{1+} , Si^{2+} , Si^{3+} and Si^{4+}). The second model, the random mixtures model (RMM) [12, 18], suggests SiO_x ($x < 2$)

films consist of $Si-Si_4$ (Si^0) and $Si-O_4$ (Si^{4+}) tetrahedras, neglecting the existence of intermediate states.

Figure 3.8 shows the Si2p-XPS peak of the $SRO_{12.7}$, $SRO_{5.1}$, SRO_4 films annealed at 1100° C; the sub-index in the notation refers to the silicon excess. As it is shown, an almost symmetric peak is observed at 104.3 and 103.8 eV for the SRO_4 and $SRO_{5.1}$ films, respectively. Then, according to the RMM model, these $SRO_{5.1}$ and SRO_4 films should be stoichiometric; however, a phase separation must take place in these samples due to the high annealing temperature ($\gg 700$ °C). Indeed, it has been reported that a phase separation starts at temperatures of 400-700 °C [9]. As it can be seen, the peak energy shifts toward a lower energy when the silicon excess is increased, at the same time that the distribution width becomes broader, indicating the contribution of different oxidation states, in agreement with the description of the RBM model.

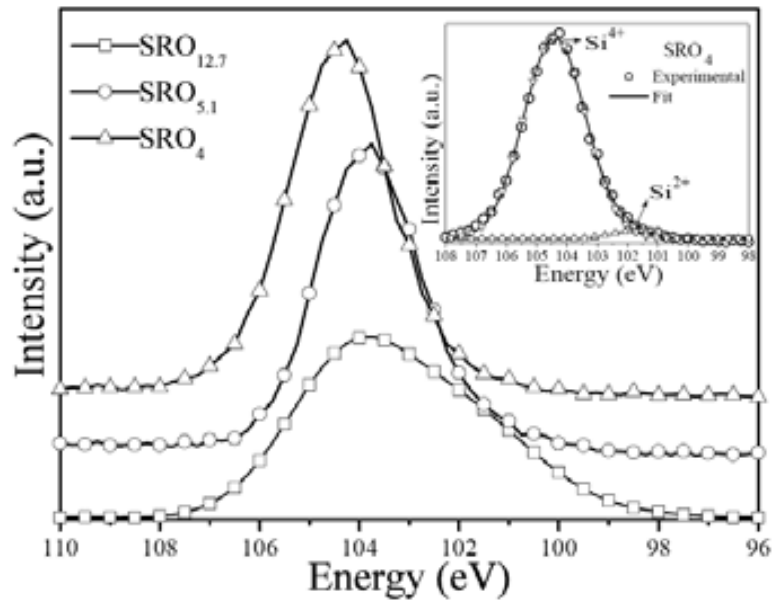


Figure 3.8. Variation of the Si2p peak in the SRO films thermally annealed at 1100 °C respect to the silicon excess. Inset: Si2p peak fitting of SRO_4 film.

The inset of figure 3.8 shows the fitting Si2p-XPS peak for SRO_4 film using Gaussian components. It has been found a contribution of two peaks placed at 101.9 and 104.4 eV related to Si^{2+} ($Si-Si_2O_2$) and Si^{4+} ($Si-Si-O_4$), respectively. The strongest component is associated to pure silicon dioxide, as expected due to the low silicon excess. The fitting of the Si2p-XPS peak for $SRO_{5.1}$ film produced the same oxidation states, Si^{2+} and Si^{4+} , but an increasing in the area of the Si^{2+} peak was observed, as shown in table 3.9.

The presence of Si^0 was not observed in these SRO_4 and $\text{SRO}_{5.1}$ films, indicating the absence of $\text{Si}-\text{Si}_4$ tetrahedra. The low silicon excess in these films could be the cause of this behaviour, that is, the phase separation forming Si-nanoparticles inside of a SiO_2 matrix could be present; however, it is possible that the size of Si-nanoparticles compared to the SiO_2 matrix surrounding them is relatively small, being easier to detect the $\text{Si}-\text{Si}-\text{O}_4$ component in the Si2p-XPS peak.

When the silicon excess was increased ($\text{SRO}_{12.7}$), the Si2p spectra displayed an asymmetrical peak, indicative of the presence of larger concentration of suboxide components. In this film, the fitting produced as well as the Si^{2+} and Si^{4+} peaks, the peak corresponding to Si^0 indicating the presence of elemental silicon. Nevertheless, the areas corresponding to elemental silicon (Si^0) and suboxide (Si^{2+}) were smaller than SiO_2 (Si^{4+}) area. Table 3.9 shows the peaks and area from different oxidation states.

Oxidation state	$\text{SRO}_{12.7}$			$\text{SRO}_{5.1}$			SRO_4		
	Peak	Area	Width	Peak	Area	Width	Peak	Area	Width
Si^0 ($\text{Si}-\text{Si}_4$)	98.7	0.52	1.9	-	-	-	-	-	-
Si^{2+} ($\text{Si}-\text{O}_2-\text{Si}_2$)	101.8	22.3	2.8	101.8	4.62	1.9	101.9	1.4	1.3
Si^{4+} ($\text{Si}-\text{O}_4$)	104.1	32.5	2.5	103.9	48.9	1.9	104.4	58.5	2.0

Table 3.9. Oxidation states obtained from Si2p peaks.

3.2.4. Energy Filtered Transmission Electron Microscopy (EFTEM)

In order to know the microstructure of SRO and SI-SRO films and corroborate the Si-nanoparticles formed inside of these films after thermal annealing, some samples were analyzed by means of Energy Filtered Transmission Electron Microscopy technique. EFTEM images were obtained using a JEOL JEM 2010F electronic microscope. All the EFTEM images were measured using a Si plasmon of 17 eV and cross-section views.

Cross view EFTEM images from whole SRO films are shown in figure 3.9. The thickness of these samples is about 605, 780, and 765 nm for $\text{Ro} = 10, 20,$ and $30,$ respectively. These values are slightly above to the measured by ellipsometry, except for

SRO_{12.7}. Nevertheless, the EFTEM images indicate the approximate value of only one point, meanwhile the ellipsometric measurements is the result of an average value.

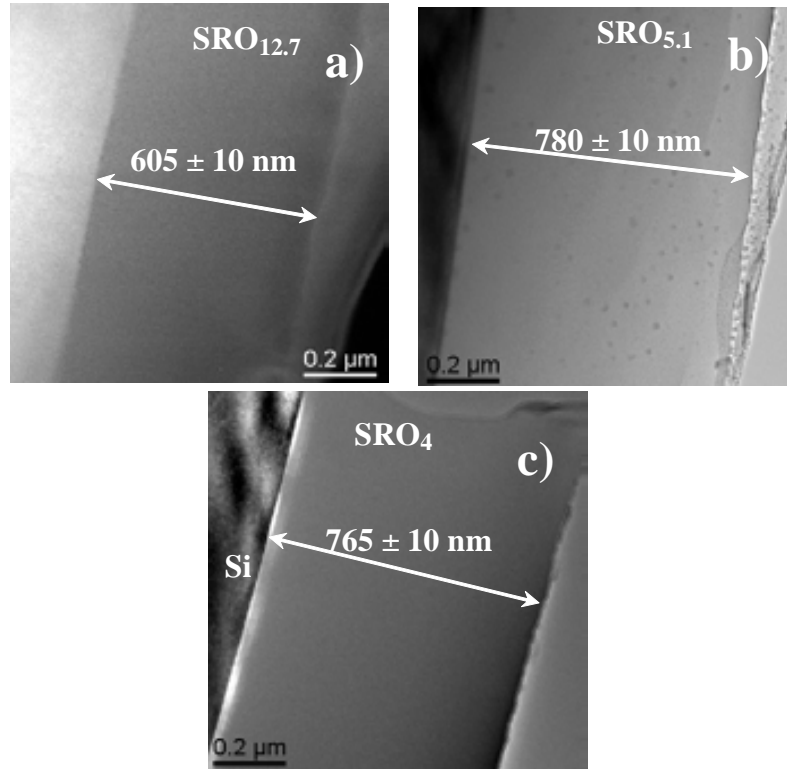


Figure 3.9. Cross view EFTEM images of SRO films with (a) 12.7, (b) 5.1 and (c) 4 at.% of silicon excess and annealed at 1100° C for 60 minutes. The image shows the real thickness of SRO films.

Figure 3.10 shows the cross view EFTEM images and the size distribution of Si-nanoparticles for the SRO films after thermal annealing at 1100° C for 60 minutes. In all of these images, the bright zones are associated to the presence of silicon in the film.

Figure 3.10(a) indicates the presence of silicon agglomeration forming Si-nanoparticles in the SRO film with 12.7 at.% of silicon excess. Meanwhile some of the Si-nps show an elliptical shape, other has an enlarged one, which could be a result of the agglomeration of neighboured Si-nps. A great dispersion of sizes is observed; the size is in the 0.5 to 7.5 nm range, being the mean size around 4.1 nm as indicated in the histogram.

Figure 3.10(b) shows the EFTEM image for the SRO film with 5.1 at.% of silicon excess. Si-nps are also observed in this film. The image exhibits Si-nps uniformly distributed into the SRO film. The Si-nps size extended from 1.5 up to 4 nm, with an average size of 2.7 nm, as indicated in the histogram. That is, a narrower distribution in

Si-nps size was obtained in this film compared to the higher Si-excess. In this film, the Si-nps present a spherical-like shape and agglomeration between Si-nps is not observed.

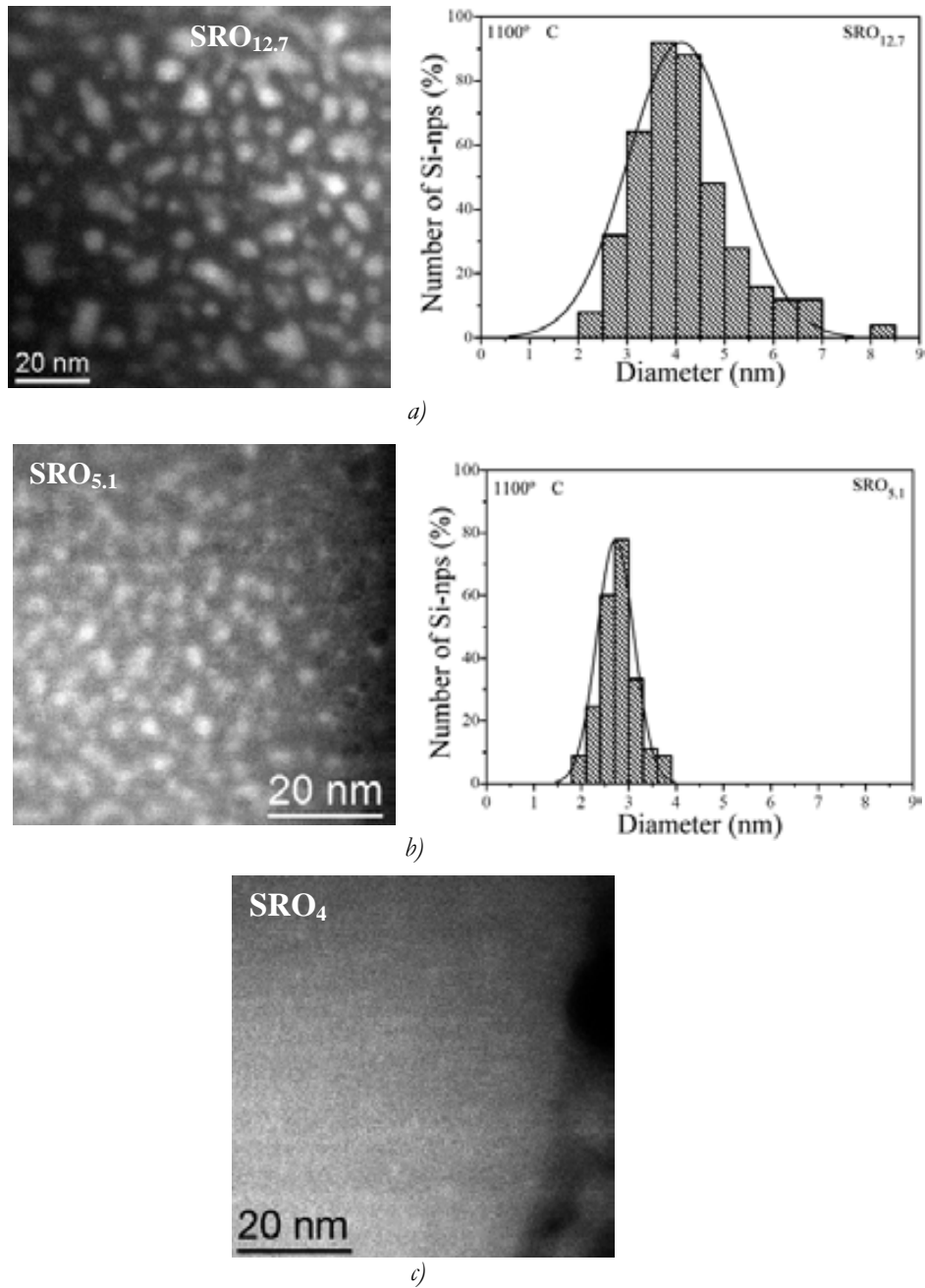


Figure 3.10 . Cross view EFTEM images and size distribution of Si-nps in SRO films with (a) 12.7, (b) 5.1 and (c) 4 at.% of silicon excess annealed at 1100° C for 60 minutes.

Si-nps were not observed at the first instance in the SRO film with 4 at.% of silicon excess, as seen in the EFTEM image from figure 3.10(c) and 3.11(a). However, silicon excess exists within the film; therefore Si-nanoparticles could be present inside as reported in another paper [19]. It is possible that the relatively small size of the Si-nps

and their probably amorphous nature are the causes that prevented their observation with EFTEM at first glance. In fact, a detailed study of this sample shows that Si-nps were observed after the sample remains under the electron beam for a few seconds, as exhibited in figure 3.11(b) and 3.11(c). These images indicate some slightly bright zones. However, because of low contrast and sharpness, the contour and size of the Si particles is not clear, but it is expected to be lower than 2.7 nm because the low silicon excess in these films.

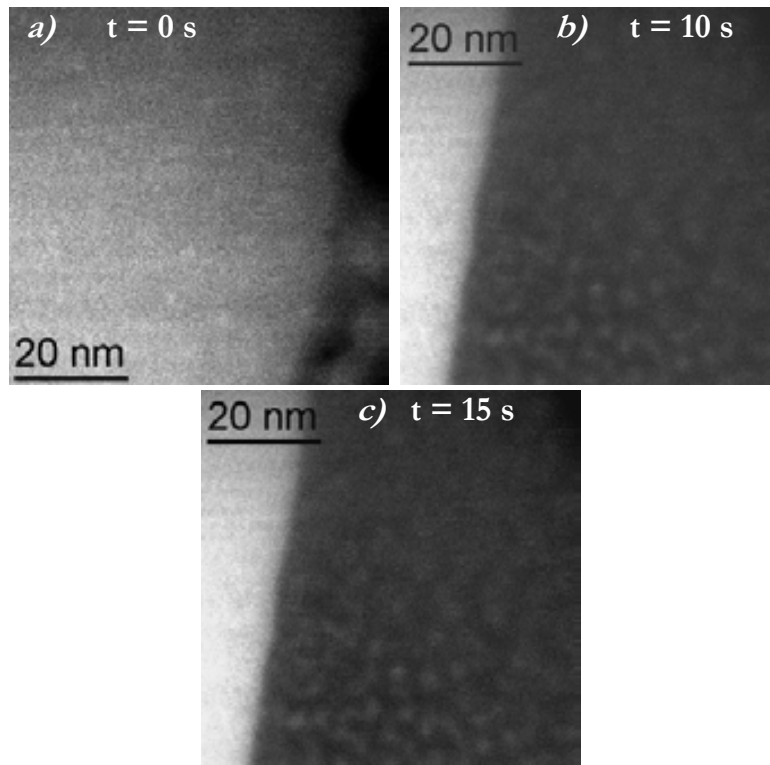


Figure 3.11. Observation of Si-nps during a) 0, b) 10, and c) 15 seconds of electron beam exposure in EFTEM measurements.

The analysis of the Si2p–XPS peak from SRO₄ and SRO_{5.1} films did not show the presence of elemental silicon agglomeration (Si⁰), contrary to EFTEM measurements where Si-nps were observed. This could be ascribed to the low sensitivity of Si2p–XPS in SRO films with low silicon excess, moreover, it has been reported that the clustered silicon concentration is significantly lower than the initial silicon excess concentration [20].

Figure 3.12 shows the EFTEM images and histograms of the Si-nps inside the SRO film with 5.1 at.% of silicon excess annealed at different temperatures and from that SRO

film implanted with silicon (SI-SRO_{5.1}) and annealed at 1100° C. On the one hand, the silicon agglomeration increases when the temperature of annealing increased (1250° C) forming Si-nps of larger size. On the other hand, the silicon implantation in SRO (SI-SRO) films produced an increasing in the number of Si-nps.

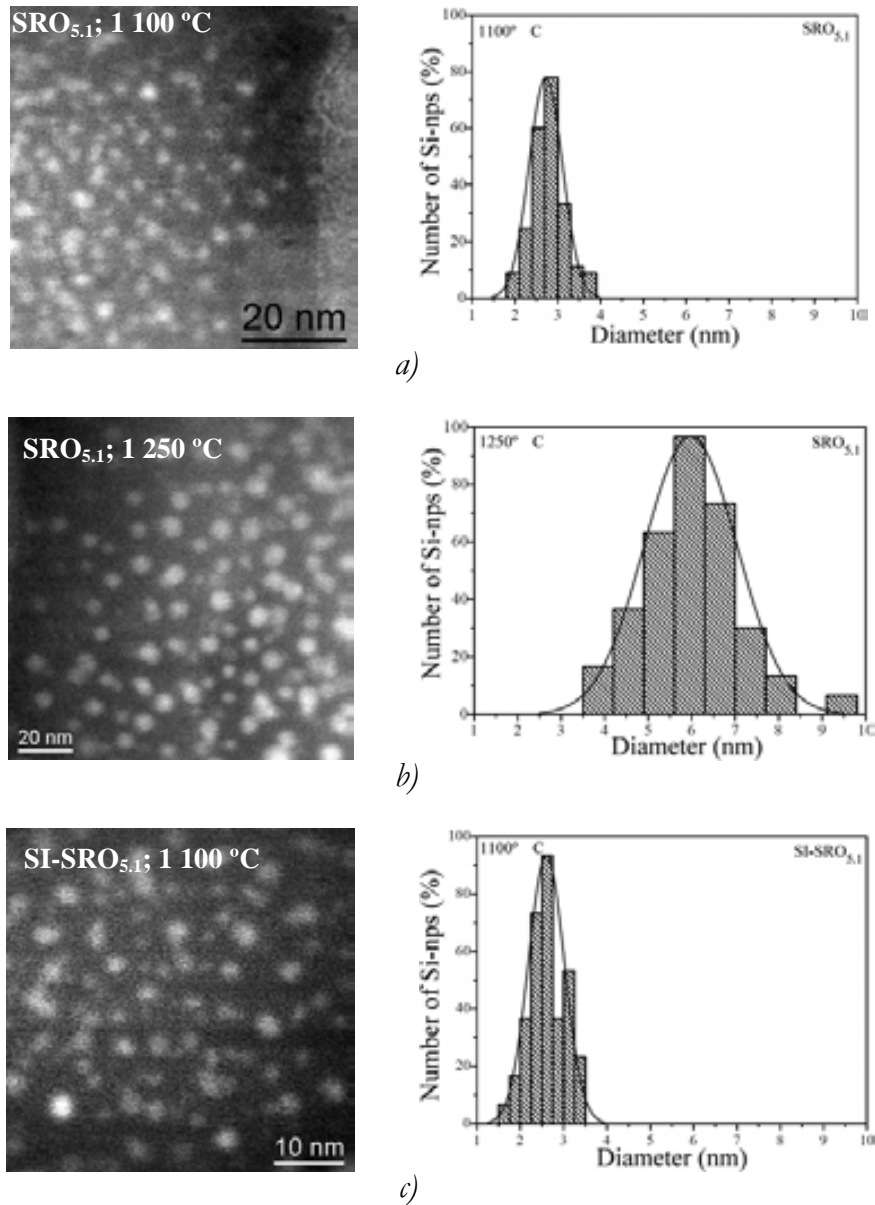


Figure 3.12. Cross view EFTEM images and size distribution of Si-nps in SRO films with 5.1 at.% of silicon excess annealed at (a) 1100 , (b) 1250° C and SI-SRO annealed at (c) 1100° C for 60 minutes.

Si-nps with a mean size of 2.7 nm are clearly observed after 1100° C as shown in figure 3.12(a). However, at 1250° C of anneal, the number and size of Si-nps becomes larger and with a broader distribution, as observed in figure 3.12(b). The silicon agglomeration

was also increased when the SRO film was implanted with silicon ions and annealed at 1100° C; see figure 3.12(c). It can be observed that the number of Si-nps with size below 2.7 nm was increased if compared to the non-implanted SRO film. The average size of the Si-nps inside the SI-SRO film was about 2.6 nm, almost the same that the SRO film without implantation.

3.2.5. Photoluminescence (PL)

Room temperature PL and PL excitation (PLE) measurements were carried out with a Perkin-Elmer spectrometer LS-50B model with a Xenon source. The samples were excited using a 250 nm radiation and the emission signal was collected in wavelength region of 400-900 nm with a resolution of 2.5 nm. A cut-off filter to pass only wavelengths above 430 nm was used to block the light scattered from the source. PLE spectra were scanned in the 200-400 nm range also with a resolution of 2.5 nm.

Figure 3.13 shows the PL spectra normalized to thickness for the SRO and SI-SRO films thermally annealed at 1100° C. All the films exhibited a PL band in the 1.4–2.1 eV range. A dependence of the PL peak energy and its intensity on the silicon excess is observed.

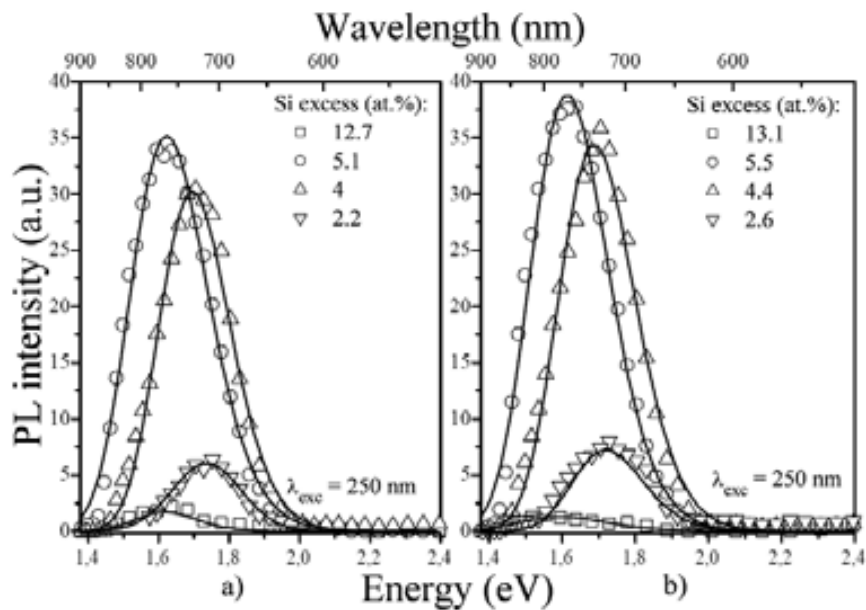


Figure 3.13. PL spectra from a) SRO and b) SI-SRO films with different silicon excess and annealed at 1100° C for 60 min. Symbols are experimental data and lines are the Gaussian fits.

The SRO film with the highest (12.7 at.%) silicon excess emitted a PL peak at 1.62 eV, but with a very low intensity, as observed in figure 3.13(a). As the silicon excess reduces to 5.1 at.%, the PL intensity increases for 20 times. In spite of a difference in the mean size of the Si-nps between these two films, 4.1 nm for 12.7 at.% and 2.7 nm for 5.1 at.% of silicon excess, the PL peak remains at the same energy. On the other hand, the SRO film with 4 at.% of silicon excess showed a PL peak at 1.69 eV; that is, a redshift took place when the silicon excess was increased from 4 to 5.1 at.%. Although the PL intensity is almost similar, Si-nps were not clearly observed by EFTEM in SRO film with the 4 at.% of silicon excess. For the SRO film with the lowest Si-excess (2.2 at.%), the PL peak shifted towards 1.74 eV but with a small intensity.

The PL peaks emitted by the SI-SRO films were at the same energy that non-implanted SRO films, as exhibited in figure 3.13(b); nevertheless, a more intense photoluminescence (see scales in figure 3.13) was obtained with the Si implantation, which is produced by an increasing in the density of Si-nps, as measured by EFTEM.

When the annealing temperature is increased to 1250° C, PL emission in both SRO and SI-SRO films practically disappeared, as shown in figure 3.14 (compare scales between figs. 3.13 and 3.14).

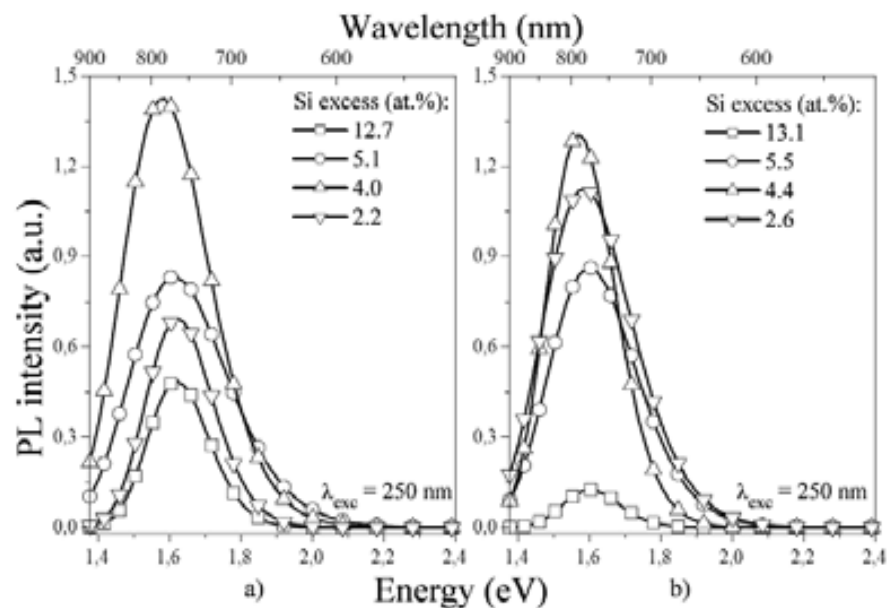


Figure 3.14. PL spectra from a) SRO and b) SI-SRO films with different silicon excess and annealed at 1250° C for 60 min.

The energy of the emission peak does not seem to depend on the silicon excess, contrary to the intensity. A maximum emission was observed with the SRO_4 film. However, as mentioned before, the emission of these films is extremely low compared to that annealed at 1100°C .

A comparison of the PL emitted by the SRO films with 5.1 at.% of silicon excess with and without Si implantation annealed at 1100°C and that $\text{SRO}_{5.1}$ film annealed at 1250°C is observed in figure 3.15.

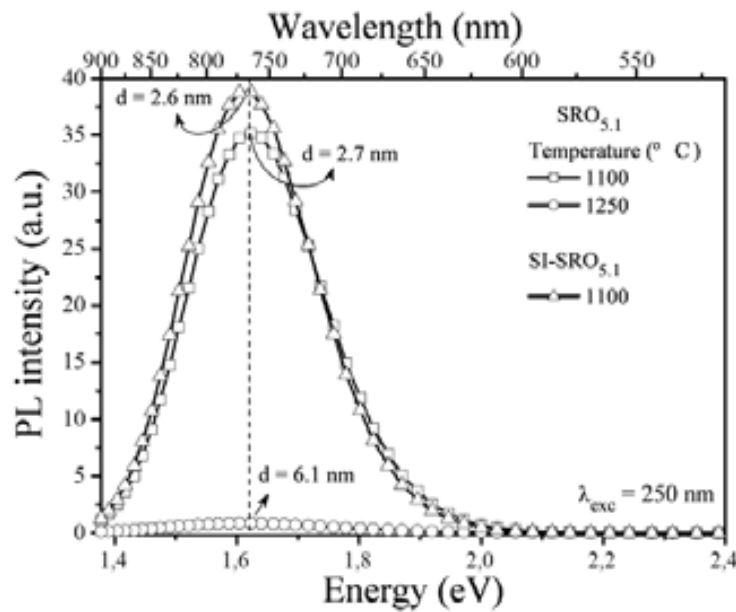


Figure 3.15. PL dependence on the temperature and Si implantation in SRO film with 5.1 at.% of silicon excess.

A maximum PL peak is observed at the same energy for samples annealed at 1100°C , which contains Si-nps of 2.6 nm and 2.7 nm in size, however for the SRO film annealed at 1250°C where larger Si-nps ($\sim 6.1\text{ nm}$) were created, changes in the PL peak position are not observed, it remains at $\sim 1.62\text{ eV}$ for all samples. Contrary to this, the PL intensity seems to depend on the size of the Si-nps.

PL intensity of 35 a.u. was observed in the SRO film annealed at 1100°C (Si-np of 2.7 nm); when the annealing temperature was increased to 1250°C (Si-np of 6.1 nm), the PL intensity was dramatically reduced by more than 40 times. However, the SRO implanted with silicon and annealed at 1100°C (Si-np of 2.6 nm) emitted the most

intense PL. Then, there exist a direct relation between the Si-np size and the PL intensity rather than with the emission energy. All the SRO and SI-SRO films annealed at 1250° C exhibited a PL of very low intensity. In these films annealed at 1250° C, the Si-np size is expected to be larger than the annealed at 1100° C, such as depicted by EFTEM images.

In order to clarify the photoabsorption process of the red PL peaks emitted by the SRO and SI-SRO films, PL excitation (PLE) spectra were measured. Figure 3.16(a) and 3.16(b) exhibit the PLE spectra from SRO and SI-SRO films annealed at 1100° C, respectively. All spectra show an intense peak at around 225 nm, independently of the emission energy and the excess silicon. The peak intensity at 225 nm grows as the silicon excess increases for both SRO and SI-SRO films; however, it practically disappears for the highest excess. PL intensity decreases as the excitation wavelength is larger than 225 nm for all films. An increasing in the PL intensity was obtained in all SRO and SI-SRO films when they were excited with a wavelength of 225 nm.

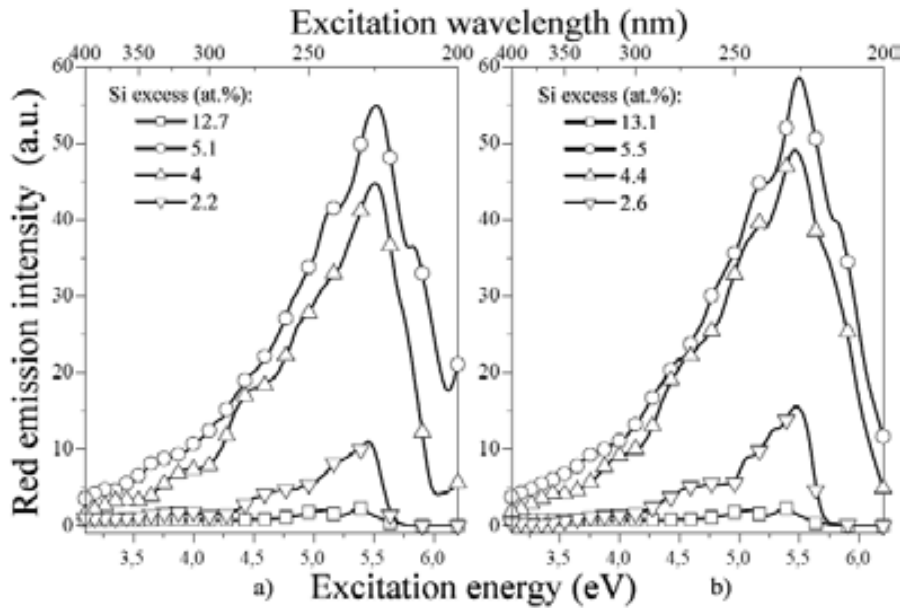


Figure 3.16. PLE spectra from a) SRO and b) SI-SRO films with different silicon excess and annealed at 1100° C for 60 min.

Although the PL intensity is low when SRO films are excited with wavelength larger than 225 nm, an intense red PL is observed for SRO_{5.1} film when excited with a He-Cd laser ($\lambda_{exc} = 320$ nm), even at naked eye, as shown in figure 3.17.

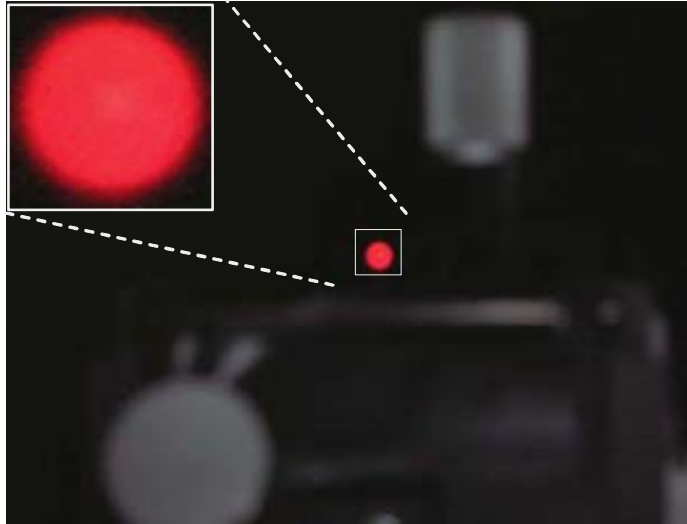


Figure 3.17. Red emission in the $\text{SRO}_{5.1}$ film excited with a He–Cd ultraviolet laser ($\lambda_{\text{exc}} = 320 \text{ nm}$).

3.3 Summary

In this chapter, the composition, structure and optical properties of SRO and SI-SRO films fabricated by LPCVD have been studied by ellipsometry, FTIR, XPS, EFTEM, as well as PL.

Ellipsometry measurements and XPS studies on both SRO and SI-SRO films showed the presence of Si excess ($\text{Si} > 33.3\%$). In addition, the compositional analysis obtained from FTIR did not exhibit vibration bands related to impurities such as H or N neither before nor after thermal annealing. Although, XPS measurements showed the presence of N in these films, its profile was relatively low, about 0.8 at.%.

From FTIR spectra, it was deduced that a phase separation took place when the films were thermally annealed due to a displacement of the TO_3 band to higher frequencies ($\sim 1088 \text{ cm}^{-1}$ for SiO_2), and then corroborated by EFTEM images.

EFTEM analysis showed Si-nanoparticles in the samples with silicon excess higher than 5.1 at.%, which were thermally annealed at 1100° C . The average size of the Si-nps increased when both the silicon excess and the thermal annealing temperature were increased.

A strong PL was observed in films with 4 and 5.1 at.% of silicon excess. However, the photoluminescence was strongly reduced when the silicon excess was around 12.7 at.%, where the most of Si-nps have an average size of ~ 4.1 nm. A redshift only took place when the silicon excess was increased from 4 to 5.1 at.%, but no redshift was observed when the silicon excess was further increased to 12.7 at.%. Finally, it was found that SRO and SI-SRO films with Si-nps of different sizes emitted a PL peaked at the same energy.

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Chapter 4

Fabrication and characterization of MOS-like devices

Metal–oxide–semiconductor (MOS) structures were fabricated to study the electrical and electro–optical properties of SRO films. SRO films with $R_o = 30$ and 40 were deposited by LPCVD on p type silicon wafers ((100)-oriented, resistivity 0.1 – $1.4 \Omega\text{-cm}$) as discussed in chapter 3. The fabrication process developed to obtain the MOS structures and their electrical characterization are described below.

4.1. Fabrication process

Figure 4.1 shows the main fabrication steps for the MOS-like structures studied in this work.

- a) The process starts with the substrates. For this experiment P type Si-wafers ((100)-oriented) four inches in diameter and with resistivity of 0.1 – $1.4 \Omega\text{-cm}$ were used.
- b) Once the wafers were cleaned, 400 nm thick SiO_2 film was thermally grown on the Si substrate, which will work as a field oxide to isolate the devices.



Figure 4.1. Fabrication steps of MOS-like structures.

- c) The thermally grown SiO_2 film is etched to define the region of the active layer (SRO film) by means a photolithographic process followed by a wet etching process. At the same time, the back SiO_2 film was also eliminated.
- d) Then, a silicon rich oxide film (SiO_x , $x < 2$) was deposited by low pressure chemical vapor deposition as described in chapter 3. The parameters of the deposited SRO films are enlisted in table 4.1.

Wafer	Pressure of gases (Torr)		Time
	N_2O	SiH_4	(minutes)
3390-1	1.5	0.050	5.5
3390-2			11.0
3390-3	1.8	0.045	7.0
3390-4			14.0

Table 4.1. Parameters of the deposited SRO films, $T = 720^\circ \text{C}$.

Two different Si-excesses and thicknesses were deposited. In this step, ellipsometry measurements were performed on monitor samples in order to obtain the thickness and refractive index value, which are summarized in table 4.2. The number of monitor samples corresponds to the wafer's number. As observed, the refractive index values are very close to the samples analyzed in chapter 3 (see section 3.2.1, table 3.3). The silicon excess is also listed in the table 4.2.

Sample	Thickness (nm)	Refractive index	Si-excess (at.%)
1	24.1 ± 3.2	1.49 ± 0.060	4.0
2	53.4 ± 2.6	1.48 ± 0.001	
3	41.0 ± 5.9	1.47 ± 0.008	2.2
4	80.0 ± 2.1	1.47 ± 0.004	

Table 4.2. Thickness, refractive index and Si-excess of the annealed SRO films in MOS-like structures.

- e) After deposition, a thermal annealing at 1100° C in N₂ atmosphere was carried out for 180 minutes to induce the Si and SiO₂ phase separation and therefore the Si-nps formation.
- f) Boron ions were implanted at backside of the wafers with a dose of 5×10^{14} /cm² with an energy of 80 keV to ensure a good semiconductor/aluminium (ohmic) contact.
- g) Then, 140 nm thick SiO₂ film was deposited at the backside of the wafer by plasma enhance chemical vapor deposition to isolate it of the subsequent polysilicon layer deposition.
- h) After that, a 350 nm thick n+ polysilicon layer was deposited by LPCVD onto the SRO film to form the top contact of the devices. Polysilicon was highly doped with POCl₃.
- i) A photolithographic process was used to define and etch the polysilicon layer as the top contact. At the same time, the polysilicon which was deposited at the backside of the wafer was also etched. A thermal annealing at 800° C for 30 minutes was done to activate the impurities in the backside of the wafer.
- j) A 1.0 μm thick Al/Cu layer was deposited onto the wafer surface by sputtering.
- k) Then, this Al/Cu layer was etched using a photolithographic process to define the contact pads, which will be used for biasing the devices.
- l) Finally, the backside SiO₂ film was removed and a 1.0 μm thick Al/Cu layer was deposited by sputtering to act as a backside contact. The MOS-like structures were sintered in forming gas by a thermal annealing at 350° C.

Figure 4.2 exhibits an image of a dice in which different MOS-like structures are observed. The dimensions of the dice L₁ and L₂ are 1.95 mm and 2.79 mm, respectively. About ~1100 dices were fabricated on each wafer.

As it can see, each dice contains five MOS-like devices with different gate areas:

1. $9.604 \times 10^{-3} \text{ cm}^2$
2. $2.304 \times 10^{-3} \text{ cm}^2$
3. $3.24 \times 10^{-4} \text{ cm}^2$
4. $6.4 \times 10^{-5} \text{ cm}^2$
5. $2.6 \times 10^{-5} \text{ cm}^2$, for devices marked as 1–5, respectively.

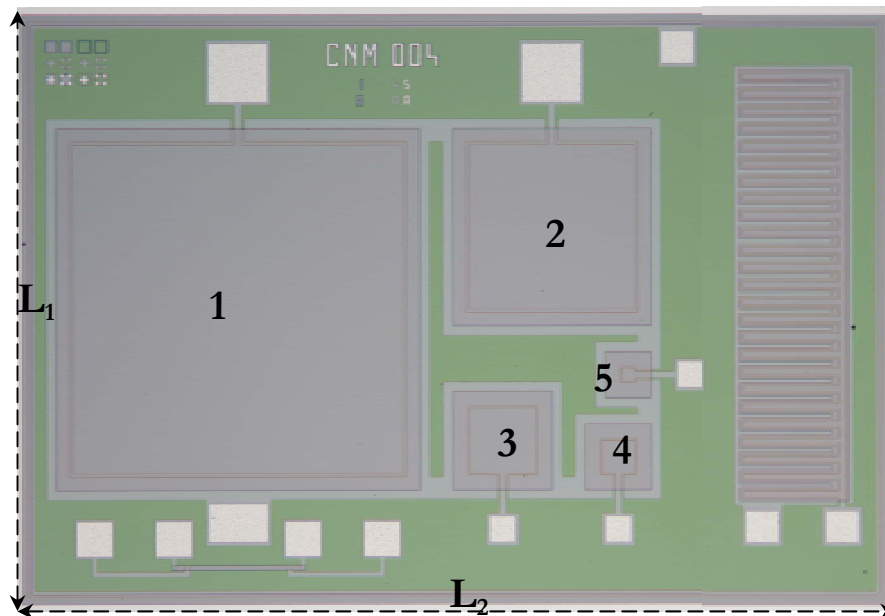


Figure 4.2. Image from devices fabricated with different area of gate electrode.

4.2. Electrical characterization set-up

Two different set-ups have been used to electrically characterize the fabricated MOS-like devices.

4.2.1. Electrical set up

Capacitance–frequency ($C-f$) curves were done using a computer-controlled HP4192A impedance analyzer biasing the devices in the accumulation region. $C-f$ curves demonstrate that the capacitance is more stable for a frequency of 100 kHz. Then, high frequency capacitance–voltage ($C-V$) measurements were performed at 100 kHz using a

computer-controlled HP4192A impedance analyzer and current–voltage (I – V) measurements were done with a semiconductor parameter analyzer HP4155B.

Electrical stress was applied between the gate electrode and the back contact in order to study the electrical properties of the SRO films. All the electric measurements were carried out at room temperature in the dark using a Karl Suss PA200 probe system, as shown in figure 4.3.



Figure 4.3. Electrical equipment used for the electrical characterization.

4.2.2. Electro-optical set up

Pulsed voltage set-up

EL studies were carried out by biasing the devices with voltage pulses using an Agilent 8114A pulse generator. Time-resolved electroluminescence was acquired with a photoncounting set-up composed by a Hamamatsu thermoelectric cooled H7422-50 photomultiplier and a Stanford Research SR430 multi-channel scaler. The EL spectra were measured by means of a Princeton Instruments LN (liquid nitrogen) cooled 100B CCD camera and an Oriel MS257™ 1/4 m monochromator.

The set-up used for the pulsed electroluminescence studies is shown in figure 4.4. This set-up is located at the Electronics department of the University of Barcelona (Group of Prof. Blas Garrido).



Figure 4.4. Schematic of the set-up used for pulsed EL measurements.

Continuous voltage set-up

The continuous EL measurements were carried out by biasing the devices with a constant gate voltage using a standard voltage source. Light emission was collected with an optical fiber with a core of 50 μm , which was located just onto the shining spots and connected to a high resolution spectrometer model HR4000 and analyzed with a computer, as schematized in figure 4.5. The electrical measurements were carried out at room temperature using a Karl Suss PA200 probe system.

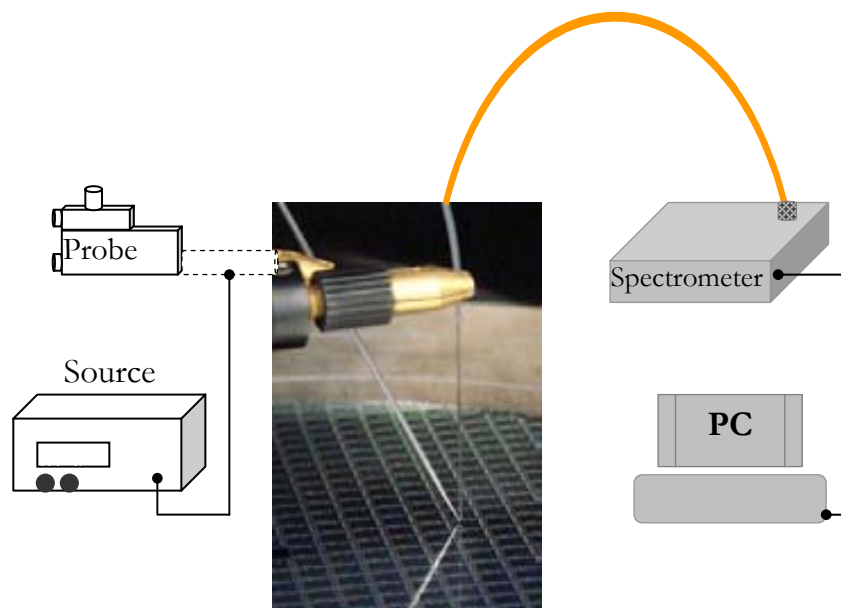


Figure 4.5. Schematic of the set-up used for continuous EL measurements.

4.3. Electrical characterization results

4.3.1. C-w and C-V characteristics

Figure 4.6 reports the normalized capacitance as a function of the frequency for different MOS-like structures with gate area of $9.604 \times 10^{-3} \text{ cm}^2$. C-w curves were measured biasing the devices with a gate voltage of $V_G = -5 \text{ V}$ and an oscillation of 30 mV, that is, remaining the devices in the accumulation region. The capacitance oscillates at low operation frequencies and it decreases when the frequency is higher than 100 kHz. These effects are more evident for MOS-like structures with higher Si-excess, see figure 4.6(a). MOS-like structures with lower Si-excess (2.2 at.%) exhibit a more stable behaviour in the C-w, as observed in figure 4.6(b). Nevertheless, all C-V measurements reported in this work were done at a frequency of 100 kHz in order to obtain repetitive data.

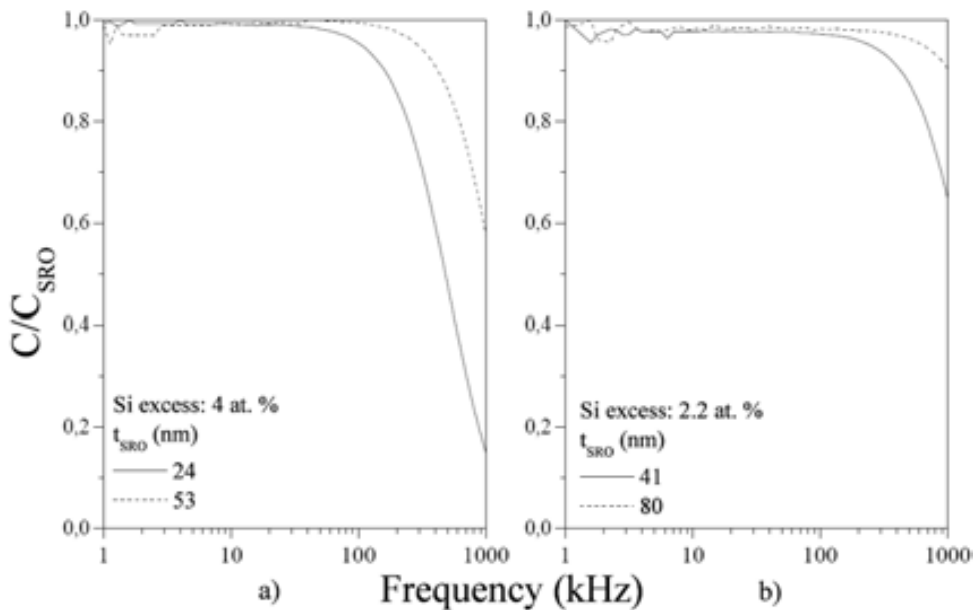


Figure 4.6. Normalized C-w curves of MOS-like structures with a) 24 nm and 53 nm and b) 41 nm and 80 nm thick SRO films with 4 and 2.2 at.% of Si-excess, respectively. All measurements were done with a gate voltage of $V_G = -5V$ and an oscillation of 30 mV.

Figure 4.7 shows the C-V curves measured from different MOS-like devices with gate area of $9.604 \times 10^{-3} \text{ cm}^2$. Variations on the maximum capacitance are observed for different thickness and composition of the SRO films.

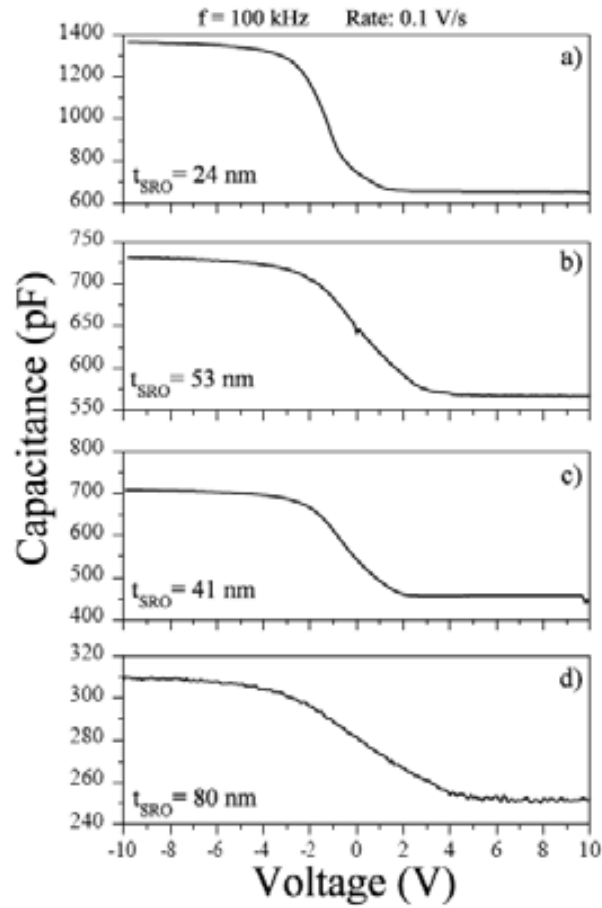


Figure 4.7. C - V curves of MOS structures with a) 24 nm and b) 53 nm thick SRO_4 and c) 41 nm and d) 80 nm thick $\text{SRO}_{2.2}$ films as the active layer at 100 kHz. All measurements were done from inversion to accumulation and a sweep rate of 0.1 V/s.

Table 4.3 lists the statistical data of the maximum capacitance (C_{SRO}), SRO thickness (t_{SRO}), substrate doping (N_a), the flat band voltage (V_{FB}), and the interface trap density (N_{it}) obtained from measurements done on 10 different devices for each SRO film.

	3390-1	3390-2	3390-3	3390-4
C_{SRO} (pF)	1297.0 ± 55.3	755.7 ± 14.9	708.4 ± 32.1	305.9 ± 12.4
t_{SRO} (nm)	25.6 ± 1.1	43.9 ± 0.87	50.2 ± 2.3	108.5 ± 4.28
N_a (cm^{-3})	$1.4 \times 10^{17} \pm 9.1 \times 10^{16}$	$7.1 \times 10^{17} \pm 2.7 \times 10^{17}$	$2.1 \times 10^{17} \pm 6.5 \times 10^{15}$	$3.09 \times 10^{17} \pm 2.35 \times 10^{16}$
V_{FB} (V)	-1.1 ± 0.16	-2.2 ± 0.16	-2.05 ± 0.1	-4.02 ± 0.28
N_{it} (cm^{-2})	$1.2 \times 10^{11} \pm 1.2 \times 10^{10}$	$6.2 \times 10^{11} \pm 6.9 \times 10^{10}$	$4.4 \times 10^{11} \pm 3.6 \times 10^{10}$	$6 \times 10^{11} \pm 4.28 \times 10^{10}$

Table 4.3. Data obtained from electrical characterization for different MOS structures.

The thickness of the SRO films as estimated from electrical measurements is 25.6, 43.9, 50.2, and 108.5 nm for wafers 1-4, respectively. These values are close to the obtained by ellipsometry (except wafer 4, where an 80 nm thick SRO film was measured), as measured on monitor samples and reported in table 4.2.

As the resistivity of the wafers is about 0.1 to 1.4 Ω -cm, the doping density (N_a) is expected to be in the range 1.01×10^{16} - 2.77×10^{17} cm^{-3} . From table 4.3, it can be seen that this value is within this doping range. The flat-band voltage (V_{FB}) varies depending on the Si-excess and on the SRO thickness. The interface trap density (N_{it}) is about 10^{11} cm^{-2} for all wafers.

Figure 4.8 shows the hysteresis C-V curve performed with the sweep voltage at both directions, that is, from inversion to accumulation and back to inversion. As it can be seen, no flat-band voltage shifting is observed. This effect could be due to charges flow through the SRO films without being trapped. Moreover, no V_{FB} shifting was observed for all MOS-like structures with different Si-excess under this condition.

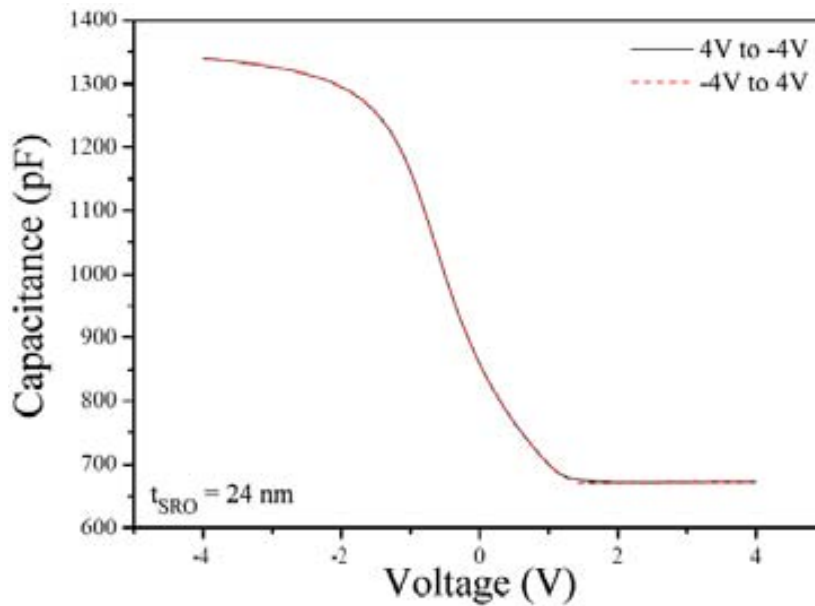


Figure 4.8. Hysteresis C-V curve at 100 kHz measured from the MOS-like structure with 24 nm thick SRO film and 4 at.% of Si-excess.

Even though no hysteresis is found on these devices, one of the remarkable electrical characteristics of SRO films containing Si-nps is the charge trapping capability under a

constant electrical stress. Then, C-V measurements were done before and after applying different gate voltages on as-fabricated devices for each capacitive structure.

Figure 4.9 shows the C-V curves before and after a constant electrical stress is applied on the MOS like structures with 4 at.% of Si-excess. Instead of a V_{FB} shifting, the capacitance reduces when the devices with 24 and 53 nm thick SRO films are electrically stressed. As shown in figure 4.9(a), the accumulation capacitance for the thinness SRO film (24 nm) decreases from 1200 pF to 180, 160 and 40 pF when the device is biased with -4, -8 and -17 V, respectively. However, no capacitance drop was observed in the inversion region. On the other hand, from figure 4.9(b) can be seen that both the accumulation and inversion capacitance of the thicker SRO film reduces from 679 and 534 to 502 and 362 pF, respectively, after biased with $V_G = -20$ V. As mentioned before, in spite of the electrical stress, no flat band voltage difference was measured. These effects were not observed for MOS like structures with the lowest Si-excess (2.2 at.%, wafers 3 and 4).

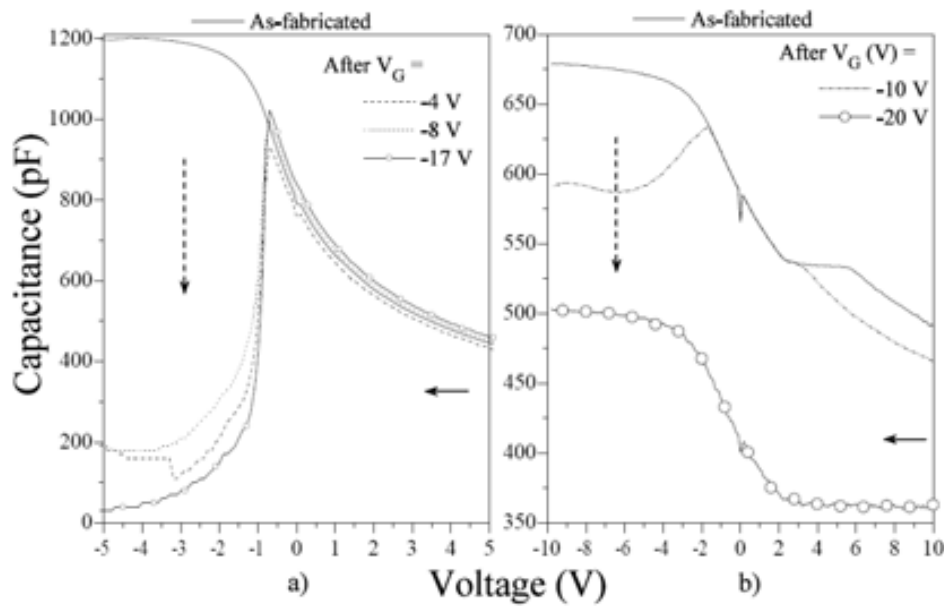


Figure 4.9. C-V characteristic before and after applying constant electrical stress V_G for 60 seconds on the MOS-like structures with a) 24 nm and b) 53 nm thick SRO and gate area of $9.604 \times 10^3 \text{ cm}^2$.

C-V measurements were done on MOS-like structures with 24 nm thick SRO but smaller gate area ($3.24 \times 10^4 \text{ cm}^2$), as shown in figure 4.10. The accumulation capacitance reduces when the device is electrically stressed with -3 V. After the device is biased with

$V_G = -6$ V, both the accumulation and inversion capacitance decreases from 100 pF and 88.4 to 47.6 and 23.8 pF, respectively, such as the thicker SRO film (53 nm).

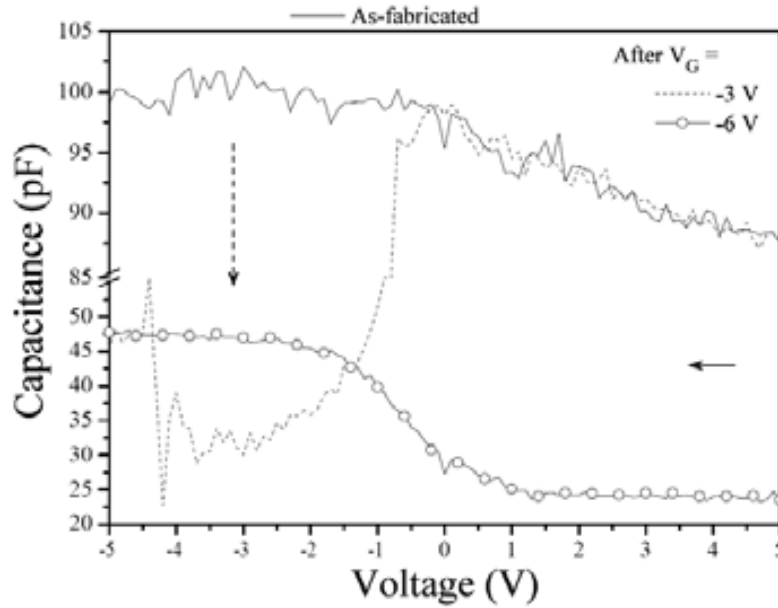


Figure 4.10. C - V characteristic before and after applying constant electrical stress V_G for 60 seconds on the MOS-like structures with a) 24 nm and gate area of $3.24 \times 10^4 \text{ cm}^2$.

Since the capacitance dropping depends on the gate area and probably of the thickness, a more detailed study about this behaviour is done on the devices with Si excess of 4 at.% and 53 nm thick SRO film (wafer 2) and with different gate area, as shown in figure 4.11. These measurements were done before and after applying a constant gate voltage on as-fabricated devices for each capacitive structure.

Measurements on devices without any electrical stress (as-fabricated devices) showed a maximum capacitance of 732.3, 275.6, and 208.5 pF for each gate area of $9.604 \times 10^{-3} \text{ cm}^2$, $2.304 \times 10^{-3} \text{ cm}^2$, and $3.24 \times 10^{-4} \text{ cm}^2$, respectively. However, the capacitance value is reduced after stressing the devices with a gate voltage $V_G = -22$, -18 , and -13 V for each gate area of $9.604 \times 10^{-3} \text{ cm}^2$, $2.304 \times 10^{-3} \text{ cm}^2$, and $3.24 \times 10^{-4} \text{ cm}^2$, respectively. As it can be seen, the gate voltage needed to obtain the capacitance dropping varies depending on the gate area.

Although such capacitance dropping might be related to a charge trapping phenomenon, no changes have been measured on the flat-band voltage (V_{FB}).

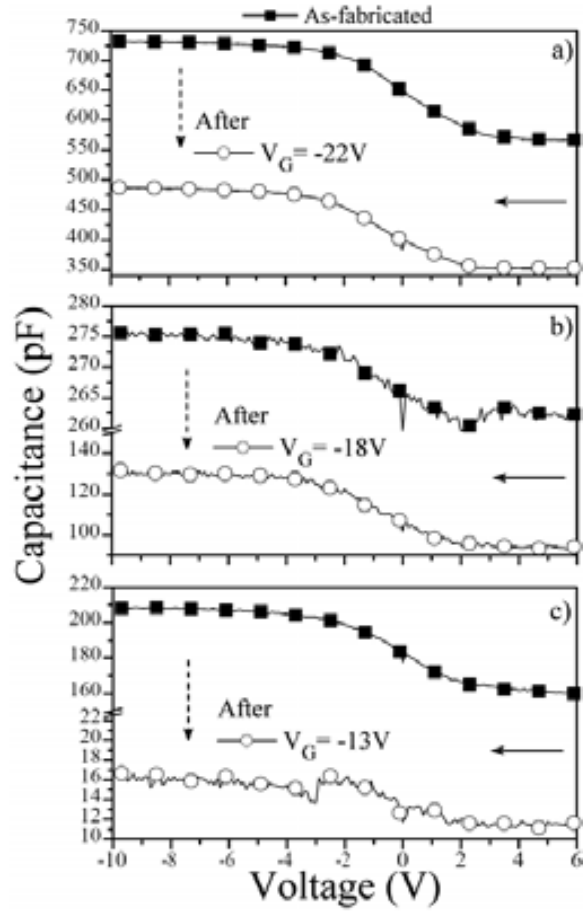


Figure 4.11. C - V characteristic before and after applying a constant electrical stress V_G for 60 seconds on the MOS-like structures with gate area of (a) $9.604 \times 10^{-3} \text{ cm}^2$, (b) $2.304 \times 10^{-3} \text{ cm}^2$, and (c) $3.24 \times 10^{-4} \text{ cm}^2$ and 53 nm thick SRO film (4 at.% of Si-excess). All measures were done from inversion to accumulation with a sweep rate of 0.1 V/s.

Similar effects to the capacitance dropping have been observed by other authors [1] ascribing them mainly to the charge trapping in Si-ncs. However, if charge gets trapped in a SiO_2 matrix with Si-nps embedded it should produce a V_{FB} shift in the C - V curves [2, 3]. In this experiment, a V_{FB} shifting is only obtained after the capacitance has dropped at a lower value and applying gate voltages higher than that where the capacitance dropping is obtained, that is $|V_G| \geq 20, 18, \text{ and } 13 \text{ V}$ for the MOS-like structures with gate area of $9.604 \times 10^{-3} \text{ cm}^2$, $2.304 \times 10^{-3} \text{ cm}^2$, and $3.24 \times 10^{-4} \text{ cm}^2$, respectively.

Figure 4.12 displays C - V curves from as-fabricated devices with 53 nm thick SRO film and Si excess of 4 at.% (wafer 2) and gate area of $9.604 \times 10^{-3} \text{ cm}^2$ before and after

electrical stress. As in figure 4.11, the capacitance drops after the device is electrically stressed with $V_G = -25$ V. After that, the device was biased with several voltages and two behaviours can be clearly observed: first, the $C-V$ curve exhibits a positive shift for gate voltages of $V_G = 20$ to 30 V, indicating electrons trapping. Second, the $C-V$ curve shifts toward negative voltages for higher electrical stresses, e.g. gate voltages of $V_G = +48$ and -48 V, indicating holes trapping.

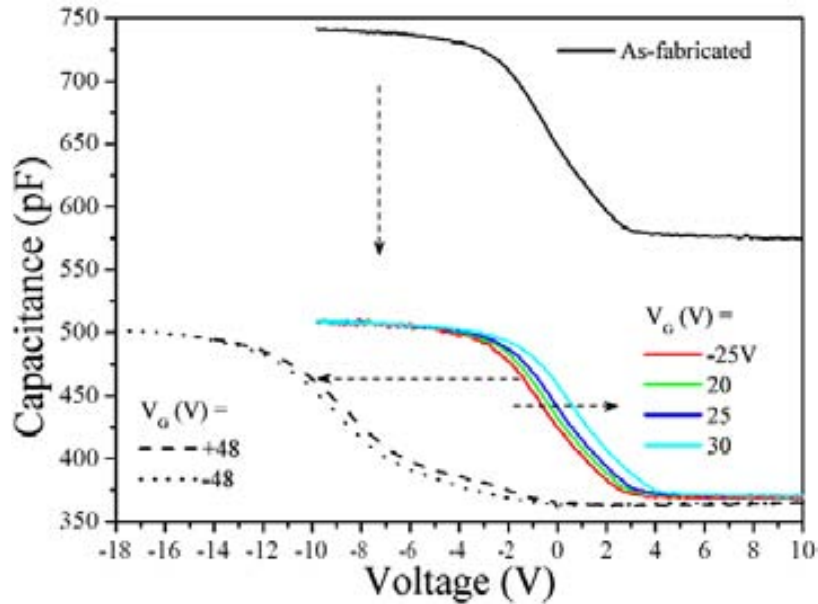


Figure 4.12. $C-V$ curves before and after applying a constant electrical stress for 60 seconds on the MOS-like structures with 53 nm thick SRO film (4 at.% of Si-excess) and gate area of $9.604 \times 10^{-3} \text{ cm}^2$. All measures were done from inversion to accumulation with a sweep rate of 0.1 V/s.

This capacitance dropping is not only observed at negative voltages, but also at positive voltages. Figure 4.13 exhibits the typical $C-V$ curve measured from as-fabricated devices with the largest gate area before and after positive stress. It can be seen that the accumulation capacitance decreases after the MOS-like structure is biased with a gate voltage of $V_G = +15$ and 25 V. For a gate voltage $V_G = +30$ V, the accumulation and inversion capacitances drop at a lower value, which is close to the obtained with negative voltage.

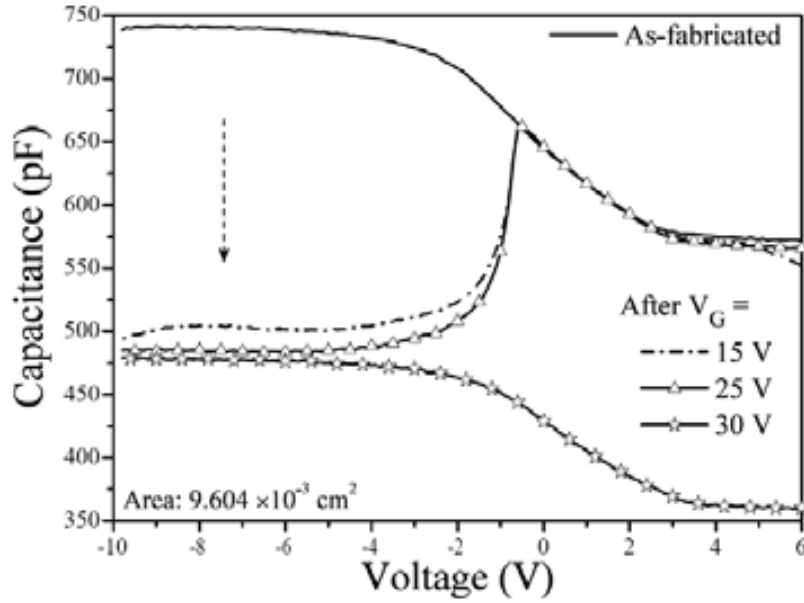


Figure 4.13. C - V curves before and after applying positive electrical stresses for 60 seconds on the MOS-like structures with 53 nm thick SRO film (4 at.% of Si-excess) and gate area of $9.604 \times 10^{-3} \text{ cm}^2$. All measures were done from inversion to accumulation with a sweep rate of 0.1 V/s .

4.3.2. I-V characteristics

The current density versus electric field (J-E) curves measured from devices with a gate area of $9.604 \times 10^{-3} \text{ cm}^2$ is reported in figure 4.14. High current densities were measured in devices with higher silicon excess (4 at.%, wafers 1 and 2) at low electric fields, as shown in figure 4.14(a). Meanwhile the current density is at a lower level for devices with silicon excess of about 2.2 at.% and for both thicknesses (wafers 3 and 4), as depicted in figure 4.14(b). High currents in these structures are only observed when the electric field is high enough ($> 6 \text{ MV/cm}$) to see the F-N conduction such as in a SiO_2 film. Therefore, the decreasing of the electric field needed for high conduction can be associated with the silicon excess within the SRO films.

In figure 4.14(a), a current drop is observed in devices with 53 nm thick SRO film and Si-excess of 4 at.% (wafer 2) at both biases (forward and reverse bias). Moreover, the electric field (gate voltage) where the current dropping is observed (at both positive and negative V_G) correlates with that where the capacitance dropping was observed. Therefore, there is a clear relation between the capacitance and current dropping.

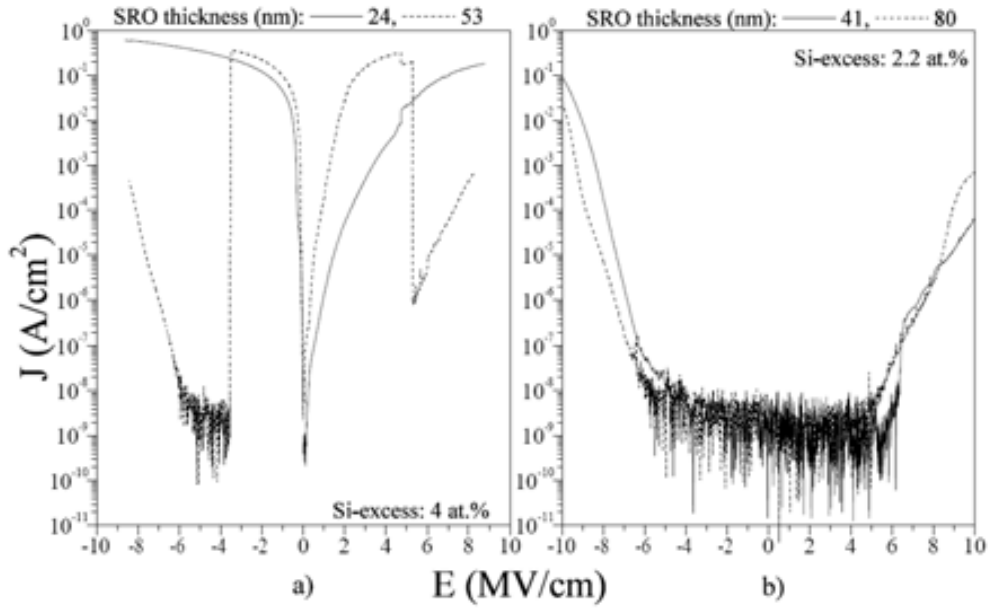


Figure 4.14. I - V curves of MOS structures with a) 24 nm and 53 nm and b) 41 nm and 80 nm thick SRO films with 4 and 2.2 at.% of Si-excess, respectively. All measurements were done with a sweep rate of 0.1 V/s.

Since the SRO films used in devices from wafer 1 and 2 have the same silicon excess, similar behaviours are expected. However, no current drop is observed for the thinner SRO film (24 nm). This could be related to both, the SRO thickness and the gate area. In fact, it was observed that the gate voltage where the capacitance dropping occurs increases as the gate area is larger. Because of this, I - V curves are measured on the MOS-like devices with a smaller gate area.

Figure 4.15 exhibits the I - V curves from devices with 4 at.% of Si-excess and 24 nm thick SRO film (wafer 1) with gate area of $3.24 \times 10^{-4} \text{ cm}^2$. For as-fabricated devices, a current drop is observed at $\sim -6.8 \text{ V}$ and then it oscillates around 10^{-11} A . This current drop (I_{drop}) is also related with the capacitance dropping reported before (see figure 4.10). Moreover, the current dropping is also observed at positive voltages ($V_G = 16.7 \text{ V}$). At high voltages, the current enters in a high field conduction regime such as the behaviour of devices with thicker SRO film (see figure 4.14(a)). Once the current dropping is obtained, a new I - V measurement (figure 4.15, curve 2) shows that it remains at a low level current (10^{-10} A) for low gate voltages, until a high field conduction regime is obtained.

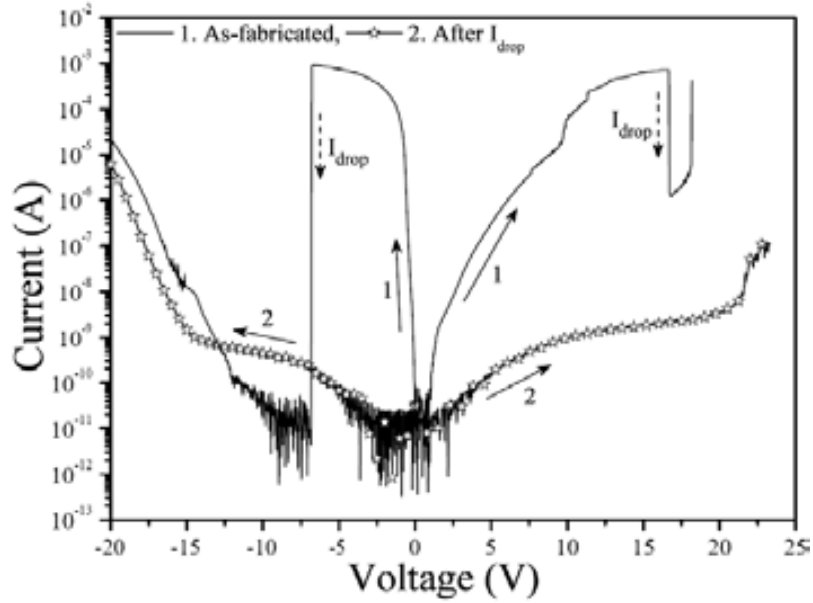


Figure 4.15. I - V characteristic in as-fabricated devices (1) and after I_{drop} (2) on the MOS-like structures with 24 nm thick SRO and gate area of $3.24 \times 10^4 \text{ cm}^2$. All measurements were done with a sweep rate of 0.1 V/s.

A more detailed study about this behaviour is newly done on the MOS-like devices with 53 nm thick SRO film, Si-excess of 4 at.% (wafer 2) and with different gate area, as observed in figure 4.16.

Figure 4.16(a) shows the typical I - V characteristics measured in devices with three different gate areas in accumulation regime (forward bias). According to V_G , four different regions can be identified in A , B , C , and D corresponding to [0 to \sim -21 V], [-21 to \sim -32 V], [-32 to \sim -44 V] and [-44 to \sim -50 V], respectively. The width of “ A ” zone reduces (less negative V_{drop}) as the gate area of MOS-like device becomes smaller. B zone is defined as the region where the current remains at \sim pA after dropping from 10^{-3} and until entering in a high field conduction regime (C and D zones). Figure 4.16(b) depicts the occurrence of each zone as a function of the gate area. The current dropping, which splits A and B zones, is observed at a more negative gate voltage as the gate area becomes larger; meanwhile C and D zones does not seem to depend on the gate area. Moreover, the gate voltages where the current drops are close to the gate voltage in which the capacitance dropping was obtained. Figure 4.16(c) exhibits the current through the SRO films as a function of time for the MOS-like structures with different gate area and at gate voltage $V_G = V_{\text{drop}}$. A high current (10^{-3} A) is observed for

a period of time until it drops at a low level at 10.3, 25.8 and 40.7s for each gate area of $9.604 \times 10^{-3} \text{ cm}^2$, $2.304 \times 10^{-3} \text{ cm}^2$, and $3.24 \times 10^{-4} \text{ cm}^2$, respectively. Then, the current dropping can be obtained either during the voltage sweep or by applying a gate voltage $V_G = V_{\text{drop}}$.

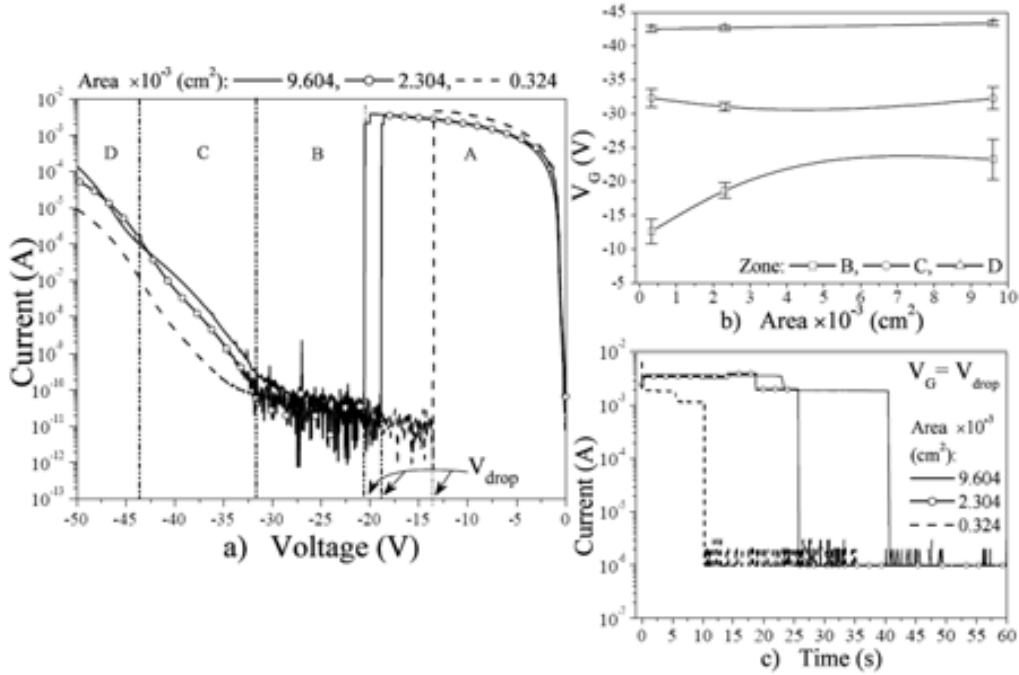


Figure 4.16. a) I - V curves done with a sweep rate of 0.1 V/s , b) Occurrence of the different zones as a function of gate area (lines are plotted as an eye-guide), and c) I - t curves at a gate voltage $V_G = V_{\text{drop}}$ of MOS-like structures with different gate area and Si-excess of 4 at. %.

The switching behaviour between 10^{-3} to 10^{-12} A current has been observed before by other authors and it is known as negative differential resistance (NDR) [4]. In this experiment, a very high peak to valley current ratio is observed. Theoretical studies on the transport properties through a clusters' array have shown similar results [5]. A "Coulomb Blockade Gap" (CBG) was observed, similar to the B zone from figure 4.16(a). Its origin was attributed to the formation of a trapped-electron configuration or the stationary charge configuration (SCC) where charge trapped on the Si-nps blocks the electrical conduction.

C and D zones are obtained when the electric field inside the oxide is strong enough ($> 6 \text{ MV/cm}$) to have a strong band bending, so electrons tunnel through a triangular barrier from the polysilicon gate towards the silicon substrate. On the other hand, in the

A zone (low electric fields) the current exhibits a strong dependence on the gate voltage. In this region, tunnelling mechanisms such as Fowler–Nordheim (F-N) [2, 6] or Poole–Frenkel (P-F) [6, 7] should be excluded because of the SRO thickness. Other conduction mechanism should be responsible for that current observed; the trap-assisted tunnelling (TAT) [8] being the most probable. As these SRO films are composed by very small Si-nps due to the low silicon excess [9], these characteristics may be strictly related to the SRO films properties.

Figure 4.17 reports the I–V curves measured from devices with 53 nm thick SRO film (4 at.% of Si-excess) and different gate area, before and after applying a similar electrical stress to C–V measurements, where the capacitance reduction was observed (see figure 4.11).

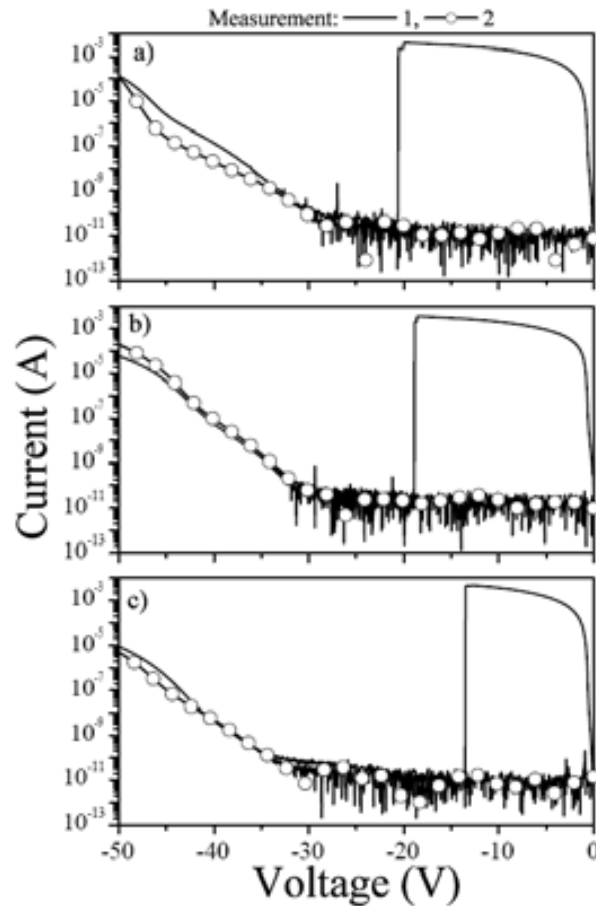


Figure 4.17. I–V characteristic before (1) and after applying a constant electrical stress $V_G = V_{drop}$ (2) for 60 seconds on the MOS-like structures (53 nm thick SRO film with 4 at.% of Si-excess) with gate area of (a) $9.604 \times 10^{-3} \text{ cm}^2$, (b) $2.304 \times 10^{-3} \text{ cm}^2$, and (c) $3.24 \times 10^{-4} \text{ cm}^2$. All measures were done with a sweep rate of 0.1 V/s.

In as-fabricated devices, the current exhibits the same behaviour than reported in figure 4.16(a). However, after the $V_G = V_{\text{drop}}$ stress was applied, a very low level current of about 10^{-12} A was measured in the A and B zones. Then, this effect could be explained by the annihilation of conduction paths in the SRO film, which connect the silicon substrate with the polysilicon gate. As the gate voltage becomes more negative, C and D regions are observed.

As mentioned before, the current drop is not only obtained at negative voltages, but also at positive voltages. Figure 4.18(a) exhibits the typical I-V curve measured from as-fabricated devices with 53 nm thick SRO film (4 at.% of Si-excess) and for three different gate areas in inversion regime (reverse bias, RB). The gate voltage (V_{drop}) where the current dropping occurs is also observed to depend on the gate area, such as in forward bias measurements. Once the current drops, C and D regions are observed, such as in forward bias.

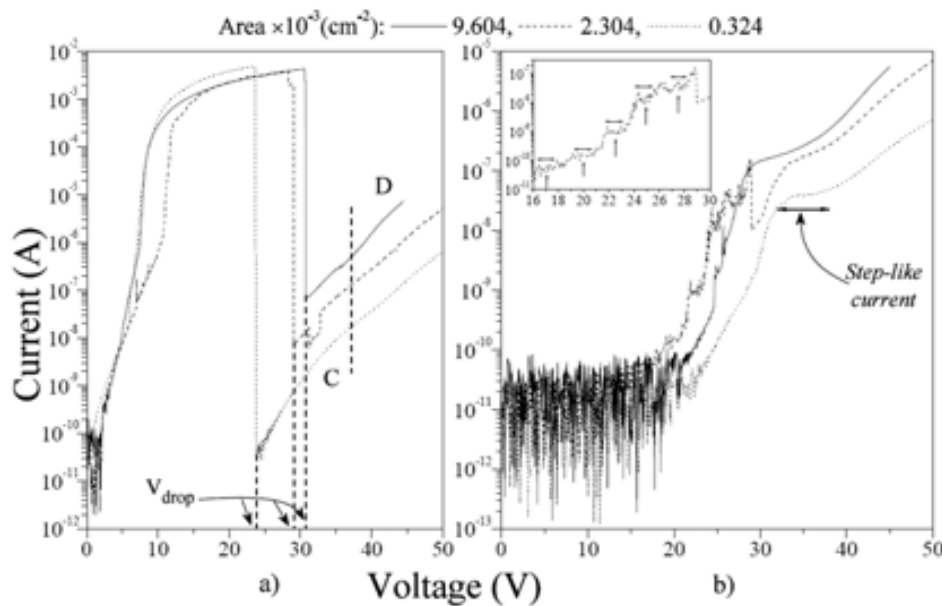


Figure 4.18. I-V characteristic under inversion a) before and b) after applying a constant electrical stress $V_G = V_{\text{drop}}$ for 60 seconds on the MOS-like devices with 53 nm thick SRO film (4 at.% of Si-excess) and different gate area. Inset of figure (b) shows the staircase-like current measured for the MOS-like structure with gate area of $2.304 \times 10^{-3} \text{ cm}^2$.

Figure 4.18(b) shows the I-V curves from MOS-like devices with different gate area after applying a constant electrical stress $V_G = V_{\text{drop}}$ for 60 seconds. This current behaviour was obtained by making the sweep in positive voltages (RB) after the current

has dropped. At low voltages (< 20 V), the current oscillates at a low level ($< 10^{-10}$ A) for all gate areas. For gate voltages $V_G \geq 20$ V, the current increases until a step-like behaviour is observed at about 29 V for devices with the largest gate area ($9.604 \times 10^{-3} \text{ cm}^2$) and ~ 32 V for the two smaller ones. This step-like current is almost constant (as marked by the arrow in figure) until the current enters to the high field conduction regime. Such step-like current behaviour has been reported [7, 10] and ascribed to charge trapping in a Si-ncs layer through tunnelling and a consequent Coulomb blockade effect on the charges trying to tunnel behind. In fact, the I - V measured from the device with gate area of $2.304 \times 10^{-3} \text{ cm}^2$ exhibits a staircase-like behaviour between 16 and 28 V, as shown in the inset of figure 4.18(b). This quantum phenomenon is related to Coulomb blockade (CB) effects and they are the result of single electron trapping in the silicon nanoparticles embedded in the SRO films [11]. Moreover, the voltage range for this staircase current correlates with that voltage range where the electrons' trapping is obtained (see figure 4.12). Therefore, that behaviour is correlated with electrons trapped in Si-nps.

4.4. Electro-optical characterization results

Electroluminescence has been observed in the fabricated devices with 53 nm thick SRO film and Si-excess of 4 at.% under pulsed (positive to negative) and continuous voltage stimulation.

4.4.1. Pulsed electroluminescence

Measurements were done on MOS-like devices from all wafers, however pulsed EL was only observed for devices with 53 nm thick SRO film, Si-excess of 4 at.%, and for all gate areas.

Figure 4.19 shows the time resolved EL for a driving voltage of 20 V. As it can be seen, a stretched exponential EL behaviour is observed after alternating the voltage bias from negative (positive) to positive (negative). However, a low intensity EL was observed when the bias was changed from positive to negative voltage contrasted to the contrary switching.

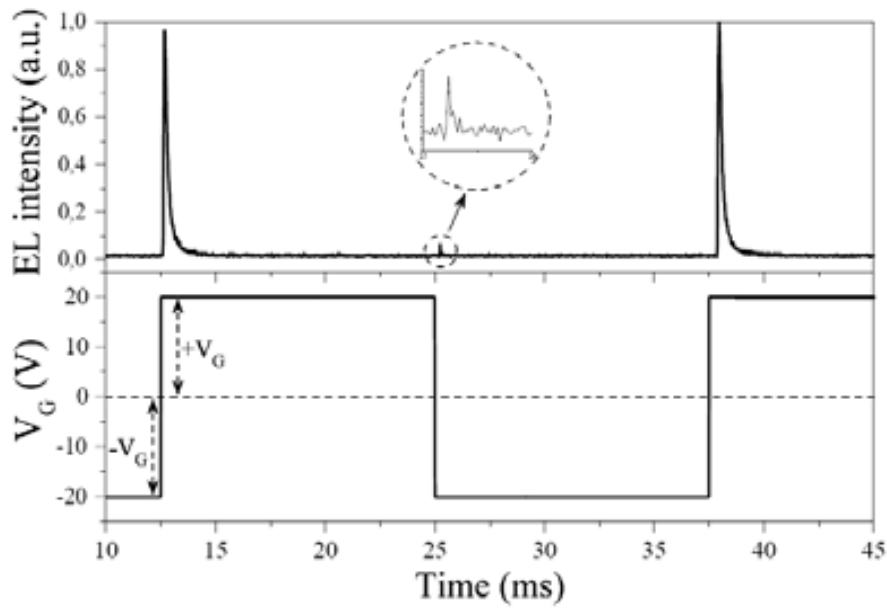


Figure 4.19. Time resolved EL of 53 nm thick SRO film in MOS-like devices biased with a pulsed voltage of $V_G = \pm 20$ V.

The dependence of the EL intensity on the driving voltage with a pulse width of 50 ms was also studied, as showed in figure 4.20(a).

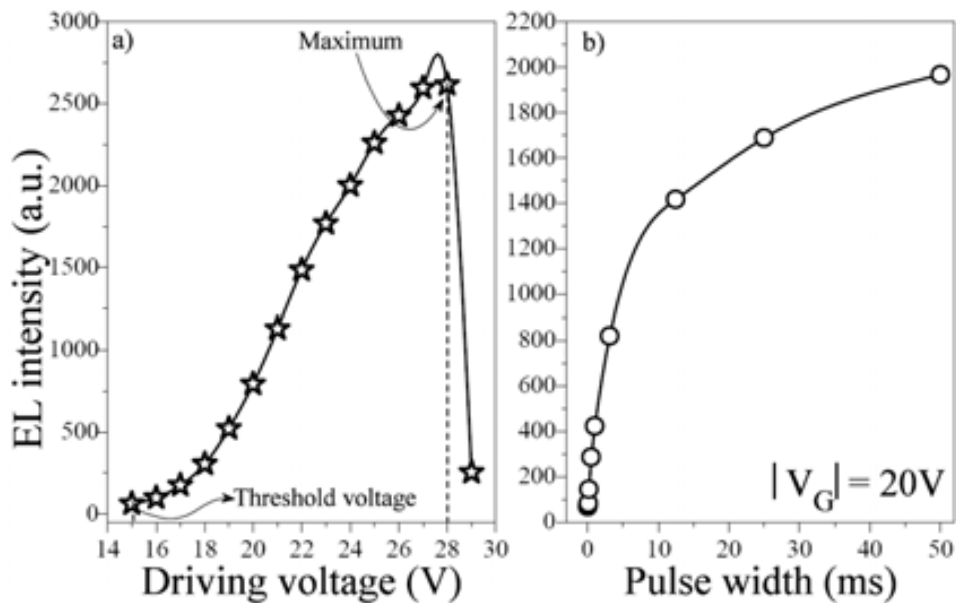


Figure 4.20. EL intensity as a function of the a) driving gate voltage (pulse width of 50 ms) and b) pulse width for a driving gate voltage of ± 20 V.

The EL emission is observed after a threshold voltage of 15 V and it increases as the voltage of the pulse excitation is higher. However, the maximum EL intensity is

observed with 28 V and then quenches with 29 V. The EL intensity was also found to depend on the pulse width, for a driving gate voltage of 20 V, as shown in figure 4.20(b). As it can be observed, the EL is more intense as the pulse width is increased. As the frequency increases, the number of e-h pairs formed in the switching of negative to positive (positive to negative) voltage decreases due to there is not time enough to inject charges into the SRO film.

Figure 4.21 shows the EL spectra measured on these devices at different driving gate voltages. A broad spectrum is observed with several maximum peaks. Gaussian fits were done and four different EL peaks at 503, 567, 653, and 784 were obtained for all driving voltages, as observed in figure 4.22(a).

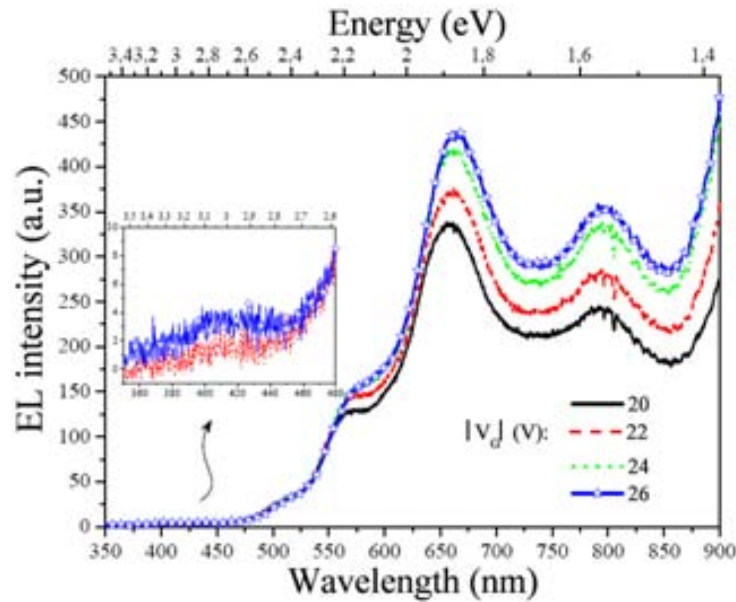


Figure 4.21. EL spectra measured from MOS-like devices with 53 nm thick SRO film at different gate voltages. Inset exhibits an EL peaked at 422 nm for a gate voltage of 22 and 26 V.

On the one hand EL peaks slightly shift towards longer wavelengths as the voltages increases. In addition to these EL peaks, a tail from a luminescent peak at longer wavelengths is also observed (~ 900 nm), which can be related to the emission of silicon substrate. On the other hand, an emission peak at 420 nm is also observed for driving voltages higher than 22 V, as shown in the inset of figure 4.21.

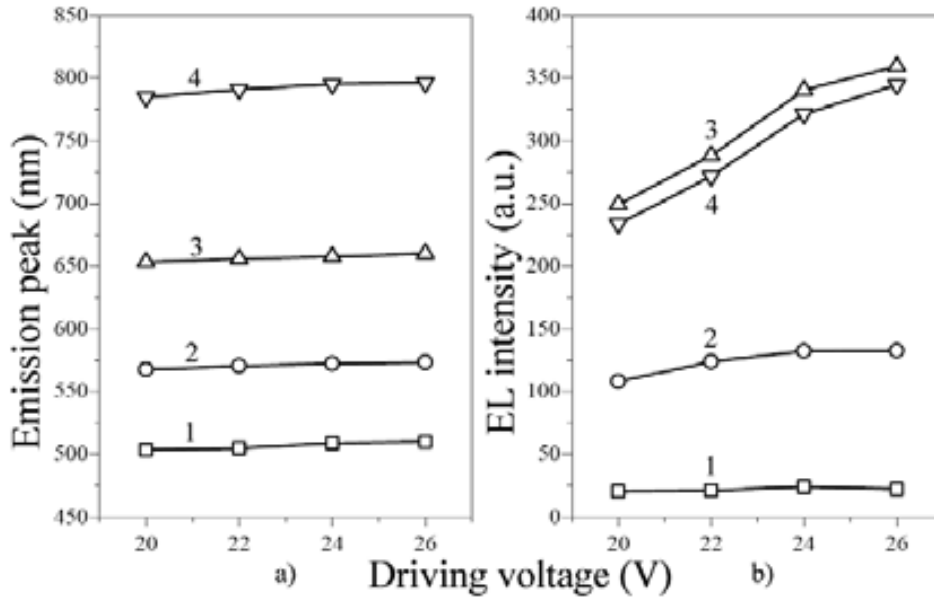


Figure 4.22. a) Wavelength and b) intensity of the EL emission peaks as a function of the driving gate voltage. Numbers indicate the emission peak at both position and intensity.

Figure 4.22(b) depicts that the intensity of these peaks becomes stronger by increasing the driving voltage, being more evident for the EL peaks at longer wavelengths (peaks 3 and 4). This emission is different from that observed in PL measurements for these kind of SRO films because only one peak was observed at about 733 nm (1.69 eV), as reported in chapter 3.

4.4.2. Continuous electroluminescence

EL at continuous voltage was also studied and shining spots were clearly observed at naked eye when devices were reversely biased (RB, positive voltage applied to the gate respect to the Si-substrate). Measurements were done on several MOS-like devices with 24 and 53 nm thick SRO film, which contain a Si-excess of 4 at.% (wafer 1 and 2, respectively).

Figure 4.23 shows an image from the light emission in a MOS-like device with 24 nm thick SRO film when reversely biased with 5 V (RB). As it can be seen, the light emitted is clearly observed at naked eye. The emission is observed as a line of shining spots at the middle of the gate area, as shown in the inset of figure 4.23.

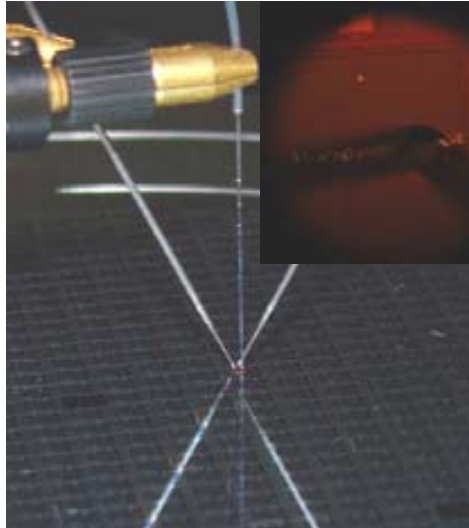


Figure 4.23. MOS-like device with a 24 nm thick SRO film emitting when biased with 5V. Inset shows the same device but taken from one lens of the microscope. Images were taken using a typical digital camera.

Figure 4.24 exhibits the EL spectra from the MOS-like structure with 24 nm thick SRO film at different gate voltages when the device is reversely and forwardly biased. The optical fiber was put on a part of the line of shining spots, as shown in the inset of figure 4.23. A broad spectrum with maximum peaks is observed for all gate voltages when the device is at RB, as shown in figure 4.24(a). Moreover, the emission is observed at very low voltages as 1 V.

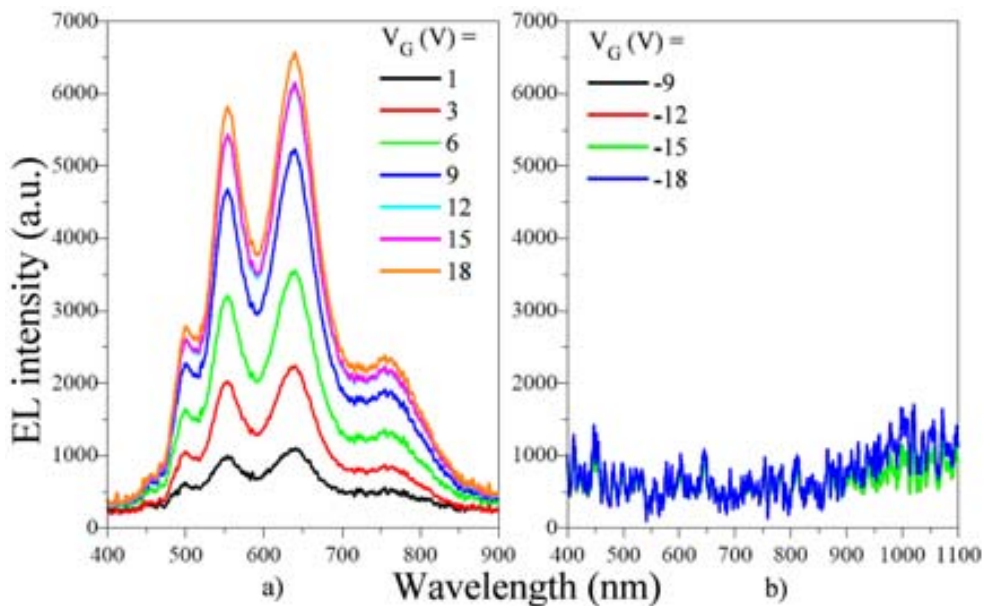


Figure 4.24. EL spectra measured from the line of shining spots from figure 4.27 at different gate voltages when device is a) reversely and b) forwardly biased.

Light emission was not observed between 400–900 nm when the device is FB, as shown in figure 4.24(b). Nevertheless, an EL peak at about ~ 1000 nm with low intensity is observed. This emission could be produced by the recombination of electrons flowing from the polysilicon gate with holes from the accumulated layer at the Si-substrate surface.

All spectrums from figure 4.24(a) were fitted to Gaussians curves and five different EL peaks were obtained at about 450, 500, 550, 640, and 750 nm, as observed in figure 4.25(a). These EL peaks do not seem to depend on the gate voltage because they appear at the same wavelength. The intensity of the EL peaks as a function of the gate voltage is shown in figure 4.25(b). The emission at 450 nm (peak 1) remains almost constant for all gate voltages, contrary to others EL peaks, which are more intense as the gate voltage is raised. A maximum EL intensity is observed with 12 V and then remains almost constant. It can be seen that the most intense EL peaks are those placed at 550 and 640 nm (peaks 3 and 4).

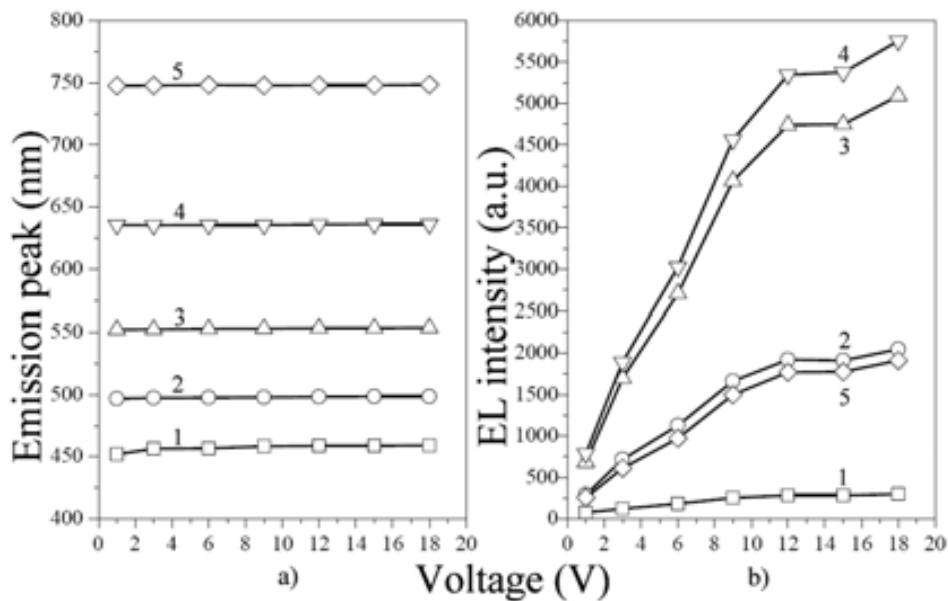


Figure 4.25. a) Wavelength and b) intensity of the EL emission peaks as a function of the gate voltage at RB. Numbers indicate the emission peak at both position and intensity.

Light emission from a MOS-like device with the thicker SRO film (53 nm) when biased with 25 V (RB) is shown in figure 4.26. The emitted light is clearly observed at naked eye, as well. The emission is observed as three shining spots separated on the gate area,

as observed in the inset of figure 4.26. The optical fiber is also observed onto the shining spot marked as 3 to collect its spectra.

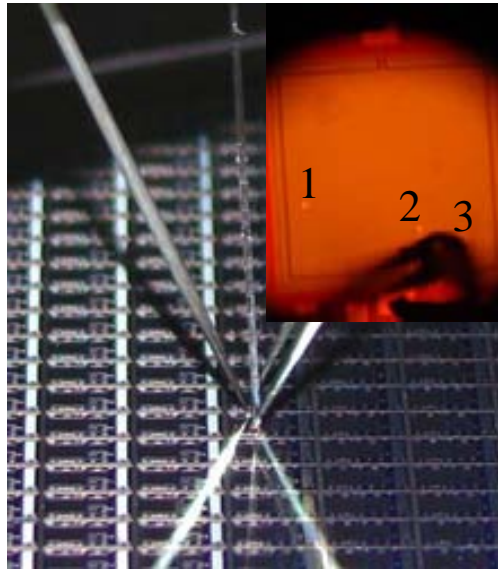


Figure 4.26. MOS-like device with a 53 nm thick SRO film emitting when biased with 25 V (RB). Inset shows the same device but taken from one of the lens of microscope. Images were taken using a typical digital camera.

The spectra of the light emitted from shining spots marked as 1 and 3 is shown in figure 4.27. As it can be seen, the EL spectrum of both shining spots is quite similar. There appear the same three main EL peaks for both spectra.

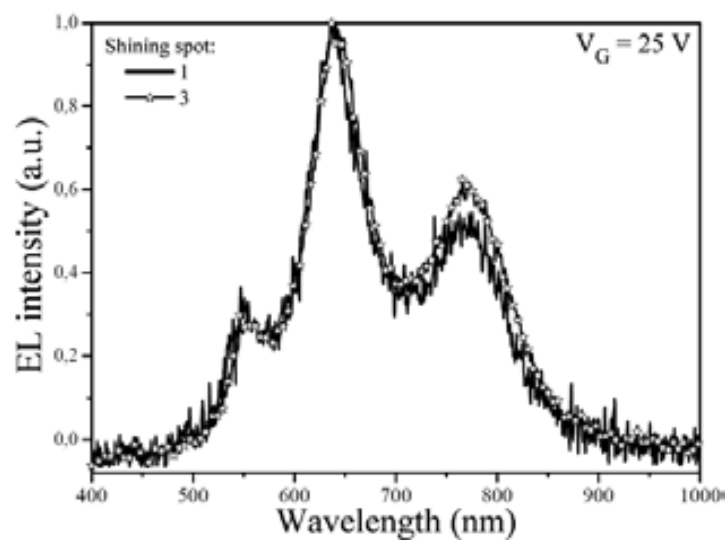


Figure 4.27. EL spectra measured from the shining spots marked as 1 and 3 for a gate voltage of 25 V (RB) in the figure 4.32.

The EL spectra as a function of the gate voltage at RB and measured from the shining spot marked as 3 is shown in figure 4.28(a). A broad spectrum with maximum peaks is observed for all gate voltages.

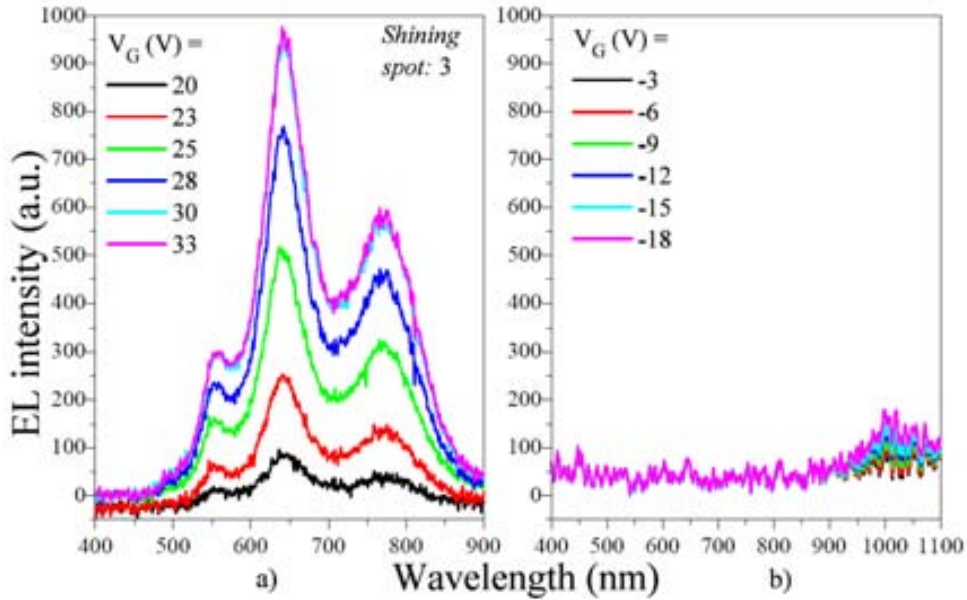


Figure 4.28. EL spectra measured from the device with 53 nm thick SRO when a) reversely and b) forwardly biased.

At FB, light emission is not observed between 400–900 nm, as shown in figure 4.28(b), but, an EL peak at about ~1000 nm with low intensity is observed. As mentioned before, this emission could be produced by the recombination of e-h pairs at the Si-substrate surface.

Gaussian fits to the EL spectra measured at RB were done and four EL peaks were obtained, as shown in figure 4.29(a). Three EL peaks at about 550, 650, and 770 nm are obtained for gate voltages of 20 and 23 V. However, for gate voltages above 23 V, other EL peak is activated at about 500 nm. All these luminescent peaks remain at the same wavelength when the gate voltage is increased. Nevertheless, their intensity is stronger as the gate voltage increases, as observed in figure 4.29(b). The intensity of the EL peaks increases in a linear way from 20 to 30 V and saturates when higher gate voltages are applied.

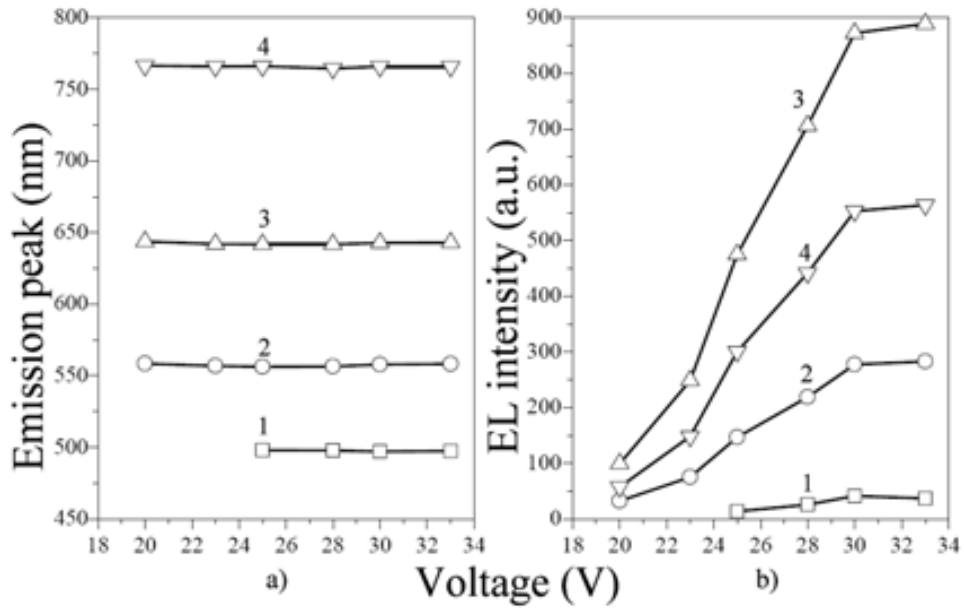


Figure 4.29. a) Wavelength and b) intensity of the EL emission peaks at RB and as a function of the gate voltage. Numbers indicate the emission peak at both position and intensity.

Figure 4.30 exhibits the EL intensity as a function of time when the MOS-like device with 53 nm thick SRO film and Si-excess of 4 at.% is reversely biased with 18.5 V. EL intensity remains stable at about 207 a.u. in the time and after 15 hours of operation.

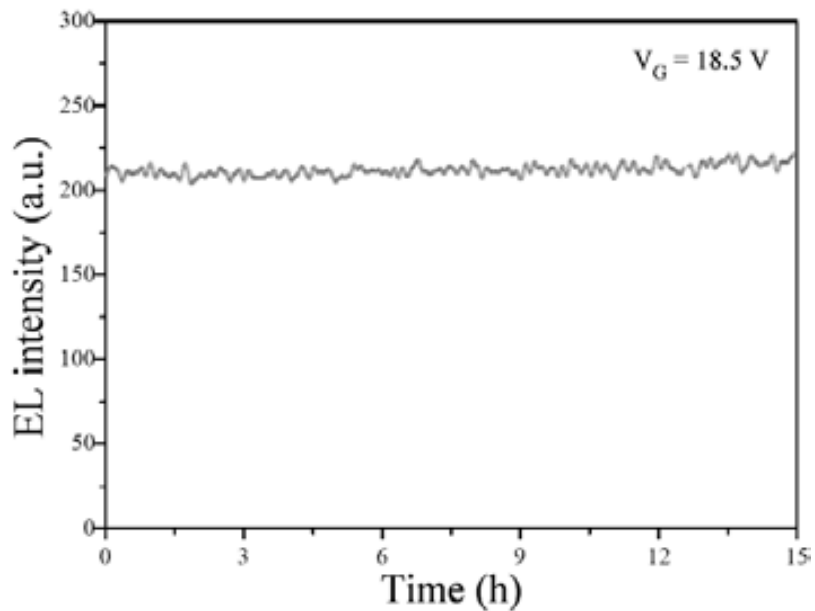


Figure 4.30. EL as a function of time measured from the MOS-like device with 53 nm thick SRO (4 at.% of Si-excess) when reversely biased with 18.5 V.

4.5. Summary

Metal–oxide–semiconductor (MOS) structures with five different gate areas and using the SRO films with 4 and 2.2 at.% of Si-excess as the dielectric layer were fabricated. The electrical and electro-optical properties of these devices were measured.

For SRO films with low Si-excess (2.2 at.%), electrical properties similar to the SiO₂ films were obtained. Nevertheless, C-V and I-V anomalous behavior where the current and capacitance drops were observed in the MOS-like structures with higher Si-excess (4 at.%).

These electrical properties were studied as a function of the gate area in the MOS-like devices with 53 nm thick SRO film. A clear correlation between capacitance and current dropping was observed. This capacitance and current dropping was obtained when the devices were forwardly and reversely biased or during the sweep voltage in the I-V measurement.

The conduction mechanism in these SRO films with 4 at.% of Si-excess was split in four different regions (A, B, C and D) depending on the operation voltage zone. The occurrence of each zone was studied as a function of the gate area.

Electro-optical studies were done under pulsed and continuous stimulation on devices with 4 at.% of Si-excess. For pulsed stimulation, a broad electroluminescent emission spectrum (400-900 nm) with maximum peaks was measured. The EL intensity was found to depend on the pulse width, being more intense as the pulse width was increased. However, a maximum and then switching-off of the EL intensity was observed.

At continuous stimulation, luminescent spots (seen with the naked eye) on the MOS-like devices appeared when the devices were reversely biased. A broad electroluminescent emission spectrum (400-900 nm) with maximum peaks was also measured. Fitting the EL spectra, peaks at about 450, 500, 550, 640, and 750 nm were obtained.

When the devices were forwardly biased, an EL peak at about ~ 1000 nm with low intensity was observed, which could be produced by the recombination of electrons flowing from the polysilicon gate with holes from the accumulated layer at the Si-substrate surface.

The EL intensity increased when the gate voltage was higher for both pulsed and continuous stimulation.

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Chapter 5

Correlation between optical and electrical properties

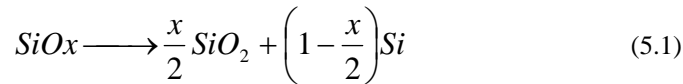
A discussion about the experimental results obtained and reported in chapter 3 and chapter 4 is presented with the aim of elucidate the mechanism that give rise in the optical and electrical properties of SRO films.

5.1. Composition, microstructure, and optical properties

The mechanism of light emission observed in silicon based materials has not yet been completely understood, specially the red one of the visible spectra. Depending on the emission wavelength, multiple luminescence centers (LC's) have been reported to act as radiative recombination centers. Defects, Si-nps, as well as interaction between defects at the SiO₂/Si-nps interface and Si-nps have been proposed. Luminescent (PL) peaks at 415, 450, 520, and 620 nm are mainly due to defects such as weak oxygen bond (WOB), neutral oxygen vacancy (NOV, O₃≡Si-Si≡ O₃), E'₈ defect (Si↑Si≡Si), and the non-bridging hole center (NBOHC, (O₃≡Si-O•), respectively [1-6]. However, due to differences in experimental results, the emission in longer wavelengths (red region) is still controversial and two main models have been proposed to explain that emission: the first one describes that the luminescence takes place in silicon nanocrystals (Si-ncs) by quantum confinement effects (QCE) where the emission is given as a band to band

radiative recombination of electron-hole pairs which are confined inside the Si-ncs [7-10] meanwhile the second model relates the PL with the presence of defects in the SiO₂/Si-nc interface [1, 3, 11-13].

It is widely accepted and demonstrated that Si-nanoparticles are created when SRO films are subjected to high temperature anneal because the thermal annealing produces a phase separation between Si and SiO₂ following the equation [7, 14]:



Then, when SRO films are thermally annealed, the silicon atoms diffuse creating silicon nanoparticles (Si_n, n ≥ 3) around of a nucleation site [1]. In this work, SRO films with different Si-excess were deposited varying the flow ratio between the reactant gasses (N₂O and SiH₄). Analyzing the obtained FTIR spectra of as-deposited films, it was observed that the TO₃ band slightly shifted toward higher frequencies as Ro was changed from 10 to 40 corresponding to a larger oxygen concentration. This assumption is confirmed with XPS, where Si-excess of 12.7, 5.1, 4.0, and 2.2 at.% was measured for Ro =10, 20, 30, and 40, respectively.

It can be deduced that a phase separation took place when the SRO and SI-SRO films were thermally annealed due to a displacement of the TO₃ band toward higher frequencies. Moreover, the FWHM is reduced after the thermal annealing, indicating that a microstructural arrangement is created in these films. Other important point is that impurities such as hydrogen (H) and nitrogen (N) were not observed in the SRO films according to the IR and XPS studies. This could be related to the temperature of deposition, about 720° C [15].

Based on the analysis of the XPS-Si2p spectra, the microstructure of SRO films was studied. The XPS-Si2p spectra indicated a combination of different coordinations of Si in the SRO films. Although the fitting of the XPS-Si2p peak of the SRO₄ and SRO_{5.1} did not show the presence of a silicon phase, the FTIR results indicated that a complete phase separation took place after thermal annealing. EFTEM images corroborated the presence of Si-nanoparticles inside of the SRO and SI-SRO films, where their mean size and density increased as the silicon excess was greater, according to other results [7, 16].

Si-nps inside the SRO₄ film were slightly observed after it was remained under the electron beam for a period of time; apparently, with a smaller mean size than the observed in the SRO_{5.1} (< 2.7 nm), as expected due to the lower silicon excess.

The fact that the Si2p–XPS peak from SRO₄ and SRO_{5.1} films did not show the presence of elemental silicon agglomeration (Si⁰), could be ascribed to the low sensitivity of Si2p–XPS in SRO films with low silicon excess, moreover, it has been reported that the clustered silicon concentration is significantly lower than the initial silicon excess concentration [17].

A strong PL was observed in these SRO and SI-SRO–LPCVD films. Different emission peaks were obtained depending on the silicon excess as shown in figure 5.1(a). As it can be seen, as the silicon excess increases the emission peak tends towards lower energy, that is, PL peak shifts from 1.74 and 1.71 eV to 1.62 when the silicon excess increases from 2.2 to 5.1 and 5.5 at.%, respectively.

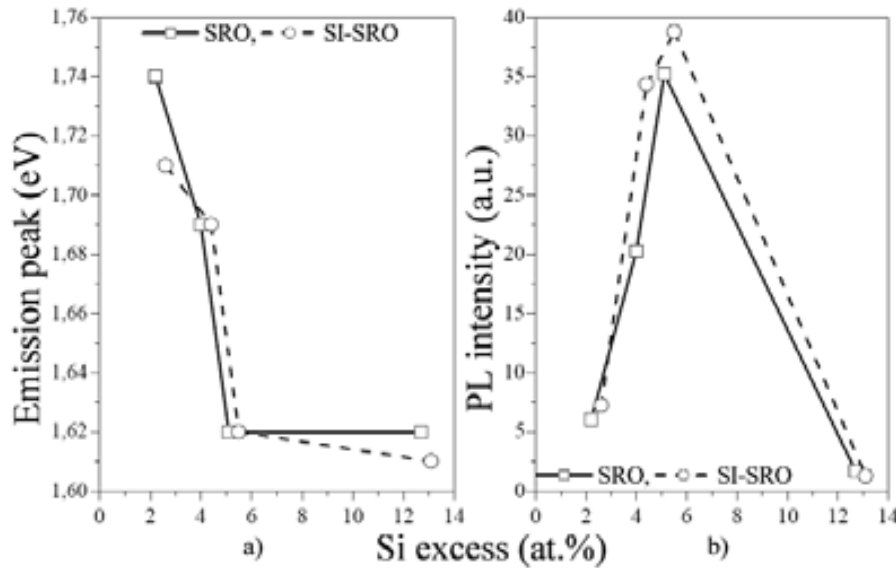


Figure 5.1. a) Energy and b) intensity of the emission peaks observed in the SRO and SI-SRO films annealed at 1100° C.

In [18], the authors related the PL of SiO_x (x < 2) films to quantum confinement effects (QCE) in materials which contain Si-ncs with a similar size of the Si-nanoparticles obtained in the SRO film with 5 at.% of silicon excess. Then, in our results, the PL band at 1.62 eV could be correlated to the Si-nanoclusters inside of the SRO_{5.1} film; however, in the SRO_{12.7} film (highest silicon excess) where the size of the Si-nanoparticles

increased, the PL band was strongly reduced (see figure 5.1(b)) and no redshift was observed, contrary to the QCE model. Therefore, other mechanism should be the responsible for the emission in these SRO and SI-SRO films.

A possible explanation is the presence of defects at the Si-nps/SiO₂ interface. In fact, it has been reported that a SiO_x shell exists at the surface of the Si-nps and then a SiO₂ matrix [19, 20]. Then, some defects in the SiO_x shell could exist. The participation of localized surface states or defects in the oxide has been suggested to influence the luminescent peak energy [12, 13]. Then these localized states, which can be induced by an atomic disorder, either compositional or structural, exist at the Si-nps' surface and are energetically placed within the band gap. As a result, there exists a direct relation between the Si-np's size and the PL intensity rather than with the emission energy.

Figure 5.2 depicts the mean diameter of the Si-nps and the PL intensity as a function of the silicon excess. It can be seen that the Si-nps' mean diameter becomes larger as the silicon excess increases, at the same time the PL intensity decreases. Then, there is a relation between Si-np's size and its surface. Therefore, since the surface to volume ratio increases as the Si-np's size decreases, the influence of surface states on the PL from smaller nanoparticles is highly enhanced. Furthermore, the PL peak was placed at the same energy (1.62 eV) independently of the Si-np's size.

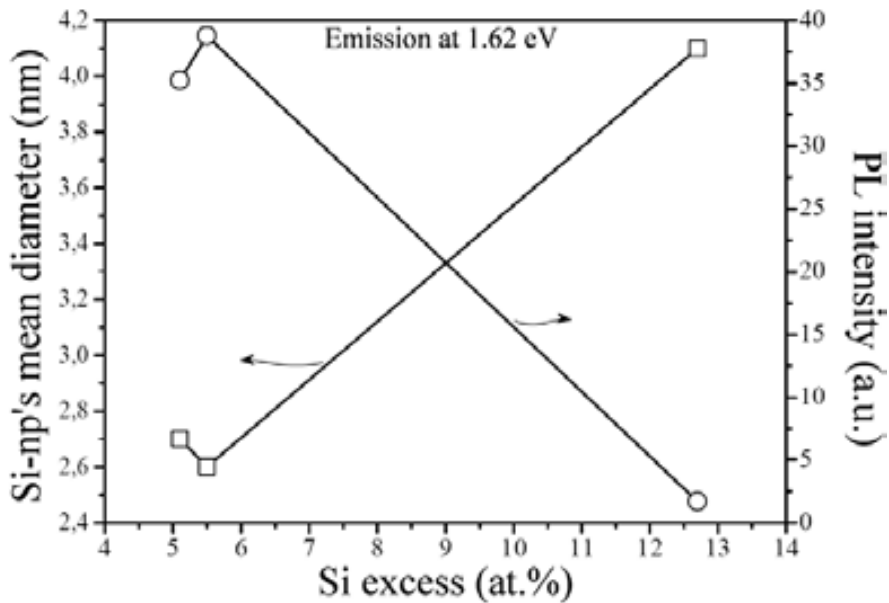


Figure 5.2. Relation between Si-nps mean diameter and PL intensity on the silicon excess in SRO and SI-SRO films emitting at 1.62 eV.

A maximum PL intensity was observed in the SRO and SI-SRO films where the mean size of Si-nps is about 2.7 ± 0.1 nm and 2.6 ± 0.1 nm (respectively), so 2.6 nm could be considered as the optimum size for these experiments. Figure 5.3 shows the dependence of Si-nanoparticles with mean size below 2.7 nm and the PL intensity on the silicon excess in SRO and SI-SRO films emitting at 1.62 eV.

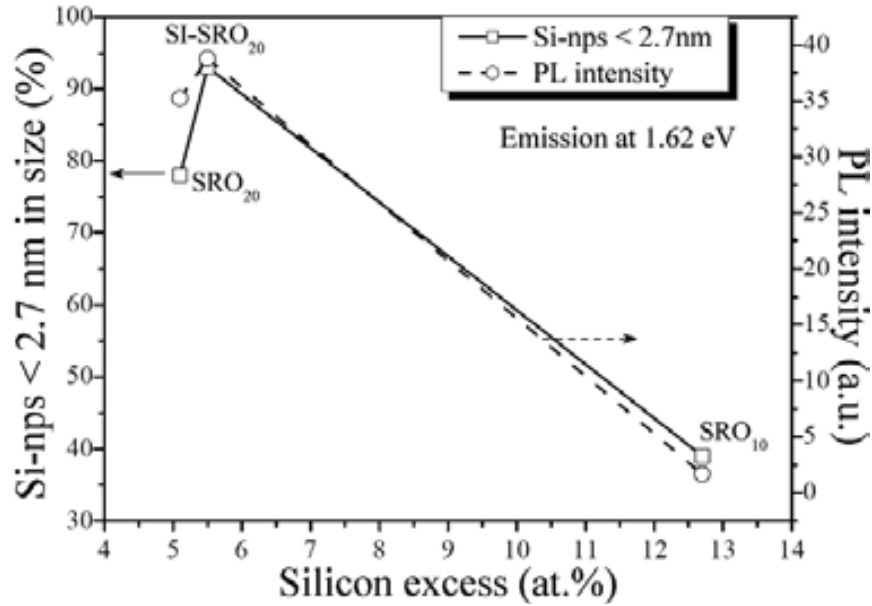


Figure 5.3. Dependence of the PL intensity and density of Si-nanoparticles with mean size below 2.7 nm on the silicon excess in SRO and SI-SRO films emitting at 1.62 eV.

For SRO films (SRO₂₀ and SRO₁₀), the number of Si-nanoparticles reduces as the silicon excess increases, as a consequence, a strong reduction of the PL intensity in the SRO film with 12.7 at.% of silicon excess was observed. When the SRO₂₀ film was implanted with silicon (SI-SRO₂₀), the number of Si-nps increased producing a more intense photoluminescence.

It is known that the implantation produces a scattering of atoms, then when the SRO films are implanted with silicon (SI-SRO films), Si and O atoms are scattered. Therefore, after the SI-SRO films are subjected to the thermal annealing, a higher density of Si-nanoparticles is obtained to interact with defects and therefore obtain a stronger PL intensity. Then, the silicon implantation rather than increasing the size of the Si-nps, it appears to increase the density of Si-nps.

As explained before, when the SRO films are thermally annealed, silicon tends to agglomerate, and then Si-nps and defects at their surface are created. Therefore, it can be considered that the Si nanoparticles are surrounded by defects and they could be acting as localized states. As a result, the mechanism of emission can be explained as follows: The e-h pairs are generated inside the Si-nps. Then, electrons are excited to the defects, and the emission takes place when electrons in the localized state return to the positive Si-nps, or the ground state. When the size of the Si-nps is small, the band gap energy is large, and then the energy difference between the localized state and the ground state is big enough to produce the emission. This is similar to the donor-acceptor mechanism of emission in semiconductors. As their size increases, the energy difference is reduced, and eventually, when the size exceeds an optimum size, the energy of the localized state will be such that electrons decay will not produce emission, and then PL will not be observed. The optimum size of Si-nps required in which a maximum PL intensity is observed for these experiments is about 2.6 nm.

5.2. Electrical properties

MOS-like structures using SRO films with 4 and 2.2 at.% of Si-excess as the dielectric layer were fabricated and electrically characterized. In the fabrication process, the SRO films were thermally annealed in order to produce the agglomeration of Si-excess and therefore Si-nps. SRO films with Si-excess of 2.2 at.% showed an electrical behaviour similar to a SiO₂ film. Nevertheless, C-V and I-V anomalous behaviours were obtained in the MOS-like structures with 4 at.% of Si-excess. In this SRO films, Si-nps with size below 2.7 nm must be embedded, as evidenced by EFTEM images. Moreover, due to the low silicon excess and assuming a dispersion in the Si-nps' size, other very small Si-nps (< 1 nm, with few Si atoms bonded) could exist.

C-V and I-V anomalous behaviors were obtained in the MOS-like structures with 4 at.% of Si-excess, where the current and capacitance drops. The anomalous CV and IV could be owing to the existence of the very small Si-nps connecting the larger ones or possibly due to the distance between Si-nps. It could happen that the distance between Si-nps be quite small making that the charges flow without being trapped.

To understand our results, we will call “clusters” to the very small Si-particles (< 1 nm) and “Si-nps” to the more stable nanostructures (≥ 1 nm). It is expected that all of these Si-nps and Si-clusters (Si-cl) would be randomly distributed; such as some of the Si-clusters could be placed between stable Si-nps, as shown in figure 5.4(a). In this system, it is assumed that the charges do not flow uniformly through the whole capacitor area, but instead, it passes through narrow conductive paths within the oxide.

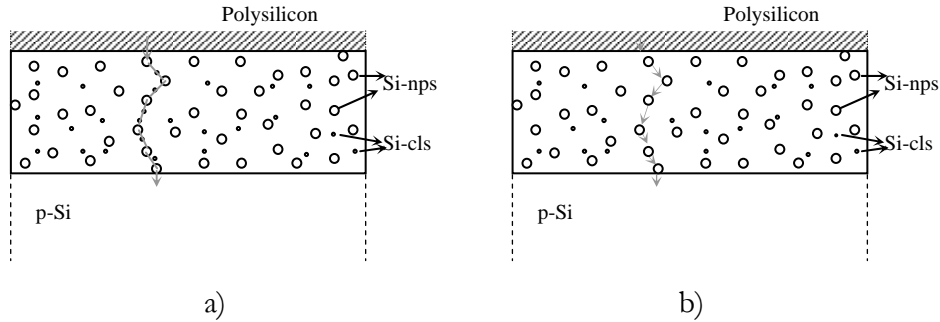


Figure 5.4. Scheme of the MOS-like structure a) before and b) after the capacitance and current dropping.

As mentioned before, it is expected that all of these Si-nps and Si-cl could be randomly distributed; such some of the Si-cl could be placed between Si-nps. If the distance between them is small, they can act as conduction paths between the polysilicon gate and the Si-substrate and then making possible a high current conduction at low voltages. Therefore, the only possible reason for the capacitance and current dropping is a change in the conductivity of the films by the annihilation of the Si-cl’s effect, as shown in figure 5.4(b).

A particular case may be depicted by the E’ centers formation [21] in our SRO films. E’ centers can be created in the SRO films when charges are injected into the film breaking-off Si-Si bonds during the negative (positive) voltage sweep or during the negative (positive) electrical stress. This would explain why the capacitance drops to a low value without a noticeable V_{FB} shifting.

The accumulation capacitance values measured before and after stressing the MOS-like structures with 53 nm thick SRO film and 4 at.% of Si-excess are shown in table 5.1. The theoretical value of the silicon oxide capacitance of an equivalent MOS structures (C_{SiO_2}) is also listed and it would be 620.7, 148.9 and 20.9 pF for each gate area of 9.604

$\times 10^{-3}$, 2.304×10^{-3} , and $3.24 \times 10^{-4} \text{ cm}^2$, respectively. These values of capacitance for a SiO_2 film, as calculated for each gate area, are smaller than the SRO capacitance measured from as-fabricated devices. However, the theoretical capacitance is slightly closer to the mean value of the capacitance measured after apply a $V_G = V_{\text{drop}}$ for each gate area (measure 2).

Table 5.1. Experimental accumulation capacitance from MOS-like structures with 53 nm thick SRO film and 4 at.% of Si-excess before and after applying a constant gate voltage. A theoretical maximum capacitance of a SiO_2 film with the same thickness than SRO film is also reported.

Gate area (cm^2)	C_{SRO} (pF)		Theoretical C_{SiO_2} (pF)
	Measure 1	Measure 2	
	As-fabricated	After $V_G = V_{\text{drop}}$	
9.604×10^{-3}	707.6 ± 26.02	494.8 ± 6.65	620.7
2.304×10^{-3}	269.2 ± 7.08	131.2 ± 0.82	148.9
3.24×10^{-4}	212.2 ± 6.84	18.1 ± 1.69	20.9

Therefore, the total capacitance (C_T) of these MOS-like structures could be given by the combination of the capacitance of the SRO film (C_{SRO}) in series with the capacitance of silicon substrate surface (C_S), where C_{SRO} is represented by the sum of Si-nps (C_{np}), Si-cls (C_{cl}), and SiO_2 (C_{SiO_2}) capacitances, as depicted in the equivalent circuit shown in figure 5.5(a), where the total capacitance is given by:

$$C_T = \frac{C_{\text{SRO}} \cdot C_S}{C_{\text{SRO}} + C_S} = \frac{(C_{\text{np}} + C_{\text{cl}} + C_{\text{SiO}_2}) \cdot C_S}{C_{\text{np}} + C_{\text{cl}} + C_{\text{SiO}_2} + C_S} \quad (5.2)$$

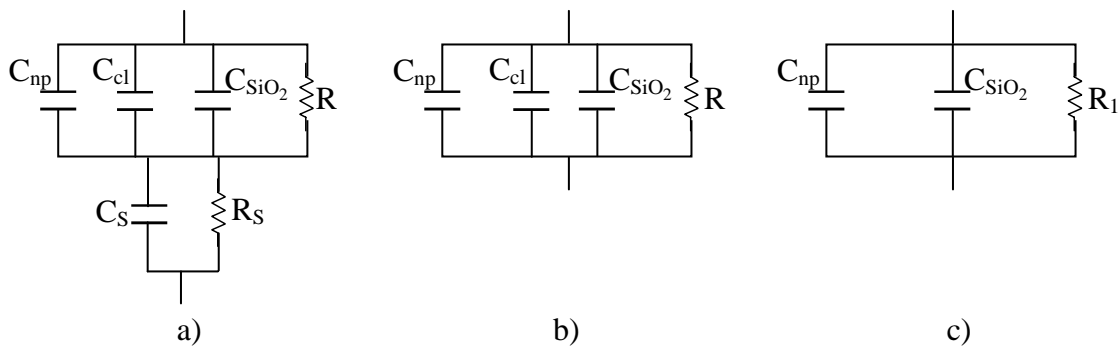


Figure 5.5. Equivalent circuit of MOS-like structures with 4 at.% of Si-excess a) without any electrical stress and in accumulation region b) before and c) after the current and capacitance drop.

At negative gate voltages ($V_G < 0$), that is, when the devices are in accumulation region, C_s is much higher than C_{SRO} and thus, the total capacitance is dominated by the SRO capacitance, i.e., $C_T = C_{SRO} = C_{np} + C_{cl} + C_{SiO_2}$, as depicted in figure 5.5(b), where the resistance R is the sum of Si-nps, Si-cls, and SiO₂ resistances as $R^{-1} = R_{np}^{-1} + R_{cl}^{-1} + R_{SiO_2}^{-1}$. As the silica resistance is expected to be quite high, $R_{cl} < R_{np} \ll R_{SiO_2}$, we can assume that the Si-nps and Si-cls contribution to the total resistance should be prevalent, such as $R = \sim R_{np} + R_{cl}$.

In as-fabricated devices there is a plenty of Si-nps and Si-cls which contribute with large capacitance, therefore the total capacitance is high as well. However, an electrical anneal, which drastically diminishes the Si-cls contribution (E' centers formation), can be produced by applying $V_G = V_{drop}$ for 60 seconds or during a sweep voltage in the I-V measurements. As a result, C_{cl} becomes very small and the total capacitance is also decreased getting close to C_{SiO_2} , as depicted by the equivalent circuit from figure 5.5(c). Now, $R = R_1 = \sim R_{np} + R_{SiO_2}$. Then, R increases and the capacitance effect in the MOS-like devices become now dominant.

The conduction mechanism in these SRO films with 4 at.% of Si-excess was split in four different regions (A, B, C and D) depending on the operation voltage zone, as shown in figure 4.16 and repeated as figure 5.6 below in order to clarify. Moreover, it was found that the reduction of capacitance is directly correlated to the reduction of current.

In the A zone, the current exhibits a strong dependence on the gate voltage, as shown in figure 5.6(a). Then, in this zone Si-cls could be acting as traps near to the mid-gap of SRO film making possible the high current conduction at low voltages. Indeed, current fits well to the TAT model as [22]:

$$J = J_0 \cdot e^{\left(\frac{B}{E}\right)} \quad (5.3)$$

Where E is the electric field through the SRO film. Values of $J_0 = 0.6$ and 2.32 A/cm² and $B = 1.435 \times 10^6$ and 8.82×10^6 MV/cm were found for negative and positive biases, respectively.

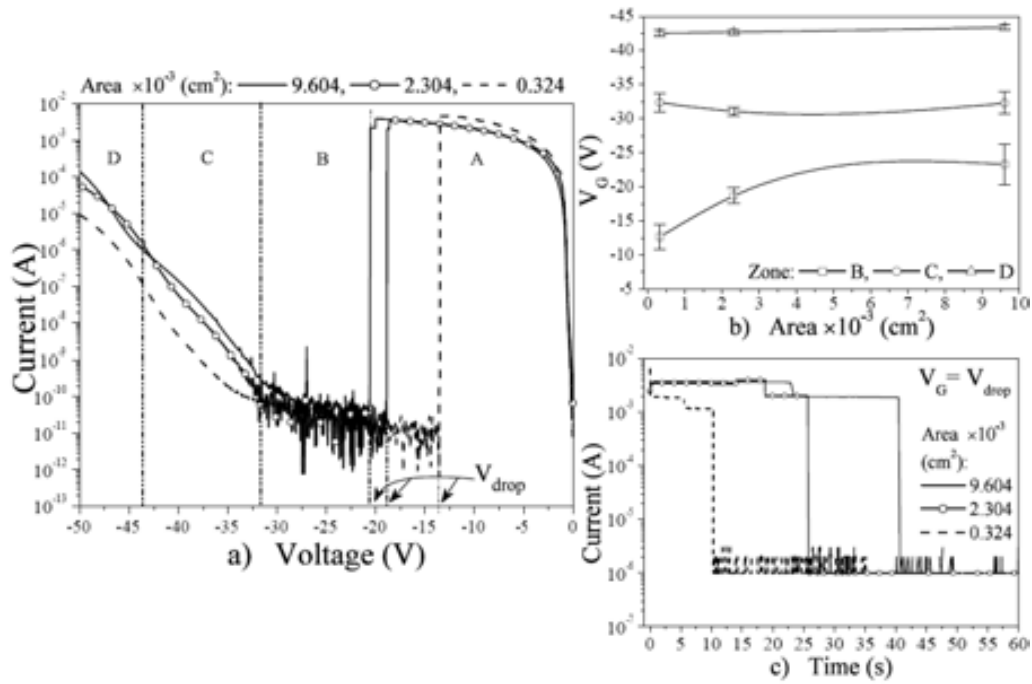


Figure 5.6. a) I-V curves done with a sweep rate of 0.1 V/s, b) Occurrence of the different zones as a function of gate area (lines are plotted as an eye-guide), and c) I-t curves at a gate voltage $V_G = V_{drop}$ of MOS-like structures with different gate area and Si-excess of 4 at.%.

The breaking-off of Si-Si bonds in the Si-cls (< 1 nm) embedded in SRO films lead to a strong decreasing in current by the annihilation of conduction paths. In as-fabricated devices, these Si-cls are undamaged and then conduction paths are available for the current flow. During the sweep at negative (positive) voltage, electrons from polysilicon gate (Si-substrate) tunnel into the SRO film through such conduction paths. When charges are flowing through the Si-cls, they break-off some of their Si-Si bonds (E' center), annihilating in that way the conduction paths and leading to current drops. The difference between the voltage needed to obtain the current dropping at forward and reverse bias is due to the P-type Si-substrate.

For high electric fields -C and D voltage regions- at both forward and reverse biases, Fowler-Nordheim plots were used to fit data, see figure 5.7. Data fits quite well at both C and D regions with F-N conduction regimes, as shown in figure 5.7(a) and figure 5.7(b), respectively. At C region, the conduction could be dominated by the flow of electrons from the polysilicon gate (Si-substrate) towards the Si-substrate (polysilicon

gate), meanwhile as the electric field is higher (D region), the flow of holes is enhanced and an increase in the conductivity is obtained.

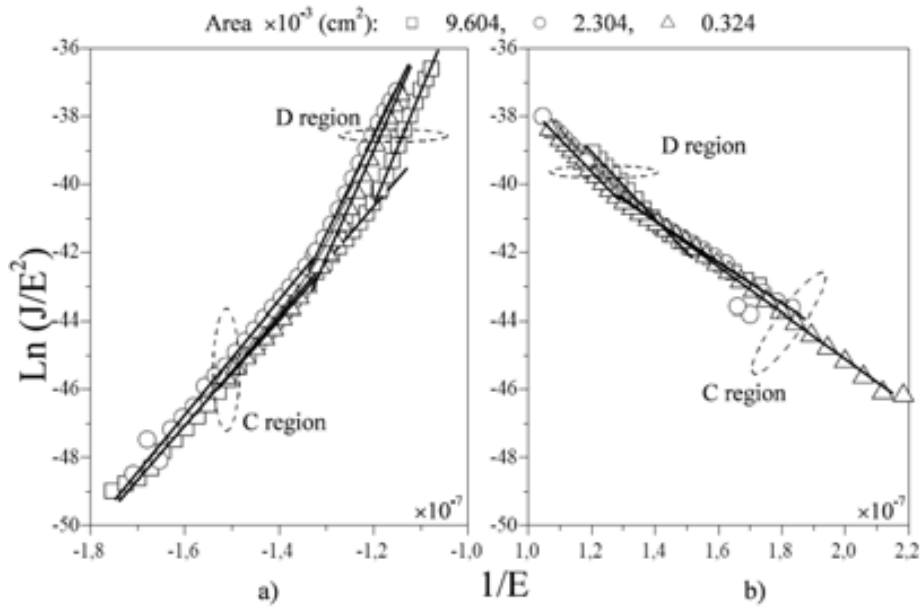


Figure 5.7. $F-N$ plots at a) FB and b) RB from devices with 53 nm thick SRO (4 at.% of Si-excess) and three different gate areas where a linear region in high voltages is observed. Symbols and lines are the experimental data and linear fits, respectively.

Once the current has dropped, the current conduction is observed at high electric fields and due to Fowler–Nordheim tunnelling.

The results showed above and their analyses have been exposed taking into account the existence of Si-cl and that their separation is quite small. However, when the distance between Si-np and Si-cl is large, the flow of charges is not in a continuous way. Instead, charges flow from Si-np to Si-np or Si-np to Si-cl and in that process, charges can get trapped in Si-np. This phenomenon has been demonstrated to depend on the sweep rate.

Figure 5.8 shows the $C-V$ curves measured from inversion to accumulation and at different sweep rates in both SRO films (24 and 53 nm thickness) with 4 at.% of Si-excess. In these $C-V$ curves, the charge trapping (Ch) is observed in the form of downward valleys.

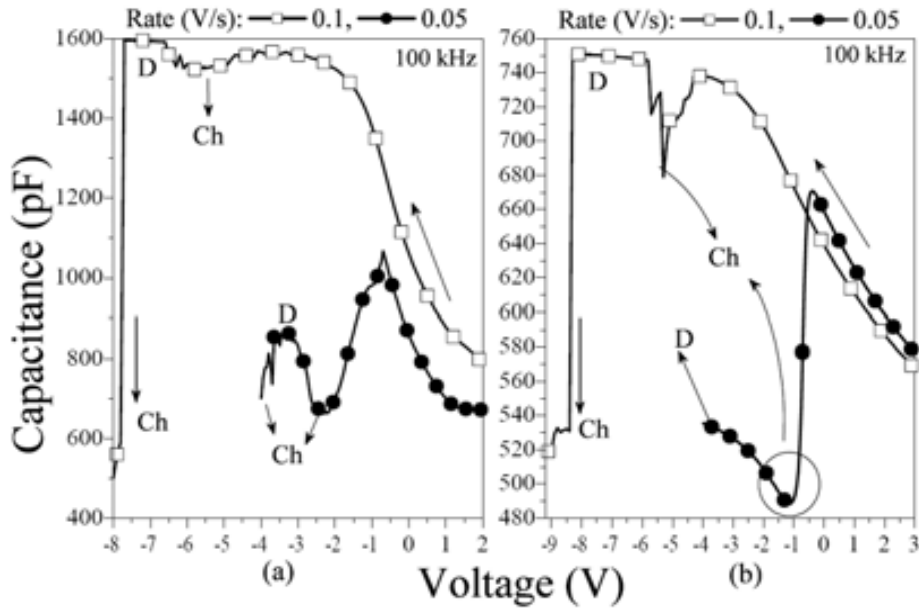


Figure 5.8. Charge trapping (Ch) and de-trapping (D) effects observed in C - V curves of MOS-like structures with gate area of $9.604 \times 10^3 \text{ cm}^2$ and using SRO films (4 at.% of Si-excess) as the active layer and thickness of a) 24 nm b) 53 nm for two different sweep rates.

The C - V curves of the MOS structure with 24 nm thick SRO film are depicted in figure 5.8(a). When the sweep was done at a rate of 0.1 V/s, a downward valley was obtained in the capacitance between -4.5 and -6.5 V. As the gate voltage becomes more negative, the capacitance tends to increase to a maximum value. However, when voltage is even more negative, the capacitance decreases three times in an abrupt way (until 500 pF). For a sweep rate of 0.05 V/s, the maximum capacitance value is not reached, but a downward valley is observed at a lower capacitance value and at a lower voltage. Afterwards, the capacitance tends to rise as the negative gate voltage becomes larger, but finally decreases.

Similar behaviour was observed in the MOS-like structure with 53 nm thick SRO films, as depicted in figure 5.8(b). A downward valley between -4.2 and -5.8 V and an abrupt decreasing in capacitance at -8.4 V were measured for a fast sweep. When the sweep rate was reduced to 0.05 V/s, then the accumulated capacitance jumps to a lower value at a small voltage of about -0.5 V.

As mentioned before, Si-nps inside these SRO films create conduction paths between the substrate and polysilicon gate. Therefore, these effects would be associated with the charge trapping (Ch) and de-trapping (D) in the Si-nps during the voltage sweep, as

indicated in figure 5.8. A possible explanation will be discussed later. Figure 5.9(a) shows the current–voltage characteristics of both MOS-like devices with 4 at.% of Si-excess (24 and 53 nm thick SRO) for a sweep rate of 0.05 V/s. Different anomalies are observed for both thicknesses, such as the spike-like peaks, current jumps and a very clear staircase current.

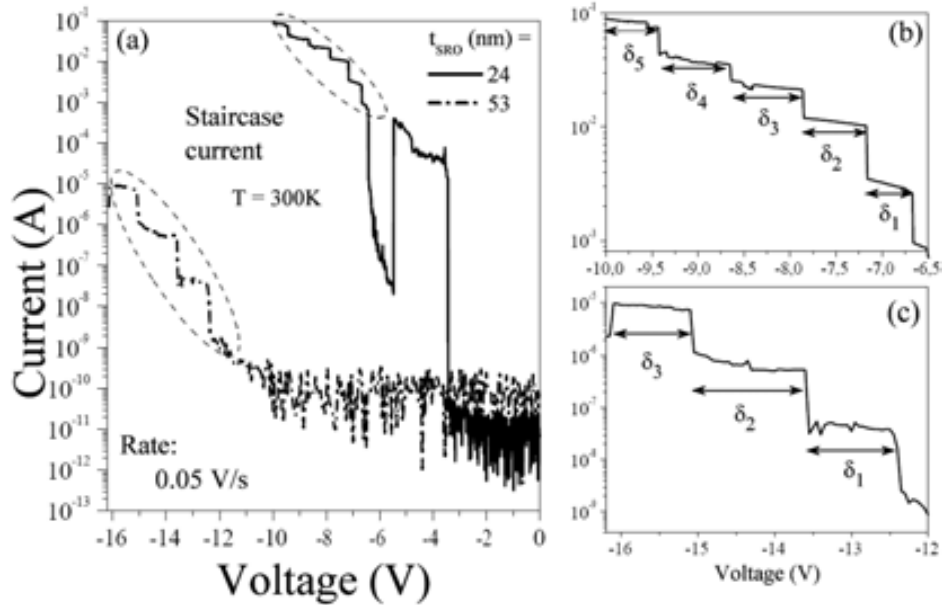


Figure 5.9. a) Current–voltage characteristics of MOS-like structures with gate area of $9.604 \times 10^3 \text{ cm}^2$ and zoom-in showing the clear staircase current in b) 24 nm thick SRO and c) 53 nm thick SRO (4 at.% of Si-excess).

For the thin SRO film (24 nm), current fluctuations, sudden current jumps and staircase current were observed in the voltage ranges of 0 to -3.4 V , -3.5 to -7 V , and -7 to -10 V , respectively. For the thick SRO film, current fluctuations and staircase current were observed in voltage ranges of 0 to -12 V and -12 to -16 V , respectively.

As it can be seen, the stair width for the thin SRO film is smaller than that of thicker SRO, although it varies for each kind of device, as shown in figures 5.9(b) and 5.9(c). These effects could be associated with that charge trapping and de-trapping effects observed in the form of downward valleys in $C-V$ curves during the sweep voltage.

It has been stated that the total capacitance (C_T) of the MOS-like structure is given by the combination of the capacitance of the SRO film (C_{SRO}) in series with the capacitance of silicon substrate surface (C_S) as equation 5.2. Moreover, the total capacitance in the

accumulation region is dominated by the SRO capacitance as $C_T = C_{SRO}$. Therefore, the observed effects such as downward peaks in the C-V curve during the voltage sweep would be related to changes in C_{SRO} .

Then, during the voltage sweep, when V_G is negative, holes accumulate at the substrate surface meanwhile electrons do in the polysilicon gate. These charges, whether electrons or holes tunnel into the SRO film through the conduction paths. Charges close to Si-nps can get trapped in the Si-nps and if charge-trapping occurs, some conduction paths will be switched-off due to the Coulomb blockade effect.

At a fast sweep rate (0.1 V/s), most of the carriers can transport through the entire SRO layer. However, at a slow sweep rate (0.05 V/s) and when the bias is larger than a threshold value, charge-trapping will occur and in this case, most of the conduction paths will be blocked, making the capacitance at a lower value.

The transport mechanism for the staircase observed in $I-V$ curves (figure 5.9) could be explained in a similar way: In zero bias, the Si-nps are uncharged and therefore the band diagram does not present bending as shown in figures 5.10(a) and 5.10(b), respectively.

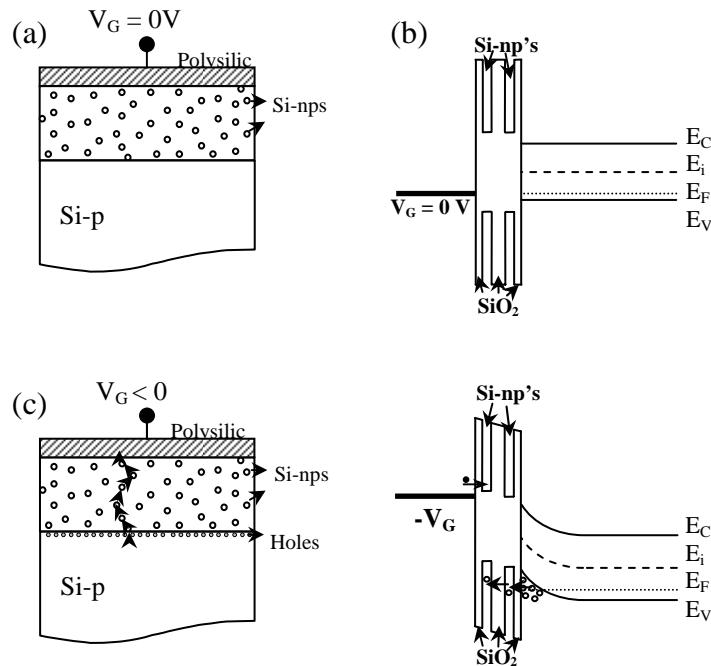


Figure 5.10. Schematic of MOS-like structure with SRO film and band diagram at a), b) zero bias and c), d) with negative voltage applied at gate, respectively.

However, at a certain negative voltage, -7 and -12 V for 24 and 53 nm thick SRO film, respectively, holes at the SRO/Si interface tunnel towards the polysilicon gate through adjacent Si-nps (conduction path) as shown in the schematic of figures 5.10(c) and 5.10(d).

At the same time, electrons at the polysilicon/SRO interface could tunnel towards the silicon substrate through adjacent Si-nps as well. In this transport mechanism, when a Si-np is charged, this charge blocks other charges trying to tunnel to or through this Si-np. As the voltage becomes more negative, the band bending is even larger, more electrons and holes accumulate at the polysilicon/SRO and SRO/Si interface, respectively, forcing finally to that trapped charge in the Si-np to tunnel out, switching on the current path and as a result a current jump is observed. Different charged Si-nps require a different amount of accumulated charge, i.e. voltages to discharge, so between two discharges, a current plateau is observed (see figure 5.9). Therefore, the observed staircase behaviour is due to the concatenation of these two phenomena, i.e. current jumps and plateaus. Variations in the width of plateau (δ_i) observed in figures 5.9(b) and 5.9(c) are produced by the Si-nps' size and their separation.

Since the SRO films contain embedded Si-nps, it would expect that properties such as the dielectric constant must to be different from that of SiO₂ films. It is known that Si-nps inclusion produces differences in the electrical properties such as current conduction, shifts in the flat band voltages, and some others [23].

The expression of the SRO capacitance in accumulation is given by equation 5.4, where A is the gate area, $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm², C_{SRO} and t_{ox} are the capacitance and thickness of the SRO film, respectively. k_{SRO} is estimated to be 4.9, as calculated using equation 5.4. This value is slightly larger than the SiO₂ value (3.9), as expected by the silicon excess in the film.

$$C_{SRO} = \frac{Ak_{SRO}\epsilon_0}{t_{ox}} \quad (5.4)$$

k_{SRO} would represent an average value for Si-nps embedded in the SRO film. A relation between the dielectric constant of Si-nps and their size has been reported [24] as:

$$\varepsilon_{SRO} = 1 + \left\{ \frac{(\varepsilon_{Si} - 1)}{\left[1 + (1.38/d)^{1.37} \right]} \right\}. \quad (5.5)$$

Where ε_{Si} is the dielectric constant of bulk crystalline silicon, d is the Si-np's size and ε_{SRO} the permittivity of SRO film calculated from equation 5.6. The Si-nps' size as estimated from equation 5.5 is about $d = 0.95$ nm.

$$\varepsilon_{SRO} = k_{SRO} \cdot \varepsilon_0 \quad (5.6)$$

Since silicon excess is low, we could expect the separation between two nearby Si-nps (t_{np-np}) to be larger than the mean size of Si-nps. Actually, as reported in other works for SRO films with silicon excess below 6 at.% [22] t_{np-np} should be ~ 10 nm.

Taking into account nearly spherical Si-nps with diameter d , the self-capacitance of the nanoparticles and the inter-capacitance between two nearby Si-nps can be estimated from equations 5.7 and 5.8, respectively.

$$C_{np} = 2\pi\varepsilon_0 d \quad (5.7)$$

$$C_{np-np} = A_{np}\varepsilon_0/t_{np-np} \quad (5.8)$$

where

$$A_{np} = \pi d^2/4 \quad (5.9)$$

The corresponding Coulomb charging energy (E_C) and the stair width (V_{stair}) are obtained by using equations 5.10 and 5.11, respectively, with q as the elementary charge.

$$E_C = q^2/2(2C_{np-np} + C_{np}) \quad (4.10)$$

$$V_{stair} = q/2(2C_{np-np} + C_{np}) \quad (4.11)$$

Thus, with $d = 0.95$ nm; $C_{np} = 5.28 \times 10^{-20}$ F, $E_C = 1.04$ eV and $V_{stair} = 1.04$ V are obtained.

Table 5.2 reports the stair width δ_i ($i = 1, \dots, n$) values from the staircase current observed in figure 5.9. Making the stair width δ_i to be equal to V_{stair} , the Si-np size (d), self-capacitance (C_{np}), capacitance between two nearby Si-nps (C_{np-np}) and the Coulomb charging energy (E_C) can be calculated according to the equations above for each δ_i . Results are also listed in table 5.2.

Sample	Stair (V)	d (nm)	Cnp (F)	Cnp-np (F)	E _C (meV)	
24 nm	δ_1	0.49	1.64	9.12×10^{-20}	3.63×10^{-20}	490
	δ_2	0.68	1.30	7.23×10^{-20}	2.28×10^{-20}	680
	δ_3	0.78	1.18	6.56×10^{-20}	1.88×10^{-20}	780
	δ_4	0.77	1.18	6.56×10^{-20}	1.88×10^{-20}	780
	δ_5	0.57	1.48	8.23×10^{-20}	2.96×10^{-20}	570
53 nm	δ_1	1.10	0.91	5.06×10^{-20}	1.12×10^{-20}	1100
	δ_2	1.30	0.80	4.45×10^{-20}	8.65×10^{-21}	1300
	δ_3	1.05	0.94	5.23×10^{-20}	1.19×10^{-20}	1050

Table 5.2. Theoretical results calculated from δ_i of figure 5.9.

It can be seen that the average size of Si-nps is around 1.36 and 0.89 nm for the structures with 24 and 53 nm thick SRO films, respectively. These values are very close and agree with that obtained before. Nevertheless, a variation in V_{stair} from 0.49 to 0.78 V and from 1.05 to 1.3 V can be observed for the 24 and 53 nm thick SRO film, respectively. This variation is ascribed mainly to the variation in the size of Si-nps as well as variations in their separation, as observed in the calculated size of Si-nps and reported in table 5.2. Because the charging energy of the Si-nps is much larger than the thermal energy at room temperature (26 meV), Coulomb blockade effects were observed at room temperature in the MOS-like devices from this work.

A staircase current was also observed after the current dropped (see figure 4.18(b), page 68). As the current dropping was ascribed to the annihilation of conductive paths

produced by Si-clusters, and more stable Si-nps remained embedded in the SRO films. Then, once the current has dropped, the conductive paths are available through these more stable Si-nps. It can be assumed that the conduction will be through Si-nps. The mean stair width (V_{stair}) value obtained from that stair current is about 1.21 ± 0.06 V. If t_{np-n} is close to ~ 10 nm, then the size of Si-nps is about 1.15 ± 0.06 nm. This value is in accordance with the obtained before. Moreover, it is demonstrated that Si-nps with ~ 1.1 nm are inside the SRO films with 4 at.% of Si-excess and this effect could explain why they were not observed at first glance with EFTEM.

5.3. Electro-optical properties: Model verification

The model exposed above involving Si-nps, and Si-clusters may correlate the optical and electrical properties of the SRO films presented in this work. A broad electroluminescent emission spectrum was observed in MOS-like devices with SRO films (4 at.% of silicon excess) at both, alternating the gate voltage in pulsed way and direct current voltage. Unlike the EL peaks were observed at 450, 500, 550, 640, and 750 nm, in PL emission only one peak was observed at 734 nm.

In order to understand the light emission process in these devices the time resolved EL measured at a driving voltage of 20 V is analyzed, as shown in figure 5.11.

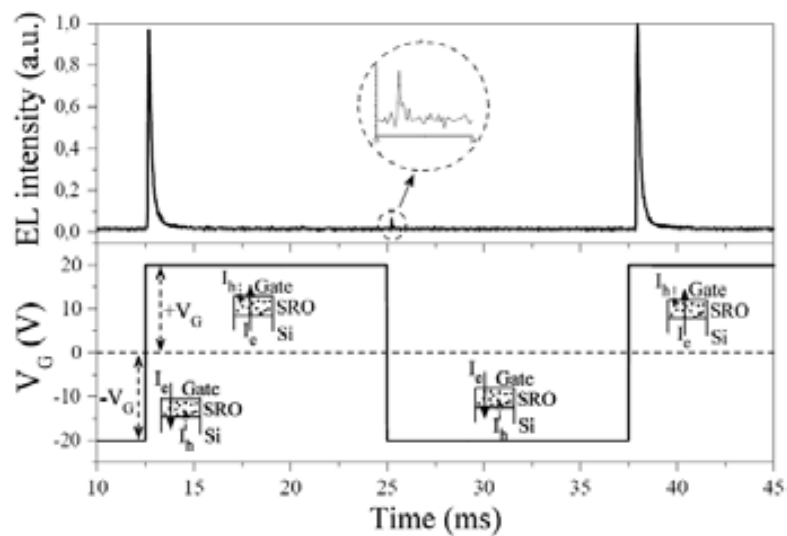


Figure 5.11. Time resolved EL of 53 nm thick SRO film in MOS-like devices biased with a pulsed voltage of $V_G = \pm 20$ V.

A stretched exponential EL behaviour is observed after alternating the voltage bias from negative (positive) to positive (negative). However, a low intensity EL was observed when the bias was changed from positive to negative voltage compared to the contrary switching.

This can be understood as follows: when the pulse excitation is at negative voltage, electrons from the polysilicon gate flow toward the Si-substrate through the SRO film (I_e). At the same time holes do from the Si-substrate towards the polysilicon gate (I_h). However, as observed in the electrical characterization, the electrons conduction domains. When the pulse changes from negative to positive voltage, an inversion layer at the Si-substrate surface is formed. Then, electrons are now injected into the SRO film from the inverted layer meanwhile holes are supplied from the polysilicon gate. Electrons which were flowing during the positive pulse towards the Si-substrate come back to the polysilicon gate and add to the electrons coming from the Si-substrate, recombining with that holes supplied from the gate, and then light is emitted. At the same time, holes which were flowing towards the polysilicon gate from the Si-substrate come back to the Si-substrate recombining with that electrons supplied from the inverted layer, and then light is emitted. Therefore, the emission is obtained at both inside the SRO film and at the Si-substrate surface, because of this, the EL spectra exhibit the visible (~450-800 nm) and infrared (~1000 nm) emission bands, respectively.

When the pulse excitation comes back to negative, electrons are newly injected from the polysilicon gate and holes from the accumulation layer, e-h pairs are created again. EL emission is observed, but with a lower intensity. This difference in EL intensities could be due to the electrons tunnel directly toward the substrate and recombine with holes from the Si-substrate.

Other explanation is the exposed by Walters [25], where holes and electrons trapping in Si-nps are obtained during the negative and positive pulse, respectively. This charge trapping creates e-h pairs, which recombine emitting light. However, from the electrical characterization, it has been observed that the resistivity of SRO is low, producing that the charges flow directly from the polysilicon gate (Si-substrate) towards the Si-substrate (polysilicon gate) at negative (positive) voltages.

This can be clarified if the bipolar stimulation pulse is separated at both positive and negative pulsed stimulation. Figure 5.12(a) exhibits the EL spectra from the MOS-like structure when it is biased with a positive stimulation pulse of 26 V. It shows a broad emission which goes from 450 to 900 nm, such as the observed in continuous EL.

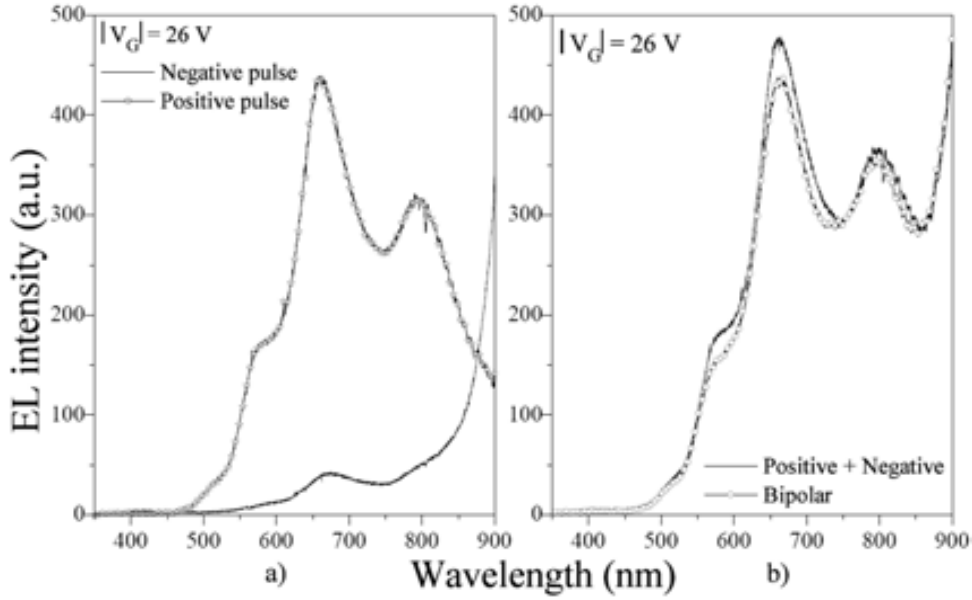


Figure 5.12. EL spectra measured from MOS-like devices with 53 nm thick SRO film at a) negative and positive stimulation pulse, b) sum of both EL spectra and EL spectra obtained with a bipolar stimulation pulse.

For the negative pulse stimulation, the emission at 450 to 900 nm is strongly reduced and an emission peak at wavelength above of 900 nm is observed. Moreover, when the EL spectra obtained from the positive pulse is added to that obtained with the negative pulse, an EL spectra quit similar to the measured with bipolar stimulation is obtained, as shown in figure 5.12(b).

The mean lifetime was also analyzed by fitting the EL decay with a stretched exponential [26]:

$$I(t) = I_0 e^{\left(-t/\tau\right)} \quad (5.12)$$

A mean lifetime of 109 μs has been found for a driving voltage of 28 V and pulse width of 50 ms, as observed by the fitting from figure 5.13. This value is a typical mean lifetime for Si-ncs' systems.

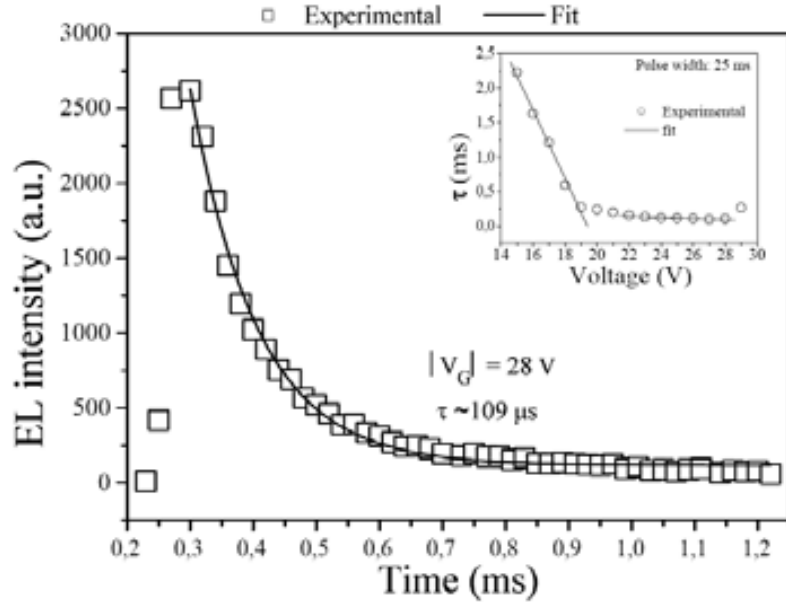


Figure 5.13. EL decay from device biased with 28 V and pulse width of 50 ms. Inset shows the mean lifetime (τ) as a function of the pulsed gate voltage.

The dependence of the mean lifetime on the driving voltage showed two behaviours as observed in the inset of figure 5.13. First, the mean lifetime decreases from 2.23 ms to 201 μs as the driving voltage is increased from 15 to 21 V, and second, the mean lifetime remains constant at about 109 μs for driving voltages above 21 V. Due to the light was collected without analysing it with a monochromator, that is, light at different wavelengths is collected, these two behaviours could be related to the emission of the Si-substrate as well as Si-nps and Si-cls (traps) in the infrared ($\sim 1000 \text{ nm}$) and the visible red ($\sim 600\text{-}800 \text{ nm}$) wavelengths, respectively.

Si-nps ($\sim 1 \text{ nm}$, as theoretically calculated) and Si-cls ($< 1 \text{ nm}$ in size) are embedded in these SRO films. Nevertheless, probably weak oxygen bonds (WOB), neutral oxygen vacancy (NOV) and non-bridging oxygen hole center (NBOHC) defects could be also present due to the silicon excess or created by the electrical stress; however, it is possible that these defects are not stimulated by light excitation in our SRO films during the PL measurements. In fact, cathodoluminescence (CL) studies on SRO films with the same

silicon excess as SRO films from this work exhibit an emission band with a maximum peak at about 460 nm and a tail at longer wavelengths [1, 27].

Figure 5.14 shows the normalized EL (pulsed and continuous), PL and CL spectra from SRO films with the same silicon excess (4 at.%). The CL spectrum can be well fitted by four Gaussian components at about 446, 479, 523, and 626 nm. These CL peaks correlate with those peaks at 450, 500, 550, and 640 nm observed in EL measurements.

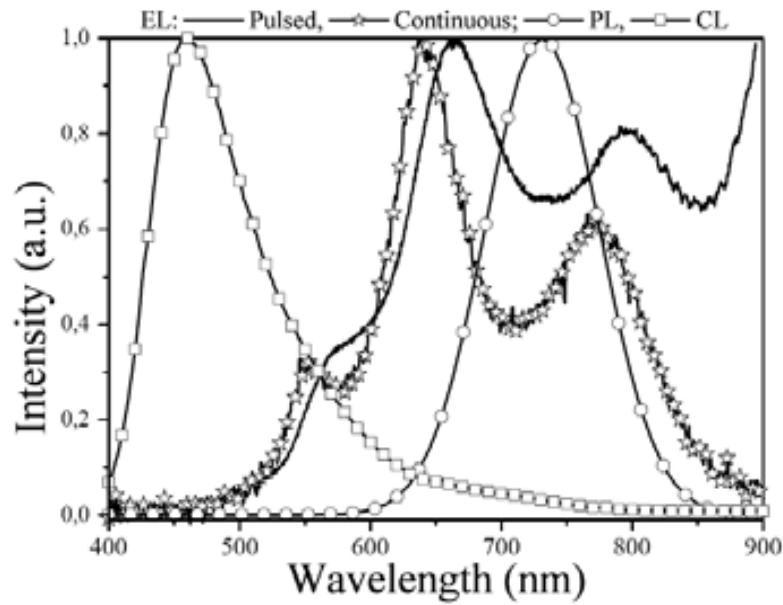


Figure 5.14. Pulsed and continuous EL, PL and CL spectra measured from SRO film with 4 at.% at 25 V driving gate voltage, excited with 250 nm and excited with 5 keV acceleration voltage and 0.3 mA current [1], respectively.

It is well known that such radiative WOB, NOV, and NBOHC defects mentioned before emit at about 415, 455, and 600 nm, respectively [1, 5, 27-34]. Since CL measurements have shown luminescent peaks close to those wavelengths, such defects could be inside the SRO films, which are only excited with carriers of high energy or with the applying of high current (10^{-3} A) in MOS-like structures as reported in this work.

On the other hand, the luminescence at 520 nm has been associated with E'_8 defects [30, 31, 35, 36], one of the at least four different E' centers [37]. The E'_8 center comprises an unpaired spin delocalized over five silicon atoms and suggest the presence

of very small Si-nps in the films [36]. This 520 nm luminescence peak has been observed as in CL as EL measurements in the SRO films from this work.

As E' centers in SiO_x (x<2) films disappear after a thermal annealing at above of 600 °C [35] and given that the SRO films from this work have been thermally annealed at 1100° C, E' centers should not exist. Then, E' centers in the SRO film could be created during the charge injection toward the SRO film during the electrical stress (pulsed and continuous).

From the electrical characterization, it was mentioned that E' centers generation could be activated by the breaking of Si-Si bonds when charges are flowing through the Si-cl, creating some of the types of E' center including the E'_δ center. Moreover, from the electrical characterization, a current dropping was observed.

Figure 5.15 shows the current at RB and the normalized EL intensity (pulsed and continuous) as a function of the gate voltage applied to the MOS-like structure with SRO film of 4 at.% of Si-excess. As the voltage increases from zero, the current through the SRO film increases and at a certain gate voltage where the current reaches a value of 1 mA, the emission (both pulsed and continuous) is observed. Nevertheless, after a gate voltage $V_G = V_{drop}$ is reached, the current drops switching-off the EL.

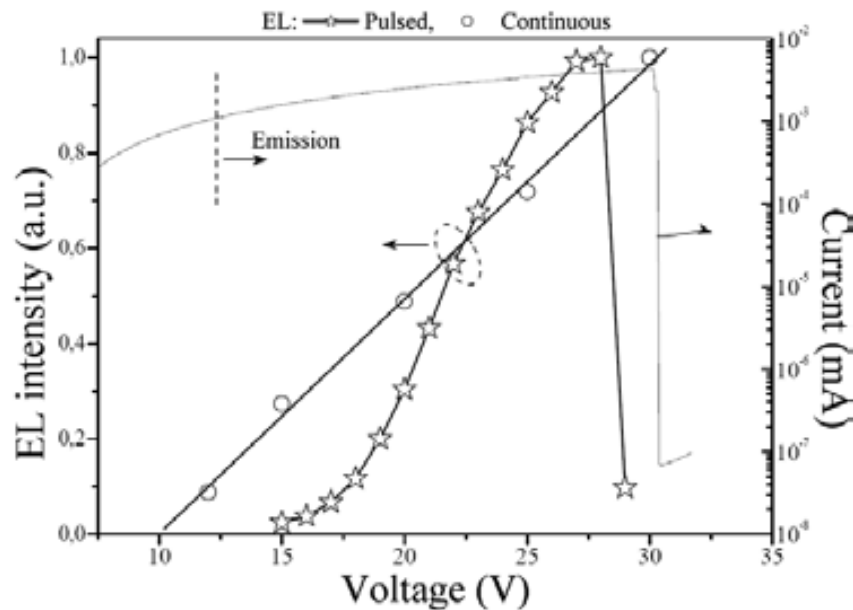


Figure 5.15. Correlation between current and EL (pulsed and continuous) in MOS-like devices with SRO films (4 at.% of Si-excess) as the active layer.

The emission mechanism could be explained using the band energy diagram showed in figure 5.16.

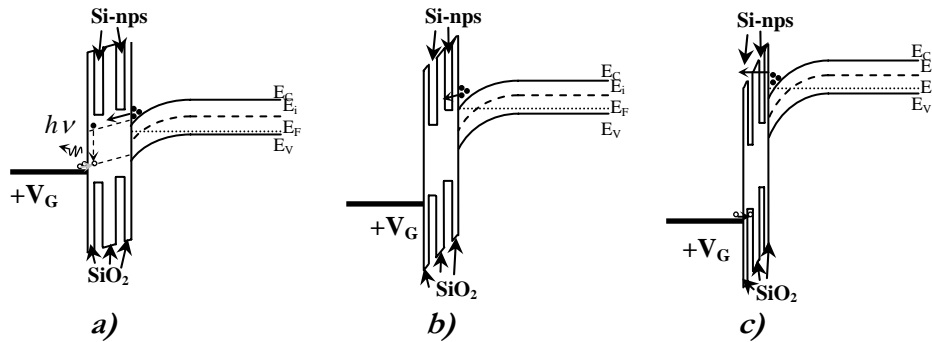


Figure 5.16. Band energy diagram of the MOS-like structure at reverse bias and gate voltages of a) $V_G < V_{drop}$, b) $V_G > V_{drop}$, and c) $V_G \gg V_{drop}$.

As mentioned before, a trap level created by the Si-cls is assumed to be placed near the mid-gap of SRO film. When a positive gate voltage (RB) is applied to the MOS-like structure, electrons are attracted to the silicon surface creating an inverted layer. As shown in figure 5.16(a), electrons from this inverted layer and holes from the polysilicon gate are injected toward the Poly/SRO and SRO/Si interfaces through traps (Si-cls), respectively. However, since the mobility of electrons in silica is higher than the mobility of holes, electrons reach the Poly/SRO interface faster and then recombine themselves emitting light. As the gate voltage is raised, the current and the EL intensity increase. Since it is assumed that the charges do not flow uniformly through the whole capacitor area, instead, it passes through narrow conductive paths within the oxide, the light is observed as shining spots on the surface of the MOS structure.

When the gate voltage becomes higher, charges which are flowing through the Si-cls break off some of their Si-Si bonds (E' center), annihilating the conduction paths and leading to current drops. Then, flow of charges toward the SRO film is not obtained and as a consequence, the EL intensity is switched-off.

Once the current dropping occurs (at V_{drop}), the SRO conductivity changes. Conductive paths are now available through more stable Si-nps and higher voltages are needed to inject charges toward the SRO film. Then, when a gate voltage higher than V_{drop} is applied to the MOS-like structure, electrons from the inverted layer are injected to the SRO film where they can get trapped into the Si-nps, as shown in figure 5.16(b) and

demonstrated by the V_{FB} shifting in the C-V curves. As the gate voltage increases even more, electrons tunnel directly toward the polysilicon gate from the inverted layer as F-N conduction and holes which are injected from the polysilicon gate toward the Si-substrate are trapped in Si-nps (see figure 5.16(c)), as demonstrated by the V_{FB} shifting in the C-V curves (see figure 4.12, page 62).

The EL peak observed at ~ 1000 nm can be explained in a similar way: When a negative gate voltage (FB) is applied to the MOS-like structure, holes are attracted to the silicon surface creating an accumulation layer. As shown in figure 5.17(a), holes from this accumulated layer and electrons from the polysilicon gate are injected toward the Poly/SRO and SRO/Si interfaces through traps, respectively. However, as mentioned before, since the mobility of electrons in silica is higher than the mobility of holes, electrons reach the SRO/Si interface faster and then recombine themselves emitting light at the Si-substrate surface. As the gate voltage becomes more negative, the EL increases and at a certain voltage $V_G = V_{drop}$ the current is quenched. Then, conductive paths are then available through more stable Si-nps and higher voltages are needed to inject charges toward the SRO film. When a gate voltage $V_G > V_{drop}$ is applied to the MOS-like structure, electrons from the polysilicon gate are injected to the SRO film where they can get trapped into the Si-nps, as shown in figure 5.17(b). As the gate voltage becomes even more negative, electrons tunnel directly toward the Si-substrate from the polysilicon gate as F-N conduction and holes which are injected from the Si-substrate toward the polysilicon gate are trapped in Si-nps, see figure 5.17(c).

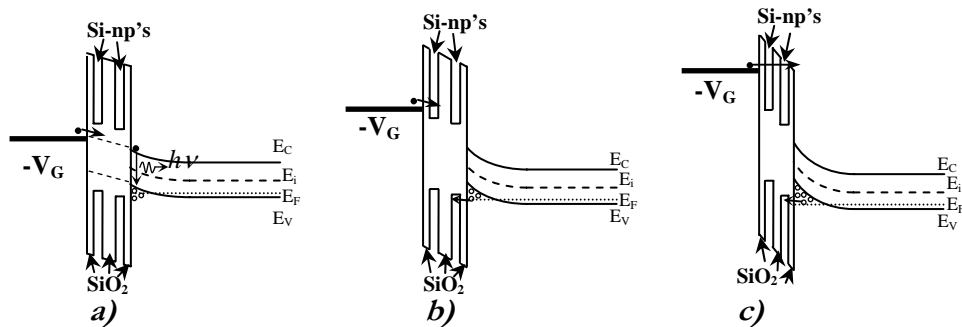


Figure 5.17. Band energy diagram of the MOS-like structure at forward bias and gate voltages of a)

$|V_G| < V_{drop}$, b) $|V_G| > V_{drop}$, and c) $|V_G| \gg V_{drop}$.

As observed, the red emission in EL (774 nm) and PL (734 nm) are not placed at the same energy. This fact could be due to the optical properties of the poly/SRO film stack

[26]. Therefore, both red EL and PL could be due to the same origin, where the interaction between defects and Si-nps are taken into account, as reported before. However, studies of EL measurements on devices with a transparent gate material which permits the light to be observed without disturb the real luminescence peaks is necessary.

Above, we have been assuming that the charges do not flow uniformly through the whole capacitor area, instead, it passes through narrow conductive paths within the oxide, therefore light is observed as shining spots. Moreover, these conductive paths are annihilated with electrical stress. Nevertheless, if multiple conductive paths are available in the SRO film, the SRO resistance is so small that a current dropping is not observed, such as in the 24 nm thick SRO film with the largest gate area ($9.604 \times 10^{-3} \text{ cm}^2$, figure 4.14(a), page 64). This behaviour was also observed in the 53 nm thick SRO film as observed in figure 5.18(a). High current conduction is reached at low voltages and no current drop is observed. EL measurements under positive pulsed stimulation in these devices are shown in figure 5.18(b). For a gate voltage of 26 V, a broad EL spectra with maximum peaks is observed, meanwhile for higher gate voltages, $V_G = 45$ and 48, the EL intensity is increased in almost 4 times and a more defined peak at $\sim 720 \text{ nm}$ is observed.

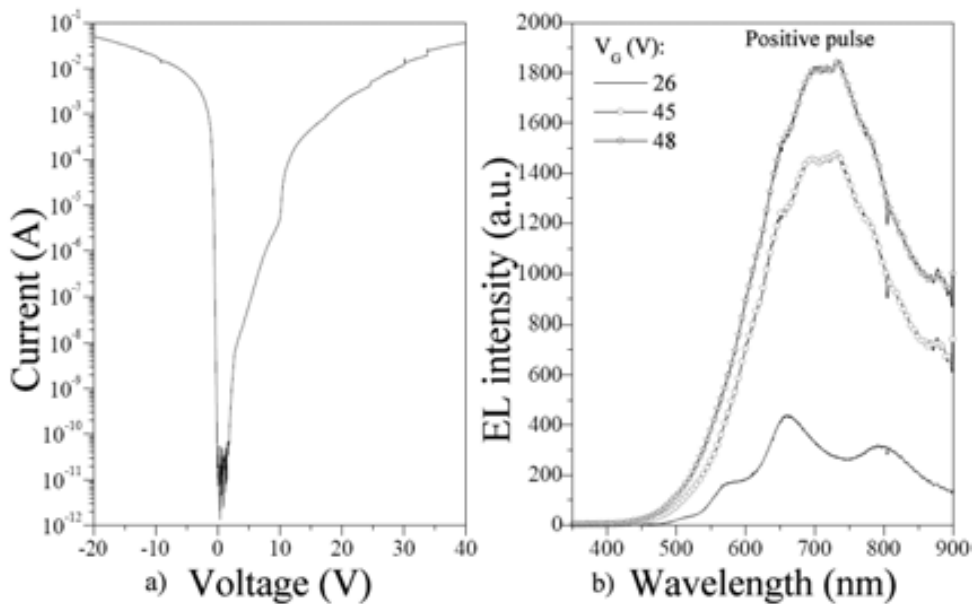


Figure 5.18. a) I - V curve from MOS-like devices with 53 nm thick SRO film and 4 at.% of Si-excess and b) EL spectra measured with positive pulsed stimulation.

Images of the MOS-like structure without bias and biased with 26 V are shown in figure 5.19(a) and 5.19(b), respectively, where multiple shining spots are clearly observed.

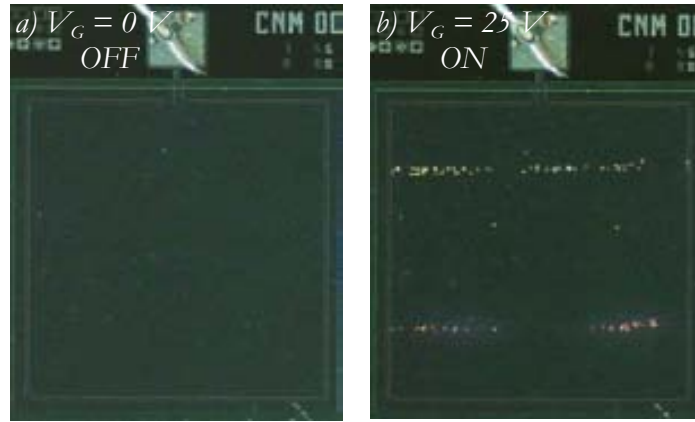


Figure 5.19. Image of the MOS-like devices with 53 nm thick SRO film and 4 at.% of Si-excess a) without bias (OFF) and b) biased with 25V (ON).

When high voltages are applied to the MOS-like structures, electrons from the Si-substrate (polysilicon gate) and holes from the polysilicon gate (Si-substrate) are injected to the SRO film through Si-nps, Si-cls and defects, these charges recombine and light is emitted showing a broad spectrum. Moreover, the maximum EL peak is quite similar to the maximum PL peak, as shown in figure 5.20. This indicates that the red EL and red PL emission are due to the same effect.

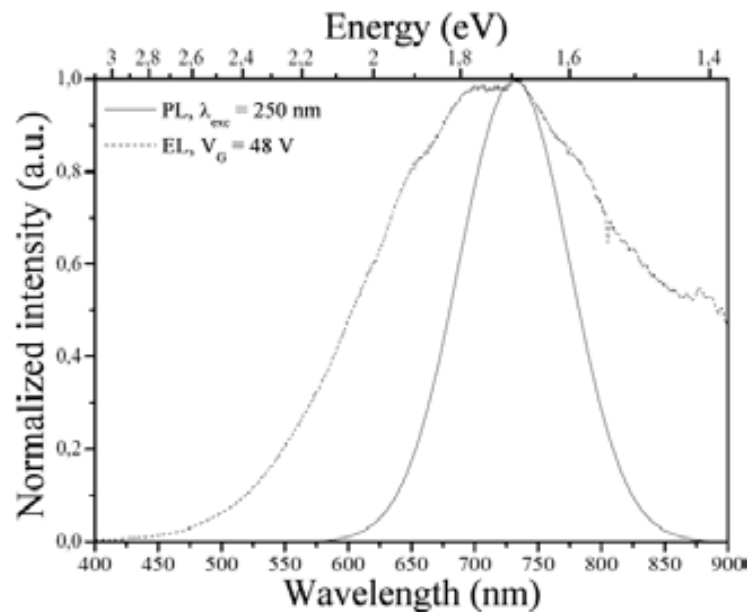


Figure 5.20. EL and PL spectra measured at a gate voltage of 48 V and excited with 250 nm, respectively.

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Chapter 6

Conclusion

The composition, structure and optical properties of SRO and SI-SRO films obtained by LPCVD have been studied. Ellipsometry, FTIR, XPS, EFTEM, as well as PL techniques were used to obtain a basic characterization of the material. Ellipsometry measurements and XPS studies on SRO films from this work showed the presence of Si excess (Si > 33.3%) in the films. Nevertheless, the compositional analysis obtained from FTIR did not exhibit vibration bands related to impurities such as H or N neither before nor after thermal annealing. Although, XPS measurements showed the presence of N in the films, its profile was relatively low, about 0.8 at.%. From FTIR spectra, it was deduced that a phase separation took place when the SRO films were thermally annealed due to a displacement of the TO_3 band toward higher frequencies ($\sim 1088 \text{ cm}^{-1}$ for SiO_2), and then corroborated by EFTEM images.

EFTEM analysis showed Si-nanoparticles in films with silicon excess higher than 5.1 at.%, which were thermally annealed at 1100°C . The average size of the Si-nps varied according to the silicon excess, being 2.7 nm for the SRO film with 5.1 at.% and it increased to 4.1 nm for 12.7 at.% of silicon excess.

A strong PL was observed in films with 4 and 5.1 at.% of silicon excess. However, the photoluminescence was strongly reduced when the silicon excess was about 12.7 at.%, where most of the Si-nps have an average size of ~ 4.1 nm. A redshift only took place when the silicon excess was increased from 4 to 5.1 at.%, but no redshift was observed when the silicon excess was further increased to 12.7 at. %. A part from that, SRO films

with Si-nps of different sizes emitted at the same energy, contrary to the QCE. As a result, the PL origin was related to defects surrounding the Si-nps.

The mechanism of emission was explained as follows: The e-h pairs are generated inside of the Si-nps. Then, electrons are excited to the defects, and the emission takes place when electrons in the localized state return to the positive Si-nps, or the ground state. When the size of the Si-nps is small, the band gap energy is large, and then the energy difference between the localized state and the ground state is big enough to produce the emission. This is similar to the donor-acceptor mechanism of emission in semiconductors. As their size increases, the energy difference is reduced, and eventually, when the size exceeds an optimum size, the energy of the localized state will be such that electrons decay will not produce emission, and then PL will not be observed. It was found that the optimum size of Si-nps required in which a maximum PL intensity is observed for these experiments is about 2.6 nm.

The density of Si-nps is the main effect affecting the PL intensity on the SRO and SI-SRO films. Moreover, the silicon implantation increased the density of Si-nps producing a more intense photoluminescence. The strongest photoluminescence was observed in the SI-SRO film which is annealed at 1100° C for 60 minutes and having Si-nps with 2.6 nm in size.

Metal–oxide–semiconductor (MOS) structures using the SRO films with 4 and 2.2 at.% of Si-excess as the dielectric layer were fabricated in order to study their electrical and electroluminescent properties. For the SRO films with low Si-excess, electrical properties similar to the SiO₂ films were obtained. Nevertheless, two main electrical behaviors were observed in the MOS-like structures with higher Si-excess (4 at.%): first, a C-V and I-V anomalous behavior where the current and capacitance drops, and the second one, the Coulomb blockade effects (CBE), where a staircase current was obtained.

For the first case, the electrical properties of annealed SRO films were studied and analyzed as a function of the gate area. A clear correlation between a dropping in capacitance and current of SRO films was observed. The capacitance and current dropping were the result of an electrical anneal, produced by the annihilation of

conductive paths. This anneal was related to the creation of E' defects in the SRO layer.

The current conduction mechanism through the SRO film was also analyzed. The high current observed in low voltages was related to trap assisted tunnelling, while for high voltages Fowler–Nordheim tunnelling were found. After the current dropping, no current conduction was observed at low voltages, whereas F-N conduction was observed at high electric fields.

In the second behaviour, current fluctuations and a clear staircase current at room temperature were observed in different structures and related to Coulomb blockade effect produced by charge trapped in Si-nps. Si-nps with ~1 nm in size were estimated from these electrical results (stair width). The variation in the width of the plateaus was ascribed to the size and separation of Si-nps.

Electro-optical studies were done under pulsed and continuous stimulation. Luminescent spots (seen with the naked eye) on the MOS-like devices with SRO films (Si-excess of 4 at.%) appeared when the devices were reversely biased. A broad electroluminescent emission spectrum (400-900 nm) was measured. Fitting the EL spectra, peaks at about 450, 500, 550, 640, and 750 nm were obtained and related to defects such as weak oxygen bond (WOB), neutral oxygen vacancy (NOV, $O_3 \equiv Si-Si \equiv O_3$), E'₈ defect ($Si \uparrow Si \equiv Si$), non-bridging hole center (NBOHC, $(O_3 \equiv Si-O \bullet)$), and defects at the SiO₂/Si-nps interface, respectively.

Although photoluminescence in the blue/green region of the visible spectra was not observed in this SRO films, catholuminescence peaks at the same wavelengths that EL peaks have been observed for SRO films with similar Si-excess, indicating the existence of such defects. A maximum and then switching-off of the EL intensity was observed. This effect was related with the current drop, which was produced by the annihilation of conductive paths (E' centers) during the charge injection in the SRO films.

Nevertheless, when multiple conductive paths were available in the SRO film, no current dropping was observed, such as in the 24 nm thick SRO film with the largest gate area ($9.604 \times 10^{-3} \text{ cm}^2$). This effect is ascribed to that the multiple conductive paths produce that the SRO resistance is quite small. In these devices, multiple shining spots

were clearly observed. Moreover, it was found that the maximum EL peak is quite similar to the maximum PL peak, indicating that the red EL and red PL emission are due to the same effect.

Further work

Studies of EL measurements on devices with a transparent gate material which permits the light be observed without disturbing the real luminescence peaks is necessary. Electrical and opto-electronic studies of MOS-like structures with SRO films containing higher Si-excess. MOS-like structures but with N-type silicon wafers should be studied in order to improve the electron injection inside the SRO film.

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