Nasir, Usman and Costabeber, Alessando and Wheeler, Patrick and Rivera, Marco (2017) A new AC/AC power converter. In: Southern Power Electronics Conference (SPEC 2017), 4-7 Dec 2017, Puerto Varas, Chile.

A New AC/AC Power Converter

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***Abstract*— The Future Electrical Network will be based on the integration of different renewable energy sources. In this regard, modular bidirectional power converter architectures will get special attention. Galvanic isolation in such power converter architectures plays a vital role in confining faults. This paper presents a new AC/AC converter concept suitable for Solid State Transformer (SST) applications. The basic operation of the topology is first presented, followed by the development of suitable modulation, commutation and protection methods. The proposed idea is validated in simulation with PLECS.**

Keywords—solid state transformer; isolated AC/AC; four-step commutation; isolated matrix converters; cycloconverters

I. INTRODUCTION

Classical matrix converters (MC) offer a single stage high power density conversion solution [1] by avoiding the intermediate DC link stage. As the semiconductor devices directly connect the input to the output of the converter, it is not feasible to employ classical MC in applications requiring galvanic isolation. An example of a system requiring galvanic isolation can be AC transmission or distribution grids [2]. Although line frequency transformers can provide the isolation, they are expensive and bulky in size [3]. However, increasing the operating frequency of the transformer can considerably reduce the cost and size. The operating frequency of the transformer can be increased by utilizing a power converter which modulates the line frequency to a medium or high frequency (MF/HF) waveform, suitable for a MF/HF transformer, and another power converter unfolds the MF/HF waveforms back to low frequency. In literature, this concept has been reported as solid-state transformer (SST) [4, 5] and is illustrated in Fig. 1. SST topologies based on bidirectional switches can provide additional benefits such as reduced footprint and weight.

A single phase to single phase MC based SST, proposed in [6], has limited applications due to the single phase nature of the topology, and to the fact that input and output frequencies must be the same, thus preventing the use of this topology in the interconnection of asynchronous grids. To overcome this problem, a new modular and flexible MC based SST topology has been proposed in [7] and an appropriate modulation, i.e. Venturini Modulation (VM), and commutation techniques were developed.

This paper proposes a new topology based on a different arrangement of bidirectional H bridges, shown in Fig. 2. The figure shows the three-phase to three-phase embodiment, made by simply repeating the three-phase to single-phase version for each phase. The potential advantages of the proposed topology in SST applications are the lower number of transformers as well as the reduced semiconductor device count meanwhile keeping the modularity intact. Therefore, the proposed SST topology of Fig. 2 offers some additional benefits over the SST topology of [6].

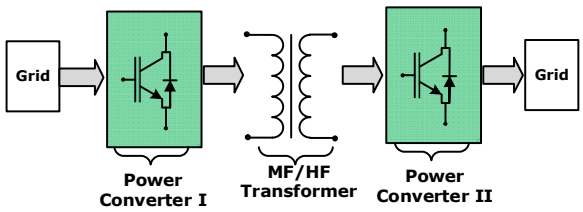


Fig. 1 A general architecture of a Solid State Transformer (SST)

Section II focusses on the operating principle of the proposed SST topology by analyzing and developing an appropriate scalar modulation method. Furthermore, it briefly discusses the commutation technique which is required for a safe operation of the bidirectional H bridges in the converter and also it presents an open circuit fault protection method. Section III presents the key simulation results from PLECS, confirming the correct operation of the converter.

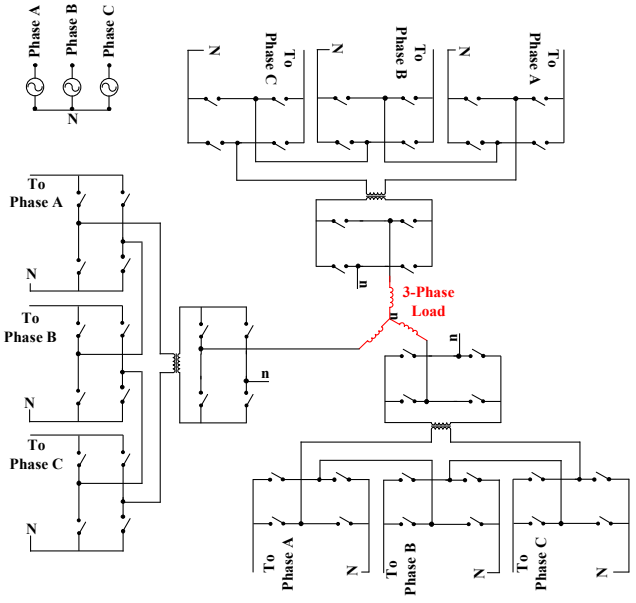


Fig. 2 A new 3-phase to 3-phase isolated AC/AC matrix converter for solid-state transformer applications

II. Converter Operation And Analysis

The three-phase to single-phase version of the proposed SST topology, reported in Fig. 3, is comprised of 4 bidirectional H bridges and one MF/HF isolation unit. Three bridges are at the primary side of the transformer while only one is at the secondary side. Each bridge achieves a four-quadrant operation, with respect to voltage polarity and current direction, at the input and output side. The three cascaded input bridges feed the MF/HF transformer which then connects to the output bridge.

In order to develop a modulation technique for this topology, it is important to briefly discuss the operation of an Indirect Matrix Converter (IMC). In the IMC, the rectifier stage generates a virtual DC voltage which is then modulated, by inverter stage, to generate the required frequency. It is important to mention that the virtual DC voltage is actually the envelop of the three phase input voltages, and therefore at any time instant t the input voltage with the maximum amplitude is selected [8].

A. Modulation Technique

In order to apply a suitable modulation method, the proposed topology can be represented in terms of switching functions which relate output voltage to input voltages. From Fig. 3, the individual bridge voltages at the primary side of the transformer can be represented in (1) – (3). Due to the cascade connection of the three input bridges, the voltage of the transformer can be represented as (4);

$$V_{OA} = V_A\left[S_{A1}S_{A2} - \bar{S}_{A1}\bar{S}_{A2}\right] \tag{1}$$

$$V_{OB} = V_B\left[S_{B1}S_{B2} - \bar{S}_{B1}\bar{S}_{B2}\right] \tag{2}$$

$$V_{OC} = V_C\left[S_{C1}S_{C2} - \bar{S}_{C1}\bar{S}_{C2}\right] \tag{3}$$

$$V_T = \sum_{k=A,B,C} V_k\left[S_{k1}S_{k2} - \bar{S}_{k1}\bar{S}_{k2}\right] \tag{4}$$

In order to obtain a 50% duty cycle waveform at the transformer, the input bridges moves between the states (5) and (6) with a frequency suitable for the operation of the MF/HF transformer.

$$V_T = \begin{cases} \textit{Voltage} & \textit{State} & \textit{Condition} \\ V_A & \left\langle \begin{array}{l} S_{A1}=S_{A2}=1, \bar{S}_{A1}=\bar{S}_{A2}=0 \\ \bar{S}_{B1}=S_{B1}=0, S_{B2}=\bar{S}_{B2}=1 \\ \bar{S}_{C1}=S_{C1}=0, S_{C2}=\bar{S}_{C2}=1 \end{array} \right\rangle & \begin{array}{l} V_A > V_B \\ V_A > V_C \end{array} \\ V_B & \left\langle \begin{array}{l} \bar{S}_{A1}=S_{A1}=0, S_{A2}=\bar{S}_{A2}=1 \\ S_{B1}=S_{B2}=1, \bar{S}_{B1}=\bar{S}_{B2}=0 \\ \bar{S}_{C1}=S_{C1}=0, S_{C2}=\bar{S}_{C2}=1 \end{array} \right\rangle & \begin{array}{l} V_B > V_A, \\ V_B > V_C \end{array} \\ V_C & \left\langle \begin{array}{l} \bar{S}_{A1}=S_{A1}=0, S_{A2}=\bar{S}_{A2}=1 \\ \bar{S}_{B1}=S_{B1}=0, S_{B2}=\bar{S}_{B2}=1 \\ S_{C1}=S_{C2}=1, \bar{S}_{C1}=\bar{S}_{C2}=0 \end{array} \right\rangle & \begin{array}{l} V_C > V_A, \\ V_C > V_B \end{array} \end{cases} \tag{5}$$

It is worth mentioning that the transformer voltage is a "virtual square wave" as it is a function of the square wave of the switching function and of the virtual DC wave as given in (7). Therefore, it contains additional harmonics which must be analyzed to design the complete modulation of the converter.

$$V_T = \begin{cases} \textit{Voltage} & \textit{State} & \textit{Condition} \\ -V_A & \left\langle \begin{array}{l} S_{A1}=S_{A2}=0, \bar{S}_{A1}=\bar{S}_{A2}=1 \\ \bar{S}_{B1}=S_{B1}=0, S_{B2}=\bar{S}_{B2}=1 \\ \bar{S}_{C1}=S_{C1}=0, S_{C2}=\bar{S}_{C2}=1 \end{array} \right\rangle & \begin{array}{l} V_A > V_B \\ V_A > V_C \end{array} \\ -V_B & \left\langle \begin{array}{l} \bar{S}_{A1}=S_{A1}=0, S_{A2}=\bar{S}_{A2}=1 \\ S_{B1}=S_{B2}=0, \bar{S}_{B1}=\bar{S}_{B2}=1 \\ \bar{S}_{C1}=S_{C1}=0, S_{C2}=\bar{S}_{C2}=1 \end{array} \right\rangle & \begin{array}{l} V_B > V_A, \\ V_B > V_C \end{array} \\ -V_C & \left\langle \begin{array}{l} \bar{S}_{A1}=S_{A1}=0, S_{A2}=\bar{S}_{A2}=1 \\ \bar{S}_{B1}=S_{B1}=0, S_{B2}=\bar{S}_{B2}=1 \\ S_{C1}=S_{C2}=0, \bar{S}_{C1}=\bar{S}_{C2}=1 \end{array} \right\rangle & \begin{array}{l} V_C > V_A, \\ V_C > V_B \end{array} \end{cases} \tag{6}$$

$$V_T(t) = s(t).V'_{vir\_dc}(t) \tag{7}$$

The Fourier series of a square wave and a virtual DC wave can be expressed using (8) and (9) respectively:

$$s(t) = \frac{4}{\pi}\sum_{m=1,3,5\ldots}^{\infty}\frac{\sin(m\omega_s t)}{m} \tag{8}$$

$$V'_{vir\_dc}(t) = a_o + \sum_{n=1}^{\infty} a_n\cos(3n\omega_i t) + \sum_{n=1}^{\infty} b_n\sin(3n\omega_i t) \tag{9}$$

The Fourier series of the virtual DC wave in (10) can be calculated by considering Fig. 4. During the interval from $\pi/6$ to $5\pi/6$ the input phase 'A' will be selected as it has the highest value than the remaining phases i.e. $V_A > V_B$ and $V_A > V_C$. Note that when phase 'A' is selected, the states of (5) and (6) bypass the remaining phases without disturbing the load current. Therefore, calculating the Fourier series coefficients, such as DC coefficient in (10), the virtual DC wave can be expressed as seen in (11).

$$a_0 = \frac{3\omega_i}{2\pi}\int_{\pi/6\omega_i}^{5\pi/6\omega_i}\sin(\omega_i t).dt \tag{10}$$

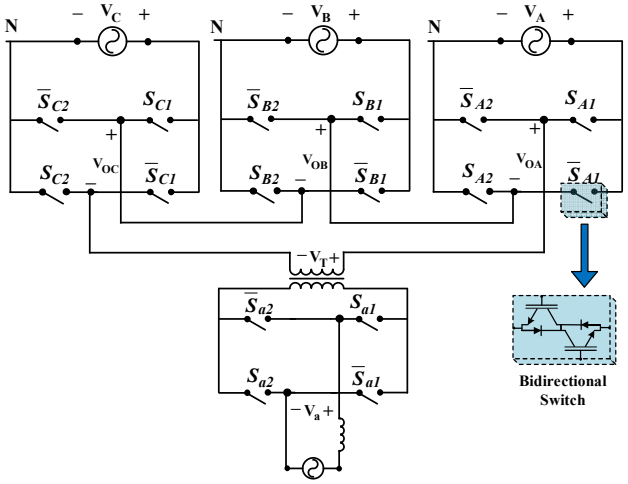


Fig. 3 The proposed isolated AC/AC topology - three-phase to single-phase version

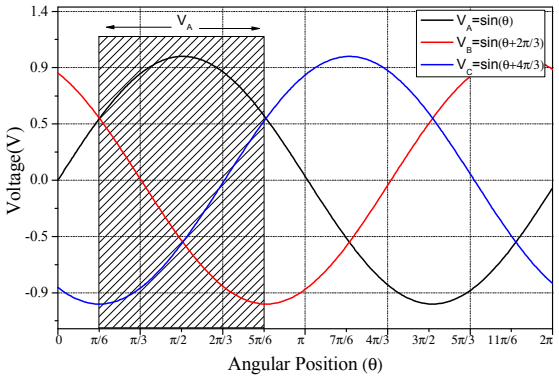


Fig. 4 Illustration of the interval during which input phase 'A' will be selected. Voltage in p.u. where the base voltage is V_{base}=220V.

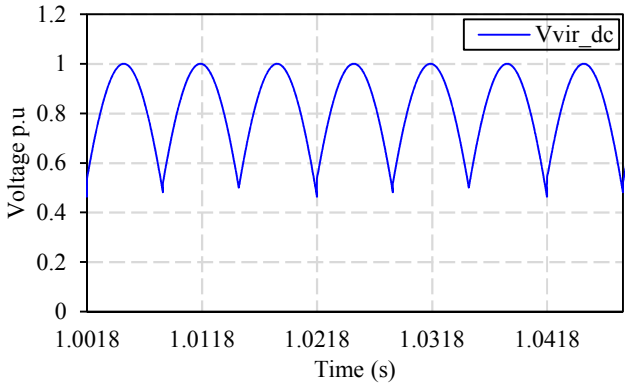


Fig. 5 The virtual DC voltage wave. Voltage in p.u. where the base voltage is V_{base}=220V.

$$V'_{vir\_dc}(t)=\frac{3\sqrt{3}}{\pi}\left[\begin{array}{l}\frac{1}{2}+\sum_{n=2,4,6..}^{\infty}\frac{(-1)^{\frac{n}{2}}}{(1-9n^2)}\cos(3n\omega_i t)+\\ \sum_{p=1,3,5...}^{\infty}\frac{(-1)^{\frac{2p-3-(-1)^p}{4}}}{(1-9p^2)}\sin(3p\omega_i t)\end{array}\right] \quad (11)$$

The FFT spectrum of the virtual DC wave of Fig. 5, given in (11), has been shown in Fig. 6. The Fourier series of the transformer voltage can be found by substituting (8) and (11) in (7) which will form (12);

$$V_T(t)=\frac{12\sqrt{3}}{\pi^2}\left[\sum_{m=1,3,5...}^{\infty}\frac{\sin(m\omega_s t)}{m}\right]\left[\begin{array}{l}\frac{1}{2}+\sum_{n=2,4,6..}^{\infty}\frac{(-1)^{\frac{n}{2}}}{(1-9n^2)}\cos(3n\omega_i t)+\\ \sum_{p=1,3,5...}^{\infty}\frac{(-1)^{\frac{2p-3-(-1)^p}{4}}}{(1-9p^2)}\sin(3p\omega_i t)\end{array}\right] \quad (12)$$

It is key to note from Fig. 7 that the input bridges are applying a 50% duty virtual DC enveloped waveform at the transformer. Since the voltage at the transformer is a virtual square wave, with the FFT spectrum of Fig. 8, the transformer design must consider all the harmonic components present in the transformer voltage. Designing the transformer at the switching frequency, by neglecting the harmonic components, can cause core saturation. Hence, the transformer core area must be calculated considering all the harmonic components in the transformer voltage as given in (13).

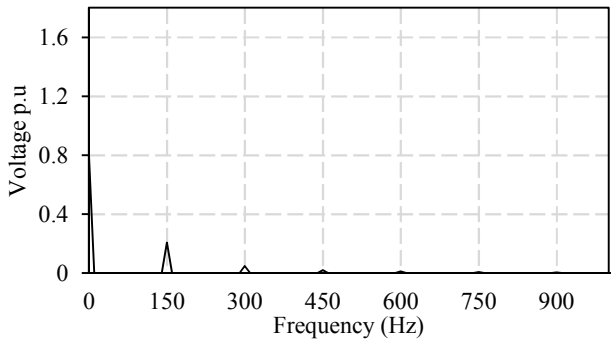


Fig. 6 Fourier spectrum (FFT) of the virtual DC wave with fundamental, 2nd and 3rd harmonics appearing at 150 Hz, 300 Hz and 450 Hz respectively. p.u. base voltage is V_{base}=220V.

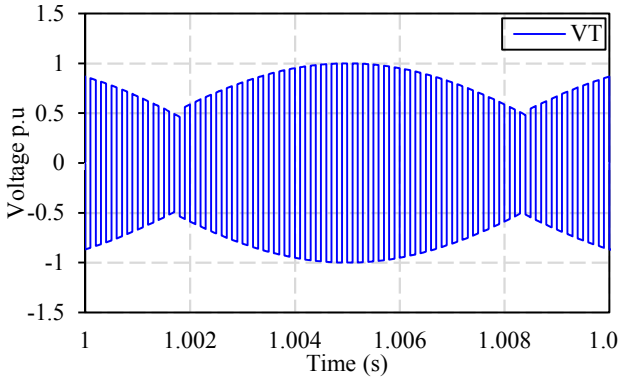


Fig. 7 The 50% duty cycle voltage virtual DC enveloped wave at MF/HF transformer with switching component at 5 kHz. Voltage in p.u. where the base voltage is V_{base}=220V.

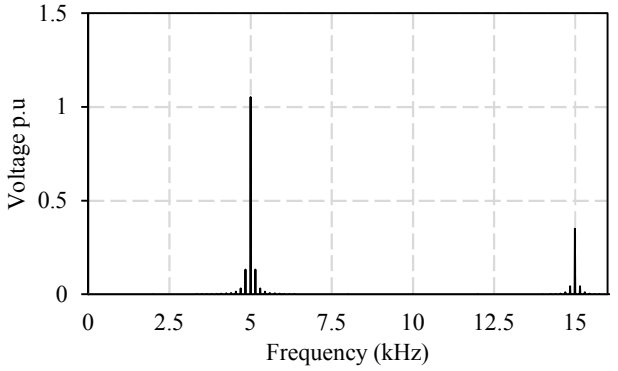


Fig. 8 Fourier spectrum (FFT) of the transformer voltage with fundamental of 1.05 p.u magnitude appearing at 5 kHz with side band of 0.13 p.u appearing at 4.850 kHz and 5.150 kHz. p.u. base voltage is V_{base}=220V.

$$A_{\max}=\frac{1}{N.B_{\max}}\int V_T(t).dt \quad (13)$$

Where N is the number of turns, $B_{\max}$ is the maximum magnetic flux density of the material and $A_{\max}$ is the maximum core area required. An active control of the Volt-Second balance across the transformer, such as given in [7], can be added in order to avoid saturation of the core due to undesired DC components

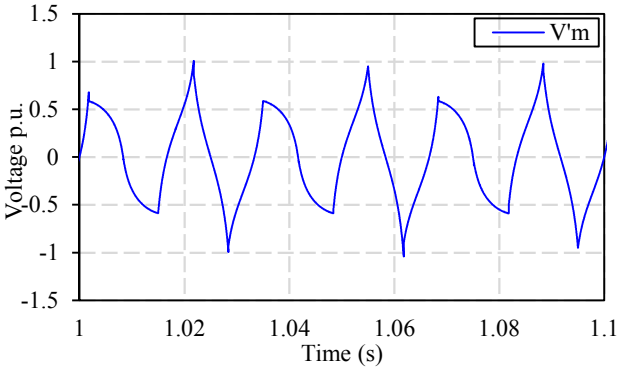


Fig. 9 Adjusted modulating wave for bipolar sine-triangular PWM. Voltage in p.u. where the base voltage is V_{base}=220V.

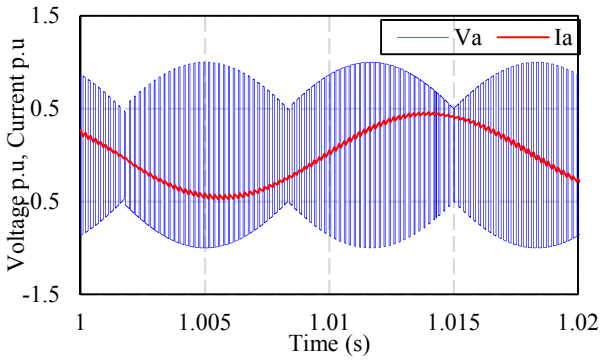


Fig. 10 Output voltage and output current waveforms at 60Hz as a result of bi-polar sine-wave PWM in the proposed isolated AC/AC SST topology. Voltage in p.u. with base voltage V_{base}=220V. Current in p.u. with base current I_{base}= 110A

generated by converter asymmetries – e.g. differences in the turn on/off times of switches, gate driver delays etc. Now, the output voltage can be represented as a function of transformer voltage and the output bridge switches as in (14);

$$V_a = V_T\left[S_{a1}S_{a2} - \bar{S}_{a1}\bar{S}_{a2}\right] \tag{14}$$

Similar to the input side state matrix, given in (5) and (6), an output modulation state matrix can also be defined in a way that it unfolds the 50% duty cycle transformer voltage waveform while implementing a sine-wave modulation. The output modulation matrix, which implements a bi-polar PWM, is defined in (15).

$$V_a = \begin{Bmatrix} \textit{Voltage} & \textit{State} & \textit{Interval} & \textit{When} \\ +V_T & S_{a1}=S_{a2}=1, \bar{S}_{a1}=\bar{S}_{a2}=0 & 0 \;\; to \;\; D & \\ -V_T & S_{a1}=S_{a2}=0, \bar{S}_{a1}=\bar{S}_{a2}=1 & D \;\; to \;\; 0.5 & 0<D<0.5 \\ +V_T & S_{a1}=S_{a2}=1, \bar{S}_{a1}=\bar{S}_{a2}=0 & 0.5 \;\; to \;\; 1 & \\ +V_T & S_{a1}=S_{a2}=1, \bar{S}_{a1}=\bar{S}_{a2}=0 & 0 \;\; to \;\; 0.5 & \\ -V_T & S_{a1}=S_{a2}=0, \bar{S}_{a1}=\bar{S}_{a2}=1 & 0.5 \;\; to \;\; D & 0.5<D<1 \\ +V_T & S_{a1}=S_{a2}=1, \bar{S}_{a1}=\bar{S}_{a2}=0 & D \;\; to \;\; 1 & \end{Bmatrix} \tag{15}$$

The duty cycle D is obtained using classical sine-triangle or sine-sawtooth comparison. As the output bridge unfolds the transformer voltage, the fundamental component of the output voltage can simply be expressed by (16):

$$V_a = V'_m \cdot V'_{vir\_dc} \tag{16}$$

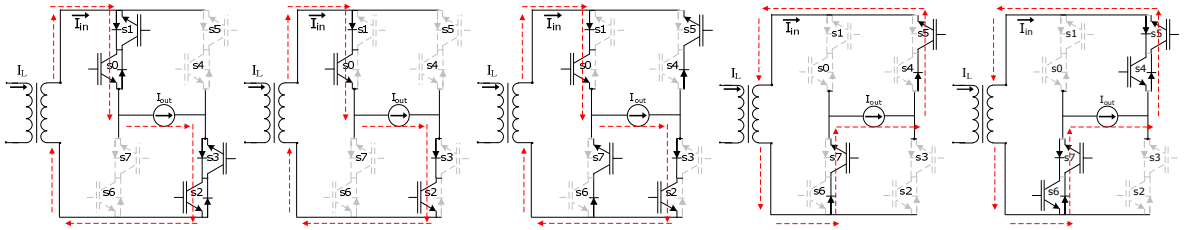
However, the modulating wave needs adjustment to compensate the fact that the virtual DC of (11) contains harmonics and therefore the actual modulating wave can be expressed using (17).

$$V'_m = \frac{V_m}{V'_{vir\_dc}} = \frac{\frac{\pi}{3\sqrt{3}}\sin(\omega_o t)}{\left[\frac{1}{2} + \sum_{n=2,4,6..}^{\infty} \frac{(-1)^{\frac{n}{2}}}{(1-9n^2)}\cos(3n\omega_i t) + \sum_{p=1,3,5...}^{\infty} \frac{(-1)^{\frac{2p-3-(-1)^p}{4}}}{(1-9p^2)}\sin(3\omega_i t)\right]} \tag{17}$$

B. *Commutation Method*

Due to the absence of the free-wheeling path in a bi-directional switch, a suitable commutation strategy must be developed to achieve successful operation of the power converter. The commutation can either be voltage based or current based.

In the current based commutation, the output current is sensed and based on its direction, the commutation process is initiated whereas in the voltage based commutation the process is initiated based on the sign of the voltage. Each bidirectional H-bridge commutates independently. Note that voltage at the input and current at the output are at low frequency therefore, it is preferable to use voltage based commutation on the input side bridges and current based commutation on the output side bridge. A case of current based commutation of the output bridge is illustrated in Fig. 11. The shown current based commutation process has four steps and during the process, it is assumed that the current direction doesn't change.



(a) state 1 (b) state 2 (c) state 3 (d) state 4 (e) state 5

Fig. 11 4-step current based commutation of output bridge for the case $I_{out}>0$ and Commutation from s0…s3 ON to s4…s7 ON

State 1: The output bridge of the converter is in steady state with s0, s1, s2, s3 turned on. Fig. 11 (a).

State 2: Non-conducting switches s1, s3 can be turned off as I_{out} has a path through the antiparallel diodes. Fig. 11 (b).

State 3: The switches s5, s7 can conduct the current in the direction of I_{out} and can be turned on safely. Fig. 11 (c).

State 4: Since s5, s7 are already on, they can provide a path for I_{out} and the switches s0, s2 can be turned off. Fig. 11 (d).

State 5: For the bridge to reach the new steady state, the switches s4, s6 are turned on. Fig. 11 (e).

It is important to mention that the commutation sequence is designed by utilizing two constraints i.e. voltage source must not short-circuit and current source must not open-circuit. By keeping these constraints in mind, voltage based commutation sequence can also be deduced. In a similar manner, the commutation from active state to a zero state i.e. s0…s3 ON to s2…s7 ON can also be considered.

C. Protection using Clamp Circuit

Although the 4-step commutation sequence presents a safe operation of the converter without open circuiting the current source or short circuiting the voltage source. Practically, it is possible that the measurement of the current direction, gate driver circuit delay, converter asymmetries or control unit malfunction may change the commutation sequence which can interrupt the inductive current path. Depending on the energy present in the inductive load, a voltage spike of corresponding magnitude can pose threat and eventually it can cause permanent damage to the semiconductor devices. Therefore, an overvoltage clamp circuit, which in case of open circuit fault, will provide an alternative path to dissipate the load energy has been designed as shown in Fig. 12. This clamp circuit improves the overall reliability of the proposed topology. The clamp circuit must be sized carefully such that it accommodates the peak inductive load energy without creating dangerous over voltages. Therefore, the load energy can be represented by (18).

$$E_{load} = \frac{1}{2} L I_{\max}^{\ 2} \tag{18}$$

Where E_{load} is the load energy, L is the load inductance and $I_{\max}$ is the maximum load current. The change in the energy of the clamp capacitor from its initial to final voltage is given in (19).

$$E_{clamp} = \frac{1}{2} C (V_{final}^{\ 2} - V_{initial}^{\ 2}) \tag{19}$$

$$C = \frac{L I_{\max}^{\ 2}}{V_{final}^{\ 2} - V_{initial}^{\ 2}} \tag{20}$$

During the fault condition, the load energy will be clamped i.e. $E_{load} = E_{clamp}$ therefore the size of the capacitor can be calculated by (20). Note that the resistor sizing can be done based on the application as it will define the speed of energy dissipation in the clamp circuit. V_{final} is the final voltage of the capacitor and this value must be kept below the voltage rating of the semiconductor devices.

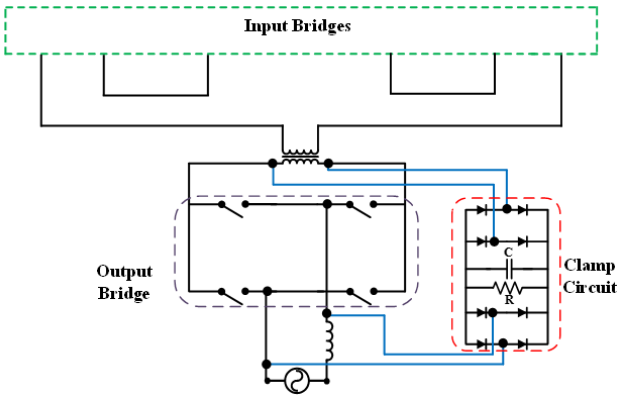


Fig. 12 Over voltage protection clamp circuit for the proposed isolated AC/AC SST topology

III. Simulation Results

A time domain simulation has been done in PLECS Toolbox which validates the theoretical modulation concept developed in the previous section. The following simulation parameters have been used.

TABLE I. Simulation Parameters

Parameter		Symbol	Value
Input voltage		V_{in}	220V AC (peak)
Input frequency		f_{in}	50 Hz
Output frequency		f_o	60 Hz
Switching frequency		f_{sw}	5kHz
Output Load	Resistor	R	1.9 Ω
	Inductor	L	1 mH

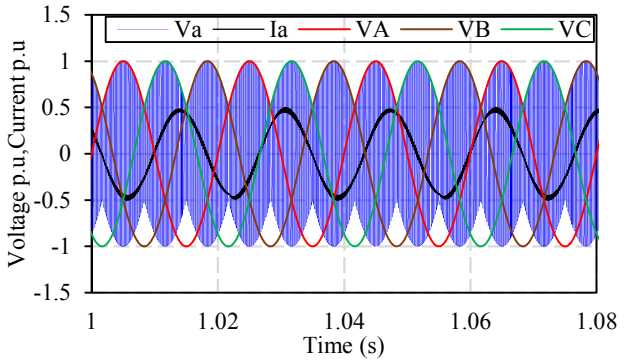


Fig. 13 Input and output voltages and current with fi=50Hz and fo=60Hz in the proposed isolated AC/AC SST topology. Voltage in p.u. with base voltage Vbase=220V. Current in p.u. with base current Ibase= 110A

The proposed SST topology has been compared with the topology of [7] in Table II and both topologies use the input bridges to generate a 50% duty ratio MF/HF voltage at the transformer which is then modulated by the output bridge(s). It can be noted that the proposed topology uses a simpler modulation method than that of [7] while offering a reduced number of switches. The traditional MC consisting of 18 semiconductor devices will have the minimum volume in comparison to the other two but it doesn't provide galvanic isolation whereas the topology of [7] provides galvanic isolation but this comes at the cost of high volume due to increased number of semiconductor devices. However, the proposed

topology is assumed to be smaller in volume than [7] due to the reduction in number of devices.

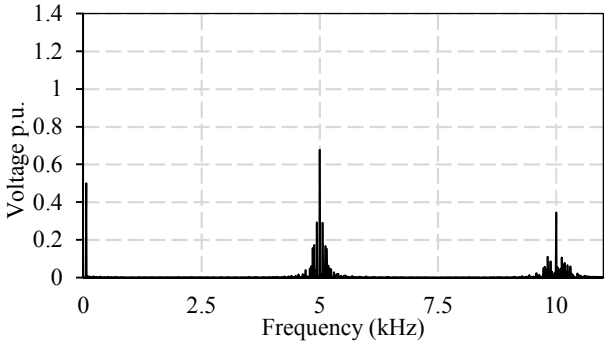


Fig. 14 Fourrier spectrum (FFT) of the output voltage as a result of sine-wave PWM with fundamental appearing at 60Hz while switching component appearing at 5 kHz. Voltage in p.u. with base voltage V_{base}=220V

In order to highlight the operation of the clamp circuit, an open circuit fault has been introduced by a sudden shutdown of all the switches in the converter and voltage of the clamp circuit has been monitored as shown in Fig. 15. The initial capacitor voltage is the peak of the virtual DC wave and as soon as the fault occurs, the energy from the inductive load is taken up by the clamp capacitor which will cause a corresponding increase in the voltage until it reaches the final voltage and then the clamp circuit will be discharged based on the value of the resistor connected in parallel to the capacitor.

TABLE II. COMPARISON OF PROPOSED SST TOPOLOGY, TOPOLOGY OF [7] AND MATRIX CONVERTER

Parameter	Proposed Topology	Topology of [7]	Matrix Converter
Modulation Method Employed	Sine-triangular PWM	Venturini Modulation	Venturini Modulation
Commutation	4-Step commutation	4-Step commutation	4-Step commutation
Number of switches	32	48	18
Voltage regulation ratio	0.5	0.5	0.5
Comparative volume	Medium	High	Low
Galvanic Isolation	Yes	Yes	No

CONCLUSION

This paper has discussed a new modular and isolated AC/AC power converter topology which is suitable for grid interconnection systems. The proposed topology extends the concept of indirect matrix converter to the isolated case. Just as the rectifier stage in the indirect matrix converter generates a virtual DC wave, the input bridges in the proposed topology

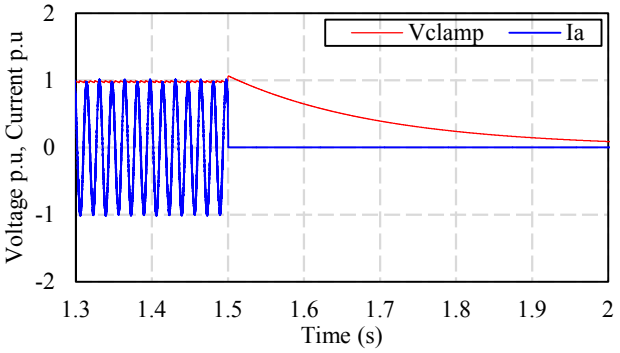


Fig. 15 Clamp circuit in operation due to open circuit fault generated due to sudden shutdown of the converter at t=1.5s. Voltage in p.u. with base voltage V_{base}=220V. Current in p.u. with base current I_{base}= 55A

generate a virtual square wave. The output bridge can be modulated to generate any desired output voltage and frequency. Furthermore, considering a balanced three phase system, unity voltage regulation ratio can be achieved.

The analysis and operation of the converter concept, including modulation and commutation has been validated in PLECS software.

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