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Design of a class-D audio amplifier

by

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Abstract

Amplifier technology has greatly advanced the last two decades. MOSFET transistors have successfully replaced bipolar junction transistors with comparable audio performance. Switching power amplification has gained increased attention after research publications that presented models with high fidelity, high efficiency and low complexity.

After looking up several different topologies, Class D seemed the most fitting switching amplification topology: was not as inefficient as mainstream market classes (A, B, AB), not as complex as other classes (e.g. G or H) and has a renewed interest after the breakthroughs in power FET technology which enabled a considerably better performance.

I chose to work on this subject so I could gain a deeper insight of how switching amplification functions and in which ways the parameters of specific system components can affect performance (e.g. SNR or THD).

Thus, I decided – with the invaluable help of my professor Fotis Plessas - to work on Class D. The project was interesting and challenging since I had to design and combine three stages: a Pulse Width Modulator, a Power Amplifier and a low pass Filter.

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Σύνοψη εργασίας

Η παρούσα εργασία πραγματεύεται την μελέτη της τοπολογίας ακουστικής ενίσχυσης τάξης D. Η επιλογή της συγκεκριμένης τοπολογίας έγινε με κριτήριο τις ανάγκες υψηλής απόδοσης ενέργειας και χαμηλού θερμικού αποτυπώματος που έχουν προκύψει στην αγορά της ενίσχυσης ήχου και το γεγονός ότι οι παραδοσιακές τοπολογίες δεν μπορούν πλέον να ανταποκριθούν επαρκώς στις νέες αυτές προσδοκίες.

Με την αυξημένη ανησυχία για τις περιβαλλοντικές επιπτώσεις της αύξησης της θερμοκρασίας στον πλανήτη και την αυξημένη ζήτηση φορητών και μικρών σε μέγεθος συσκευών ενίσχυσης ήχου, ανοίγεται ουσιασικά μια νέα αγορά με σωρεία εφαρμογών σε ήδη υπάρχοντα προϊόντα: φορητους ενισχυτές, smartphones, tablets, τηλεοράσεις, car audio players. Η διαφορά της τάξης D με τις κλασσικές τάξεις ενίσχυσης (A,B ή AB) είναι ότι με την χρήση ειδικών μεθόδων διαμόρφωσης, μπορεί να πετύχει θεωρητικά επίπεδα αποδοτικότητας 100% και πρακτικά επίπεδα τόσο υψηλά όσο 95%. Αυτό σημαίνει ότι είναι σε πολύ ανώτερη θέση σε σύγκριση με τη μέγιστη δυνατή πρακτική απόδοση της τάξης AB που ανέρχεται στο 50%. Ακόμη, το γεγονός ότι λιγότερη ενέργεια καταναλώνεται στα MOSFET σημαίνει αυτόματα και μικρότερες σε μέγεθος ψύκτρες (για εφαρμογές περιορισμένης ισχύος μπορεί να μην χρειαστούν ψύκτρες).

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Για τους προαναφερθέντες λόγους λοιπόν, θα γίνει μια διερεύνηση στους διάφορους τρόπους διαμόρφωσης, τις παραμέτρους του κάθε σταδίου στην αλυσίδα επεξεργασίας του σήματος μέχρι την ανάκτηση του ενισχυμένου σήματος στην έξοδο. Θα ξεκινήσουμε με μία αναφορά στις παραδοσιακές μεθόδους ενίσχυσης για να ακολουθήσει μια ενδελεχότερη επισκόπηση της τάξης D. Προς το τέλος της αναφοράς, θα δείξουμε τα εργαστηριακά σχέδια ενός πρότυπου ενισχυτή τάξης D, για να καταλήξουμε στα συμπεράσματα της εργασίας.

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Acknowledgements

My family, my professor and my friends.

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Audio reproduction has certainly transformed over the decades in order to become what it is today. Long gone are the times one would need half a drawer's size of a stereo system to drive two loudspeakers. With the boom of smart devices, audio industry has shifted decades' long interest in high fidelity towards portability and efficiency. Coupled with the rising concerns about environmental sustainability and the ever growing cost of energy, we could safely assume that a sound reproduction technology which would not account for the latter qualities can hardly survive in the current market. This assumption is correctly verified by the spectacular increase in the use of Class D Amplification in consumer electronics.

Class D

Class D is redefining the trade-offs in audio power amplifier design, simultaneously delivering smaller size and higher power density with better sound than Class AB audio systems. Class D also has the advantage of offering low distortion and more stable dynamic response compared to Class AB audio systems while power semiconductors also help boost efficiency and facilitate audio performance.

Operation

Class D is a topology which involves modulating an analog input signal to digital and then switching it at the speed of some hundreds of KHZ with power MOSFETS. The last stage includes the filtering of the high frequency signal and the acquisition of the original signal (amplified) on the output. The use of negative feedback is more than welcome (if not necessary) as to reduce distortion levels.

Chapter 1

Introduction

1.1 Goals of this project

The goal of this project was to design a class D audio amplifier using PSPICE.

PSPICE was the tool of choice because it could provide transistor and passive component modeling closer to the real world, helping us take into consideration the parasitic capacitance and inductance circuit components might exhibit.

1.2 Report Organization

This report follows the progress made throughout this project. In Chapter 2, background research is presented to prepare the reader for the rest of the report. Chapter 3 deals with the Class D PSPICE design. The results of the testing done on this revision are given in Chapter 4. In Chapter 5 are noted the conclusions of the project and comments regarding future work on the subject.

Chapter 2

Background

This chapter contains an overview of common amplifier stages.

In the last part, Class D amplifier operation will be explained.

2.1 Synopsys of main Amplification Stages

Class A

Class A amplifiers usually consist of a Bipolar Junction Transistor (BJT) that operates constantly in the linear region to amplify the input signal (even when there is none). The voltage between the collector and the emitter depends on the voltage between the base and the emitter. This means that the amplified signal at the output is proportional to the input signal (with a 180° phase shift). Linearity is what class A amplifiers are famous for. HIFI enthusiasts choose them for their exceptional fidelity in reproducing audio.

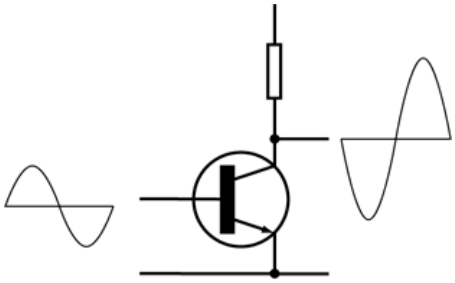


Figure 2.1.1: The operation of a class A amplifier.

Class-A designs are simpler than other classes; for example class AB and B designs require two devices (push–pull output) to handle both halves of the waveform; class A can use a single device single-ended. The point at which the device comes closest to being cut off is not close to zero signal, so the problem of crossover distortion associated with class-AB and -B designs is avoided.

The main drawback of class A amplifiers is low efficiency. The power transistors have to constantly operate close to saturation and this amounts to high heat dissipation (and the need of massive heat sinks).

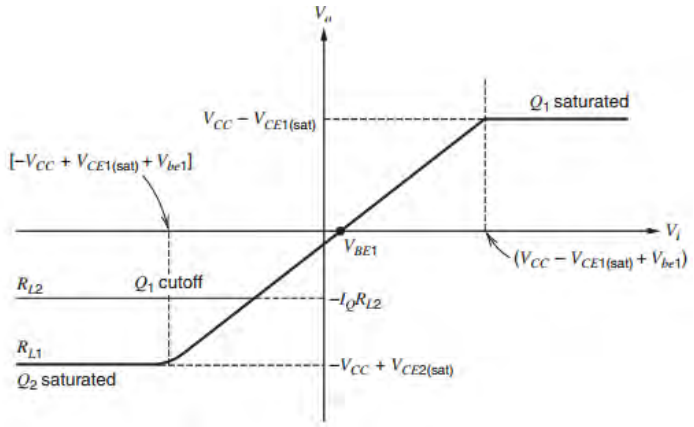


Figure 2.1.2 Transfer characteristic of circuit in Fig. 2.1.1

Inefficiency comes not just from the device always conducting to some extent but also from the fact that the standing current is roughly half the maximum output current (though this can be less with a square law output stage), and a large part of the power supply voltage develops across the output even at low signal levels.

If high output power is needed from a class A circuit, the power waste (in the form of heat) becomes significant. For every watt delivered to the load, the amplifier itself, at best, dissipates another watt. At higher power levels this means very large and expensive power supplies and heat sinks.

To calculate the exact maximum efficiency of Class A would mean to find the ratio of the power generated from the supply to the power delivered to the load.

$$\eta_C = \frac{P_L}{P_{supply}} \qquad 2.1.1$$

Since the power delivered to the load depends directly on the value of the load itself, we need to calculate the value of the load:

$$R_{Lmax} = (V_{CC} - V_{CE\ (sat)})/I_Q$$

2.1.2

The average power delivered to the load with a sinusoidal input voltage V_i would be:

$$P_L = \frac{1}{2} V_o I_o$$

2.1.3

Maximum power is delivered to the load when the values of V_o and I_o are also at their peak (just before clipping).

$$P_L\,|_{max} = \frac{1}{2} V_{om} I_{om}$$

2.1.4

V_{om} is the maximum voltage value before clipping and is equal to:

$$V_{om} = V_{CC} - V_{CEsat})$$

2.1.5

I_{om} is the corresponding current which amounts to the quiescent current I_Q.

Therefore, replacing the aforementioned values in (2.4) results in:

$$P_L\,|_{max} = \frac{1}{2}(V_{CC} - V_{CEsat})I_{Q})$$

2.1.6

Supply power: The current drawn from the positive supply is the collector current of Q1, which is assumed sinusoidal with an average value IQ. The current flowing in the negative supply is constant and equal to IQ. Since the supply voltages are constant, the average power drawn from the supplies is constant and independent of the presence of sinusoidal signals in the circuit. The total power drawn from the two supplies is thus:

$$P_{supply} = 2\,V_{CC}\,I_Q$$

2.1.7

Thus, the final result is:

$$\eta_{\max} = \frac{1}{4}\left(1 - \frac{V_{CE\ (sat)}}{V_{CC}}\right)$$

2.1.8

When $V_{CE\ (sat)} \ll V_{CC}$ the maximum efficiency is 25%.

This figure concerns direct coupling of the amplifier to the load and is very low, since 25% in theory can easily mean half of that amount for a real world circuit.
A technique that uses inductive coupling to the load can further improve the efficiency up to 50%. By coupling the load with a transformer, half of the DC power which was dissipated by the load being directly coupled is now flowing to the transistor.

Emitter follower
In this class A topology, a resistor is placed In series with the emitter for increased gain stability. When input signal Vs is applied to the base, the resulting emitter current I_e develops an output voltage equal to $I_e * R_e$ across the emitter resistance R_e. This voltage opposes the ac signal voltage Vs as it is in phase opposition to Vs. Thus it provides negative current feedback. Moreover, this voltage (V_{out}) feedback to the input is proportional to the emitter current hence this circuit is also called negative current feedback circuit.

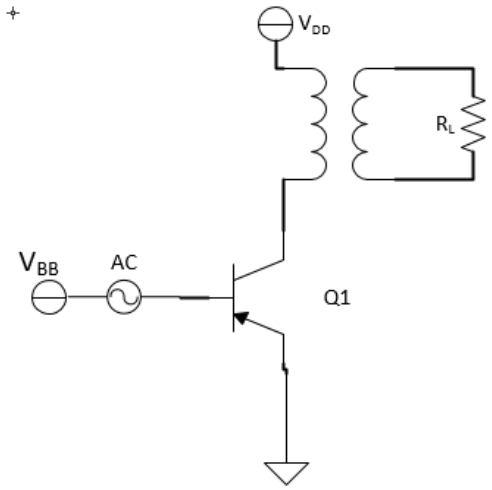


Figure 2.1.3 Class A amplifier using inductive coupling

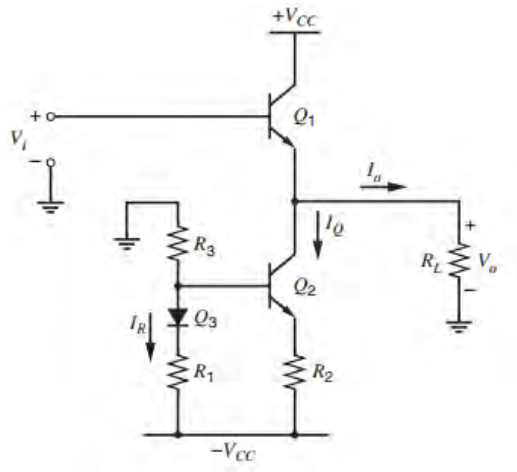


Figure 2.1.4 Current mirror biased emitter follower stage

Class B

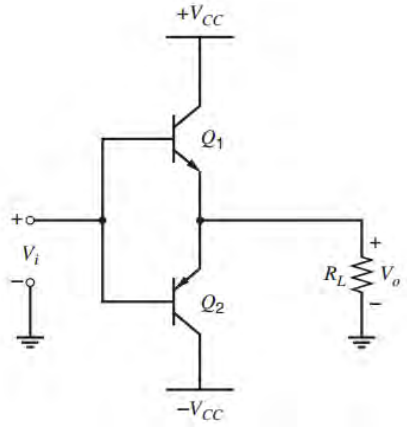


Figure 2.1.5: A class B circuit.

Class B amplifier technology managed to alleviate the efficiency issues of Class A.

The first issue addressed was the continuous operation of the transistor even when the input signal was 0. The solution was the introduction of a second transistor in the topology. In a push-pull topology, each transistor would drive the signal for half a cycle, a N type for the positive cycle and a P type for the negative one.

This advance had its tradeoffs: the transistors did not have a bias circuit and that meant that they could not drive any input below the ON voltage between the Base and the Emitter (that is usually 0.7 Volts for the NPN and -0.7 Volts for the PNP), an effect known as crossover distortion. This introduced a significant nonlinearity issue which had to be addressed (and so it was with the introduction of class AB).

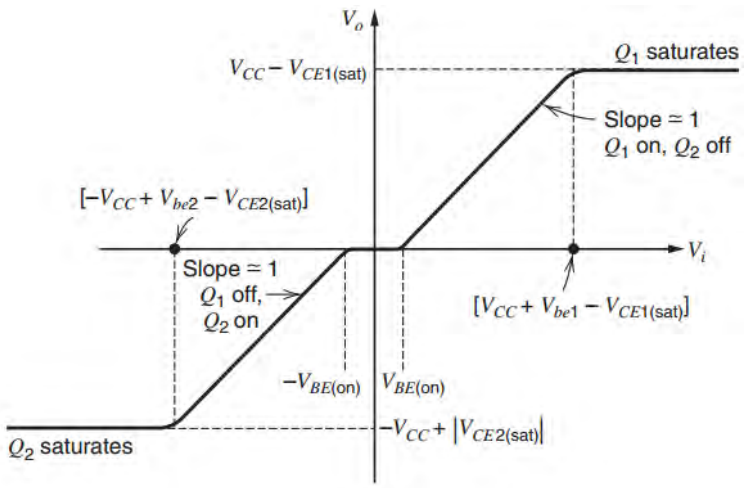


Figure 2.1.6: The transfer characteristic of Class B.

Class AB

The purpose of the creation of Class AB was to make up for the lack of biasing in the B Class circuit (in the "dead zone") while maintaining a fair efficiency.

That was realized with the use of diodes at the input of the push-pull amplification stage. The diodes help keep each transistor at the threshold of its linear region. The amount of diode biasing voltage present at the base terminal of the transistor can be increased in multiples by adding additional diodes.

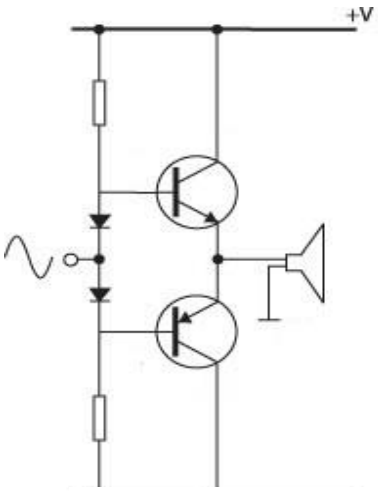


Figure 2.1.7: Class AB stage.

In class-AB operation, each device operates the same way as in class B over half the waveform, but also conducts a small amount on the other half. As a result, the region where both devices simultaneously are nearly off (the "dead zone") is reduced. The result

is that when the waveforms from the two devices are combined, the crossover is greatly minimized or eliminated altogether.

The exact choice of quiescent current, the standing current through both devices when there is no signal, makes a large difference to the level of distortion (and to the risk of thermal runaway, that may damage the devices); often the bias voltage applied to set this quiescent current has to be adjusted with the temperature of the output transistors (for example in the circuit at the beginning of the article the diodes would be mounted physically close to the output transistors, and chosen to have a matched temperature coefficient).

Another approach (often used as well as thermally tracking bias voltages) is to include small value resistors in series with the emitters. Class AB sacrifices some efficiency over class B in favor of linearity. Figures are below 78.5% for full-amplitude sine waves in transistor amplifiers, much less is common in class-AB vacuum-tube amplifiers. In any case, it is much more efficient than class A.

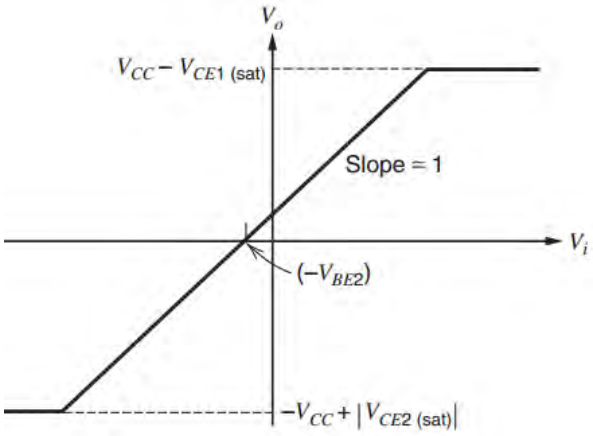


Figure 2.1.8: Class AB transfer characteristic.

Class C

The quiescent point of a class C amplifier is tuned so that it is below the cutoff point. It has a duty of less than half a cycle. Even though this amplifier can achieve a stunning efficiency of about 90%, it sadly has high distortion figures which constrain its use in RF applications.

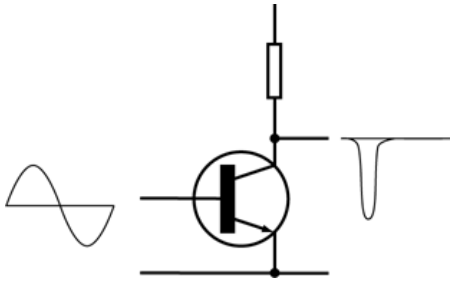


Figure 2.1.9: Operation of a class C amplifier. [Wiki]

Classes G and H

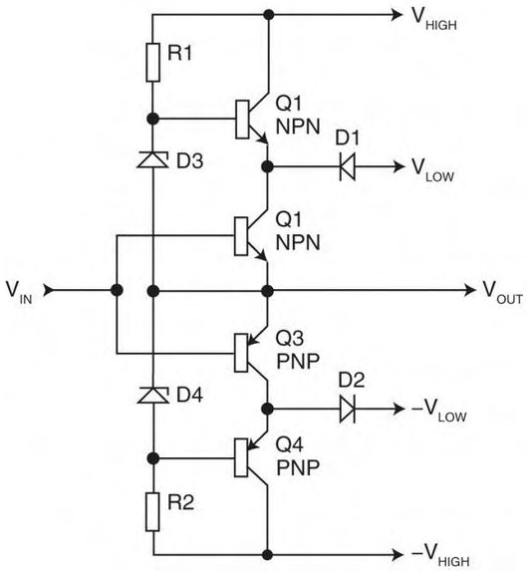


Figure 2.1.10
A Class G Amplifier using two levels of voltage rails V_{HIGH} and V_{LOW}

Class-G amplifiers (which use "rail switching" to decrease power consumption and increase efficiency) are more efficient than class-AB amplifiers. These amplifiers provide several power rails at different voltages and switch between them as the signal output approaches each level. Thus, the amplifier increases efficiency by reducing the wasted power at the output transistors. Compared with class D, Class-G amplifiers are less efficient when compared to class D but do not suffer the adverse effects of EMI.

Class-H amplifiers take the idea of class G one step beyond creating an infinitely variable supply rail. This is done by modulating the

supply rails so that the rails are only a few volts larger than the output signal at any given time. The output stage operates at its maximum efficiency all the time. Switched-mode power supplies can be used to create the tracking rails. Significant efficiency gains can be achieved but with the drawback of more complicated supply design and reduced THD performance. In common designs, a voltage drop of about 10V is maintained over the output transistors in Class H circuits.[1]

Class T

Class T is actually a modification of Class D. The difference lies in their switching speed which is of magnitudes larger than class D (in the range of 50 MHz) and the use of feedback directly from the switching node (instead of feeding the signal back after it has been filtered). It has been patented by Tripath on 1996 (the TA2020 amplifier was named one of the twenty five chips that shook the world by the IEEE Spectrum magazine) [IESpec].

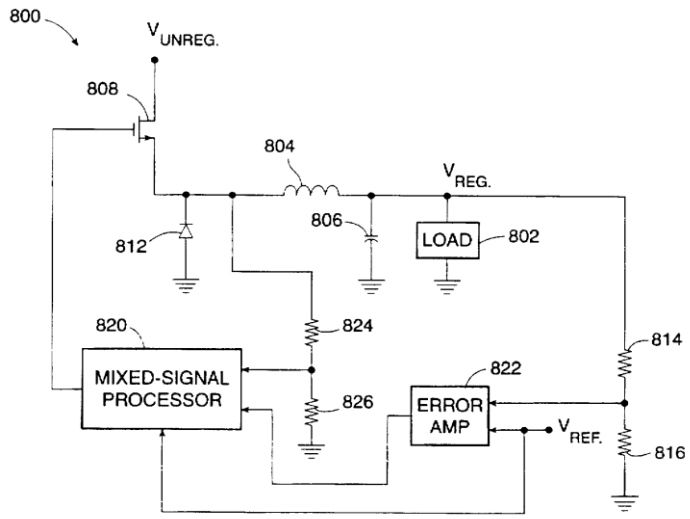


Figure 2.1.11: Class T Amplifier Block Diagram

[1] <http://en.wikipedia.org/wiki/Amplifier#Classes_G_and_H>

[1] Glenn Zorpette, "Class-D Audio: The Power and the Glory" - IEEE Spectrum, 30 Dec 2010 | 15:41 GMT <http://spectrum.ieee.org/geek-life/tools-toys/classd-audio-the-power-and-the-glory>

Class T amplifiers were implemented with various control techniques, some of them including Digital Signal Processing (DSP) chips and higher order modulators similar to Delta Sigma (ΔΣ).

2.2 Class D

Having described in general the operation of the most popular amplifier classes along with their advantages and disadvantages, we will continue by explaining the advantages of Class D over the rest and the general disadvantages and critical factors of design. Also, we will see in which way it can be applied in the audio industry and the several challenges that engineers face.

As we can see on the following figure, a pulse modulator codes the input signal into a stream of pulses which are used to drive a MOSFET power amplification stage. The amplified signal is demodulated using a LPF (low pass filter) before being finally delivered to the load (a speaker),

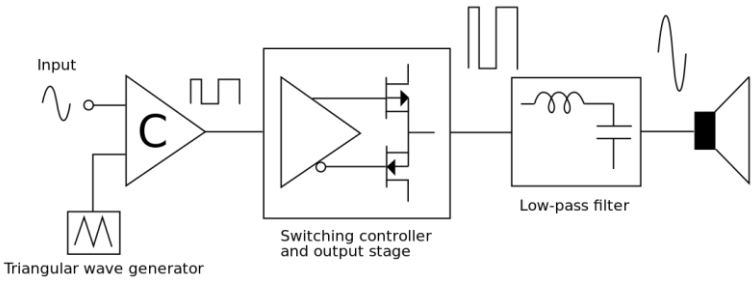


Figure 2.2.1: Block diagram of a basic Class D amplifier.

The MOSFET is the active device which is used in the power stage of this topology. The reason is that its behavior is closer to the ideal switch, when compared with a BJT or an IGBT. Also, it has faster switching times, since it is a "majority carrier"

device and a good linearity and output impedance when it is conducting. Even though MOSFETs have evolved dramatically towards the ideal switch model, there are still delays and distortions during switching that amount to errors which need to be controlled in order to maintain efficiency and overall performance. Two broad categories of errors are Pulse Timing errors and Pulse Amplitude errors.

To track the evolution of class D is close to examining the progress of power FET technology. Over the past three decades, we could roughly classify power FET technology in three 'generations' that match with the according engineering breakthroughs made at the given time.

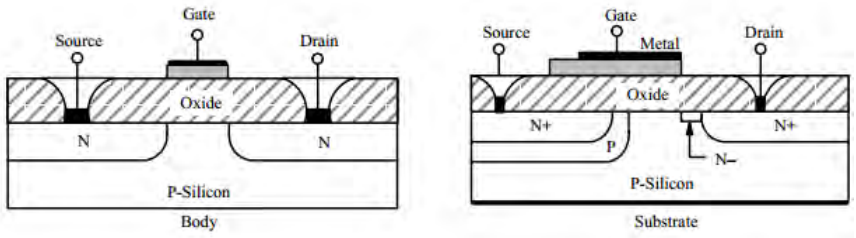


Figure 2.2.2: Cross section of a planar MOSFET (left) and a DMOS (right)

Historic review: Even though production of power MOSFETs had begun since late 1970's, the first generation dates back in the early 1980's when International Rectifier introduced double-diffused planar MOSFETs (DMOS). Because of technologic limitations of photolithography, older MOSFETs had significant restrictions regarding switching speeds and the on resistance of the Drain-Source channel. With the improved channel construction of DMOS there was an alternative to Junction FETs.

The double-diffused source resulted in a shorter channel to the drain which affected the switching speed positively. Also, the vertical flow of the current from the source to the drain enabled the device to handle larger breakdown voltages. The light doping of the N-body epitaxial layer contributed to a higher on resistance which affected low voltage operation.

Siliconix introduced the second generation of power MOSFETs in the 1990's by launching TrenchFET, which implemented the trench FET technology and offered improved Drain-Source on resistance. The difference with DMOS was that instead of having a planar gate under which the current flew, the current circulated through the

vertical walls of the trenches. This allowed for a higher channel density in a given silicon unit. Also, the minimization of the cell 'pitch' enabled a lower on resistance.

These advantages made trench technology an industry standard until the beginning of the 21st century. However, while the technology improved over the decade, it still suffered from gate to drain parasitic capacitances developed across the large walls of the trench. This had an immediate impact on the switching speed of the device.

Trench technology continued to improve through the 2000's with some innovations in the device epitaxy, such as the reduction of the Miller capacitance by adding a silicon oxide layer at the bottom of the trench. Another achievement was the splitting of the gate electrode and the connection of the lower part to the source terminal. This part had a shielding effect; it decoupled the gate from the drain in order to reduce the parasitic capacitance between them.

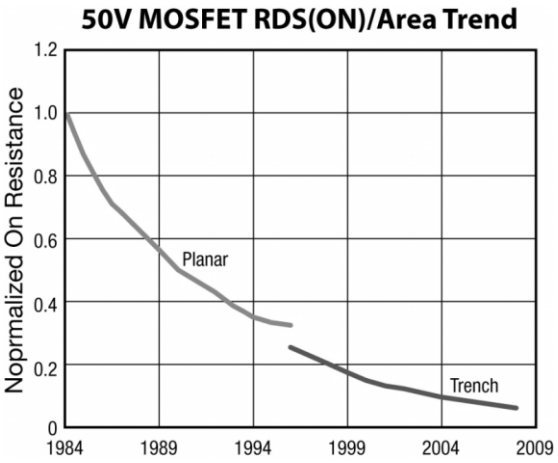


Figure 2.2.3: $R_{DS\ (ON)}$ versus time

It wasn't until the 1990s that cheap and reliable MOSFETs became fast enough to handle the high frequency PWM output. [2] Still, since the circuit engineering was in early stages of development, the final product had high levels of distortion and was by no means able to compete with other analogue 'state of the art Hi Fi' amplifiers.

To achieve the highest efficiency in a Class-D amplifier, the conduction loss from $R_{DS(ON)}$ and switching loss dictated by gate charge Qg should both be as low as possible. Consider the evolution of 200V rated MOSFETs over the last couple of decades. International Rectifier IRF640 from the 1980s, which has a planar structure, has a $R_{DS(ON)}$ of 180mΩ with Qg of 70nC. The latest trench structure MOSFET IRFB4227 has $R_{DS(ON)}$ of 20mΩ with the same 70nC Qg. The FOMs has been reduced from 12,600 to 1400; a nine-fold improvement in the course of two decades.[3]

2.2.1 Class D

Having reviewed the most prominent amplification topologies, we can clearly see that there are theoretical limits to the operation of traditional amplification topologies which cannot be overcome, but only dealt with at a small extent by techniques which benefit efficiency. Designing a Class D is by no means a simple task, as there are numerous parameters to be taken into account and all the signal manipulation stages need to be carefully engineered in order to obtain a sustainable final product. The slightest miscalculation or component misplacement on the board can cause an avalanche of problems with the introduction of noise/distortion being the least significant ones. Let's not forget that high distortion and noise levels were the reason Class D was used to amplify boom boxes instead of Hi Fi sound systems.

Even if Class D sounds like an ideal audio amplification case, this is not the reality. There are constant risks of emitting high amounts electromagnetic interference (EMI) –even beyond FCC approved levels, that is why designs even fail to pass the tests- and/or distortion which can sever the final result's overall quality and performance.

[3]By examining the On resistance ($R_{DS(ON)}$) x gate charge (Qg) figure of merit (FOM) illustrates how closely the performance of today's MOSFETs now approaches that of an ideal power switching device.

The pulse modulated signal must be controlled tightly in order to have the best efficiency to audio quality relation possible from the power stage. The overall result depends on the attenuation performance of the output filter and the user of feedback loops for controlling the inherent errors of the topology.

Applications in the audio industry

Class D has a specific target group in the audio amplification market. This includes mostly amplification solutions with requirements which give high priority to small size and high efficiency. This implies most devices which use audio amplifiers in: home electronics (small to medium powered stereo sound systems, televisions multimedia speakers), car audio, portable devices (instrument amplifiers, laptops, portable music players, smartphones, tablets). With the booming growth of the latter aforementioned devices, Class D has a high potential of dominating the market as the solution of choice because there is a gap of efficiency with the next most efficient topology in line. The option of omitting the filter stage for small size designs (e. g. smartphones) is a nontrivial factor when analyzing the cost of production.

Operation

As we have already mentioned, a class D amplifier consists of three basic stages: modulation, power amplification and filtering. Each stage is essential to the integral operation of the circuit, even though we might encounter some designs which –for financial reasons mainly- omit the filtering stage.

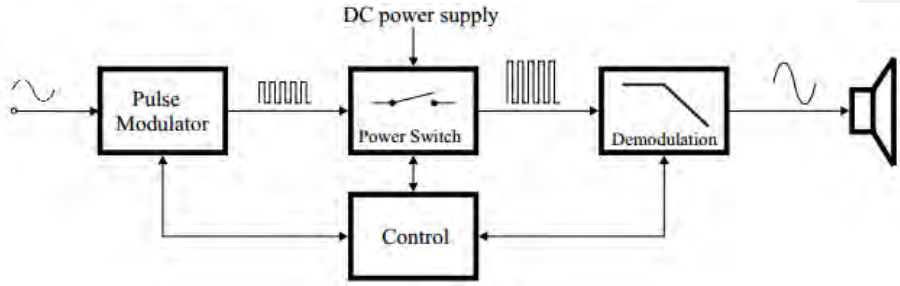


Figure 2.2.4: A basic signal chain for Class D.

The modulation stage is responsible for transforming the signal at the input in pulses which in order to drive the power MOSFETs efficiently. Even though the modulation scheme can be implemented in a variety of ways, the actual function of the pulse

modulator remains the same. The medium that the signal will be sampled to, depends on the specific technique used (can be time, amplitude, frequency etc.). The input audio signal is sampled to a series of high frequency pulses (representing ON and OFF states) which are used to drive the power MOSFETs.

The most popular techniques include Pulse Width Modulation (PWM) and ΔΣ modulation. There are numerous specific implementations of higher complexity that extend upon these two basic sampling forms. In our design we will use PWM but ΔΣ will also be reviewed in order to explain the trade-offs between the two. The performance requirements for the modulator include fast switching times and low noise and EMI figures on the output.

Pulse Modulation

Input signal modulation is the core principle behind the high efficiency of Class D. Without it, the transistors would be have to operate in the linear region for longer periods of time in order to amplify the same signal, thus dissipating larger amounts of heat and becoming inefficient. By modulating the input signal, the transistor is spending the least possible amount of time operating in resistor mode (the exact amount depends on the DV / DI slope or the on resistance of the Drain – Source).

A pulse modulator generally processes the input signal and generates a series of pulses whose spectral content resembles that of Figure 2.2.5. We can discern three discrete elements in the output of the modulator: the input signal component, the distortion components of the input signal and the high frequency (HF) spectrum which may be composed of a mixture of discrete components that arise from the carrier frequency and input signal and stochastic components (noise).

The main concept in class D amplification is that the MOSFET transistors need to operate as switches by having fast transitions between on and off states. The frequency of this switching is between 10 to 15 times larger than the maximum frequency present in the source signal (22 kHz for audio signals). The transistors at the power amplification stage need a logic High to drive the output at the supply voltage level or a logic Low to stop transmitting energy.

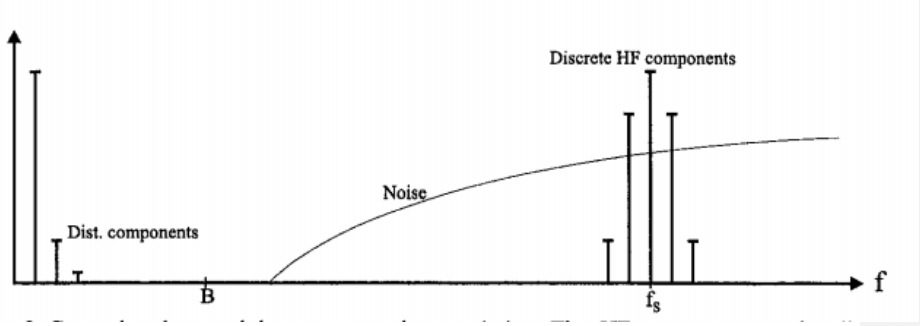


Figure 2.2.5: The spectral components of a pulse modulator's output

Ideally, a pulse modulator should be natively linear (so the need for error correction is diminished), have a minimal switching frequency (f_S) to bandwidth (B) ratio and present the least possible HF spectral content (the ideal condition is to generate none).

The pulse modulator needs to be simple, because we would not want to make the circuit overly complicated and thus more prone to errors and complications debugging these errors; reliable because any loss of information in this primary stage will be replaced in the output by noise and distortion.

The most common methods of modulating the signal are Pulse Width Modulation (PWM, also known as pulse duration modulation) and Delta-Sigma (a discrete time technique, abbreviated as ΔΣ). Also, a new input modulation technique includes the use of Digital Signal Processors (DSP) which significantly reduce the noise.

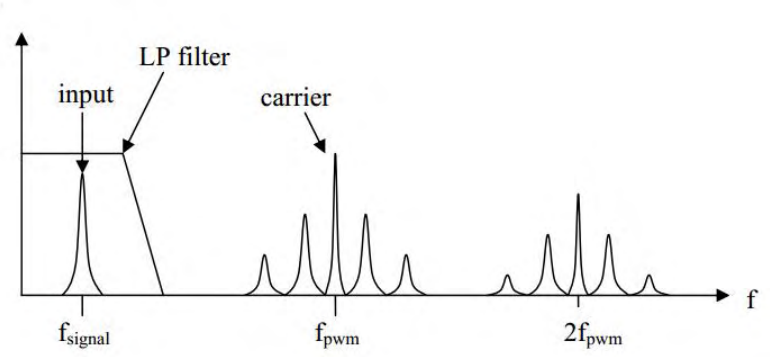


Figure 2.2.6: PWM switching frequency spectrum and harmonics

The four basic Pulse Modulation techniques are Pulse Amplitude Modulation (PAM), Pulse Width Modulation (PWM), Pulse Position modulation (PPM) and Pulse Density modulation (PDM). In Pulse Amplitude Modulation (PAM), the signal is converted into amplitude-modulated pulses (Figure 2.2.7). The bandwidth requirements are given by the Nyquist sampling theorem, so the modulated signal can be uniquely represented by uniformly spaced samples of the signal at a rate higher or equal to two times the signal bandwidth. An advantage of PAM is that its low bandwidth requirements mean a lower switching frequency f_{sw} and this results in less heat dissipation, EMI and a better THD+N figure. PAM though suffers when it comes to the amplification of the amplitude modulated pulses. The power stage cannot amplify accurately the pulses and this is why techniques which use two or three discrete amplitude levels are much easier for the power stage to amplify.

PWM is much different from PAM since the sampling of the signal results in pulses modulated by time, not amplitude. The signal information is sample into the pulse time position within each switching interval. In contrast to PAM, PWM can be implemented using two or three discrete output levels. The disadvantage or PWM is that the requirement for a high switching frequency introduces non-linear problems.

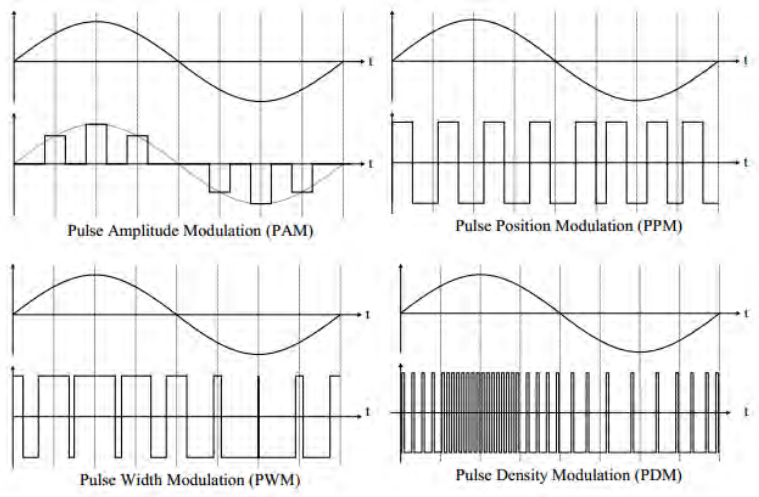


Figure 2.2.7: Basic Pulse Modulation Techniques

Pulse Position Modulation (PPM) differs from PWM in that the value of each instantaneous sample of a modulating wave is caused to vary the position in time of a

pulse, relative to its non-modulated time of occurrence. Each pulse has identical shape independent of the modulation depth. This is an attractive feature, since a uniform pulse is simple to reproduce with a simple switching power stage.

PPM is the requirements for pulse amplitude level if reasonable powers are required. The power supply level of the switching power stage will have to be much higher than the required load voltage. This leads to sub-optimal performance on several parameters as efficiency, complexity and audio performance.

Pulse Density Modulation is based on a unity pulse width, height and a constant time of occurrence for the pulses within the switching period. The modulated parameter is the presence of the pulse. For each sample interval it is determined if the pulse should be present or not, hence the designation density modulation. It is appealing to have a unity pulse since this is easier to realize by a switching power stage.

Another advantage is the simplicity of modulator implementation. Since PDM is a quantizing pulse modulation scheme, the HF spectrum has a stochastic nature. There are reports that have been given regarding the use of PDM both in a digital modulator implementation and analog implementation with the power stage incorporated in the loop. However, the average switching frequency is higher than that obtainable with PWM. This leads to lower performance and a considerably lower efficiency compared with e.g. the PWM based topologies. A further disadvantage is the necessity for a high order loop filter in order to obtain a sufficient noise shaping effect. This is difficult to realize and limits the modulation depth of the modulator. Consequently, PDM is not considered to be a suitable modulation scheme for audio amplification systems, and will not be investigated further.

Type	Bandwidth Requirements	Modulation depth	Efficiency	Complexity
PAM	+	+	-	-
PPM	-	-	-	-
PWM	-	+	+	+
PDM	-	+	+	+

Table 2.1: Comparison of basic pulse modulation techniques

From all this information we presented, PWM looks like the most appealing choice for the specifications of our design which give priority to high efficiency and low noise and distortion figures. Thus, a more in depth look will be taken in PWM.

Natural Sampling Pulse Width Modulation (NPWM)

Pulse Width Modulation and its different modes of operation will now be reviewed. PWM is a technique that codes the amplitude of the input signal in the form of a duty cycle (a percentile of the supply voltage). The most common way this is achieved consists of a comparator being fed the input signal (analog) and a triangle/saw tooth wave. The result of the voltage difference between the two is a logic High if the input signal is higher than the triangle wave and a logic Low otherwise. Pulse width modulation is typically classified in two types, depending on the input signal's nature: natural sampled PWM (NPWM) and uniform sampled PWM (UPWM). We will discuss the analog pulse sampling method, which is NPWM. There also are differentiations in the number of modulation levels (two or three) and the edges modulated (single sided or double sided). All these different modes of operation can also be combined together and produce different results.

The triangle-wave oscillator acts as the sampling clock. The resulting duty cycle of the square wave is proportional to the level of the input signal. When no input signal is present, the duty cycle of the output waveform is equal to 50%. .[4]

Pulse-width modulation uses a rectangular pulse wave whose pulse width is modulated resulting in the variation of the average value of the waveform. If we consider a pulse waveform (t) , with period T , low value y_{min}, a high value y_{max} and a duty cycle D (see figure 2.2.8), the average value of the waveform is given by: $y = \frac{1}{T}\int f(t)dt.$

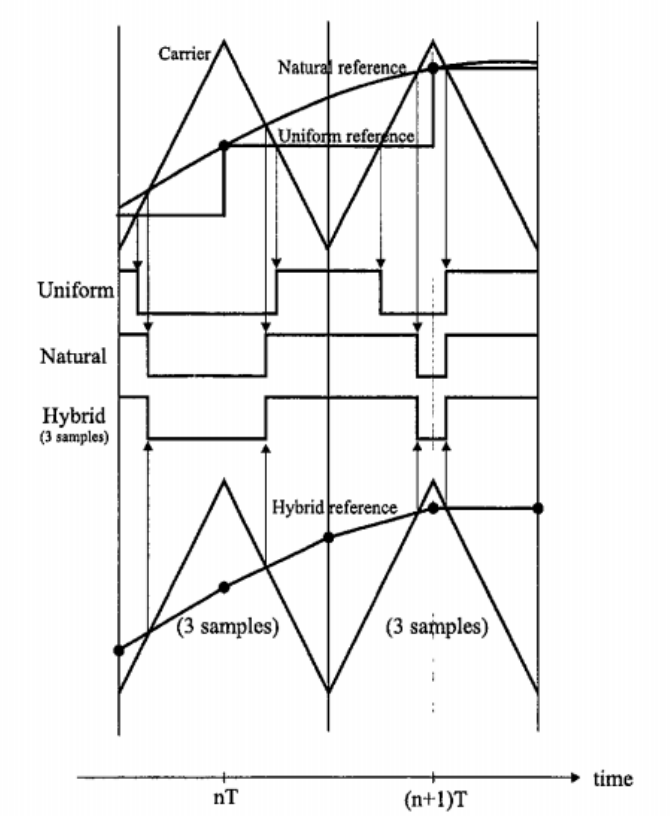


Figure 2.2.8: Basic PWM methods

PWM was the modulation of choice because of its simplicity compared to other methods (e.g. ΔΣ) and its availability to use freely as it is not intellectual property. The frequency ratio is defined as the ratio between signal angular frequency ω and carrier angular frequency ω_c:

$$q = \frac{\omega}{\omega_c} \quad 2.2.1$$

The theoretical maximum for the frequency ratio, is not defined by Nyquist criteria as it would for normal amplitude sampling, but depends on the carrier signal slew rates. For Single Sided modulation, the slew rate would be:

$$SR_S = \frac{\omega_c}{2\pi} \quad 2.2.2$$

In general, the high frequency spectral characteristics will have determining influence on the maximal frequency ratio (the bandwidth limit of the modulation process). Practical considerations as easy demodulation will therefore put tighter constraints on the possible frequency ratios than the limits defined in (2).

The choice of frequency ratio is not of primary importance in order to reveal the characteristics and differences between modulation schemes. The results can easily be generalized to other frequencies. However, it is appropriate to choose a frequency ratio close to a worst case situation, which is the case with q=l/16.

PWM types

There are two basic types of PWM used in class D amplification with the H-bridge topology, AD and BD PWM. AD is the most commonly used technique since it employs the LC low pass filter to attenuate the signal outside the audio spectrum and the surplus energy drawn from the supplies because of voltage spikes.

BD can be used without a filter, since it minimizes switching current, which allows for the speaker to act as the filter. This way, there are larger efficiency margins, since there are no induction losses as in AD. The problem is EMI which is actually driven to the speaker. Since any cable longer than a few centimeters can easily work as an antenna, this technique is mostly used in devices with built-in speakers (e.g. phones).

A review of AD (two level) and BD (three level) NPWM will follow along with the four possible combinations with single and double sided edge modulation. The type of wave that the input signal is compared to depends on the depth of modulation used. A sawtooth wave is used for single sided modulation and a triangle wave for double sided modulation. Since there are four possible combinations of modulation switching type and modulation depth for Natural PWM, we will be using an abbreviation scheme for ease of reference.

The abbreviations for the matter will follow the format:

{Switching}{Edge} (E.g. AD-S for AD single sided NPWM)

AD PWM (single sided) - ADS

Single sided AD is the mostly used PWM technique when it comes to implementing a typical Class D H-bridge amplifier. The duty cycle of a rectangular waveform is modulated, such that its average content corresponds to the input analog signal. The bridge-tied load (BTL) outputs are the inverse of each other. Either the leading or the trailing edge can be modulated in single sided modulation, however the amplitude spectrum is the same for both variants or there will be no differentiation between the two variants.

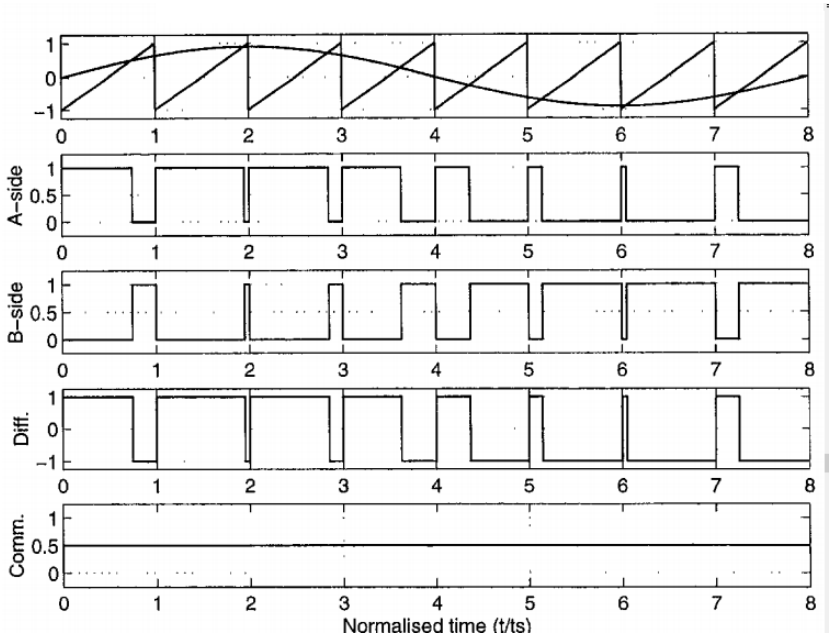


Fig.2.2.9: Natural Sampling, Single sided, AD PWM using a sawtooth wave (ADS).

Note from Fig. 2.18 that no common-mode components are present over the bridge phases. The following will show, that this is a general characteristic of the two level modulation process.

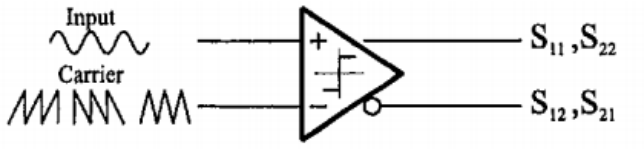


Figure 2.2.10: ADS/ADD modulator

The Discrete Fourier Series (DFS) for Natural AD Single Edged (NADS):

$$F_{ADS}(t) = M\,cos(y) \qquad 2.2.3$$
$$+2\sum \frac{1 - J_0(m\pi M)cos(m\pi)}{m\pi}\, sin(mx)$$
$$-2\sum\sum \frac{1 - J_n(m\pi M)}{m\pi}\, sin\left(mx + ny + m\pi - \frac{n\pi}{2}\right)$$

Where:

M	Modulation index. Ranges from 0 to 1.
$x = \omega_c t$	Carrier signal angular frequency, ω.
$y = \omega\, t$	Input signal angular frequency, ω.
J_n	Nth order Bessel function.
n	Input signal harmonics index.
m	Carrier signal harmonics index.

Some remarks about NADS include:

- The intermodulation components are very pronounced at mx + ny, and depend heavily on the modulation index M.
- The components related to the even harmonics of the carrier reduce with M, and are totally eliminated at idle. At lower M, the dependency between the dominating IM-components and M is nearly linear due to the characteristics of the 1st order Bessel function Jl(x)

One of the most important conclusions form the expression for ADS is that the modulating signal is left unchanged by the modulation, i.e. there are no direct forward harmonics. This means that the modulation process by appropriate filtering can be considered ideal in terms of distortion. This is a very pleasant general characteristic of natural sampling.

AD (Double sided) PWM - ADD

Obviously, NADD modulates both leading and trailing edges of the pulses by using a triangle shaped reference. To calculate the expression of NADD, a simple approach is the direct derivation from ADS by simple superposition:

$$F_{ADD}(t) = F_{ADS}(t) + F_{ADS}(-t) \quad 2.2.4$$

A prerequisite for the above simple addition is that the leading and trailing edge modulated waveforms do not overlap.

The following observations about ADD are made:

- Only IM-components with (m +n) odd are present in the spectrum, meaning that about half the HF spectrum is eliminated in comparison to ADS.
- Similar to ADS, ADD does not have a pleasant spectrum at low M, since the odd harmonics of the carrier are present with maximal amplitude.

From the modulation spectral characteristics, ADD must be concluded to be superior to NADS, but not as attractive as BDS mainly due to the characteristics at lower modulation index.

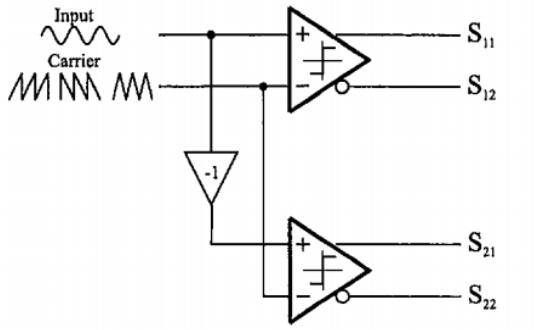


Figure 2.2.11: BDS/BDD modulator

BD PWM (three legs, single edged) - BDS

To define the DFS for BDS we will devise the expression by simple superposition rules from the expression for ADS, since BDS can be synthesized by a 180 degree phase shift of the modulating signal to the opposing half-bridge. Subsequently, what is needed is a general expression for ADS with a phase shifted modulating signal. This is found by simply replacing y with y-φ in function (3).

Finally, $F_{BDS}(t)$ is:

$$F_{BDS}(t) = \frac{F_{ADS}(t) - F_{ADS,\pi}(t)}{2} \qquad 2.2.5$$

The time domain signal characteristics of NBDS are shown in Figure 2.2.12 the existence of a high frequency common-mode signal at the bridge phases, which illustrates the necessity for common-mode filtering.

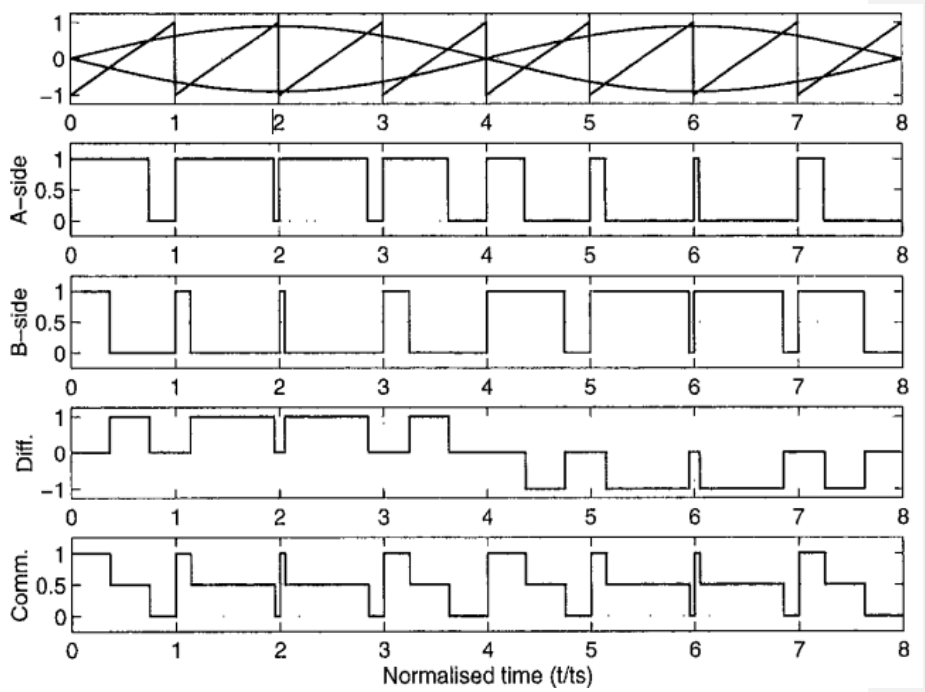


Fig.2.2.12: Natural Sampling, Single sided, BD PWM using a triangle wave.

Some observations about single sided BD PWM include:

- Whereas all harmonics of the carrier were present in NADS (especially the odd harmonics), they are not present in NBDS at all.
- All IM-components mx + ny with even n are eliminated, meaning that the spectrum only contains half the components compared to ADS.

- The maximal IM-component amplitudes are lower than in ADS, as a consequence of the synthesis of three switching levels.

Having asserted these features of BDS, we can safely assume that it is superior in terms of modulation spectral performance to ADS.

BD PWM (three legs, double edged) – BDD

Figure 2.22 depicts the time domain behavior of double sided BD PWM. The differential output illustrates a doubling in the number of samples, i.e. NBDD provides two samples pr. switch period.

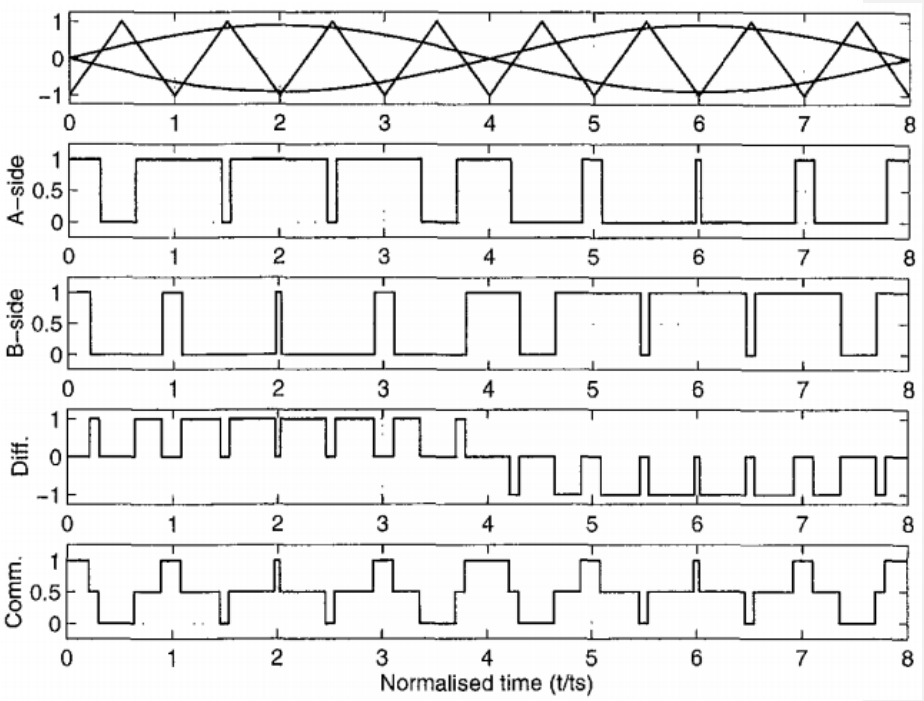


Fig. 2.2.13: Natural Sampling, Single sided, BD PWM using a triangle wave.

Like previous attempts with the aforementioned PWM techniques, the spectrum for NBDD can however also be derived by simple superposition rules as:

$$F_{BDD}(t) = \frac{F_{ADD}(t) - F_{ADD}(t-\pi)}{2}$$

2.2.6

The above outlined advantages of NBDS over NADS also hold when comparing NBDD with NADD. Furthermore, there is one extremely important advantage by using NBDD:

The effective sampling frequency is doubled, while the' carrier frequency (and thereby the switching losses) are retained.

Natural PWM conclusions

The progressive analysis of NPWM given above has illustrated the differing spectral characteristics for the four variants. The most important conclusion of the analysis is that NPWM is totally free from 'forward' harmonic distortion and that in terms of modulation quality, we can deduce that BD switching is always superior to AD as double sided modulation depth is to single sided.

Since BDD is the technique which exhibited the most preferred behavior, some comments will be added. Its HF-characteristics combine three attractive features:

- An effective doubling of the sampling frequency, which is beneficial for demodulation and control system design.
- A total elimination of all components related to the carrier.
- A near linear relationship between M and IM-component amplitude at lower modulation indexes, which causes the idle spectrum to be totally free from components.

PWM drawbacks

Even if PWM might consist an appealing design decision because of its simplicity, there are some considerable drawbacks. The noise spectrum, while having a higher SNR than other types of modulation contains a large amount of high amplitude noise contained in a series of very narrow frequency bands. This makes the noise more difficult to remove with filters than if the noise were of equal or even higher energy, but was spread evenly over a larger number of frequencies.

The use of PWM is imposing limits in the systems which implement it in how they can be altered the final design which will be printed onto the circuit board should differ from the theoretical CAD amplifier design. Without the use of feedback in the system, it is very difficult to modify the response and overall behavior of the modulator.

Total Harmonic Distortion

An important comparison parameter is the forward harmonic distortion of the modulated signal. This parameter differs widely between the general sampling schemes of PWM. THD is generally dependent on both frequency and modulation index, so an investigation vs. both of these parameters are required.

Power Amplification Stage

The output signal of the modulation stage needs to be amplified. In the power amplification stage -every few μs- MOSFET transistors constantly switch the output voltage level from ON (Supply Voltage) to OFF (0 Volts). This process has certain considerations that should be considered in order for the amplifier to function with fidelity and efficiency. Since all of these requirements cannot be satisfied altogether there are tradeoffs and some design decisions are to be made.

Class D amplifiers are commonly configured to operate in half bridge or H-bridge (full-bridge) mode. Half Bridge mode offers a more economical and compact design but the design needs more care in order to have low distortion, EMI and a good THD+N performance (e.g. below 0.1%).The H-Bridge mode has a higher complexity and overall cost –double the components of the respective half bridge model for filtering and amplification are required- but offers higher SNR levels and less distortion. For simplicity, we will use the half bridge model.

Since the power stage consists of two MOSFET transistors in push-pull topology, there is a cross over region where both are simultaneously on.

The smaller the width of this region the lower the distortion (there is less signal cancellation). However, if the duration of the mutual shutdown of the MOSFETs is too small, that means that they can overlap. Having both transistors on though means the formation of a path from the positive to the negative supply and causes large shoot

through currents that put the integral operation of the transistors at risk. It is important at this point to ensure and prioritize the safe and reliable operation of the amplifier over audio quality.
The introduction of such practices to control the timing of MOSFET operation needs extreme caution because is very sensitive and prone to distortion and errors. These errors belong to the so called Pulse Timing Errors and

The following table depicts the most important differences between the two models:

	Half Bridge	**H-Bridge (Full Bridge)**
Supply voltage	0.5 x 2ch	1
Current ratings	1	2
MOSFET	2 MOSFETs/CH	4 MOSFETs/CH
Gate Driver	1 Gate Driver/CH	2 Gate Drivers/CH
Linearity		No even order HD
DC Offset	Adjustment is needed	Can be cancelled out
PWM pattern	2 level	3 level PWM can be implemented
Notes	Pumping effect Need a help of feed back	Suitable for open loop design

Table 2.2: Qualitative Comparison between H-bridge and half bridge

Half Bridge

The half bridge circuit consists of an upper and lower MOSFET connected in a cascade arrangement. If considered as a circuit in itself, it would have five terminals, two connections for each MOSFET's gate input, two more for the DC supply and one for the output to the demodulation filter. The half bridge is also called a "totem pole" since the MOSFETs are stacked on top of each other in that way. There are two possible configurations for the half bridge: either there are two N- channel MOSFETs (from which the one on the LOW is being driven with the inverted signal) or there is a HIGH P-channel MOSFET with a LOW N-channel MOSFET.

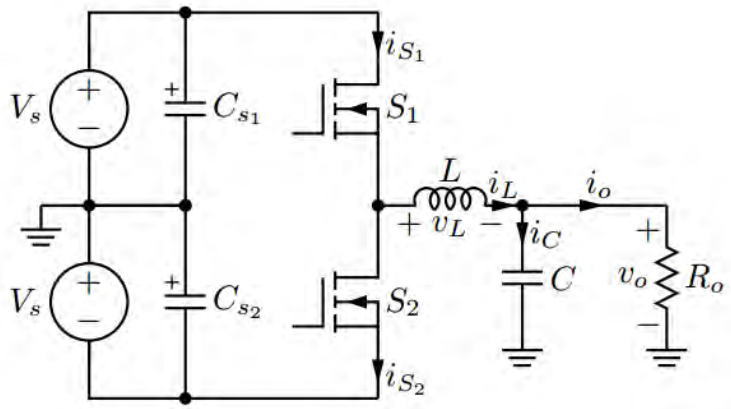


Fig. 2.2.14 Simplified rendition of the half bridge topology

Figure 2.23 depicts a half bridge composed by N-channel MOSFETs which delivers energy to LC demodulating filter and finally to the load. The HIGH side MOSFET is used to switch the positive supply to the load for forward direction (high-side switching) while the LOW side MOSFET is used to switch the negative supply to the load for reverse direction (low-side switching).

The following table shows the possible modes of operation for the power MOSFETs and their effect on the load (speaker).

S1	S2	Speaker Function
OFF	OFF	No motion
ON	OFF	Forward Cone Motion
OFF	ON	Reverse Cone Motion
ON	OFF	Shoot Through Current

The half-bridge topology requires the use of a split-supply to deliver a ground-referenced output signal with no DC component to the load. In some implementations a half-bridge power stage is operated from a single supply.
However, this requires the use of an output DC blocking capacitor in series with the load. Placing a capacitor in series with the load is less than optimal since it leads to increased levels of distortion and, unless the capacitor value is very large, a modified frequency response. Depending on the power level of the amplifier, the capacitor will also be physically large.

The drawback when using a split supply is that the gate-drive circuitry operates relative to the negative supply rail. Level-shifting circuitry is needed for the gate-drive circuitry to interface with the control circuitry, which typically operates relative to ground potential.

Full Bridge

A full bridge amplifier always has two of the four MOSFETs on at a time. This differs from the half-bridge amplifier, which has only two possible states, in that the full bridge can achieve three different states. The states are positive, negative and neutral. The amplifier gives the load a positive voltage when switches AH (left side HIGH MOSFET) and BL (right side LOW MOSFET) are on at the same time, a negative voltage when BH (right side HIGH MOSFET) and AL (left side LOW MOSFET) are on, and the load is grounded when AL and BL are on at the same time.

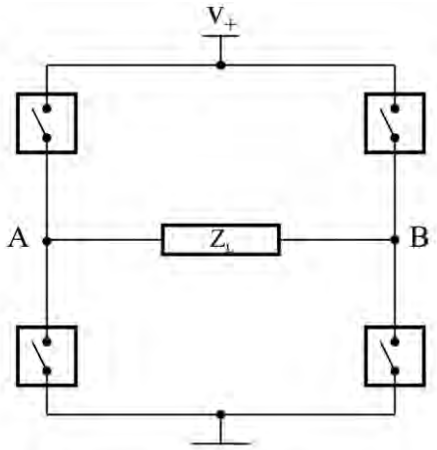


Figure 2.19 H-bridge configuration

When using an H-bridge it is extremely important to make sure that AH and AL are never on at the same time and that BH and BL are never on at the same time because this would short the rails and damage both the amplifier and the speaker.

Two of the big advantages of the full-bridge are that even order harmonic distortion and DC offsets are canceled out, which is extremely important in audio systems. Harmonic distortion negatively affects the quality of the output and DC offsets can damage a speaker. Removing this harmful DC offset in a half-bridge amplifier would require using a more complicated power conditioning stage.
On the other side, almost twice the quantity of components (compared to the half bridge model) are needed –this includes the low pass filter components and the MOSFET drivers and depending on the topology, PWM modules-.

MOSFET parameter considerations

Drain-Source Breakdown Voltage, BV_{DSS}

It is important to choose the lowest BV_{DSS} possible because this parameter is related to others such as $R_{DS(on)}$. Higher BV_{DSS} results in higher $R_{DS(on)}$ and higher MOSFET power losses. MOSFET conduction losses are directly related to $R_{DS(on)}$ parameter.

Drain-to-Source On-Resistance, $R_{DS(on)}$

$R_{DS(on)}$ -the Drain-Source resistance- is typically specified on datasheet at 25°C with V_{GS} = 10V for standard Gate MOSFETs. $R_{DS(on)}$ along with Drain current define MOSFET conduction losses during amplifier operation, and can be calculated as follows: $P_{CONDUCTION} = (I_{D\,RMS})^2 * R_{DSon_)}$

Amplifier efficiency is related to MOSFET total power losses. These power losses are the result of MOSFET conduction, switching, and Gate charge losses. Furthermore, the MOSFET's junction temperature T_J and heatsink size depend on this power losses amount. High power losses increase T_J, and therefore, heatsink size.
$R_{DS(on)}$ is temperature-dependent, increasing when T_J increases. Care must be taken during the thermal design, regarding this, to avoid thermal runaway. In addition, it is important that the maximum MOSFET junction temperature $T_{J\,max}$, should not be higher than specified in the datasheet during all amplifier operating conditions. Then, the maximum MOSFET conduction losses calculation should be done at maximum amplifier operating conditions, using $R_{DS(on)}$ at $T_{J\,max}$, typically specified in the datasheet, and maximum $I_{D\,RMS}$ current.

Gate Charge, Qg.

The MOSFET Gate charge Qg is the charge required by the Gate to fully turn-on the MOSFET. This parameter is temperature-independent and is directly related to the MOSFET's speed. Lower Qg results in faster switching speeds and lower Gate losses; consequently, lower switching losses and better efficiency is achieved.

Overall linearity is affected by switching timing errors such as MOSFET turn-on and turn-off delay times. This implies that the amplifier linearity is also affected by higher Qg. However, these timing errors caused by MOSFET switching are not as significant when compared to dead time (both transistors being on) and, can be significantly reduced by selecting the right dead time value.

As is shown below, the gate of the High Side MOSFET needs time to be charged, which amounts to the ON delay depicted. Also, there is overshoot and some ringing which

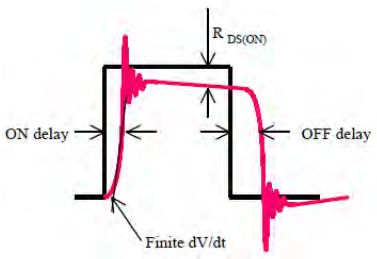


Fig. 2.2.16: Difference between ideal and actual MOSFET outputs

follows caused mainly by stray inductance. The Drain-Source ON resistance is responsible for the slope of the voltage. The same phenomena apply when switching to OFF from ON. [Power basics]

The MOSFET switches exhibit behavior far from what would be an ideal amplification to the input signal.

Figure 2.28 below depicts some causes of degradation of the original pulse shape and these parameters will be commented on.

Body Diode Reverse Recovery Charge, Qrr

Intrinsically by design, the MOSFET structure has a built in reverse diode, and its reverse recovery characteristics are related to amplifier performance as well. Reverse recovery charge Qrr, is defined as the area under Irr during trr. Qrr is mainly determined by IF and dIF/dt. It is a temperature dependent parameter, increasing when TJ increases.

Qrr affects amplifier efficiency and EMI performance. The relationship with efficiency is due to the power bridge circuit configuration. During operation, the reverse recovery current generated by the MOSFET's body diode after commutation current, flows also in the complementary MOSFET of bridge circuit, causing an increase in turn-on switching losses due to the current increment.

Internal Gate Resistance, $R_{G(int)}$.

Internal Gate Resistance $R_{G(int)}$ is a temperature dependent parameter, increasing when temperature increases. This parameter affects MOSFET on and off switching times. Higher $R_{G(int)}$ increases total Gate resistance, decreases Gate current (as shown in Figure 10), increases switching times, and thus, MOSFET switching losses. Furthermore, a large variation of $R_{G(int)}$ affects dead time control. Therefore, $R_{G(int)}$ parameter distribution should be taken in consideration for amplifier performance tolerances.

Dead time

When the transistors in the power stage are on, they have a very low resistance (around half an Ohm). This means that in situations where they both are on, there is a low resistance path created from the positive rail supply to the negative one, resulting in large shoot-through current. This mode of operation not only does reduce the overall efficiency of the amplifier; (since the large current amounts to more heat being dissipated by the transistors) it can severely -even irreparably- damage the MOSFETs. The time intervals in which both transistors are off are called non overlap time or dead time. Dead time is typically controlled by using a MOSFET driver. The driver might contain additional circuitry which adds an amount of delay to one rail so that the switching time does not coincide with that of the opposite transistor half. The dead time needs to be carefully adjusted as it is a figure that highly effects amplifier stability, noise and distortion levels. If for example, the dead time is too low, this will result in more shoot-through current which can severely damage the transistors or even destroy them (if they constantly handle currents beyond manufacturing tolerance). Additionally, a wrongly set dead time can introduce additional harmonic distortion, since opposite signals of the same amplitude can be cancelled out.

Level Shifting

It is fair to say that the level shifter is one of the important parts of the circuit when a low distortion figure is required, and this is evidenced by the wide variety of vendor integrated circuits designed for the job. Each will have advantages and disadvantages, but in all cases the complexity is far greater than may be implied by the simplified block diagrams.

In order to excite the MOSFET driver, the PWM signal has to be referred to -Vss. So, as the modulator usually works from +/-5 to +/-12V, typically, a level shifting function is needed. One can choose to shift the level of the PWM signal and then generate the inverted version, or generate both outputs and invert both of them. It depends, for example, on the comparator type used (if complementary outputs are available, the decision is made).

Gate Drivers

Due to the comparator's inherent inability to support large currents, a new model component for the class D amplifier is needed to provide sufficient current ratings. If we model it as a capacitor in series with a resistance, it needs a considerable amount of current (more than the output of the PWM) to be charged and discharged quickly enough to stay synchronized with the train of pulses generated by the comparator.

MOSFET drivers are circuits specifically designed to control the flow of the PWM output and drive both transistors with adequate current and voltage to minimize the switching delay time and prevent from having both of the transistors on simultaneously.

The gate of a MOSFET transistor needs a gate to source voltage referenced to the positive power supply in order for the high transistor to switch ON. There are several configurations available to drive the two MOSFETs with many different applications.

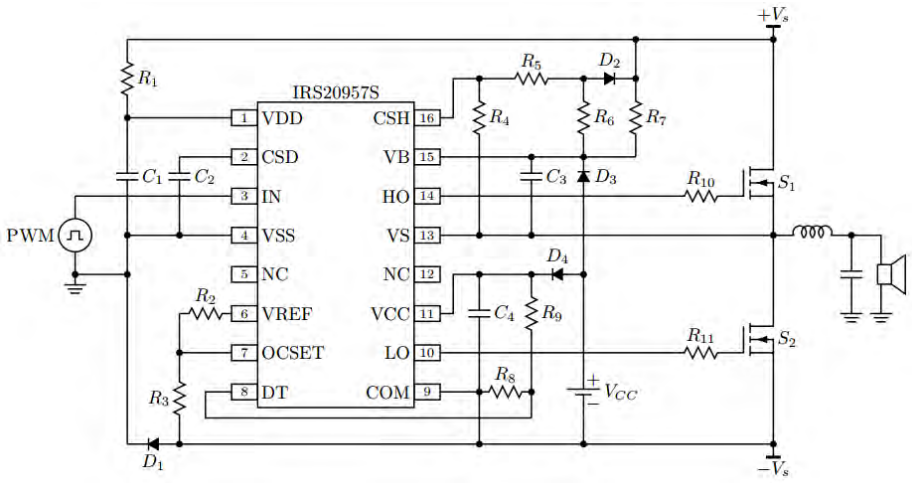


Figure 2.2.17: IRS20957S driving MOSFETs in half bridge

Most gate drivers can only provide positive output voltages, therefore only NMOS can be turned on by them. A gate driver for class D operation has to provide a high and low output voltage in order to turn on and off simultaneously two cascaded NMOS transistors.

Even though the totem pole configuration of a half bridge Class D amplifier consists of a HIGH side N- channel MOSFET in cascade with a LOW P-channel MOSFET, it is required for both the transistors to possess the same characteristics in order to have low noise and good CMRR when stimulated by the driver. Both the P-channel and the N-channel devices can be driven by a single gate drive IC as the one shown above.

Bus Pumping

The power supply voltage buses of half-bridge circuits can be "pumped" beyond their nominal values by large inductor currents from the LC filter. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

The bus pumping effect can be aggravated if the operating frequency is low (the period is longer and so is the pumping effect), the bus capacitors are small (same energy causes a larger voltage spike) or if the output voltage and / or load impedance have high values (). The dV/dt of the pumping transient can be limited by adding large decoupling capacitors (usually electrolytic) between VDD and VSS.

Full-bridge circuits do not suffer from bus pumping, because inductor current flowing into one of the half-bridges flows out of the other one, creating a local current loop that minimally disturbs the power supplies.

Distortion and switching speed

Two significant design challenges for MOSFET driver circuits in class D amplifiers are keeping dead times and linear mode operation as short as possible. "Dead time" is the period during a switching transition when both output MOSFETs are driven into Cut-Off Mode and both are "off". Dead times need to be as short as possible to maintain an accurate low-distortion output signal, but dead times that are too short cause the MOSFET that is switching on to start conducting before the MOSFET that is switching off has stopped conducting. The MOSFETs effectively short the output power supply through themselves, a condition known as "shoot-through".

Meanwhile, the MOSFET drivers also need to drive the MOSFETs between switching states as fast as possible to minimize the amount of time a MOSFET is in Linear Mode, the state between Cut-Off Mode and Saturation Mode where the MOSFET is neither fully on nor fully off and conducts current with a significant resistance, creating significant heat. Driver failures that allow shoot-through and/or too much linear mode operation result in excessive losses and sometimes catastrophic failure of the MOSFETs.

Types of Errors

It is appropriate to divide the error sources in to pulse timing errors (PTE) and pulse amplitude errors (PAE).

Pulse Timing Errors arise from:

· The turn-on and turn-off delays t_{dr} and t_{df}.

· The blanking delay t_d.

· The finite rise- and fall-times t_r and t_f.

Pulse Amplitude Errors (PAE) are attributed to:

· Perturbations on the power supply that feeds the switching power stage.

· Finite impedance for the power switches.

· High frequency resonant transients on the resulting pulse power signals.

Filtering Stage

After being amplified, the PWM signal contains large amounts of high frequency energy (that can even exceed FCC approved levels) that need to be filtered out in order for the audio signal can be driven to the load. Depending on the performance needed the design can have many levels of complexity and there are certain considerations that need to be taken into account for the filtering circuit to successfully exclude unwanted frequency ranges while not degrading the signal. E.g. this may include phase shift, distortion, output impedance tampering or equalization).

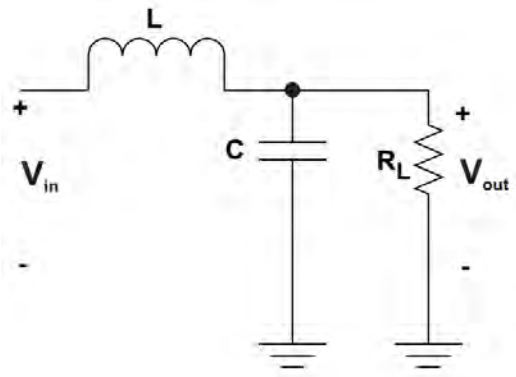


Figure 2.2.18: A typical low pass LC Filter (Single Ended)

Since the signal contains the high frequency PWM carrier (and its harmonics) we need a Low pass filter which should ideally block any signal containing frequencies higher than 22 kHz (also called the frequency corner,f_c). The corner frequency of the filter is chosen so that the filter will have minimal effect on the desired output frequency range while attenuating the switching noise as much as possible. For our design, a first order Low pass filter exhibited an acceptable transfer function and thus was chosen. The theoretical aspect of this filter will be reviewed followed by comments on two other filtering techniques combined with H-Bridge mode.

2nd order Butterworth LC filter

This is the most common and simple type of low pass filter which is designed with the relatively flat response in the audio spectrum pass-band. It is implemented by using an inductor in series and a capacitor in parallel with the load. There are cases which the second order low pass filter does not reduce EMI adequately in order for a second filter to be connected in series with the circuit, equaling to a fourth order filter. Even though the fourth order filter has a much steeper cutoff frequency knee, there phase noise and overall design cost are increased. An inductor, as a low pass filter, is difficult to optimally tune

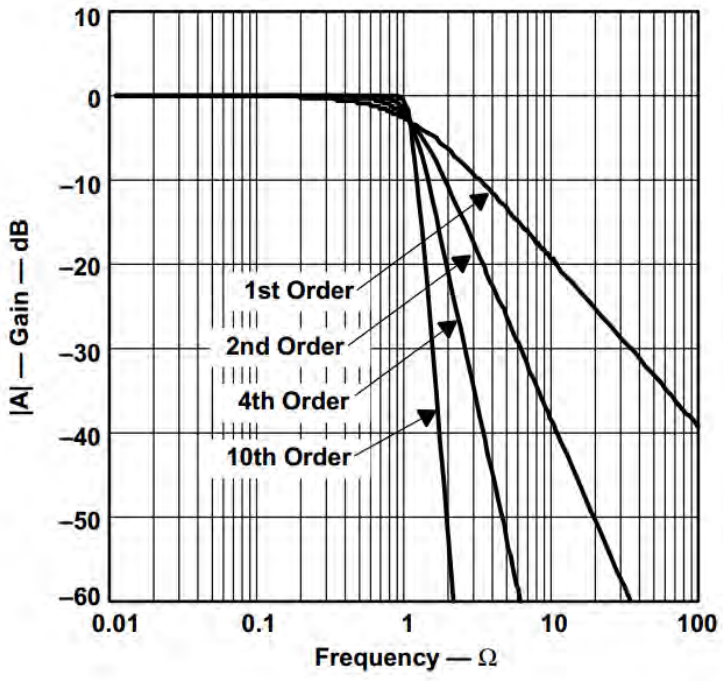


Figure 2.2.19 LPF Cutoff Frequency knees for different order magnitudes

Active Filters

Instead of employing passive components, an active filter is composed of one or more powered components –typically an operational amplifier-. This allows for the addition of gain to the filter and allows the filter to be more accurate. Figure 2.31 shows a simple schematic of an active low-pass filter:

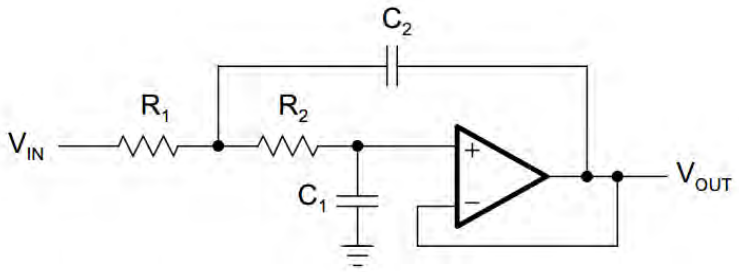


Figure 2.2.20 Second Order Unity Gain active Low-Pass Filter

There is an even simpler approach to building an active filter: connecting a low pass filter to a finite gain amplifier. The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

The difficulty with op-amps is that they require external power and are limited in what frequencies they can handle and they require external power and are limited in what frequencies they can handle

Balanced Filters

Using a balanced filter (against a single ended filter) is desirable because it eliminates the DC offset by centering the signal on zero without the use of a negative rail. This is the reason that it can be used in combination with having a single (positive) power supply. The 2-pole filter provides low-pass filtering before the waveform reaches either speaker lead. With two inductors now required, having a high impedance at the switching frequency for load and LP filter is still a benefit. The next figure depicts a filter suited for and H-bridge amplifier.

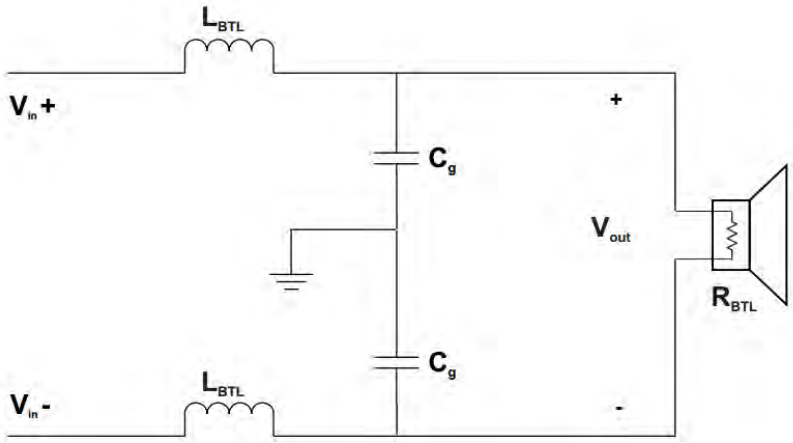


Figure 2.2.21 Balanced Filter for Bridge Tied Load (BTL)

Noise – Sound Quality

Class D amplifiers are extremely susceptible to noise, as the modulation of the signal adds noise to the system. While it is easy to identify that the presence of excessive noise will degrade the audio quality of the system, there are actually several different types of noise, each with their own characteristics.

The amount of noise which is –almost unavoidably- generated in several parts of the class D amplifier, is driven to the speaker and impairs overall sound quality. Since audio quality is almost identical to the amplifier's aural performance, it is critical for the noise figure to be the least possible. Noise is a general concept which is quantitatively defined by its two subtypes: general noise which is portrayed in the SNR (Signal to Noise Ratio) of the output and harmonic noise which relates directly to the THD (Total Harmonic Distortion) figure.

Signal to Noise Ratio (SNR)

A Signal to Noise Ratio is a parameter that describes the ratio of the signal power to the noise power in a system. In the application of audio amplifiers, the output SNR is measured on the output of the filtering stage and is considered to be the ratio of the final amplified signal power to the final amplified noise power. For audio signals, this ratio is represented in decibels (dB), and can be calculated using:

$$SNR = 10\log\frac{P_{signal}}{P_{noise}}$$

In general, the SNR measures the difference between the audio signal and the noise floor. The noise in the noise floor contains several different types of noise that can sum to create an audible "hiss" in high power applications. For the most part, it is impossible to eliminate this background noise entirely by conventional means, although it can be reduced significantly with careful design. One cause of noise is thermal excitation in the amplifier.

While MOSFETs are generally very accurate, there can be random thermal excitation in the silicon, which may cause a small current to flow when none is desired. Similarly, if there is any sort of background noise in the input signal, it will be amplified and will contribute to the system noise floor, reducing the SNR. It is therefore important to have an SNR that is as high as possible, because a higher SNR allows for a higher quality output.

Total Harmonic Distortion

THD is a ratio of the fundamental frequency to the sum of the harmonics, though in practice anything more than the fifth harmonic usually will not contribute significantly to the THD. THD can be caused by several different problems in the system. One such example is clipping of the audio signal. The modulator is designed to support signals up to a certain amplitude. At that amplitude, the modulator outputs a signal that is a constant logic high. The filter will then be designed such that at that amplitude, the output signal will also have a known amplitude. For any input values higher than the system can support, the output signal will have the same known amplitude that it does when the input value is exactly as high as the

system can support. The information that represents the exact amplitude will therefore be lost, and the system will only indicate that the amplitude is at or above a threshold. Fortunately, this is easy to avoid by carefully monitoring input levels to ensure that the input stays within the correct range. Another issue that may decrease THD values is non-linearity in the amplifier. Acceptable linearity can be achieved, but that linearity is dependent upon modulation technique and filter quality. Even if the amplifier is not perfectly linear, a filter may be able to help reduce spurious noise if it is above the audible band of frequencies.

2.2.2.1 Design challenges

Additional Design Considerations

Circuit Protection

The output stage can be exposed to a number of potentially hazardous conditions which need to be:

Overheating

Class D's output-stage power dissipation, though lower than that of linear amplifiers, can still reach levels that endanger the output transistors if the amplifier is forced to deliver very high power for a long time. To protect against dangerous overheating, temperature-monitoring control circuitry is needed. In simple protection schemes, the output stage is shut off when its temperature, as measured by an on-chip sensor, exceeds a thermal shutdown safety threshold, and is kept off until it cools down. The sensor can provide additional temperature information, aside from the simple binary indication about whether temperature has exceeded the shutdown threshold. By measuring temperature, the control circuitry can gradually reduce the volume level, reducing power dissipation and keeping temperature well within limits—instead of forcing perceptible periods of silence during thermal-shutdown events.

Excessive current flow in the output transistors: The low on resistance of the output transistors is not a problem if the output stage and speaker terminals are properly connected, but enormous currents can result if these nodes are inadvertently short-circuited to one another, or to the positive or negative power supplies. If unchecked, such currents can damage the transistors or surrounding circuitry. Consequently, current-sensing output transistor protection circuitry is needed. In simple protection schemes, the output stage is shut off if the output currents exceed a safety threshold. In more sophisticated schemes, the current-sensor output is fed back into the amplifier—seeking to limit the output current to a maximum safe level, while allowing the amplifier to run continuously without shutting down. In these schemes, shutdown can be forced as a last resort if the attempted limiting proves ineffective. Effective current limiters can also keep the amplifier running safely in the presence of momentarily large transient currents due to speaker resonances.

Undervoltage

Most switching output stage circuits work well only if the positive power supply voltages are high enough. Problems result if there is an undervoltage condition, where the supplies are too low. This issue is commonly handled by an undervoltage lockout circuit, which permits the output stages to operate only if the power supply voltages are above an undervoltage-lockout threshold

Electromagnetic interference

The switching power stage generates both high dV/dt and dI/dt, which give rise to radiated emission whenever any part of the circuit is large enough to act as an antenna. In practice, this means the connecting wires and cables will be the most efficient radiators so most effort should go into preventing high-frequency signals reaching those: Avoid capacitive coupling from switching signals into the wiring.

Avoid inductive coupling from various current loops in the power stage into the wiring. Use one unbroken ground plane and group all connectors together, in order to have a common RF reference for decoupling capacitors.

Include the equivalent series inductance of filter capacitors and the parasitic capacitance of filter inductors in the circuit model before selecting components.

Wherever ringing is encountered, locate the inductive and capacitive parts of the resonant circuit that causes it, and use parallel RC or series RL snubbers to reduce the Q of the resonance.

Do not make the MOSFETs switch any faster than needed to fulfil efficiency or distortion requirements. Distortion is more easily reduced using negative feedback than by speeding up switching.

Power supply design

Class D amplifiers place an additional requirement on their power supply, namely that it be able to sink energy returning from the load. Reactive (capacitive or inductive) loads store energy during part of a cycle and release some of this energy back later. Linear amplifiers will dissipate this energy away, class D amplifiers return it to the power supply which should somehow be able to store it. In addition, half-bridge class D amps transfer energy from one supply rail (e.g. the positive rail) to the other (e.g. the negative) depending on the sign of the output current. This happens regardless of whether the load is resistive or not. The supply should either have enough capacitive storage on both rails, or be able to transfer this energy back.]

Chapter 3

PSPICE Design

In this section each class D stage simulated using component models PSPICE design will be presented. The review of each stage will follow the description of Class D given in the theoretical analysis of Chapter 2. Thus, we will firstly see the designs for the Modulation Stage the Power Amplification Stage and the output filter.
Lastly, all the stages will be wired together in order for the final design to be simulated and assessed appropriately.

3.1 The Modulation Stage

The modulation method of choice was single sided PWM using an operational amplifier as the comparator between the input signal and a sawtooth wave. The Texas Instruments LM111 PSPICE model was used as this is a general purpose operational amplifier. The analog input signal (input V1 in the figure below) is modelled using an ideal AC source with a 1 Volt AC amplitude, 1V VAMPL and a frequency of 20k Hertz. The sawtooth generator is a pulse generator with a very low t_{fall} figure. Also, a feedback circuit is created by connecting a 4.7kOhm resistor between the output and the positive supply rail. The comparator is powered by 5 Volt supply rails

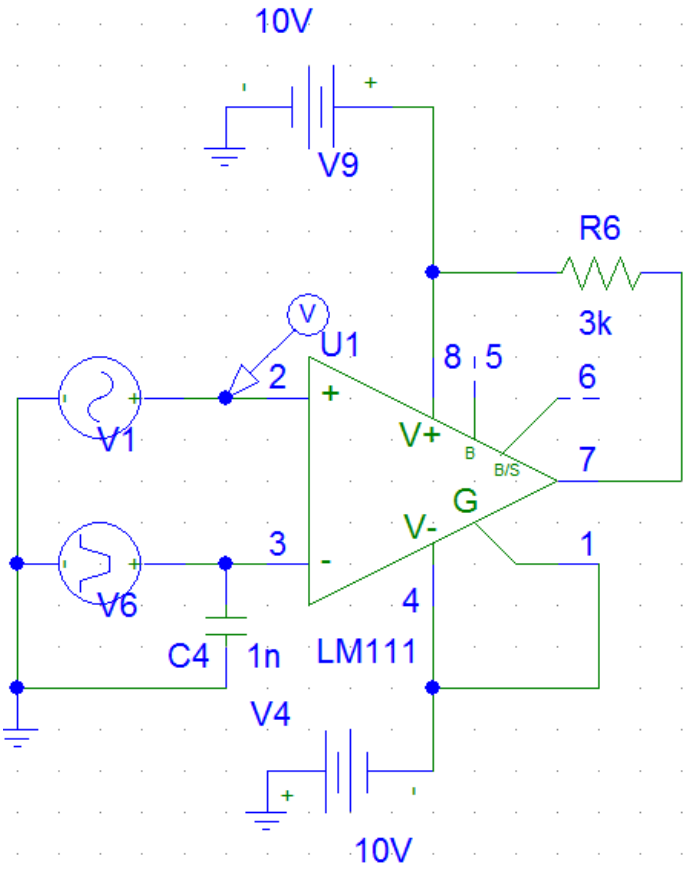


Figure 3.1 PWM implementation using ideal sources and a TI LM111 op amp

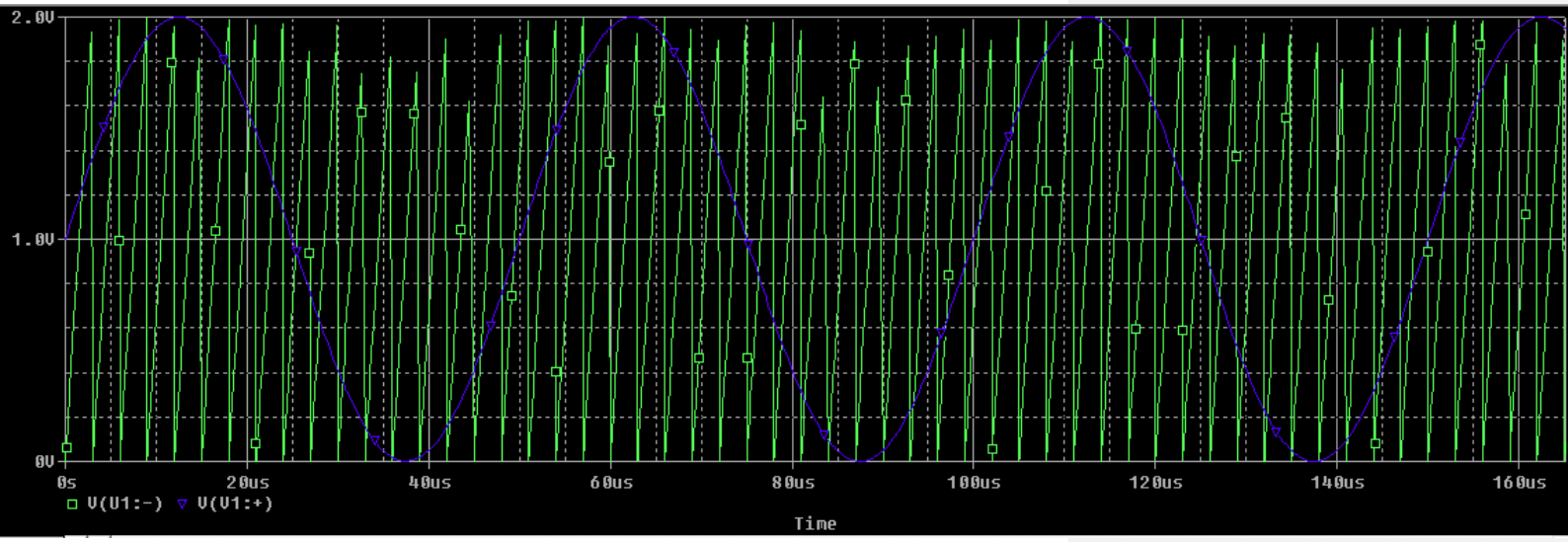


Figure 3.1 PWM

Inputs. Blue is the analog input signal and green is the sawtooth wave.

Figure 3.3 PWM output. Since the input is a perfect sine wave, the duty cycle is at 50%.

3.2 The Power Stage

The design of the power stage is a crucial factor in the efficiency of the amplifier. After reviewing the available power stage topologies in Chapter 2, half bridge was the amplification model of choice since it provided a better budget in a possible real world implementation of the circuit, even if it has a disadvantage in overall performance when compared to the H-bridge topology.

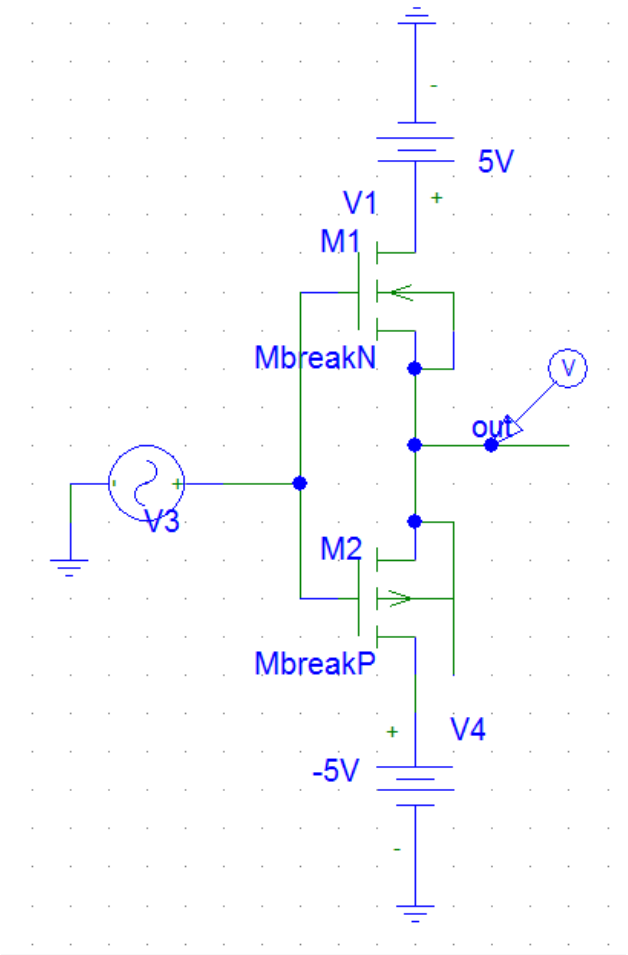


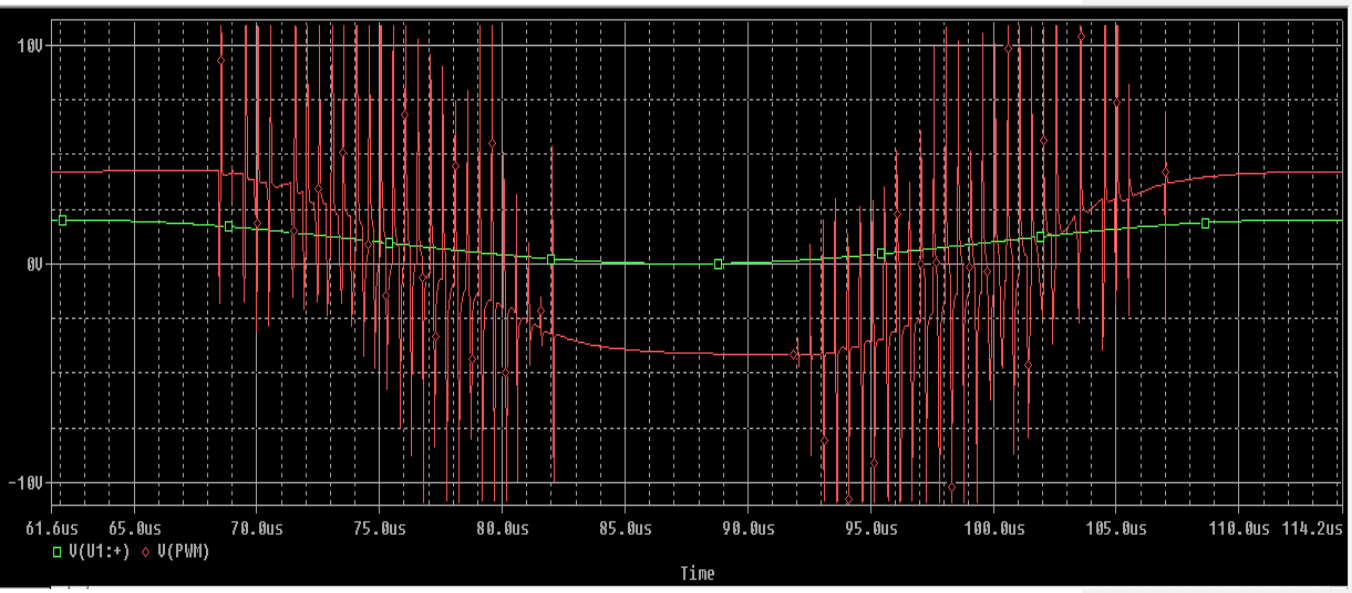
Figure 3.2 Power Stage using MOSFETs in totem pole configuration

The choice of MOSFETs for the amplification stage is also a major design decision that can rule whether the design can meet set specifications on a given power rating. Of the most important characteristics of the MOSFETs are the peak drain to source voltage the transistor can handle (V_{DSpeak}), he resistance in the drain to source (R_{DSon}), the gate capacitance (C_{GS}), the time it takes to turn on and off (t_{rise} and t_{fall}) and the voltage required to drive it.

The model characteristics in PSPICE for each MOSFET are depicted in the following table:

Model	**MbreakN-X NMOS**	**MbreakP-X PMOS**
LAMBDA	0.027	0.027
Vto	4V	-4V
KP	0.3	0.3

Commented [ND1]:



3.3 The Filter

The Design of the low pass filter will

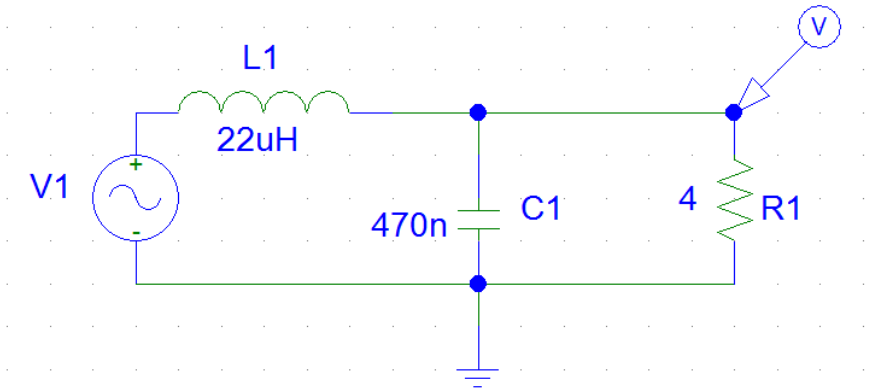


Figure 3.3 LC Filter

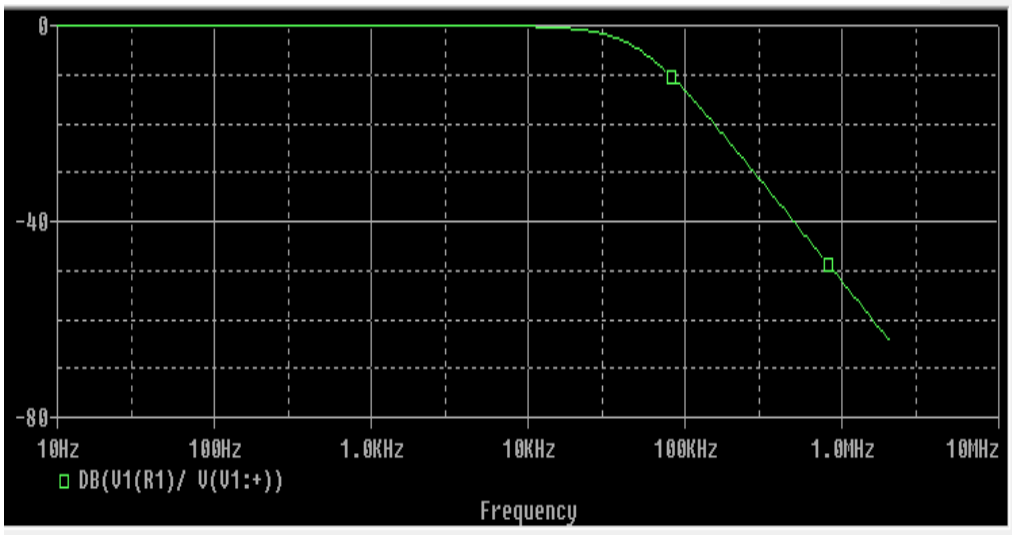


Figure 3.4 LC Filter Frequency response using a 4 Ohm Load

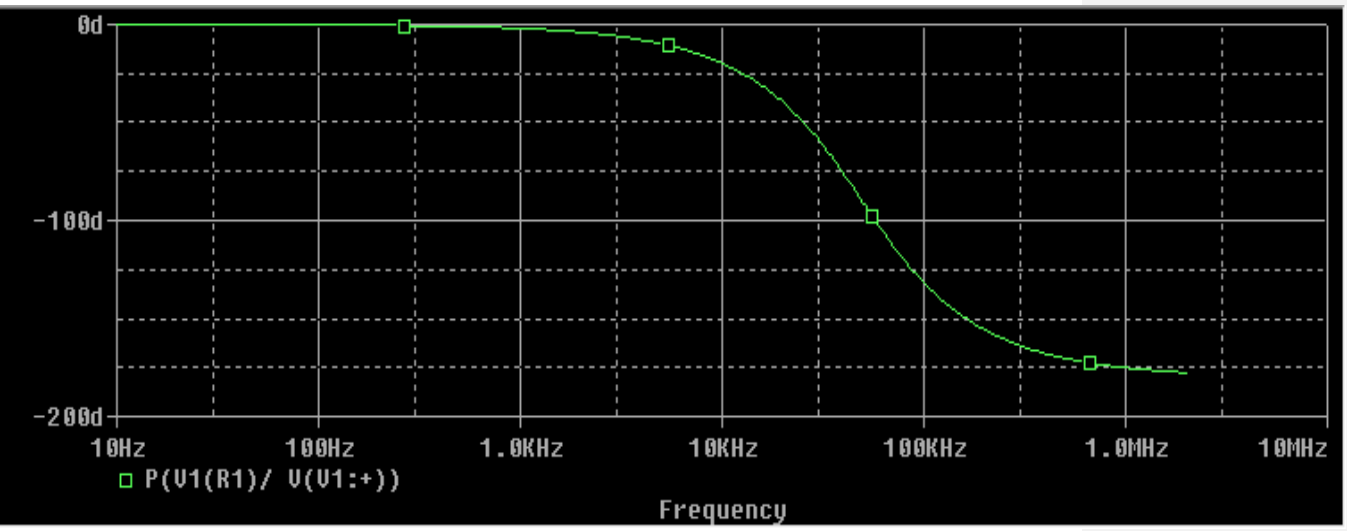


Figure 3.4 LC Filter Phase Shift on a 4 Ohm Load

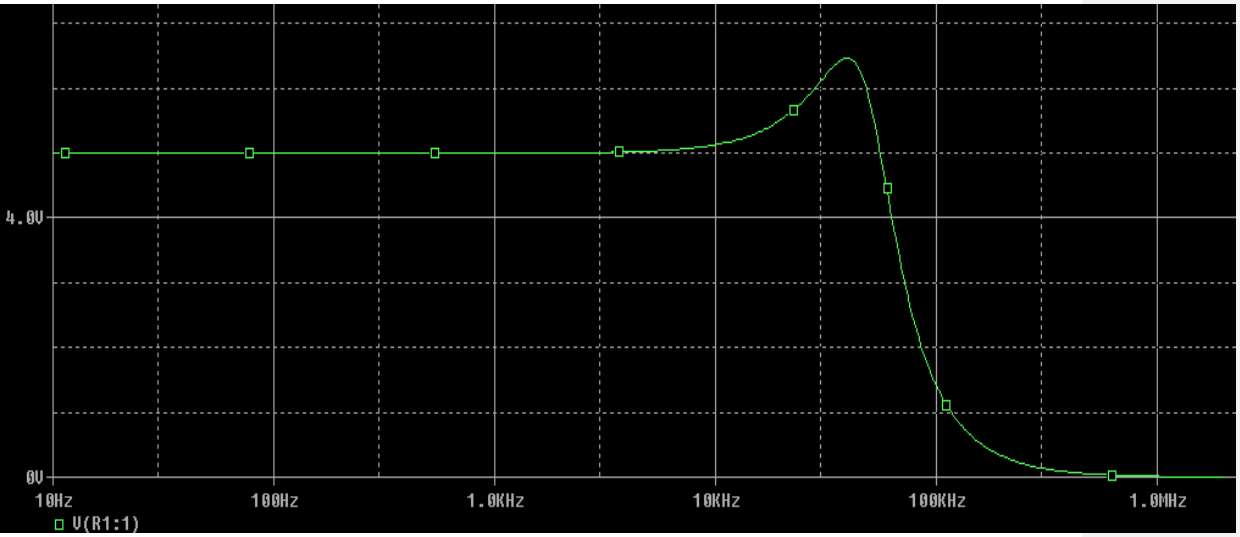


Figure 3.4 LC Filter Frequency response using a 8 Ohm Load

3.4 The Final Design

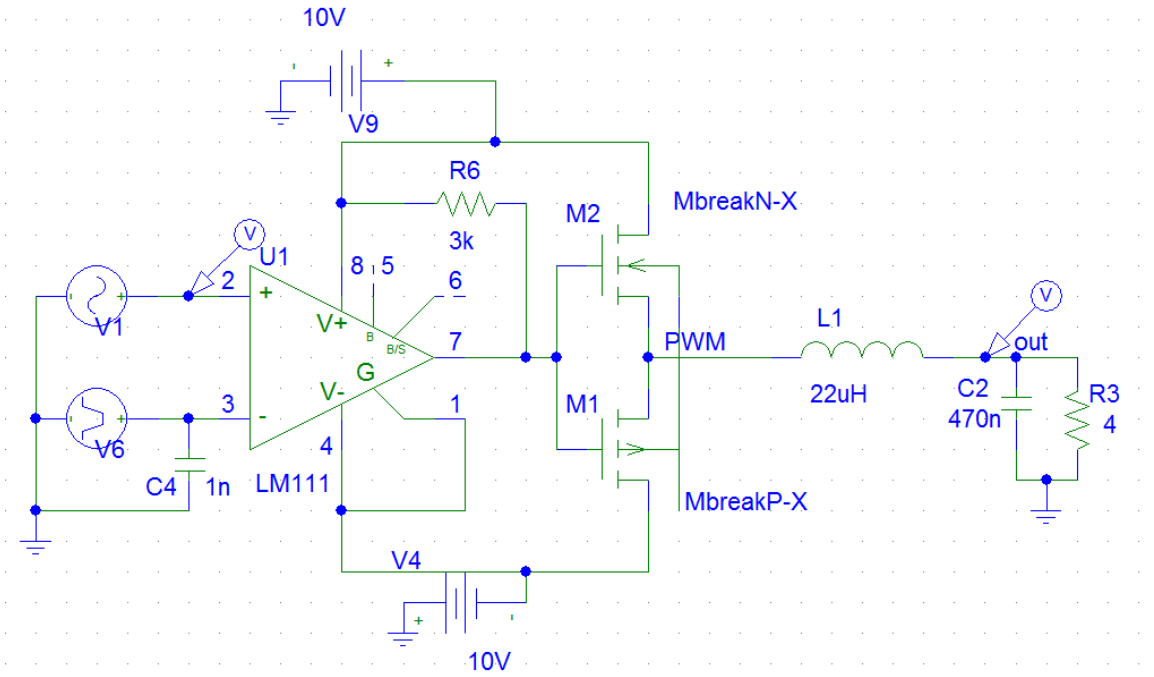


Figure 3.5 The Class D amplifier design

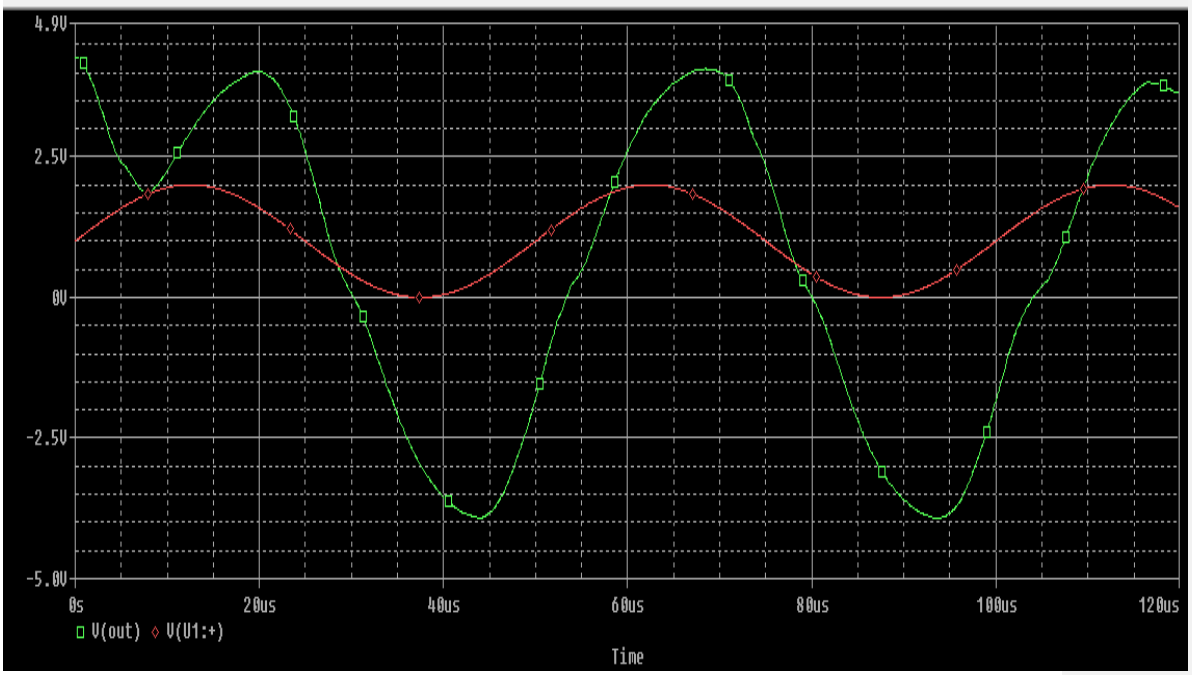


Figure 3.5 The Class D amplifier's output Voltage/time

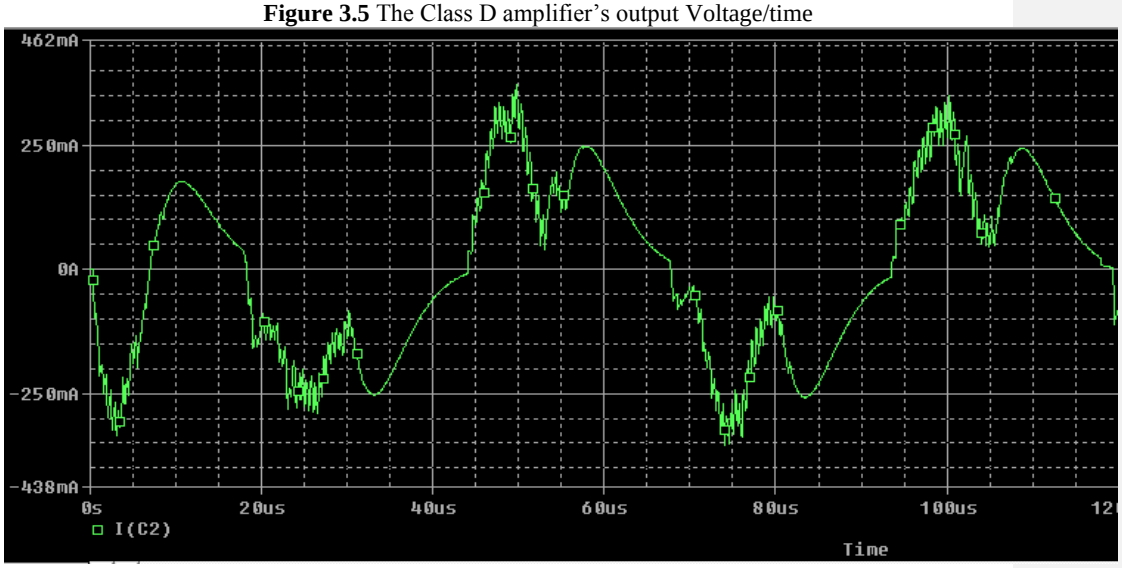


Figure 3.5 The Class D amplifier's output Current/time

Conclusions

After reviewing Class D amplification and the several implementations each stage of this topology may have, we have asserted successfully the benefits of the efficiency and low thermal print it offers. With the latest breakthroughs in MOSFET technology and theoretical analysis of PWM the audio performance of Class D amplifiers can reach THD+N figures of 0,0001% and minimal distortion rates which are competitive to state of the art class AB designs. In any case, a good Class D amplifier should be designed and taped on the circuit board with extra caution, as any misstep can cause a surge of EMI and noise.

Future work

Future implementations of the PSPICE design can include DSP chips which can make the PCB layout process easier. Also, the PWM techniques mentioned in the theoretical part can be simulated in PSPICE and compared in order to assert the best performing ones.

Glossary

AD modulation (traditional)
Modulation scheme with a differential output, where each output is 180 degrees out-of-phase and changes from ground to the supply voltage, VCC. Therefore, the differential pre-filtered output varies between positive and negative VCC, where filtered 50 percent duty cycle yields zero volts across the load. This class-D modulation scheme has the maximum differential voltage at 0 V output (50-percent duty cycle). The large differential voltage causes high peak output current, which in turn causes filter loss, thus increasing supply current and lowering efficiency. An LC filter is required with the traditional modulation scheme so the high switching current is re-circulated in the LC filter instead of being dissipated in the speaker.

BD modulation (filter-free)
Modulation scheme developed to greatly reduce or eliminate the output filter. The filter-free modulation scheme minimizes switching current, which allows a speaker to be used as the storage element in place of an LC filter and still lets the amplifier be very efficient.

BTL (bridge-tied load)
An output configuration for power amplifiers, used mainly in audio applications. The load (for example, a speaker) is connected between two amplifier outputs, bridging the two output terminals. This can double the voltage swing at the load (compared with SE amplifier operation) if the outputs are driven in opposite phases.

Efficiency
The power conversion efficiency (η_C) of the circuit at an arbitrary output power level is defined as the ratio of the average power delivered to the load to the average power drawn from the supplies.

EMI (electromagnetic radiation)
Radiation that is emitted by electrical circuits carrying rapidly changing signals, such as the outputs of a class-D audio power amplifier. EMI must be below limits set by regulatory standards such as CISPR 22 or FCC Part 15 Class B.

Gain
A specification of the insertion gain of the system typically specified in dB.

Frequency response / Bandwidth
The ability of amplifier to amplify signals over a range of frequencies, with defined source and load. Specifications are generally a –3dB bandwidth, and a tolerance on the deviation from the desired response at any frequency up to the bandwidth limit.

Harmonic distortion / Intermodulation distortion
The non-linear behavior of the amplifier causes harmonic distortion (THD) and intermodulation distortion (IMD). Moreover, the distortion will in general depend on parameters as signal level, frequency and load parameters. Distortion has to be well controlled within this parameter space. Distortion is normally specified in percentage or dB.

Noise / Signal-to-noise ratio / Dynamic range
All amplifiers have internal noise sources that contribute to the output noise. Typical specifications are the residual noise referred to the output with terminated input or the Signal-to-noise ratio relative to a given output level e.g. 1W. Also frequently used is the dynamic range, which is the relationship between the maximal RMS voltage output before clipping and the RMS of the residual noise.

Output impedance / Loading
The load impedance is generally frequency dependent with resonant peaks etc. The influences of a variable load in system frequency response should be minimized. Furthermore, the amplifier output impedance should be as low as possible to cope with variations in nominal load impedance.

Power Supply Rejection Ratio
The power amplifier has to cope with the inevitable power supply perturbations. The amplifier should be able to suppress these perturbations such that the output is not influenced. A widely used specification is the power supply rejection ratio (PSRR), which is the sensitivity of the output to perturbations on the power supply. The rejection of such perturbations has to be controlled over the complete bandwidth.

SE (single-ended)
Signaling that is the simplest method of transmitting electrical signals over wires. One wire carries a varying voltage that represents the signal, while the other wire is connected to a reference voltage, usually ground. The alternative to single-ended output configuration is the bridge-tied load (BTL) configuration. SE signaling is less expensive to implement; however the signal cannot be transmitted over long distances or quickly, it has poorer low-frequency response, and a smaller voltage swing (compared to the BTL amplifier operation).

Stability
A control system is generally required to secure robust performance for the power amplifier. This introduces a potential risk of instability. The amplifier should be prevented from instability under all circumstances, since this will generally

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