Planar Edge Terminations and Related Manufacturing Process Technology for High Power 4H-SiC Diodes

A THESIS

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by

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Notation

Symbol	Description	Unit
A^*	Richardson´s constant	A/cm^2K^2
E	Electric field	V/cm
E_C	Critical electric field	V/cm
E_M	Electric field at the Metal-Semiconductor junction	V/cm
E_F	Fermi energy level	eV
E_i	Intrinsic Fermi energy level	eV
E_A	Acceptor energy level	eV
E_D	Donor energy level	eV
E_g	Energy of the bandgap	eV
E_C	Conduction band edge	eV
E_V	Valence band edge	eV
E_{TRAP}	Traps energy level	eV
I	Current	A
J	Current density	A/cm^2
N_A	Acceptor impurity concentration	cm^{-3}
N_D	Donor impurity concentration	cm^{-3}
N_V	Valence band density of states	cm^{-3}
N_C	Conduction band density of states	cm^{-3}
Q	Charge	C
Q_F	Effective fixed oxide charge density	cm^{-2}
R	Resistance	Ω
R_{on}	Specific on-resistance	Ωcm^2
R_{SH}	Sheet resistance	Ω/□
T	Temperature	ºC or ºK
U	Recombination rate	$cm^{-3}s^{-1}$
V	Voltage	V
V_B	Breakdown voltage	V
V_{bi}	Built-in voltage	V
W	Depletion layer width	μm

Φ_B	Barrier height	eV
Φ_M	Metal work function	eV
Ψ	Surface potential	eV
χ_s	Semiconductor electron affinity	V
ρ_s	Charge density per unit volume	C/cm^{-3}
ρ	Resistivity	Ωcm
ρ_c	Contact resistivity	Ωcm^2
q	Electron charge	C
n	Ideality factor	
k_B	Boltzmann´s constant	eV/K
m_o	Electron mass	kg
m_{de}	Effective electron mass	kg
m_{dh}	Effective hole mass	kg
g	Degeneracy factor	
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
n_i	Intrinsic concentration	cm^{-3}
n	Electron free carrier concentration	cm^{-3}
p	Hole free carrier concentration	cm^{-3}
t	Thickness	µm
x_j	Junction depth	µm
v_{sat}	Saturation velocity	cm/s
τ	Carrier lifetime	s
ε_s	Semiconductor permittivity	F/cm
ε_o	Permittivity in vacuum	F/cm
λ	Thermal conductivity	W/cmK
h	Planck´s constant	eV·s

Abbreviations used

Acronym	**Meaning**
AFM	Atomic Force Microscope
BJT	Bipolar Junction Transistor
BIFET	Bipolar Injection Field Effect Transistor
BPD	Basal Plane Dislocations
CVD	Chemical Vapour Deposition
ECR	Electron Cyclotron Resonance
EMI	Electromagnetic Interference

FGR	Floating Guard Rings
FP	Field Plate
HTCVD	High Temperature Chemical Vapour Deposition
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IGBT	Insulated Gate Bipolar Transistor
JBS	Junction Barrier Diode
JFET	Junction Field Effect Transistor
JTE	Junction Termination Extension
LED	Light Emitting Diode
MEMS	Microelectromechanical Systems
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Field Effect Transistor
MPS	Merged PiN/Schottky
MS	Metal-Semiconductor
NPT	Non-punch Through
PT	Punch-Through
PVT	Physical Vapour Transport
RIE	Reactive Ion Etching
RF	Radio Frequency
RMS	Root Mean Square
RTA	Rapid Thermal Anneal
RCA	Radio Corporation of America
SB	Schottky Barrier
SBH	Schottky Barrier Height
SBD	Schottky Barrier Diode
SEM	Scanning Electron Microscopy
SiC	Silicon Carbide
SF	Stacking Faults
SIMS	Secondary Ion Mass Spectroscopy
SOA	Safe Operating Area
TEM	Transmission Electron Microscopy
TFE	Thermionic Field Emission
TLM	Transmission Line Model
XRD	X-ray Diffraction

Introduction and Thesis Outline

When semiconductor technology is discussed today, the topic is likely to involve how to increase the number or decrease the size of integrated devices on a silicon chip for a particular microelectronic application. An important but rarely mentioned field for semiconductors, however, is that of power devices. Power semiconductor devices are required whenever sending, transmitting or receiving almost any type of electrical and electromagnetic energy or signal/information. In times of escalating power consumption and increasing environmental awareness, these small electronic devices can play a big role. A large fraction of the "consumed" power never reaches the intended consumer but is lost, mainly as heat, during the transfer. By cutting these power losses there is thus a large room for power savings and reduction of the negative side effects without having to taper down on the available amount of end-user power. Since much of the losses occur within the actual power devices, an optimisation of the same would increase the consumer's yield significantly. Of large importance here is naturally the choice of semiconductor material. Silicon carbide (SiC) is a wide bandgap material that has some of the desired properties to reduce these losses. Short drift regions can be utilized without reducing the blocking voltage thanks to the extremely high electric field strength. This instantly leads to a smaller on-state voltage drop, but also a reduction in switching losses of the device due to the decreased amount of charge carriers that must be swept away after blocking. Moreover, the wide bandgap and high thermal conductivity of SiC compared to silicon allow higher current densities and higher operating temperatures of the devices. The size and complexity of power systems are significantly reduced with smaller components and reduced need for cooling systems.

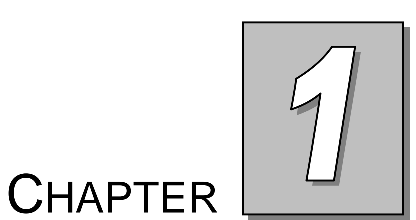
Nevertheless, today's material of choice for most applications of power electronics is still silicon. The reason is, as within many other fields of semiconductor technology, silicon's advantages of cost efficiency and process friendliness. However, substantial energy savings can thus be achieved by changing to silicon carbide and, furthermore, silicon has physical limitations that exclude the very high frequency and high power electronic applications. The properties of silicon carbide are described in more detail and discussed in relation to silicon in Chapters 1 and 2. Thereafter this thesis will deal exclusively with the 4H-SiC polytype.

Although SiC offers substantial advantages over Si, it is still immature as a semiconductor material. Single crystal wafers of SiC have only been commercially available since around 1990 and a number of critical material and processing issues are still under active investigation. In addition, certain critical fabrication processes are still under intensive research, including activation of ion implanted impurities, thermal oxidation of high quality dielectric films suitable for MOS devices, formation of thermally stable ohmic and Schottky contacts and reliable and controllable etching techniques. However, new breakthroughs in the fields of material growth and of technological processes have been proposed recently, which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers (4") is now possible, allowing the fabrication of reliable and high current power devices. Concerning technology, new gate dielectric growth with improved channel mobility have been demonstrated, opening the way to MOSFET technology in SiC.

This thesis concerns the design, process integration, fabrication and evaluation of PiN, JBS and Schottky rectifiers in SiC. A process sequence has been developed based on the available silicon process technology in the CNM cleanroom environment. As the material technology continues to improve, the role of SiC power device design is becoming more important. Specifically, to fully exploit the high reverse blocking capabilities of SiC, proper device edge termination is required to alleviate the device from the well known field crowding effect at the main junction edge that significantly decreases the theoretical one-dimensional breakdown voltage. Thus, one principal aim of this thesis is the design and development of high efficient edge terminations for high power planar SiC diodes. In Chapter 2, it will be presented the design and optimisation of various edge termination techniques using specific 4H-SiC calibrated numerical simulations. Main attention will be focused on junction termination extension techniques (JTE), and a novel edge termination structure namely "Floating guard rings assisted JTE" will be presented with great blocking performances.

Characterisation and analysis of the main processes involved in the fabrication of our high power diodes will be reported in Chapter 3, including ion implantation, activation annealing and contact formation. The obtained results are directly applicable and focus on important

problems in the fabrication of SiC power devices. Chapter 4 will demonstrate the high blocking efficiency on fabricated diodes of our previously designed edge terminations, specially that of the novel developed structure, and an analysis of the breakdown behaviour will be reported. Moreover, we will also analyse second order design parameters, which are not usually considered but clearly important as our results will shown. Finally, Chapter 5 will cover the current-voltage performance at high temperature operation, up to 300ºC, of the three different fabricated power rectifiers: PiN, JBS and Schottky.

CHAPTER 

Silicon Carbide: Properties and Progress

This chapter will describe the basic properties of SiC, and show the advantages of using SiC over other semiconductor materials. First an historical background will be detailed giving an overview of the progress and actual SiC material and technology status. The main part of the chapter covers the material properties focusing on the electrical ones relevant for electronic devices. Finally, an overview of the characteristics and the state-of-the-art in high power silicon carbide rectifiers and power switches will conclude this chapter.

1.1 Historical Background

Silicon carbide is the only stable compound in the Si-C equilibrium system at atmospheric pressure. SiC was first observed in 1824 by Jöns Berzelius [1]. The properties and potential of the material were, of course, not understood at the time. The growth of polycrystalline SiC with an electric smelting furnace was introduced by Eugene Acheson around 1885. He was also the first to recognize it as a silicide of carbon and gave it the chemical formula SiC. The only occurrence of SiC in nature is found in meteorites. Therefore, SiC cannot be mined but must be manufactured with elaborate furnace techniques.

In its polycrystalline forms, silicon carbide has long been a well proven material in high-temperature, high-strength and abrasion resistant applications. Silicon carbide as a semiconductor is a more recent discovery. In 1955, Jan Antony Lely [2] proposed a new method for growing high quality crystals which still bears his name. From this point on, the interest in SiC as an electronic material slowly began to gather momentum; the first SiC conference was held in Boston in 1958. During the 60´s and 70´s SiC was mainly studied in the former Soviet Union.

Year 1978 saw a major step in the development of SiC, the use of a seeded sublimation growth technique also known as the modified Lely technique [3]. This breakthrough led to the possibility for true bulk crystal preparation. The first blue LED was fabricated already in 1979 and in 1987, Cree Research Inc., the first commercial supplier of SiC substrates [4], was

founded. Today, there are a few companies and many active research groups in the field, but SiC industrially still remains a small business. In the beginning, the SiC industry was concentrated around the blue LEDs that are impossible to manufacture using conventional silicon technology. The potential of power electronics industry is much larger and its interest has grown in recent years as the progress of silicon devices have began to stagger. This also explains the rapidly increasing research on SiC growth. Figure 1.1 shows a curious symbolic representation of the evolution of semiconductors.

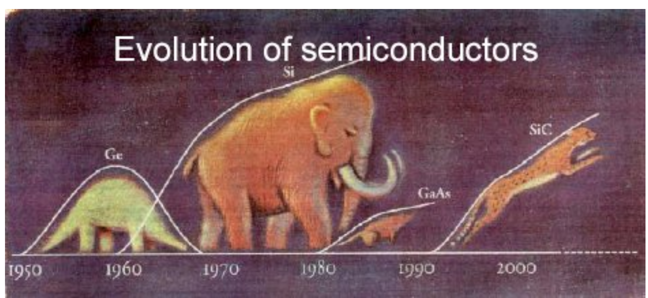


Figure 1.1 Symbolic graph of the historical evolution of semiconductors.

1.2 Material Properties

1.2.1 Crystal structure

Silicon carbide occurs in many different crystal structures, called polytypes. The crystal structure of silicon carbide is based on a lattice in which carbon and silicon atoms are alternated; in Fig 1.2 one carbon atom with four silicon atoms in tetrahedral arrangement is represented. The distance between two first neighbour Si atoms and two first neighbour Si-C atoms are 3.08Å and 1.89Å, respectively.

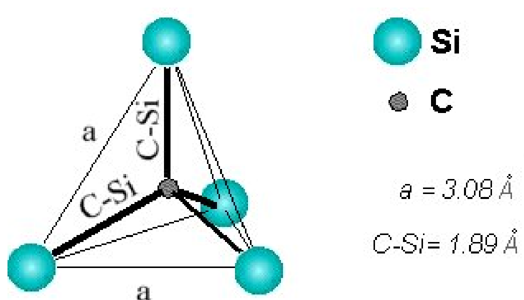


Figure 1.2 Tetrahedral arrangement of a C atom surrounded by four Si first neighbours.

Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical semiconductor properties. While there are over 200 known polytypes of SiC, only a few are

commonly grown in a reproducible form acceptable for use as an electronic semiconductor. With the aim to distinguish different polytypes, the Ramsdell notation is commonly used [5], in this case the first number indicates crystalline planes, called with A, B, C letters as shown in Fig 1.3, and the following letter indicates Bravais cell type: cubic (C), hexagonal (H) or rhombohedral (R). The most common polytypes of SiC presently being developed for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. 3C-SiC is the only form of SiC with a cubic crystal lattice structure. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with hexagonal crystal structure. Similarly, 15R-SiC is the most common of many possible SiC polytypes with a rhombohedral crystal structure.

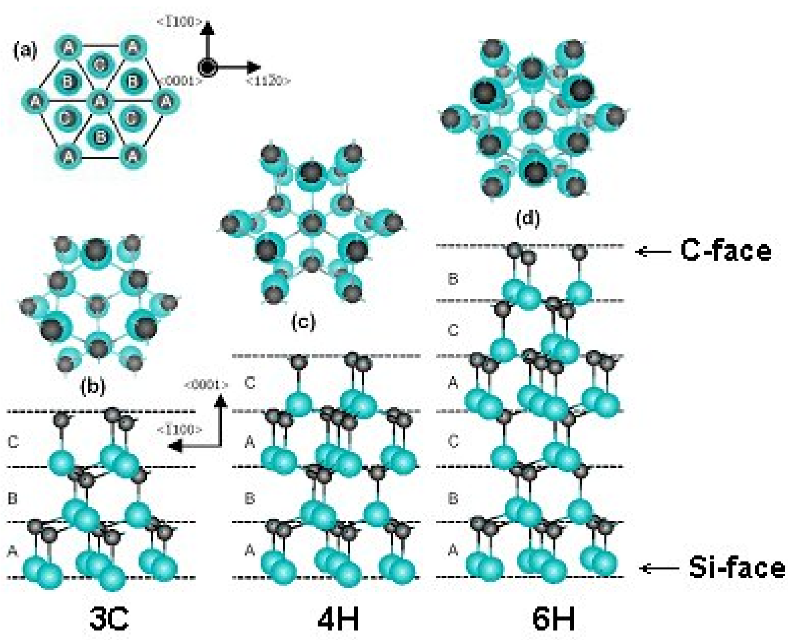


Figure 1.3 The different order of stacking in SiC is shown: (a) the position of the first layer of atoms of Si and C is illustrated as A whereas the next layers can be shown as B and C. The top- and side-view of 3C-, 4H-, and 6H-polytype stacks are shown in (b), (c), and (d), respectively.

Because some important electrical device properties are non-isotropic with respect to crystal orientation, lattice site, and surface polarity, some further understanding of SiC crystal structure and terminology is necessary. Different polytypes of SiC are actually composed of different stacking sequences of Si-C bilayers (also called Si-C double layers), where each single Si-C bilayer can simplistically be viewed as a planar sheet of silicon atoms coupled with a planar sheet of carbon atoms. The plane formed by a bilayer sheet of Si and C atoms is known as the basal plane, while the crystallographic *c*-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to Si-C bilayer plane. Figure 1.3 schematically depicts the stacking sequence of 3C, 4H and 6H SiC polytypes. As an example, it can be clearly seen that the 6H-SiC polytype requires six Si-C bilayers to define the unit cell repeat distance along the *c*-axis [0001] direction. The $[\bar{1}100]$ direction depicted in Fig. 1.3 is

often referred to as the *a*-axis direction. SiC is a polar semiconductor across the *c*-axis, in that one surface normal to the *c*-axis is terminated with 4 silicon atoms while the opposite normal *c*-axis surface is terminated with carbon atoms. As shown in Figure 1.3, these surfaces are typically referred to as “silicon face” and “carbon face” surfaces, respectively.

Silicon carbide bulk material is generally cut and polished perpendicularly to the *c*-axis (or 3-8° slightly off-axis towards $\langle 11\bar{2}0 \rangle$ for better epitaxial layer quality). This means that either the (0001) silicon face or the $(000\bar{1})$ carbon face will be polished before growth of epitaxial layers and/or device fabrication. The difference between the two faces is surprisingly large, and it is important to keep track of which face is being used in the experiments. For instance, the oxidation rate is several times larger on the carbon face and contact properties like the barrier height can vary too. The silicon face is commonly used for devices, since epitaxial growth has been more successful on this face.

1.2.2 Crystal Imperfections

Deviations from the perfect crystal lattice are commonly called *defects*. In the scope of this thesis it is important to distinguish between three major classes of defects always present in the currently available silicon carbide material:

Point defects — “Misplaced” single atoms or smaller clusters of atoms in the lattice. These can be intrinsic points defects such as silicon and carbon vacancies and intersticials, or silicon on carbon lattice sites, and viceversa. Also intentionally introduced dopant atoms, such as N, P, Al and B, and unintentional impurities like H or O, are point defects in the lattice.

Dislocations — The crystal lattice is distorted along a dislocation line while the periodicity of the lattice is not affected. Dislocation lines can only be bound by larger defects, voids or inclusions in the crystal or by the crystal surface. In [0001]-oriented SiC screw dislocations and threading edges dislocations parallel to the *c*-axis of the crystal can penetrate whole wafers and epitaxial layers.

Screw dislocations are present in state-of-the-art silicon carbide material in densities in excess of 10^4cm^{-2}. The amount of distortion along the direction of the dislocation line is given by the length of the Burgers vector B. In the case of pure screw dislocations the Burgers vector is parallel to the *c*-axis of the silicon carbide crystal and the length of the Burgers vector corresponds to the step height of the screw dislocation. It was found that all screw dislocations with $B>3c$ form an open core or a pinhole along the dislocation line. This is explained by the surface free energy according to Frank´s theory [6]. Screw dislocations with hollow core are called *micropipes* and are found in densities of 10^{-1}-10^2cm^{-2} in state-of-the-art epitaxial layers and substrates.

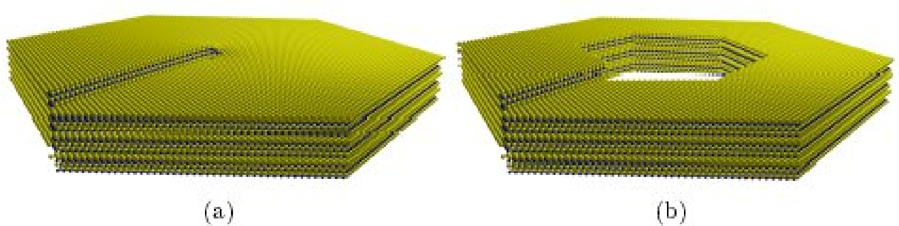
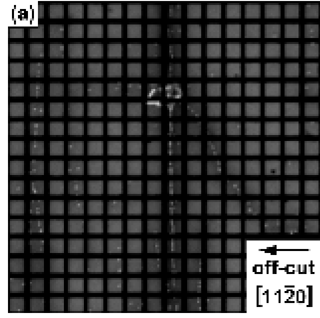


Figure 1.4 Illustration of (a) a closed-core and (b) an open-core screw dislocation with a Burgers vector B=1c in the crystal lattice of 4H-SiC.

Along with the progress in material growth, the densities of micropipes has been reduced by at least two orders of magnitude during recent years, due to a massive research effort. However, the disappearance of micropipes revealed the influence of other crystal defects on device performance.

Stacking Faults — The periodicity of the stacking sequence is broken along a lattice plane. Below and above of this plane, the crystal shows the full periodicity of the crystal lattice of the corresponding polytype. Recently the presence of stacking faults in the active volume of silicon carbide devices has attracted the attention of a number of research institutes worldwide. It was observed that an increase in the forward voltage drop and thus in the power loss of *PiN* diodes was correlated with the appearance of stacking faults in the hexagonal stacking sequence of the typically used 4H-SiC polytype. Calculations have shown [7] that the stacking fault can form a 2-dimensional quantum well, reducing the effective carrier lifetimes in the active region. Stacking faults can be introduced into the epitaxial silicon carbide layers during growth, where they originate at imperfections at the substrate-epilayer interface, during oxidation [8] and during device operation in the presence of dense electron-hole plasmas in the drift region of bipolar devices, as it is shown in Figure 1.5.



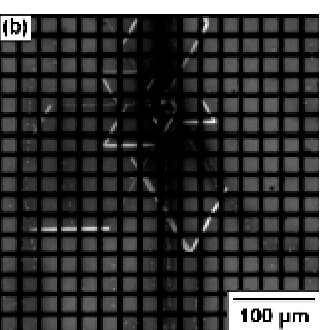


Figure 1.5 Plan-view optical emission microscopy images showing a simultaneous development of various rhombic stacking faults in a 4H-SiC *p-i-n* diode: (a) the "virgin" diode before degradation showing the pre-existent dislocations in the blocking layer. The 8º off-cut toward the [1120] direction is marked with an arrow; (b) the same area after 5 min of biasing at 50 A/cm^2. Numerous wedge-shaped bright lines emanated from a point source corresponding to rhomb-shaped Shockley-type stacking faults in basal planes. (Images taken from the work of S. Ha *et.al.* [9]).

1.2.3 Electrical properties

Silicon Carbide belongs to a class of materials commonly referred to as *wide-bandgap* semiconductors. This means that the energy gap between the valence and conduction band is significantly larger than in silicon. It implies, for example, that it is less probable that thermally excited electrons would jump over the gap. Therefore SiC devices are less sensitive to high temperatures and should be able to operate at temperatures exceeding 500ºC.

Because of its high bond strength and hardness, SiC is physically rugged and chemically inert. The crystal structure will influence the band structures, manifesting itself in the electrical characteristics of the polytypes through the density of states and phonon dispersion. Material properties like the bandgap energy varies from 2.2 to 3.3eV for the different polytypes. The ionisation energy levels of the dopants are also different, and fairly deep, leading to incomplete ionisation of dopants at room temperature. Most striking is the varying anisotropy of the polytypes of silicon carbide; only the cubic 3C structure has completely isotropic bulk properties. Among several SiC polytypes, 4H-SiC is the most attractive one due to the higher carrier mobility and more isotropic nature of its properties. Some of the electrical properties of the most common silicon carbide polytypes compared to some other semiconductors are listed in Table 1.1. Silicon and gallium arsenide (GaAs) are the traditional semiconductors. Gallium nitride (GaN) and diamond are, like SiC, wide bandgap materials also considered as future power semiconductor materials.

Table 1.1 Comparison of electrical properties for the traditional power semiconductor materials Si and GaAs and the wide bandgap semiconductors SiC, GaN and diamond.

Property at T=300K	Silicon	GaAs	3C-SiC	4H-SiC	6H-SiC	GaN	Diamond
E_g (eV)	1.12	1.42	2.3	3.26	2.96	3.4	5.45
n_i (cm^{-3})	1.5×10^{10}	2.1×10^{6}	6.9	8.2×10^{-9}	2.3×10^{-6}	1.6×10^{-10}	1.6×10^{-27}
m_n (cm^2/V·s)*	1200	6500	750	//c:950 ⊥c:800	//c:85 ⊥c:400	1000	1900
m_p (cm^2/V·s)*	420	320	40	115	90	30	1600
n_{sat} (cm/s)	1×10^{7}	2×10^{7}	2.5×10^{7}	2×10^{7}	2×10^{7}	2.5×10^{7}	2.7×10^{7}
E_C (MV/cm)**	0.2	0.4	2	2.5	2.4	3.3	5.6
l (W/cm·K)	1.5	0.5	4.9	4.9	4.9	1.3	20
ε_r	11.8	12.8	9.6	10	9.7	8.9	5.5

* for $N_D=1\times10^{16}cm^{-3}$; **for $N_D=1\times10^{17}cm^{-3}$

The intrinsic carrier concentration n_i is determined by the fundamental energy gap E_g and the effective density of states N_C and N_V in the conduction and valence bands, respectively. Neglecting bandgap narrowing, the intrinsic carrier concentration is defined as:

$$n_i(T) = \sqrt{N_C N_V}\, exp\left(-\frac{E_g}{2k_B T}\right) \tag{1.1}$$

Figure 1.5 shows the temperature dependence of the intrinsic carrier concentration for the 4H and 6H-SiC polytypes in comparison to silicon. The horizontal line shows the temperature where devices may stop working since n_i exceeds the background doping concentration (e.g. typically 10^{14}cm^{-3} for the low-doped region of power devices). As it can be observed, thanks to its wide bandgap, SiC has an intrinsic temperature over 1000ºC (depending on polytype and doping).

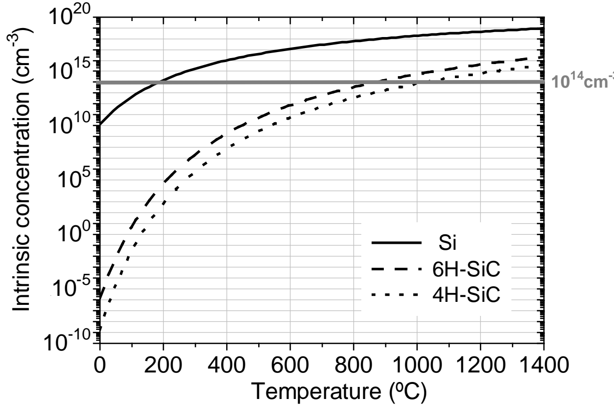


Figure 1.5 Intrinsic carrier concentration dependence on temperature for the silicon and the two most common SiC polytypes.

As SiC has a critical electric field around ten times higher than that of Si, the breakdown voltage given by:

$$V_B = \frac{E_C W}{2} \tag{1.2}$$

can be ten times higher for the same depletion width (*W*). Similarly, for the same breakdown voltage design, a 10 times thinner depletion region or 100 times higher doping level in the low-doped region of a *pn* junction can be realized in SiC. As a result, a simple calculation of the unipolar on-resistance;

$$R_{on} = \frac{W}{q\mathbf{m}_n N_D} = \frac{4V_B^2}{\mathbf{e}\mathbf{m}_n E_C^3} \tag{1.3}$$

for the low-doped region gives 1000 times lower values by using a 10 times thinner depletion region and 100 times higher doping (see Fig. 1.6). However, in the actual case the electron mobility $\mathbf{m}_n$ and dielectric constant $\mathbf{e}$ are lower in SiC than in Si, and the advantage is between 200 and 400 depending on the polytype.

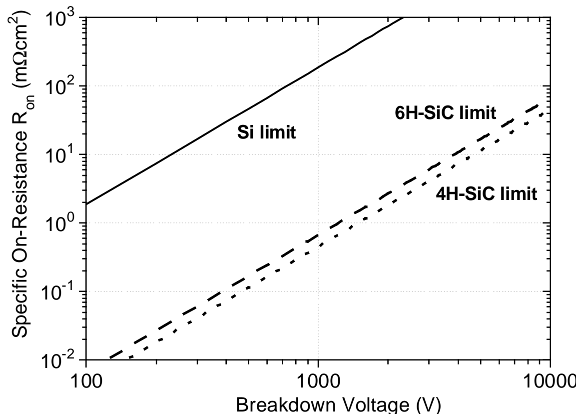


Figure 1.6 On-resistance versus breakdown voltage V_B for Si, 6H-SiC and 4H-SiC blocking layers. The substrate contribution to the overall device on-resistance is not taken into account.

Moreover, high frequency SiC devices can exhibit better performance than in Si due to the higher saturated drift velocity v_{sat} and lower permittivity *e*. In principle, the high thermal conductivity λ of SiC allows higher power densities as compared to Si and GaAs. A higher thermal flow (*P/A*, where *P* is the power dissipation and *A* is the area normal to heat flow) can be provided for the same amount of junction temperature increase.

The most beneficial inherent material superiorities of SiC over silicon listed in Table 1.1 are its exceptionally high breakdown electric field, wide bandgap energy, high thermal conductivity and high carrier saturation velocity. These properties are thus desirable for efficient high power, high temperature and high frequency device operation in harsh environments. The electrical device performance benefits that each of these properties enable are discussed in the next section, as are system-level benefits enable by improved SiC devices.

1.2.4 Applications and benefits of SiC electronics

Recent development advances have caused Si semiconductor technology to approach theoretical material limits; however, power device requirements for many applications have changed to the point where Si based power devices cannot meet them. The requirements include higher blocking voltages, switching frequencies, efficiency, and reliability. Therefore, new semiconductor materials for power device applications are needed.

However, it is already proven that even the first SiC semiconductor-based power devices surpass Si's theoretical limits. SiC semiconductor power devices, with their superior characteristics, offer great performance improvements and can work in harsh environments where Si power devices cannot function. Some of the advantages compared with Si based power devices are as follows:

- SiC semiconductor-based unipolar devices are thinner and have lower on-resistances. Lower R_{on} also means lower conduction losses; therefore, higher overall converter efficiency is attainable.

- SiC semiconductor-based power devices have higher breakdown voltages because of their higher electric breakdown field; thus, while Si Schottky diodes are commercially available typically at voltages lower than 300 V, the first commercial SiC Schottky diodes are already rated at 600V and 1200V.

- SiC devices have a higher thermal conductivity (4.9 W/cm·K for SiC, as opposed to 1.5 W/cm·K for Si). Therefore, SiC-based power devices have a lower junction-to-case thermal resistance. This means heat is more easily transferred out of the device, and thus the device temperature increase is slower.

- SiC semiconductor-based power devices can operate at high temperatures. The literature notes operation of SiC devices up to 600°C. Si devices, on the other hand, can operate at a maximum junction temperature of only 200°C.

- Forward and reverse characteristics of SiC semiconductor-based power devices vary only slightly with temperature and time; therefore, they are more reliable.

- SiC semiconductor-based bipolar devices have excellent reverse recovery characteristics. With less reverse recovery current, switching losses and electromagnetic interference (EMI) are reduced, and there is less or no need for snubbers. As a result, there is no need to use soft-switching techniques to reduce switching losses.

- Because of low switching losses, SiC semiconductor-based devices can operate at higher frequencies (>20 kHz) not possible with Si-based devices in power levels of more than a few tens of kilowatts. Higher switching frequency in power converters is highly desirable because it permits use of smaller capacitors, inductors, and transformers, which in turn can reduce overall system size and weight.

- While the smaller on-resistance and faster switching of SiC help minimize energy loss and heat generation, the higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient, the ability of SiC to operate at high junction temperatures permits much more efficient cooling to take place, so that heatsinks and other device-cooling hardware

(i.e. fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high power devices from overheating can be made much smaller or even eliminated.

- The high breakdown voltage and high thermal conductivity coupled with the high carrier saturation velocity allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite the disadvantage in low-field carrier mobility of SiC. The high power density reduces the number of devices required to generate large total RF powers needed for fixed-base high-power RF transmission applications, thus minimizing RF matching difficulties and cooling requirements to reduce the overall system size and cost.

Uncooled operation at high-temperature and/or high-power SiC electronics would enable revolutionary improvements in aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed "smart" electromechanical controls and sensors capable of harsh-ambient operation will lead to substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability. SiC high power solid-state switches will also afford large efficiency gains in electric power management and control. Performance gains from SiC electronics could enable the public power grid to meet the increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through "smart" power management. More efficient electric motor drives, enabled by improved SiC power devices, will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses.

Although SiC semiconductor-based power devices have these advantages compared with Si, the present disadvantages limit their widespread use. Some of these disadvantages are:

- Low processing yield because of defects density in SiC wafers.
- High cost; (7$ for a 600V- 4A SiC Schottky diode, while a similar Si *PiN* diode is <<1$).
- Limited availability, since only SiC Schottky diodes and MESFETs at relatively low power are commercially available; and
- The need for high-temperature packaging techniques that have not yet been developed.

These drawbacks are to be expected, given that SiC semiconductor technology has not yet matured.

1.3 Silicon Carbide Technology: State-of-the-art

1.3.1 Silicon carbide substrate and epitaxial growth

The availability of high purity and defect free on large area wafers is of vital importance for the industrial development. The feasibility to produce low cost, high volume large area Si wafers has been one of the main reasons for its success and domination in the microelectronic applications. Currently SiC has not reached yet the performances of Si in terms of material quality but recent breakthrough should be a step forward allowing the fully industrialization of SiC devices and systems. Today, the main polytype of SiC produced is the 4H polytype due to its superior carrier mobility and critical electric field. The main techniques currently used to grow SiC are based on vapour phase growth techniques, such as sublimation (PVT) and Chemical Vapor Deposition (CVD), for both bulk SiC and epilayers. Concerning bulk growth, the Lely modified technique based on the sublimation of SiC at temperatures higher than 2000ºC is used by the main SiC substrate providers from USA (CREE), Japan (Sixon) and Europe (SiCrystal). The growth rate is in the range of few mm/hour. Currently the standard commercially available wafer size is 3 inches. It is widely considered by the device manufacturers that 4 inches is the minimum wafer diameter to manufacture industrially viable devices. Up to date 4 inches wafers have been demonstrated with high quality and low defects density. Micropipes are the main device killer defects in the SiC substrates, and the micropipe density is the main parameter limiting the size of the microelectronic devices. Micropipe densities lower than 5 $\mu p/cm^2$ on 3 inches commercial wafers have been obtained. Micropipes densities lower than 1 $\mu p/cm^2$ have been demonstrated and are expected in the market very soon.

Other defects however are also present in the SiC crystal such a dislocations (500-1000cm^{-2}) and stacking faults, which are particularly prejudicial for bipolar device fabrication [9]. Then, other approaches can be used for SiC bulk growth. In the case of semi-insulating substrates used especially for RF devices, wafers grown by means of a high temperature CVD (HTCVD) process [10] have shown better characteristics than the Lely modified wafers since the purity of the starting material is higher, resulting in a lower residual doping. The HTCVD technique can also be used for N^+ or P^+ substrate growth but it has not provided superior characteristics than the conventional method. Recently CVD has been also used by Hoya to grow 3C bulk material.

Nevertheless, the main breakthrough in bulk growth was proposed in 2004 by Toyota/Denso [11]. This process, known as *Repeated a-face growth process (RAF),* allows obtaining micropipe free 4H-SiC substrates with a very low density of dislocations. The concept is based on the sequential growth of the substrate along 3 different orientations. It was shown that SiC growth along the a-face reduces significantly the micropipe density.

However, for device fabrication, a *c*-face grown material provides better electrical results. Consequently, this new process combines both aspects, a first growing perpendicular to the a-face axis and then to the *c*-face axis, as depicted in Fig. 1.7 [11]. The last growth step is performed on the standard *c*-face taking profit of the defect free material obtained from the two previous steps. The commercial availability of this novel material at a reasonable cost should definitively boost the SiC devices production. The main remaining question is the industrialization of this process for mass production.

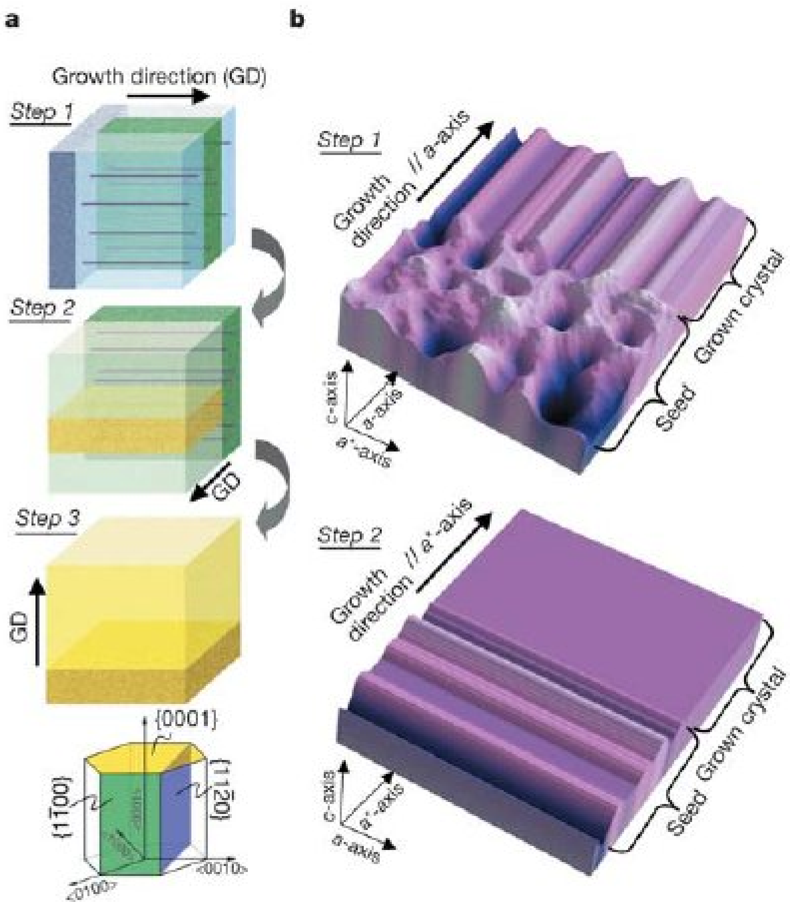


Figure 1.7 Schematic illustrations of "repeated a-face" (RAF) growth process. The growth sequences are as follows. Step 1: first *a*-face growth (seed and grown crystal are shown dark blue and light blue, respectively). Step 2: second *a*-face growth perpendicular to the first *a*-face growth (seed sliced from first a-face growth crystal, and the grown crystal are shown dark green and light green, respectively). Step 3: *c*-face growth with offset angle of several degrees (seed sliced from second *a*-face growth crystal, and the grown crystal are shown dark yellow and light yellow, respectively). At the bottom of panel **a)** are shown the major crystallographic axes and lattice planes in the RAF process.

In addition to the continuous improvement of wafer diameter and defect density, several challenges remain in the SiC bulk growth technology. The first one is the absence of highly doped low defects P^+ substrates. These substrates are necessary for several applications such as power IGBTs (Insulated Gate Bipolar Transistor). The second one is the impossibility up to now to obtain low doped N- substrate, which also have a lot of applications in the fields of

power devices and radiation detectors. Another need is the availability of Silicon Carbide on Insulator. Several tentatives have been done to growth by CVD 3C-SiC on Si and SiO_2/Si substrates. The high lattice mismatching between SiC and Si results in highly defective SiC layers. The best solution proposed up to now seems to be the SMARTCUT© technique patented by SOITEC [12]. This technology allow to bond 3C or 4H SiC thin layers on different type of substrates such as SiO_2/Si (SiCOI) or even on metallized Si substrates. Moreover, the resulting cost of this technique is lower than the bulk growth of 4H-SiC.

Concerning epilayer growth, CVD is the more stable, reliable and extended technique today. The main limitation of CVD is its low growth rate, a few um per hours, resulting in a high cost of thick (>10um) epilayer production. Since many application for power electronics require 3KV-20KV voltage rated devices, epilayers with thickness range from 30μm to 200μm are needed as starting material. The cost of CVD epi growth results very high in this case. This is why other techniques, such as sublimation are also studied to increases the growth rate of SiC epilayers. Growth rates of 100um/hours can be achieved. Sublimation epitaxy also allow a reduction of defect density of the starting substrate. However, the main disadvantage is that this technique is intrinsically more susceptible to chemical contamination than CVD, leading to higher residual doping and compensation phenomena.

1.3.2 Doping

The dopants introduced during *in situ* SiC PVT epitaxial growth are aluminum and boron for p-type and nitrogen and phosphorus for n-type, with trimethylaluminum ($(CH_3)_3Al$), diborate (B_2H_6), nitrogen gas (N_2), and phosphine (PH_3), as the most common dopant precursors. The precursors are all gases, except trimethylaluminum, which is a liquid, and delivered into the reactor from a bubbler by using hydrogen as a carrier gas. In order to obtain high resistivity or semi-insulating material vanadium can be added.

As p-type dopant, aluminum is the most frequently used. It has a low diffusivity in SiC over the temperature range of interest, high incorporation efficiency and, compared to boron, lower acceptor ionisation energy (see Table 1.2). The incorporation is almost linear to the flow of trimethylaluminum and a maximum doping level of about $2\times10^{20}cm^{-3}$ can be reached. Boron is less used, partly due to its higher acceptor ionisation energy and lower solubility in SiC. Boron also has a higher diffusivity than aluminum, and a tendency to stick to the reactor walls, and subsequently evaporate. Both of these effects lead to non-abrupt doping profiles.

Table 1.2 Ionisation energies of the most common impurities in 4H- and 6H-SiC.

Type	Dopant	Ionisation energy (meV)	
		4H-SiC	6H-SiC
n (donors)	N	42 (hex), 82 (cub)	82 (hex),137 (cub)
	P	53 (hex), 93 (cub)	82 (hex),115 (cub)
p (acceptors)	B	300	310
	Al	190	225
	Ga	281	290

As n-type dopant, nitrogen is preferred to phosphorus, even though the acceptor ionisation energy is practically the same for both. The incorporation of nitrogen from N_2 is a thermally limited process, even at the growth temperatures, due to the high dissociation energy of the gas. The dopant incorporation is proportional to the N_2 flow, and saturates at around $1\times10^{20}cm^{-3}$. The vapour pressure of phosphorus is extremely high at the growth temperature, which reduces the incorporation probability two orders of magnitude below that of nitrogen. In addition, phosphine is a highly toxic precursor, and should thus be avoided, if possible. The lowest background doping levels obtained are in the low $10^{14}cm^{-3}$ range.

The dopants are incorporated into Si or C lattice site. A large dopant atom will preferably replace the larger Si atom in order not to distort the lattice. Aluminum and phosphorus, both with an equivalent covalent radius comparable to that of silicon are hence regularly incorporated into Si lattice sites. Dopants with smaller diameters can be incorporated into either lattice site, without disturbing the lattice, which is the case of nitrogen. On the other hand, boron seems to be incorporated into the Si site only. This can be understood from the fact that hydrogen is incorporated together with boron, forming a B-H complex, too large to fit into a C site. The hydrogen incorporated in the lattice together with boron has been found to passivate the boron acceptor. Probably this is achieved by hindering the transfer of an electron from a carbon, to the boron atom. A similar, but weaker, interaction has been observed between aluminum and hydrogen. By performing an anneal of the aluminum- or boron-doped sample in an inert atmosphere, e.g. argon at a temperature above 1000ºC for 30min, the hydrogen is released, and the net carrier concentration accordingly increases [13].

1.3.3 Etching

Reliable and controllable etching techniques with a high resolution, a strong anisotropy and a high selectivity with respect to the mask material are required for the successful fabrication of SiC based devices. At room temperature, no known wet chemical etches single-crystal SiC. Due to strong bonding between Si and C, SiC can only be conveniently etched by molten salts or chlorine and fluorine based gases at temperatures higher than 500ºC which induces problems with the photoresist, oxide or metal masks. Therefore, most patterned

etching of SiC for electronic devices and circuits is accomplished using dry-etching techniques.

The most commonly employed process involves reactive ion etching (RIE) of SiC in fluorinated plasmas. Sacrificial etch masks (often metals) are deposited and photolithographycally patterned to protect desired areas from being etched. The SiC RIE process can be implemented using standard silicon RIE hardware, and typical 4H- and 6H-SiC RIE rates are of the order of hundreds of angstroms per minute. Well-optimised SiC RIE processes are typically highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces.

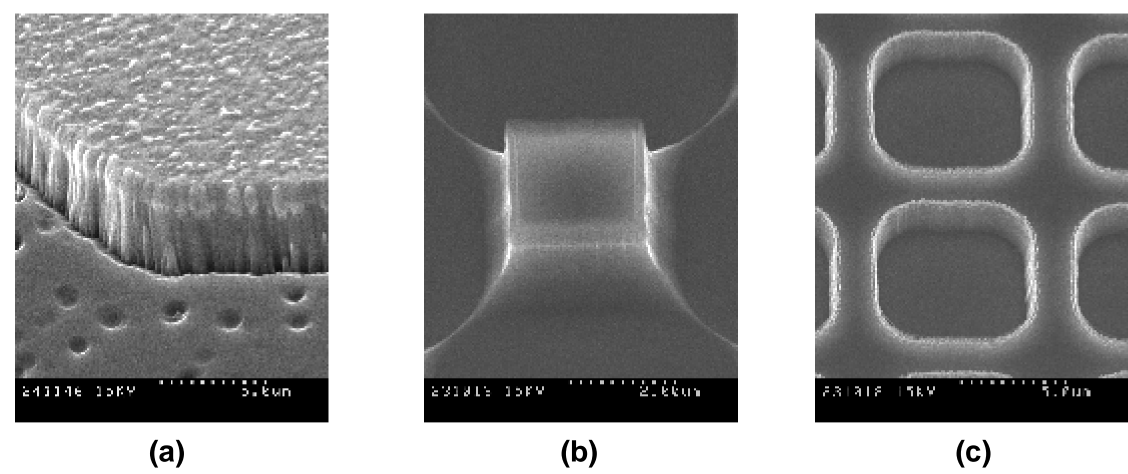


Figure 1.8 SEM pictures of SiC samples selectively etched with dry plasma etching: (a) RIE etching with Al mask, (b) ICP etching with SiO_2 mask, (c) ICP etching with Al mask .

While RIE rates are sufficient for many electronic applications, much higher SiC etch rates are necessary to delineate features of the order of tens to hundreds of micrometers deep that are needed to realize advanced sensors, microelectromechanical systems (MEMS), and some very high-voltage power devices structures. High-density plasma dry-etching techniques, such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP), have been developed to meet the need for deep etching of SiC. Deep dry etching with ICP techniques are progressing toward higher etching rates of SiC without micromasking and surface degradation effects typical of RIE (see Fig 1.8a). The slope of the sidewall can be controlled with the adequate choice of the mask layer and etching conditions. A SiO_2 mask layer will allow a soft slope of the sidewall (Fig. 1.8b), useful for better coverage of passivation layers for example. An Al mask layer will present a higher selectivity and very sharp sidewall (Fig 1.8c).

1.3.4 Contact formation

In SiC devices for high temperature and high power applications both ohmic and Schottky contacts are required which are stable at high temperature. Different materials are needed to n- and p-type SiC layers to create rectifying Schottky contacts or ohmic contacts with low contact resistivity. Based on the simple Schottky-Mott theory of metal-semiconductor contacts the Schottky barrier height of a certain metal or its ohmic nature depends exclusively on its work function, once it is brought into intimate contact with SiC (deposited onto that). Based on the above theory one may think that it is possible to sort the elemental metal layers into two groups: good ohmic or good Schottky contacts. However, the Schottky-Mott model needed a substantial modification, what was done later by Bardeen by introducing the idea of surface states. It is not possible to sort the metallic contacts as Schottky or ohmic as their basic electrical behaviour depends not only on the work function of the metal, but also on several parameters, even on alloying temperature of the contacts. For example, Ni contacts on n-type SiC annealed up to 600ºC are Schottky contacts, however, the same contacts annealed at 900ºC become ohmic [14]. This can be explained by the solid phase reactions that occurred during annealing.

N-type SiC ohmic contacts have developed to the point where specific contact resistances on heavily doped material are now in the 10^{-6} Ωcm^2 range. This is due to the fact that high quality heavily doped material is now available and that processes involving silicide formation using metals such as Ni appear to lead to lowered Schottky barrier heights at the metal-semiconductor interface. Implant technology has not generally been required to meet most device specifications for n-type contacts. N-type contacts submitted to ageing at high temperatures for long times and then characterised at room temperature indicate good thermal stability [15]. Most of the elemental metal layers deposited on n-type SiC exhibit a Schottky contact at room temperature with high barrier height [16]. Platinum and copper layers are good Schottky contacts up to 500ºC [17]. Tungsten and tungsten-based contacts are considered for high-temperature rectifying purposes, as well [18]. Molybdenum proved to be Schottky contact up to 900ºC, despite the fact that Mo_2C was formed during annealing [19]. Table 1.3 shows some selected measurements of Schottky barrier heights on 4H-SiC from the literature. The I-V (current-voltage) and C-V (capacitance-voltage) columns accounts for the electric measurement used to extract the Schottky barrier height.

P-type ohmic contacts are not as well developed or understood as n-type contacts. The very large Schottky barrier height that exists at the metal-p-type SiC interface has led to the need for extremely heavy surface doping since sufficient barrier lowering to enable ohmic contact formation has not been achieved. Enhanced doping for the formation of p-type ohmic contacts has been achieved either during epitaxial growth, by ion implantation, or it is generally believed, by contact processes using Al and Al based alloys. On that substrate Al/Ti

contacts are commonly used for ohmic contacts deposited either subsequently (Al/Ti, Al layer over the Ti layer) or simultaneously (Al-Ti) [25-27]. For Schottky contact purposes on p-type SiC, tungsten is a promising candidate [28]. Table 1.4 reports some selected results on ohmic contacts on n-type and p-type 4H-SiC material from the literature.

Table 1.3 Selected measurements of Schottky barrier heights on 4H-SiC from the literature.

n-type* or *p-type	**Metal**	**Schottky barrier height F_b (eV)** ¾¾¾¾¾¾¾ **I-V**	**C-V**	**Ideality factor** h	**Comment**	**Ref.**
n-type	TiW	1.22	1.23	1.05	As-deposited	[20]
		1.18	1.19	1.10	500ºC, 30min	
p-type	TiW	1.41	2.11	3.11	As-deposited	
		1.91	1.66	1.08	500ºC, 30min	
p-type	Ni	1.31	1.56	1.29	As-deposited	[21]
	Au	1.35	1.49	1.08		
	Ti	1.94	2.07	1.07		
n-type	Ni	1.59	-	1.05		
	Pt	1.39	-	1.01		
n-type	Al	0.65	-	2.28	As-deposited	[22]
n-type	Ti	0.83	-	1.02	As-deposited	[23]
	Ti	1.01	-	1.27	400ºC anneal	
	Ni	1.56	-	1.21	As-deposited	
	Ni	1.55	-	1.13	350ºC anneal	
n-type	W	1.19	-	1.02	500ºC anneal	[24]
	Mo	1.03	-	1.02		
	Ni	1.56	-	1.02		

Table 1.4 Review of specific contact resistance measurements on 4H-SiC in the literature.

n-type or p-type	**Metal**	**Doping (cm^{-3})**	**Contact resistance r_c (Wcm^2)**	**Annealing**	**Ref.**
n-type	TiC	1.3×10^{19}	4×10^{-5}	950ºC	[29]
p-type	TiC	$>10^{20}$	6×10^{-5}	950ºC	
	Ti	$>10^{20}$	8×10^{-4}	950ºC	
n-type	Ni	1×10^{19}	6×10^{-6}	1050ºC 10min	[30]
p-type	Ni	1×10^{21}	1.5×10^{-4}	1050ºC 10min	
n-type	Ni	1×10^{19}	7×10^{-6}	950ºC 30min	[31]
	TiW	1×10^{19}	3×10^{-5}	950ºC 30min	
p-type	TiW	6×10^{18}	1×10^{-4}	950ºC 30min	
p-type	Ni/Al	$3\text{-}9\times10^{18}$	5×10^{-3}	800ºC 2min	[32]
	Ni/Ti/Al	$3\text{-}9\times10^{18}$	6×10^{-5}	800ºC 2min	
p-type	Ge/Ti/Al	4×10^{18}	1×10^{-4}	600ºC 30min	[33]
p-type	Al-Ti	5×10^{18}	2×10^{-4}	1000ºC 2min	[28]
n-type	Ni/C	3×10^{19}	1×10^{-6}	700ºC 2h	[34]
	Ni/C	1×10^{17}	8×10^{-5}	900ºC 2h	
n-type	Co/Si/Co	1×10^{19}	4×10^{-5}	800ºC 10min	[35]

1.3.5 Oxidation

The thin SiO_2 plays an unique role in Si technology. The availability of high quality SiO_2 grown on Si substrate has led to the development of planar technology and permits fabrication of diffused or ion implanted junctions of precisely controllable dimensions. SiC is the only compound semiconductor in that its native oxide is SiO_2, the same oxide as Si. This means that the workhorse power devices in Si (power MOSFET, IGBT, MOS controlled thyristor) can be fabricated in SiC. Moreover, a good knowledge on the SiO_2/Si interface has been accumulated and has led to great progress in Si technology that can be applied to develop SiC technology.

As with the Si technology, the oxide layer on SiC can be obtained in different ways such as thermal oxidation and CVD. SiC surfaces can be thermally oxidized using dry and wet oxygen at around 1000 °C in the same way as Si. It has been found that the oxidation rate of all SiC polytypes is much lower than that of Si. It normally takes a much longer time to get the same thickness on SiC than on Si under the same oxidation conditions. Another unique characteristic in the oxidation process of SiC is that the oxidation rates are different between the silicon face and the carbon face i.e. the oxidation rates depend on the crystal orientation of SiC, thus SiC shows an anisotropic oxidation [36].

The SiO_2/Si interface plays a crucial role in the development of MOS devices. To build high performance MOS devices in SiC, the SiO_2/Si interface needs to be improved. For years, the progress has been hampered by problems with the gate oxide, reflecting in very poor channel-carrier mobility and oxide reliability. A lot of research efforts have been poured into the improvement of quality SiO_2/Si interface in SiC. A figure of merit in MOS devices can be described in terms of their interface state and fixed charge densities. Dramatic improvements have recently been reported with nitrided SiO_2–SiC interfaces [37, 38], leading to improved reliability and to recently reported values for inversion-layer mobility in 4H-SiC of about 50cm^2/Vs [39].

1.3.6 Packaging

The unavailability of a mature packaging technology for 300ºC–600ºC operation partially hinders development and demonstration of electronic devices for this temperature range. The major challenges to realizing such a packaging technology are chemical, physical, and electrical stability of both the packaging materials themselves as well as the interfaces between these materials. Most metals and alloys, including some noble metals, undesirably oxidize at temperatures approaching 500ºC when atmospheric oxygen is present. Therefore, most metals and alloys commonly used in conventional IC packaging, such as Cu, Al, and Au/Ni-coated Kovar, would not be practical for this environment, unless they are maintained in a perfectly hermetically sealed inert/vacuum environment by the rest of the package. If

more than one metallic material is used in an electrical connection, in some cases undesirable intermetallic phases may form at interface of different metals, such as Al and Cu, at high temperatures. These intermetallic phases often reduce the mechanical strength of an interconnection system.

As the part is thermally cycled, the large temperature range encountered (55ºC–600ºC) increases stress caused by mismatch in the coefficient of thermal expansion (CTE) between different materials in the package. CTE mismatch between the die, die-bond material, and the package baseplate will place stress on the wide bandgap die itself. Therefore, to minimize stress, the CTE of all materials in the die-attach should be matched as best as possible. In cases where a backside electrical contact is required, the die-bonding material must be chemically and electrically compatible with the wafer backside metallisation. The requirement of CTE match at package seals restricts the sealing material selection in order to ensure hermeticity under thermal cycling. Besides the CTE match requirement for obtaining a hermetic seal that would withstand thermal cycling, high temperatures significantly promote thermal processes such as diffusion and degassing at material surfaces that would likely lead to contamination of the hermetic cavity atmosphere over time. Achieving and verifying hermetic seal for long-term 300ºC–600ºC operation will be challenging. In order to realize practical high-temperature electronics packaging, innovative packaging materials and package designs concepts are required. Recently, aluminum nitride (AlN) insulating noncrystalline ceramic, which has CTE properties very close to SiC, was proposed as substrate material for high-temperature device packaging [40,41]. Thick-film materials appear promising for use as substrate metallisation in realizing 500ºC hybrid packaging [42]. A gold thick-film metallisation on AlN ceramic-based 500ºC packaging for SiC devices has been demonstrated [43]. The electrical interconnection system of this approach has been tested in an air environment for over 5000h at 500ºC and a packaged SiC test device operated for over 1000h. High-temperature passive components, such as inductors, capacitors, and transformers, must also be developed for operation in demanding conditions before the full system-level benefits of high ambient temperature power electronics can be successfully realized.

1.4 Power Rectifiers

Switches and rectifiers are key components in power electronics systems, which cover a wide range of applications, from power transmission to control electronics and power supplies (see Table 1.5). The total power handling ranges from 40W in control electronics to several MW in power transmission.

Table 1.5 Example of common applications that utilize power rectifiers

Application	Diode blocking voltage	Diode current	Switching frequency
High Voltage DC transmission	5000 -25000V	100 -3000A	50Hz - few kHz
Traction and industrial drives	1700 -6500V	500 -1500A	50 – 1kHz
Power supplies and motor drives	300 -1200V	3 -100A	2kHz - 250kHz
Control electronics	40 -300V	1 -10A	50kHz - several 100kHz

When realizing SiC power devices that will operate in applications with lower power losses compared to Si it is important to design and fabricate devices that really make use of the better electrical properties of SiC. The improved device performance should result in higher possible operating temperatures (above 150ºC). Then the benefit is fewer components and less cooling equipment. The natural approach is to start with power diode structures well known in Si and GaAs technology, and then adapt and modify the design, finalizing with the process to the SiC material. Generally speaking, there are three main device structures of power rectifiers (see Fig 1.9):

1) **Schottky diode –** Unipolar diode that offers extremely high switching speed, but suffers from high leakage currents. A unipolar device means that the current is governed only by majority carriers (electrons).

2) **PiN diode –** Bipolar diode that offers low leakage current but shows reverse recovery current charge during switching as a consequence of minority (holes) and majority (electrons) carriers are both involved in the current conduction.

3) **Junction Barrier Schottky (JBS) diode –** Unipolar diode, which combines Schottky-like on-state and switching characteristics with *PiN*-like blocking characteristics.

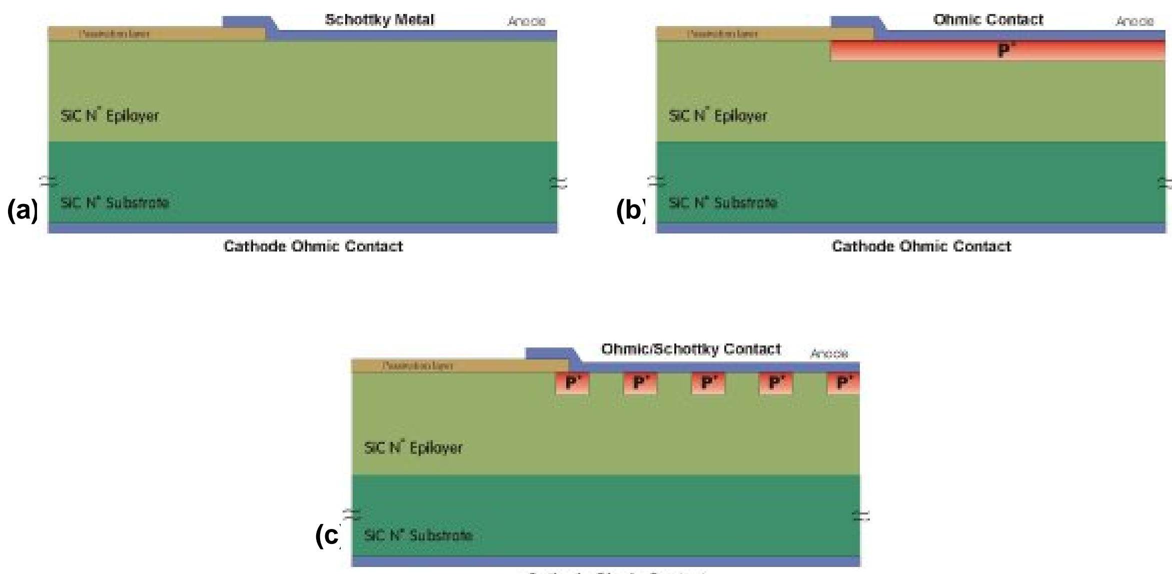


Figure 1.9 Schematic diode structures of (a) Schottky, (b) PiN, and (c) JBS diodes.

Whether an unipolar or a bipolar rectifier is preferred depends on many device parameters, such as reverse blocking voltage, forward current density, maximum allowable reverse current density, operating temperature and switching frequency. The particular device type is often chosen to either minimize the total power dissipation or maximize the safe-operating-area (SOA) during device turn-on or turn-off.

As far as the process technology is concerned, the Schottky rectifier is constructed on the metal-semiconductor junctions whereas the junction rectifier is based on the PN junctions. The device process technology of the former depends on the choice of the Schottky metal as well as on the surface cleaning techniques and post-metal deposition annealing procedure. By contrast, the junction rectifier characteristics are controlled by the PN junction formation technology, the most popular of which are in-situ doped epitaxy and compensation doping by ion implantation. Due to its bipolar nature, the junction rectifier is very sensitive to the carrier lifetimes of the material.

A list of experimental results on high-voltage rectifiers in 6H- and 4H-SiC is shown in Table A1 in Appendix A.

1.4.1 Power Schottky Barrier Diodes (SBDs)

SiC SBDs are commercially available since 2001. Table 1.6 summarises the commercially available SBDs to date. The most remarkable advantage of SiC SBDs is the continuing increase in blocking voltage and conduction current ratings. They range from the initial 300V, 10A and 600V, 6A to the current 600V, 20A and 1.2kV. With the latest ratings, it is foreseen

that these diodes may replace Si bipolar diodes in medium power motor drive modules. Power Factor Correction and High-Voltage Secondary Side Rectification are applications of 600V SiC Schottky diodes [44]. Besides, it is expected that SBDs can be advantageously applied for blocking voltages up to 3.5kV.

Table 1.6 Comercially available SiC Schottky rectifiers.

<table>
<tr><th>Company</th><th>V_{br}</th><th>I_f (A)</th><th>V_f (V) @I_f</th><th>I_r (mA)</th></tr>
<tr><td>Cree</td><td>1.2kV</td><td>5-20</td><td>1.6</td><td>200</td></tr>
<tr><td>Cree</td><td>600V</td><td>1-20</td><td>1.6</td><td>200</td></tr>
<tr><td>Infineon</td><td>600V</td><td>4-12</td><td>1.5</td><td>100</td></tr>
<tr><td>Infineon</td><td>300V</td><td>10</td><td>1.5</td><td>20</td></tr>
<tr><td>Microsemi</td><td>200V</td><td>1-4</td><td>1.3-1.8</td><td>50</td></tr>
<tr><td>Microsemi</td><td>400V</td><td>1-4</td><td>1.3-1.8</td><td>50</td></tr>
<tr><td>Microsemi</td><td>600V</td><td>1-4</td><td>1.3-1.8</td><td>50</td></tr>
<tr><td>Rockwell</td><td>1.2kV</td><td>7.5</td><td>2.1</td><td>10</td></tr>
<tr><td>Semelab</td><td>600</td><td>5</td><td colspan="2" rowspan="2">Preliminary</td></tr>
<tr><td>Semelab</td><td>1.2kV</td><td>5</td></tr>
</table>

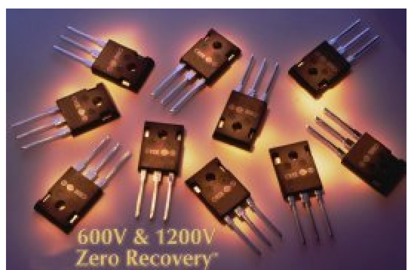


Figure 1.10 Cree SiC SBDs diodes.

Figure 1.11 Semelab/CNM prototype 1mm^2 SiC diode

In comparison with Si counterparts, a 10x increase in voltage blocking is possible with the same SiC drift layer thickness. The main difference to ultra fast Si pin diodes lies on the absence of reverse recovery charge in SBDs. Therefore, SiC SBDs are well suited for high switching speed applications. 1.2kV SiC SBDs match perfectly as freewheeling diodes with Si IGBTs. Efficiency tests of the commercial SiC Schottky rectifiers carried out on a DC-DC buck converter demonstrate that as the temperature and converter switching frequency increase (up to 200ºC and 150kHz, respectively), the efficiency of the SiC Schottky diode compared to the ultra fast Si pn-junction diode becomes significantly better and show the clear advantage of using the SiC Schottky diode for high temperature and high frequency operation (see Fig. 1.12) [45].

The high thermal conductivity of SiC is also a great advantage in comparison with Si and GaAs diodes since it allows to operate at higher current densities ratings as well as to minimize the size of the cooling systems.

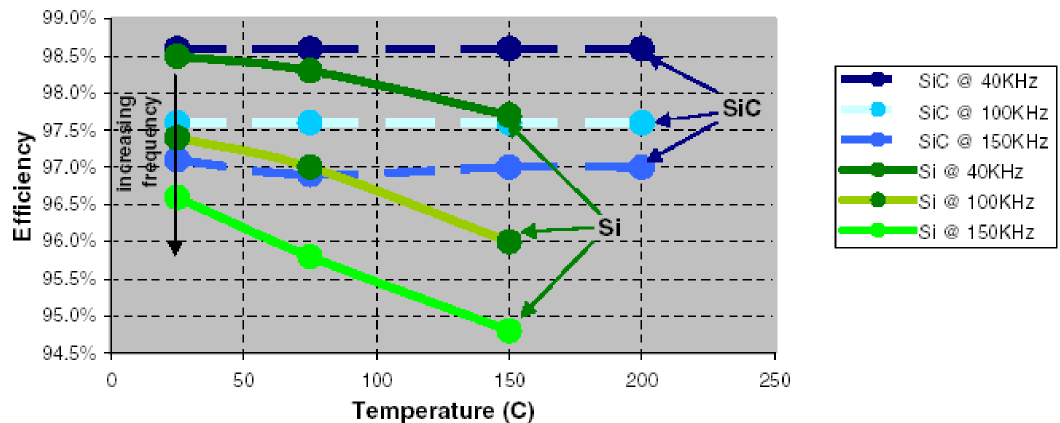


Figure 1.12 Buck converter efficiency as a function of temperature and switching frequency using either the Infineon (600V/6A) SiC Schottky diode or the IXYS (600V/ 8A) ultra fast Si *pn*-junction diode.

Commercial Schottky rectifiers are expected to continue to increase in voltage and current ratings. For the typical application of 3-5kV large currents, in the range of 100A, are needed; this being still far from the state-of-the-art of the SiC technology. Another limitation of SiC Schottky diodes is the temperature behaviour linked to its unipolar nature. There is a strong increase of the on-resistance at high-current ratings when internal temperature increases, limiting the surge current capability of the diodes. To overcome this problem JBS diodes have to be contemplated.

1.4.2 SiC PiN diodes

The best forward I-V characteristics of 4H-SiC *PiN* diodes have been shown for epitaxed *PN* diodes (not implanted junctions) [46]. The reason for this is the inability to eliminate the lattice damage produced by the ion implantation just below the metallurgical junction.

Due to the wide band gap of SiC (3.25eV@25ºC for 4H-SiC), it is necessary a forward voltage of about 3V to get a significant current from a SiC *PiN* diode. Power electronics high-voltage applications require high-current ratings as well. Thus, a large area device is required. However, the yield of large area devices is still low with the starting material available today. Nevertheless, there are significant long terms prospects for SiC PiN diodes and a rapid advancement has been shown for 4H-SiC *PiN* diodes. CREE has reported that high quality epitaxial drift layers as thick as 100µm (for 10kV) and 200µm (for 20kV) has been growth for PiN diodes having forward voltage drops (at 100A/cm^2) as low as 3.9V and 6.3V, respectively [47]. Large area diodes have been fabricated, which are capable of handling up to 50A and blocking 10kV.

Unfortunately, it has been reported [48] that high power SiC PiN diodes exposed to long term operation exhibit an increase of the static forward voltage drop after the testing. Various

physical characterization techniques have shown that structural defects are created in the epilayers during the operation. The structural defects are interpreted as stacking faults in the 4H-SiC (0001) basal plane, propagating progressively through the entire *n*-epilayer under electrical stress conditions. The stacking faults, or defects associated with these, act as recombination centers reducing the carrier lifetime in the material. Encouragingly, Cree researchers have reported [47] that a process modification, which suppresses this degradation phenomenon, has been found but they have not released any detail. This has allowed to demonstrate high voltage SiC PiN diodes with large area that show no forward voltage degradation [47].

Unlike Si diodes, the reverse recovery current waveforms of SiC bipolar diodes show no significant temperature dependence up to 200ºC [49], probably due to the recombination centers deepness. In Fig 1.13, typical reverse recovery waveforms of 12 and 19kV 4H-SiC PiN diodes are shown along with Si rectifiers. From this figure, it is clear that the reverse recovery charge (Q_{rr}) and recovery time (t_{rr}) of the SiC pin diodes are substantially smaller than those of an equivalent Si diode of the same voltage rating.

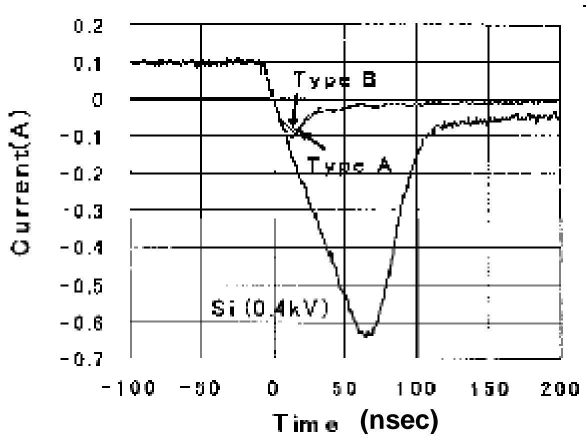


Figure 1.13 Experimental reverse recovery currents waveforms of 15kV (Type A) and 19kV (Type B) 4H-SiC junction rectifiers and comparison to that of 400V Si junction diode [45].

SiC PiN rectifiers, only relevant for voltage ratings over 3kV, need to overcome the forward voltage degradation. Nevertheless, 3kV 600A PiN diode modules have been integrated successfully [50].

1.4.3 SiC JBS diodes

Schottky rectifiers are expected to dominate for blocking voltages below 3kV. However, the reverse leakage current of the SBDs is generally excessive, particularly at high temperatures, due to Schottky barrier lowering at high reverse voltages. JBS rectifiers have been explored for SiC up to 3.7kV [51]. They utilize adjacent *pn* junctions to prevent the electric field from rising at the Schottky junctions.

SB diodes as well as JBS diodes operating at a voltage lower than the turn-on voltage of the *pn* junctions exhibit faster switching speed than *PiN* diodes due to the absence of minority carrier injection. A common tendency observed through recent publications is that SiC JBS diodes with the reverse leakage well maintained closer to the *PiN* diode level tend to show forward current densities reasonably lower (20- 30%) than those of the SB diodes. However, ideally the forward and reverse current densities of a JBS diode should not depend on each other since the reverse leakage is related to the effectiveness of the field-shielding structure with the SB interface surrounded by the *pn* junctions, while the reduction in forward current densities is related to the area occupied by the *p*-diffusions. Nevertheless, in reality the two factors are process dependent involving the quality of the SB interface in the JBS diode process fabrication. Fig. 1.14 shows the experimental forward and reverse I-V characteristics of JBS, SB and *PiN* diodes from [52]. In conclusion, generally speaking the JBS diodes show on-state and switching characteristics similar to Schottky diodes and blocking characteristics similar to *PiN* diodes. In addition, this type of rectifiers shows a superior surge current capability.

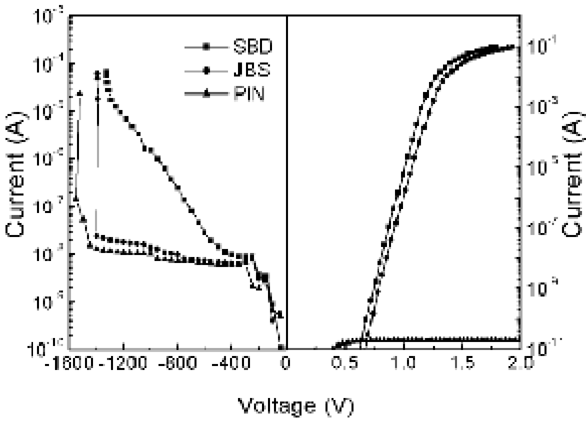


Figure 1.14 Reverse and forward I-V characteristics at RT of 300μm diameter SBD, JBS and PiN diodes on 10μm thick and $1.4\times10^{16}cm^{-3}$ doped epilayer.

1.5 SiC Power Switches

SiC power switches in the 600V range have two strong Si competitors: the power MOSFET (including CoolMOS and other advanced trench devices) and the IGBT. Nevertheless, the Si MOSFET has a drawback when its intrinsic diode is turned on under hard switching conditions. A low on-resistance SiC switch able to operate at high junction temperatures has clear advantages in comparison with its Si counterparts. In addition, there is an increasing demand of high-voltage, voltage controlled switches, which opens the possibility of having new application fields.

1.5.1 Unipolar SiC Switches

JFETs

For the blocking voltage range from 1.2kV to 1.8kV, the Si MOSFET is not a realistic option and the Si IGBT shows high dynamic losses requiring fast switching. SiC JFET may be an excellent alternative since this switch shows an ultra low specific on-resistance and is also able to operate at high temperatures and high frequencies. Infineon has developed a 1.5kV, 0.5Ω on-resistance hybrid switch made up of a 1.5kV vertical SiC JFET and a 60V Si MOSFET in cascode configuration [53]. The SiC JFET is a normally-on device, thus a cascode arrangement is necessary. This switch is aimed at resonant converters and power supplies. Recently, a $3\times4.1mm^2$ 1.8kV SiC JFET die has been presented by Infineon with a current capability of 15A at an on-state voltage of just 2V. The technology is said to be viable at voltages of up to 4.5kV [54]. In order to increase the current capability of high voltage (>3kV) JFET switches, new devices have been proposed adding a bipolar component. This is done to create a conductivity modulation inside the drift region and thus reducing the on-resistance as it was done in the Si IGBT.

In this sense, 1.6kV, 40A, 6mm×6mm SIJFET (Static induction carrier Injected JFET) has been demonstrated [55] with high switching speed and lower on-resistance than equivalent JFET. In a similar way, the BIFET (Bipolar Injection FET), a normally-on JFET with a pn junction at the cathode, which provides conductivity modulation in the drift region, has also been proposed by SiCED [56].

MOSFETs

The very low inversion channel mobilities that are achieved on 4H-SiC have for many years prevented the fabrication of the low-resistance MOSFETs that would be able to demonstrate the potential of SiC as a material for power devices. Indeed, the MOS interface and MOSFETs in general attracts a great deal of attention.

Two approaches have emerged as being effective in improving the quality of the MOS interface: the use of nitrogen during post-oxidation annealing and the use of alternative crystal faces for the formation of the MOS channel.

Great improvements in MOS channel mobility by using the (1120) crystal face rather than the more commonly used (0001) face have been demonstrated [57], showing a greatly reduced density of interface states and a small temperature dependence of threshold voltage. Results on MOSFETs produced on the (1120) and (0338) crystal faces are also encouraging. Another work [60] has reported significant improvements in the channel mobilities of MOSFETs fabricated on the (1120) face using hydrogen post-oxidation annealing. A peak mobility of 110 cm^2/Vs has been reported for an enhancement mode device with an inversion

channel. The (0338) face has also been analysed [57], achieving an improvement in mobility by a factor of four, and an order of magnitude improvement in current drive capability when compared with devices fabricated on (0001) face. However, these mobilities are obtained on epitaxied p-layers. Besides, channel mobility has been demonstrated to be lower when measured on p-implanted regions due to the implantation damage.

Therefore, novel power MOS structures on epitaxied p-bodies have been proposed recently. The highest channel mobilities and the highest current MOSFETs have been measured on buried channel devices. MOSFETs with a peak channel mobility of 216cm^2/Vs have been fabricated on the (1120) face [58]. Besides, a peak channel mobility of 140cm^2/Vs for MOSFETs fabricated on the (0001) face has also been reported [59]. In addition, Cree has reported large-area (3.3mm×3.3mm) buried channel devices capable of handling currents of up to 10A with voltage blocking capabilities of up to 2.4 kV [60]. Nevertheless, the mobility sharply drops to values in the range of 20-50cm^2/Vs for operating gate voltages (see Fig. 1.15).

On the other hand, passivation of the SiC-SiO_2 interface with nitric oxide [61] shows an order of magnitude reduction in the level of interface states and a corresponding increase in current drive capability. However, interface state densities are still two orders of magnitude higher than those that are achievable with state-of-the-art Si MOS technology. The technique has been adopted by Cree and used to demonstrate high-current (2A) large area (2mm^2) lateral MOSFETs. Further results from Cree have indicated that nitrous oxide was equally effective in improving the MOS interface.

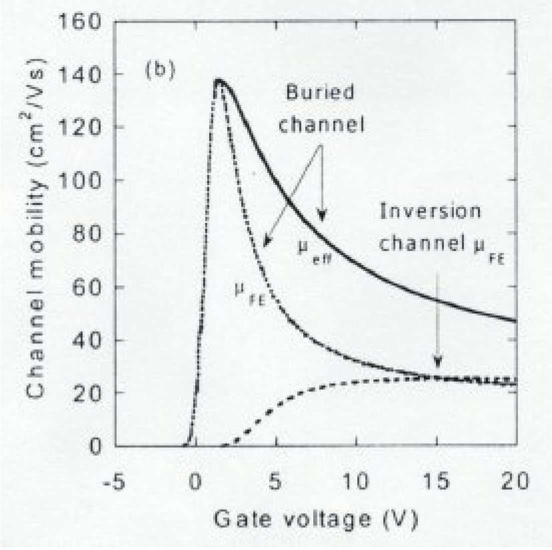


Figure 1.15 Channel mobility versus gate voltage in the inversion channel and buried channel MOSFETs. Drain voltage: 0.1 V.[59].

1.5.2 Bipolar SiC switches

For 4.5kV and higher blocking voltage ratings, bipolar SiC devices are in theory more suitable than unipolar devices. Nevertheless, as mentioned in SiC pn diodes section, a significant progress in material quality (staking faults, etc.) and minority carrier lifetime control is required before utilizing these devices in applications such as high voltage drives, traction or high-voltage dc transmission (HVDC) systems. This means that it will take some years to industrialize power, high-voltage bipolar SiC switches, regarding switch performance/industrialization cost. Dynamic performance together with high temperature operation and blocking rating in the range of 10kV or higher is the application for which SiC is an excellent candidate.

However, it could be a short term industrialization of SiC bipolar junction transistors (BJTs) or Darlingtons for applications ranging form 600V to 1.7kV due to their high temperature capability and a normally-off operation, but they will compete with unipolar SiC switches, which can be easily paralleled to get high-current ratings as well as connected in series to increase the blocking capability.

Unlike Si npn BJTs, the SiC counterpart suffers no degradation of the open-base breakdown voltage (VCEO). Nevertheless, the current gain (β) is still low (lower than 12) at high-current ratings [62] (see Fig. 1.16). Darlington configuration allows to increase significantly the current gain (β>462) [63]. An interesting and complete summary of these achievements is reported in [64].

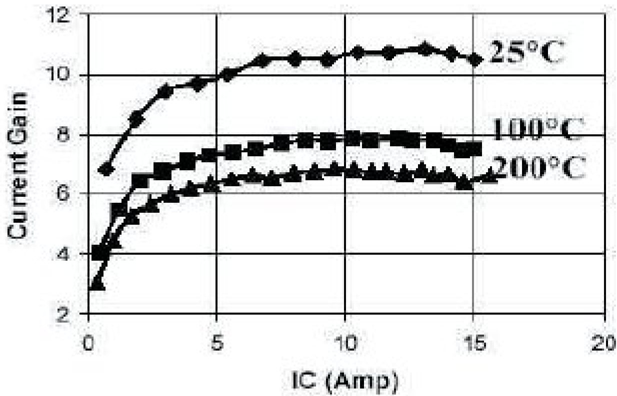


Figure 1.16 BJT current gain as a function of collector current and temperature from [62].

1.6 Summary

Silicon carbide (SiC) is currently under intensive investigation as an enabling material for a variety of new semiconductor devices in areas where silicon devices cannot effectively compete. These include high-power high-voltage switching applications, high temperature electronics, and high power microwave applications in the 1-10 GHz regime. SiC is attractive for these applications because of its extreme thermal stability, wide bandgap energy, and high breakdown field. The thermal stability promises long term reliable operation at high temperatures, but it also presents problems in certain fabrication steps, e.g. selective doping, where impurities must be introduced by ion implantation due to the exceedingly low diffusion coefficients of common dopant impurities at reasonable processing temperatures. Because of the wide bandgap energy (3.0eV and 3.25eV for the 6H and 4H polytypes respectively), leakage currents in SiC are many orders of magnitude lower than in silicon, and the intrinsic temperature is well over 800ºC. These electronic properties make SiC attractive for high temperature electronics applications. In addition, the breakdown field in SiC is around 8x higher than in silicon. This is critical for power switching devices, since the specific on-resistance scales inversely as the cube of the breakdown field. Thus, SiC power devices are expected to have specific on-resistances 100-200x lower than comparable silicon devices. Finally, SiC is the only compound semiconductor which can be thermally oxidized to form a high quality native oxide (SiO_2). This makes it possible to fabricate MOSFETs, insulated gate bipolar transistors (IGBTs), and MOS-controlled thyristors (MCTs) in SiC.

Although it offers substantial advantages over silicon, SiC is still immature as a semiconductor material. Single crystal wafers of SiC have only been commercially available since around 1990, and a number of critical material and processing issues are still under active investigation. The main limitations of the technology are in the area of crystal growth, and will be addressed in more detail below. In addition, certain critical fabrication processes are still under development. The most important of these fabrication issues are (i) activation of ion implanted impurities, (ii) formation of thermally stable low resistance ohmic contacts, and (iii) thermal oxidation (or deposition) of high quality dielectric films suitable for MOS devices.

Silicon carbide (SiC) electronic systems will perform an enabling function in the energy and transport technologies of the 21st century. Their inherent ability to operate at high temperatures and increased conversion efficiencies compared to silicon based electronics will facilitate technological advances across a range of application areas including combustion process controls, the more electric aircraft, electric traction and power transmission and distribution. Although its potential has been known for over 40 years, it is only in the last 10 years that commercial material has become available. Progress in the last 5 years has been rapid and many research groups across the world are now reporting excellent results.

The high critical breakdown field strength of SiC (a factor of 10 greater than Si) permits high efficiency power electronic switching devices to be fabricated with high voltage ratings. For example, SiC Schottky diodes are a realistic proposition at voltage ratings of 2 kV or more whereas Si Schottky diodes are limited to voltages below 200 V. A similar argument applies to other unipolar devices such as MOSFETs, JFETs and MESFETs. In Si technology the voltage limitations of unipolar carrier devices are overcome by utilising bipolar technology with devices such as IGBTs, PiN diodes and thyristors. Although they exhibit improved conduction characteristics compared to MOSFETs and Schottky diodes, they carry the penalty of relatively poor switching performance. The improved performance of SiC unipolar devices can be shown to have a significant impact on power electronic system efficiency. For example, it can be demonstrated that the substitution of SiC Schottky diodes and SiC power FETs for existing Si IGBTs and PiN diodes will result in a 50% reduction in total conversion losses in a typical 20 kW PWM motor drive.

CHAPTER 2

Device Design

This chapter will describe the device design procedure, and show the optimisation process of the different periphery protection structures implemented in our diodes. The first part of the chapter covers the 4H-SiC electronic models implemented for the numerical device simulations performed using the commercial program MEDICI™. The analysis and design of the edge termination structures developed in the scope of this thesis are also presented. Finally, it will be shown and commented the photolithographic mask set designed in order to fabricate the devices.

2.1 Modelling and Simulation

Numerical device modelling and simulation are essential for analysing and developing semiconductor devices. They help a design engineer, not only gain an increased understanding of the device operation, but also provide the ability to predict electrical characteristics, behaviour, and parameter-effects influence of the device. With this knowledge and abilities the designer can design a better structure, estimate device performances, perform worst case analysis, and optimise device parameters to yield an optimise device performance.

The simulator used in this work was MEDICI™ from Synopsys Inc.[65]. This software is a 2-dimensional device simulator for general purposes. Its primary function is to solve the Poisson´s equation and the continuity equations based on the Boltzmann carrier transport theory self-consistently for the electrostatic potential Ψ and for the electrons and holes concentrations n and p, respectively.

The Poissons´s equation governs the electrical behaviour of the semiconductor device and its given by

$$\varepsilon \cdot \nabla^2 \Psi = -q \cdot (p - n + N_D^+ - N_A^-) - \rho_S \qquad (2.1)$$

where e is the semiconductor dielectric constant, r_S is the surface charge density that may be present due to fixed charge in insulating materials or charged interface states, and N_D^+ and N_A^- are the ionised impurity concentrations.

The continuity equations for electrons and holes are given by

$$\frac{\partial n}{\partial t} = \frac{1}{q}\cdot\vec{\nabla}\overrightarrow{J_n} - U_n \tag{2.2a}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\cdot\vec{\nabla}\overrightarrow{J_p} - U_p \tag{2.2b}$$

where J_n and J_p are the electron and hole current densities, and U_n and U_p the net electron and hole recombination rates. From Boltzmann transport theory, J_n and J_p in Eq. 2.2 can be written as a function of Ψ, n, and p, consisting of drift and diffusion components

$$\overrightarrow{J_n} = q m_n \overrightarrow{E_n} n + q D_n \vec{\nabla} n \tag{2.3a}$$

$$\overrightarrow{J_p} = q m_p \overrightarrow{E_p} p - q D_p \vec{\nabla} p \tag{2.3b}$$

where m_n and m_p are the electron and hole mobilities and D_n and D_p are the electron and hole diffusivities.

The numerical algorithms used in MEDICI to solve these five basic device equations are based on the finite element method, which discretised these equations on a simulation grid. This discretisation process yields a set of coupled non-linear algebraic equations which represent a number of grid points, for the unknown potentials and free-carrier concentrations. This set of coupled non-linear algebraic equations in return must be solved by a non-linear iteration method. Two iteration approaches, Gummel's and Newton's method are available in MEDICI. Regardless which iteration method used, the solutions are carried out over the entire grid until a self-consistent potential (ψ) and free-carrier concentrations (n, p) are obtained. Once the potentials (ψ) and free-carrier concentrations (n, p) have been calculated at a given bias, it is possible to determine the quasi-Fermi levels (φ) and the hole and electron currents (J_n and J_p) from Eq. 2.3a – 2.3b.

The results of device simulations depend critically on the physical models and parameters used. A number of physical models are incorporated in MEDICI for accurate simulations, including models for recombination, photogeneration, impact ionisation, energy bandgap narrowing, band-to-band tunnelling, mobility, and lifetime [65]. To accurately simulate the electrical performance of the device, properly choice of the physical models and the corresponding parameters must be considered. The physical models in the simulation software are basically based on Si device technology. Therefore the model parameters in the simulator

must be adjusted for the closest agreement with the physical models for 4H-SiC. In the following section the physical models and parameters of 4H-SiC for device simulations are presented with the values based on the recent literature, which are applicable to electronic devices.

2.1.1 Band structure

The electron band structure and effective masses in SiC are complex because several non-parabolic bands in reciprocal *k*-space are to be considered. It has been observed that the exact theoretical band structure calculations vary in different works. The small variations in the atomic positions of the hexagonal planes affect the spin-orbit splitting and crystal-field splitting [66] and stacking faults may have to be considered [67].

However, the effective electron and hole masses are not significantly affected and they are given as in Eq. 2.4 by assuming parabolic bands and taking the values m_{de}=0.76m_o and m_{dh}=1.20m_o [68]. The room temperature value of N_C and N_V were taken from reference [69] and calculating the density of states gives 1.67×10^{19} and 3.19×10^{19} for N_C and N_V, respectively.

$$N_C(T) = 2\cdot\left(\frac{2p\cdot m_{de}\cdot k_B T}{h^2}\right)^{\frac{3}{2}} \tag{2.4a}$$

$$N_V(T) = 2\cdot\left(\frac{2p\cdot m_{dh}\cdot k_B T}{h^2}\right)^{\frac{3}{2}} \tag{2.4b}$$

The model for the temperature dependency of the energy gap for 4H-SiC is taken from 6H-SiC, and its given by

$$E_g(T) = E_g(T_0) - a^{E_g}\cdot T \tag{2.5}$$

where $E_g(T_o)$=3.26eV is the room temperature bandgap value and a^{Eg}=3.3×10^{-4}eV/K is an experimentally determined parameter.

The intrinsic carrier concentration n_i is determined by the energy gap E_g and by the conduction and valence band density of states, N_C and N_V, respectively.

$$n_i = \sqrt{N_C\cdot N_V}\cdot exp\left(-\frac{E_g}{2k_B T}\right) \tag{2.6}$$

The intrinsic carrier concentration n_i of 4H-SiC is extremely low (~10^{-9}cm^{-3} at room temperature) due to its wide bandgap. Because of the low value of intrinsic carrier concentration, 4H-SiC based devices can operate at higher temperature than other materials as already explained in Chapter 1 section 1.2.3 (see Fig. 1.5).

2.1.2 Bandgap narrowing

The modification of the density of states by heavy doping leads to an additional influence which is generally modelled by rigid shifts of the band edges, the so-called “bandgap narrowing”. Theoretical models for doping-induced band edge displacements and bandgap narrowing in both *n*-type and *p*-type 4H-SiC were presented by Lindefelt [70]. The model takes into account the three different electron effective mass components associated with hexagonal lattices (instead of two as in Si and Ge). The results for the band edge displacements are expressed in simple analytical form as functions of doping concentration.

The band edge displacements for *n*-type semiconductors can be summarised with the formulas

$$\Delta E_C = A_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{1/3} + B_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{1/2} \tag{2.7a}$$

$$\Delta E_V = A_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{1/4} + B_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{1/2} \tag{2.7b}$$

For *p*-type semiconductors we get

$$\Delta E_C = A_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{1/4} + B_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{1/2} \tag{2.8a}$$

$$\Delta E_V = A_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{1/3} + B_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{1/2} \tag{2.8b}$$

The resulting bandgap narrowing DE_g then becomes

$$\Delta E_g = \Delta E_V - \Delta E_C \tag{2.9}$$

In agreement with the convention used in device modelling, the bandgap narrowing defined here is a positive quantity.

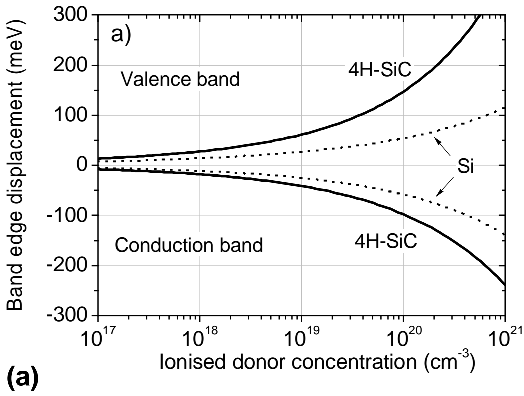
The coefficients A_{nb}, A_{pb}, B_{nb}, and B_{pb} can be adjusted in the device simulator model by introducing their values for the specific material. For 4H-SiC Lindefelt reported the values [70]:

4H-SiC *n*-type A_{nc}= -1.5×10^{-2} ; B_{nc}= -2.9×10^{-3} ; A_{nv}= 1.9×10^{-2} ; B_{nv}= 8.7×10^{-3}

4H-SiC *p*-type A_{pc}= -1.6×10^{-2} ; B_{pc}= -3.9×10^{-4} ; A_{pv}= 1.3×10^{-2} ; B_{pv}= 1.1×10^{-3}

giving the band edge displacements in eV.

Equations 2.7 and 2.8, with the parameter values given above, have been plotted in Fig. 2.1. The results for silicon are also shown for comparison. The bandgap narrowing is obtained as the energy distance between the valence band and conduction band shifts.



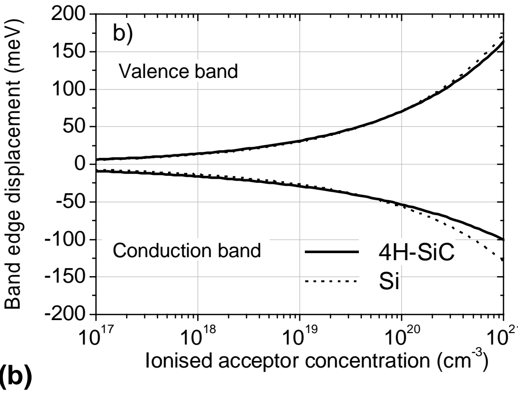


Figure 2.1 Conduction band displacements and valence band displacements for 4H-SiC *vs* ionised concentration, (a) donor and (b) acceptor. For comparison, the band edge displacements for Si are shown.

From Fig. 2.1 it is clear that for *n*-type material the bandgap narrowing is substantially larger in 4H-SiC than in Si at high donor concentrations. For *p*-type material, the valence band shifts for 4H-SiC and Si are almost identical, and the conduction band shifts are very close. Finally, we note that in all cases except *n*-type Si, the valence band displacement is larger than the conduction band displacement at medium and high doping.

2.1.3 Incomplete Ionisation of dopants

As in silicon, dopant atoms can be selected from group III and V in the periodic table for *p*-type and *n*-type SiC, respectively. However, the energy levels of dopants are much deeper than in Si and therefore the dopants are not fully ionised at room temperature in SiC [71]. This effect is also known as the dopant freeze-out in Si at low temperatures. The ionisation energies of commonly used dopant atoms in SiC are shown in Table 2.1.

Table 2.1 Dopants in SiC and their ionisation energy with the lattice site

Type	Dopant	Ionisation Energy (meV)		
		4H-SiC	6H-SiC	Si
n (donors)	*N*	42 (hex), 82 (cub)	82 (hex),137 (cub)	45
	P	53 (hex), 93 (cub)	82 (hex),115 (cub)	45
p (acceptors)	*B*	300	310	45
	Al	190	225	67

Al (substituting on Si site) and *N* (substituting on C site) are the most common acceptor and donor impurities for SiC, respectively. Doping with nitrogen (*N*) leads to a donor with

two different energy levels below the conduction band due to the existence of two different lattice sites, one with cubic surrounding and the other with hexagonal surrounding. A nitrogen atom sitting on these sites will therefore give rise to different ionisation energies. In actual simulations, these two donor levels can be lumped together and replaced by a single level [68]. Phosphorus presents a similar behaviour with slightly higher activation energies. However, it has been shown that phosphorus has a superior activation to nitrogen at high dopant concentrations ($>2\times10^{19}$cm^{-3}) [72].

From the neutrality condition in electrothermal equilibrium we obtain that the ionisation rate of a single acceptor level in p-type material is given by,

$$I_A(E_A) = \frac{N_A^-}{N_A} = \frac{-1+\sqrt{1+4g_A\frac{N_A}{N_V}exp\left(\frac{E_A-E_V}{k_BT}\right)}}{2g_A\frac{N_A}{N_V}exp\left(\frac{E_A-E_V}{k_BT}\right)} \tag{2.10a}$$

where E_A-E_V is the energy difference between the valence band maximum and the acceptor level, N_A^- is the number of ionised acceptors, and g_A is the acceptor level degeneration factor (g_A=4).

Similarly, for single donor level in n-type material the ionisation rate is given by,

$$I_D(E_D) = \frac{N_D^+}{N_D} = \frac{-1+\sqrt{1+4g_D\frac{N_D}{N_C}exp\left(\frac{E_C-E_D}{k_BT}\right)}}{2g_D\frac{N_D}{N_C}exp\left(\frac{E_C-E_D}{k_BT}\right)} \tag{2.10b}$$

where E_C-E_D is the energy difference between the conduction band minimum and the donor level, N_D^+ is the number of ionised donors and g_D is the donor level degeneration factor (g_D=2). Using the values of Table 2.1 and taking into account the temperature dependency of the density of states, the ionisation degree of *Al* and *N* calculated with Eq. 2.10a and 2.10b respectively, is shown in Fig. 2.2 as a function of temperature and doping concentration. For nitrogen, the highest ionisation energy (82meV) has been used as a reference of the minimum ionisation degree. In the simulation, Poisson´s equation is solved for the ionised impurity concentrations (N_D^+, N_A^-).

At room temperature and N_A = 10^{16}cm^{-3}, only 60% of *Al* are ionised. I_A decreases with increasing center concentration and decreasing temperature which finally leads to the freeze-out of holes at low temperatures.

Incomplete ionisation of *N* becomes only relevant at low temperatures and high doping concentrations. More than 90% of *N* is ionised for temperatures above 250K at N_D $<10^{16}$ cm^{-3}.

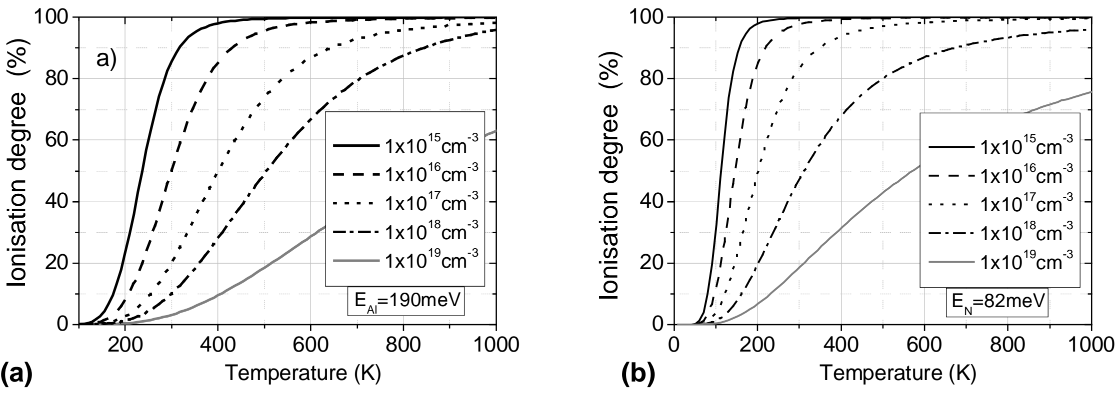


Figure 2.2 Ionisation degree of *Al* (a) and *N* (b) in electrothermal equilibrium.

2.1.4 Recombination Models

U_n and U_p in Eq. 2.2 represent the net electron and hole recombination, respectively. These net recombination are the result of three main processes: Shockley-Read-Hall (SRH) recombination, Auger recombination, and direct recombination (also known as band-to-band or optical recombination).

SRH recombination

Schottky, Read, and Hall (SRH) described the recombination process with the phonon transitions by the way of defects or traps. The SRH recombination rate is given by

$$U_{SRH} = \frac{np - n_i^2}{\tau_p \left[n + n_i \, exp\left(\frac{E_{TRAP} - E_i}{k_B T} \right) \right] + \tau_n \left[p + n_i \, exp\left(\frac{E_i - E_{TRAP}}{k_B T} \right) \right]} \tag{2.11}$$

where E_{TRAP} -E_i is the distance between the trap level and the intrinsic Fermi level, and τ_n, and τ_p are the lifetime of electrons and holes at low injection, respectively. The lifetimes can be concentration-dependent and can be described by the Selberherr relation:

$$\tau_p = \frac{\tau_{po}}{1 + \left(\frac{N_D + N_A}{N_p^{SRH}} \right)} \qquad \tau_n = \frac{\tau_{no}}{1 + \left(\frac{N_D + N_A}{N_n^{SRH}} \right)} \tag{2.12}$$

Measured carrier lifetimes in 4H-SiC range from a few hundred nanoseconds up to some microseconds and generally they are correlated to the thickness and quality of epitaxial layers. For our simulations we will use the values:

$$\tau_{no} = 5 \cdot 10^{-7}\ \text{s}\ ,\ \tau_{po} = 1 \cdot 10^{-7}\ \text{s} \qquad ; \qquad N_p^{SRH} = 1 \cdot 10^{30} \text{cm}^{-3}\ ,\ N_n^{SRH} = 1 \cdot 10^{30} \text{cm}^{-3}$$

taken from reference [68].

Auger recombination

Auger recombination, which is an important model parameter for high-power device design, occurs both at high doping level and in the high injection regime due to the direct band-to-band recombination between an electron and a hole across the forbidden gap, accompanied by the transfer of energy to other free electron or hole. It is given by equation (2.13), where $C_{n,p}$ are the Auger coefficient for electrons and holes, and their sum is extracted from the measurement in the high-level injection regime.

$$U_{Auger} = \left(C_n n + C_p p\right)\left(np - n_i^2\right) \tag{2.13}$$

The values we used for C_n and C_p are 5×10^{-31} and 2×10^{-31} $cm^{-6}s^{-1}$, respectively for *n*-type 4H-SiC at room temperature [73].

Direct recombination

Direct band-to-band transitions of a thermal generation process happens most likely in direct-bandgap semiconductors and the thermal-generation rate of this process is directly proportional to the intrinsic concentration, according to the simple relation,

$$U_{dir} = C_d\left(np - n_i^2\right) \tag{2.14}$$

Knowing that SiC is an indirect and wide-bandgap semiconductor with extremely low intrinsic-carrier concentration, n_i^2 is so small for 4H SiC that the thermal-generation rate can be neglected. So, the generation of carriers at room temperature by this type of transition is almost impossible to happen in SiC.

2.1.5 Mobility Models

It is well known that an accurate *I-V* model is strongly based on physical and accurate mobility and velocity saturation models for any devices. At low electric fields, the carrier mobility in a semiconductor is a function of the total doping concentration and the temperature. As in the case of Si, lattice scattering (acoustic phonons) and ionised impurity scattering, together with anisotropic scattering, seem to be the most relevant mechanisms to limit the mean free path of carriers at low electric fields in SiC [74]. Since the free-carrier mobilities depend strongly on the magnitude of electric field, the mobility model in MEDICI consists of low field and high field mobility components. An optional module that described the anisotropic mobility is also available.

Low field mobility

The carrier mobilities μ_n and μ_p account for the scattering mechanisms in electrical transport. Physically the electron mobility describes the electron drift velocity v under the influence of an electric field according to

$$\vec{v} = \mu \cdot \vec{E} \tag{2.15}$$

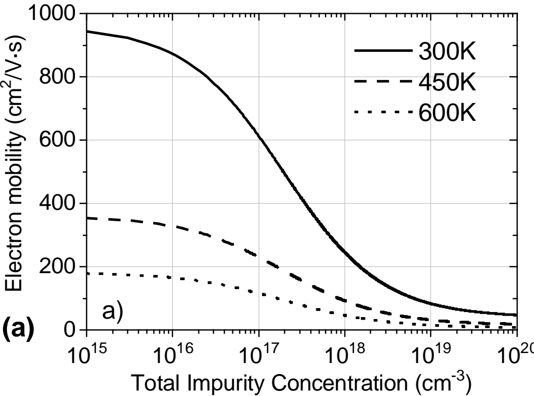
At low electric fields the electron velocity increases almost linearly with field and the mobility has the constant value μ_0 (low-field mobility). The low-field mobility is a function of the doping concentration and temperature. A widely used empirical expression for modelling the doping and temperature dependence of the low-field mobility is given by

$$\mu_\nu(N,T) = \mu_\nu^{min}\left(\frac{T}{T_O}\right)^{\alpha_\nu^{mob}} + \frac{\mu_\nu^{T_O}\cdot\left(\frac{T}{T_O}\right)^{\alpha_\nu^{mob}} - \mu_\nu^{min}\left(\frac{T}{T_O}\right)^{\alpha_\nu^{mob}}}{1+\left(\frac{N_D+N_A}{N_\nu^{mob}}\right)^{\gamma_\nu^{mob}}} \quad \text{where} \quad \nu = n \text{ or } p \tag{2.16}$$

where N_D and N_A are the density of donors and acceptors, respectively. The mobility is more anisotropic for 6H-SiC than it is for 4H-SiC. Schaffer et al. [75] presented the results from measurements of electron and hole majority carrier mobilities in both 4H- and 6H-SiC as functions of temperature, doping, and directions in epitaxially grown crystals. The parameter values of Eq. 2.16 for 4H-SiC are extracted from the work of Mnatsakanov *et al.* [76] and are summarized in Table 2.2 below. Figure 2.3 shows the low field mobilities of μ_n and μ_p as a function of the doping concentration at different temperatures (300K, 450K, and 600K) for 4H-SiC, respectively.

Table 2.2 4H-SiC mobility parameters.

	μ_n^{To} [cm^2/Vs]	μ_n^{min} [cm^2/Vs]	N_n^{mob} [cm^{-3}]	γ_n^{mob}	α_n^{mob}
Electrons	950	40	1.94×10^{17}	0.76	-2.6
Holes	117	16	1.76×10^{19}	0.34	-2.6



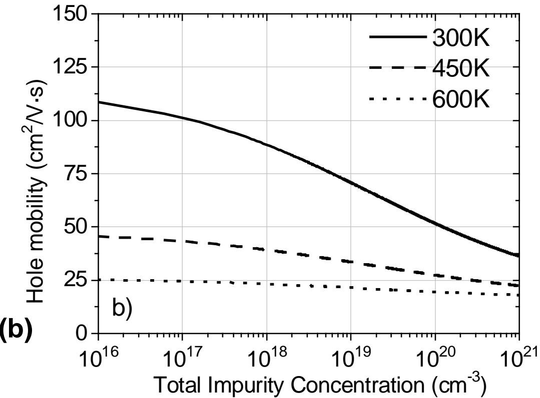


Figure 2.3 Calculated mobility values for, (a) electrons and (b) holes in 4H-SiC as a function of doping concentration at different temperatures.

High field mobility

The low field mobility in SiC is not high compared to other semiconductor materials. Nevertheless, at high fields, the carrier drift velocity v saturates due to the increase of the optical phonon scattering and reaches the saturation velocity v_{sat}, which is two times higher than in Si. The high drift mobility in SiC can be described by the same model as Si;

$$\mu_\nu(E) = \frac{\mu_\nu^o}{\left[1+\left(\frac{\mu_\nu^o \cdot E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \qquad \textit{where} \qquad \nu = n \text{ or } p \tag{2.17}$$

where μ_ν^o is the low field carrier mobility, v_{sat} is the saturation velocity, E the electric field, and β is a fitting parameter. For 4H-SiC Khan *et al.* [77] reported the values β=1.2 and v_{sat}=2.2×10^{7}cm/s. The temperature dependence of v_{sat} and β can be modelled by

$$v_{sat}(T) = v_{sat}^o \left(\frac{T}{T_o}\right)^{\delta_{sat}} \qquad\qquad \beta(T) = \beta^o \left(\frac{T}{T_o}\right)^{\alpha_{sat}} \tag{2.18}$$

with δ_{sat} = -0.44 and α_{sat}=1 for 4H-SiC [63]. Figure 2.4 shows the electron drift velocity versus the electric field for T=300K and T=600K. All measured data refer to a current flow perpendicular to the c-axis (usual growth axis of epilayers). No measured data of holes is presently available.

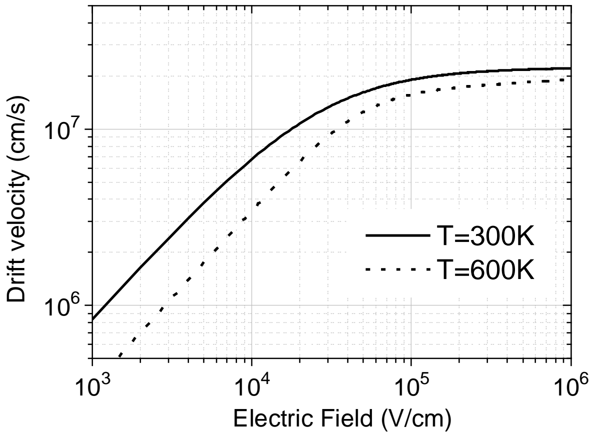


Figure 2.4 Electron drift velocity as a function of electric field in 4H-SiC at T=300K and T=600K.

Anisotropy in mobility

The hexagonal SiC substrates are typically cut perpendicular or offset a few degrees to the c-axis of the crystal. Thus one needs to be concerned with the carrier mobility either perpendicular to the c-axis (in direction of the basal of the crystal) or parallel to the c-axis, depending on the device structure and operation. In all hexagonal type SiC polytypes, the

carrier transport properties exhibit an anisotropic behaviour with regard to crystallographic orientation in each polytype. Measurements of the electron mobility anisotropy in *n*-type 6H and 4H SiC using the Hall effect and through Montecarlo calculations have been studied in [76, 78-80]. These studies show an agreement of a ratio value of μ(1120)/μ(0001)=0.83 for 4H-SiC and this ratio is temperature independent in homogeneous samples [81].

The high field mobility model (Eq. 2.17) expresses the dependence of carrier mobility on the component of electric field that is parallel to the current flow. Due to anisotropic behaviour of SiC material, the effects caused by anisotropic in scattering need to be included in the device model. In MEDICI, the so-called Anisotropic Material Advanced Application Module (AM-AAM) can be used to model the anisotropic properties within semiconductor materials. The carrier mobility tensor, (X, Y, Z), can be used in AM-AAM as to model the anisotropic mobility behaviour. This tensor is a dimensionless vector that multiplies the normal carrier mobility as calculated using the selected mobility models. Thus in the case of 4H SiC, a tensor of (1, 0.83, 1) is included in the mobility model.

2.1.6 Impact ionisation

The breakdown voltage of a power semiconductor device is one of its most important characteristics. Together with its maximum current handling capability, this parameter determines the power rating of the device. Depending on the application of the power device, its breakdown voltage can range from as low as 25V for high-speed output rectifiers used in switching power supplies for integrated circuits to over 10kV for thyristors used in high-voltage DC transmission networks. In these devices, the voltage is supported by a depletion layer formed across either a *PN* junction, a metal-semiconductor interface (Schottky barrier), or a metal oxide-semiconductor interface (MOS). The high electric field that exists across the depletion layer is responsible for sweeping out any holes or electrons that enter this region, by either the process of space-charge generation or diffusion from the neighbouring quasi-neutral regions. As more voltage is applied across the depletion layer, the electric field increases and the mobile carriers are accelerated to higher velocities. In SiC, when the electric field exceeds 2×10^6 V/cm, the mobile carriers attain a saturated drift velocity of about 2×10^7 cm/s. At higher electric fields, these carriers have sufficient energy that their collisions with the atoms in the lattice can excite valence band electrons into the conduction band. This process for the generation of electron-hole pairs is called *impact ionisation*. Since the electron-hole pairs created in the depletion layer by the impact ionisation process undergo acceleration by the existing electric field, they also participate in the creation of further electron-hole pairs. Consequently, impact ionisation is a multiplicative phenomenon that leads to a cascade of mobile carriers transported through the depletion layer. The device is considered to undergo

avalanche breakdown when the rate of impact ionisation approaches infinity because it cannot support an increase in applied voltage. Avalanche breakdown represents a fundamental limitation to the maximum operating voltage of power devices.

To characterize the impact ionisation process it is useful to define ionisation coefficients. The impact ionisation coefficient for electrons (α_n) is defined as the number of electron-holes pairs created by an electron crossing 1cm through the depletion layer along the direction of the electric field. The same definition is applied for the hole ionisation coefficient (α_p). The model commonly used in the device simulator to calculate the impact ionisation coefficients is based on the model suggested by Chynoweth [82];

$$a_n(x) = a_n \cdot exp\left(\frac{-b_n}{E(x)}\right) \quad ; \quad a_p(x) = a_p \cdot exp\left(\frac{-b_p}{E(x)}\right) \qquad (2.19)$$

where $E(x)$ represents the magnitude of the electric field and $a_{n,p}$ and $b_{n,p}$ are fitting parameters.

The reports of measurements of the impact ionisation coefficients of 4H-SiC are few, and they are not in agreement with one another [83-86]. Generally, the impact ionisation coefficients of electrons are significantly smaller than those of holes. Recently, it was shown that a significant reduction of the breakdown field in 4H-SiC occurs when the electric field is applied perpendicular to the *c*-axis [87]. In order to predict the breakdown voltage of a real power device precisely, it must considered the anisotropy of impact ionisation coefficients, because the direction of the electric field at the field crowding part is not necessarily parallel to the *c*-axis when the reverse bias is applied, even if the device is fabricated on (0001) 4H-SiC wafer. Hatakeyama *et al.* [85] reported the impact ionisation coefficients of 4H-SiC for $\langle 0001 \rangle$ and $\langle 11\bar{2}0 \rangle$ directions that reproduce avalanche breakdown behaviour of p^+n diodes on (0001) and $(11\bar{2}0)$ epitaxial 4H-SiC wafers. Table 2.3 summarizes the newly reported impact ionisation coefficients by Hatakeyama *et al.* in comparison with the traditional commonly accepted values for 4H-SiC reported by Konstantinov *et al.* [83]. Figure 2.5 shows the resulting avalanche breakdown voltages as a function of doping density of the *n*-epitaxial layer for the two previously reported set of parameters. The anisotropy of the impact ionisation coefficients is due to the highly anisotropic band structure of 4H-SiC, which is derived from a long period along the *c*-axis of the crystal structure of 4H-SiC.

Table 2.3 Parameters of the electron and hole impact ionisation coefficients for 4H-SiC.

	Axis direction	a_n [cm^{-1}]	b_n [V/cm]	a_p [cm^{-1}]	b_p [V/cm]
Hatakeyama [85]	(0001)	1.76×10^8	3.30×10^7	3.41×10^8	2.50×10^7
	$(11\bar{2}0)$	2.10×10^7	1.70×10^7	2.96×10^7	1.60×10^7
Konstantinov [83]	(0001)	4.07×10^5	1.67×10^7	1.63×10^7	1.67×10^7

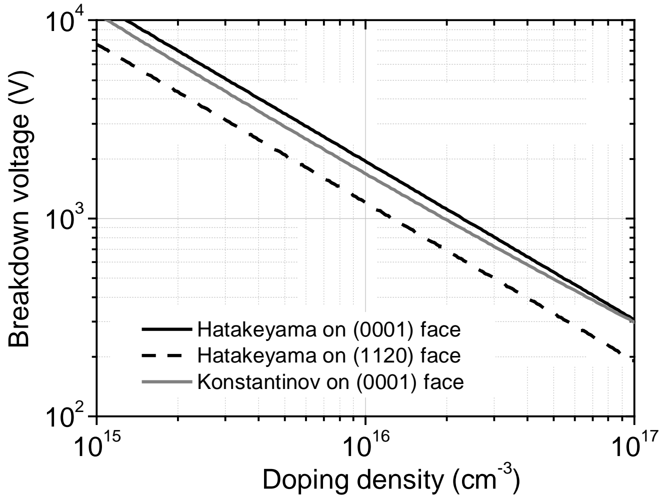


Figure 2.5 Avalanche breakdown voltage of a p^+n diode as a function of doping density of the *n*-epitaxial layer. The curves shown are derived from the impact ionisation coefficients reported in references [85] and [83].

To compute the avalanche breakdown voltage, it is necessary to determine the condition under which the impact ionisation achieves an infinite rate. A detailed description of the avalanche multiplication process can be found in any power device semiconductor book [87,88]. Avalanche breakdown is defined to occur when the total number of electron-hole pairs *M(x)*, also commonly known as the multiplication coefficient, tends to infinity. It can be concluded that this will occur when

$$\int_0^W a_n \cdot exp\left[\int_0^x (a_p - a_n)dx\right]dx = 1 \tag{2.20}$$

The expression on the left-hand side of Eq. (2.20) is known as the ionisation integral. Calculation of the breakdown voltage of devices is generally performed by evaluation of this integral either in closed form or by numerical techniques.

An important property for the application in power devices is the temperature coefficient of the avalanche breakdown voltage. If the breakdown voltage was decreasing at higher temperatures, a local avalanche and the self-heating caused by its breakdown current would cause a filamentation of the leakage current, possibly leading to catastrophic device failure. First measurements of breakdown voltages in silicon carbide diodes seemed to indicate such a negative temperature coefficient of the breakdown voltage. It was later shown that the temperature coefficient of the breakdown voltage in defect-free 4H-SiC actually was positive [86,89,90].

2.2 4H-SiC PiN Diode Design for the 1.7kV Power Range

2.2.1 Punch-through diode

In the case of the breakdown voltage calculation treated in section 2.1.6 (Fig 2.5), it was assumed that the lightly doped side of the junction extends beyond the edge of the depletion layer under avalanche breakdown conditions. In bipolar devices, where the lightly doped side of the junction is flooded with minority carriers during current conduction, it is often preferable to achieve a desired breakdown voltage by using a punch-through structure. In the punch-through case, the drift region is designed so that the depletion region reaches the highly doped N^+ substrate before junction breakdown occurs, see Fig. 2.6.

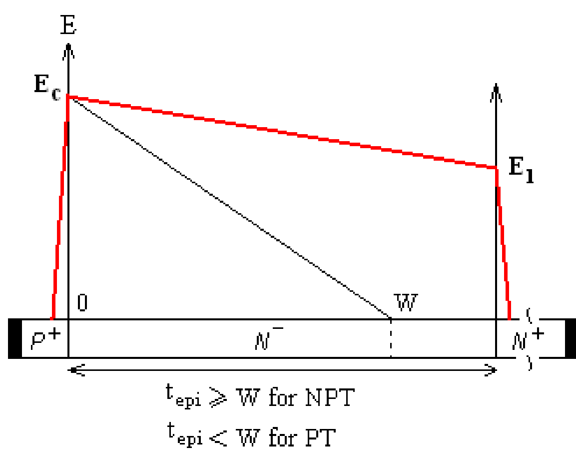


Figure 2.6 Definition of a punch-through (*PT*) and non punch-through (*NPT*) design for a *PiN* diode. The optimal epilayer *N* doping is not equal for the *PT* and *NPT* case.

For a non punch-through design the voltage supported by the N^- drift region is given by;

$$V_{B,npt} = \frac{E_C \cdot W}{2} \tag{2.21}$$

where E_C is the critical electric field and t_{epi} is the epilayer thickness.

For a punch-through design the blocking voltage is:

$$V_{B,pt} = \frac{(E_C + E_1) \cdot t_{epi}}{2} \tag{2.22}$$

where E_1 is the electric field at the epilayer-substrate (N^-/N^+) junction.

Assuming an abrupt $P^{+}N$ junction, the electric field varies linearly with distance and it can be proved that

$$E_1 = \frac{q \cdot N_A \cdot t_{epi}}{\varepsilon} \tag{2.23}$$

where N_A is the doping concentration of the epilayer and ε is the dielectric constant of the semiconductor material. Substituting Eq. 2.23 into Eq. 2.22, it can be shown that,

$$V_{B,pt} = \frac{E_C \cdot t_{epi}}{2} + \frac{q \cdot N_A \cdot t_{epi}^2}{2 \cdot \varepsilon} \tag{2.24}$$

The breakdown voltage of punch-through diodes can be calculated by using this expression together with the corresponding critical electric field for 4H-SiC [85]. The results obtained for several base region widths are provided in Fig. 2.7. Note that the breakdown voltage goes through a maximum when the doping level changes. This is due to a decrease in the electric field for breakdown when the doping level decreases.

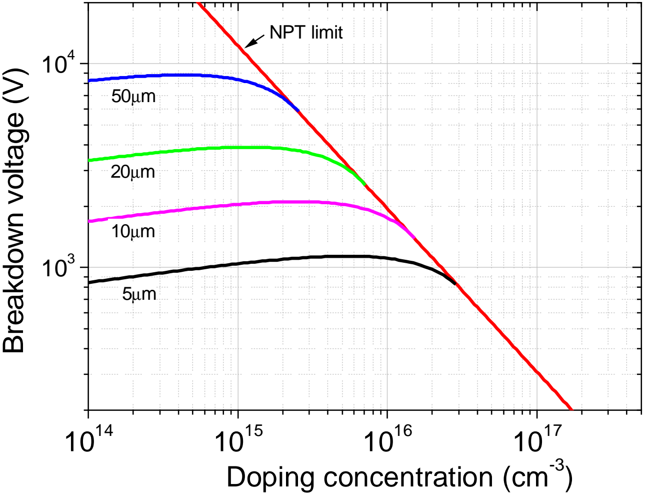


Figure 2.7 Calculated breakdown voltages for 4H-SiC diodes as a function of the low-doped epilayer thickness and doping. The diagonal red line marks the non punch-through limit.

The advantage by using a punch-through (*PT*) design is that the drift region thickness can be made thinner than for the non punch-through (*NPT*) case for the same breakdown voltage. Consequently, an improvement in the drift region resistance is obtained if epitaxial layer thickness and doping level are optimised. The second advantage is that the doping can also be made lower for the same drift region resistance as for a *NPT* design. Thus the breakdown voltage is less dependent on the doping compared to the *NPT* case. Usually a *PT* structure is designed with both lower epilayer thickness and doping.

2.3 Edge Termination Design and Optimisation

This chapter has so far only considered one-dimensional structures where the electric field vector was perpendicular to the sample surface. In real devices, however, the junction shows curvatures and the device geometry shows edges, where the peak electric field will be increased due to field crowding. Since the breakdown voltage of a device is closely related to the maximum electric field at the junction of the devices, areas of increased electric field will significantly reduce the ability of power devices to withstand and block high reverse voltages. Electrical breakdown will preferably occur at the periphery of the three-dimensional junction if the maximum electric field in these areas is not reduced by proper edge termination techniques. In fact, the edge termination limits the breakdown voltage of practical devices to below the "ideal" limits set by the semi-infinite junction analysis. If the junction is poorly terminated, its breakdown voltage can be as low as 10-20% of the ideal case.

The study of device terminations is an intensively researched topic that has resulted in the development of a large variety of innovative designs currently used in silicon technology. They have to be adapted to silicon carbide technology taking into account the unique technological processing constraints of this semiconductor material. The development of two-dimensional numerical solution techniques allows the design of edge terminations with a high degree of confidence.

Many techniques have been employed to solve this periphery problem. Guard rings [91], field plates [92], argon implantation [93], and junction termination extensions (JTEs) [94,95] have been used for planar SiC devices. Bevelled sidewalls [96] and multiple-step etching [97], as well as mesa-JTEs [98], have been used for mesa-isolated SiC devices. These methods have been successful for the most part, but each method has its particular drawbacks. Guard rings are often difficult to optimise and fabricate; field plates are limited by the strength of the dielectric used; argon implantation can increase reverse leakage current; bevelled etching is less effective with abrupt, one-sided negative junctions; and multiple-step etching complicates the bevelling process with additional fabrication steps. Junction termination extensions have been widely used, but JTEs are difficult to optimise and often require multiple zones of decreasing implant dose in order to achieve ideal breakdown for a junction.

Our aim is to develop proper edge termination techniques for planar 4H-SiC bipolar power diodes. Single JTE design will be analysed in detail for many epitaxial drift layer configurations while double JTE, multiple guard rings, and the novel developed "guard rings assisted JTE" structure will be optimised for the 1.7kV power range. For this power range an n-type epitaxial layer of 10µm thickness and 9×10^{15}cm^{-3} doped was used for the simulations.

Breakdown analysis was performed by calculating the electron and hole integral along potential gradients paths through the device structure at each potential update. Maximum blocking voltage was determined when the calculated ionisation integral exceeded unity. To

make simulation more accurate to real devices the p-type doping profiles were introduced using a specific SiC implantation simulator developed at CNM [99]. All simulations were performed at 300K.

2.3.1 Single zone JTE

The junction termination extension (JTE) has become the most prevalent edge termination method for SiC planar devices because of its ease design and fabrication, and the potential high ideal breakdown values they can achieve. The JTE technique consists in extending the highly doped main junction by a connected surrounding region of the same type but presenting a lower doping level, in order to allow the spreading of the equipotential lines emerging below the junction edge curvature towards the surface. The JTE layer is designed so that is fully depleted at the maximum blocking voltage, acting as a high resistivity layer able to support the high fields. Figure 2.8 shows a schematic cross-section view of the diode with planar single JTE structure. Simulations were performed in rectangular coordinates with the left boundary of the structure in Fig. 2.8 representing a symmetry axis, thus leading to simulation of a half-cell of the diode. The extension in the third dimension is assumed to be infinite (two-dimensional simulation).

Traditional JTE designs required precise control of dopants in the JTE layer in order to totally deplete it at the desired blocking voltage. For a given doping and thickness of the diode epitaxial layer, the doping level and extension junction length are the main parameters affecting the blocking voltage.

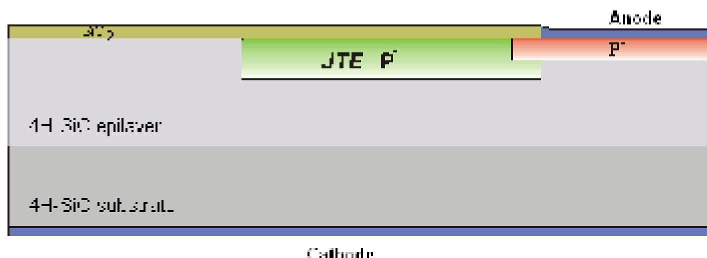


Figure 2.8 Schematic cross section of a PiN diode with JTE structure.

JTE dose optimisation

For maximum effectiveness, the charge in the JTE layer is typically designed so that at the desired blocking voltage, the dopants in the JTE are fully depleted and act as a high resistivity layer in which to support the high surface and bulk fields. Thus, the carrier freeze-out due to the high ionisation energies in SiC plays no role in the JTE efficiency, and all introduced dopants in substitutional positions act as an active dopant. Without enough active dopants in

the JTE, the extension layer will deplete at a much lower voltage and result in premature breakdown at the corner of the main junction. Excess of active dopants in the JTE will prevent the region from fully depleting and will act as an extension of the main junction, causing the breakdown to occur at the outermost JTE edge. Hence, in order to achieve maximum efficiency, the amount of dopant charge in the JTE layer must be precisely controlled.

From an ideal one-dimensional analysis, the optimum amount of charge needed (Q_I) in the JTE to be fully depleted is simply the given critical electric field (E_C) at breakdown, multiplied by the dielectric constant of the material (e_s). Assuming the variation of the critical electric field with epilayer doping concentration given recently by Hatakeyama et al. [85], Fig. 2.9 shows the ideal implanted charge for a given drift layer, along with the simulation results. To make simulation more accurate to real fabricated devices the *p*-type doping profiles were introduced using the specific SiC implantation simulator developed at CNM [99]. The doping level and depth of the emitter doping profile were 2×10^{19}cm^{-3} and 0.25µm, respectively. The JTE doping level varied as a function of the total implanted dose with a constant depth of 0.8µm. The epilayer thickness for the simulations was 10µm and the JTE length was set to 100µm to achieve the highest percentage of the plane parallel breakdown value. As it can be observed, a great accordance between the theoretical curve and the simulation results is obtained. With the optimum charge, breakdown voltages to within 95% of the parallel-plane case can be achieved.

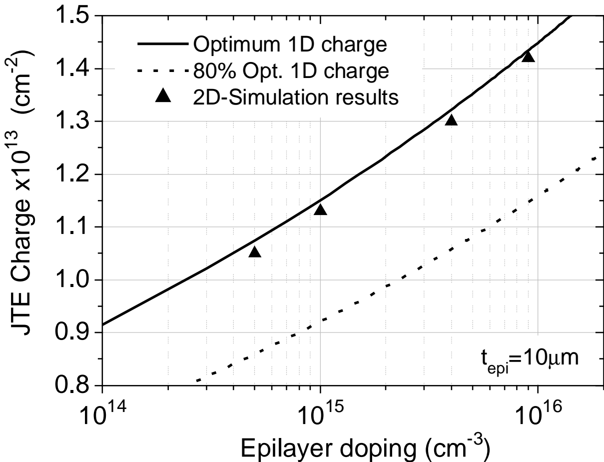


Figure 2.9 1-D theoretical and 2D simulated optimised planar JTE charge. 80% of the optimum 1D charge is plotted for reference.

A more detailed plot of each optimal JTE dose (i.e. ideal charge Q_I) value is shown in Fig. 2.10. It is obvious from the narrow peak in the dose *vs.* breakdown curves in Fig. 2.10 that for a drift layer doping concentration greater than about 1×10^{16}cm^{-3}, the JTE doping concentrations must be very precisely controlled in order to achieve the maximum breakdown voltage. On the other hand, JTE concentration in lightly doped epilayers can have a significant variation from the ideal JTE dose with little degradation in efficiency. Since most

power devices will require drift layer concentrations below $1\times10^{16}cm^{-3}$, an error of up to 25% in the activation process can be tolerated with only a 10% decrease in blocking capability. From the curves shown in Fig 2.10, it is concluded that special care must be considered in not to introduce doses higher than the optimum one, since the reduction of the breakdown voltage is much more pronounced for this range of doses than for doses lower than the ideal JTE charge.

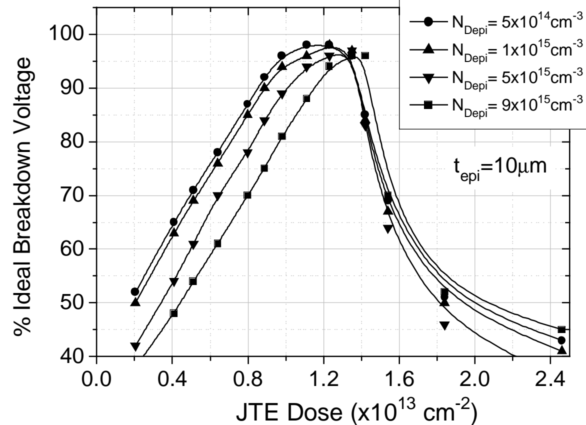


Figure 2.10 Dependence of the breakdown voltage with variation in JTE dose for several epilayer concentrations.

Although the ideal charge will in theory give the maximum breakdown voltage, it has been shown in Si devices that including only a fraction of the ideal charge, usually 60-80% of Q_I [88], can help in controlling high surface fields. These high surface fields can lead to a number of detrimental effects in power devices, including: excess leakage, breakdown walkout, and premature breakdown at the surface of the device due to trapped charges or defects [100]. Fig. 2.11 shows the simulated normalized electric field (peak surface field/ peak bulk field) as the JTE dose is varied from 50 to 150% of Q_I for two different epilayer doping levels. As it can be deduced from the analysis of Fig 2.10 and 2.11, for a structure with blocking layer concentration of $9\times10^{15}cm^{-3}$, a reduction of the optimum charge in JTE to $0.8Q_I$ results in a normalized field of ~0.7 while the blocking voltage remains near 90% of the ideal parallel plane value. Therefore, including only about 80% of the optimum JTE dose should give a good trade-off between the blocking capabilities and the reduction of surface fields in SiC devices.

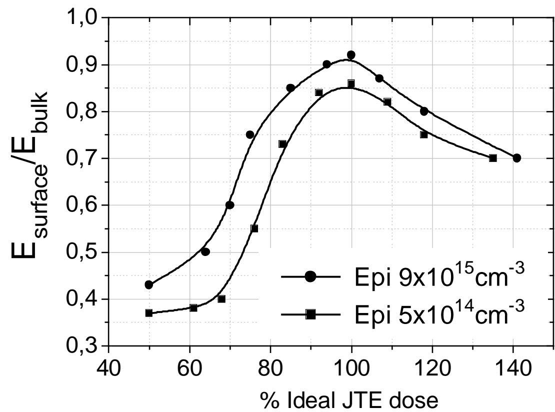


Figure 2.11 Simulated normalized peak electric fields *vs.* percentage of ideal charge in JTE layer.

Doping profile optimisation

To further allow a greater reduction of the surface electric field we have investigated the influence of the JTE doping profile near the surface. As the doping process in SiC must be carried out by ion implantation technique due to the extremely low diffusivity of dopants, we can displace the impurity concentration from the surface by increasing the first ion implantation energy. Fig. 2.12 shows the simulated doping profiles for increasing values of the lowest implantation energy defining a box-like aluminum profile with the 80% of the optimum dose for the 9×10^{15}cm^{-3} epilayer doping case.

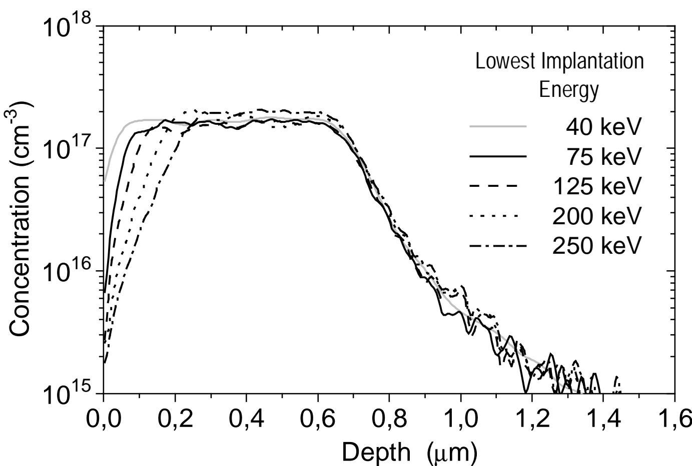


Figure 2.12 Simulated aluminum doping profiles for different values of the first implantation energy.

Table 2.4 Maximum values of bulk and surface electric field at breakdown as a function of the first implantation energy, for the box-like aluminum implantations profiles displayed in figure 2.12.

Lowest impl. energy	E_{bulk} (MV/cm)	$E_{surface}$ (MV/cm)	***Norm. field*** (E_{surf}/E_{bulk})
40 keV	2.82	2.03	0.72
75 keV	2.75	1.89	0.68
125 keV	2.70	1.72	0.64
200 keV	2.86	2.05	0.71
250 keV	3.05	2.42	0.79

Table 2.4 shows peak values of bulk and surface electric field at breakdown as a function of the first implantation energy (profiles shown in Fig. 2.12). It can be concluded that with a surface depletion of aluminum doping we can achieve a reduction of the surface electric field at breakdown up to 15% without degradation in blocking capabilities. Moreover, it has to be noticed that the normalized field (E_{surf}/E_{bulk}) also shows a great reduction due to the surface depletion of the doping profile. This surface electric field peak reduction is due to the formation of a weak second field peak at the anode edge, that alleviates the field at the end of the JTE, as it can be seen in Fig. 2.13. This fact is important in reducing reliability

degradation due to possible charge buildup in the passivation layer. Thus, an aluminum implantation profile with a first implantation energy value of 125keV proves to be a good choice in order to alleviate the surface field and reach high breakdown voltages.

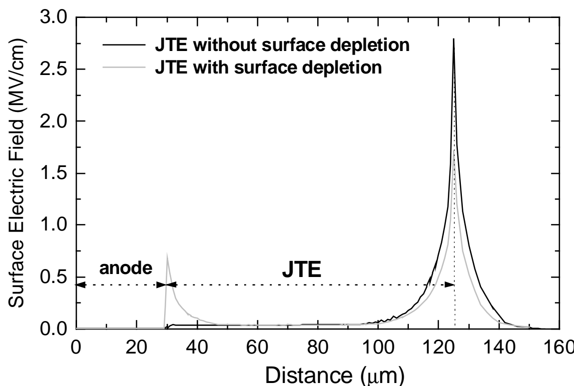


Figure 2.13 Surface electric field distributions for two different JTE doping profiles. The black line corresponds to a profile without surface depletion (first ion implantation energy of 20keV). The red line corresponds to a profile with surface depletion (first ion implantation energy of 125keV).

JTE length optimisation

The length of the JTE is an important aspect that has a significant effect on breakdown voltage and thus is important in maximizing available substrate area. Temple et al. [101] has investigated the required JTE length through breakdown experiments with silicon diodes of varying extension length, and have fit their results to the following empirical equation:

$$\frac{V_B}{V_{B,ideal}} = 1 - exp\left(-\frac{L_{JTE}}{W_C} \right) \tag{2.25}$$

where (L_{JTE}/W_C) is the JTE´s geometrical factor (the JTE length normalized to the epilayer critical depletion width). In our case, the epilayer is fully depleted when reverse breakdown occurs (punch-through); thus the critical depletion width equals the epilayer thickness.

Equation 2.25 is plotted in Fig. 2.14 together with our simulation results on optimum JTE length for two epilayer thickness and two different epilayer dopings. The simulations results and the curve obtained from the empirical equation are in good agreement, and indicate that in order to achieve a high percentage of the parallel plane breakdown value, the JTE length must be approximately three times the epilayer thickness. However, our simulations results on electric field strength suggest that the JTE length should be extended to about five times the epilayer thickness as a technique to further relax surface fields. It can also be observed in Fig. 2.14 that there is a slight degradation of the JTE efficiency as the epilayer thickness increases. This could be due to the increased field crowding at the relatively shallow SiC JTE as the substrate depletion width increases.

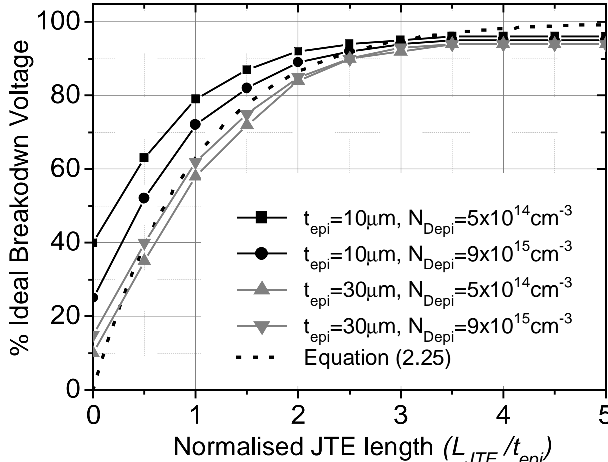


Figure 2.14 Dependence of breakdown voltage on the normalised JTE length for two different epilayer thickness and doping.

Although it is an important design variable in most existing Si edge termination techniques, the junction depth of the JTE implant has little effect on the termination efficiency in SiC because the electric field along the JTE spreads laterally instead of increasing the effective junction radius of curvature. However, simulations performed with various junctions depths of the JTE doping profile keeping the same implanted dose revealed a lower normalized field for the 0.6-0.9μm junction depth range.

2.3.2 Double zone JTE

Since a reduction of JTE charge to decrease the peak surface electric field would result in a significant blocking capability loss, the multiple zone JTE structure was proposed to allow further control of peak electric fields without compromising the breakdown voltage. Due to the technological process constraints of SiC that require of ion implantation to introduce the impurities in the selective area regions, we have considered the double zone JTE structure as an edge termination that provides an acceptable trade-off between technological process complexity and reachable blocking capabilities. The double JTE structure is similar to a single JTE layer, but with two unequally doped regions JTE1 and JTE2, see Fig. 2.15.

The doping concentration in JTE1 is larger than that in JTE2. In this way JTE2 will be fully depleted at a lower voltage than JTE1, moving a second electric field peak to the JTE1/JTE2 junction, thus reducing the overall surface electric field peak. The doping ratio between JTEs is of great importance since, if the implantation dose of the first JTE is too high, the breakdown will occur prematurely at its edge, the second JTE becoming less effective. On the contrary, if it is too low the structure will become less electric field relaxed. Another benefit from the double JTE configuration comes from the fact that we get a wider optimum impurity dose range for the JTE2 (which mainly determines the breakdown voltage).

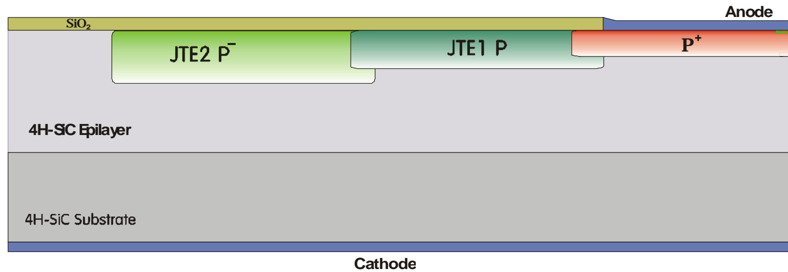


Figure 2.15 Schematic cross-section of a double zone JTE in a side by side configuration.

The surface electric field profiles for an optimised JTE of length 100μm and a double JTE structure of length 50μm for JTE1 and 50μm for JTE2 are shown in Fig. 2.16. As it can be seen, with the addition of the second zone, the peak field is effectively split into two peaks of significantly lower field strength. In order to reduce the fields further, this concept can be extended to multiple zone JTE structures with 3 or more JTE zones. Unlike for Si devices where individual zones can be created during the same fabrication process by using a graded or non-linear spaced diffusion mask, each zone in SiC devices must be implanted separately, thus increasing processing complexity. An alternative method would require a deep single implant, and then a selective etch-back of each zone in order to provide the required charge [97]. However, this approach requires several additional mask steps and may introduce reliability concerns from etch-induced passivation defects along the plasma etched surfaces and sidewalls [100].

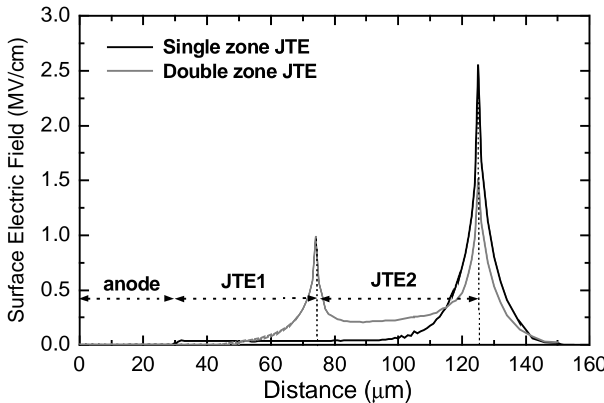


Figure 2.16 Simulated surface electric field profiles for an optimised single JTE (100μm) and double zone JTE structures (50μm each zone)

Two types of double JTE configurations have been considered: a side by side design (Fig. 2.15) and a JTE1 embedded into the JTE2 region (Fig. 2.17). In the case of the side by side configuration there is an overlap of five microns between the two zones to take into account possible misalignments in the technological process. From simulations, similar results have

been obtained in terms of blocking capabilities and electric fields for the two configurations although from the technological point of view the embedded configuration is expected to have better reproducibility since it is a more flexible design.

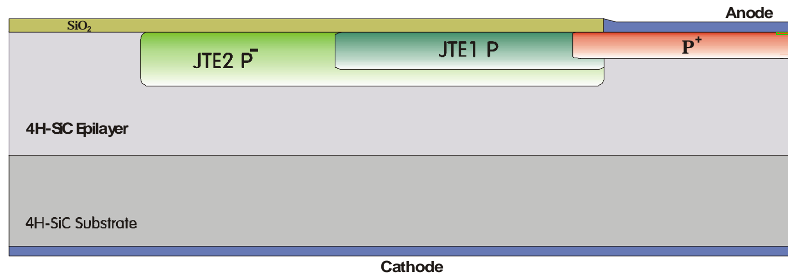


Figure 2.17 Schematic cross-section of a double zone JTE in a embedded configuration.

Another benefit of the double JTE configuration is that we obtain a wider optimum impurity dose range for the JTE2, which mainly determines the value of the breakdown voltage. To account for the optimum doping relation when maximum breakdown voltage and minimum electric peak are achieved, JTE1 is implanted with a $1\times10^{14}cm^{-2}$ and 0.5µm depth doping profile, keeping JTE2 the same values as in the single case ($1.2\times10^{13}cm^{-2}$, 0.8µm).

In Fig. 2.18 it can be seen that the range of the impurity doses for obtaining high breakdown voltages is extended toward the lower impurity dose of the JTE layer, in comparison with the single JTE structure. The data correspond to an epilayer configuration of 10µm thick and $9\times10^{15}cm^{-3}$ doping level , with an ideal plane parallel breakdown voltage of 1900V.

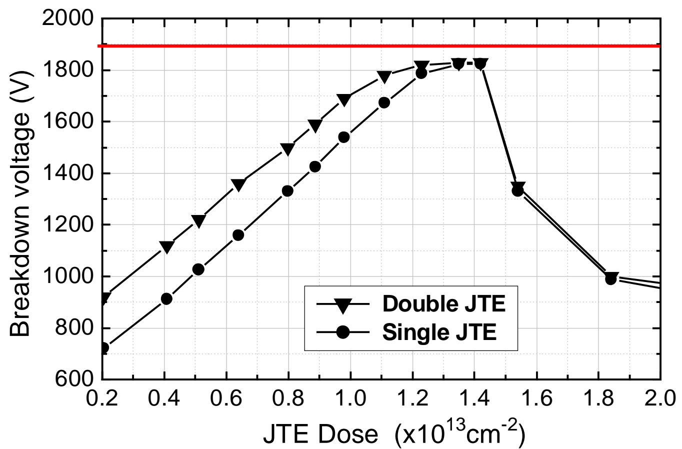


Figure 2.18 Simulated breakdown voltage *vs.* dose for the single JTE (-▼-) and double zone JTE (-●-) structures. The JTE dose in double zone structure corresponds to JTE2.

2.3.3 Multiple Floating Guard Rings

The multiple floating guard ring (FGR) structure (Fig. 2.19) has been widely used in Si technology as an effective means of planar edge termination [102]. It is an attractive method of edge termination since it is usually formed simultaneously with the main junction or anode contact, thus saving costly processing steps. The guard ring structure serves to reduce the amount of field crowding at the main junction by spreading the depletion layer past consecutively lower potential floating junctions (rings). A ring becomes biased when the spreading depletion layer punches through to the floating junction. To remain in equilibrium, the ring´s potential will follow that of the surrounding material to within the built-in potential of the junction. These independent junctions act to increase the depletion layer spreading, thereby decreasing the high electric field at the main junction. Optimised designs have the electric field shared equally among the main junction and floating guard rings.

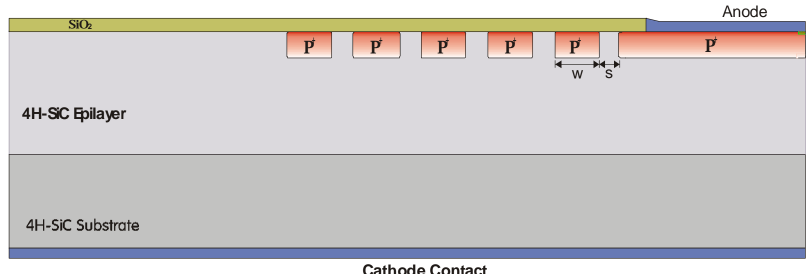


Figure 2.19 Schematic cross section of an implanted *pn* diode with multiple floating guard rings.

The optimisation of floating guard ring structures is extremely complex, with the results being strongly coupled to both solution method and grid conditioning [103]. To simulate the potential in the floating guard rings, the hole quasi-Fermi potential must be calculated independently for each p^+-floating ring. Therefore, a coupled solution of both Poisson´s equation and both current continuity equations must be used for accurate results. Device gridding was also determined to play a significant role in convergence stability. Since the gridding requirements vary with device structure and solution method, correct meshing techniques are difficult to relate quantitatively and are often gained heuristically through trial and error. We have found that a minimum gridding of 0.05µm near floating junctions results in good convergence stability and accurate solutions during subsequent potential update.

Figure 2.20 illustrates the dependence of the breakdown voltage on the spacing for a single guard ring for various ring´s width (for a 10µm thick, 9×10^{15}cm^{-3} doping level epilayer configuration).

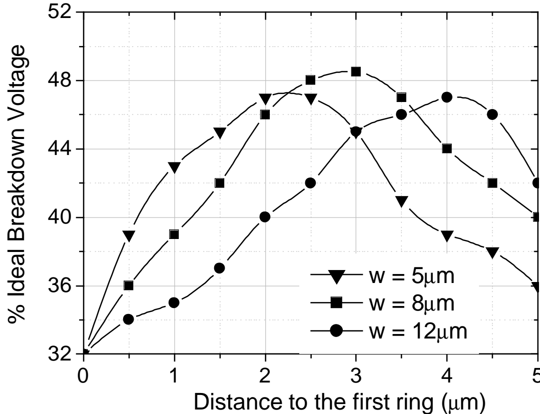


Figure 2.20 Simulated dependence in breakdown voltage as a function of the first guard ring spacing (*s*) for three different ring´s width (-▾- w=5μm, -■- w=8μm, -•- w=12μm).

It is obvious from this graph that the exact spacing of the guard rings can have a significant effect on the breakdown voltage. For a single ring, the optimum junction-to-ring spacing depends on the ring´s width, as the ring´s width increases the optimum distance also increases. It can be also seen that for w=8μm the breakdown voltage is slightly higher than for w=5μm or w=12μm. Moreover, due to possible photolithographic alignment error we decided to set the ring´s width equal to 8μm. In comparison with silicon, the breakdown voltage is much sensitive to ring space due to the reduction of epitaxial thickness and to the low junction depth (0.25μm) of the rings. An increase in S_1 shifts the peak field to the edge of the main junction, resulting in a lower breakdown voltage, but if S_1 is decreased, the peak electric field is maintained at the ring edge, but the electric field shielding of the main junction is diminished and the breakdown voltage is lowered.

We have also analysed the dependence of optimum single ring spacing on the epilayer doping level. As it can be observed in Fig. 2.21, the optimum distance from the main junction to the first ring is increased when the epilayer concentration decreases (for a fixed ring´s width of 8μm). The optimum distance increases from 3μm for a $9\times10^{15}cm^{-3}$ doped layer to 5μm for a $5\times10^{14}cm^{-3}$ doping layer concentration.

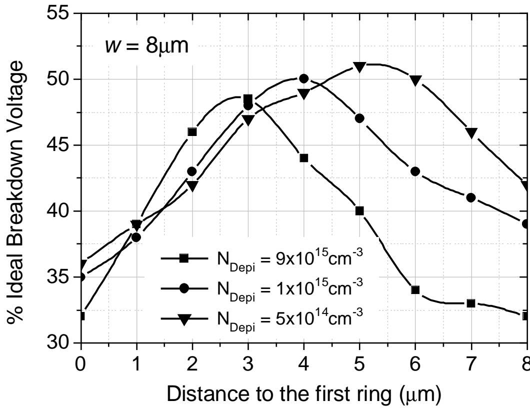


Figure 2.21 Simulated variation in breakdown voltage as a function of the first guard ring spacing (*s*) for three different epilayer concentrations (-■- $N_D=9\times10^{15}cm^{-3}$, -•- $N_D=1\times10^{15}cm^{-3}$, -▾- $N_D=5\times10^{14}cm^{-3}$).

The next step is to increase the number of guard rings to improve the termination efficiency. We decided to keep the same distance between rings (s=3μm) and the same ring´s width (w=8μm) for all of them. With this configuration it is observed a gradual increase in the breakdown voltage as the number of rings is increased, reaching a saturation value for 5 rings, as it is shown in Figure 2.22 (epilayer thickness is 10μm, doped $9\times10^{15}cm^{-3}$).

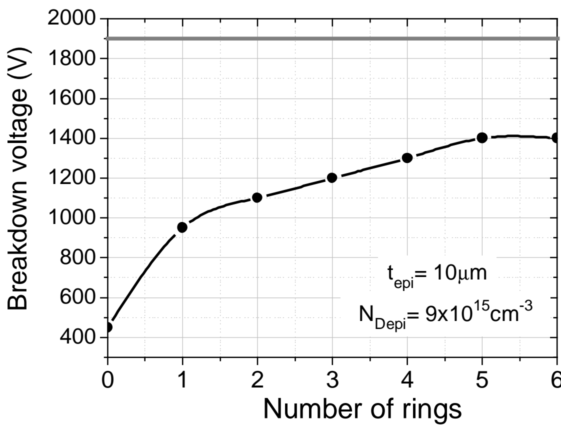


Figure 2.22 Variation of breakdown voltage with the consecutive addition of guard rings, w=8μm, s=3μm.

As we can see, the breakdown voltage increases from 950V for a single ring up to 1400V with five guard rings. This last breakdown voltage represents around 75% of the ideal breakdown voltage value. Thus, it is concluded that multiple guard rings is a less effective edge termination technique than single or double JTE structures (which are able to reach near 95% of the ideal breakdown), as it was already observed in other works [104-106].

2.3.4 "Floating Guard Rings assisted JTE" novel structure design

Floating guard rings (FGR) suffer from surface instabilities because electric fields on the surface are very high and surface charges can cause variation of the surface potential and create conductive surface channels on the low doped layer between the rings. To make FGRs less sensitive to surface charge and, at the same time, extend the JTE range of impurity concentration for obtaining high breakdown voltages we have developed a novel "guard rings assisted JTE" structure shown in Fig. 2.23. It is also an attractive structure because the guard rings are formed simultaneously with the main junction, thus reducing processing steps.

The implemented inner guard rings follow the optimised configuration shown in previous section (five equally spaced rings, *s*=3μm, of 8μm width). The main geometrical parameter to be optimised in this termination is the distance (*d*) between the last guard ring and the JTE edge. The optimised distance shows the electric field equally shared between the last ring and the end of the JTE region for the optimal dose, which from numerical simulations results is

d=35μm, as seen in Fig. 2.24. In this case, the range of the impurity doses yielding the highest breakdown voltage becomes extended toward the lower impurity JTE doses because of the P^+ inner FGRs´ effect, as it can be seen in Fig. 2.25. We also observe a reduction of the electric field at breakdown in comparison with the single JTE structure.

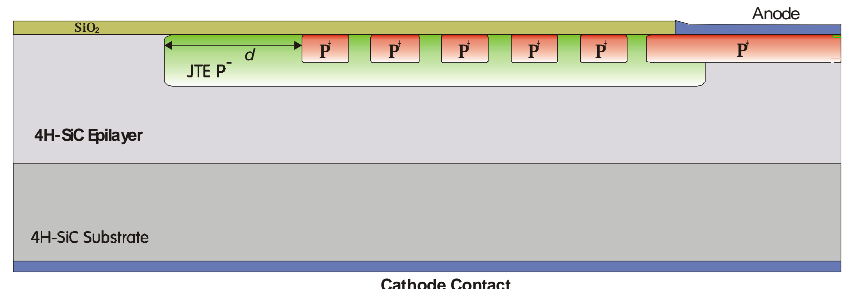


Figure 2.23 Schematic cross-section of the "FGRs assisted JTE" structure.

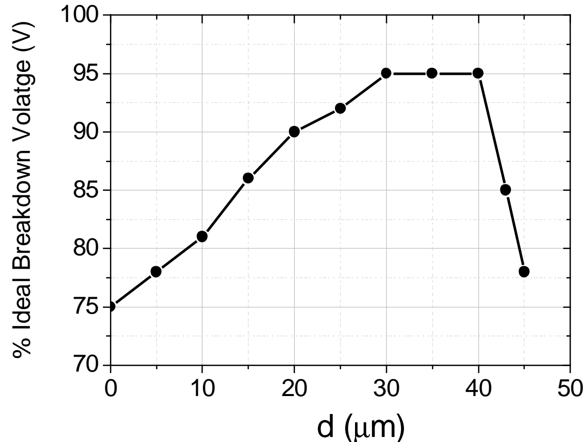


Figure 2.24 Breakdown voltage *vs* distance from the last ring to the end of the JTE zone for 5 equally spaced rings (*s*=3μm), of 8μm width.

Several technological effects such as an incomplete activation of Al dopant (substitutional), exodiffusion, non uniform doping and thickness of the epilayer and dose variation make the JTE effective dose lower than the ideal implanted one, thus reducing the breakdown voltage. Nevertheless, the inner guard rings of the JTE in the novel structure reduce greatly this effect and make the termination efficiency (i.e., breakdown voltage) less sensible to implantation dose variations, as it can be observed in Figure 2.25.

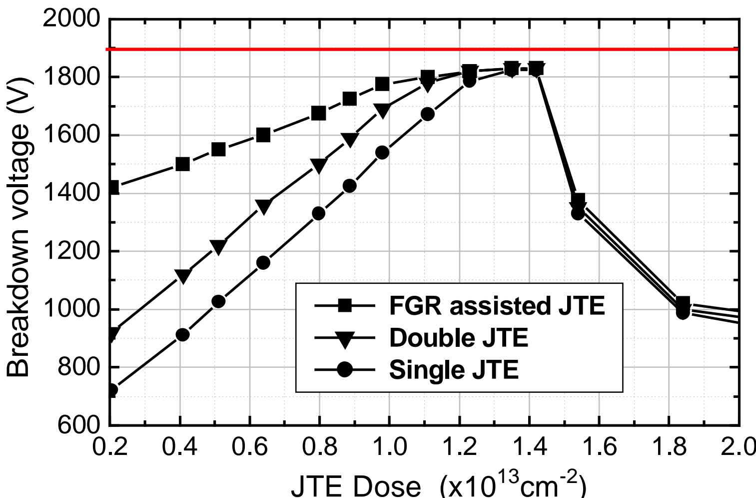


Figure 2.25 Simulated breakdown voltage *vs.* dose for the *FGRs assisted JTE* structure (-■-) in comparison to that for single JTE (-●-) and double zone JTE (-▼-) structures.

As an illustration of the effect of P^+ inner rings on the mechanism of sustaining high breakdown voltages, Fig. 2.26 shows the impact ionization distribution of the “FGRs assisted JTE structure” at the breakdown, where impurity concentration of the JTE layer is higher, equal and lower than the optimum charge.

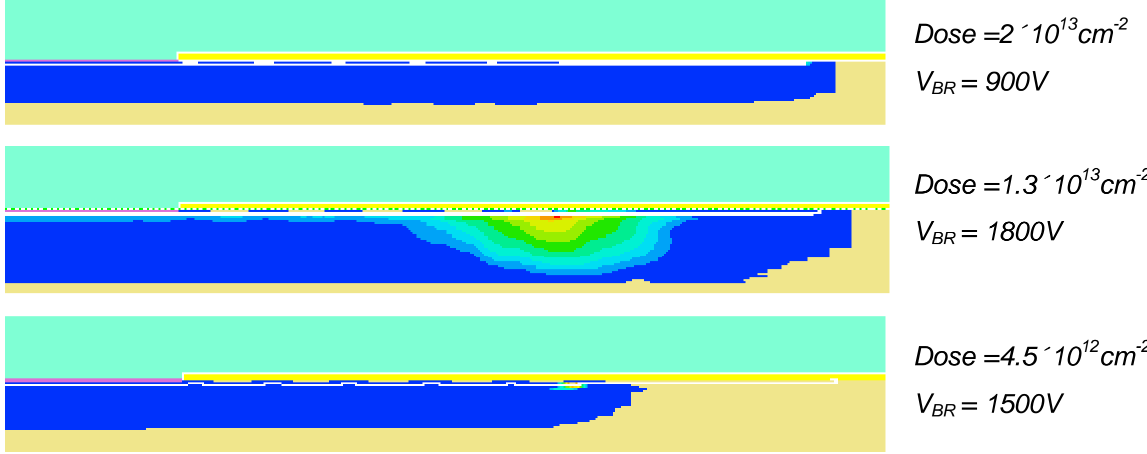


Figure 2.26 Impact ionization distributions of the “FGRs assisted JTE” structure showing the inner ring´s effect on assisting the JTE layer for impurity concentration lower than the ideal one.

2.3.5 Surface charge sensitivity

An additional termination design issue in SiC is the potential sensitivity of the optimised structure to surface charge. As in Si device technology, surface charges resulting from processing conditions or operating stress can significantly alter planar junction breakdown values by either enhancing or restricting depletion layer spreading. The surface charge effects are enhanced due to planar junction formation in SiC, where the implantation and subsequent anneals can often leave the surface damaged or morphologically altered. Interface charge over these areas has been shown to be greatly enhanced, with both positive and negative effective charges polarities possible depending on passivation growth conditions [107-109].

Since the JTE structure relies on precise control of implanted charge, additional charge on the surface of the device will alter the intended potential distribution in the JTE. To analyse the influence of interface charges on termination efficiency, simulations were performed with different fixed oxide (SiO_2)/SiC interface charges. The effect of both positive and negative oxide/SiC interface surface charge on the effectiveness of the different JTE structures analysed in previous sections is shown in Fig. 2.27.

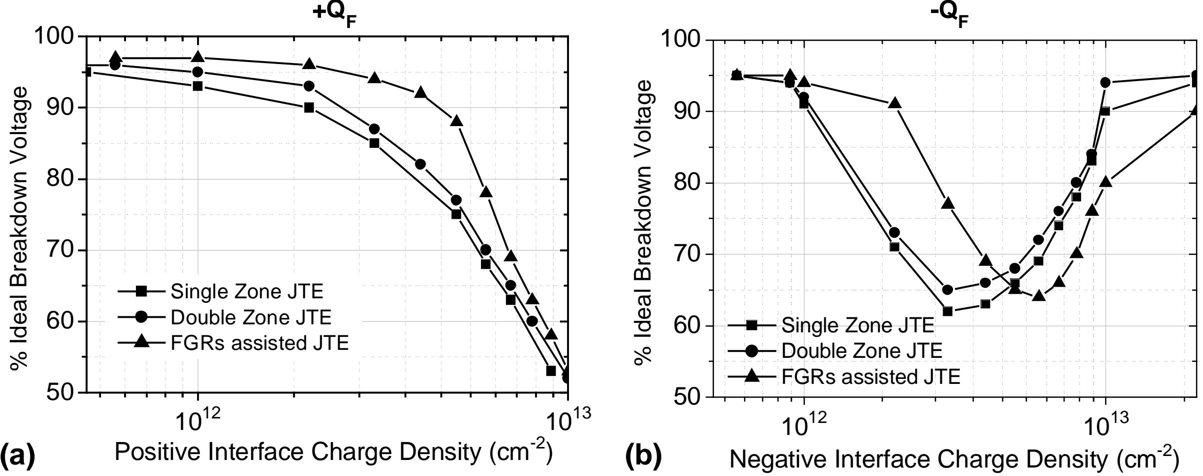


Figure 2.27 Effect of oxide/SiC interface charges on the breakdown of planar JTE structures developed. (a) Effect of positive charges, (b) Effect of negative charges.

These simulations show that either polarity of surface charge does not have a significant effect on the efficiency of the different JTE structures until the surface charge density exceeds approximately 1×10^{12}cm^{-2}. For a positive surface charge, the breakdown voltage of the device rapidly decreases above 2×10^{12}cm^{-2} because the surface charge effectively pins the depletion region at the edge of the JTE.

An increase in the negative surface charge will decrease the JTE effectiveness until the surface charge becomes comparable to the amount of charge in the depletion layer under the

surface of the device. This depletion layer spreading results in reduced field crowding at the JTE edge and thus higher breakdown voltage.

An improvement in the quality of the SiO_2/SiC interface has been achieved in the past recent years. Effective fixed oxide charge densities (Q_F) well below $2\times10^{12}cm^{-2}$ have been recently reported for both dry and wet oxidation in oxides grown on either n- or p-type 4H-SiC [108-112], achieving . In general, Q_F is found to be either positive or negative, depending not only on whether oxidation has been performed in wet or dry oxygen, but also on the annealing conditions.

Our thermal oxidation process consists in growing a dry oxide followed with a wet re-oxidation anneal which has been proved to produce an oxide with the dielectric strength of a dry oxide and the high-quality interface of a wet oxide, with reported fixed oxide charges densities below $1\times10^{12}cm^{-2}$ [112]. Thus, it is expected that the blocking efficiency of the developed edge termination structures should not be altered by the presence of fixed charges at the SiO_2/SiC interface.

2.4 Photolithographic Mask Layout Design

Unlike other common wide-bandgap semiconductors, such as the III-nitrides compounds, silicon carbide is compatible with established silicon process technology. Standard processes and equipment can be used without the risk of contamination.

In this section, a brief description of the 4H-SiC prototype diode layouts and the associated test structures, such as TLM (Transmission Line Model) structures and areas for SIMS measurements, is given. The mask layout has been designed using the CADENCE environment. An alignment error of 2 µm and a minimum feature size of 15 µm have been assumed. The complete mask layout is shown in Fig. 2.28 and the implemented devices and structures are identified in the floorplan of the layout given in Fig. 2.29. The structures were transferred by standard photolithography in a manual mask aligner from chromium plated glass reticles onto the resist covered samples. Positive photoresist was used.

The mask set consists of 6 levels as follows:

1. *Plasma etch of alignment marks*. This step must be done first, because the high temperature activation annealing does not permit the use of conventional reference patterns, required for the alignment of the following masks. However, this also enables changing the mask sequence for the manufacture of different processes.

2. *P^+ implant mask.* A 2µm thick, deposited silicon dioxide layer is etched with this pattern and serves as a mask for the ion implantation of anodes and multiple guard ring edge termination.

3. *P implant mask*. The patterned silicon dioxide layer etched with this pattern serves as a mask for the ion implantation of regions with medium doping level concentration, 2×10^{18}cm^{-3} (first JTE in double JTE structures, JBS grid, a FGRs edge termination).

4. *P^- implant mask*. An oxide/aluminum multilayer mask is etched with this pattern and acts as a mask for the high energy ion implantation to form the low-doped regions (single JTE, second JTE in double JTE structures, JBS grid, a FGRs edge termination).

5. *Contact windows*. A 2 µm thick oxide layer is deposited and serves as device isolation and surface passivation. Contact holes are etched into this layer to access the underlying SiC structures.

6. *Metal.* The same metal layer is used for both ohmic and Schottky contacts.

Figure 2.30 shows the 6 mask layers designed for the fabrication of the devices. Each mask layer contains alignment marks to allow accurate positioning of subsequent process steps.

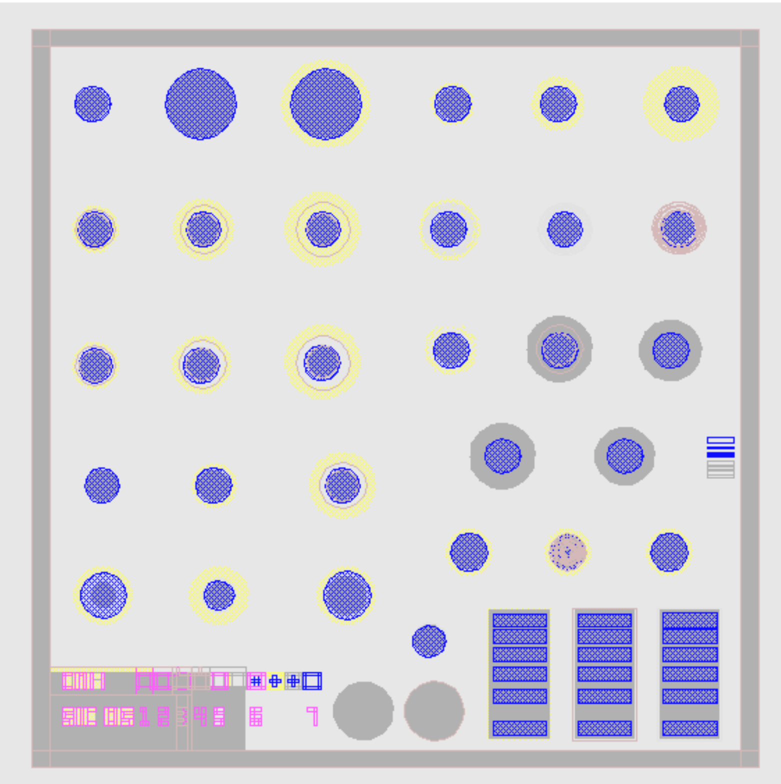


Figure 2.28 Schematic diagram of the mask layout.

Basic PiN diodes

200µm 400µm 400µm+ JTE 60 µm

Single JTE PiN diodes

JTE 30µm JTE 60 µm JTE 120µm

2 zone JTE embedded diodes

20-40µm 40-80µm 60-120µm

Multiple Guard Ring diodes

FGRP+ + JTEP- FGRP+ FGRP

2 zone JTE side-by-side diodes

20-20µm 40-40µm 60-60µm

FGR P-

Unpassivated diodes

2JTE super. 1JTE 60µm

FGRP+ + JTEP- FGRP+

Schottky diodes

Unterm. 1JTE P- 40µm 2JTE 40-80µm

JBS diodes

JBSP+ JBSP JBSP-

Diodes with Field Plate

FP over P- region Short FP Extended anode over P- region

Test diode

TLM structures

P- P P+

Alignement marks

SIC 05

SIMS

P- P

Figure 2.29 Floorplan of the mask layout.

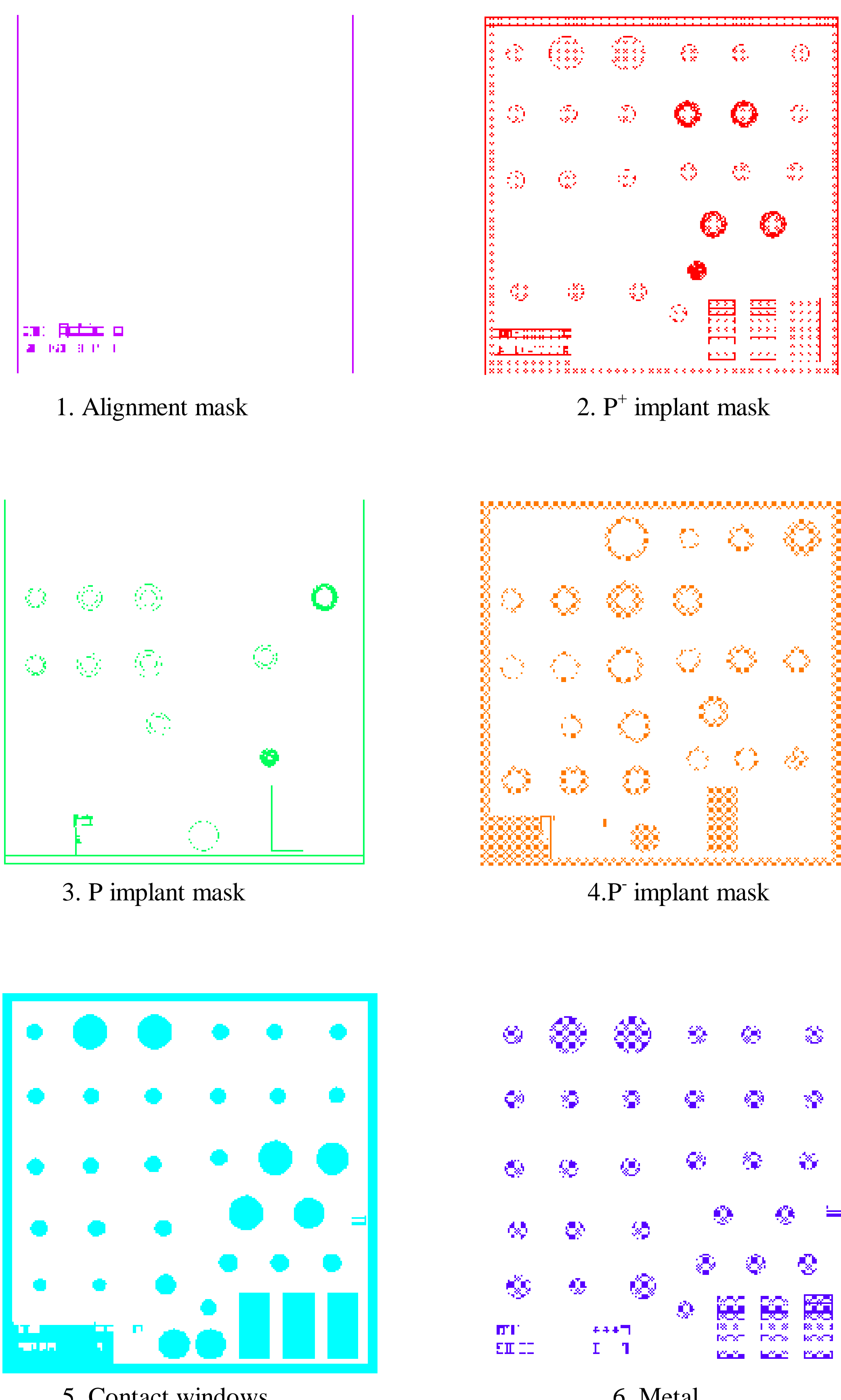


Figure 2.30 Layout of the different mask levels.

2.4.1 Implemented devices and test structures

The main purpose of the diodes is to analyse the efficiency of the different edge terminations optimised by simulation, focusing mainly on the single and double zone JTE technique. Therefore, they are designed with varying JTE lengths (30, 60 and 120 µm) in both single and double zone configurations (see Fig. 2.29). We have also designed a five floating guard rings edge termination which we have implemented in the mask set with the three different doping concentrations that will be carried out (P^+, P and P^-). The novel developed "guard rings assisted JTE" termination has also been implemented in one PiN diode.

Schottky and JBS diodes have been also designed in the mask set. Three Schottky diodes with different edge termination (unterminated, single JTE of 40 µm length, and double zone side-by-side JTE of 60 µm zone length) were implemented to analyse the unipolar behaviour of SiC devices and the different metal-SiC Schottky barrier heights. JBS diodes terminated by single JTE of 40 µm length were designed with concentric p-type doped rings (6 µm wide, 6µm spaced) in the emitter region, leading to a 50% of total Schottky area. The three different doping levels were implemented in the emitter regions of three different JBS diodes to evaluate the influence of the implanted *p*-type concentration on the current-voltage characteristics of this kind of devices.

All diodes have circular geometry with an emitter diameter of 200 µm, except two specific diodes designed with a diameter of 400 µm to evaluate the impact of the device area on current-voltage characteristics. Table 2.5 summarises the different diode designs implemented in the mask set for fabrication.

Transmission Line Model (TLM) test structures have also been implemented in the mask set to evaluate the substitutional activation rate of the three different implantation profiles after the high temperature treatment process. This test structure also allows the extraction of the contact resistivity value of the deposited metal, which is of special interest for the characterisation of the ohmic contact characteristics of the metal-semiconductor junction on our PiN diodes. The dimensions of this test structure are shown in Fig. 2.31.

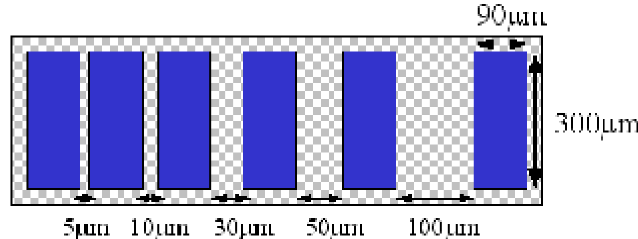


Figure 2.31 Schematic view with the corresponding dimensions of the implemented TLM structure.

To open the possibility to make a SIMS (Secondary Ion Mass Spectroscopy) analysis on the two implanted profiles corresponding to the two JTE zones (P and P^-) we have designed

two implanted circular areas of 500 μm of diameter at the bottom of the mask. The SIMS analysis is of special interest in the case where boron is used as the implanted impurity because its profiles are modified in a great manner after the high temperature activation anneal [113].

Table 2.5 Summary of the diode designs implemented in the fabrication mask set.

ID. Nº	Type	Diameter (㎜)	Edge Termination	Special Features	Research objective
1	PN	200	Unterminated		Analysis of the device area on I-V characteristics.
2	PN	400	Unterminated		
3	PN	400	Single JTE L=65μm		
4	PN	200	Single JTE L=35μm		Analysis of the JTE length optimisation.
5	PN	200	Single JTE L=65μm		
6	PN	200	Single JTE L=125μm		
7	PN	200	Double JTE L_1=25μm, L_2=45μm	Double JTE in embedded configuration	Analysis of the JTE length optimisation and zone configuration in the double JTE structure.
8	PN	200	Double JTE L_1=45μm, L_2=85μm		
9	PN	200	Double JTE L_1=65μm, L_2=125μm		
10	PN	200	GR(p$^+$) +JTE L=90μm		Analysis of the p-type concentration influence on GR termination efficency.
11	PN	200	GR p$^+$		
12	PN	200	GR p		
13	PN	200	GR p$^-$		
14	PN	200	Double JTE L_1=25μm, L_2=25μm	Double JTE in side-by-side configuration	Analysis of the JTE length optimisation and zone configuration in the double JTE structure.
15	PN	200	Double JTE L_1=45μm, L_2=45μm		
16	PN	200	Double JTE L_1=65μm, L_2=65μm		
17	PN	200	Double JTE embedded L_1=45μm, L_2=85μm	Unpassivated devices	Analysis of the passivation layer influence on different edge terminations.
18	PN	200	Single JTE L=60μm		
19	PN	200	GR(p$^+$) +JTE L=90μm		
20	PN	200	GR (p$^+$)		
21	Schottky	200	Unterminated		Analysis of the Schottky characteristics with different metal and RTA processes.
22	Schottky	200	Single JTE L=40μm		
23	Schottky	200	Double JTE side-by-side L_1=45μm, L_2=65μm		
24	PN	260	Single JTE L=80μm	55μm field plate	Analysis of the field plate effect on different metal-termination configuration.
25	PN	180	Single JTE L=80μm	10μm field plate over p$^+$	
26	PN	260	Single JTE L=80μm	20μm field plate over JTE	
27	JBS	200	Single JTE L=40μm	P$^+$ grid doping	Analysis of the different p-type grid concentrations on I-V characteristics.
28	JBS	200	Single JTE L=40μm	P grid doping	
29	JBS	200	Single JTE L=40μm	P$^-$ grid doping	

2.5 Summary

In this chapter, the main important electrical models together with the corresponding material parameter set for 4H-SiC device simulation in MEDICI 2D-simulation program have been compiled from literature data. The associated parameters of the most important models for bipolar devices simulation described in this chapter, are given in Appendix B.

Using calibrated numerical simulations, edge termination structures for planar SiC power devices have been investigated. The single zone JTE has been proved to yield high ideal breakdown values (95% of the ideal plane-parallel breakdown voltage) with only moderate constraints on the precise dopant activation. A moderate surface depletion of the JTE doping implantation profile has shown to be effective in the reduction of the surface electric field at breakdown without degradation in blocking capabilities. Double zone JTE structures have been also considered to allow further control of peak electric fields without compromising the breakdown voltage and have shown to wide the optimum impurity dose range for lightly doped JTE zone where high breakdown voltages are achieved. Multiple floating guard rings (FGR) termination structure has also been optimised for 4H-SiC diodes demonstrating less blocking efficiency than single or double zone JTE structures. Furthermore, we have developed a novel edge termination structure namely "Floating Guard Rings assisted JTE" which has proved to be a robust termination providing high breakdown voltages with less sensitivity to technological parameters. With this novel termination the range of the impurity doses for obtaining high breakdown voltages is extended toward the lower impurity dose of the JTE layer by the inner FGRs effect. All these JTE structures maintain excellent efficiency with additional surface charge densities approaching $2\times10^{12}cm^{-2}$ for either positive or negative polarities.

Finally, the photolithographic mask set layout designed for the fabrication of diodes has been presented together with a detailed description of the design of implemented devices and test structures.

CHAPTER 3

Device Fabrication and Characterisation

This chapter will describe the device fabrication procedure, and show the details of the different processes carried out. The different starting material used in the scope of this thesis is presented first together with the samples classification. Thereafter, the different implantation and activation anneal procedures are presented in detail for each sample together with the activation rate results. The main part of the chapter will cover the electrical characterisation of the different metal-semiconductor junctions formed. A detailed analysis of different investigated contact systems for both Schottky and ohmic purposes will be carried out.

3.1 Device Fabrication Process

3.1.1 Starting Material

During this thesis, high power diodes have been fabricated on three different 4H-SiC wafers purchased from two different suppliers, Table 3.1 summarises the material characteristics of each wafer.

Table 3.1 Characteristics of the three main epitaxial wafers used during this thesis.

			Substrate		***Epilayer***	
Supplier	**Wafer nº**	**Diameter**	**Resistivity**	**Thickness**	**Doping**	**Thickness**
CREE	AD-0602-02	2”	0.017 Ωcm	350 μm	9.5×10^{15} cm^{-3}	10 μm
CREE	XU-0884-01	2”	0.021 Ωcm	421 μm	2.0×10^{15}cm^{-3}	20 μm
Sterling	B-8141-13	1.37”	0.050 Ωcm	300 μm	2.5×10^{15}cm^{-3}	15 μm

Other materials have been used for test on ohmic and Schottky contact formation.

All three wafers are *n*-type (both substrate and epilayer) *Si*-face polished with an orientation of 8º towards $\langle 11\bar{2}0\rangle$. CREE wafers are high quality production grade with a specified micropipe density of 31-100 micropipes/cm^2, while Sterling specifies a micropipe

density of <200 micropipes/cm^2. Furthermore, as it can be seen from images in Fig. 3.1, Sterling´s wafer suffers from a great number of macroscopic surface defects appearing as great holes.

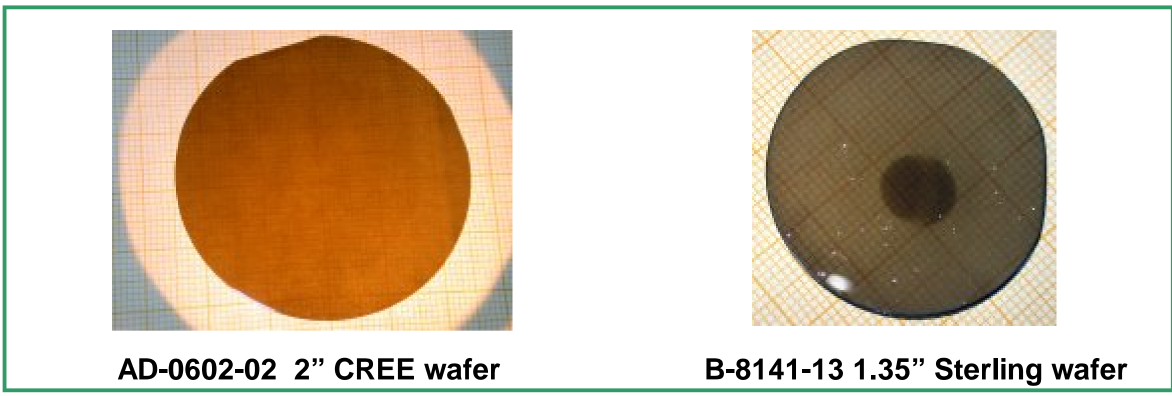


Figure 3.1 Photographic images of 4H-SiC wafers used for the fabrication of diodes during this thesis.

The two CREE wafers were cutted into quarters to be able to apply different fabrication procedures on each one, and thus widen the analysis of the influence of different technological processes on final device performance. Sterling´s wafer was accidentally broken and divided into two main parts. Table 3.2 summarises the name of the processed samples that will be referenced hereafter. Appendix C resumes the different processes performed on each sample.

Table 3.2 Reference names of the samples processed during this thesis.

CREE wafers								*Sterling wafer*	
AD-0602-02				XU-0884-01				B-8141-13	
CQ1	CQ2	CQ3	CQ4	CB1	CB2	CB3	CB4	S1	S2

The as-received wafers were initially cleaned with a conventional procedure based on Acetone, Isopropanol, and RCA cleaning prior to the first process step.

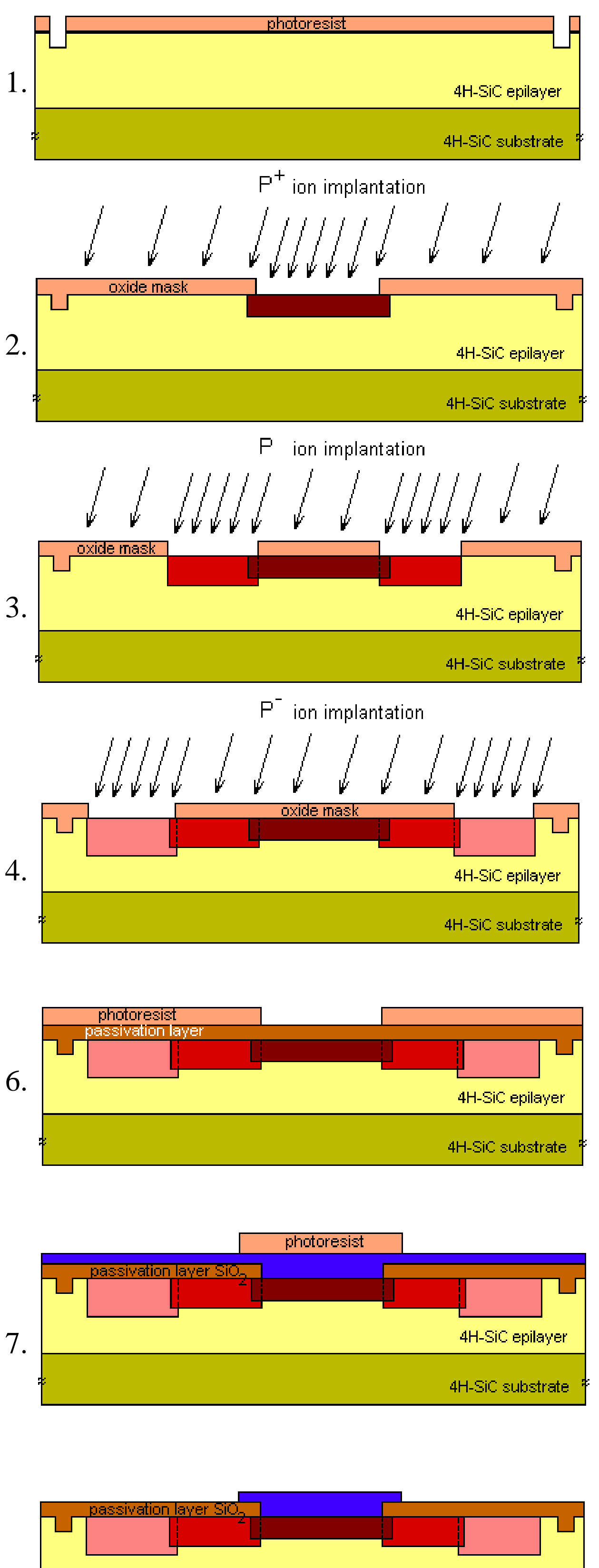
3.1.2 Fabrication Process Steps

The schematic diagram placed in next page shows the different process steps carried out for the fabrication of diodes designed on the photolithographic mask set shown in Chapter 2 section 2.4, together with a descriptive figure of each process. A diode with double JTE termination structure in a side-by-side configuration has been chosen as an example for the general fabrication process description.

Process Step

1. Alignment marks etching (first photolitographic step)
2. • Deposition of oxide mask and second photolitographic step
   • P^+ implantation (Al^+ or B^+ ions)
3. • Deposition of oxide mask and third photolitographic step
   • P implantation (Al^+ or B^+ ions)
4. • Deposition of oxide mask and fourth photolitographic step
   • P^- implantation (Al^+ or B^+ ions)
5. High temperature activation annealing (1650ºC-1700ºC)
6. • Deposition of passivation layer (SiO_2)
   • Contact opening (fifth photolitographic step)
7. • Deposition of Ti and Ni by sputtering
   • Patterning of contact metal by wet etching of Ni/Ti bilayer (sixth photolitographic step)
8. • Backside metalisation
   • Metal annealing (RTA)
9. • Deposition of thick Au layer
   • Patterning of contact metal by wet etching of Au metal layer (seventh photolitographic step)

Illustrative picture



3.2 Ion Implantation for Selective Doping

Since the diffusivities and impurity incorporation rate in silicon carbide surface are extremely low, doping by gas phase diffusion as used in silicon technology is not viable in the case of SiC. In order to create lateral structures with different doping levels, ion implantation of the dopant species is therefore commonly used. This somewhat restricts the depth that most dopants can be implanted to less than 1 µm using conventional dopants and implantation equipment. With the precise control over the energies and doses of the implanted species, it is possible to tailor the implanted doping profile to the needs of the device design. Since ion implantation is the most promising technology for selective doping of SiC, research on this topic is conducted worldwide.

A major problem with the use of ion implantation in SiC technology is the need for a high temperature post-implantation anneal at temperatures of 1500ºC-1900ºC to heal the implantation damage and to electrically activate the implanted species [114]. Implantation at elevated temperatures in the range of several hundred centigrades has been used to improve the activation rate and reduce the amount of crystal damage [115]. The elevated-temperature during implantation promotes some lattice self-healing during the implant, so that damage and segregation of displaced silicon and carbon atoms does not become excessive, especially in high-dose implants often employed for ohmic contact formation. Co-implantation of carbon or silicon with *p*-type dopants has recently been investigated as a means to improve the electrical conductivity of implanted *p*-type contact layers [116,117].

For the selective doping process of our diodes we precise to define a multiple energy implantation with a box-shaped doping profile, from which we need to know the uniform doping level and depth. All implantations carried out during this thesis were previously designed by a specific SiC implantation simulator (I^2SiC) developed at CNM [99]. This software is based on Montecarlo code, developed in the binary collision approximation, and it takes into account the hexagonal crystalline structure of SiC.

As it was explained in chapter one, aluminum (Al) and boron (B) are the two species commonly used to create *p*-type regions in SiC devices. To analyse the suitability of this two different dopants to create selective *p*-type regions in SiC devices, we have fabricated two different batches of diodes.

3.2.1 Aluminum implantations

Efficient *p*-type doping requires acceptor atoms which have a natural tendency to substitute the *Si* atoms in the SiC compound. Fortunately, *Al* fulfils this requirement in a nearly ideal manner, because in contrast to *B,* only replacement of *Si* by *Al* is energetically favourable as demonstrated by tight-binding calculations [118]. Two additional advantages of the *Al* acceptor are connected with its physical similarity to *Si*. The similar atomic size

prevents large lattice distortions which could act as scattering centers or even traps for the holes. Moreover, the almost equal masses facilitate the direct replacement of *Si* by *Al* in atomic collisions during ion implantation doping.

All *p*-type regions of samples from wafers AD-0602-02 and B-8141-13 were formed by multiple energy aluminum implantations performed at high temperature (300ºC or 400ºC). Three different doping profiles were implanted to form the emitter and edge termination regions. Figure 3.2 shows the simulated doping profiles designed to create the P^+ regions ($2\times10^{19}cm^{-3}$ doping level) and the *P* doping level regions ($2\times10^{18}cm^{-3}$ doping level).

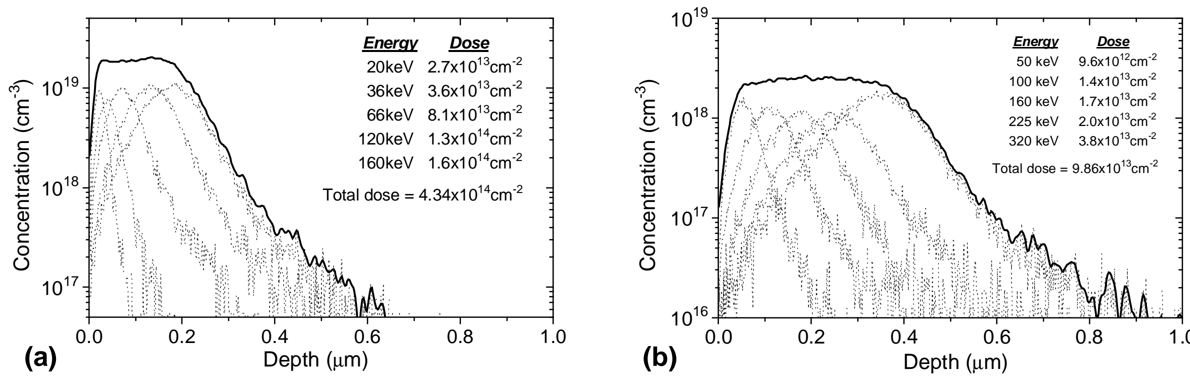


Figure 3.2 I^2SiC simulated Al^+ implantation doping profiles to create the P^+ regions (a) and the P doping level regions (b).

The P^+ implantation mainly creates the emitter region, the guard rings and the JBS P^+ grid, and the *P* implantation is mainly designed for the formation of the first JTE zone in the double zone JTE termination. These two implantation processes were performed at 400ºC through an oxide mask layer by IBS (Ion Beam Services) in France.

For the P^- implantation needed for the second and single JTE zone, two different profiles were designed in order to analyse the influence of the doping depth on the breakdown capabilities. Figure 3.3 shows these two simulated doping profiles.

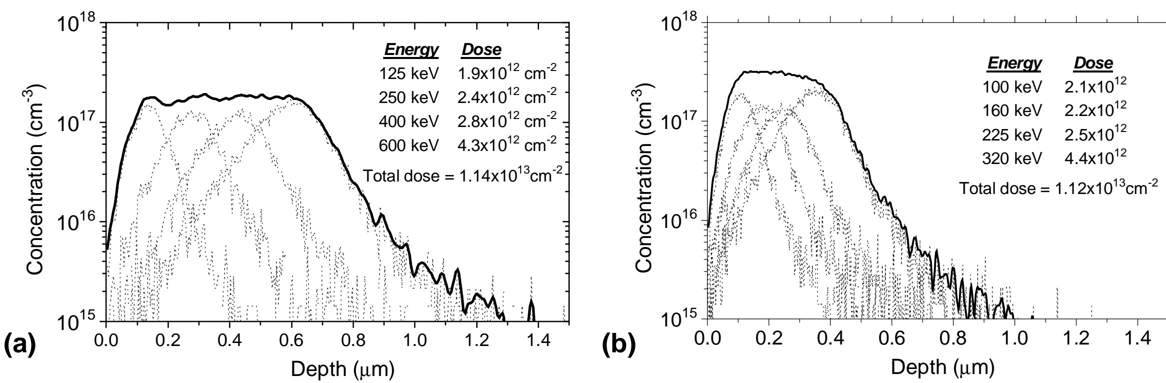
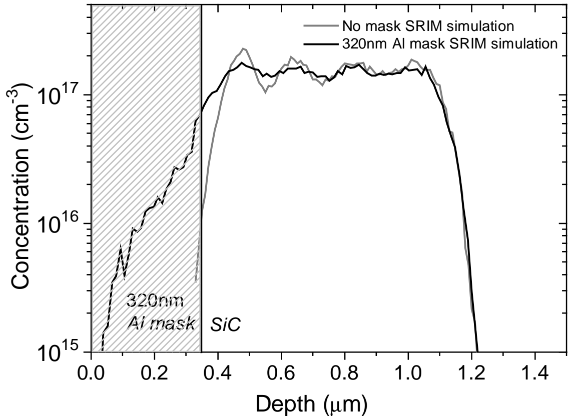


Figure 3.3 I^2SiC simulated Al^+ implantation doping profiles designed to create the P^- regions. (a) High-energy implantation with an estimated depth of 0.9μm; (b) Multiple energy implantation with an estimated depth of 0.6μm.

The high-energy multiple Al^+ implantation (Fig 3.3a) was carried out in samples CQ1, CQ2, CQ4, S1 and S2 at *Istituto LAMEL* (Bologna) at high temperature (300ºC) through an oxide/aluminum multilayer mask. The multiple energy implantation profile shown in Fig 3.3b was carried out at 400ºC at IBS in sample CQ3 through an oxide mask.

It must be pointed out here that due to the fact that the minimum implantation energy of the high-energy implantation equipment (1.7MV HV-Tandetron) is 300keV, the implantation energies of the profile shown in Fig 3.3a had to be shifted and recalibrated taking into account an optimal aluminum mask thickness (320nm). For this purpose we used the commercial implantation simulator SRIM^{TM} [119] which can simulate the implantation through multiple layers. Figure 3.4 shows the SRIM^{TM} simulation of the high energy implantation through the 320nm thick aluminum mask together with the new implantation feature.



Energy	***Dose***
300 keV	2.2×10^{12} cm^{-2}
425 keV	2.5×10^{12} cm^{-2}
600 keV	2.8×10^{12} cm^{-2}
850 keV	4.3×10^{12} cm^{-2}

Total dose = 1.18×10^{13} cm^{-2}

Figure 3.4 Modified P^- implantation doping profile taking into account the aluminum mask layer needed to perform the high-energy implantation. The table on the right side shows the energy and doses used to define the doping profile.

3.2.2 Boron implantations

Because boron is much lighter and smaller than aluminum, the projected range for boron is about a factor of 2 higher than the projected range for aluminum, when implanted with the same energy. To form implanted *p*-type SiC layers with a thickness of more than 1μm, energies of around 1MeV are needed in the case of aluminum and about 0.5MeV in the case of boron. Hence, if thick *p*-type layers are required, boron has an advantage over aluminum, because it can be implanted deeper with industrial accelerators available in semiconductor processing. In addition, boron causes less damage to the crystal due to its size and mass. But boron as a dopant has the disadvantages of forming an impurity level with a higher ionisation energy compared to aluminum and suffering from enhanced diffusion during post-implantation annealing [120,121].

Samples from wafer XU-0884-01 were implanted with B^+ to form both the P^+ doped regions and the P^- doped edge termination zones. The two simulated implantation profiles are shown in Fig. 3.5.

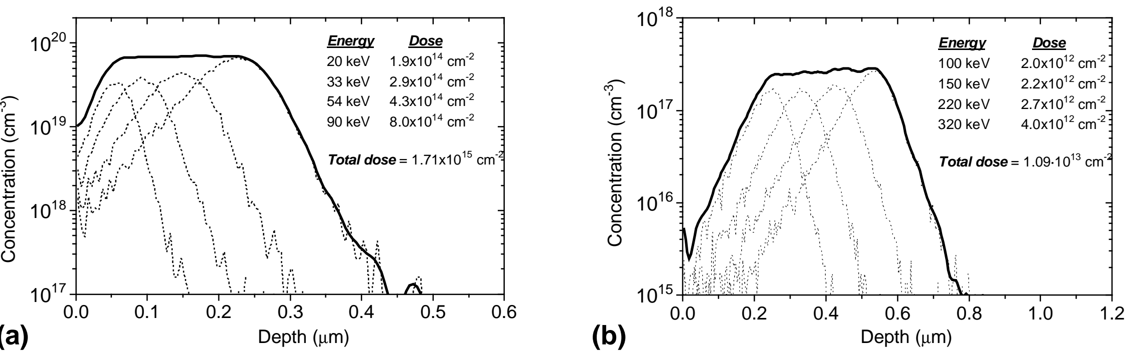


Figure 3.5 Simulated I^{2}SiC boron implanted doping profiles for the (a) P^+ and (b) P^- doped regions.

In order to analyse the influence of the total dose in single JTE on the blocking capabilities, three different total doses (but with the same implantation energy scheme of the profile in Fig. 3.5b) were implanted on different samples. Table 3.3 summarises the different doses implanted on samples from wafer XU-0884-01.

Table 3.3 Total boron implanted doses in JTE of samples from wafer XU-0884-01.

Sample	***CB1***	***CB2***	***CB3***	***CB4***
Implanted dose	$1.1´10^{13}\ cm^{-2}$	$1.65´10^{13}\ cm^{-2}$	$2.20´10^{13}\ cm^{-2}$	$1.1´10^{13}\ cm^{-2}$

All boron implantations were carried out at room temperature in the clean room of the CNM. A thick oxide film was used as a mask layer for all implantations.

Figure 3.6 shows the AFM images in 3D representation of the sample CB1 before (*as-received*) and after the boron implantation process. As it can be observed, the surface morphology is not altered by the implantation process and the sample shows a smooth surface with low roughness.

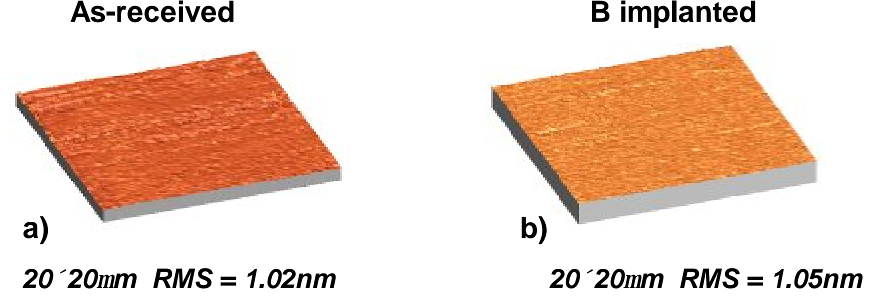


Figure 3.6 3D AFM images of the sample CB1 surface in the as-received stage (a) and after the boron implantation process (b). The size of the scans are 20x20μm.

3.3 High Temperature Activation Anneal

After implantation, the implanted dopants predominantly occupy interstitial lattice sites, where they are usually not electrically active. Therefore, a thermal annealing process is necessary to electrically activate the implanted dopants and to reduce the lattice damage. During the high temperature anneal, these implanted dopants compete with interstitial silicon and carbon atoms for empty lattice sites. The number of dopant atoms that manage to reside on a lattice place divided by the total number of introduced dopant atoms is called the degree of activation, which is a key figure for the quality of the doping process.

The final annealing conditions are crucial to obtain desired electrical properties from ion implanted layers. At higher implant anneal temperatures, the SiC surface morphology can seriously degrade as damage-assisted sublimation etching of the SiC surface begins to take place [122]. Because sublimation etching is driven primarily by loss of silicon from the crystal surface, annealing in silicon overpressures can be used to prevent surface degradation during high temperature anneals. Such overpressure can be achieved by close-proximity solid sources, such as using an enclosed SiC crucible with SiC lid and/or SiC powder near the wafer, or by annealing in a silane-containing atmosphere.

Thus both the surface roughness and carrier properties are necessary to be considered when optimising the post implantation annealing process. For this purpose we have investigated the surface morphology and electrical characteristics of 4H-SiC implanted samples and subsequently annealed under different conditions (as summarised in Table 3.4). In all the samples, the activation annealing of all implanted regions was carried out simultaneously in a J.I.P.ELEC™ rf-induction heating furnace at the centre of the susceptor. Before to reach a constant temperature plateau in the 1650-1700ºC interval, a preliminary heating rate of 40ºC/s was utilised. The decreasing of temperature at the end of the annealing is governed by thermal inertia. We have also changed the ambient gas for the annealing process to check its effect on the sample properties.

Table 3.4 Activation annealing features of the different samples processed during this thesis.

Sample	***Temperature***	***Time***	***Atmosphere***
CQ1	1700ºC	30min	Ar
CQ2, CQ3, CQ4	1650 ºC	45 min	N_2
S1	1700ºC	30min	Ar
S2	1650 ºC	30min	N_2
CB1	1650 ºC	45min	Ar
CB2, CB3, CB4	1650 ºC	45min	N_2

3.3.1 Surface morphology

As mentioned above, due to the very high annealing temperature, the surface morphology after electrical activation annealing becomes very rough, which is undesirable for the fabrication of electronic devices based on SiC. Selective preferential evaporation of Si atoms from the SiC surface during annealing causes local formations of C-rich phases and serious surface morphology roughening as the SiC substrates are placed on a heating holder or in a crucible for a long time [115, 122].

The surface morphology of the samples was characterised using the AFM (Atomic Force Microscopy) equipment from *Molecular Imaging* at ICMAB. The scanning size of the samples was performed in tapping mode and two scan sizes were acquired (20x20µm and 5x5µm).

Table 3.5 shows the acquired images from the analysed samples after high temperature activation anneal. To quantitatively evaluate the surface roughness we have calculated the statistical value RMS (Root Mean Square) of the image. This parameter is conventionally employed in engineering as a measure of surface roughness. This roughness calculation is based on finding a median surface level for the image and then evaluating the standard deviation within the image. The equation for determining the surface roughness is [123]:

$$R_q = \sqrt{\frac{1}{N^2}\sum_{i=1}^{N}\sum_{j=1}^{N}\left(z(i,j)-\overline{Z}\right)^2} \tag{3.1}$$

where i and j are the pixel locations on the AFM image, $\overline{Z}$ is the average value of the height across the entire image, and N is the number of data points in the image (AFM images are typically stored as 256×256 or 512×512 data arrays).

As it can be observed from images in Table 3.5, the surface morphology is mainly affected by the appearance of grooves. The depth and width of the grooves on the SiC surface increases with increasing annealing temperature resulting in grooves of ~25nm depth and ~600nm width for 1650ºC 45min annealing in Ar. According to Capano et. al. [122], groove formation is possibly due to sublimation and redeposition of Si species Si, Si_2C, and SiC_2 on the off-cut crystal surfaces. As the species redeposit they assume an equilibrium crystal layer shape that results in long, repeating furrows. The crystal geometry can be pictured as like a set of books, where each book corresponds to a crystal layer, tipped sideways on a shelf , with the wafer surface analogous to the uneven tops of the books. The offset of the parallelepiped crystal layers results in a V-shaped groove where the end of one layer sits back from the end crystal faces. Hence, as higher-temperature and longer-duration annealing permits greater atomic migration, more atoms on the SiC crystal edges will migrate into the faces of neighbouring crystal layers, enlarging some crystal layers and eliminating others. The initial smooth surface of the unannealed SiC samples (Fig 3.6a) is a result of both thin crystal layers

Table 3.5 AFM images of samples after high temperature activation anneal.

Sample	***Scan size 20x20mm***	***Scan size 5x5mm***
S1 Al implanted 1700ºC, 30min, Ar	**RMS =10.2 nm**	**RMS =10.9 nm**
S2 Al implanted 1650ºC, 30min, N_2	**RMS = 6.1 nm**	**RMS = 5.4nm**
CB1 B implanted 1650ºC, 45min, Ar	**RMS = 12.5nm**	**RMS = 13.7 nm**
CB2 B implanted 1650ºC, 45min, N_2	**RMS = 4.5nm**	**RMS = 5.2nm**

and polishing. Consolidation into larger crystal layers during annealing results in a widening and deepening of the surface grooves. The surface roughness increases somewhat with increasing anneal temperature. Annealing time plays a secondary role in the macrostep formation, but not negligible. We have seen that in N_2 atmosphere at 1650ºC, a 10min annealing has a higher roughness than 30 min ones.

Comparison of the annealed SiC surfaces under N_2 atmosphere with those annealed under Ar atmosphere reveals several differences in terms of surface morphology. Nitrogen does not favour the appearance of a step bunched morphology and show less surface roughness for temperatures up to 1650ºC. The explanation of this macrostep reduction is correlated to the Si/C ratio in the gas phase. The use of N_2 instead of Ar increases both Si and C solubilities in the gas phase by forming gaseous nitride species. These nitrides, mainly C_2N_2, CN and SiN, are even in higher amount than the carbonated sublimation species CSi_2 or C_2Si. An important parameter for surface stabilization of SiC is the relative amount of both Si and C species. Younes et al. [124] showed that the step bunching morphology is mainly produced by the nature of the gaseous species above the SiC surface: C-rich ambiance does not affect the surface strongly whereas Si-rich modify the surface structure and enhance the formation of big steps. The use of N_2 as gas atmosphere during high temperature anneal produces C-rich ambiance for temperatures up to 1650ºC. On the other hand, when Ar is used, the gas phase is always largely Si-rich.

However, for temperatures higher than 1650ºC, annealing in N_2 promotes the apparition of carbon clusters on the sample surface (see Figure 3.7a). This limits the temperature range of use of N_2 as ambient gas in SiC annealing.

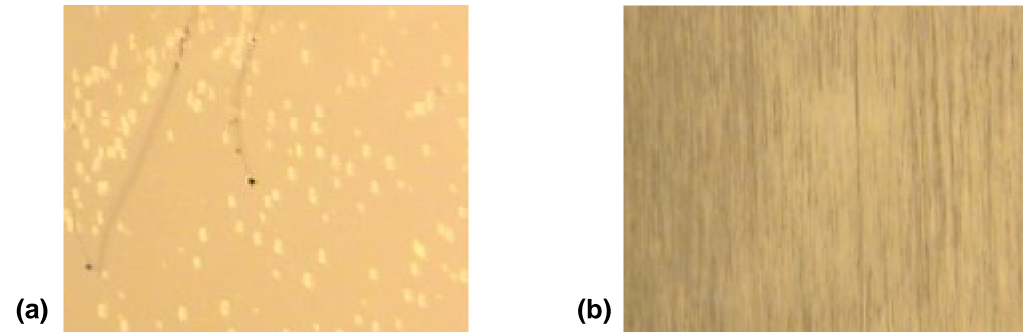


Figure 3.7 Optical pictures of (a) sample annealed at 1700ºC in N_2, the bright spots are identified as carbon clusters, (b) sample annealed at 1700ºC in Ar, for comparison.

The samples previously shown are implanted at high temperature. In figures 3.8a and 3.8b, we can see an optical microscopic pictures of a sample implanted P^+ at room temperature and annealed at 1650ºC in N_2. We can observed a clear surface degradation, making the sample unusable for device fabrication. For comparison, an optical photo of a

sample implanted with the same P^+ doping profile but at high temperature (600ºC) and annealed with the same conditions is shown in Fig 3.8c.

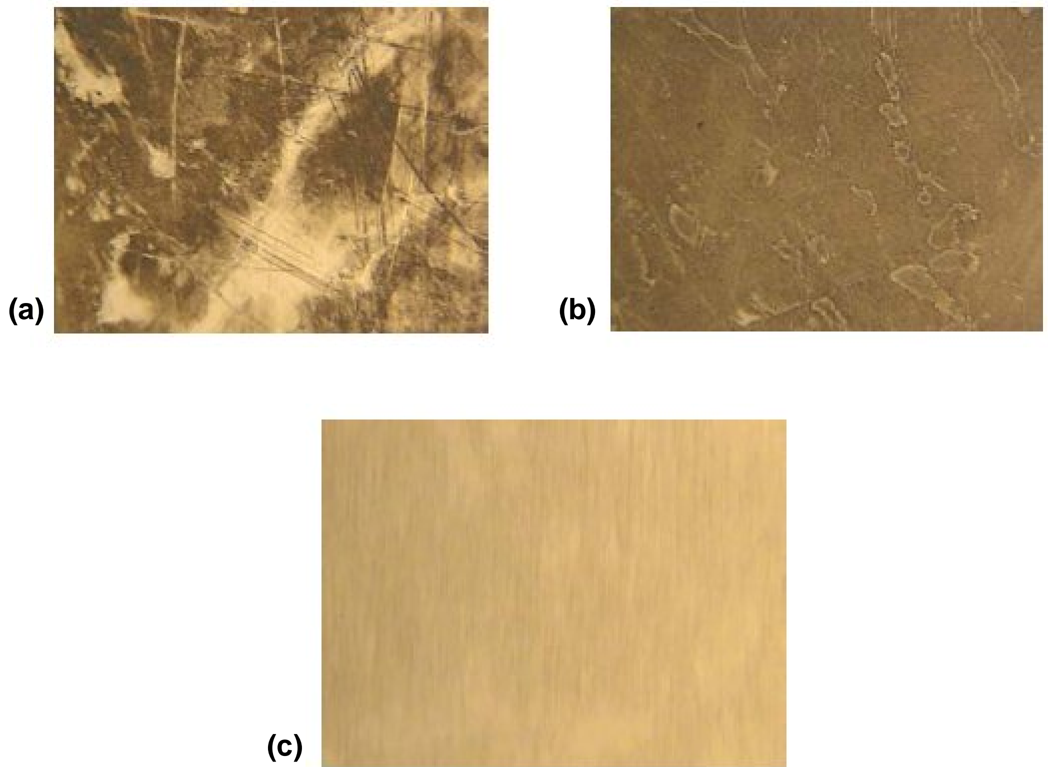


Figure 3.8 Optical microscopic pictures of samples implanted and annealed. (a) and (b) P^+ implantation at room temperature and annealed at 1650ºC in N_2. (c) P^+ implantation at 600ºC and annealed at 1650ºC in N_2.

3.3.2 Activation grade

Traditionally, the acceptor activation grade which depends on the processing conditions has been taken as a quality mark of the doping process. Usually, doped semiconductors are characterised by Hall and SIMS measurements in order to determine the free hole concentration (p) and the doping concentration (N_A). Then, the activation rate can be calculated via $A = p/(I \cdot N_A)$, where I is the ionisation degree. This procedure is straightforward if the temperature during the Hall measurements is high enough for almost complete ionisation ($I \approx 1$). Unfortunatelly, the temperatures necessary to approach the complete ionisation regime in moderate or heavily *Al* doped SiC are too high as illustrated in Fig 2.3 of chapter 2. As an example, in order to obtain an ionisation grade $I > 0.8$ for an Al concentration of $1 \times 10^{19} cm^{-3}$, the temperature must be raised to about 2000ºC. This temperature is clearly out of the typical temperature range of Hall measurements (-200ºC to 600ºC).

Therefore, in order to evaluate the quality of doping by implantation and subsequent annealing it seems much more reasonable to compare resistivities because the radiation damage influences the acceptor activation as well as the mobility.

3.3.2.1 Substitutional activation of the implanted Aluminum

Table 3.6 shows the sheet resistance (R_{SH}) values extracted from TLM measurements at room temperature together with the corresponding resistivity (*r*) values for the three different aluminum implantations (P^+, P, and P^- doping levels) performed on various samples. The *I-V* curves from TLM structures were measured in force-sense configuration in order to minimize the parasitic resistance contributions from the experimental setup.

Table 3.6 Sheet resistance (R_{SH}) and resistivity (*r*) values extracted from TLM measurements at RT for the three different aluminum doping levels implanted.

Sample	Annealing Temp/Time/Gas	P^+ (2´10^{19}cm^{-3})		P (2´10^{18}cm^{-3})		P^- (2´10^{17}cm^{-3})	
		R_{SH} (kW/□)	r (Wcm)	R_{SH} (kW/□)	r (Wcm)	R_{SH} (kW/□)	r (Wcm)
CQ1	1700ºC 30min Ar	19.2	0.48	58.9	2.94	1620	129
CQ3	1650ºC 45min N_2	15.5	0.38	33.5	1.67	609	30
CQ4	1650ºC 45min N_2	15.8	0.39	44.4	2.22	885	71
S1	1700ºC 30min Ar	20.1	0.50	60.0	3.00	1750	140
S2	1650ºC 30min N_2	15.4	0.38	52.5	2.62	600	48

The resistivity values are obtained from the sheet resistance values by multiplying these with the corresponding depth of the implanted box-like doping profile. The redistribution of aluminum during high temperature activation anneal is almost negligible. Figure 3.9 shows a multiple-energy implanted profile after anneal at 1700ºC for 30 min in *Ar* together with the I^2SiC and TRIM simulated profiles. No outdiffusion of aluminum on the surface and no diffusion deep in the crystal is observed. Therefore, from figures shown in section 3.2 we get *d*=0.25 µm, 0.5 µm and 0.8 µm for the P^+, P, and P^- doping level profiles, respectively, with the exception of sample CQ3 where the depth of the P^- doping level is 0.5 µm.

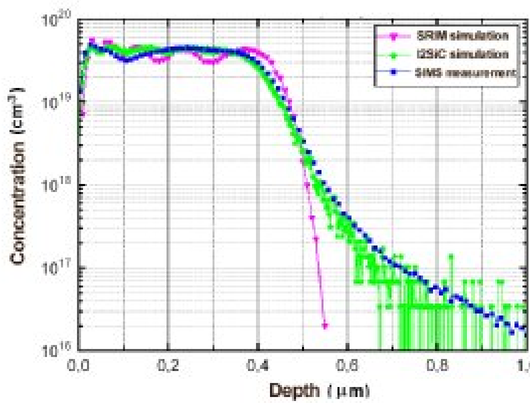


Figure 3.9 SIMS measurement of a multiple energy aluminum implantation profile. SRIM and I^2SiC simulated profiles are also shown for comparison.

As it can be inferred from the resistivity values obtained in the different samples, the anneal at 1650ºC for 45min in N_2 (samples CQ3 and CQ4) shows higher efficiency in terms of electrical activation grade in comparison to that at 1700ºC for 30min in Ar (samples CQ1 and S1). It can also be observed that annealing time plays no substantial role in the activation process for times greater than 30 min. It must be pointed out here that the high sheet resistance values in Al implanted samples is not due to lack of implant substitutional activation, but due to high carrier ionisation energy.

In Table 3.7, some resistivity results obtained after Al implantation and subsequent annealing extracted from the literature are presented along with the parameters of the doping process.

Table 3.7 Process parameters of selected doping experiments for the production of low resistivity p-type SiC.

Al concentration (cm^{-3})	Implantation temperature (ºC)	Annealing temperature/time	Resistivity (Wcm)	Polytype	Reference
1.5×10^{21}	400	1650ºC 10 min	0.06	6H	[199]
1×10^{21}	650	1670ºC 6 min	0.09	4H	[127]
5×10^{20}	500	1800ºC 30 min	0.10	4H	[133]
5×10^{20}	400	1650ºC 10 min	0.11	6H	[199]
1.8×10^{20}	1000	1650ºC 5 min	0.23	4H	[129]
1.8×10^{20}	650	1650ºC 5 min	0.59	4H	[129]
1.8×10^{20}	650	1700ºC 5 min	0.40	4H	[129]
1.5×10^{20}	800	1600ºC 30 min	0.20	6H	[115]
1×10^{20}	850	1600ºC 45 min	0.40	6H	[115]
1×10^{20}	650	1670ºC 12 min	0.51	4H	[127]
1×10^{20}	650	1650ºC 30 min	0.53	4H	[200]
5.7×10^{19}	400	1650ºC 30 min	0.6	4H	[201]
5×10^{19}	400	1650ºC 10 min	0.49	6H	[199]
4×10^{19}	RT	1700ºC 30 min	0.45	6H	[202]
2×10^{19}	400	1650ºC 45 min	0.38	4H	This thesis
2×10^{19}	400	1700ºC 30 min	0.50	4H	This thesis
1×10^{19}	650	1670ºC 12 min	2	4H	[127]
3.3×10^{18}	650	1670ºC 12 min	5	4H	[127]
2×10^{18}	400	1650ºC 45 min	1.67	4H	This thesis
2×10^{18}	400	1700ºC 30 min	3	4H	This thesis
2×10^{18}	500	1600ºC 30 min	9	4H	[203]
2×10^{18}	500	1700ºC 30 min	5	4H	[203]
2×10^{17}	300	1650ºC 45 min	30	4H	This thesis
2×10^{17}	300	1700ºC 30 min	140	4H	This thesis
1.6×10^{17}	1000	1600ºC 5 min	420	4H	[128]

The Al acceptor is best-suited for the production of low resistivity p-type SiC because it has the lowest ionisation energy in SiC and a natural tendency to occupy electrically active Si sites. A further advantage is its high solubility which reduces the problems associated with acceptor losses by precipitation as known from B doping. However, also in the ideal case of

uncompensated and fully activated acceptors, the RT resistivity cannot be brought below 0.05Ωcm in heavily Al doped SiC as long as normal, thermally stimulated band conduction is the dominating process. This limit is settled by the physical constraints for the acceptor ionisation and hole mobility under the conditions of high Al concentrations. The very upper concentration where normal band conduction has been observed is $1\times10^{21}cm^{-3}$. However, for fully activated Al acceptors the Mott transition to impurity band, metallic-like conduction can be predicted for $2\times10^{20}cm^{-3}$. Nevertheless, Al impurity band conduction can be exploited for the formation of low resistivity contact areas to p-type material.

The resistivity r of p-type SiC is given by

$$r = \frac{1}{q \cdot p \cdot m_p} \tag{3.2}$$

where q, p and m_p are the electron charge, the concentration of holes in the valence band and their mobility, respectively. The highest mobility values are observed in defect-free epilayers. [125]. Using the maximum hole mobility value (m_p=117 cm^2/Vs) and the hole concentration of uncompensated material (taking into account the incomplete ionisation of aluminum dopants at room temperature, with E_A=190meV), the minimum resistivity can be calculated via Eq. 3.2. Figure 3.10 shows the room temperature resistivity of aluminum doped SiC considering two different mobility values (solid and dashed black line) and compensating donor centers (red line) as a function of the acceptor concentration. The maximum and minimum experimental data values (scatter points) are also shown for comparison.

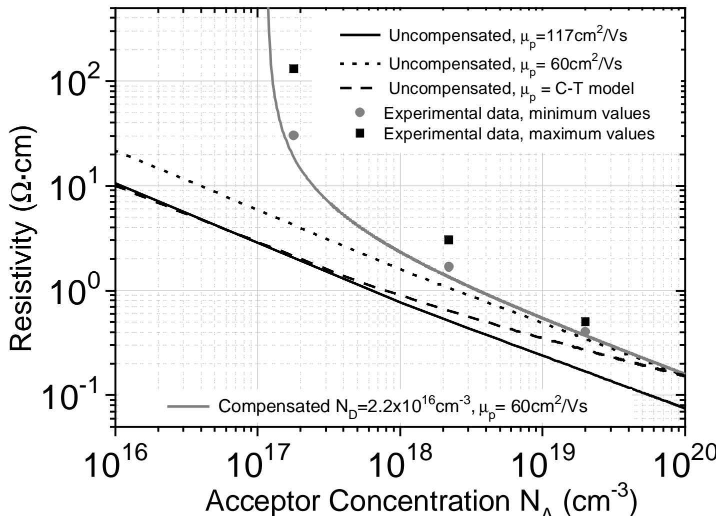


Figure 3.10 Resistivity at RT as function of Al concentration. Black lines represent the predicted resistivity assuming complete acceptor activation, no compensation and constant mobilities. Maximum epilayer mobility (μ_p=117 cm^2/Vs) is used in the solid black line while a reduce mobility for implanted layers (μ_p=60 cm^2/Vs) is used in dashed line. Blue line curve is calculated taking into account the concentration dependence hole mobility using the Caughey-Thomas model. The red line represents the theoretical resistivity for a compensated material with N_D=2.2×10^{16} cm^{-3} and μ_p=60 cm^2/Vs. The experimental data from Table 3.6 is also presented for comparison.

As it can be observed from Fig. 3.10, the resistivity curve approaches better to the experimental data using the reduced mobility value μ_p=60 cm^2/Vs instead of the maximum epilayer mobility of 117 cm^2/Vs. The resistivity has also been plotted using the analytical expression for the hole mobility dependence on acceptor concentration calculated from the Caughey-Thomas model

$$\mu_p = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_D + N_A}{N_{ref}} \right)^{\gamma}} \tag{3.3}$$

where μ_{max}=117 cm^2/Vs, μ_{min}=16 cm^2/Vs, N_{ref}= 1.76×10^19 cm^{-3} and γ=0.34 [126].

Previous research on *p*-type implantations has demonstrated that the mobility is substantially smaller in the implanted layers compared to bulk mobility [127,128]. Saks et al. [128,129] reported a hole mobility values of 60cm^2/Vs and 8-18cm^2/Vs for 4H-SiC aluminum implanted layer with a targeted acceptor concentrations of $1.33\times10^{17}cm^{-3}$ and $1.8\times10^{20}cm^{-3}$, respectively, after an activation anneal at 1600ºC for 5min in Ar. The reduction in hole mobility in the implanted layers is probably due to scattering from unannealed implant damage- that is, donor-like compensating traps. Since most compensating donors in a *p*-type layer are occupied by holes at 300K and therefore are positively charged, these donors will be effective coulombic scattering centers which reduce the mobility. As the density of activated *Al* acceptors increases the hole mobility decreases due to increased impurity scattering.

Results in Fig 3.10 show that there is a high density of compensating donors N_D (~$2.2\times10^{16}cm^{-3}$) in all measured samples. Some of this compensation arises from the *n*-type doping in the epitaxial layer ($9\times10^{15}cm^{-3}$ for CQ1, CQ3 and CQ4 samples, and $2.5\times10^{15}cm^{-3}$ for S1 and S2 samples). The remainder presumably arises from unannealed implant damage. Thus, compensating donors levels of about $1.3\times10^{16}cm^{-3}$ and $1.9\times10^{16}cm^{-3}$ are obtained for samples CQ and S, respectively. These values correspond to a 10-15% of the lowest acceptor doping concentration ($2\times10^{17}cm^{-3}$) and they are in good agreement with the range of values obtained in other works [128]. This amount of compensation is substantial, and it is in the same range of compensation (5-20%) associated with n-type nitrogen implant doping [130]. The accuracy of this calculation of the compensation level is poor because it depends on many constants which are not well known. As a best guess from performing many fits to determine the sensitivity of the fits to N_D, the error in N_D may easily be ~±20%. Hallén and co-workers [131] have studied the evolution of defects in Al-implanted 4H-SiC using TEM. They observed significant densities of interstitial “planar faults” after annealing at 1600-1700ºC which reside primarily around the projected range of the implanted aluminum. These or other defects such as di-interstitial or di-vacancies [132] may be responsible for the electrically active compensating defects observed.

To allow a more detailed analysis of the resistivity behaviour on aluminum implanted layers, high-temperature measurement (up to 290ºC) of the sheet resistance from TLM structures were carried out in sample CQ3. Figure 3.11 shows the temperature dependence of the resistivity obtained for the three different targeted concentration.

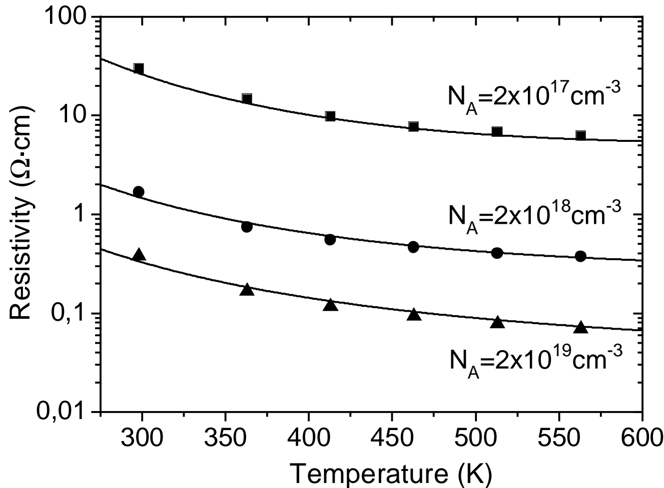


Figure 3.11 Temperature dependence of the resistivity obtained for the three different targeted concentrations (-▲- $2\times10^{19}cm^{-3}$, -●- $2\times10^{18}cm^{-3}$, -■- $2\times10^{17}cm^{-3}$).

The observed temperature dependence is very similar to recent results [127, 128]. The results shown in Fig 3.11 are fitted with theoretical curves, using the temperature dependence expressions for the resistivity calculation;

$$\rho = \frac{1}{q \cdot p(T) \cdot \mu_p(T)} \tag{3.4}$$

where

$$p(T) = \frac{-1 + \sqrt{1 + 4 g_A \dfrac{N_A}{N_V(T)} exp\left(\dfrac{E_A - E_V}{k_B T}\right)}}{2 g_A \dfrac{N_A}{N_V(T)} exp\left(\dfrac{E_A - E_V}{k_B T}\right)} \cdot (N_A - N_D) \tag{3.5}$$

with the $N_V(T)$ expression given by Eq 2.4b, $g_A = 4$ and (E_A-E_V= 0.19eV).

$$\mu_p(T) = \mu_{p\,max} \cdot \left(\frac{T}{300}\right)^{\alpha} \tag{3.6}$$

with μ_{pmax}= 60 cm^2/V·s and α = -1 as the obtained fitting parameters.

Performing the fitting of the experimental data with the above expressions allows a rough estimation of the electrical activation grade through the evaluation of the N_A value that best fits the resistivity temperature dependence for each different implanted doping level. We find that the fitting values of N_A agree very well with the targeted concentrations for each of the

three different doping levels. Thus, this approach gives an activation rate in the range of 90-100% for the three targeted concentrations. This result is in good agreement with high activation rates in the range of 70-100% reported recently for aluminum implants in SiC, at similar doses and annealing temperatures [129,133,134]. It demonstrates that our implantation and annealing conditions are effective for an efficient p-type doping process.

3.3.2.2 Analysis of the Boron implanted transient diffusion

Behaviour of implanted boron is qualitatively quite different from aluminum. Transient-enhanced diffusion of boron during high-temperature activation anneals is experimentally observed in 4H-SiC [135,136]. B atoms are light and can be implanted to a greater depth without amorphizing the implanted layer. However, they show a transient enhanced diffusion into the damage region during the anneal, which results in an almost complete out-diffusion of the implanted fluence.

Figure 3.12 shows the SIMS profile of the P^- implanted layer in sample CB1 after high temperature annealing (1650ºC for 45min) together with the I^2SiC simulated profile of the as-implanted stage. A clear redistribution of the implanted B profile is observed after the activation anneal.

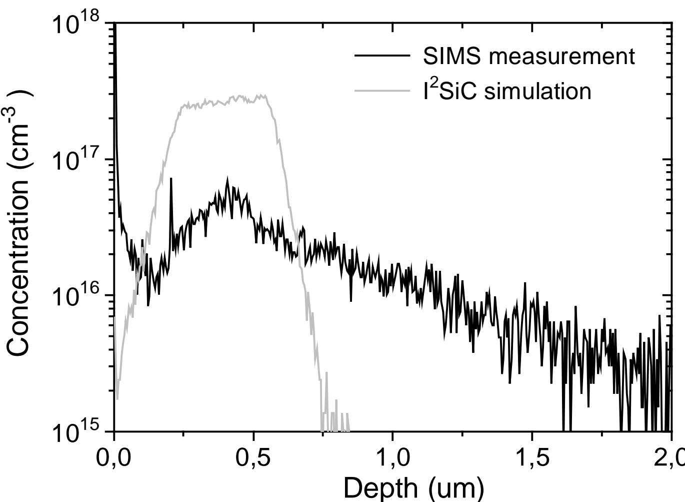


Figure 3.12 SIMS profile after high temperature activation anneal of sample CB1 (red line). The I2SiC simulated profile for the as-implanted stage (blue line) is also shown for comparison.

The SIMS profile shows a B concentration near the surface lower than 2×10^{16}cm^{-3}, a maximum concentration of 5-6$\times10^{16}$cm^{-3} at about 0.45µm within the damage region of the implanted layer, and a pronounced B diffusion tail which extends 2 microns into the undamaged SiC epilayer.

The fast diffusion of B in SiC compared to other dopants and the fact that B prefers the substitutional position of the Si sublattice suggest that interstitial-substitutional (*i-s*) mechanism, namely the dissociative and the kick-out mechanisms, control the diffusion. These mechanisms have been established for the diffusion of Au, Pt, and Zn in Si and also for Zn in GaAs. For B in SiC, the *i-s* mechanisms are expressed by the reactions

$$B_i + V_{Si} \rightleftarrows B_{Si} \quad (3.7)$$

$$B_i \rightleftarrows B_{Si} + Si_i \quad (3.8)$$

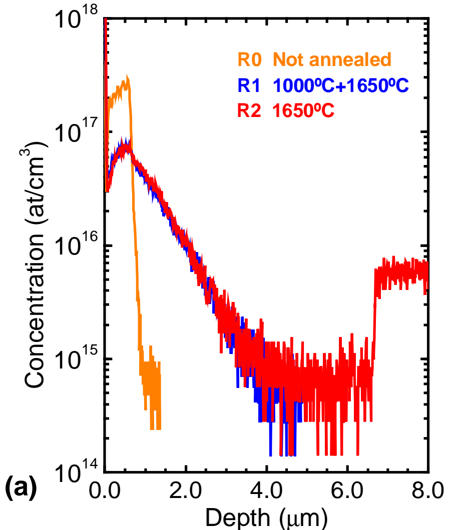
Equation (3.7) represents the dissociative reaction. Mobile interstitial B atoms (B_i) occupy vacancies on the Si sublattice (V_{Si}) and thereby become substitutional defects (B_{Si}). In the kick-out mechanism [see Eq. (3.8)], the *i-s* exchange creates a Si self-interstitial Si_i.

The driving force for the accumulation of B atoms at the surface is not yet clear. It is suggested that this pile-up is caused by a high concentration of Si and C interstitials generated in the surface-near region by the B^+ implantation itself. According to Christel and Gibbons [137] Si atoms are accumulated closer to the surface because of their heavier mass in comparison to C. This surplus of Si interstitials in the vicinity of the surface become highly mobile during the annealing and thereby enhance the diffusion of boron towards the surface. The surface acts as a sink for both elements and evaporation can occur according to their vapour pressure. This causes an enhanced B out-diffusion, and as a consequence, the observed dip close to the surface. An analysis of the SIMS profile of Fig. 3.12 reveals that only a 36% of the implanted B dose remain in the sample after the anneal.

It has not been possible to directly obtain the resistivity of any of the two different doping concentrations (P^+ and P^- levels) of the B-implanted layers from TLM measurements, because the sheet resistance of these samples was very high (>3×10^6 Ω/□) and the contact resistivity was non-ohmic even after a high rapid thermal anneal (RTA) of the metal at 950ºC for 3min. Moreover, due to the redistribution of the implanted profile after the activation anneal it is not possible to precisely determine the depth of the diffused profile.

The diffusion away from the implanted region is not always desired for device structures. In particular, the outdiffusion at the surface is detrimental to the preparation of ohmic contacts to the surface. Ohmic contacts with low contact resistance require high doping concentration. Hence, a way has to be found to considerably suppress the boron outdiffusion. This means the concentration of silicon interstitials in the region damaged by the ion implantation has to be strongly reduced before boron starts to move. Two approaches have been proposed:

1) It is known from the literature that in 6H-SiC carbon and silicon vacancies recombine with carbon and silicon interstitials at temperatures of 250ºC and 750ºC, respectively [138]. At temperatures below 1000ºC the boron diffusion is almost negligible. A two-step annealing with the first step at 900ºC for at least 2h and the second step with a temperature of 1700ºC for 30min was tried and a considerable reduction in the boron diffusion could be observed [139]. To verify this approach we performed a two steps annealing process on a lightly boron implanted test sample ($1.3\times10^{13}cm^{-2}$ implanted dose). The first annealing step was performed at 1000ºC for 30min follow by the second annealing step at 1650ºC for 45min. Figure 3.13 shows the obtained SIMS profiles for the two step annealed sample together with that of a single step annealed sample and a reference sample not annealed.



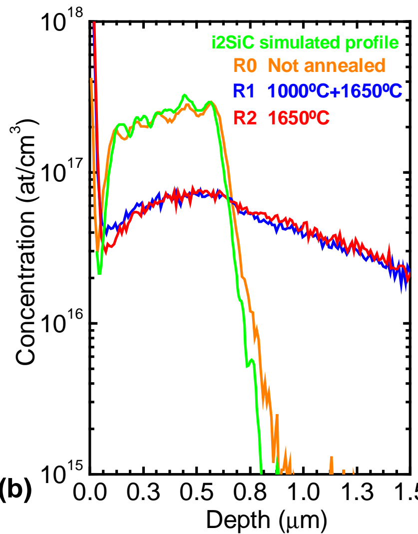


Figure 3.13 SIMS profiles of the analysed samples (a) High in-diffusion (up to 4μm in depth) of the two annealed samples showing no suppression of boron diffusion for the two-step annealed sample, (b) Zoom of the SIMS profiles near the surface region, the I^{2}SiC simulated profile is also shown for comparison.

As it can be clearly seen, no suppression of boron in-diffusion is observed for the two-step annealed sample in comparison to that annealed in only one high temperature step. Moreover, our experimental test of the two-step annealing could not totally prevent the boron from diffusing out at the surface. An integration of the SIMS profiles shows that 38% and 37% of boron is outdiffused in samples R1(two-step annealed) and R2 (single process annealed), respectively. One possible cause of this low efficiency of our two-step annealing process on boron diffusion suppression is the short time (30min) of the first annealing step, that in the reported work by Pensl et al. is of 2h. However, our outdiffusion percentages values are close to those reported by Pensl [139].

2) Another way of reducing the silicon interstitials is known from silicon. Introducing carbon into silicon binds silicon interstitials by forming stable pairs of interstitial silicon and carbon. All the silicon interstitials bound to carbon no longer participate in promote the boron diffusion. In SiC, carbon interstitials are always present. An increased carbon interstitial concentration by carbon co-implantation could substantially reduce the amount of interstitial silicon. SIMS investigations of boron/carbon co-implanted SiC show a strongly suppressed migration of boron [139]. The amount of boron migrating into the material is reduced by almost an order of magnitude and the outdiffusion of boron can be reduced by approximately a factor of 2. But also in the case of boron/carbon co-implantation the outdiffusion cannot be totally avoided.

This means that the formation of low-resistive ohmic contacts to boron-implanted *p*-type SiC has to involve a dry etching step to remove the low-doped top layer before the actual metal deposition.

Due to low activation rates, dose-dependent activation, and diffusion of boron atoms during annealing, it would be difficult to use boron to achieve a specific *p*-type doping profile by implantation. Consequently, aluminum may be preferred when uniform, accurate doping profiles are required.

3.4 Metal-semiconductor Contacts

All useful semiconductor electronics require conductive signal paths in and out of each device as well as conductive interconnects to carry signals between devices on the same chip and to external circuit elements that reside off-chip. While SiC itself is theoretically capable of fantastic operation under extreme conditions (see chapter one), such functionality is useless without contacts and interconnects that are also capable of operation under the same conditions to enable complete extreme-condition circuit functionality. Previously-developed conventional contact and interconnect technologies will likely not be sufficient for reliable operation in extreme conditions that SiC enables. The durability and reliability of metal-semiconductor contacts are one of the main factors limiting the operational high-temperature limits of SiC electronics. Similarly, SiC high-power device contacts and metallization will have to withstand both high temperature and high current density stress never before encountered in silicon power electronics experience. There are both similarities and a few differences between SiC ohmic contacts and ohmic contacts to conventional narrow-bandgap semiconductors (e.g., Si, GaAs). Therefore, pre-metal-deposition surface preparation, metal deposition process, choice of metal, and post-deposition annealing can all greatly impact the resulting performance of metal-SiC contacts.

According to the model of Chang and Sze [140], lowering the barrier height or increasing the doping concentration can reduce the ohmic contact resistance. Therefore a low Schottky barrier is necessary to create good ohmic contacts. However, a large barrier is necessary to obtain a good Schottky, or rectifying contact with low leakage current. In some applications, like self-aligned metal-semiconductor-field-effect-transistor (MESFET), forming the ohmic contact and the Schottky barrier with the same material can be useful to simplify the fabrication procedure and reduce the gate length. A detailed description of the general theory on metal-semiconductor junction formation can be found in Appendix D.

3.4.1 Ni/Ti bilayer contact

Although different metallic contacts have been object of study in the last decade (Al, Co, Pd, W), Ni and Ti are those which are presently widely used in the technology of SiC Schottky diodes both for the rectifying-front and/or for the ohmic-back contact. Recently, some efforts have been spent in the fabrication of dual-metal Schottky diodes, using both Ni and Ti as barrier metals [141,142]. This bi-layer configuration can give a good compromise between the low forward voltage drop of a low barrier Ti/4H-SiC diode and the low leakage current values of a high barrier Ni/4H-SiC diode. Thus, we have implemented a Ti/Ni bilayer contact to our samples.

Obviously, the possibility to control the electrical properties of contacts is strictly related to the effects of thermal annealing on dual-metal systems. Thus, in the next sections it is reported the electrical and structural characterization of Ni/Ti bi-layer contact on our 4H-SiC aluminum implanted samples for both Schottky and ohmic purposes after rapid thermal anneals at different temperatures. The reported results are those extracted from sample CQ3 (AD-0602-02 CREE´s wafer) measurements.

After contact opening, Ti and Ni layers were sequentially deposited by sputtering and patterned by wet etching to define the circular diodes. The thickness of the Ti and of the Ni layers was in the range 25-35 and 90-110nm, respectively. Both Schottky and PiN diodes were processed on the same sample to fabricate Schottky contacts on *n*-type epilayer and ohmic contacts on implanted p^+-type regions, respectively.

In order to analyse the influence of the RTA contact anneals on the electrical characteristics of both Schottky and PiN diodes, several sequential thermal processes were performed at different temperatures, up to 900ºC for 3min. The electrical characterization of the Ni/Ti contact under the different thermal anneals was carried out by measuring the current-voltage (*I-V*) characteristics of diodes at room temperature and by extracting the contact resistivity value from TLM structures. Forward measurements were performed using a Wentworth chuck equipped with a Keithley 238 source meter, while reverse characteristics were measured using a Tektronix 370 curve tracer. The *I-V* curves were acquired in force-sense configuration in order to minimize the parasitic resistance contributions coming from the experimental setup. The structural characterization of the metal-semiconductor structure was monitored by X-Ray Diffraction (XRD) performed with a Rigaku Rotaflex diffractometer.

3.4.1.1 Schottky contact

Figure 3.14 shows the forward current-voltage characteristics at room temperature of the Schottky diodes after contact RTA at different temperatures for 3min. Characteristics parameters such as forward voltage drop at 100A/cm^2 (V_F), Schottky barrier height (Φ_B), ideality factor *n* and on-resistance (R_{on}) were determined by *I-V* analysis following the thermionic-emission theory [143] and are summarised in Table 3.8.

As it can be seen, a thermal annealing at 350ºC provides the optimal forward performances of Schottky contacts with the lowest forward voltage drop and low specific on-resistance. It is worth to mention here that the specific on-resistance value achieved is close to the theoretical value of our epitaxial configuration (1mΩcm^2). The increase of the Schottky barrier from a value of 0.77eV (typical of Ti) in the as-deposited stage towards 1.25eV (typical of Ni_2Si) in the high temperature annealed stage is due to the solid state reaction involving the metallic Ni/Ti bi-layer, as it is inferred from XRD measurements shown in

Figure 3.15. At high temperatures (above 500ºC) the interdiffusion of the two elements in the bi-layer occurs and the Ni atoms that reach the interface with SiC can form silicides. When increasing the annealing temperature, the nickel silicides tend to transform into the most stable phase (Ni_2Si), implying an increase of the Schottky barrier value.

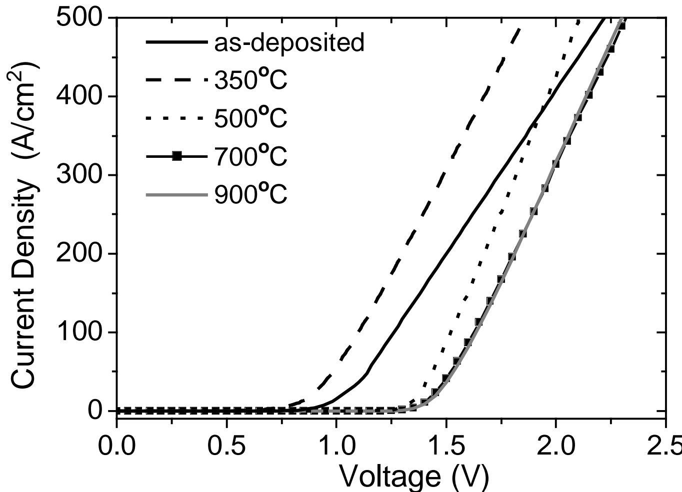


Figure 3.14 Forward *I-V* characteristics of Schottky diodes after different RTA temperature.

Table 3.8 Main electrical parameters of Schottky diodes extracted from *I-V* characteristics measured after RTA of Ni/Ti contact at different temperatures.

RTA Temperature	V_F @100A/cm² [V]	$Φ_B$ [eV]	Ideality factor *n*	R_{on} [mΩ·cm²]	Breakdown voltage [V]
as-deposited	1.28	0.77	2.1	2.4	800
350ºC	1.10	0.85	1.9	1.6	875
500ºC	1.52	1.10	1.7	1.5	1025
700ºC	1.61	1.15	1.6	1.7	1400
900ºC	1.61	1.25	1.5	1.8	1610

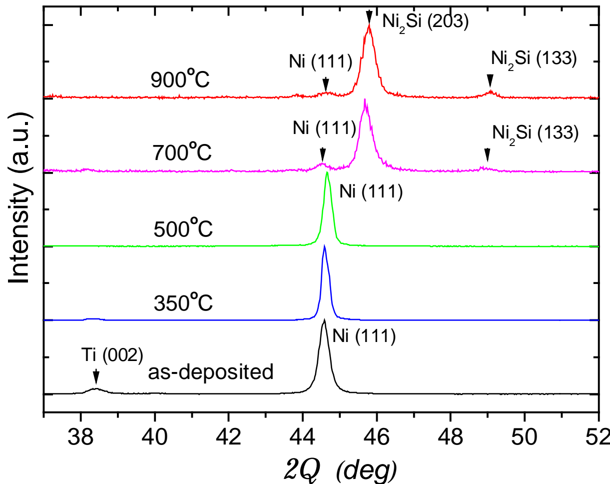


Figure 3.15 XRD pattern of the Ni/Ti/4H-SiC contact annealed at different temperatures between 350ºC and 900ºC for 3 minutes.

This increase of the Schottky barrier height is also reflected in the reverse characteristics of the diodes. Under reverse bias a continuous reduction of the leakage current is observed by increasing the RTA temperature, as it can be seen in Figure 3.16. The reduction of leakage current is due to the increase of the Schottky barrier and leads to a significant improvement of the breakdown voltage, increasing it from 800V at the as-deposited stage up to 1610V after the 900ºC RTA, thus approaching to the theoretical maximum breakdown voltage value for our epitaxial layer (~1900V). The results shown in Figure 3.16 correspond to a Schottky diode with a double zone JTE structure as an edge termination.

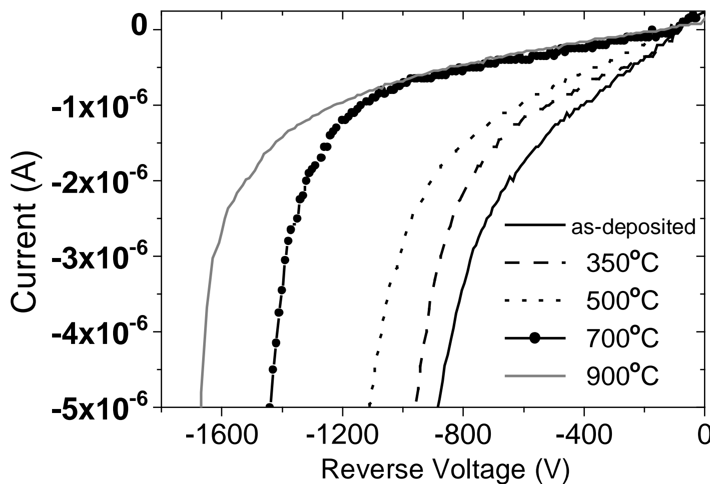


Figure 3.16 Reverse *I-V* characteristics of Schottky diodes after RTA at different temperatures.

3.4.1.2 Analysis of the Schottky Barrier Inhomogeneities

Recent interest in wide-bandgap semiconductors such as SiC and GaN has increased the demand for better understanding and control of the metal contacts, in order to make performant ohmic and rectifying Schottky contacts. However, fabricated Schottky contacts on these wide-bandgap materials often exhibit significant device-to-device variations and/or “nonideal” behaviour in current-voltage (*I-V*) characteristics. It is important to understand the physical origin of such nonideal behaviour so that it can be controlled in future device applications. Inhomogeneities and/or residual processing-induced contamination in the interface are commonly the reason for deviations from the ideal behaviour in the electrical characteristics of Schottky contacts on SiC.

An accurate theoretical modelling of the effect of such inhomegenities on the electron transport across the metal semiconductor (MS) interface was developed by Tung [144], taking into account the possible presence of a distribution of nanometer-size “patches” with lower barrier height embedded in a uniform high barrier background. This model gives an explanation for a large series of abnormal experimental results on “real” Schottky contacts,

such as ideality factors greater than unity, temperature dependence of the Schottky barrier height (SBH) and ideality factor, soft reverse characteristics, and the strong correlation that is often observed between the SBH and the ideality factor measured on sets of diodes [145].

In this section we address the above questions by using the previously reported Ni/Ti bilayer barriers formed on weakly *n*-doped epitaxial 4H-SiC high quality wafers. The model is applied to evaluate the interface quality of Schottky diodes obtained with different fabrication process and areas.

Using the measured *I-V* curves, we first applied the model to the circular Schottky diodes annealed at 900ºC. The thermionic emission theory predicts that the current across a uniform metal-semiconductor interface is given by [143]:

$$I = I_S \left[exp\left(\frac{qV}{nk_B T} \right) - 1 \right] \tag{3.9}$$

where I_S is the saturation current expressed by

$$I_S = S\,A^* T^2 exp\left(-\frac{q\Phi_B}{k_B T} \right) \tag{3.10}$$

where S is the diode area, A^* is the effective Richardson constant (146A/cm^{2}K^2 for n-type 4H-SiC [142]), T is the absolute temperature, k is the Boltzmann constant, q is the electronic charge, Φ_B is the Schottky barrier height, V is the applied voltage and n is the ideality factor.

Figure 3.17 shows the semi-log *I-V* characteristics of the measured Schottky diodes at different temperatures, ranging from 300 to 455K. The ideality factor n and the Schottky barrier height Φ_B were determined by fitting the linear region of the forward *I-V* curves reported in Fig. 3.17 according to the Eq. (3.9). As it can be clearly seen from Fig. 3.18, these parameters are both temperature dependent.

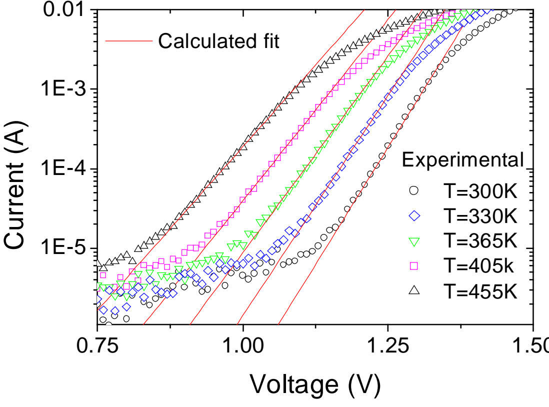


Figure 3.17 Forward *I-V* characteristics of Schottky diodes at different temperatures between 300 and 455K.

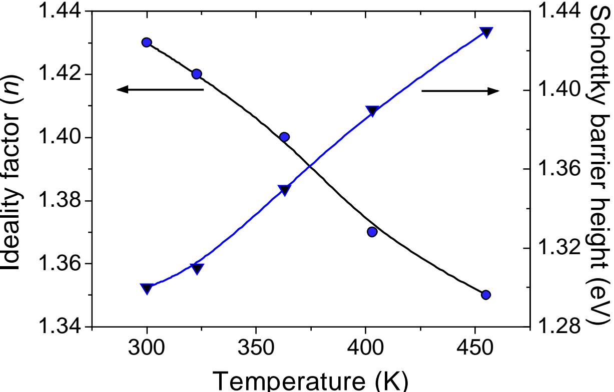


Figure 3.18 Ideality factor n and Schottky barrier height Φ_B as a function of the absolute temperature.

The barrier height shows an increase with temperature and the ideality factor n follows a temperature behaviour already observed [146] and referred as the "T_o anomaly". It means that the ideality factor can be expressed in the form $n \sim 1+T_o/T$, with T_o=104 K in our case. This plot is shown in Fig. 3.19, in which the straight line representing the behaviour of an ideal Schottky contact (i.e., with n=1) is also reported as reference. These parameters dependences are typical of a real Schottky contact with a distribution of barrier inhomogeneities [146, 147].

The conventional Richardson´s plot taking into account the temperature dependence of the ideality factor (plotting the $ln(I_S/T^2)$ as a function of $1/nkT$) has been plotted in Fig. 3.20. This plot allows the determination of the effective SBH and the evaluation of the Richardson constant. From the slope of the linear fit to the data, an effective barrier height Φ^{eff}_B=1.68eV was found, while from the y-axis intercept a value of A^*=1.15 A/cm^{2}K^2 was determined using the total contact area of the diode. The resulting extracted value of A^* is much lower than the theoretical value of 146 A/cm^{2}K^2 for 4H-SiC.

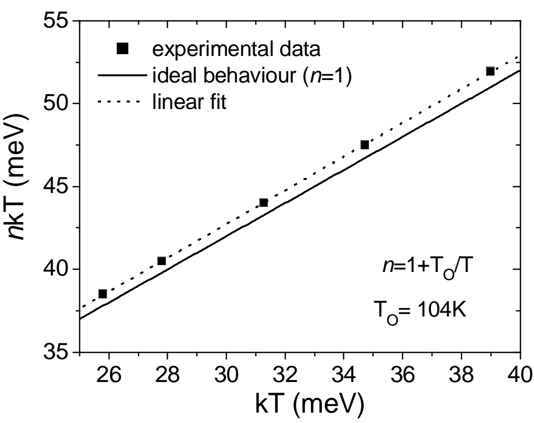


Figure 3.19 Plot of *nkT* as a function of *kT* showing the T_O anomaly n =1+ T_O/T.

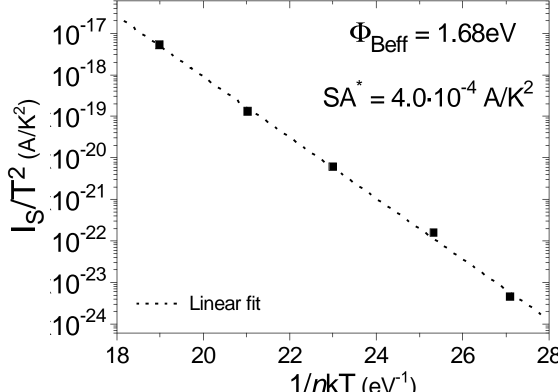


Figure 3.20 Richardson plot *ln(Is/T²) vs 1/nkT*. From the slope of the linear fit to the data, an effective SBH of 1.68eV was determined.

The variation of the experimental SBH versus the ideality factor extracted at different temperatures is presented in Figure 3.21. As it can be observed, a linear relationship exists, that can be explained by lateral inhomogeneities of the barrier height in Schottky barrier diodes [145]. Accordingly, the uniform barrier height Φ^o_B (i.e., the value which is expected for an homogeneous ideal contact) can be found by the extrapolation of Φ_B at n=1 of the line drawn in Fig. 3.21. In our case, a value of Φ^o_B =1.98eV was determined. These experimental values we have found agree with theoretical considerations predicting that the effective barrier Φ^{eff}_B, which characterizes an inhomogeneous contact, is smaller than that of a spatially homogeneous uniform barrier Φ^o_B [144].

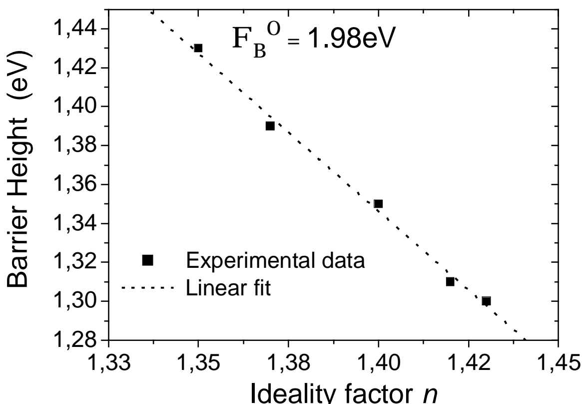


Figure 3.21 Schottky barrier height Φ_B *vs* ideality factor *n*.

Applying the Tung´s model [144], the effective Schottky barrier height Φ^{eff}_B and the uniform barrier height Φ^o_B of the metal/semiconductor contact are related by

$$\Phi^{eff}_B = \Phi^o_B - \gamma\left(\frac{V_{bb}}{h}\right)^{\frac{1}{3}}, \tag{3.11}$$

where γ is a parameter which is introduced to describe the inhomogeneity of the SBH and includes the effective area of the patch with a lower barrier and the deviation from the uniform high barrier Φ^o_B, $V_{bb}=F^o_B-ln(N_C/N_D)(kT/q)-V$ is the band bending, and $\eta=\varepsilon_S/qN_D$, being ε_S the permittivity of the material. From Eq. (3.11) it was possible to estimate a value of $\gamma=2.52\times10^{-4}$ $cm^{2/3}V^{1/3}$. It must be pointed out that, in order to simplify our calculations, a unique value of γ was used instead of a distribution.

If we consider a configuration of low barrier circular patches embedded in one region of high barrier Φ^o_B, the current flowing through the single patch can be calculated with Eq. (3.9) using the area of the patch A_{eff} as S and the effective barrier Φ^{eff}_B as Φ_B. The effective area of the low SBH patch can be expressed as

$$A_{eff}=\frac{4p\cdot g\cdot kT}{9q}\left(\frac{h}{V_{bb}}\right)^{2/3} \tag{3.12}$$

At room temperature, a value of $A_{eff}=8.97\times10^{-12}cm^2$ was determined.

Hence, the total current flowing through the diode can be obtained by rewriting Eq. (3.10) taking into account the effective area of the diode, given by $S=N\cdot A_{eff}$, where N is the number of patches covering the area of the diode. The various *I-V* curves of Fig. 3.17 where fitted with Eq. (3.9) using the number of patches N as fitting parameter. A value of $N=2\times10^5$ gave a good fit of the experimental data for each temperature (see Fig. 3.17). Therefore, in order to correctly determine the value of A^*, the Richardson´s plot must be modified by substituting the geometric area of the diode with the value of the total effective area of the patches ($N\cdot A_{eff}$). It is worth noting that the total area involved in the current transport represents only near 2%

of the entire geometric contact area considering the ideality factor we obtained, in accordance with previous related works [148,149].

Figure 3.22 shows the modified Richardson´s plot. From the slope of the fit line, a value of Φ^{eff}_{B}=1.68eV was obtained, matching exactly with the effective barrier height obtained from the previous calculation, while from the intercept, a value of the Richardson constant of A^*=139A/cm^{2}K^2 was determined, which is in satisfying agreement with the theoretical value.

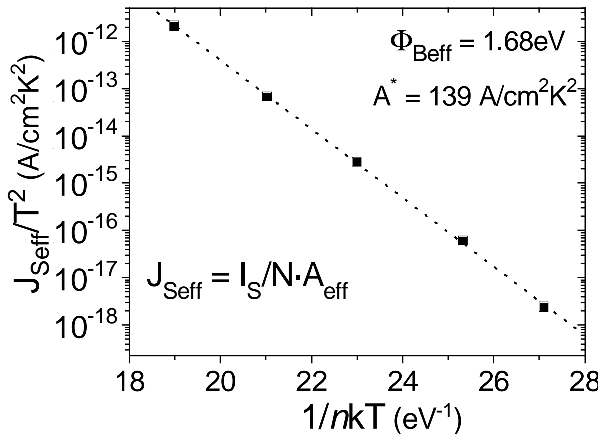


Figure 3.22 "Modified" Richardson´s plot *ln(J_{Seff}/T^2) vs 1/nkT.*

The value of the ideality factor and its temperature dependence are then a clear indicator of the quality of the interface and it also reflects the reliability we can expect for the device. In the example we chose, the ideality factor is high and results in a significant non uniformity of the current flow. However, the specific on-resistance of the diode is low (2mΩ·cm^2) and not far from the theoretical value. This means that we have very high current densities locally distributed at the metal/semiconductor interface and that the current spreads over the total area inside the semiconductor epilayer. Then, it does not significantly affect the on-resistance but it will clearly degrade the reliability of the structure inducing metal electromigration, hot spots and spiking.

Structural defects in the semiconductor, inhomogeneous doping, different metal structures at the interface, interface roughness, interfacial reactions, diffusion/interdiffusion of the applied materials, and contaminations of the semiconductor surface are possible candidates for the origin of the SBH nonuniformities. Their appearance depends sensitively on the employed materials and the preparation procedure of the Schottky contact.

Homogeneous barrier

For comparison of the interface characterisation, the model was then applied to square Schottky diodes with the same metalisation scheme (Ni/Ti) annealed at 350ºC. We have characterised square diodes with different areas and a fixed RTA annealing at 350ºC, and the

main electrical characteristics extracted from *I-V* measurements are summarised in Table 3.9. The ideality factor of the small and medium area diodes is similar to the previous one.

Table 3.9 Electrical properties of 4H-SiC Ni/Ti Schottky diodes after 350ºC contact anneal.

Area μm^2	Φ_B (eV)	*n*	R_{on} ($m\Omega \cdot cm^2$)
400x400	0.98	1.42	3.1
800x800	1.0	1.37	2.9
1200x1200	1.07	1.24	2.5

As seen in Fig. 3.23, the ideality factor and the Schottky barrier height as extracted from *I-V* curves show a less pronounced temperature dependence. This has been observed for the three different diodes areas considered. Applying the same data analysis performed in the previous section, we find nearly identical barrier values for the low barrier regions (Φ^{eff}_B=1.24eV) and for the high uniform background barrier (Φ^{o}_B=1.29eV). This indicates a higher uniformity of the interface. We associate this more homogeneous barrier formation to the low temperature value (350ºC) of the contact RTA. Temperatures higher than 450ºC are needed to start the solid state reaction between the metallic bi-layers and SiC to form nickel and titanium silicides [148]. Thus, at this low annealing temperature better interfacial quality is obtained due to the capability of Ti to grow epitaxially on hexagonal SiC [150], which results in a more uniform barrier.

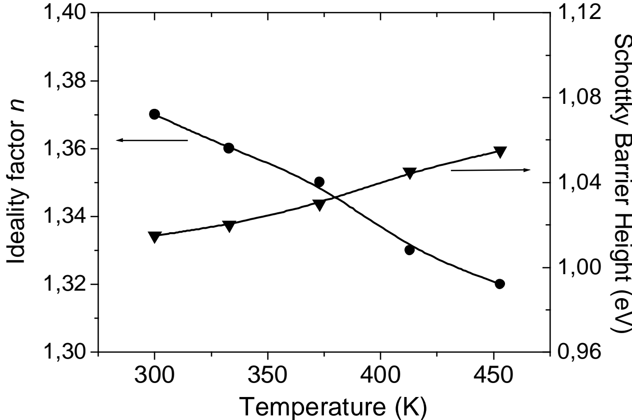


Figure 3.23 Ideality factor *n* and Schottky barrier height Φ_B as a function of the absolute temperature for the Ni/Ti/4H-SiC Schottky diode after a 350ºC contact RTA.

This characterisation methodology can be then highly useful to check a technological process for Schottky diode fabrication and optimise the deposition and annealing parameters.

3.4.1.3 Ohmic contact

Figure 3.24a shows the forward current-voltage characteristics at room temperature of bipolar PN diodes after the different RTA temperature of the contact. The contact resistivity (ρ_C) of as-deposited and annealed contacts was extracted from linear transmission line model (TLM) test structures implemented in the same set of masks used for the fabrication of the diodes. Characteristics I-V curves from TLM measurements between two pads (d=10μm) after each RTA process are shown in Fig. 3.24b. This structure also allows the evaluation of the sheet resistance (R_{SH}) of the aluminum implanted P^+ region ($2\times10^{19}cm^{-3}$ doping concentration). The extracted values of the main electrical parameters of diodes and the contact characterisation as a function of the anneal temperature are summarised in Table 3.10. As it can be seen from both Fig. 3.24 and Table 3.10 data, the contact becomes ohmic after annealing at 500ºC and it improves its ohmic characteristic significantly after RTA at 700ºC achieving a low contact resistivity value of 1×10^{-5} $\Omega\cdot cm^2$. To our knowledge, there are no reported contact materials that provide such a low contact resistivity on *p*-type 4H-SiC after annealing at 700ºC [151]. This ohmic transition can be attributed to the formation of nickel silicides at the SiC interface after the 500ºC RTA [142]. Longer contact annealing times demonstrated to have no effect on the contact resistivity. This result presupposes that the compounds responsible for the ohmic properties are formed during the first minutes and the annealing time plays no substantial role in the process.

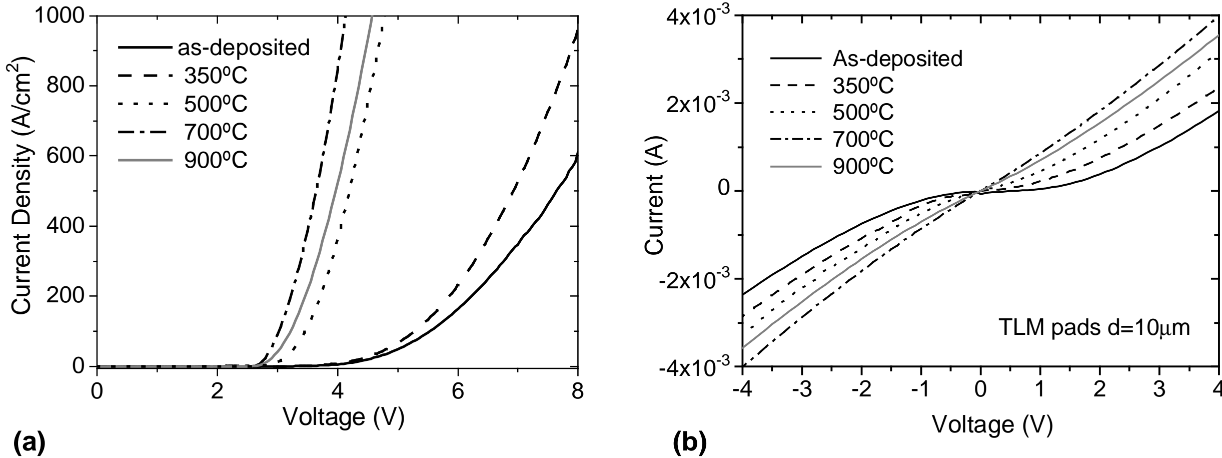


Figure 3.24 (a) Forward *I-V* characteristics of PN diodes after RTA at different temperatures. (b) The effect of RTA temperature on the TLM *I-V* characteristics measured between two pads with 10μm of distance.

The on-resistance determined at 1kA/cm^2 shows a decrease by the effect of conductivity modulation of the n^- epilayer by minority-carrier injection after the 500ºC RTA. The values of the ideality factor obtained (n~1.9) indicate that the dominant current transport mechanism is the recombination current in the space charge region. From the value of sheet resistance

obtained (~15kΩ/□) we find a resistivity of about 0.38Ω·cm for our high temperature implanted P^+ layer, and as analysed in section 3.3.2 this leads to a substitutional activation ratio of about 95%.

Table 3.10 Main electrical parameters of PN diodes and TLM structures after RTA at different temperatures extracted from *I-V* measurements.

	PN diodes				***TLM structures***	
RTA Temperature	**V_F @100A/cm^2 [V]**	**Ideality factor *n***	**R_{on}@100A/cm^2 [mW·cm^2]**	**R_{on}@1kA/cm^2 [mW·cm^2]**	**r_C [W·cm^2]**	**R_{SH} [kW/□]**
as-deposited	4.50	2.0	5.6	2.3	---	---
350ºC	4.05	1.9	4.5	1.8	---	---
500ºC	3.25	1.9	2.5	1.0	$4\cdot10^{-5}$	15.0
700ºC	3.00	1.8	2.0	0.5	$1\cdot10^{-5}$	15.5
900ºC	3.20	1.8	2.2	0.8	$3\cdot10^{-5}$	15.6

The temperature stability of the ohmic contact was studied by a temperature dependence test of the contact resistivity. The test was carried out in air from room temperature to 290ºC. The variation of the contact resistivity with temperature is presented in Fig. 3.25. The results show a decrease of the contact resistivity up to an operating temperature of 250ºC, from which it remains constant. After the test was completed and the sample was cooled down the contact resistivity was measured again at 25ºC and the value obtained did not differ from the value extracted before the test, thus showing an excellent thermal stability.

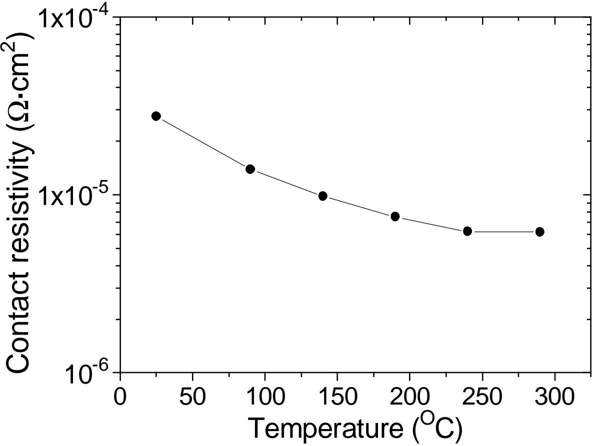


Figure 3.25 Dependence of contact resistivity on operating temperature.

The dependence of the contact resistivity on the temperature is a characteristic for contacts formed on relatively low doped semiconductors when a thermionic emission is the predominant current transport mechanism. In the thermionic emission regime, the contact resistivity is given by [143]:

$$r_C = \frac{k}{qA^{*}T} exp\left(\frac{q\Phi_B}{kT}\right) \tag{3.13}$$

where k is the Boltzmann constant, q is the electron charge, T is the temperature, A^* is the Richardson constant, and F_B is a height of potential barrier between the contact and semiconductor. The fitting of the experimental results with equation (3.13) as it is shown in Fig. 3.26 provides the potential barrier height F_B=0.058eV.

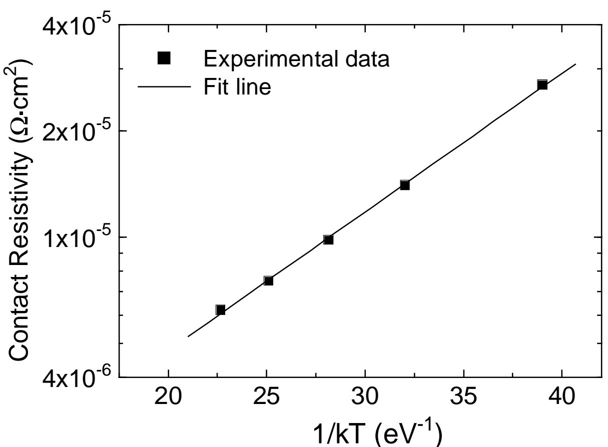


Figure 3.26 Contact resistivity dependence on the reciprocal temperature value.

3.4.2 W/Ti and W/Al/Ti multilayer contacts

Thermally stable metallic contacts to SiC are of considerable interest to those involved in high-temperature semiconductor device fabrication. For devices to operate reliably at elevated temperatures, the metal contacts must be thermodynamically stable. Elevated temperatures tend to drive chemical reactions and to create new compounds at the metal–semiconductor interface. Significant changes in the transport characteristics and physical characteristics can occur due to the new compounds formed. Reactions of the metal with the substrate not only consume substrate material, but also can additionally nullify the surface preparations of previous processing steps. Finding metals or metallic compounds which are thermodynamically stable and do not react with the substrate SiC over a desired temperature range of both device processing and operation can thus narrow the search for a Schottky barrier or ohmic contact with suitable mechanical and electrical properties. In particular, tungsten (W) has been studied by several authors because of its current use in Si technology and promise to SiC [152,153]. However, because of the refractory properties of W it is attractive for SiC processing but at the same time its use is associated with some complications, like adhesion problems during sputter deposition. To overcome this problem we have investigated W based contacts with an interlayer metal with good adhesion properties on SiC surface. For this purpose both Ti and Al/Ti metallic layers have been used.

Thus, in the next sections it is reported the electrical characterization of W/Ti and W/Al/Ti contacts on our 4H-SiC aluminum implanted samples for both Schottky and ohmic purposes after rapid thermal anneals at different temperatures.

- W/Ti contact was investigated in sample CQ4 (AD-0602-02 CREE´s wafer). After contact opening, Ti and W layers were sequentially deposited by sputtering and patterned by wet etching to define the circular diodes. The thickness of the Ti and of the W layers was in the range 25-35 and 90-110nm, respectively
- W/Al/Ti contact was investigated in sample S2 (B-8141-13 Sterling´s wafer). After contact opening, Ti, Al and W layers were sequentially deposited by sputtering and patterned by wet etching to define the circular diodes. The thickness of the Ti , Al and of the W layers was in the range 45-55, 190-210, and 90-110nm, respectively.

Both Schottky and PiN diodes were processed on the same samples to fabricate Schottky contacts on *n*-type epilayer and ohmic contacts on implanted p^+-type regions, respectively. In order to analyse the influence of the RTA contact anneals on the electrical characteristics of both Schottky and PiN diodes, several sequential thermal processes were performed at different temperatures, up to 1025ºC for 3min. The electrical characterization of the contacts under the different thermal anneals was carried out by measuring the current-voltage (*I*-*V*) characteristics of diodes at room temperature and by extracting the contact resistivity value from TLM structures.

3.4.2.1 Schottky contact

Figure 3.27 and Figure 3.28 show the forward current-voltage characteristics at room temperature of the Schottky diodes after contact RTA for 3min at different temperatures for both W/Ti and W/Al/Ti contacts, respectively. Characteristics parameters such as forward voltage drop at 100A/cm^2 (V_F), Schottky barrier height (Φ_B), ideality factor n and on-resistance (R_{on}) were determined by *I*-*V* analysis following the thermionic-emission theory [143] and are summarised in Table 3.11.

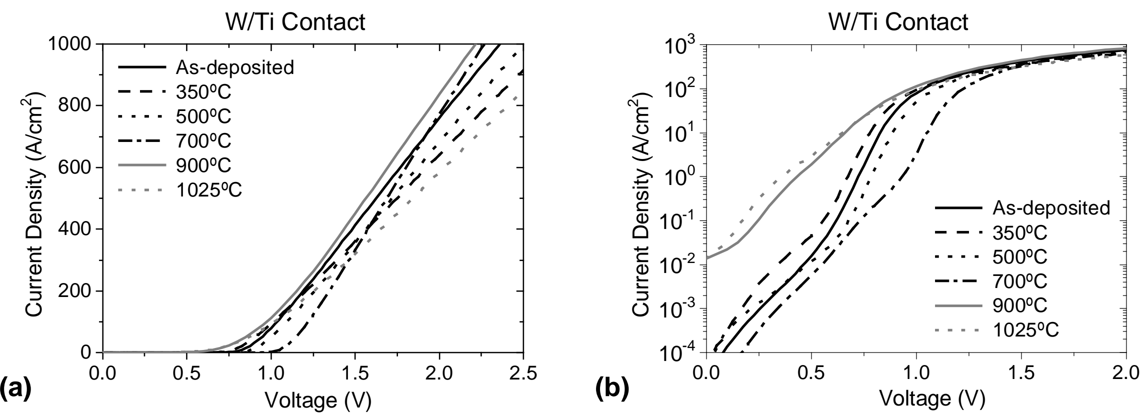


Figure 3.27 J-V characteristics of Schottky diodes with W/Ti contact. (a) Linear scale, (b) semilog scale.

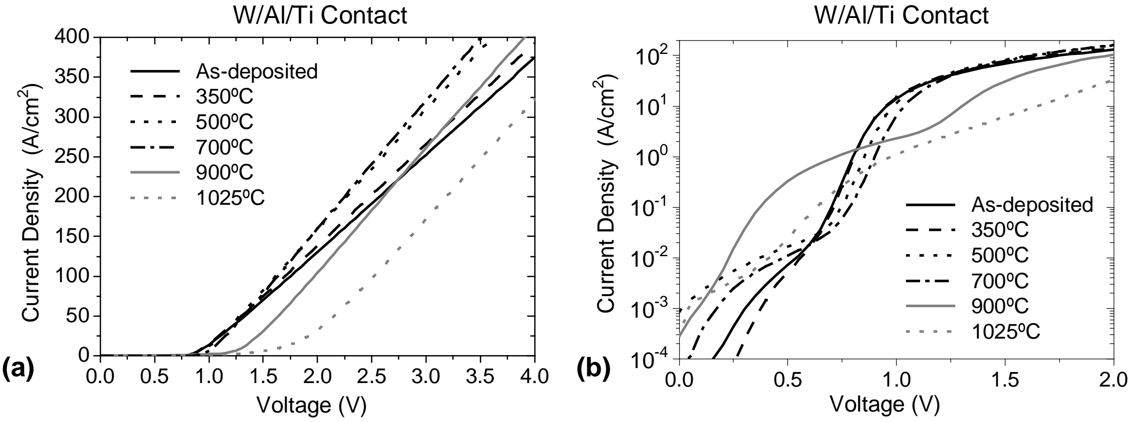


Figure 3.28 J-V characteristics of Schottky diodes with W/Al/Ti contact. (a) Linear scale, (b) semilog scale.

Table 3.11 Main electrical parameters of Schottky diodes with W/Ti and W/Al/Ti contacts extracted from I-V characteristics measured after RTA for 3min at different temperatures.

	RTA Temperature	**V_F @100A/cm^2 [V]**	**F_B [eV]**	**Ideality factor *n***	**R_{on} [mW·cm^2]**
W/Ti contact on 1.7kV wafer	as-deposited	1.03	0.85	1.75	1.4
	350ºC	1.01	0.81	1.72	1.8
	500ºC	1.10	0.88	1.70	1.5
	700ºC	1.22	0.92	1.90	1.2
	900ºC	0.98	---	---	1.4
	1025ºC	1.02	---	---	1.7
W/Al/Ti contact on 2.5kV wafer	as-deposited	1.75	0.88	1.70	8.2
	350ºC	1.70	0.89	1.66	7.8
	500ºC	1.63	0.91	1.77	6.6
	700ºC	1.62	0.93	1.86	6.3
	900ºC	1.98	---	---	6.4
	1025ºC	2.55	---	---	6.7

As it can be observed in Fig.3.27 and Fig 3.28, both contacts are degraded after the 900ºC RTA showing semilog I-V curves which could not be fitted by predicted thermionic emission theory curve and loosing the reverse blocking capabilities. Thus, Schottky barrier heights (Φ_B) and ideality factors (*n*) have not been extracted after the 900ºC RTA for both contact metallisations.

An interesting point observed in results from sample CQ4 measurements is that the extracted on-resistance values are lower than those extracted from samples CQ3 and CQ2 measurements (with Ni/Ti contact, see section 3.4.1.1), being all these samples from the same wafer. On-resistance values from sample CQ4 are very close to the theoretical value of the epilayer configuration (1mΩ·cm^2). Thus, it could be concluded that the metal contact plays an important role in determining the series resistance of the Schottky diode.

Moreover, the reverse characteristics are also affected by the Schottky metal layer. Figure 3.29 shows the reverse I-V characteristics of Schottky diodes from sample CQ4, showing a reduction in reverse leakage current and an increase in breakdown voltage associated with the increase in Schottky barrier height after the different RTA temperatures performed. This behaviour was also observed in Schottky diodes from sample CQ3 (see section 3.4.1.1). However, the reverse leakage current level is observed to be lower in diodes from sample CQ4 than from CQ3 sample, although the Schottky barrier height is higher in the later for the higher RTA temperatures. This result shows that further analysis should be carried out in order to clarify the origin of the reverse leakage current in these Schottky diodes.

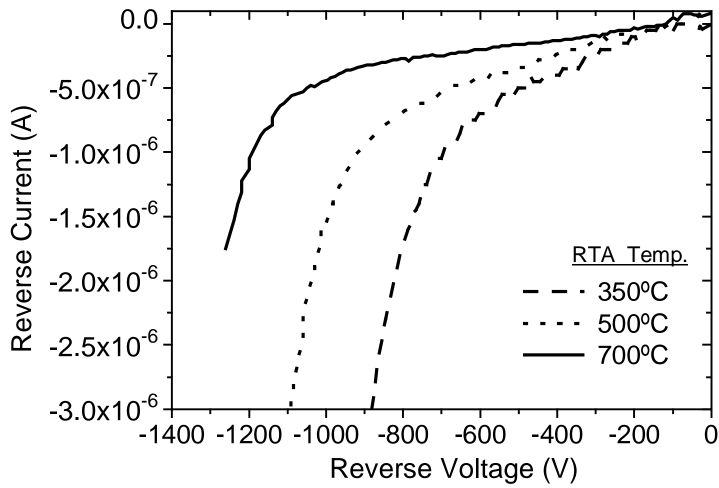


Figure 3.29 Reverse I-V characteristics of Schottky diodes after RTA at different temperatures. The curves shown correspond to a Schottky diode with single JTE structure.

3.4.2.2 Ohmic contact

Figure 3.30a and Figure 3.31a show the forward current-voltage characteristics at room temperature of the bipolar PN diodes after the different RTA temperatures for W/Ti and W/Al/Ti contacts, respectively. The contact resistivity (ρ_C) of as-deposited and annealed contacts was extracted from linear transmission line model (TLM) together with the sheet resistance (R_{SH}) of the aluminum implanted P^+ region (2×10^{19}cm^{-3} doping concentration). Characteristics I-V curves from TLM measurements between two pads (d=10μm) after each RTA process are shown in Fig. 3.30b and Fig 3.31b for the two contacts investigated. The extracted values of the main electrical parameters of diodes and the contact characterisation as a function of the anneal temperature are summarised in Table 3.12.

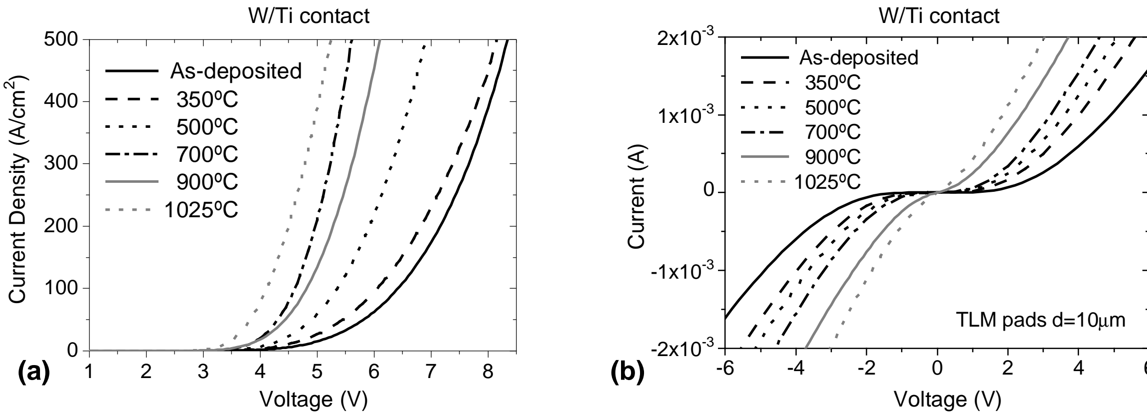


Figure 3.30 (a) Forward *J-V* characteristics of PN diodes after RTA of the W/Ti contact at different temperatures. (b) The effect of RTA temperature on the TLM *I-V* characteristics measured between two pads 10μm spaced.

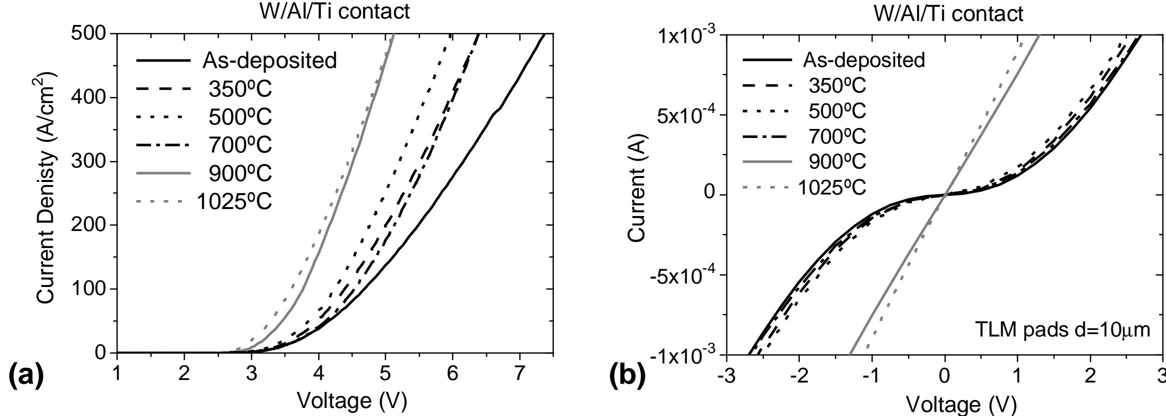


Figure 3.31 (a) Forward *J-V* characteristics of PN diodes after RTA of the W/Al/Ti contact at different temperatures. (b) The effect of RTA temperature on the TLM *I-V* characteristics measured between two pads 10μm spaced.

Table 3.12 Main electrical parameters of PN diodes and TLM structures after RTA at different temperatures extracted from *I-V* measurements for the two contacts analysed.

		PN diodes				***TLM structures***	
	RTA Temperature	**V_F @100A/cm^2 [V]**	**Ideality factor *n***	**R_{on}@100A/cm^2 [mW·cm^2]**	**R_{on}@1kA/cm^2 [mW·cm^2]**	**rc [W·cm^2]**	**R_{SH} [kW/□]**
W/Ti	as-deposited	6.42	2.5	9.8	2.1	---	---
	350ºC	6.10	2.1	9.5	2.0	---	---
	500ºC	5.35	2.0	8.9	1.8	---	---
	700ºC	4.62	1.9	5.1	1.4	---	---
	900ºC	4.82	1.8	6.0	1.5	$4.2 \cdot 10^{-3}$	15.8
	1025ºC	4.12	1.9	5.2	1.7	$1.2 \cdot 10^{-3}$	16.0
W/Al/Ti	as-deposited	4.70	3.2	9.1	5.0	---	---
	350ºC	4.40	2.6	7.1	3.5	---	---
	500ºC	4.25	2.2	6.6	3.6	---	---
	700ºC	4.52	1.9	6.8	2.8	---	---
	900ºC	3.77	2.1	5.2	2.6	$9.5 \cdot 10^{-4}$	15.4
	1025ºC	3.60	1.9	5.1	2.5	$3.0 \cdot 10^{-4}$	15.6

As observed from Fig. 3.30, Fig 3.31 and results in Table 3.12, the W/Al/Ti shows better ohmic characteristics than the W/Ti contact, achieving the lowest contact resistivity value of $3\times10^{-4}\Omega cm^2$ after the RTA at 1025ºC. However, both contacts show poor ohmic characteristics in comparison to the Ni/Ti contact reported in section 3.4.1.2. This poor ohmic behaviour cannot be ascribed to a lower p-type doping activation of the implanted emitter region, because the obtained sheet resistances in both samples (CQ4 and S2) are in the same order of values with those obtained on samples with the Ni/Ti contact. These bad ohmic performance is translated in greater on state voltage drops at $100A/cm^2$ and higher on-resistances of the bipolar diodes. Nevertheless, good conductivity modulation of the drift layer is achieved, as proved by the on-resistance decrease at high current densities.

Although there are no previous studies on reactions between W/Ti multilayers with SiC some likely reactions and reactions mechanisms can be anticipated from previous studies on Si [154, 155]. These studies suggest that films composed of two different refractory metals, both multiple layers or alloys, behave like a single metal film in which no reaction or interdiffusion between the two metals occurs for temperatures below 800ºC. In these films Si diffuses and reacts similarly to the case of single metal silicidation of Ti and W in which Si is known to be the diffusing specie. In samples annealed at temperatures higher than 900ºC both metals appear to be reacted with silicon and a certain degree of intermixing between the reacted layers is observed. However, in order to clarify the reactions mechanisms of our two formed contacts on 4H-SiC, further investigation (such as Auger sputtering profiling and XRD characterisation) is needed in order to obtain a qualitative understanding of the chemical reactions that occurs.

3.5 Summary

In this chapter we have presented and analysed the main technological processes involved in the fabrication of our diodes. Firstly, it has been shown the high-quality starting material together with the different samples processed during this thesis.

High activation ratios (90-100%) of the aluminum impurities implanted at high temperatures have been achieved after high temperature activation anneals performed at 1650ºC-1700ºC for 30-45min. Improved surface morphology after high temperature activation annealing has been demonstrated when N_2 is used as the ambient gas.

Electrical and structural characterisation of Ni/Ti bi-layer contacts on 4H-SiC with different thermal anneals for both Schottky and ohmic purposes have been reported in this chapter. It has been proved that a high temperature anneal (700ºC-900ºC) of this bi-layer contact scheme is the best choice in order to get: i) a performant ohmic contact on the PN diodes with a very low specific contact resistance value ($1\times10^{-5}\Omega\cdot cm^2$), ii) a rectifying

Schottky contact not severely degraded and exhibiting low leakage current level; and iii) a high increase in the breakdown voltage of the Schottky diodes approaching to the maximum theoretical value. It has been shown that the formation of nickel silicides at these high annealing temperatures could be the origin of the leakage current reduction in Schottky diodes and of the contact ohmic transition in p^+-type doped regions of bipolar diodes. Longer contact annealing time have no effects on contact resistivity. The high temperature implantation of aluminum impurities and the high substitutional activation ratio achieved has contributed to the good ohmic performance of PN diodes and it has allowed to show the high efficiency of our edge termination. These results may be useful to simplify the fabrication procedure of devices where the formation of both ohmic and Schottky contacts are needed together.

Investigations have been performed on W/Ti and W/Al/Ti contacts. They have shown good Schottky rectifier characteristics with low Schottky barrier shift for RTA temperatures up to 900ºC, where their rectifier properties were severely degraded. However, poor ohmic characteristics were achieved for both contacts even after an RTA at 1025ºC.

CHAPTER

Edge Termination Results and Technology Considerations

This chapter covers the results on edge termination efficiency of the different structures implemented on our 4H-SiC power diodes. A detailed analysis of the breakdown behaviour of each termination structure is carried out together with a statistical report. Correlation between processes performed on each sample and breakdown results are also investigated. Finally, we also look to the impact of a field plate associated to the JTE as well as the surface passivation influence in the reverse bias mode. The superior performance in terms of efficiency and reliability of the novel termination structure is shown with respect to the other studied terminations.

4.1 Reverse Breakdown Measurements

High voltage reverse measurements performed on diodes analysed during this thesis have been carried out in on-wafer devices and in air ambient with a Tektronix 370 curve tracer. The reverse leakage current detection limit of the curve tracer is 20nA. Two probe needles were used to contact the top metallization of the devices, while the backside was connected through the probe station chuck. In this Kelvin setup, voltage drops in the cables, along the probe needles, and the contact resistance between the probe needle and the sample do not influence the measurements. Figure 4.1 shows a photo of the lab equipment setup for high voltage reverse measurements.

All instruments were connected to a personal computer using the IEEE488 GPIB bus. Software written in *National Instruments´s* control language, *LabView,* was used to collect the measured data.

For high temperature I-V characterisation, measurements were carried out in a probe station equipped with an electric heater powered by a temperature controller PMA KS40-1. The sample temperature can be regulated from room temperature up to 350ºC.

Figure 4.1 Instrumental setup for high-voltage reverse measurements at the power lab.

4.2 Edge Termination Results

In the next sections the blocking efficiency of the designed and optimised edge termination structures shown in Chapter 2 will be reported. The results reported correspond to diodes fabricated on samples from CREE´s wafer AD-0602-02, as the high density of defects present in samples from Sterling´s wafer B-8141-13 invalidates them for reliable breakdown analysis. It must be also pointed out here that all the selective doping regions of the reported diodes in the next sections are formed by multiple energy Al^+ implantations, as explained in Chapter 3 section 3.2.1.

Therefore, as a reference data it should be remembered that the ideal 1D plane-parallel breakdown voltage of diodes from wafer AD-0602-02 is 1900V. Furthermore, as an extra data information it must be pointed out that diodes without any edge termination structure showed an experimental well defined sharp breakdown at 350V ± 50V on all processed samples.

4.2.1 Single Zone JTE

As described in Chapter 2, the single junction termination extension (JTE) structure was optimised with numerical 2D simulations and implemented in the photolitographic mask set design for device fabrication. The main subjects of investigation are the doping profile (dose and depth) and the extension junction length, which are the main parameters affecting the blocking voltage. Therefore, diodes with 3 different JTE lengths were analysed and two different Al^+ implantation profiles were performed on two different samples from the same wafer (see Chapter 3 section 3.2.1). As the ideal charge in JTE was accurately obtained from simulations, the doping profiles kept the same implanted dose but were defined with different implantation energies, thus changing the depth of the Al doping profile. Figure 4.2 shows an optical image of the fabricated diodes with the three different lengths of the JTE.

Figure 4.2 Optical photo of the fabricated diodes with different lengths of the JTE

Table 4.1 reports de breakdown results on diodes with the three different JTE lengths and two different doping profiles. For the statistical report, “bad” diodes (i.e. with breakdown voltages lower than 800V) were not taken into account. The efficiency reported is calculated by dividing the average breakdown voltage obtained experimentally by the theoretical 1D plane-parallel breakdown voltage (1900V) using Hatakeyama *et. al.* [85] impact ionisation coefficients.

Table 4.1 Single JTE length and depth influence on breakdown voltages.

JTE doping profile	JTE length	Maximum Breakdown Voltage	Average Breakdown Voltage	Standard deviation	Efficiency
Dose $1.14\times10^{13}cm^{-2}$ Depth ~ 0.9μm	35μm	1500V	1350V	100V	71%
	65μm	1620V	1525V	75V	80%
	125μm	1690V	1575V	75V	83%
Dose $1.12\times10^{13}cm^{-2}$ Depth ~ 0.6μm	35μm	1400V	1300V	100V	68%
	65μm	1590V	1500V	100V	79%
	125μm	1680V	1550V	100V	81%

As it can be observed from Table 4.1, the doping profile depth shows a little influence on the breakdown voltages although a bit higher blocking voltages are obtained for the deeper profile as a general trend. The results concerning the influence of the JTE length on the breakdown values clearly corroborate the simulation results, showing that under punch-through conditions the JTE length must be extended laterally to about six times the epilayer thickness to fully relax the surface electric field and thus getting the maximum breakdown voltage. Figure 4.3 shows a characteristic reverse I-V curve at room temperature for the single JTE structure with the three different JTE lengths, showing a sharp and well defined breakdown.

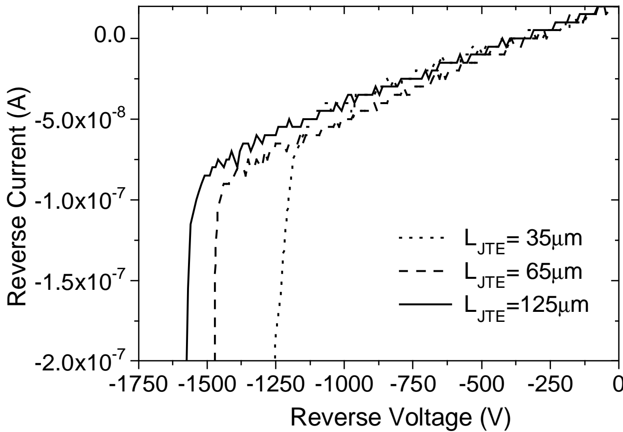


Figure 4.3 Characteristic reverse I-V curves at room temperature of diodes with single JTE structure and different JTE length.

The measured leakage current was below 1×10^{-7}A (which corresponds to reverse leakage current densities <3×10^{-4}A/cm^2) up to the onset of breakdown. The breakdown characteristics were not catastrophic in most of the tested devices, with the device surviving after the applied voltage was reduced. However, the increase of reverse current after the breakdown voltage was critical for the breakdown stability of diodes with single JTE, as destructive failure of the device occurred for reverse currents higher than 10µA due to electric arching in air from the anode metal edge to the unpassivated scribing line, as shown in Fig. 4.4. Moreover, the avalanche luminescence was not visible in diodes with single JTE nor at the end of the JTE region or at the p^+ junction edge (contrary to the bright avalanche luminescence observed in diodes with other termination structures, as it will be shown later on). No visible luminescence indicates that there is almost no electric field crowding at the p^+ junction edge or at the end of the JTE region even when breakdown occurs, where the electric field strength estimated is close to the theoretical breakdown electric field (2.23 MV/cm).

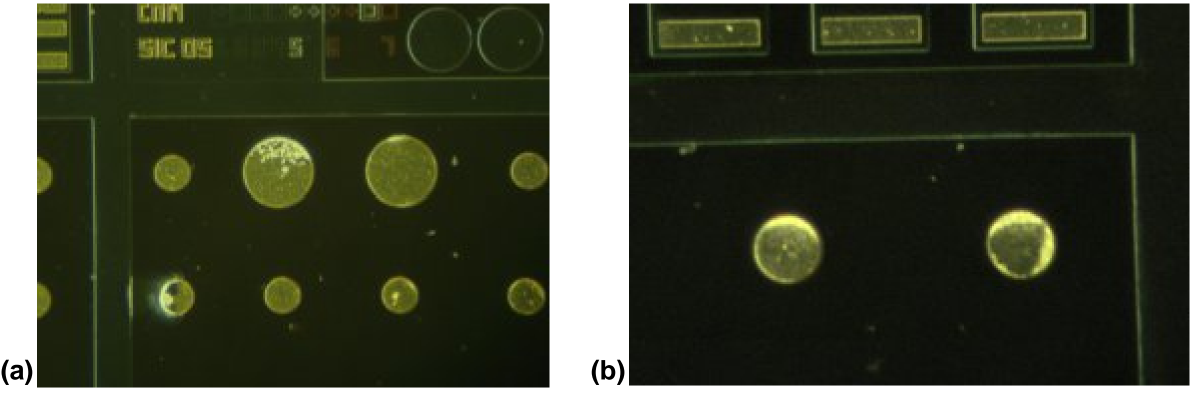


Figure 4.4 Optical micrographs of diodes showing the catastrophic failure due to surface flashover between the anode metal edge and the scribing line.(a) Large area diodes and a small diode with shorter double JTE, (b) small diodes with single JTE.

The so far reported results correspond to small area diodes (200µm diameter). However, larger area diodes (400µm diameter) were also fabricated with a single JTE of 65µm length, as shown in the photolithographic mask layout in Chapter 2 section 2.4. The average breakdown voltage on large area diodes was of 1200V, achieving a maximum breakdown voltage value of 1350V. Moreover, the yield of "good working" diodes was significantly lower for large area diodes. These results are clearly worst than those obtained on smaller area diodes with the same JTE length, thus showing the importance of the device area on blocking capabilities due to a higher amount of material defects present on large area devices. However, no clear differences were observed in reverse I-V characteristics between large and small diodes (see Figure 4.5) thus suggesting a bulk generation current instead of a perimeter related leakage current which is commonly observed in mesa diodes [156,157].

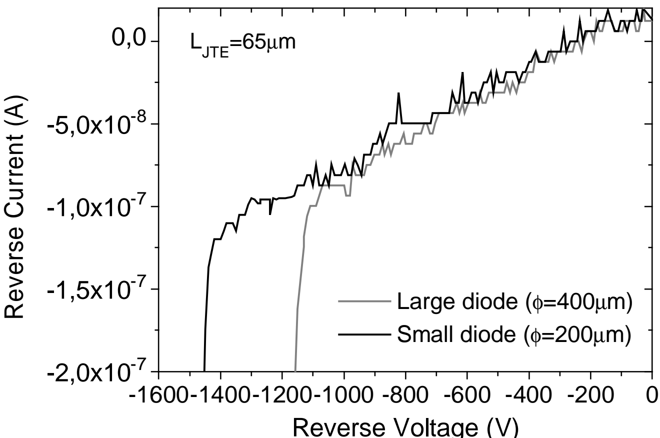


Figure 4.5 Reverse I-V characteristics at room temperature of diodes with single JTE structure of 65µm length and two different areas.

Moreover, large area diodes show a higher catastrophic failure yield due to a shorter distance between the metal edge and the scribing line, which enhances the sparking in air that destroys the anode metal, as can be clearly observed in Fig 4.4a.

4.2.2 Double Zone JTE

As in the single JTE case, the double zone JTE has been investigated in terms of the length of each JTE zone. Moreover, two different configurations have been considered: a side-by-side design and a JTE1 embedded into the JTE2 region (see Chapter 2 section 3.2.2). In the case of the side-by-side configuration there is an overlap of five microns between the two zones. Figure 4.6 shows an optical picture of the fabricated diode with double JTE in embedded configuration.

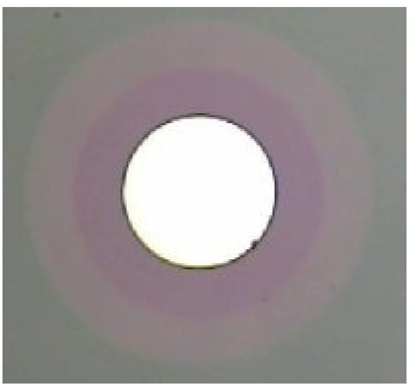


Figure 4.6 Optical image of a fabricated diode with double JTE in embedded configuration (L_{JTE1}=65µm, L_{JTE2}=125µm). The two different concentric implanted zones can be clearly distinguished.

Table 4.2 shows the breakdown results for both configurations and the different lengths of the two JTE zones. As no great differences in breakdown voltages are observed between devices with different doping profile in JTE2, the results from samples with different JTE2 implantation profile are grouped and reported together in Table 4.2.

Table 4.2 Breakdown voltages of different double zone JTE structures.

Zone config.	L_{JTE1}	L_{JTE2}	Maximum Breakdown Voltage	Average Breakdown Voltage	Standard deviation	Efficiency
Side by side	25µm	25µm	1500V	1400V	100V	73%
	45µm	45µm	1610V	1550V	50V	81%
	65µm	65µm	1690V	1650V	50V	87%
Embedded	25µm	45µm	1520V	1400V	100V	73%
	45µm	85µm	1640V	1575V	50V	82%
	65µm	125µm	1720V	1650V	50V	87%

As it can be deduced from results shown in Table 4.2, there is no remarkable difference in the blocking capability between the two configurations. Although it seems that there is not great advantage in the blocking capability with respect the single JTE case, regarding the production yield, the double JTE structure shows higher efficiency and higher breakdown voltage. Figure 4.7 shows the characteristics reverse I-V curves of diodes with double JTE structure in embedded configuration.

The measured reverse leakage current level is the same as in the single JTE case, i.e reverse current densities $<3\times10^{-4}$A/cm^2 up to the onset of breakdown and sharp avalanche breakdown is observed in the I-V characteristics. Also as in the single JTE case, the breakdown voltage increases with increasing total JTE length in the two different double zone configurations. Besides, it must be pointed out that with our highest total JTE length (125µm)

we are near to reach the saturation value of the breakdown voltage. Thus, higher JTE lengths would lead to a very low increase of the blocking voltage and a high increase of the "wasted" area on edge termination. Since the edge termination area of the device does not contribute to current conduction, it is highly desirable to minimise it and thus reduce the effective on-state resistance. At the same time, the reduction of the termination area also has a direct impact on increasing the fabrication yield.

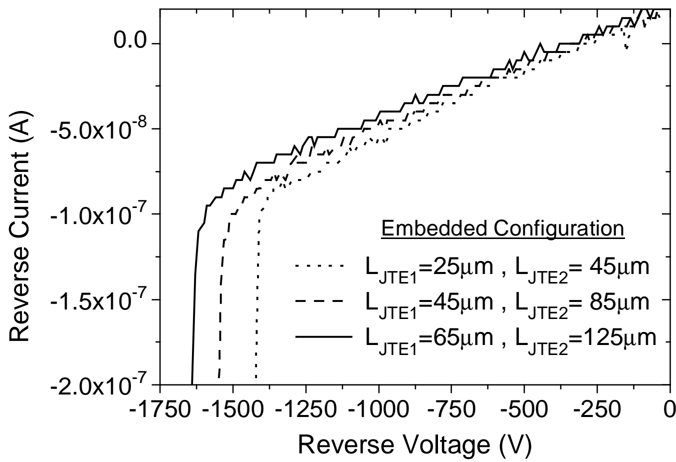


Figure 4.7 Characteristics reverse I-V curve for diodes with double JTE structure in embedded configuration and with different lengths.

To investigate the avalanche behaviour, luminescence was observed at breakdown with high reverse current. As opposed to a tunnelling process, avalanche multiplication generates a high density of electron-hole pairs, a part of which yields luminescence through radiative recombination. Bright luminescence was observed at the edge of the first JTE zone in both embedded and side-by-side configurations (see Figs. 4.8 and 4.9), meaning that the electric field crowding at the end of the first JTE zone causes significant impact ionisation. This behaviour leads to the conclusion that the implanted dose in the first JTE zone is a little bit higher than the ideal one, where the maximum avalanche rate would be equally shared between the emitter-JTE1, JTE1-JTE2 junctions and the end of the JTE2. Nevertheless, the high breakdown voltages achieved in both configurations of the double JTE structure are a proof of the good optimisation of these terminations and the high efficiency in spreading equipotential lines throughout the two JTE zones. Moreover, diodes with double JTE structure as an edge termination showed higher reverse stability after the breakdown voltage than diodes with single JTE, as they were able to sustain higher reverse current without catastrophic failure. This is due to the fact that the maximum electric field at breakdown is reached at the end of the first JTE region which alleviates the main junction edge from suffering the high electric field that leads to an electrical discharge through air.

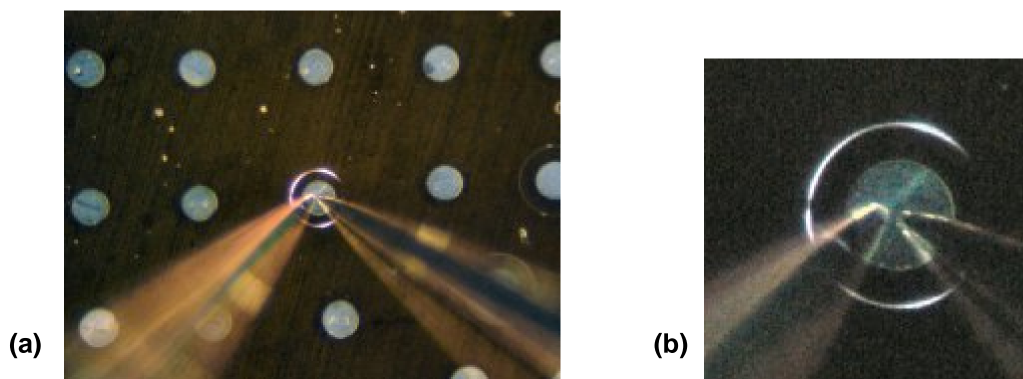


Figure 4.8 Electroluminiscence at breakdown of a diode with double JTE structure in side-by-side configuration (L_{JTE1}=65μm, L_{JTE2}=65μm). The bright luminescence is observed at the end of the first JTE zone. (a) general view (b) zoom approach.

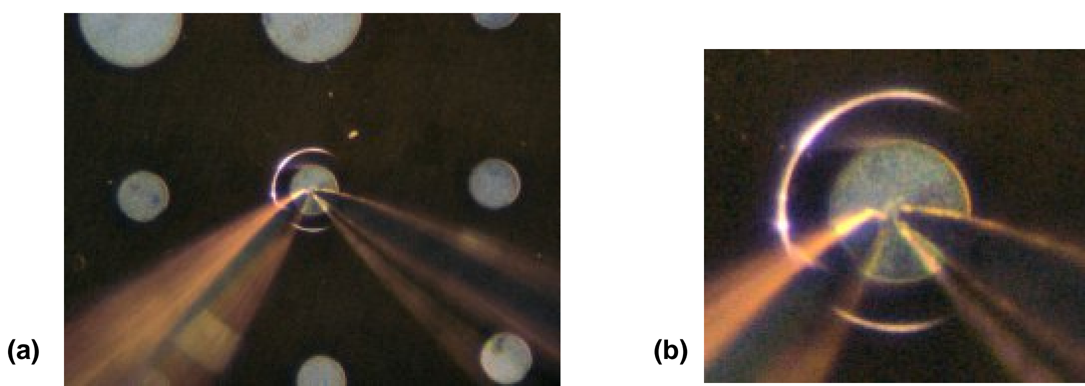


Figure 4.9 Electroluminiscence at breakdown of a diode with double JTE structure in embedded configuration (L_{JTE1}=65μm, L_{JTE2}=125μm). The bright luminescence is observed at the end of the first JTE zone. (a) general view (b) zoom approach.

Simulations were performed to confirm the above explained behaviour. Figure 4.10a shows the impact ionisation rate distribution on a double JTE structure of side-by-side configuration (65μm length each zone). It can be clearly seen that the avalanche breakdown takes place at the end of the first JTE zone, although the second JTE effectively spreads the equipotential lines, as demonstrated from the potential distribution shown in Fig. 4.10b.

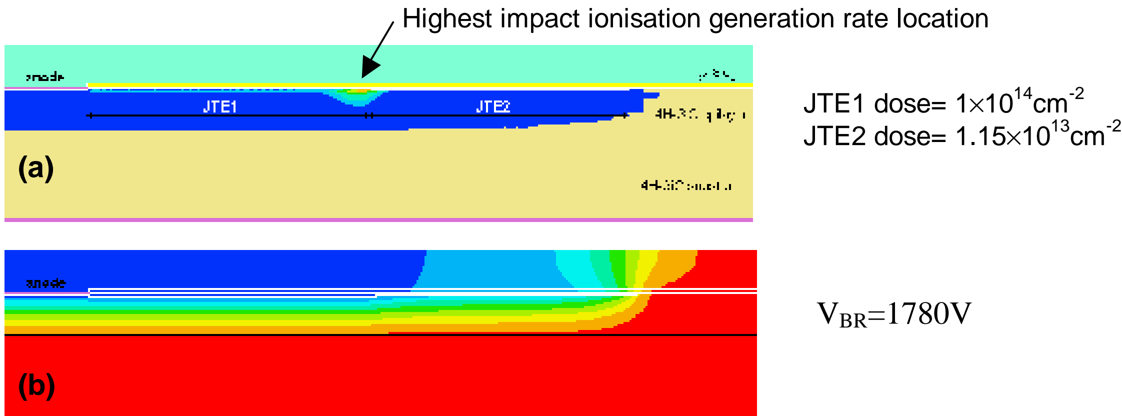


Figure 4.10 (a) Impact ionisation distribution at breakdown, and (b) equipotential lines of a double JTE structure in a side-by side configuration.

In conclusion, we have proved that is better to introduce doses higher than the ideal one in JTE1 zone in order to avoid the catastrophic breakdown at the metal junction edge without compromising the blocking capabilities of the double zone JTE structure.

4.2.3 Multiple Floating Guard Rings

A multiple floating guard rings (FGR) termination structure has been investigated. After the optimisation process shown in Chapter 2 section 2.3.3, five floating guard rings 8μm wide and 3μm spaced were implemented as a diode termination structure in the lithographic mask set for fabrication. In addition, to analyse the influence of the p-type doping concentration of the guard rings on their blocking capability, three different impurity doses were implanted leading to concentration levels of: $2\times10^{19}cm^{-3}$ (the same implantation profile as for the anode formation), $2\times10^{18}cm^{-3}$ (the same implantation as for the first JTE zone in the double JTE structure) and $2\times10^{17}m^{-3}$ (the same implantation profile as the for the single JTE). Figure 4.11 shows an optical photo of a diode with the multiple floating guard ring termination before the ion implantation process of the rings.

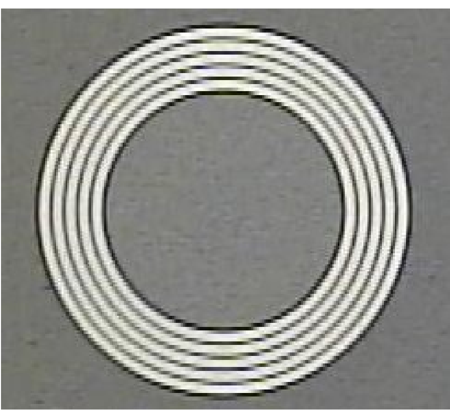


Figure 4.11 Optical micrograph of a diode with FGR termination before the implantation process of the rings. In this case, the rings will be implanted with the lowest p-type concentration ($2x10^{17}cm^{-3}$).

The breakdown voltage results obtained are summarised in Table 4.3. For the lowest p-type concentration the two different implantations profiles (see section 4.2.1) are considered.

Table 4.3 Breakdown voltages of multiple floating guard rings structures.

	p-type rings concentration	Maximum Breakdown Voltage	Average Breakdown Voltage	Standard deviation	Efficiency
	$2\times10^{19}cm^{-3}$	920V	800V	125V	42%
	$2\times10^{18}cm^{-3}$	1010V	900V	100V	47%
Depth ~ 0.9μm	$2\times10^{17}cm^{-3}$	1320V	1150V	100V	60%
Depth ~ 0.6μm	$2\times10^{17}cm^{-3}$	1200V	1050V	100V	55%

These results show an increasing efficiency when decreasing of the p-type ring´s concentration. This behaviour could probably be due to an inaccurate optimisation of the distance between rings, which leads to a JTE-like termination in the case of the lowest ring implanted dose and deeper rings. It must be pointed out that although Al^+ implanted atoms do not diffuse neither vertically nor laterally after the high temperature activation annealing process [158], a larger straggle of deeply-implanted and low doped regions enlarge the curvature at the edge of the pn junction thus reducing the distance between rings, which makes possible the depletion of the regions between rings giving rise to a JTE-like termination structure. This assumption is reinforced by the breakdown results on diodes with different profile implantation for the lowest FGR doping concentration, whose breakdown voltages difference agree well the general trend observed for diodes with single JTE structure concerning the depth of the implantation profile.

We have to note that the efficiency of the highest doped rings structure is only around 10% lower than that of earlier reported studies on FGR termination in 1.2kV SiC devices [91,105,159,160]. Thus, we can conclude that the floating guard rings structure is a less effective edge termination than the single or the double JTE, for silicon carbide devices, at least in this range of breakdown voltage. In Figure 4.12 shows the characteristics I-V curves of the diodes with FGR termination and different p-type rings concentration. As it can be clearly observed, a very sharp avalanche breakdown is obtained.

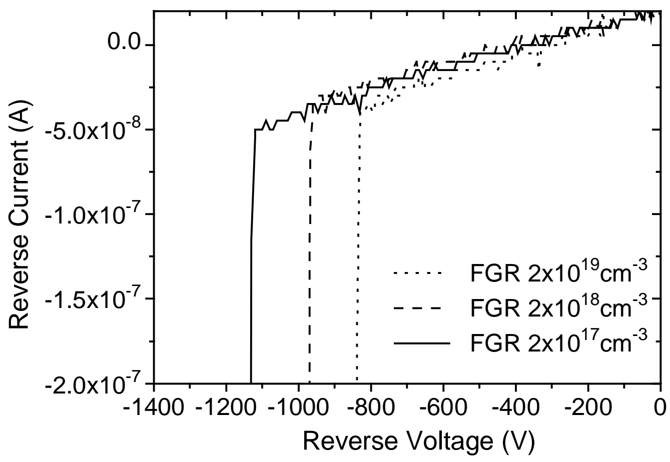


Figure 4.12 Reverse I-V curves at room temperature of diodes with the FGR termination and different ring´s p-type concentration.

Due to this sharp avalanche, luminescence was observed at breakdown with high reverse current. Figure 4.13 shows optical pictures of the avalanche luminescence on diodes with the three different ring´s concentration. The photos shown in Fig. 4.13 represent the typical luminescence avalanche breakdown behaviour observed on the three different FGR termination structures, as it was observed on various diodes with the same termination structure.

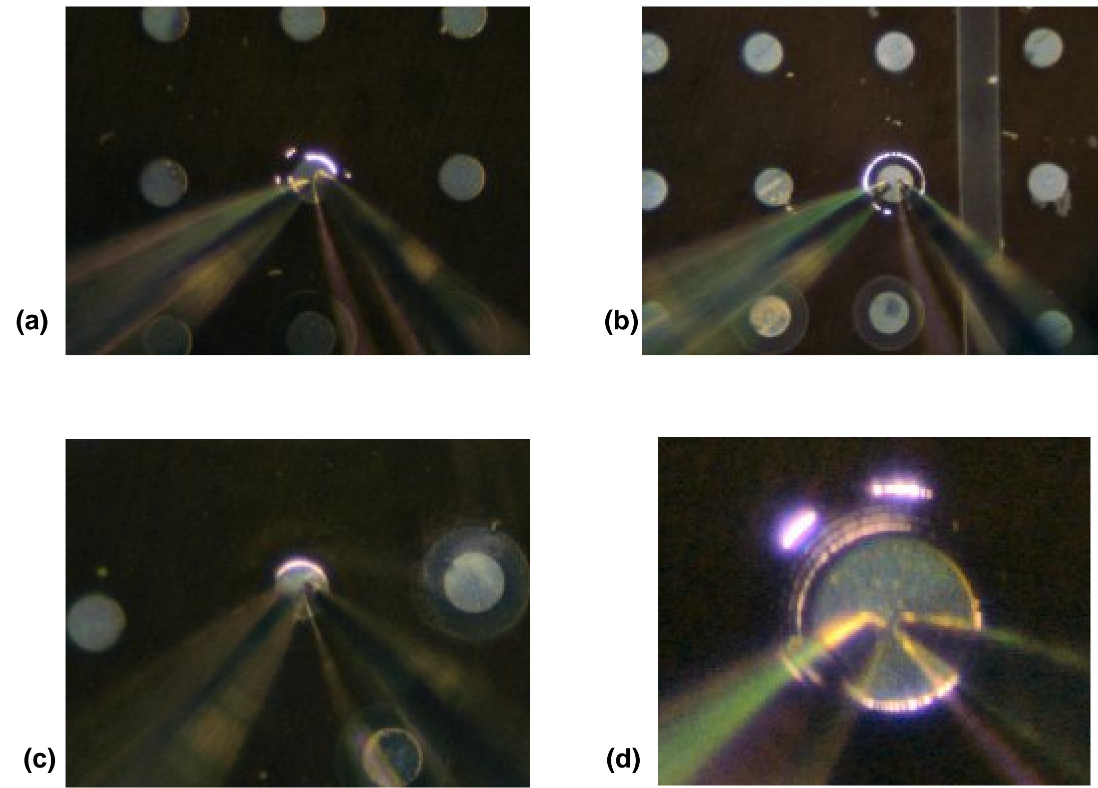


Figure 4.13 Optical pictures of the avalanche luminescence on diodes with FGR termination (a) FGR with P^+ (2×10^{19}cm^{-3}) concentration, (b) FGR with P (2×10^{18}cm^{-3}) concentration, (c) FGR with P^- (2×10^{17}cm^{-3}, 0.9μm depth) concentration, and (d) FGR with P (2×10^{18}cm^{-3}) showing the five FGR structure.

As it is seen from pictures in Fig 4.13, diodes with FGR termination structures with ring´s doping levels of 2×10^{19}cm^{-3} and 2×10^{18}cm^{-3} show an avalanche luminescence both at the emitter edge and at the end of the last floating guard ring (as clearly observed in Fig 4.13d, where the five FGR can be distinguished). On the contrary, diodes with FGR with 2×10^{17}cm^{-3} ring´s p-type concentration only showed the avalanche luminescence at the emitter edge (for both 0.6μm and 0.9μm implantation depths). Simulations were performed to analyse this different breakdown location on diodes with FGR of different p-type concentration. Figure 4.14 shows the impact ionisation distribution at breakdown for the five FGR termination with different ring´s p-type doping concentration. As it can be observed, the predicted breakdown location agrees with the experimental ones. Thus, FGR with highest (2×10^{19}cm^{-3}) and lowest (2×10^{17}cm^{-3}) p-type concentration show the highest impact ionisation rate at the emitter edge, although FGR with P^+ doping also exhibits high ionisation rate at the end of the last guard ring. Besides, FGR with P doping level (2×10^{18}cm^{-3}) clearly exhibits the highest impact ionisation rate at the end of the last guard ring.

The obtained breakdown voltages from simulations also agrees with the experimental trends (higher breakdown voltages with lower p-type concentration), although the simulated

obtained blocking values are greater than the experimental ones. The fact that diodes with FGR of lowest p-type concentration show higher breakdown voltages although the avalanche breakdown takes place at the emitter edge can be explained by a more effective spreading of the equipotential lines thus reducing in a great manner the electric field strength.

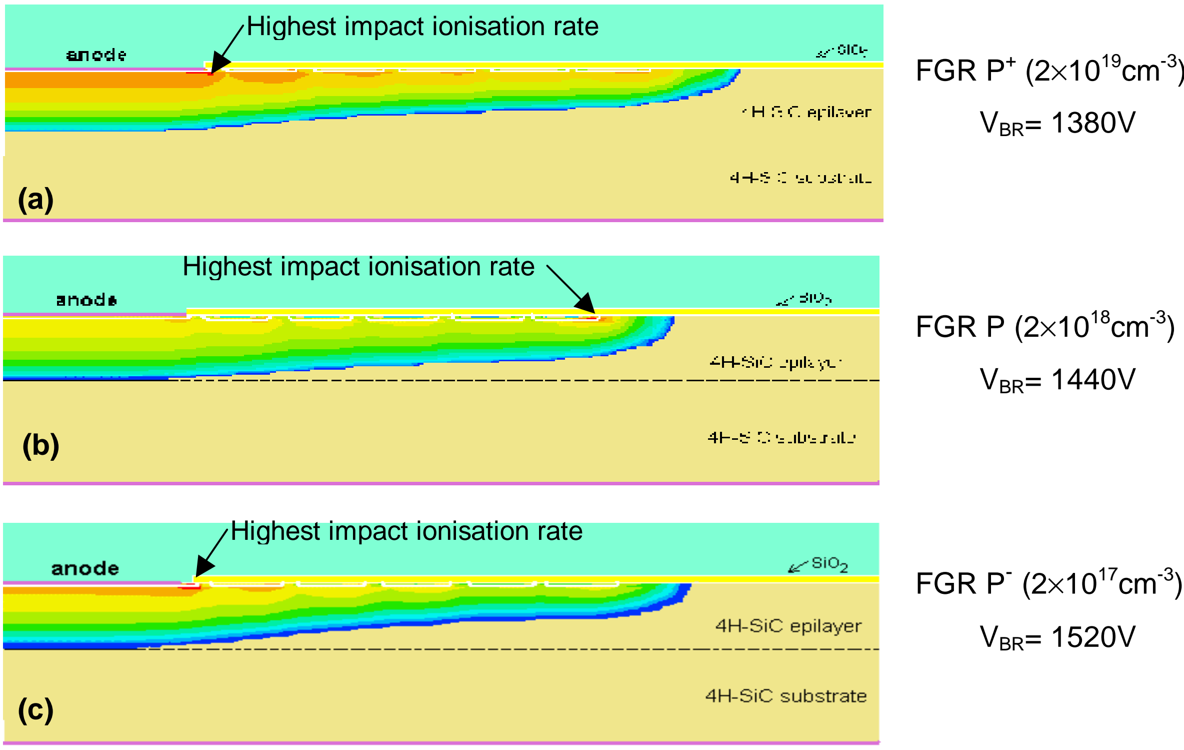


Figure 4.14 Impact ionisation distribution at breakdown of diodes with FGR termination.(a) $2\times10^{19}cm^{-3}$ ring´s doping concentration, (b) $2\times10^{18}cm^{-3}$ ring´s doping concentration, (c) $2\times10^{17}cm^{-3}$ ring´s doping concentration.

However, it must be pointed out that diodes with FGR termination with P concentration ($2\times10^{18}cm^{-3}$) showed some dispersion on the breakdown avalanche location. Most of them showed a clear uniform avalanche over the last ring (see Fig 4.13b), although some diodes also exhibited avalanche luminescence at the emitter edge and with lower intensity in the inner rings (see Fig. 4.13d).

4.2.4 Floating Guard Rings Assisted JTE

To wider the JTE range of the impurity concentration for obtaining high breakdown voltages we have proposed the "floating guard rings assisted JTE" structure (see Fig. 2.23). After the design and optimisation process carried out in Chapter 2 section 2.3.5, this structure was fabricated with five floating guard rings (s=3μm, w=8μm) of p^+ concentration inside a single JTE of 95μm length. Figure 4.15 shows optical pictures of a diode with this developed termination structure at two different stages of the fabrication process.

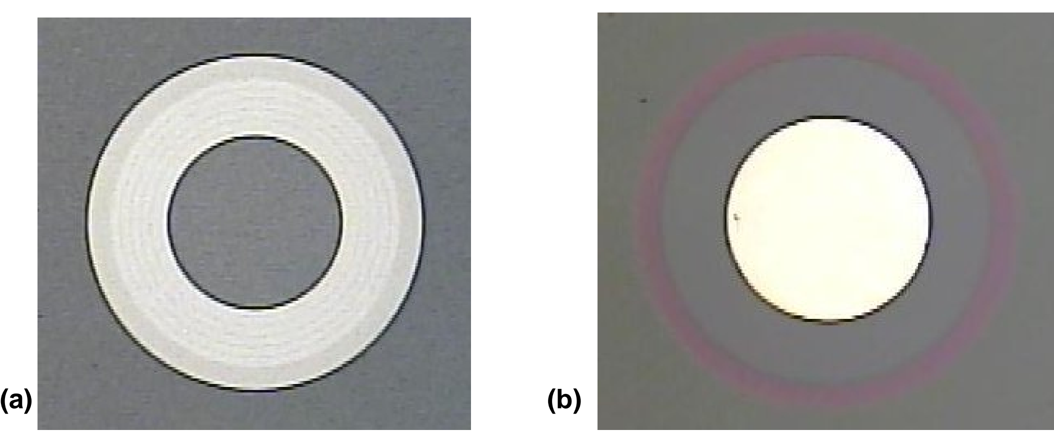


Figure 4.15 Optical micrographs of a diode with the developed "FGRs assisted JTE" structure. (a) before the JTE implantation, (b) after JTE implantation and metal deposition.

Table 4.4 shows the breakdown results on diodes with this termination structure. It must be remembered here that for the efficiency calculation the average breakdown voltage is used.

Table 4.4 Breakdown results on diodes with "FGRs assisted JTE" termination.

JTE impl. profile	Maximum Breakdown Voltage	Average Breakdown Voltage	Standard deviation	Efficiency
Depth ~ 0.9μm	1810V	1750V	75V	92%
Depth ~ 0.6μm	1760V	1700V	50V	90%

As shown in Table 4.4, the average breakdown voltage achieved with this termination structure is 1750V. This result represents over 92% of edge termination efficiency, which is attributed to a large extension of the impurity concentration range in the JTE layer, as pointed out in Chapter 2 section 2.3.5. Moreover, the effect of the inner guard rings on sustaining high breakdown voltages when the impurity concentration of the JTE layer is lower than the optimum one, alleviates the anode junction from suffering high electric fields, thus avoiding a catastrophic breakdown at the metal anode edge. This effect provides a higher stability of the high breakdown voltages achieved and makes this structure a robust termination. Figure 4.16 shows characteristics I-V curves of reverse breakdown on diodes with the new developed structure.

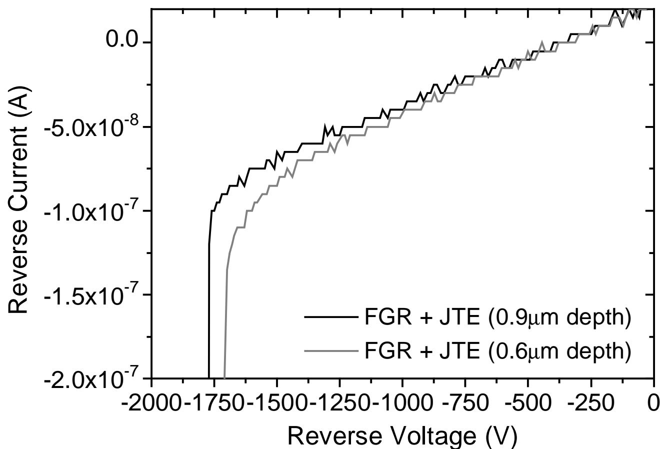


Figure 4.16 Reverse I-V characteristics of diodes with "FGR assisted JTE" termination.

The observed leakage current level is in the same range as in the other termination structures, reaching current densities of 3×10^{-4}A/cm^2 at breakdown.

No bright avalanche luminescence was observed in diodes with this termination structure, at least for reverse currents below 10μA, indicating that a relatively low impact ionisation rate is obtained at breakdown due to high spreading of the equipotential lines. However, for reverse currents higher than 10μA the diodes exhibited a catastrophic breakdown through metal sparking due to the high surface electric field reached. This behaviour is probably due to some problem with the passivation layer as it is also observed in diodes with other termination structures.

In conclusion, this novel developed termination structure has been proved to be a robust termination for high voltage diodes, as it is able to show higher blocking capabilities without degrading other aspects such as the leakage current or failure yield.

4.3 Technology and Design Considerations

4.3.1 Anode metal edge location

In order to study the influence of the anode metal edge location on the breakdown voltage of a diode with a JTE termination structure, we have analysed two configurations. Fig. 4.17 and 4.18 show the corresponding two cross-sections. For the configuration of Fig. 4.17 the metal anode contact ends at a distance of 20 μm from the edge of the main junction. In the case of Fig. 4.18 configuration the metal overlaps 20 μm the JTE layer. In both cases the length of the JTE is set to 80 μm.

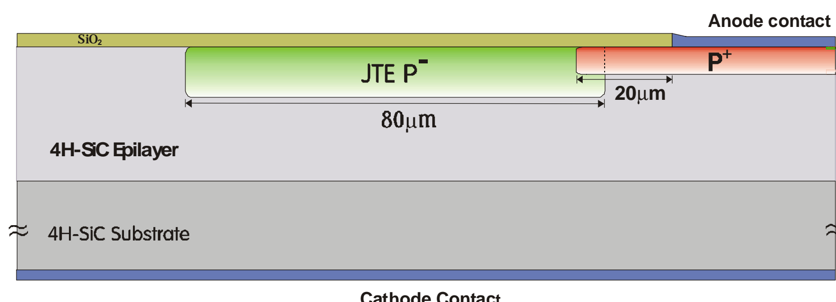


Figure 4.17 Cross-sectional schematic view of the diode configuration with the anode contact metal end inside the emitter region.

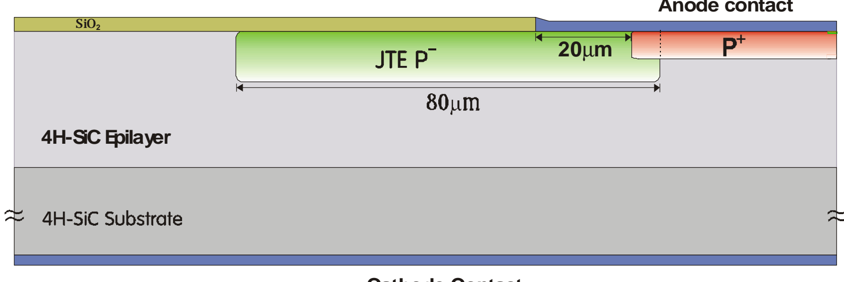


Figure 4.18 Cross-sectional schematic view of the diode configuration with the anode contact metal end overlapping the JTE region.

The experimental blocking characteristics showed differences between the two configurations. Table 4.5 reports the breakdown results of diodes with the two different metal configurations.

Table 4.5 Breakdown voltages of diodes with different anode metal configuration.

Metal configuration	Maximum Breakdown Voltage	Average Breakdown Voltage	Standard deviation	Efficiency
Metal inside the emitter (Fig. 4.17)	1640V	1550V	100V	82%
Metal end overlapping JTE region (Fig. 4.18)	1320V	1200V	125V	63%

As it is clearly observed from results in Table 4.5, diodes with the anode metal configuration as shown in Fig 4.17 are able to sustain higher blocking voltages than those with the anode metal placed as in Fig 4.18. Even if we consider that the effective JTE length is 60 μm instead of 80 μm due to the metal overlap in diodes with Fig. 4.18 configuration, the breakdown is much lower than what it was obtained previously with a single JTE zone of 65μm or even 35 μm (see Table 4.1). It is clear then that the metal overlap on the JTE has a negative influence on the breakdown. Moreover, the average breakdown voltage value measured on diodes with the Fig. 4.17 configuration agrees well with that of a single 80 μm JTE. This reduction in blocking capability of diodes with the anode metal contact edge overlapping the JTE region could be explained in terms of the high electric field strength produced at the corner of the metal contact with the JTE layer. The charge of the JTE region cannot spread the equipotential lines through the whole termination extension layer and thus the effective length of the JTE becomes reduced. In fact, the observed breakdown voltages corresponds in good agreement to that of a single 20 μm JTE. These results can be verified by numerical simulations, which predict a high electric field peak at the anode edge causing premature surface breakdown (see Fig.4.19) for the configuration of Fig. 4.18.

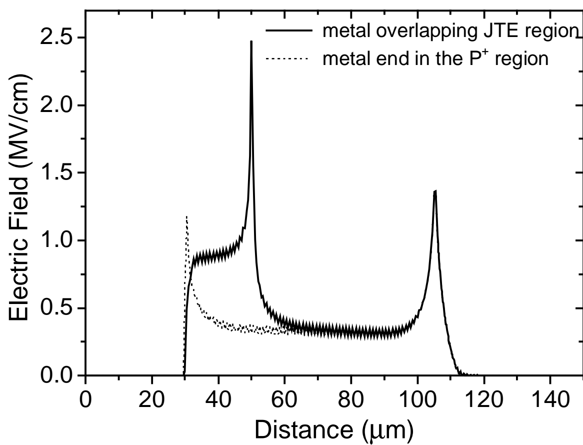


Figure 4.19 Surface electric field profile at breakdown for the two different anode metal edge location. Dot and solid lines correspond to the Fig. 4.17 and Fig. 4.18, respectively.

Figure 4.20 shows the impact ionisation distribution at breakdown for the two different configurations. It can be seen that for the case where the anode metal is placed over the JTE region (Fig 4.20a) the higher impact ionisation rate is placed at the emitter-JTE junction and at the anode metal edge. On the other hand, when the anode metal edge is placed inside the emitter region (Fig 4.20b), the higher ionisation rate takes place below the passivation layer, thus alleviating the surface electric field strength and preventing premature surface breakdown.

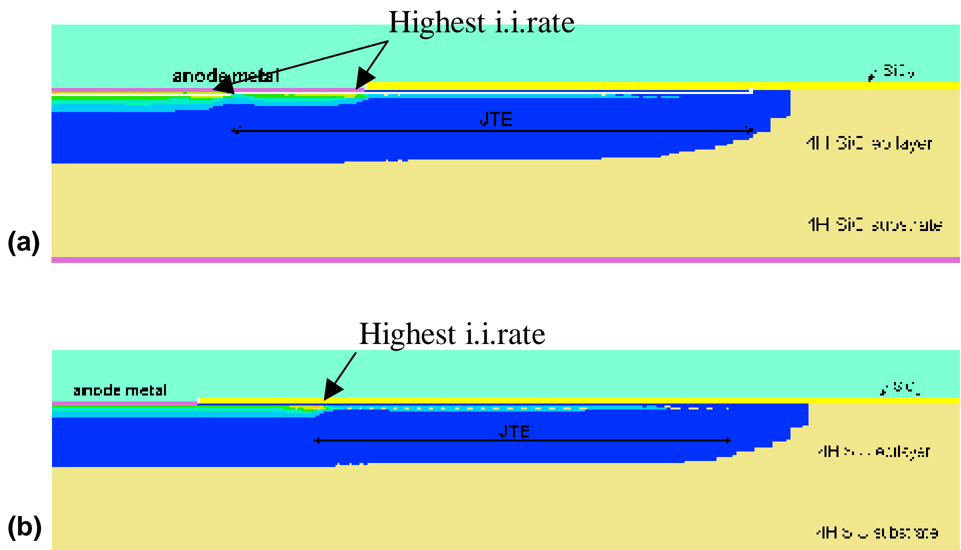


Figure 4.20 Impact ionisation generation distribution at breakdown of the two different anode metal configurations. (a) configuration of Fig. 4.18, (b) configuration of Fig. 4.17. On both simulations the dose of the JTE is $1.2 \times 10^{13} cm^{-3}$.

4.3.2 Field Plate effect

As mentioned in the fabrication process section (Chapter 3 section 3.2), after the highest contact anneal a thick metal (Au) layer was deposited to complete the diode fabrication. This metal layer was designed to form a small field plate (10 µm length) over the silicon dioxide layer. The same metal field plate was implemented on all the diodes with the termination structures analysed on previous sections. As an example, Figure 4.21 shows the schematic cross-section view of a standard diode with single JTE structure after the thick metal layer deposition.

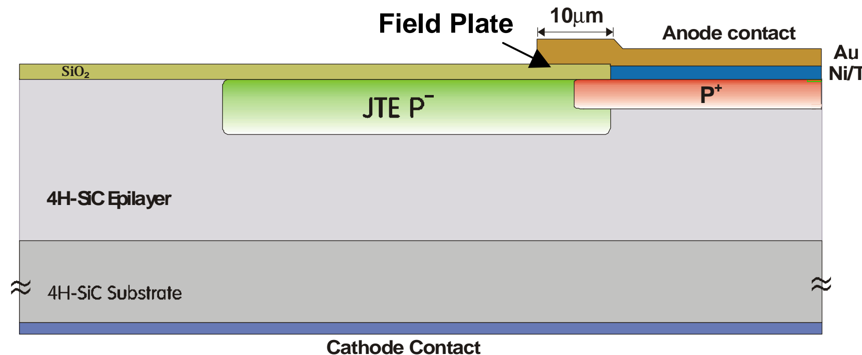


Figure 4.21 Cross-sectional view of a PiN diode with the thick Au metal deposited forming a field plate of 10µm over the silicon dioxide layer.

The effect of the metal field plate (FP) on the reverse characteristics is a great reduction in the reverse leakage current level and a small increase in the reverse breakdown voltage value, as it can be observed in Fig 4.22. With the field plate configuration the leakage current is reduced to below the 20 nA resolution limit of the curve tracer up to the onset of sharp avalanche breakdown. The increase in the breakdown voltage was shown to be more pronounced on diodes with low termination efficiency, i.e low breakdown voltages. Thus, diodes without any edge termination showed an increase of about 100V in the breakdown value, reaching blocking voltages of 450V±50V. Diodes with the multiple guard ring termination structure (in any of the three doping levels) showed an average increase of about 15% in their respective breakdown voltage values (see Fig. 4.23).

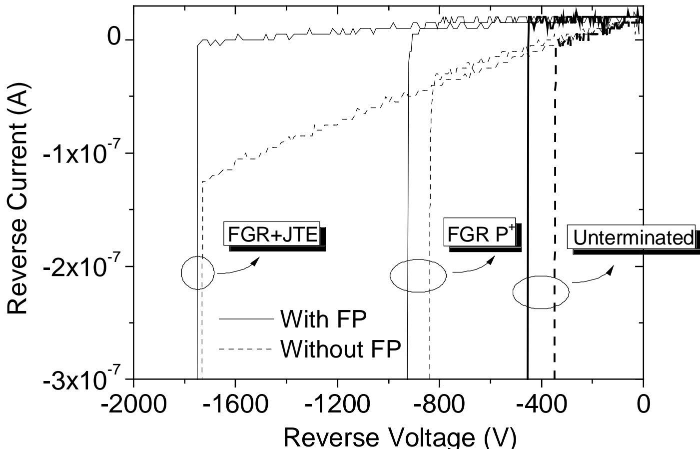


Figure 4.22 Reverse I-V characteristics of diodes with (solid lines) and without (dashed lines) field plate. The three examples shown are an unterminated diode, a diode with FGR´s assisted JTE structure and a diode with P^+ FGR´s termination.

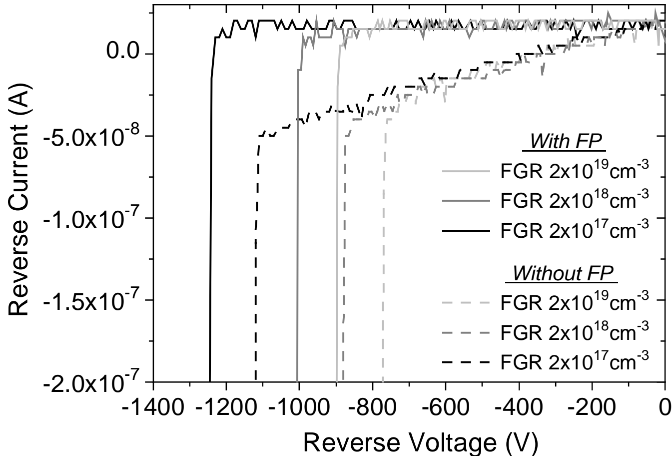


Figure 4.23 Reverse I-V characteristics of diodes with FGR termination and field plate showing the reduction in leakage current and increase in breakdown voltage. The curves presented corresponds to the same diodes measured before (dotted lines) and after (solid lines) the thick metal deposition configuring the field plate.

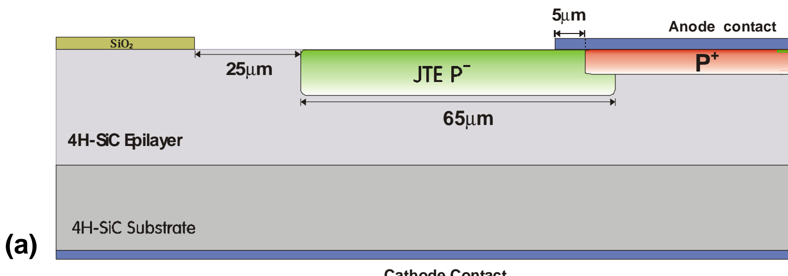
The improvement of the breakdown was less marked (practically inappreciable) in diodes with high reverse breakdown voltages, i.e. greater than 1500V, although the reduction in reverse leakage current was also observed. This behaviour reinforces the evidence that our junction termination extension structures are well optimised, being totally depleted at the breakdown voltage and thus allowing an effective spreading of the equipotential lines through the entire JTE regions.

In conclusion, it has been proved that the formation of a metal field plate over the diode periphery is important in order to obtain better blocking performances and to greatly reduce the leakage current level.

4.3.3 Passivation layer effect

In the mask set designed for the fabrication of devices some diodes without passivation layer were implemented in order to analyse its influence on the reverse characteristics of silicon carbide diodes. Figure 4.24 shows a schematic cross-section of a diode with JTE and without oxide layer (Fig 4.24a) and an optical picture of its appearance after fabrication, where the unpassivated region can be clearly seen (Fig 4.24b).

(a)



(b)

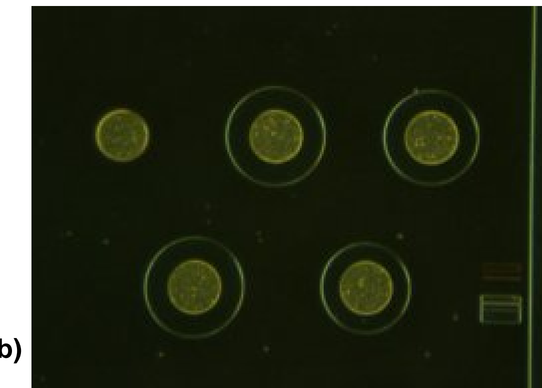


Figure 4.24 (a) Schematic cross-section of an unpassivated diode with single JTE, (b) Optical picture of the four fabricated diodes without passivation layer.

As it can be observed in Fig. 4.25, diodes without the silicon dioxide passivation layer show a high leakage current level in comparison to that of passivated diodes (without field plate). Thus, unpassivated diodes are not able to achieve the avalanche breakdown regime due

to high surface leakage current increase. Moreover, due to the high electric field present at the SiC surface and at the anode metal under high reverse voltages, an electrical arching in air is commonly observed from the anode metal to the edge of the unpassivated region, as it is clearly seen in Fig. 4.26.

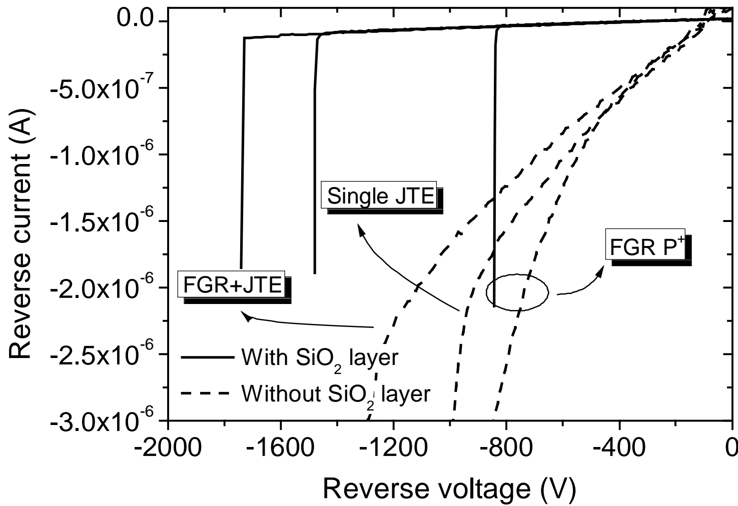


Figure 4.25 Reverse I-V characteristics of unpassivated diodes (dashed lines) and passivated diodes (solid lines). The three examples shown are a diode with FGR´s assisted JTE structure, a diode with single JTE, and a diode with P^+ FGR´s termination.

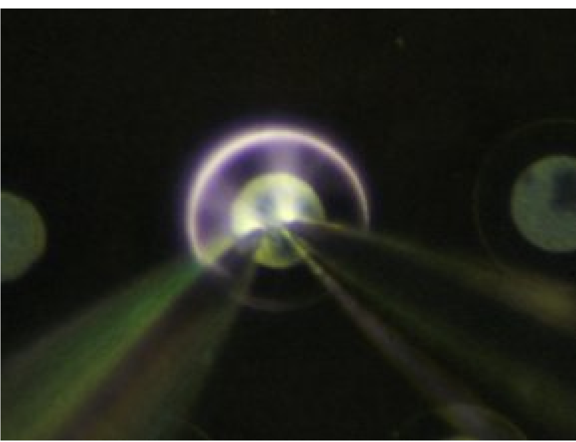


Figure 4.26 Observed electric arching in air from the anode metal to the edge of the unpassivated circular region under high reverse bias voltage.

These results reinforce the idea that a primary passivation layer (dioxide layer) is needed in order to reduce the surface leakage current and to allow the achievement of the best blocking capabilities in high power rectifiers. We have also found that to avoid sparking in air and to improve the blocking reliability of the diodes it is profitable to add a secondary passivation layer. In our case, a thick polyamide layer proved to be a good choice to fullfil these performances.

4.4 Diode Degradation in Reverse Mode

The leakage current of a $p^{+}n$ junction can be described as the sum of the diffusion current and the generation current in the depletion region,

$$J = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_g} \tag{4.1}$$

where D_p is the diffusion constant, τ_p the minority carrier lifetime, n_i the intrinsic carrier concentration, τ_g the effective generation lifetime and w the width of the depletion layer. The intrinsic carrier concentration is over 10^{15} times smaller in large band-gap materials such as SiC when it is compared to Si. This term dominates both contributions, which gives a very small leakage-current compared to that of a similar device manufactured in silicon. However, the reverse leakage current in SiC PiN rectifiers has been found to be orders of magnitude higher than predicted by standard silicon theory extensions. Obviously, material defects, such as screw dislocations, play a role in determining the reverse current [161].

Fig 4.27 shows the reverse blocking current-voltage characteristics at room temperature of the diodes with the different edge termination structures presented in the previous sections. In order to analyse the leakage current characteristics, the curves presented in Fig 4.27 are those measured without the second thick metal deposited, i.e. without the field plate configuration.

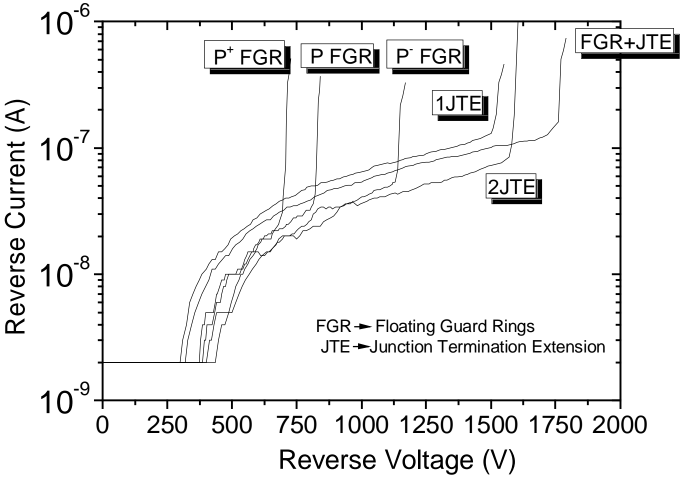


Figure 4.27 Reverse I-V characteristics of the diodes representative of the average breakdown voltage of each termination structure. The P^{+}, P and P^{-} accounts for the doping level of the FGR, $2\times10^{19}cm^{-3}$, $2\times10^{18}cm^{-3}$ and $2\times10^{17}cm^{-3}$, respectively.

The leakage current of diodes was below the 20nA resolution limit up to 400V reverse bias. For higher reverse voltages the leakage current does not follow a square-root dependence on voltage as would be the case of the conventional space-charge generation limited current. This non space-charge generation current behaviour is due to the punch-through configuration, as the drift layer becomes fully depleted at a reverse bias of about 800V. The leakage current at a

reverse voltage higher than the punch-through voltage is observed to vary as $I\mu V^m$ with m=1.4 ± 0.1 , which can be attributed to the resistive surface leakage path due to the damage caused by the p^+ and JTE implantations around the periphery of the device [162,163]. In addition, the reverse leakage current is much higher than the predicted contributions from diffusion, bulk space-charge generation or surface perimeter generation, thus, some other mechanisms likely through dislocations or other process induced defects must take place to account for the observed leakage current.

Sharp avalanche breakdown is obtained without catastrophic failure on most of the tested diodes showing reversible blocking characteristics. However, some diodes showed breakdown at the contact periphery leading to irreversible device failure due to the presence of a defect or a passivation malfunction near the active region of the device. Destructive failure of the device typically occurred when reverse currents exceeded 10 μA during high-voltage testing.

Figure 4.28 shows optical pictures of devices where catastrophic device failure has occurred due to the presence of a defect near the active device region. In these pictures it can be clearly seen the effect on the diode anode metal of the sparking due to surface ionisation of the air between the anode metal edge and the present defect.

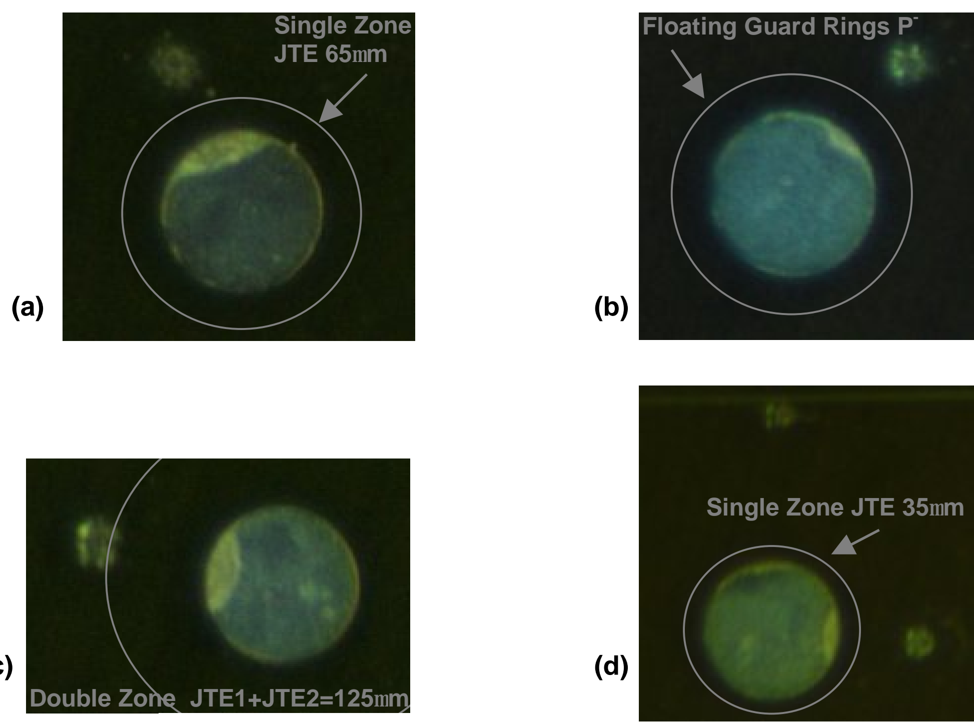


Figure 4.28 Illustrative optical pictures of the catastrophic breakdown of diodes due to the presence of a defect near the active region of the device. The white drawn circles indicate the end of the termination structure region.

The arching in air observed during irreversible device failure is due to the high electric field reached at the metal-semiconductor edge junction. The avalanche at the highest breakdown voltages (V_{BR}>1500V) occurs at the corresponding electric field of about 2.4MV/cm as estimated for 4H-SiC from analytical and empirical formulas (see Chapter 2).

Some devices did not showed the catastrophic breakdown shown in pictures from Fig. 4.27, but show a weak metal sparking that lead to high increase of the reverse leakage current without altering its blocking capability. Figure 4.29a shows a SEM image of the metal dysfunction of a diode with double JTE structure in a side-by-side configuration after thick metal deposition, i.e. with gold field plate, that shows a high increase in reverse leakage current at low reverse voltages but which is still able to block up to 1600V, as seen in Fig. 4.29b.

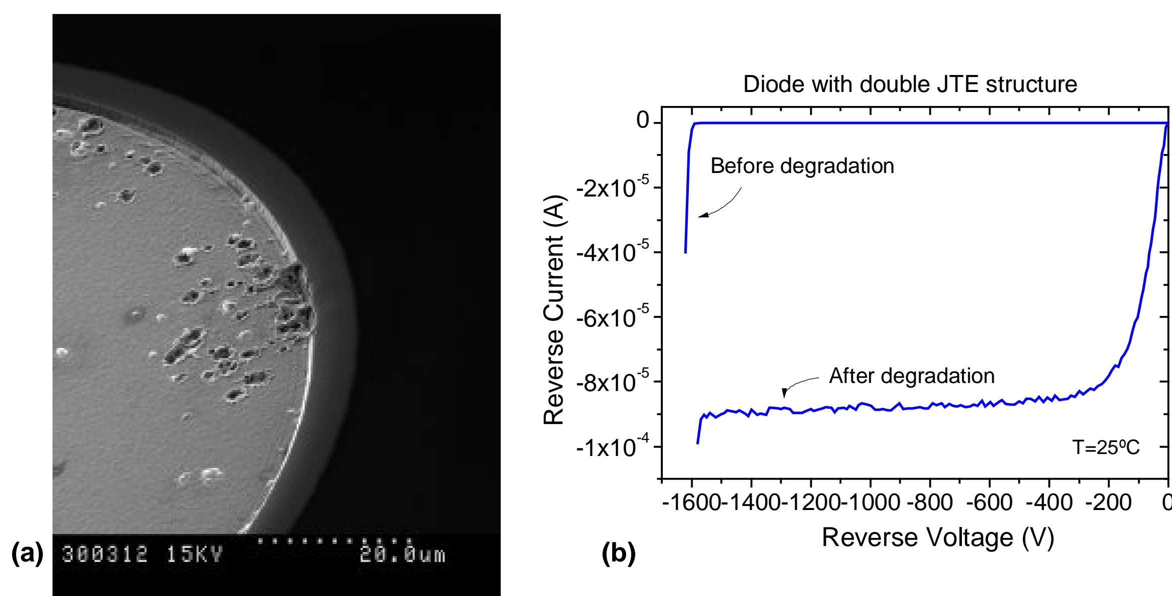


Figure 4.29 (a) SEM image of the anode metal of a diode suffering from high reverse leakage current, (b) Corresponding reverse I-V characteristics.

4.4.1 High temperature reverse characteristics

An important property for the application in power devices is the temperature coefficient of the avalanche breakdown voltage. If the breakdown voltage was decreasing at higher temperatures, a local avalanche and self-heating caused by its breakdown current would cause a filamentation of the leakage current, possibly leading to catastrophic device failure. First measurements of breakdown voltages in silicon carbide diodes seemed to indicate such a negative temperature coefficient of breakdown voltage [164,165]. It was later shown that the temperature coefficient of the breakdown voltage in defect-free 4H-SiC actually was positive [89,90,163].

Fig. 4.30 shows the leakage current characteristics at room temperature, 100ºC and 200ºC of a typical diode with "FGRs assisted JTE" termination structure. As inferred from Fig. 4.30, the reverse leakage current is thermally activated increasing an order of magnitude from room temperature to 200ºC. However, it must be pointed out that the leakage current level does not increase significantly at 100ºC, keeping near the room temperature level. Moreover, the slope of reverse current-voltage characteristics shows a weak dependence on temperature. This low temperature dependence shows that the leakage current may be caused by surface recombination, not by bulk recombination via deep defect centers. The bulk recombination generally increases exponentially with increasing temperature. This is very attractive for low-loss, high-power application at a high operating temperature.

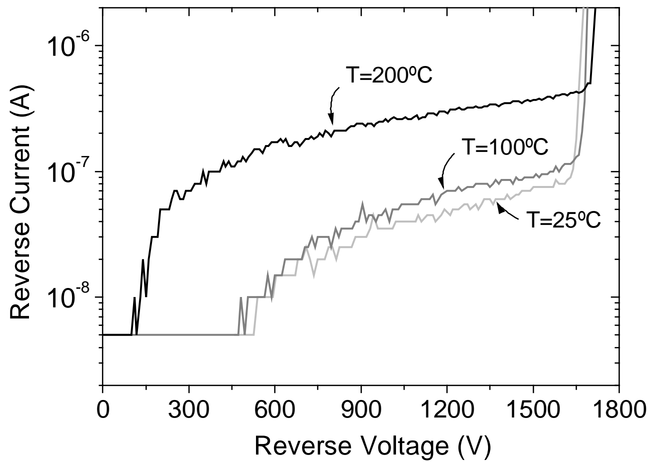


Figure 4.30 Reverse I-V characteristics at room temperature (25ºC), 100ºC and at 200ºC of a diode with FGRs assisted JTE termination.

As seen from Fig 4.30, the diodes showed a positive breakdown temperature coefficient, which clearly accounts for an avalanche breakdown mechanism and not other mechanism such as defect-assisted tunnelling. Although the positive temperature drift of the avalanche coefficient is small for the case of breakdown voltages near the ideal plane-parallel breakdown voltage (less than 0.5V/K), it was surprisingly found that diodes without any edge termination or with a low efficiency termination structure (such as a FGR) showed a high increase in breakdown voltage with increasing temperature, leading to positive temperature coefficients near 2V/K, as shown in Fig. 4.31. Moreover, the reverse measurements at temperatures up to 200ºC were found to be very stable and it was possible to measure the reversible avalanche breakdown without degradation of the blocking characteristics.

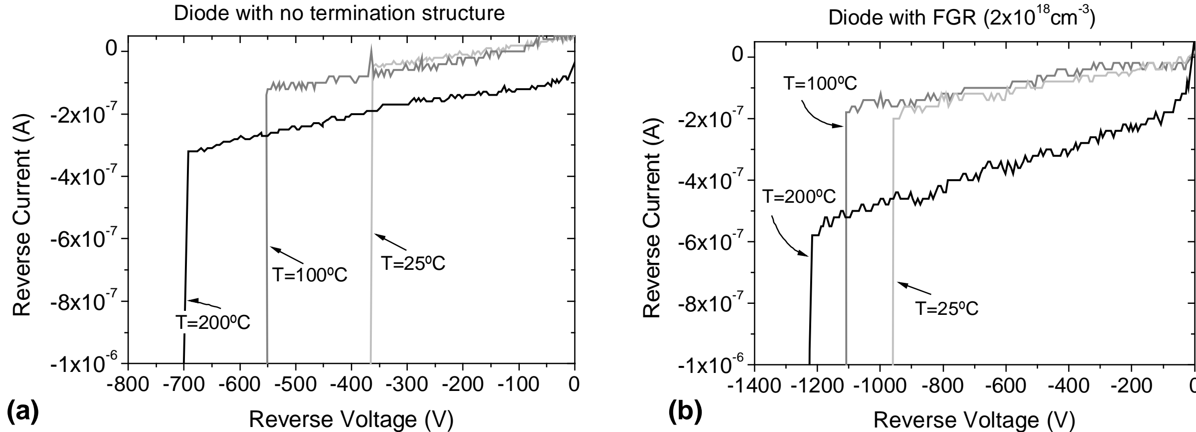


Figure 4.31 Reverse I-V characteristics at room temperature (25ºC), 100ºC and at 200ºC of , (a) diode without any termination, (b) diode with FGR ($2\times10^{18}cm^{-3}$ ring´s doping) termination structure.

As observed in Fig 4.31, an increase of nearly 350V is observed in the breakdown voltage of diodes without any edge termination structure when the temperature increases from 25ºC to 200ºC. This high positive temperature coefficient was clearly observed in a high number of tested diodes with no termination. Thus, the positive temperature drift of the avalanche coefficient observed on most of the tested devices is one of the most crucial characteristics required for reliable power devices. It indicates that robust 4H-SiC power devices with the same high reliability of modern silicon power devices should be achievable after SiC growth technology maturation greatly reduces defects such as micropipes, dislocations, and deep levels in commercial SiC wafers and epilayers.

Reverse measurements at high temperature were also carried out on diodes without surface passivation layer, and a very different temperature behaviour was observed, as shown in Fig. 4.32.

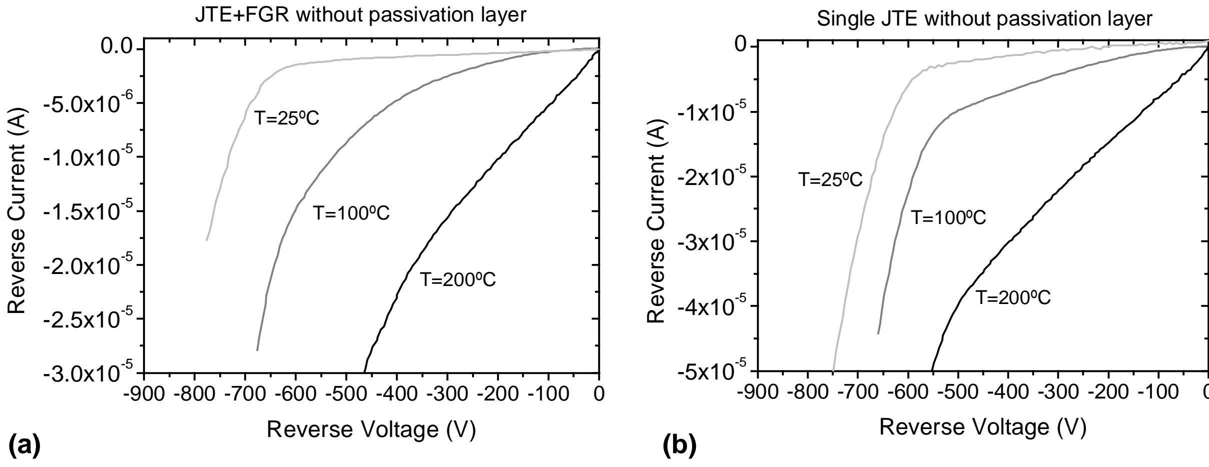


Figure 4.32 Reverse I-V characteristics at different temperatures of diodes without surface passivation layer. (a) Diode with FGR assisted JTE termination, (b) Diode with single JTE termination.

In diodes without silicon dioxide layer (reported in section 4.3.3) a negative temperature coefficient is found. As a reference, the reverse leakage current at 500V increases from 2.5×10^{-6}A up to 4×10^{-5}A when increasing temperature from 25ºC up to 200ºC. This high negative temperature breakdown behaviour is associated to the fact that these diodes do not reach the avalanche breakdown regime but suffer from high surface generation leakage current which highly increases with temperature.

This result reinforces the idea exposed in section 4.3.3 that a properly designed passivation layer is needed in SiC devices in order to exploit the intrinsic material capabilities and reach the high potential performance of SiC power devices.

4.5 Results on Boron Implanted Diodes

In this section, the performance of 4H-SiC PiN diodes with the p-type regions formed by boron implantations will be reported. As it was already explained in Chapter 3 section 3.2.2, samples from wafer XU-0884-01 were implanted with B^+ to form both the P^+ doped regions and the P^- doped edge termination regions. The two different implantation profiles are shown in the previously mentioned section. It must be noted that as no intermediate P (~2×10^{18}cm^{-3}) doping level implantation was performed, many termination structures designed in the photolito mask set (mainly the double zone JTE) were not formed. The boron implantations were carried out at room temperature in the cleanroom of the CNM. The diodes were metallised with Ni/Ti and passivated with a thick SiO_2 layer.

After the implantation processes, an activation annealing was performed at 1650ºC for 45min. As it is well known, this temperature treatment causes a rapid diffusion of B toward the surface, which results in great out-diffusion of the implanted species and thus a strong decrease of the total B concentration in the sample. In addition, a pronounced diffusion of boron into the undamaged region of the SiC epilayer is observed. To analyse this transient enhanced diffusion on our boron implanted samples, SIMS measurements were carried out on two samples with 1.1×10^{13}cm^{-2} implanted dose in the P$^-$ regions. Figure 4.33 shows the two obtained SIMS profiles together with the I^{2}SiC simulated profile of the boron implantation.

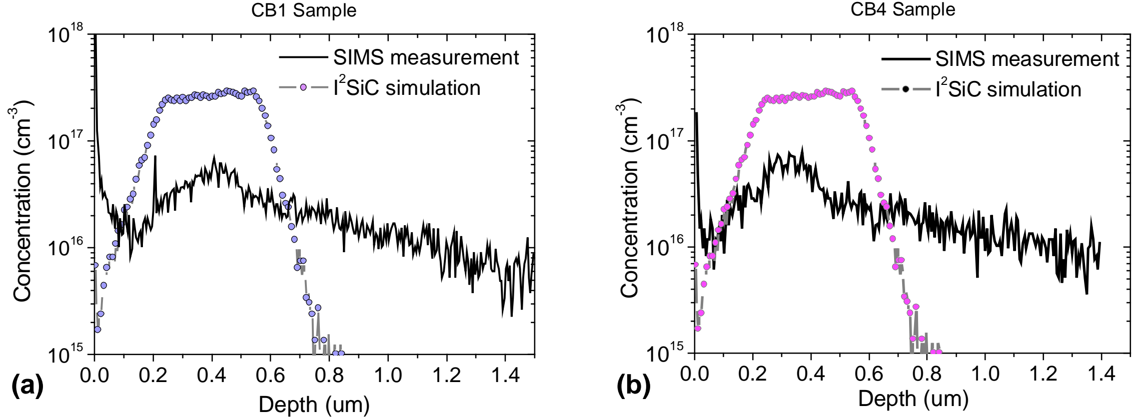


Figure 4.33 SIMS profiles (red lines) after the high temperature activation anneal of samples (a) CB1 and (b) CB4. The I^{2}SiC simulated profile for the as-implanted stage (blue line) is also shown for comparison.

As it can be seen in the two graphs from Figure 4.33, a clear redistribution of the implanted B profile is observed after the activation anneal. An analysis of the two SIMS profiles reveals that great outdiffusion has taken place. The calculated doses from the SIMS profiles are 3.3×10^{12}cm^{-2} and 3.9×10^{12}cm^{-2} in samples CB1 and CB4, respectively. Taken into account the initial implanted dose (1.1×10^{13}cm^{-2}), it can be concluded that about 68% of the targeted boron implanted dose has been outdiffused, which also leads to the observed dip close to the surface.

4.5.1 Reverse characteristics

The 1D theoretical maximum breakdown voltage of the epilayer configuration (20μm, $2\times10^{15}cm^{-3}$) of boron implanted samples is 3.5kV. Reverse breakdown simulations performed on PiN diodes with the initial implanted dose in a single zone JTE (125μm) showed that breakdown voltages close to 95% of the ideal one could be achieved. However, simulations performed with the lower dose values extracted from the SIMS profiles obtained after the activation anneal lead to breakdown voltages in the 2000-2200V range.

Initial breakdown measurements performed on all boron implanted samples revealed that an extra passivation layer was needed in order to reach high breakdown voltages, as with only the initial SiO_2 passivation layer the diodes showed a sharp breakdown caused by metal sparking in air at voltages of about 900V, as seen in Figure 4.34.

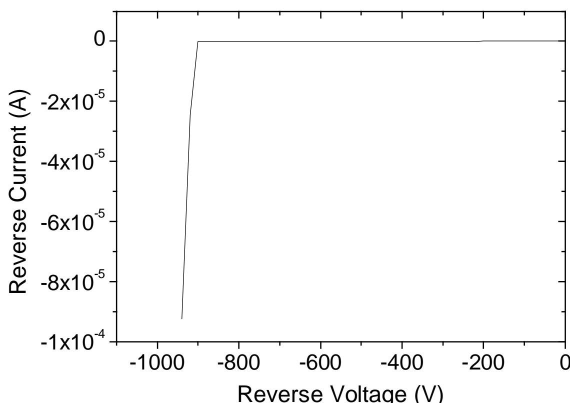


Figure 4.34 Reverse breakdown I-V curve of PiN diode with single JTE structure on sample CB1.

Thus, an extra passivation was implemented with the deposition of a thick polyamide layer. A great improvement in the measured breakdown voltages was observed with this extra passivation, and breakdown voltages up to 2000V were obtained. Although most of the highest breakdown voltages were measured on diodes with the "FGR assisted JTE structure", no reliable analysis on the efficiency of the different edge termination structures could be done due to a high scattering of the results from the different samples and a low yield of "good" devices with different terminations. Figure 4.35 shows some of the measured breakdown curves in diodes with different edge termination from sample CB4.

The reverse leakage current at breakdown measured in the boron implanted diodes ($\sim7\times10^{-6}$A) is clearly larger than that obtained in aluminum implanted diodes. Moreover, a great number of devices exhibited the degraded reverse leakage current characteristic already explained in section 4.4, as shown in Fig. 4.36. This reverse current characteristics is associated to a metal edge dysfunction probably caused by a previous measurement without the extra passivation layer.

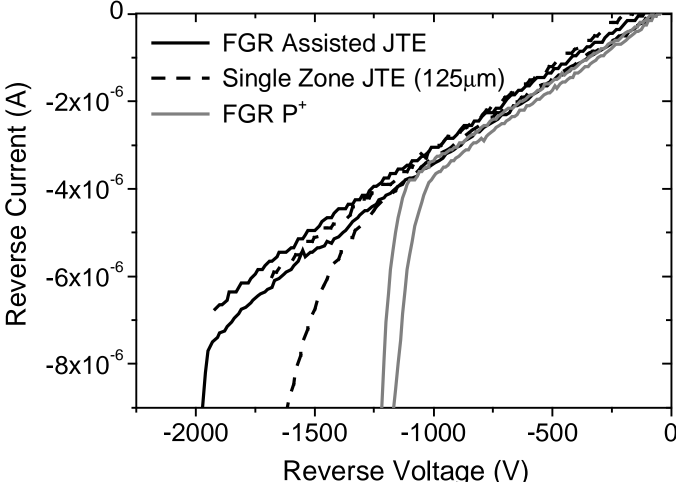


Figure 4.35 Reverse I-V characteristics of PiN diodes from sample CB4 with different edge terminations formed with boron implantations, after the extra passivation layer deposition.

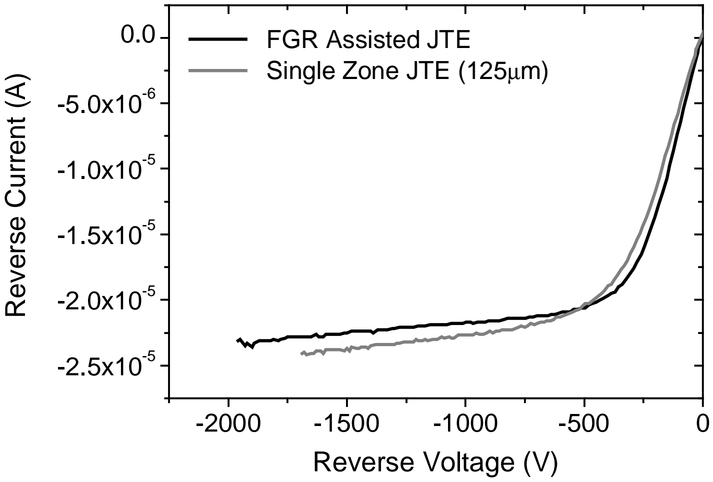


Figure 4.36 Degraded reverse I-V characteristics of PiN diodes from sample CB4 with different edge terminations formed with boron implantations, after the extra passivation layer deposition.

4.5.2 Forward operation

Concerning the forward current-voltage characteristics of boron implanted bipolar diodes, some irregular behaviour was observed. As it occurs with the lower boron doping concentration implantation (for the termination regions) after the activation anneal, it is expected that a redistribution of the implanted profile of higher boron doping implantation (for the emitter region) will take place. However, no SIMS measurements were made for the

emitter profile after the high temperature activation anneal. Nevertheless, from the I-V characteristics of bipolar diodes and TLM measurements on p^+ boron implanted regions, some speculations could be made about the emitter doping profile after the activation anneal.

Figure 4.37 and Figure 4.38 show the characteristic J-V curves at room temperature of emitter boron implanted diodes in the as-deposited metal stage (Ni/Ti) and after a RTA at 950ºC for 3min, for the samples CB2 and CB4, respectively.

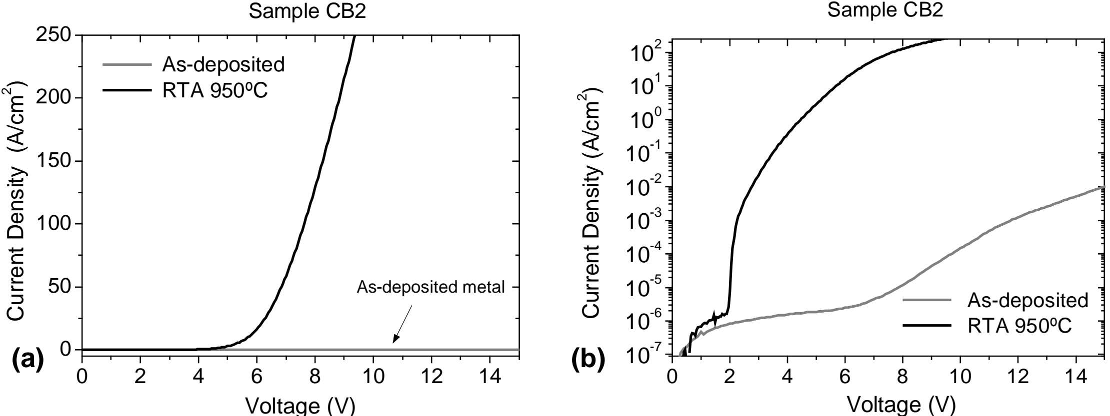


Figure 4.37 J-V characteristics of PiN diodes on sample CB2 in the as-deposited metal stage and after an RTA at 950ºC for 3min. (a) Linear scale, (b) Semilog current scale.

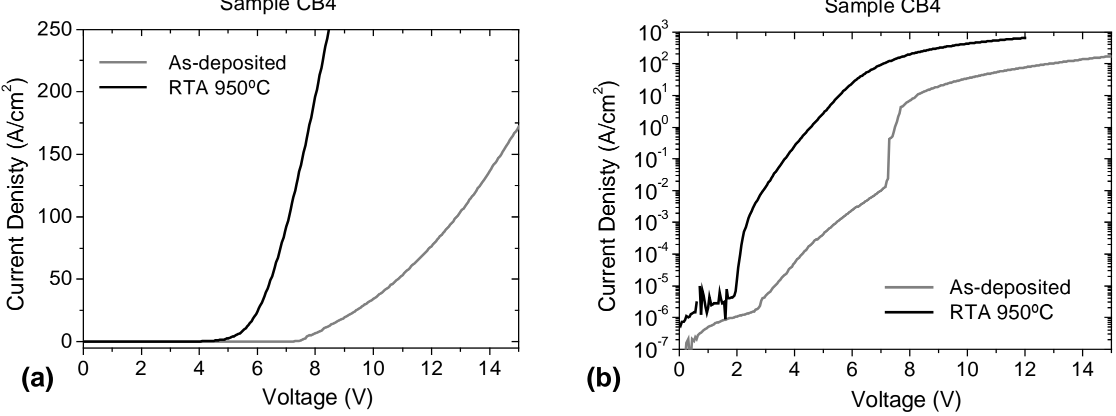


Figure 4.38 J-V characteristics of PiN diodes on sample CB4 in the as-deposited metal stage and after an RTA at 950ºC for 3min. (a) Linear scale, (b) Semilog current scale.

As it can be observed in previous figures, highly non-ideal behaviours are obtained for boron emitter implanted diodes, specially in the as-deposited metal stage. After the RTA at 950ºC for 3min, a great improve in the I-V characteristics is observed, although they are still far from the ideal bipolar behaviour. Forward voltage drops of ~7V@100A/cm^2 are obtained after the 950ºC RTA, which are clearly higher than those obtained on aluminum implanted diodes (3.1V@100A/cm^2), even taking into account the different epitaxial configuration.

This non ideal bipolar performance is associated with the redistribution of the implanted boron after the high temperature activation anneal, which may probably lead to great

outdiffusion of the implanted dose and to a displacement of the high doping concentration from the surface. Thus, the lower obtained doping level concentration and the doping depleted region near the surface translate into a non ohmic behaviour of the contact even after the high RTA at 950ºC. This is confirmed by TLM measurements performed at room temperature on P^+ boron implanted regions after the 950ºC RTA, which show a very high sheet resistance (~3MΩ/□) and a highly non ohmic behaviour, as shown in Figure 4.39.

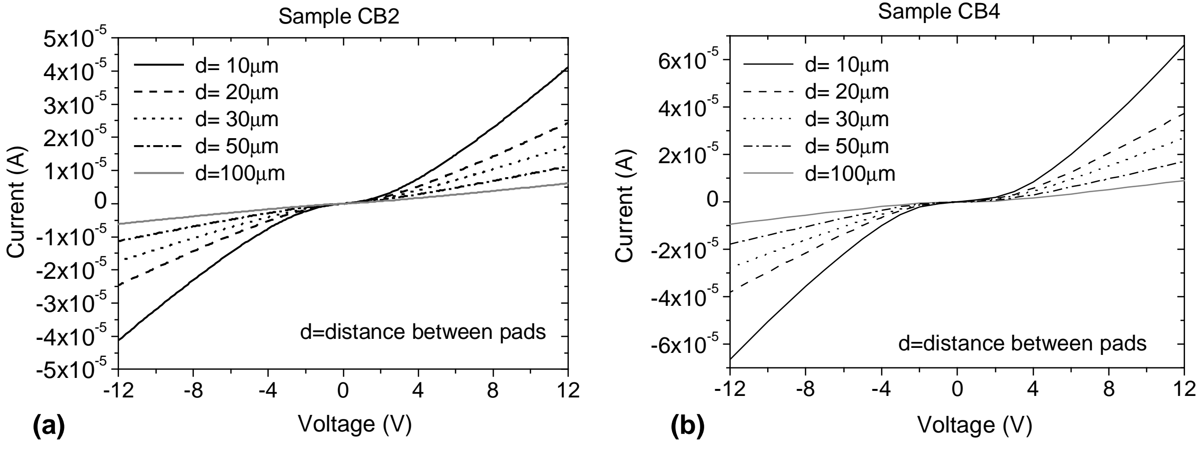


Figure 4.39 I-V characteristics of TLM structures on P^+ boron implanted regions after the 950ºC RTA. (a) Measurement performed on sample CB2, (b) Measurement performed on sample CB4.

In conclusion, it has been shown that in order to be able to fabricate reliable PiN SiC diodes with boron as an acceptor impurity, improvements in the boron redistribution after the activation anneal process have to be achieved. Further control over the boron doping profile would allow to exploit the advantages of boron as a p-type doping impurity (i.e. less implantation damage and higher implantation depths).

4.6 Summary

In this chapter, a detailed analysis of the efficiency of the different edge termination techniques developed during this thesis and commonly used in SiC devices has been presented. It has been proved that both single and double JTE structures are more effective to achieve breakdown voltages close to the ideal plane than the multiple floating guard rings termination. Moreover, it has been shown that the JTE length and the JTE implanted profile depth play an important role in achieving the maximum blocking capabilities of these termination structures. We have experimentally demonstrated the benefits of a highly effective novel junction termination structure, namely *floating guard ring assisted JTE*, which

provides a stable and high breakdown voltage (95% of efficiency), resulting less sensible to technological parameters shift.

We have also analysed second order design parameters, which are not usually considered but clearly important as our results shown. The implementation of a small field plate over the passivation layer has shown to reduce the leakage current of diodes and to improve the breakdown voltage of those with low termination efficiency. Besides, we have demonstrated the need to implement an efficient passivation layer in order to be able to obtain low reverse leakage currents and to reach high breakdown voltages. The location of anode metal edge over the JTE region has been proved to be detrimental for the efficiency of the single JTE termination, in comparison to the common case where the anode metal edge is placed over the whole emitter region.

High temperature reverse current-voltage measurements were also carried out, obtaining a stable positive avalanche breakdown behaviour. In summary, we have demonstrated the feasibility of reliable aluminum ion-implanted planar diodes with good blocking capability and thermal stability. The novel edge termination structure presented can be adopted in a wide range of power devices such as Schottky rectifiers, MOSFETs, or IGBTs as a robust breakdown termination structure.

Finally, a study performed on boron implanted diodes clearly showed that further control on the boron impurity redistribution after the high temperature activation anneal is needed in order to achieve good performances on devices with the selective regions formed by boron implantations.

CHAPTER 5

High Temperature Power Rectifiers Performance

This chapter covers the current-voltage performance at high temperature operation, up to 300ºC, of the three different power rectifiers fabricated (PiN, JBS and Schottky). A detailed analysis and description of the forward and reverse conduction mechanisms will be carried out for each type of rectifier together with the explanation of non-ideal *I-V* behaviours observed on some devices. Finally, a brief analysis of the forward bias degradation phenomenon on bipolar diodes will be reported.

5.1 Important Parameters for Power Rectifiers

The most important parameters when quantifying a power rectifier are blocking voltage (V_{BR}), on-resistance (R_{on}), and forward voltage drop (V_F). How these parameters change with temperature has to be considered. For rectifiers, the static on-state losses can be expressed in the forward voltage drop over the diode and the on-resistance in the drift region, which accommodates the specified blocking voltage. In Fig 5.1 these parameters are compared for a SiC PiN, Schottky and JBS diode. The barrier voltage over the diode is lower for a Schottky and JBS diode compared to the PiN diode since it is determined by the metal-semiconductor barrier height (Φ_B) instead of a p^+n junction barrier. On the other hand, the on-resistance is lower for the PiN diode since the forward current is conductivity modulated. The PiN diode on-resistance is a function of blocking voltage, current density and carrier lifetime in the base. In the Schottky and JBS diode the conduction is a unipolar electron current giving a linear current dependence with voltage drop (see Fig. 5.2).

For the total on-state losses contact resistances and substrate resistance must also be taken into account. Silicon carbide wafers (substrates) are normally 300 μm thick with ~10^{18}-10^{19}cm^{-3} nitrogen doping level. Then, the substrate resistance is 0.1-0.3 mΩcm^2, resulting in voltage drops of 10-30 mV at 100 A/cm^2. Reproducible contact resistances to n-type SiC using nickel as contact metal are in the 10^{-6} Ωcm^2 to 10^{-5} Ωcm^2 range, which results in voltage

drops of around 10 mV at 100 A/cm^2. Then a good estimation is that the substrate plus contact resistance contribution to the total forward voltage drop is maximum 100 mV.

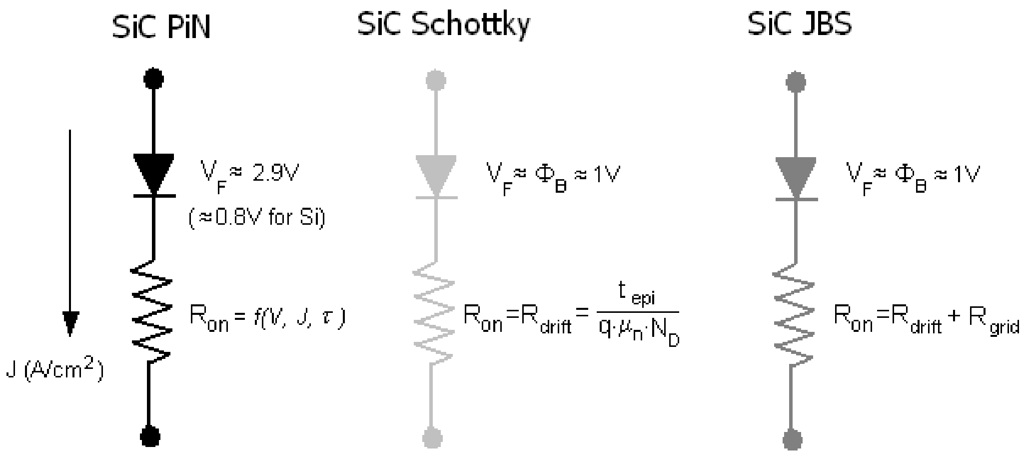


Figure 5.1 Contributions to the total on-state losses for a PiN diode, Schottky diode, and JBS diode respectively. The JBS diode has an additional resistive part from the p$^+$n junction grid compared to the Schottky diode.

In Fig 5.2 the typical current-voltage characteristics is shown for a Schottky, JBS and PiN diode. In comparison with a SiC PiN diode, the Schottky and JBS diode are attractive only as long as the unipolar on-resistance gives a lower voltage drop than that of the PiN diode. The "cross-over" point depends on blocking voltage, but also on operating current density and operating temperature.

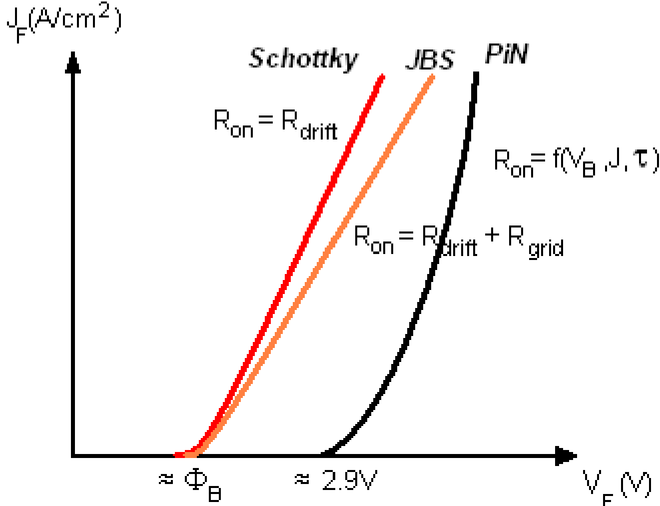


Figure 5.2 Schematic comparison of forward characteristics for a PiN, Schottky and JBS rectifier in SiC.

5.2 Schottky Diode Performance

5.2.1 Specific on-resistance and forward voltage drop

For high-power device applications, the specific on-resistance should be as low as possible. The Schottky rectifier is made by growing a thin epitaxial layer on a thick, highly doped N^+ substrate. The resistance of the substrate can be significant in low-voltage rectifiers for which the drift layer resistance becomes small. It is shown in equation 5.1, where t is the thickness of the epilayer and substrate, V_B is the breakdown voltage.

$$R_{on} = \frac{t}{q \cdot \mu_n \cdot N_D} = \frac{4 \cdot V_B^2}{\varepsilon_S \cdot \mu_n \cdot E_C^3}$$

$$= \left(\frac{t_{epi}}{q \cdot \mu_n \cdot N_D} \right)_{epilayer} + \left(\frac{t_{substrate}}{q \cdot \mu_n \cdot N_D} \right)_{substrate} \tag{5.1}$$

Using equation 5.1, the specific on-resistance versus the breakdown voltage for 4H-SiC and Si is plotted in Figure 5.3. The straight line (theoretical line) is calculated assuming that the contact resistivity of the substrate is less than ~10^{-7} Ωcm^2, and taking the parameter values (mobility, critical electric field, and dielectric constant) from those specified in chapter 2, including the doping dependence. The contribution to the specific on-resistance from the substrate is also plotted (dotted lines) for 4H-SiC in the same figure for two different doping levels and assuming a substrate thickness of 300μm.

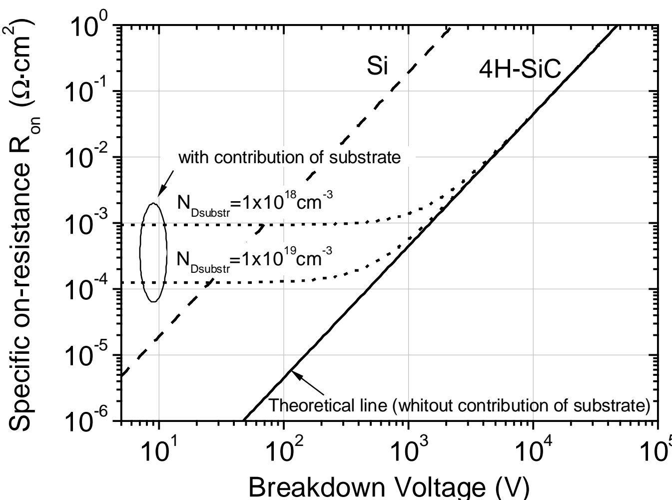


Figure 5.3 Specific on-resistance R_{on} *vs* the breakdown voltage for 4H-SiC (solid line) and Si (dashed line). The contribution from the substrate is also plotted for two different doping levels (dotted lines) but with the same thickness (300 μm).

The on-resistance increases quadratically with blocking voltage and is the reason why unipolar devices have non-attractive on-state losses for higher voltages compared to bipolar devices.

Figure 5.4 shows the typical linear current-voltage characteristics of the Schottky diodes measured at room temperature for samples from the three wafers with different epilayer doping level processed during this thesis (CQ3, S1 and CB3, for more details see section 3.1 in chapter 3). All three samples have the same metallisation scheme in both cathode and anode contacts and the reported measurements are those carried out after the same RTA at 350ºC for 3min. The Schottky barrier extracted for all three samples is $\Phi_B = 0.82 \pm 0.02$eV.

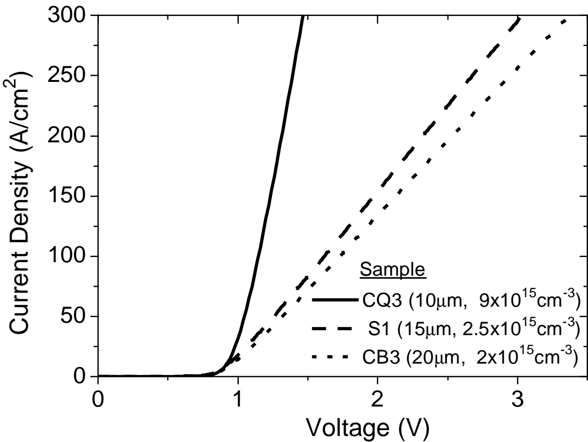


Figure 5.4 Room temperature I-V measurements of Schottky diodes on samples with different epilayer configuration. All samples have the same Ni/Ti Schottky contact and the measurement is carried out after the same RTA anneal at 350ºC for 3min for all three samples.

The on-resistance is extracted from the linear I-V behaviour at high current densities. The results are shown in Table 5.1 and are plotted in Figure 5.5 together with the theoretical lines taking into account the substrate resistance (Eq. 5.1) for on-resistance dependence on doping concentration of two different epilayer thickness (10 and 20 µm). The mobility values used for these on-resistance calculations were extracted from the work of Mnatsakanov *et. al.* [76], already shown in Chapter 2 section 2.2.5. As it can be observed, the obtained values for CREE´s wafers samples (CQ3 and CB3) are closed to the theoretical minimum on-resistance for each epilayer configuration, thus revealing the high quality of the material and indicating that the device processing produces no major degradation in the electrical properties of SiC.

Table 5.1 Experimental on-resistance and forward voltage drop values for the different processed samples.

Sample	Epilayer (thickness, doping)	On-resistance R_{on} (mΩcm^2)	Voltage drop at 100A/cm^2 V_F (V)
CQ3	10 µm, 9×10^{15}cm^{-3}	1.6	1.10
S1	15 µm, 2.5×10^{15}cm^{-3}	7.0	1.62
CB3	20 µm, 2×10^{15}cm^{-3}	8.0	1.73

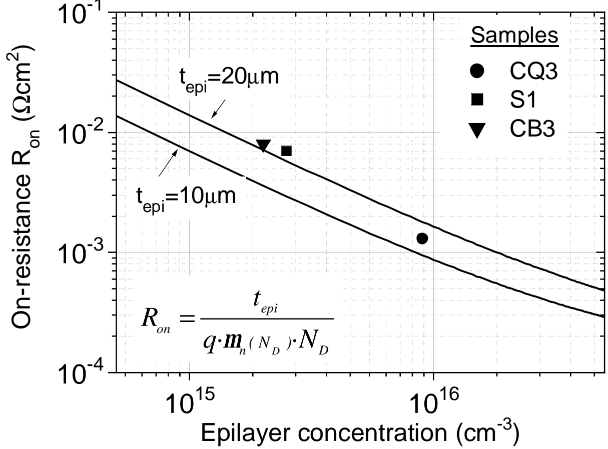


Figure 5.5 On-resistance dependence on epilayer doping concentration. Two different epilayer thickness are considered for representation. Scatter points represents experimental data from processed samples.

The forward voltage drop is a function of the Schottky barrier height and the series resistance. Based on the thermionic emission model, the total forward voltage drop across the Schottky rectifier can be written as [87]

$$V_F = \frac{nk_BT}{q} ln\left(\frac{J_F}{A^*T^2}\right) + n\Phi_B + R_{on}J_F \tag{5.2}$$

where V_F is the forward voltage drop, n is the ideality factor, k_B is Boltzman's constant, T is the temperature, J_F is the forward current density, A^* is the Richardson's constant, Φ_B is the Schottky barrier height, and R_{on} is the series or on-resistance.

For an optimal device design, once the forward current density has been specified, and the required breakdown voltage has been used to determine the epilayer doping and thickness, the only remaining variable that affects the forward voltage drop is the Schottky barrier height. In general the forward voltage drop of experimental SiC Schottky rectifiers has agreed well with thermionic emission theory and devices with ideality factors near one and specific on-resistance near the theoretical minimum have been reported [17,21,24].

When the breakdown voltage of the Schottky rectifier increases, the forward voltage drop increases with R_{on} as shown in equation 5.2. Changing the barrier height also influences V_F directly. Figure 5.6 shows the room temperature calculated forward voltage drop of 4H-SiC Schottky rectifier at 100 A/cm^2 as a function of breakdown voltage for our experimentally extracted barrier height (Φ_B = 0.82eV) and a mean ideality factor of n=1.4. Also included in figure 5.6 are the obtained experimental values from samples CQ3, S1 and CB3 (see table 5.1), and theoretical line for an ideal Ni barrier (Φ_B = 1.54eV), [142] for comparison.

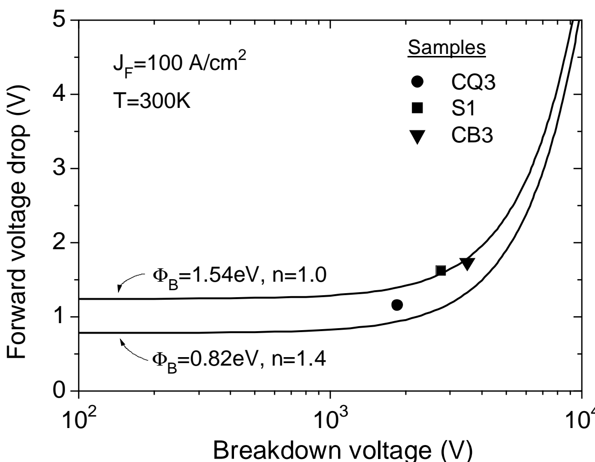


Figure 5.6 Forward voltage drop at 100A/cm^2 vs. breakdown voltage for Schottky rectifiers on 4H-SiC. Experimental data of our processed samples are plotted together with theoretical lines for two different barrier heights.

The voltage drop at 100 A/cm^2 does not increase up to a breakdown voltage rating of 1000V, beyond which a rapid increase is observed, mainly due to the increase in on-resistance. The experimental data are near the predicted minimum values. The short discrepancy from the ideal values could be attributed to parasitic contact resistance, resistive shunt defects across the metal-SiC junction, and bulk resistance. Also the uncertainties or deviation of some parameter values (mobility, Richardson constant, ideality factor and epilayer concentration and thickness) must be considered when comparing the experimental data with the theoretical prediction.

5.2.2 High temperature forward performance

High temperature operation of the 4H-SiC Schottky diodes has been investigated after the highest RTA process at 900ºC. The diodes were tested in air ambient on wafer in a thermal chuck with a PMA KS40-1 temperature controller. The temperature ranges from room temperature (25ºC) up to 300ºC. The I-V curves were acquired using an HP4155B semiconductor parameter analyser. To get insights into the temperature dependence of Schottky diodes on different epilayer configuration (i.e. different blocking voltage range) we have investigated samples CQ3 and CB3. Figures 5.7 and 5.8 show the temperature behaviour of the J-V characteristics of the Ni/Ti-4H-SiC Schottky diodes on these two samples with different epilayer configuration.

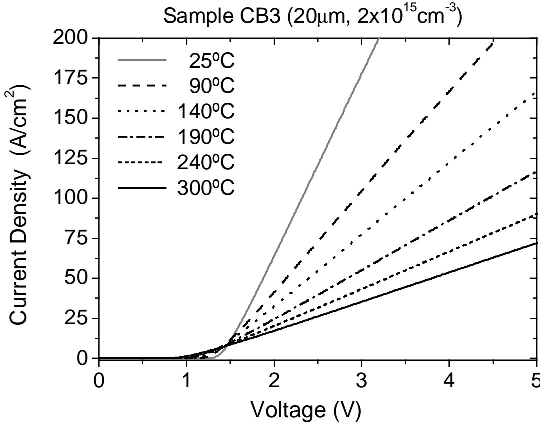


Figure 5.7 Forward J-V characteristics of Ni/Ti-4H-SiC Schottky diodes at different temperatures on sample CB3.

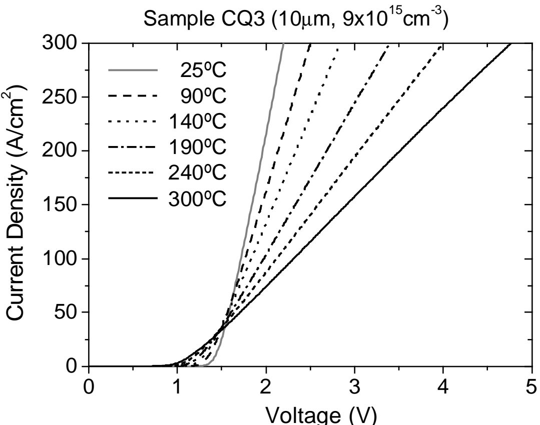


Figure 5.8 Forward J-V characteristics of Ni/Ti-4H-SiC Schottky diodes at different temperatures on sample CQ3.

As it can be observed in the above figures, at low forward bias values (up to ~1.5V), the current increases with the temperature, which is in agreement with the thermionic emission theory. Conversely, at forward bias higher than 1.5V the current decreases by increasing the temperature. This behaviour could be explained by an increase of on-state resistance with the temperature, due to a decrease in the electron mobility. As it can also be observed when comparing figure 5.7 with figure 5.8, the inflexion point where the temperature coefficient changes from positive to negative takes place for higher current density values in the higher doped and thinner sample. This effect also implies that the forward voltage drop at normal current density level (100 A/cm^2) exhibits a more pronounced increase for higher blocking designed epilayers.

Temperature dependence of the c-axis mobility in 4H-SiC Schottky diodes

The electron mobility along the c-axis of 4H-SiC can be determined by analysing the I-V characteristics of Schottky diodes measured as a function of the temperature. This procedure also enables to determine the temperature dependence of the mobility.

The specific on-resistance was determined and is reported in Figure 5.9 as a function of the absolute temperature T for the two samples examined. The on-resistance is given by the sum of the contributions $R_{on}=R_{epi}+R_{subs}+R_c$, where the three terms represents the resistances of the epilayer, of the substrate, and of the ohmic backcontact, respectively. In our case, the value of the specific contact resistance of the Ni/Ti backside ohmic contact was assumed to be in the range 10^{-4}-10^{-5} Ωcm^2, on the basis of previous measurements of specific contact resistance on this bilayer system [142]. On the other hand, we estimate a value of about 1×10^{-4} Ωcm^2 for the specific resistance of substrate, using the values of substrate doping and thickness provided by CREE and of the diode area. Therefore, within the experimental error, the contributions of the contact and of the substrate resistance can be neglected with respect to

that of the lightly doped epitaxial layer, thus allowing the approximation $R_{on} \cong R_{epi}$. Moreover, in our case, the effects of current spreading in the epilayer, already observed in SiC Schottky contacts [92], are a negligible source of error in the determination of the on-resistance values. In fact, with an epilayer layer thickness (10, 20 μm) much thinner than the Schottky contact diameter (200 μm), using the expression reported in [92], the reduction of the epilayer series resistance due to current spreading was estimated to be about 0.5-1%.

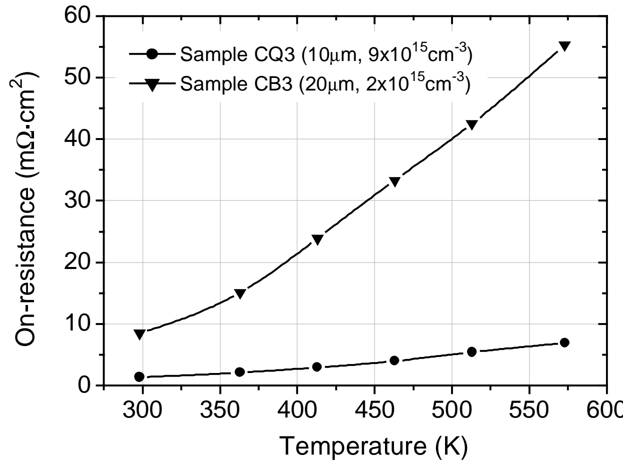


Figure 5.9 Specific on-resistance as a function of the absolute temperature for the two different samples investigated.

Hence, for the specific on-resistance, it holds

$$R_{on}(T) = \frac{t_{epi}}{q \cdot \mu_n(T) \cdot N_D(T)} \tag{5.3}$$

where N_D and t_{epi} are the concentration of ionised donors and the thickness of the epitaxial layer, respectively. In our temperature range, i.e. above 300K, for an epilayer dopant concentration in the range of $2\text{-}9\times10^{15}\text{cm}^{-3}$, almost complete ionisation (~98%) of the donor atoms is reached (see section 2.1.3 on chapter 2), and thus it is possible to assume $N_D(T)=N_D$ in equation 5.3. Therefore, the temperature dependence of the on-resistance in Eq 5.3 only arises from the dependence of the mobility on the temperature.

Based on these considerations, the mobility can be determined by inverting Eq 5.3. Since in Schottky diodes the current density J is almost parallel to the vertical direction, the mobility values measured in our samples using this procedure can be referred as the *c*-axis bulk mobility of 4H-SiC. Actually, taking into account a vertical electric field and a crystal off-axis angle of 8° would lead to mobility values about 15% larger than those found using Eq. 5.3. These corrected electron mobility μ_n values are reported as a function of the temperature in figure 5.10, which shows that in the range 300-573K the mobility decreases with increasing temperature.

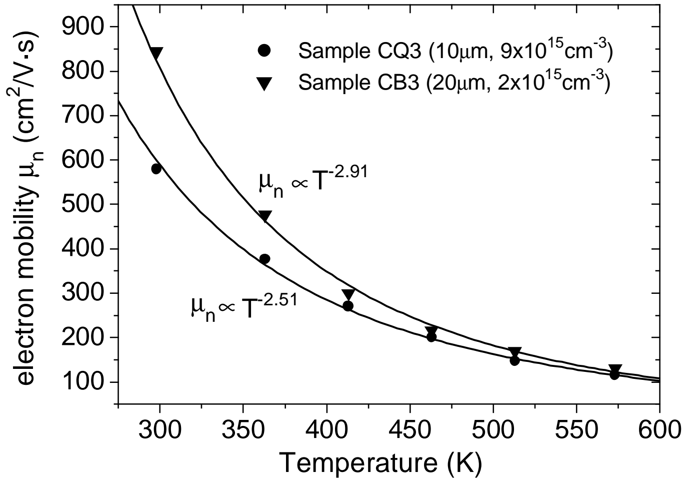


Figure 5.10 Electron mobility along the *c*-axis as a function of the absolute temperature for the two examined samples. The solid lines represent a fit to the experimental data (scatter points) according to the relation $\mu \propto T^{\alpha}$.

The value of the electron mobility obtained at room temperature was 845cm^2/Vs for the CB3 sample and 579cm^2/Vs for the CQ3 sample. The higher value is in reasonable agreement with the value of 725cm^2/Vs reported by Schaffer et al. [75] for lightly doped 4H-SiC electron mobility perpendicular to the *c*-axis, taking into account the anisotropy mobility relation $m_{\wedge c} = 0.83 \cdot m_{\parallel c}$ for 4H-SiC [80], thus confirming the validity of our procedure. The discrepancy of the CQ3 sample mobility value (579 cm^2/Vs) obtained is due to the fact that for such a low on-resistance value of the epilayer (~1mΩcm^2), the substrate resistance must be taken into account when performing the calculations. From CREE´s sample datasheet, the thickness and resistivity of the substrate are 350μm and 0.017Ωcm, respectively, resulting in a contribution from the substrate to the total on-resistance of about 0.5mΩcm^2. This value represents nearly a 40% of the measured on-resistance. Thus, subtracting the substrate resistance from the total on-resistance measured value and repeating the calculation procedure a value of 815cm^2/Vs is obtained for the CQ3 sample. This value is now in better agreement to the theoretical one for its doping range and to that obtained from CB3 sample. Besides, the substrate resistance becomes less significant as the temperature increases and this explains the much better agreement of mobility values in the two samples at high temperatures.

With increasing temperature the mobility decreases up to the value of 130cm^2/Vs at 573K in CB3 sample and 110cm^2/Vs in CQ3 sample (see Fig. 5.10). The variation of the mobility with temperature is described with a dependence as T^{α}. From a fit of the experimental data reported in Fig 5.10, it was found that $\mu_n \propto T^{-2.91}$ and $\mu_n \propto T^{-2.51}$ for CB3 and CQ3 samples, respectively. It must be pointed out here that when performing a new fitting to the CQ3 mobility data taken into account the substrate correction, the mobility exhibits a temperature behaviour of $\mu_n \propto T^{-2.89}$.

This behaviour is similar to the results obtained recently by Nakamura et al. [166] ($\sim T^{-3.2}$) by measuring the electrical characteristics of 4H-SiC high power Schottky diodes, Matsuura et al. [167] with Hall measurements ($\sim T^{-2.62}$) and by Mnatsakanov et al. [76] with an analytical approximation of the electron mobility in 4H-SiC ($\sim T^{2.6}$). Such a temperature dependence suggests that phonon lattice and intervalley scattering are the main limiting factors to the carrier transport [79,168].

5.2.3 Schottky breakdown voltage and reverse leakage current

Schottky diodes with single and double zone JTE structures were implemented in the mask set of diodes fabrication according to Figure 5.10. A Schottky diode with no edge termination structure was also designed for comparison. In this section it is reported the statistical breakdown results of the two different edge terminations on samples with the Ti/Ni Schottky barrier from wafer AD-0602-02 (Samples CQ1, CQ2 and CQ3). As Schottky diodes show a soft reverse breakdown, we take the breakdown voltage value as the voltage where the reverse current reaches the 5×10^{-6} A level, (i.e. 1.6×10^{-2} A/cm^2).

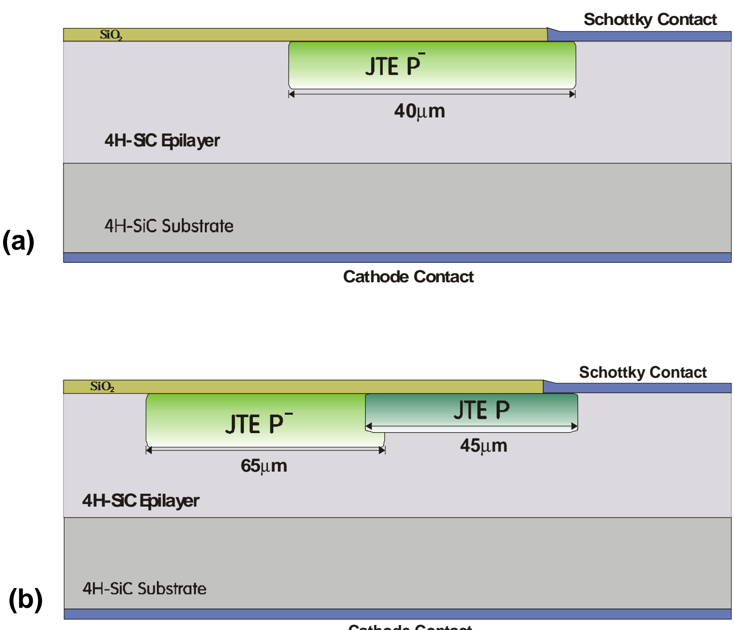


Figure 5.10 Schematic cross-section view of the two edge terminations implemented on Schottky diodes.(a) Single JTE structure (b) Double zone JTE structure.

Table 5.3 shows the statistical breakdown results and in Figure 5.11 the I-V characteristics of a representative diode for each termination structure on different samples are plotted. As it was explained in section 3.4.1 of chapter 3, the different contact RTA processes carried out on samples induced an increase of the Schottky barrier height with increasing RTA temperature which was also reflected on the reverse characteristics of Schottky diodes (see figure 3.13).

In Table 5.3 the Schottky barrier height and the temperature of the RTA carried out on the different samples are shown for comparison.

Table 5.3 Breakdown results on Schottky diodes with single or double JTE structure after different RTA process on different samples.

Sample	RTA process	Schottky barrier height	Termination Structure	Maximum V_{BR} (V)	Average V_{BR} (V)	Standard Deviation (V)
CQ1	400ºC 2min	Φ_B=0.85eV	1JTE	1150	1000	50
			2JTE	1200	1100	50
CQ2	700ºC 3min	Φ_B=1.10eV	1JTE	1425	1325	100
			2JTE	1500	1400	75
CQ3	900ºC 3min	Φ_B=1.25eV	1JTE	1500	1375	125
			2JTE	1625	1500	100

As it can be observed from the reported results on Table 5.3, the double JTE structure shows a higher blocking efficiency in comparison to the single JTE structure. The breakdown voltages of diodes with double JTE zone are about 100V higher than those with single JTE structure. It must be pointed out here that diodes without any termination structure show an average breakdown voltage of 150V in all three samples. The comparison of leakage current level between different samples with the same metallisation (Ni/Ti) and submitted to different RTA processes confirms the results obtained on a single sample (see Chapter 3, section 3.4.1). Therefore, reverse leakage current is shown to be sample independent. As it shown in Fig. 5.11, as the temperature of the RTA process increases the Schottky barrier also increases. This increase in the Schottky barrier height leads to a reduction of the reverse leakage current which is also reflected in an increase of the breakdown voltage. This dependence of leakage current on the barrier height is qualitatively consistent with thermionic emission theory. Additionally, this behaviour cannot be explained on the basis of leakage current associated with edge- or surface-generation since the magnitude of current components associated with these mechanisms would be independent of the barrier height.

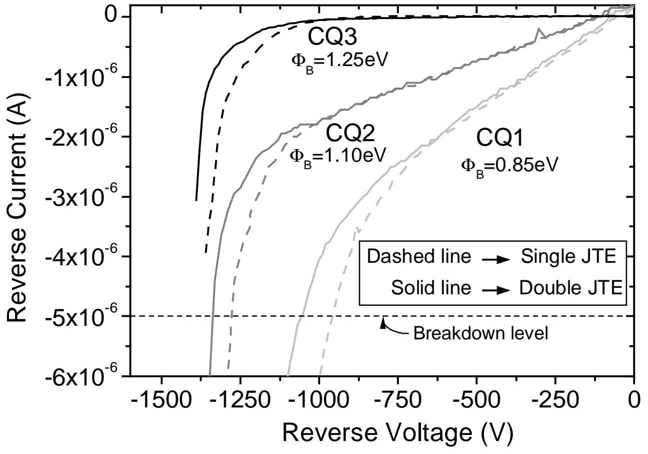


Figure 5.11 Reverse blocking I-V characteristics of Schottky diodes with single and double JTE structures on the three different samples with the Ni/Ti Schottky metallisation at different RTA temperature stage.

The basic reverse leakage current mechanisms of a Schottky rectifier are (a) thermionic emission, (b) thermionic field emission, (c) field emission, and (d) generation in the depletion region [143]. In addition to these basic mechanisms, surface leakage and defect related leakage may occur. Real world devices likely contain current caused by more than one of these mechanisms. The dominant mechanism depends on the Schottky barrier height, temperature, and applied bias. However, the relationship for depletion region generation reverse leakage current,

$$J_G = \frac{qn_iW}{2t_r} \tag{5.4}$$

where n_i is the intrinsic carrier concentration, W is the depletion width, and τ_r is the lifetime within the depletion region, makes the reverse leakage current caused by generation in the depletion region negligible due to the very small value of the intrinsic carrier concentration (n_i) in SiC.

In the case where thermionic emission is the dominant current component (as it is usually the case for lightly doped epilayers) it is affected by barrier lowering due to image force and the reverse saturation current can be expressed as

$$J_S = -A^*T^2\, exp\left(\frac{-q(\Phi_B - \Delta\Phi_B)}{k_BT}\right) \tag{5.5}$$

where $\Delta\Phi_B$ is the decrease in Schottky barrier height due to image force and it can be written in terms of the maximum electric field at the metal-semiconductor junction (E_M) as

$$\Delta\Phi_B = \sqrt{\frac{q \cdot E_M}{4 \cdot p \cdot e_S}} \tag{5.6}$$

Figure 5.12 shows the barrier height lowering as a function of the applied reverse bias for two different epitaxial doping level.

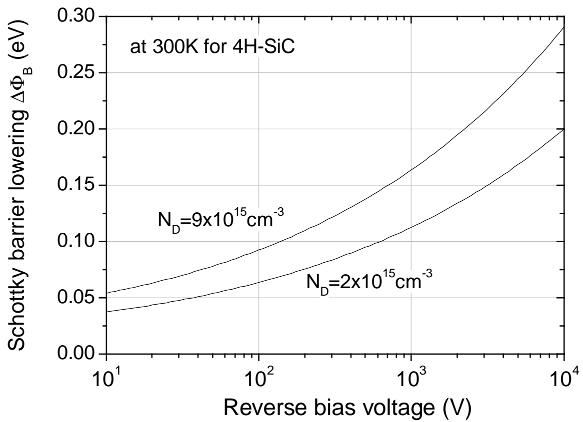


Figure 5.12 Schottky barrier lowering as a function of the applied reverse bias.

Experimental reverse leakage current in SiC Schottky diodes has been reported to be orders of magnitude higher than that predicted by thermionic emission model and a stronger voltage dependence than that given by the image-force induced barrier lowering. In our Schottky diodes, the magnitude of the reverse leakage current density predicted by thermionic emission theory is much less than the magnitude of the experimental reverse leakage current density, as it can be seen in Fig 5.13 where the experimental data are plotted together with the theoretical leakage current density predicted by thermionic emission theory accounting for the image barrier lowering effect (Eq. 5.5). The experimental data of sample CQ3 is not plotted because the leakage current level was below the experimental detection limit (20×10^{-9}A) over a wide range of reverse voltages (up to 800V approximately) due to the higher Schottky barrier height.

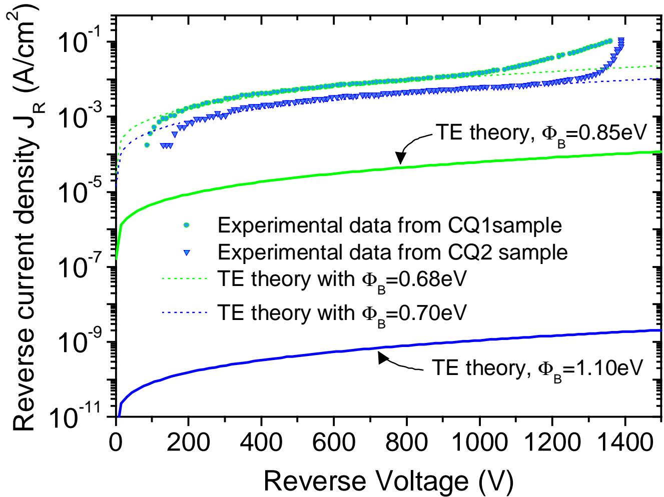


Figure 5.13 Experimental (scatter) and TE theoretical (solid lines) reverse leakage current density for samples CQ1 and CQ2. Dotted lines are fitted curves adjusting the Φ_B value.

However, the voltage dependence of the leakage current fits very well with that predicted by thermionic emission theory with a lower barrier height value than that extracted from forward I-V characteristics. A possible explanation of this behaviour is based upon the presence of localized defects in the epitaxial layer at the SiC/metal interface which may lower the barrier height of the Schottky contact at the defect site, as it will be explained in detail in section 5.2.3.2.

To explain the larger magnitude of the experimental reverse leakage current in Schottky diodes in comparison to that predicted by thermionic emission including the image-force barrier lowering effect, two different mechanisms are proposed: i) the contribution from thermionic field emission and field emission (tunnelling mechanisms)[169,170], ii) the effect of barrier height fluctuations or surface inhomogeneities [171-173]. In the next sections we will analyse the possible contribution of this two mechanisms to the experimental reverse leakage current observed in our Schottky diodes.

5.2.3.1 Leakage current from tunnelling mechanisms

Thermionic field emission (TFE) and field emission (FE) are typically not considered to contribute to the reverse leakage current of moderately and lightly doped Si Schottky rectifiers. However, the large critical field of SiC increases the likelihood of substantial thermionic field emission and field emission in SiC Schottky rectifiers. Both TFE and FE are tunnelling mechanisms that depend on the barrier height and width. The difference between TFE and FE is that thermionic field emission is the tunnelling of electrons thermally excited above the Fermi level of the metal while field emission is the tunnelling of electrons at the Fermi level of the metal. Hence, TFE will depend on temperature and FE will be independent of temperature.

The relationship between tunnelling current density and electric field for a triangular barrier may be expressed in terms of the electric field (E_M) and the Schottky barrier height (Φ_B) [143]

$$J_T \propto E_M^2 \, exp\left(\frac{-8p\sqrt{2m^*}\Phi_B^{3/2}}{3hqE_M} \right) \tag{5.7}$$

where m^* is the electron effective mass, and h is the Planck´s constant. The relationship between electric field and tunnelling current density may be demonstrated by plotting (Fowler-Nordheim plot)

$$ln\left(\frac{J_R}{E_M^2} \right) \propto \frac{1}{E_M} \tag{5.8}$$

Figure 5.14 shows the Fowler-Nordhiem (FN) plot of the previously reported reverse J-V characteristics from Schottky diodes in samples CQ1 and CQ2.

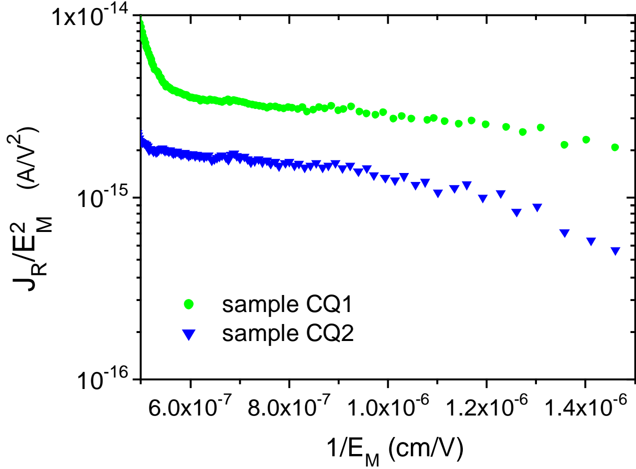


Figure 5.14 FN plot of the reverse characteristics of Schottky diodes in samples CQ1 and CQ2.

From Fig. 5.14, a weak dependence between the electric field at the metal-semiconductor junction and reverse leakage current is observed. Thus, it is suggested that both TFE and FE play a secondary role in the origin of the reverse leakage current of our diodes, at least up to the onset of breakdown. This assumption also gives support to the high efficiency of the implemented edge terminations (single or double JTE) on alleviating the electric field near the contact edges.

5.2.3.2 Leakage current from surface inhomogeneities

A model based upon the presence of localized defects in the epitaxial layer at the SiC/metal interface which may lower the barrier height of the Schottky contact at the defect site has been also proposed to explain the high leakage current observed in SiC Schottky rectifiers. The model of non-uniform barrier height is shown in Fig. 5.15.

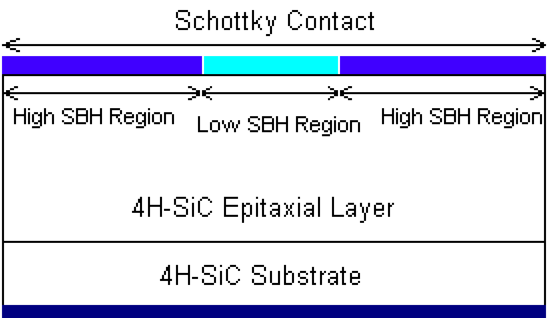


Figure 5.15 The model for metal/4H-SiC Schottky diode with non-uniform barrier height (SBH denotes Schottky barrier height).

In this structure, two regions of the metal/SiC interface are identified. The high-SBH (HSBH) region is the defect free SiC/metal interface were the barrier height is equal to the value obtained by I-V measurements on the actual 4H-SiC Schottky diodes. The region where lowering of the barrier height occurs is identified as the low-SBH region (LSBH) region. The ratio of the area of the low-SBH region to the total diode area is defined as Z. In the analytical approach of this model it is assumed that these two regions with different barrier height are equivalent to two Schottky diodes connected in parallel, thus neglecting the discontinuity in the potential profile at the boundary of the low-SBH and high-SBH. The total saturation current density of the Schottky contact is then given by

$$J_S = J_S^L \cdot Z + J_S^H \cdot (1 - Z) \tag{5.9}$$

where J_S^L and J_S^H are the saturation current density through the LSBH and HSBH regions, respectively. Saturation current density of the HSBH and LSBH regions are calculated by using Eq. 5.5 with an appropriate barrier height. The difference in the barrier height of the

LSBH (Φ_{BL}) and HSBH (Φ_{BH}) regions is defined as $\delta\Phi_B$. For modelling the room temperature *J-V* characteristics, calculations were carried out for $\delta\Phi_B$ ranging from 0.1-0.4eV and Z in the range of 0.001 to 0.1. The ratio of the saturation current density of a device with a defect modelled as SBHI (J_{SBHI}) to the saturation current of a defect free diode (J_{IDEAL}) is defined as R_{JS}. Figure 5.16 shows the variation in R_{JS} for a diode with a Φ_{BH}=0.85eV (corresponding to the barrier height of as-deposited Ti) as a function of $\delta\Phi_B$ and Z. In this case, J_{IDEAL} was calculated using Eq. 5.5 with Z being equal to zero.

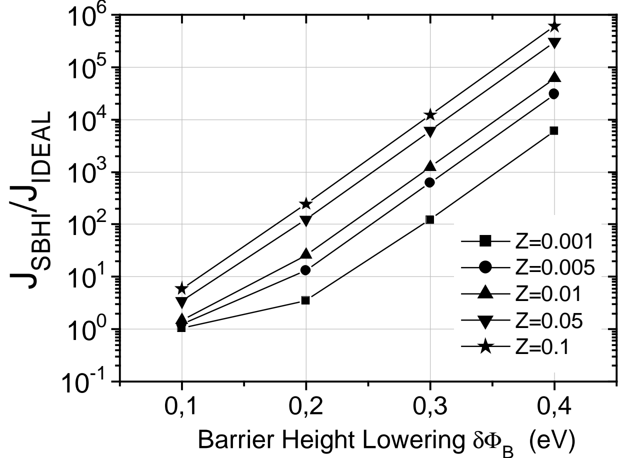


Figure 5.16 Variation in the ratio of the leakage current through a 4H-SiC Schottky diode with SBHI to that of an ideal device as a function of the SBHI parameters (Schottky barrier lowering $\delta\Phi_B$ and area ratio Z).

For a given temperature and Z, R_{JS} strongly increases with $\delta\Phi_B$ and even for a small Z such as 0.01, it is as high as ~26 and ~1230 for a $\delta\Phi_B$ of 0.2eV and 0.3eV, respectively. In fact for a device with large $\delta\Phi_B$, most of the reverse leakage current flows through the defective region and the contribution from the high-SBH region is minimal.

It was found that the influence of SBHI on the forward I-V characteristics is negligible except at very small biases. For small values of the on-state bias, the current was found to be higher for devices with Schottky barrier height inhomogeneity as compared to the ideal devices. However, as the voltage was increased, the contribution of the current component from LSBH region decreased due to the influence of the resistance of the epitaxial layer. For current densities above 1A/cm^2, the difference in the on-state current for the diodes with and without SBHI was negligible. Thus, the proposed model results in a large increase in the reverse leakage current without significantly altering the forward I-V measurements.

Though, this analytical model is adequate to illustrate the effects of SBHI parameters on the reverse I-V characteristics, it is not an accurate model to simulate the spatial variation in barrier height across a Schottky contact. This is due to the fact that in this model the potential discontinuity at the boundary of the low-SBH and the high-SBH was ignored. In fact, since a

small region of the low SBH contact is surrounded by a large area contact with higher SBH, it is expected that the potential profile in the region with lower barrier height would be influenced by the region with higher SBH. This would result in the potential distribution under the low-SBH contact to be different from the case where the entire contact was a low-SBH contact. So, the potential profile under the low-SBH region would tend to be similar to that under the high-SBH region and this would result in a pinch-off of the low-SBH region [144]. Thus, it would no longer be possible to assume that the low-SBH and the high-SBH regions are equivalent to two parallel Schottky contacts to SiC with different barrier height and it would be necessary to include the pinch-off effect in calculating the electrical characteristics of diodes with Schottky barrier height.

In order to take into account the aforementioned pinch-off effect, numerical simulations were carried out for Schottky structures similar to the one shown in Fig. 5.15 using the 2D numerical device simulator MEDICI with the appropriate modifications in various models parameters indicated in Chapter 2 to simulate the 4H-SiC based devices.

To simulate 4H-SiC Schottky contacts with regions of Schottky barrier height inhomogeneity, low-SBH regions were assumed to be in the center of the high-SBH regions. This was achieved by specifying two separate Schottky contacts with different metal work functions (Φ_M) to the 4H-SiC epitaxial layer. Since the two metal contact were physically separated, a gap was present between the two contacts. In order to prevent any distortion in the potential profile due to this gap, a grid spacing of about 10**Å** was used at the boundary of the low-SBH and high-SBH regions. For these simulations, the epitaxial layer doping and thickness were 9×10^{15}cm^{-3} and 10μm, respectively. The metal workfunction of the defect-free region (Φ_{MH}) was 5.3eV, the electron affinity of SiC was set equal to 3.9eV, $\delta\Phi_M$ was taken as 0.4 and 0.8eV and a linear geometry device with different area ratio Z was used.

Figs. 5.17 and 5.18 show the simulated forward and reverse J-V characteristics of a 4H-SiC Schottky diode at 300K with a $\delta\Phi_M$ of 0.4eV and Z=0.001.

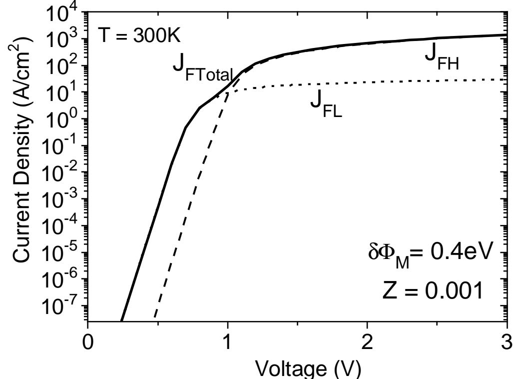


Figure 5.17 Forward J-V characteristics at 300K of a 4H-SiC Schottky diode with a Schottky barrier inhomogeneity of $\delta\Phi_B$=0.4eV and Z=0.001.

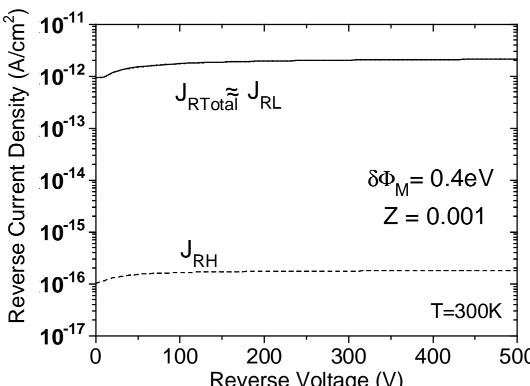


Figure 5.18 Reverse J-V characteristics at 300K of a 4H-SiC Schottky diode with a Schottky barrier inhomogeneity of $\delta\Phi_B$=0.4eV and Z=0.001.

During on-state conduction, at very low on-state biases, most of the leakage current flows through the LSBH region and the total on-state current is approximately equal to J_{FL}. However, at higher on-state biases, the voltage drop across the epitaxial layer resistance becomes large for the low-SBH region due to its higher on-state current density and thus, J_{FL} tends to saturate much faster than J_{FH}. As Z decreases the saturation occurs at lower current densities, thus increasing the "bulky" effect on total J-V characteristics. Based on these simulations it is concluded that at on-state biases greater than 1V, the on-state behaviour of the Schottky contact with the Schottky barrier height inhomogeneity is identical to that of a defect-free device.

From Figure 5.18 it is clear that even for a Schottky barrier height inhomogeneity with small $\delta\Phi_B$ and Z, J_{Rtotal} is dominated by the current flowing through the LSBH region. For a diode with a SBHI region of $\delta\Phi_B$ of 0.4eV and Z ~0.001, the simulated leakage current density is ~2×10^{-12}A/cm^2 at a reverse bias of 500V. For a defect-free diode, this value is ~1.75×10^{-16} A/cm^2. As expected the ratio of J_{RL} to J_{RH} at any given bias was found to increase with increasing $\delta\Phi_B$.

Figure 5.19 shows the experimental J-V curves at 300K in a semilog plot of a representative Schottky diode from sample CQ2 after the different RTA processes carried out. MEDICI simulations were performed to fit the experimental curves according to the proposed model and are also plotted in Fig. 5.19. This fitting procedure allows us to obtain the values of Z and $\delta\Phi_B$ of our processed Schottky diodes.

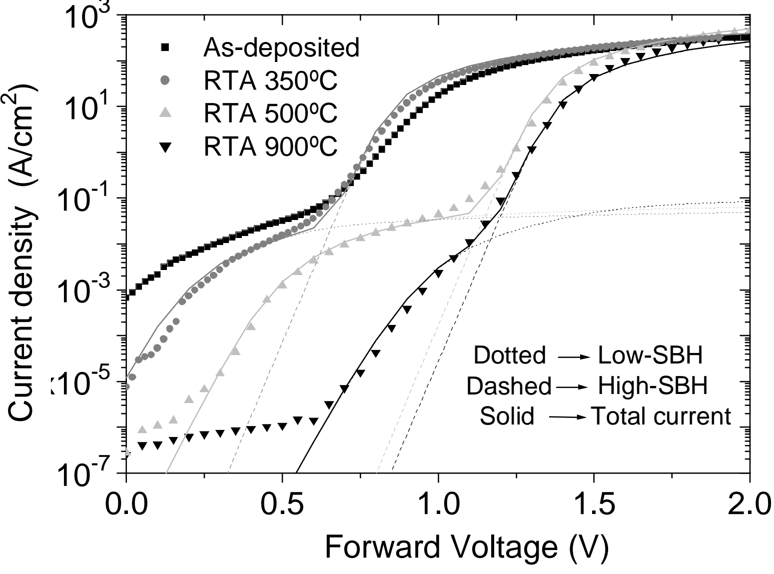


Figure 5.19 Experimental J-V characteristics of a Schottky diode after different RTA processes (scatter points) and simulated curves to fit each experimental curve according to the inhomogeneity barrier model proposed (solid lines). Dotted and dashed lines represent the contribution from LSBH and HSBH regions, respectively.

The difference in the barrier height of the LSBH and HSBH regions ($\delta\Phi_B$) lies between 0.5 and 0.6eV for our analysed curves and the ratio of the area of the low-SBH to the total diode area Z is approximately the same for all analysed curves and equal to ~1×10^{-5}. Thus, the observed reduction in leakage current with increasing temperature of the RTA of Schottky contact can be attributed not only to the previously reported increase of the HSBH, but also to the increase of the barrier height on LSBH regions, as it can be qualitatively seen in Fig. 5.19.

Various phenomena have been considered to be responsible for SBH inhomogeneities. For example, difference in the crystal symmetry of the metal with respect to the semiconductor or variation in the orientation at the metal-semiconductor interface, due to localized faceting of the interface has been observed. Mixture of different metallic phases with different SBH's, doping inhomogeneity, dopant clustering, and contaminations are other features which can lead to SBH inhomogeneities [174].

However, recent studies [175,176] indicate that there is no correlation between some extended material defects (screw or edge dislocations) and the excessive leakage current observed in SiC Schottky diodes. It has also been suggested [177] that the step bunching of the surfaces after the high temperature activation anneal (>1500ºC) may be related to the high leakage currents.

5.2.4 High temperature reverse performance

The reverse bias characteristics as a function of the operating temperature of a Ni/Ti/4H-SiC Schottky diode from sample CQ2 after the highest RTA at 900ºC are shown in Fig. 5.20. The plot clearly shows how the leakage current increases as the diode temperature increases, in accordance with thermionic emission leakage current mechanism. The typical reverse current is less than 5µA at 1000V at 25ºC which increases to 20µA at 300ºC, a very nominal increase for such a wide temperature range. Thus, the reverse voltage at which the diode's leakage current attains a specific value will be reduced as the temperature increases.

These Schottky diodes have shown good stability in reverse mode from the thermal point of view (thermal runaway) and are able to operate up to 300ºC. The above results indicate that high-temperature operation with a high blocking voltage and a low-power loss can be realized utilizing Ni/Ti/4H-SiC Schottky rectifiers with edge termination formed by Al^+ implantations.

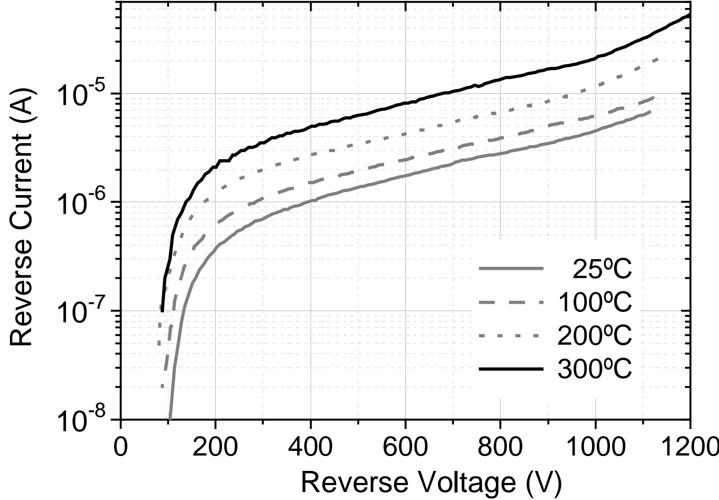


Figure 5.20 Reverse leakage current dependence on operating temperature of a Schottky diode with single JTE from sample CQ2 after the 900ºC RTA.

5.2.5 Schottky conclusions

4H-SiC Schottky diodes have been fabricated using a Ni/Ti bilayer metalisation submitted to sequential different RTA temperatures. Good forward performance is achieved after RTA at 350ºC on all processed samples, with on-resistances close to the theoretical values. The diodes have shown good thermal stability after the 900ºC RTA and measurements at temperatures up to 300ºC have shown the increase of diode forward voltage drop with increasing temperature commonly obtained on similar devices and mainly due to epitaxial layer resistance increase versus temperature that yield an ease of device paralleling.

Concerning the reverse characteristics, the reverse leakage current has been proved to follow the thermionic emission theory showing a decrease in reverse leakage current level with increasing Schottky barrier height. For the highest Schottky barrier height (Φ_B=1.25eV) after the 900ºC RTA a low leakage current density level of 1.6×10^{-4} A/cm^2 at a reverse bias of 1000V is achieved. Besides, this leakage current reduction leads to higher breakdown voltages, reaching values near 85% of the ideal 1D-plane-parallel breakdown on diodes with double zone JTE structure. However, the leakage current level is shown to be orders of magnitude higher than that predicted from thermionic emission theory including the Schottky barrier lowering effect, as it is usually observed on SiC Schottky diodes. This high leakage current level has been associated to surface inhomogeneities of the Schottky contact. Moreover, these Schottky barrier non uniformities are also consistent with the "bulky" effect observed on forward I-V characteristics. Finally, high temperature reverse measurements have shown a good thermal stability for operating temperatures up to 300ºC.

5.3 JBS Diode Performance

5.3.1 Specific on-resistance and forward voltage drop

During forward conduction in the JBS diode the current flows unipolar between the anode and the cathode in channels between the p^+n junctions. Consequently, in normal operation ($100 A/cm^2$) the Schottky current dominates and the forward current analysis can be based on thermionic emission theory for Schottky junctions.

For a JBS diode the relationship between the forward voltage drop and the current density is equal to that of a Schottky diode (Equation 5.2), except that the expression has to be modified to allow for the area taken up by the p^+ regions in the structure, see Figure 5.21. The total resistance which is a large contribution of an increasing voltage drop in JBS is the sum of the resistance in grid (R_{grid}) , in the drift layer ($R_{drift,JBS}$), in the substrate (R_{subs}), and at backside ohmic contact (R_c) as shown in Fig. 5.21. The contribution of backside ohmic contact to the voltage drop might be small (typically 1 mV at 100 A/cm) and can be ignored. Although the substrate resistance is not a negligible contribution to the total on-resistance for relatively low blocking voltage epilayers (as it was shown in section 5.2.2), we will not take it into account in the calculations for simplicity.

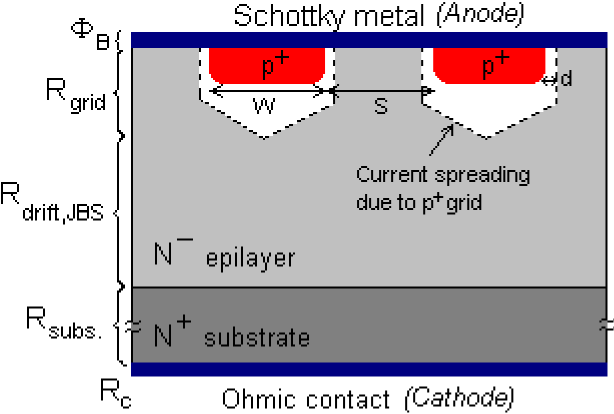


Figure 5.21 Schematic draw of a part of a JBS grid showing the main contributions to the total forward voltage drop over the diode.

The current density across the Schottky barrier J_{FS} will be modified to,

$$J_{FS} = \frac{A_{total}}{A_{Schottky}} J_F \tag{5.10}$$

where J_F is the total current density over the metal contact. For a stripped p^+ grid design the area relation between total contact area and Schottky area is:

$$A_{total} = \frac{s+w}{s-2d} A_{Schottky} \tag{5.11}$$

where w is the width of the p^+ regions and s is the spacing in between, i.e., the Schottky area region. d is the junction depletion width from the p^+ regions. If a 45 degree current spreading is assumed below the channels the JBS drift resistance $R_{drift,JBS}$ can be written as in Eq. 5.12 (with homogeneous current conduction assumed).

$$R_{driftJBS} = \frac{\left(t_{epi} - x_j - \frac{w}{2}\right)}{q\mathbf{m}_n N_D} \tag{5.12}$$

where t_{epi} is the total epilayer thickness and x_j is the p^+ grid depth. Resistive contribution from the p-type channels and current spreading is given by,

$$R_{grid} = \left(\frac{x_j + \frac{w}{2}}{q\mathbf{m}_n N_D}\right)\left(\frac{s+w}{s+2d}\right) ln\left(\frac{s+w}{s-2d}\right) \tag{5.13}$$

The total JBS on-resistance is the sum of R_{grid} and $R_{drift,JBS}$:

$$R_{on,JBS} = R_{grid} + R_{drift,JBS} \tag{5.14}$$

Now the forward voltage drop of a JBS diode can be written by modifying Eq.5.2 with Eqs 5.11 and 5.14:

$$V_{F,JBS} = \frac{nk_B T}{q} ln\left(\frac{(s+w)}{(s-2d)}\frac{J_F}{A^* T^2}\right) + n\Phi_B + R_{on,JBS} J_F \tag{5.15}$$

With Eq. 5.15 the forward conduction characteristics can be calculated. For an exact analysis, an iterative procedure is required because of the dependence of d on the forward voltage drop. In the case of JBS intended for operation at very low forward voltage drops, the depletion layer width can be assumed to be constant allowing a closed-form analytical solution of the forward conduction characteristics by using Eq. 5.15. However, for forward voltages higher than the built-in voltage it can be assumed that d≈0μm.

With the mask set design shown in Chapter 3, JBS diodes with different concentration in the p-type region (p^+=2×10^{19}cm^{-3}, p=2×10^{18}cm^{-3} and p^-=2×10^{17}cm^{-3}) were fabricated, to evaluate the impact of this parameter on the forward and reverse characteristics. The three p-type regions were formed by the Al^+ implantations analysed in section 3.2.1 of Chapter 3. The p-type grid layout of the JBS structure of our diodes was designed with circular concentric rings 6μm wide spaced 6μm between them (w=6μm, s=6μm), thus obtaining a 50% area of Schottky regions. To achieve high blocking voltages, the same optimised single junction termination extension was implemented in the three types of diodes. Figure 5.22 shows an optical photo of the processed JBS diodes before the Al^+ JTE implantation.

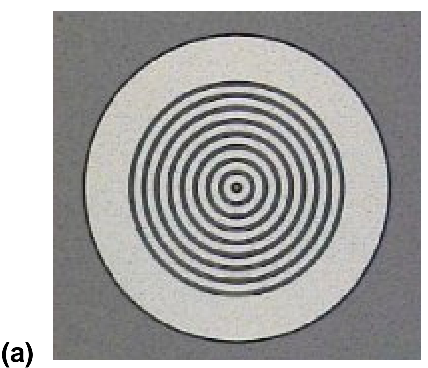
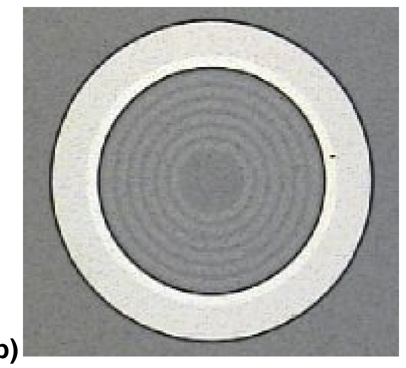
(a) 
(b) 

Figure 5.22 Optical photography of two processed JBS diodes showing the concentric grid layout (a) JBS diode with P^- grid (b) JBS diode with P^+ grid. The wide white outer zone on both diodes corresponds to the designed JTE region.

To determine the effectiveness of the JBS diode design, it is important to compare the on-state voltage and reverse bias I-V characteristics of Schottky diodes, JBS diodes and PiN diodes fabricated on the same wafer. Table 5.4 shows the characteristics electrical parameters, such as the forward voltage drop at 100A/cm^2 (V_F), Schottky barrier height (Φ_B), and specific on-resistance (R_{on}), of the three types of JBS diodes and Schottky diodes extracted from I-V measurements after each RTA process of the analysed sample (CQ2).

Table 5.4 Electrical properties of JBS with p^+ (2x10^{19}cm^{-3}), *p* (2x10^{18}cm^{-3}) and p^- (2x10^{17}cm^{-3}) grid doping concentration and Schottky diodes under different RTA processes.

	JBS diodes (p^+ grid)			**JBS diodes (*p* grid)**			**JBS diodes (p^- grid)**			**Schottky diodes**		
RTA Temp. (3min)	**V_F [V]**	**F_B [eV]**	**R_{on} [mWcm^2]**	**V_F [V]**	**F_B [eV]**	**R_{on} [mWcm^2]**	**V_F [V]**	**F_B [eV]**	**R_{on} [mWcm^2]**	**V_F [V]**	**F_B [eV]**	**R_{on} [mWcm^2]**
As-depo.	1.47	0.78	2.9	1.53	0.78	3.3	1.61	0.79	4.3	1.28	0.77	2.4
350ºC	1.21	0.83	2.4	1.25	0.84	3.0	1.35	0.85	3.8	1.10	0.85	1.8
500ºC	1.58	1.12	1.7	1.61	1.14	2.3	1.69	1.13	3.1	1.52	1.10	1.5
700ºC	1.64	1.17	1.9	1.66	1.17	2.5	1.75	1.19	3.2	1.61	1.15	1.7
900ºC	1.65	1.25	1.9	1.68	1.25	2.6	1.77	1.26	3.3	1.61	1.25	1.8

As showed in section 3.4.2 of Chapter 3, the contact becomes ohmic after annealing at 500ºC and it improves its ohmic characteristic significantly after RTA at 700ºC achieving a low contact resistivity value of $1\cdot10^{-5}\Omega\cdot cm^2$. This low contact resistivity is also reflected in the lowering of the p^+ grid resistance of JBS diodes, whose forward voltage drop and on-resistance approach that of Schottky diodes.

As it can be observed from results shown in Table 5.4, as the doping level of the p-type regions in JBS diode decreases, the diode on-resistance increases. Thus, JBS diodes with p^+ ($2\times10^{19}cm^{-3}$) grid doping level show lower on-resistances than JBS diodes with p doping level grid ($2\times10^{18}cm^{-3}$), and at the same time, diodes with p^- grid ($2\times10^{17}cm^{-3}$) show on-resistances higher than those with p level grid. As at low forward bias (below 3V), the current flows by unipolar conduction through the Schottky regions, the p-type doping level should not

influence the forward characteristics. However, an interesting point is the fact that the different p-type doping levels also have different depths, as can be seen in the implantation profiles shown in Chapter 3 section 3.2.1. Thus, the implanted p-type doping depth was increased for lower p-type doping concentrations.

Simulations were performed in order to clarify if the on-resistance increase is due to the p-type doping level or to the p-type doping depth. Figure 5.23 shows the simulated current density distribution at an applied forward bias of 2.5V for a JBS diode with two different doping depths (0.5 μm and 1.5 μm) but same doping level ($2\times10^{19}cm^{-3}$) in the p-type grid. The simulated structure consists of a 6μm Schottky contact region (with a defined metal workfunction of 5.3eV) and two ohmic contacts over p^+ ($2\times10^{19}cm^{-3}$) doped regions 6μm wide at both sides of the Schottky contact.

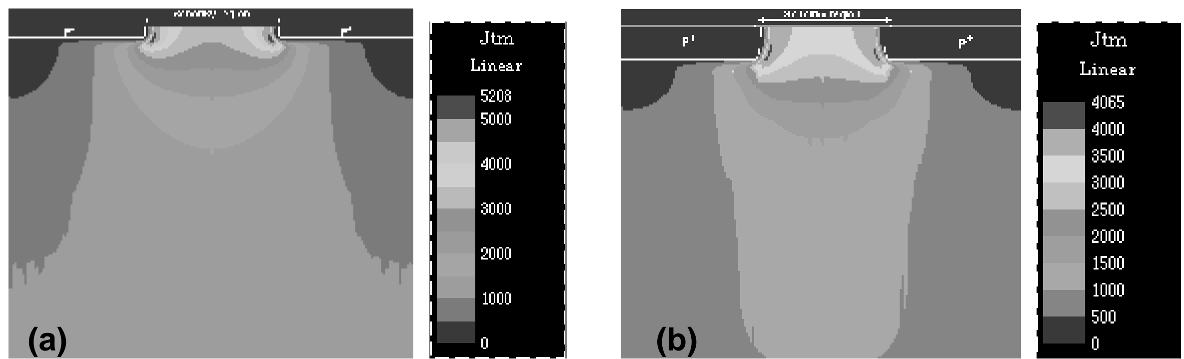


Figure 5.23 Simulated obtained forward current density distributions for JBS diodes with two different doping depths of the P^+ regions. (a) P^+ depth of 0.5μm, (b) P^+ depth of 1.5μm.

From simulations, it was observed that JBS diodes with deeper doping profiles in the p-type grid showed lower current densities (i.e. higher on-resistances) due to lower current spreading, as can be observed in Fig. 5.23. Due to the low forward bias applied (2.5V) the current flows from unipolar conduction through the Schottky contact. When the doping level was decreased in the p-type regions, no difference was observed in the current density distribution with respect the higher doping level simulations. Thus, it can be concluded that the experimental increase of on-resistance in JBS diodes with different doping profiles in the p-type grid is due to the increase of doping depth for lower p-type doping concentrations. This behaviour also confirms the theoretical predictions from equation 5.13.

5.3.2 Bipolar injection through the p^+ regions

If the potential drop under the Schottky contact exceeds the built-in potential of the *pn* junctions, minority carriers are injected into the low doped drift zone leading to conductivity modulation, this is the high-current operation mode of the JBS rectifier. Figure 5.24 shows an example of a JBS with p^+ grid diode from sample CQ2 with current injection from the p^+n junction for forward voltages V>3.0V.

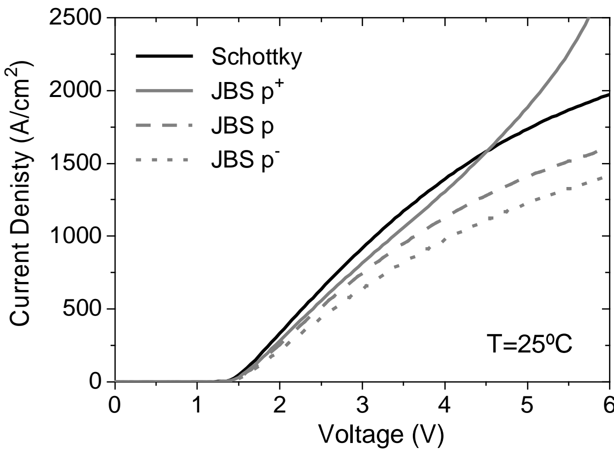


Figure 5.24 J-V characteristics at room temperature of the three different JBS diodes fabricated. The J-V curve of a Schottky diode is also shown for comparison.

The capability to handle high current pulses is a requirement in most application circuits. Schottky diodes have, due to the constant differential on-resistance characteristics, excessive high forward voltage and associated high thermal heating. Schottky diodes may experience permanent damage already in the single kA/cm^2 range. Typical applications, however, may require 2-20 kA/cm^2 of non repetitive pulses of up to 20 milliseconds. The JBS diode has the potential to show better high current characteristics than a Schottky diode if the p^+ grid could start to inject current at a certain forward voltage and thereby obtain bipolar operation for high current pulses. In our fabricated JBS diodes with p^+ grid, bipolar operation is demonstrated for a forward voltage higher than 3.0V, as it can be observed from the J-V characteristics in Figure 5.24. This minority carrier injection is also confirmed by the electroluminescence effect produced by the p^+n regions on the boundary of the JBS diode, as it can be seen in the photo shown in Figure 5.25.

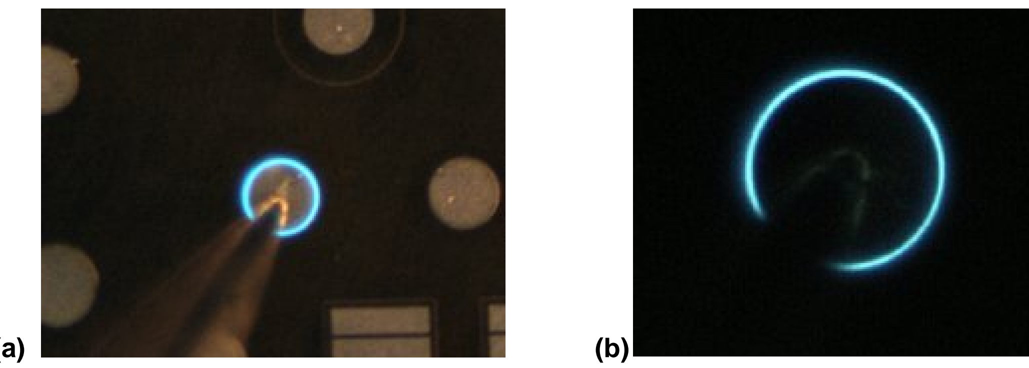


Figure 5.25 Injection electroluminescence graphs for a JBS diode with p^+ grid. The p^+n region on the boundary of the device inject minority carriers at voltages higher than 3.0V. The pictures are taken at an applied forward bias of 5V, (a) general view, (b) zoom approach.

The bipolar conductivity was achieved due to the good ohmic contact formed on the p^+ grid of the JBS diode. JBS diodes with lower implantation dose in the p-type grid were proved to behave like a Schottky diode with higher on-resistance (see Figure 5.24), thus showing insufficient hole concentration to start the carrier injection at low forward biases, even at high temperatures, as it will be shown in the next section. This result reinforces the idea that a good activation of the implanted impurities and the consistent formation of a good ohmic contact are crucial to be able to obtain good surge current capabilities in JBS diodes.

5.3.3 High temperature forward performance

After the 900ºC contact RTA, forward I-V measurements were carried out from room temperature up to 300ºC on the three types of JBS diodes and the obtained characteristics are shown in Figure 5.26.

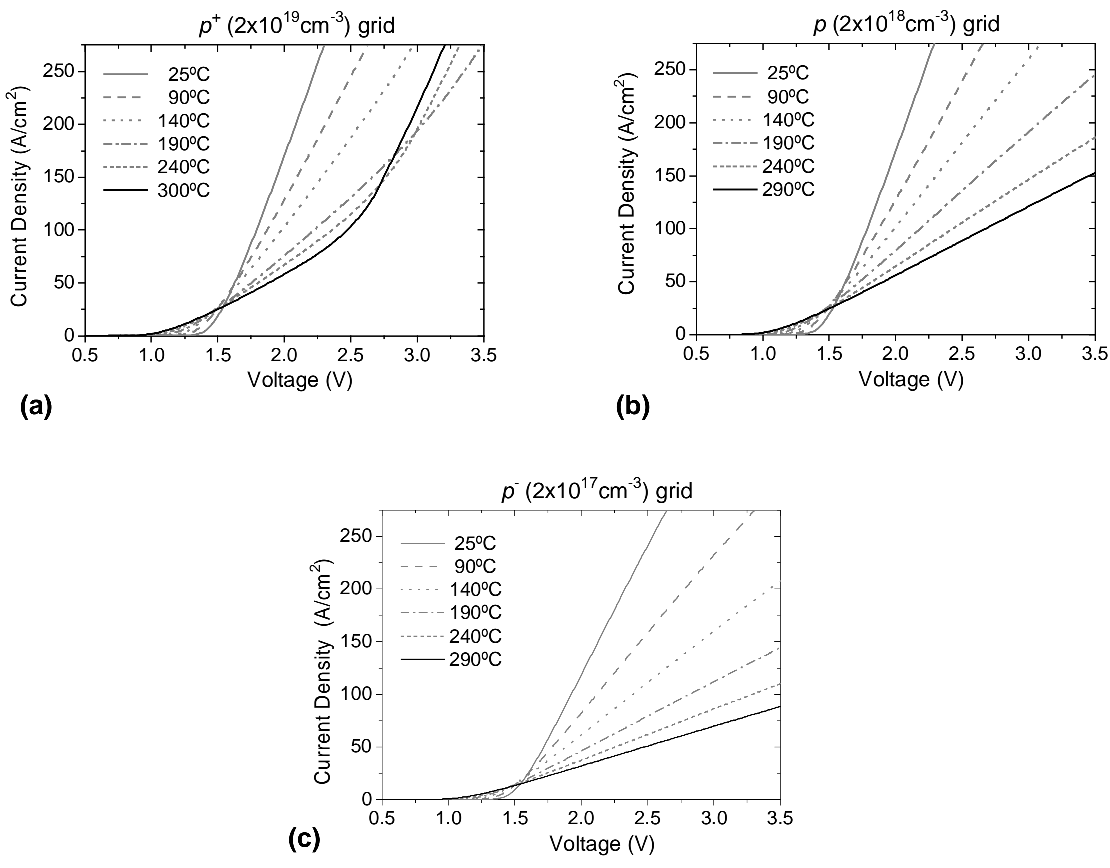


Figure 5.26 J-V characteristics at different temperatures (up to 300ºC) for the three different JBS diodes: (a) with p^+ grid, (b) with p grid, and (c) with p^- grid doping level.

As it can be observed from the above figures, only the JBS diodes with p^+ grid are able to start the minority current injection from the p-type regions even at high temperature. JBS diodes with p or p^- doping in the p-type grid regions behave like a Schottky diode with a higher on-resistance due to the p-type grid. It can also be noted that as the temperature

increases the bipolar conductivity modulation from p^+ grid starts at lower forward bias due to the decreased built-in voltage and increased carrier lifetime at elevated temperatures. Thus, the temperature dependence is shifted from unipolar positive to bipolar negative accordingly to the different current conduction mechanisms.

Figure 5.27 shows the comparison of on-state J-V characteristics at room temperature and at 300ºC of the three type of JBS diodes fabricated (p^+, p and p^- grid doping level) together with that of Schottky diodes fabricated on the same wafer sample (CQ3).

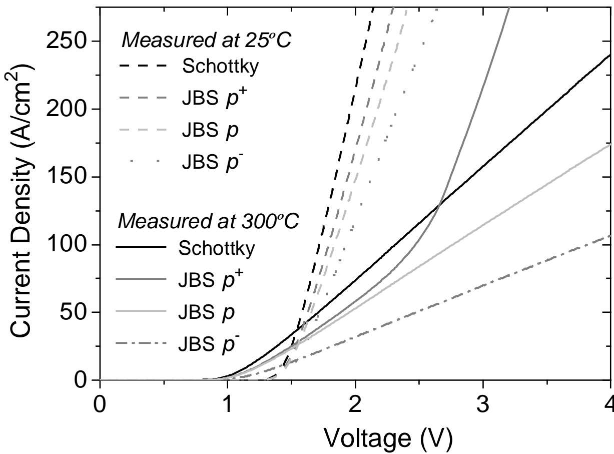


Figure 5.27 Forward *J-V* characteristics of JBS diodes with different concentration in the *p*-type grid, measured at 25ºC and 300ºC. Schottky J-V characteristics are also shown for comparison.

For moderate forward current densities and temperatures up to 150ºC the Schottky diode has a slightly better performance due to lower specific on-resistance. However, for high current densities and high temperatures the JBS diode with the highest hole concentration shows better characteristics due to bipolar current injection from the p^+ grid.

5.3.4 Breakdown voltage and reverse leakage current

The three types of JBS diodes were fabricated with an optimised single JTE structure as an edge termination like that shown in Figure 5.28.

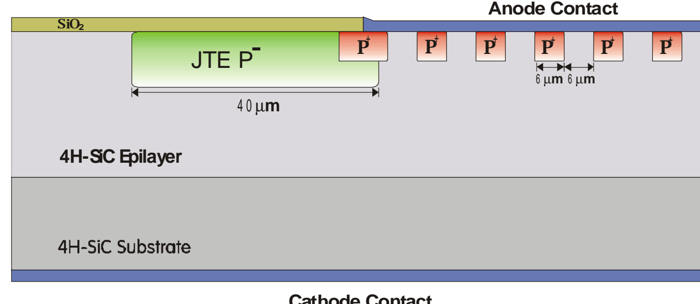


Figure 5.28 Schematic cross-section view of a JBS diode with p^+ grid and single JTE.

Table 5.5 reports the breakdown results of the JBS diodes on the different samples processed with the same metallisation scheme (Ni/Ti).

Table 5.5 Breakdown results on JBS diodes with single JTE structure after different RTA process on different samples.

Sample	RTA process	Schottky barrier height	*JBS p*-type grid	Maximum V_{BR} (V)	Average V_{BR} (V)	Standard Deviation (V)
CQ1	400ºC 2min	Φ_B=0.85eV	P^+	1265	1225	50
			P	1260	1200	50
			P^-	1270	1200	50
CQ2	700ºC 3min	Φ_B=1.10eV	P^+	1450	1350	75
			P	1480	1375	75
			P^-	1465	1375	75
CQ3	900ºC 3min	Φ_B=1.25eV	P^+	1625	1475	100
			P	1600	1500	100
			P^-	1615	1475	100

Using as yield criteria an absolute voltage value at a given maximum leakage current, this translates directly into a higher yield for the JBS diodes. In all samples a higher blocking yield was observed for the JBS diodes compared to the Schottky diodes.

There are several different factors that contribute to the better blocking yield. The phenomenon is suggested to be dominated by the different blocking mechanisms of semiconductor to metal junctions versus semiconductor *pn* junctions. For implanted *pn* junctions, used for the *p*-type grid, the employed process shows excellent blocking, even in the presence of a variety of crystal defects. On the other hand, the processing makes the effects of defects at the surface worse. A micropipe defect “contaminated” by *p*-type doping in a *pn* junction leads to a local reduction in the electric field shielding the defect effectively.

However, if the same defect is processed as a Schottky area, the deposited metal decorating the micropipe leads to a local increase in the electric field strength. Moreover, an epilayer surface contains epitaxial growth related defects only present at the surface but not in the bulk. All these facts lead to additional local peaks in the electric field at the surface and thereby at the Schottky barrier.

The JBS design moves the highest point of electric field away from the surface, placing the highest electric field points at the *pn* junction inside the crystal, and reduces the field at the Schottky junction. Simultaneously, the Schottky area is reduced by the *p*-type regions, then the sensitive Schottky area is replaced by less sensitive *pn* junctions. A further improvement in the Schottky barrier technology addressing the above issues would benefit both diodes similarly.

The important feature of the JBS diode is that depletion regions generated at the *pn* junctions pinch off the channel and the electric field is reduced at the metal-SiC junction. The electric field E at the Schottky contact depends on the channel pinch-off voltage V_p and the epilayer doping N_D ,

$$E = \sqrt{\frac{2qN_D}{\boldsymbol{e}_s}(V_p + V_{bi})} \tag{5.16}$$

where V_{bi} is the built-in voltage. The pinch-off voltage is determined by the Schottky spacing s between the p-type regions since that gives the voltage at which channel pinch-off occurs,

$$V_p = \frac{qN_D}{8\boldsymbol{e}_s}s^2 - V_{bi} \tag{5.17}$$

A brief calculation for our JBS diodes fabricated on samples from wafer AD-0602-02 gives a value of 75V for the pinch-off voltage. This pinch-off voltage does not changes in a significantly manner with the doping concentration of the p-type grid.

How much the electric field is reduced depends not only on the Schottky spacing but also on the doping concentration in the channel, the doping profile shape and depth of the p-type regions.

Figure 5.29 shows the leakage current at room temperature of the three types of JBS fabricated, together with that of Schottky and PiN diodes, shown for comparison. The I-V curves were acquired after the RTA at 900ºC when good ohmic contact properties are achieved together with low leakage current of Schottky diodes.

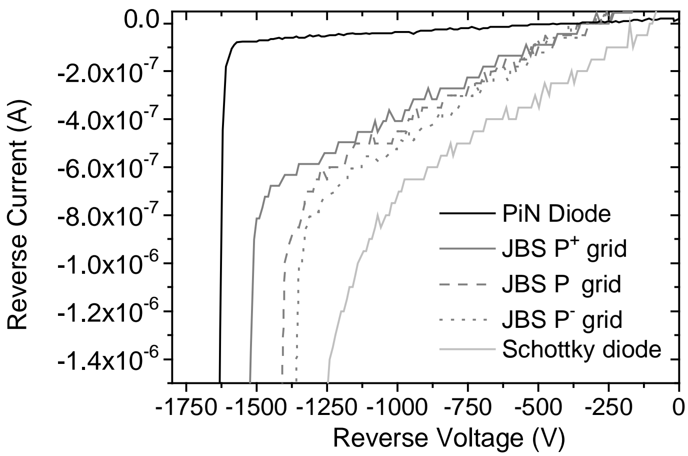


Figure 5.29 Reverse I-V characteristics of the JBS diodes with different doping concentration in the p-type grid. The I-V curves from PiN and Schottky diodes are also shown for comparison.

As it can be clearly seen in Fig. 5.29, the reverse leakage current is reduced in comparison to that of a Schottky diode by the use of a *p*-type grid. The leakage current for JBS diodes with different doping concentration in the *p*-type grid does not show big differences, although it can be observed a small decrease in leakage current with the increase in p-type doping. This shows that the *p*-type concentration decrease does not affect the pinch-off effect significantly, at least in the range of doping we considered. This assumption is reinforced by the sharper I-V curve at breakdown observed in JBS diodes in comparison to the soft breakdown due to the barrier lowering effect at high electric fields observed in Schottky diodes.

5.3.5 High temperature reverse performance

The reverse characteristics up to –1000V of PiN, JBS (P^+ grid) and Schottky diodes measured at room temperature (25ºC) and at 200ºC are shown in Fig. 5.30. As it can be seen, the leakage current of the JBS diodes is proved to be lower than that of the Schottky barrier diode both at room and high temperature. This is due to the highly doped p^+ regions that reduce the field strength at the Schottky contact region thus preventing it from the Schottky barrier lowering effect at high temperature. The PN diodes at 25ºC exhibited a leakage current level at –1000V in the range of the measurement limit (10^{-9}A) and it increased up to $3\cdot10^{-7}$A at 200ºC. The p^+ JBS diodes showed and increase of the leakage current at –1000V from $5\cdot10^{-7}$A at room temperature up to $1\cdot10^{-6}$A at 200ºC. Similar values of leakage currents and breakdown voltages at room and high temperature are obtained on the JBS diodes with lower *p*-type grid doping.

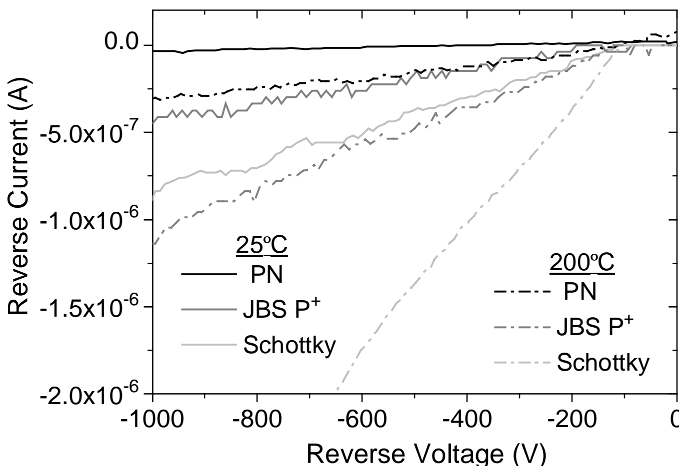


Figure 5.30 Reverse I-V characteristics up to –1000V of PiN, JBS (P^+ grid) and Schottky diodes measured at room temperature and at 200ºC.

5.3.6 JBS conclusions

Our results demonstrate that performant 4H-SiC JBS diodes together with low-leakage current Schottky diodes can be fabricated after a high temperature treatment of the contact metal. This was achieved by a Ni/Ti bi-layer metallisation scheme forming simultaneously a good Schottky contact on low doped *n*-type regions and a low ohmic contact on p^+ implanted regions. This can be used in processes where both ohmic and Schottky contacts are needed at the same time. The JBS diodes with the proposed design (concentric rings 6μm/6μm) exhibit bipolar conduction activation at moderate forward current densities and good surge current capabilities at high temperatures. They also show a low reverse leakage current level even at high temperature and higher blocking capabilities than Schottky diodes. A decrease of the concentration of the *p*-type grid of the JBS diode does not affect the reverse characteristics but eliminates the surge current capabilities, as it is not able to start the bipolar injection. Moreover, higher on-resistances were shown due to higher implanted depths of the lower doping concentrations in the p-type grid. These results clearly demonstrate that SiC JBS diodes can be optimised to be a good candidate for high power and high temperature applications.

5.4 PiN Diode Performance

5.4.1 Forward operation

A *pn* junction is formed when an opposite dopant impurity is introduced into a region of the semiconductor material. The Fermi levels E_{Fn} and E_{Fp} in the two semiconductor regions line up and a barrier with the built-in potential Φ_{bi} is formed (see Figure 5.31)[178],

$$E_{Fn} - E_i = k_B T \ln\left(\frac{n_{no}}{n_i}\right) \tag{5.18a}$$

$$E_i - E_{Fp} = k_B T \ln\left(\frac{p_{po}}{n_i}\right) \tag{5.18b}$$

Assuming full ionisation of the dopant atoms $n_{no}=N_D$, $p_{po}=N_A$ on either side of the junction, the built-in potential is given as

$$q\Phi_{bi} = (E_i - E_{Fp}) - (E_{Fn} - E_i) \cong k_B T \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{5.19}$$

where E_i is the intrinsic Fermi level and n_i the intrinsic carrier concentration of the semiconductor material.

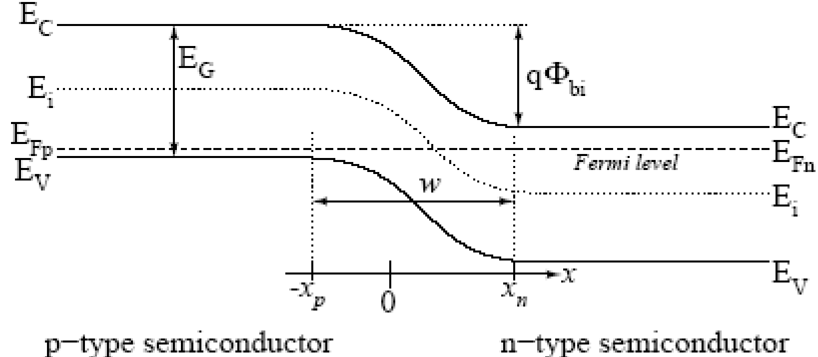


Figure 5.31 Band structure of a pn diode in thermal equilibrium without external bias. E_C is the conduction band edge, E_V is the valence band edge, E_i is the intrinsic Fermi level of the semiconductor and w is the width of the depletion region formed by the built-in potential Φ_{bi}.

When an external bias V is applied, assuming an abrupt *pn* junction, low injection conditions, and Boltzmann statistics, the *I-V* characteristics of a PiN diode can be analytically described by [179]

$$J(V)=\underbrace{\frac{qWn_i}{2t_R}\left(exp\left[\frac{qV}{2k_BT}\right]-1\right)}_{\text{Generation-recombination}}+\underbrace{q\left(\sqrt{\frac{k_BT}{q}\frac{m_n}{t_n}}\frac{n_i^2}{N_A^-}+\sqrt{\frac{k_BT}{q}\frac{m_p}{t_p}}\frac{n_i^2}{N_D^+}\right)\left(exp\left[\frac{qV}{k_BT}\right]-1\right)}_{\text{Carrier diffusion contribution}} \tag{5.20}$$

where t_R is the effective generation-recombination lifetime and W is the width of the junction depletion region at applied voltage V.

The total current density consists of two contributions: the current arising from carrier recombination within the depletion region and the current carried by minority carrier diffusion. Generally, the recombination mainly arises within the lower-doped area of the depletion region. Therefore, t_R can be identified as the corresponding minority carrier lifetime τ_n or τ_p in this case (see section 2.2.4). In reverse bias, τ_R denotes the so-called generation lifetime. The recombination current which is basically determined by the ratio of n_i/τ_R dominates the characteristics up to J=3×10^{-3}A/cm^2. The diffusion current is determined by the corresponding diffusion properties (expressed by $\sqrt{k_BTm_n/qt_n}$) and the density of injected minority carriers at the edge of the depletion regions (expressed by $n_i^2/N_{A,D}^{-,+}$). At high current ratings, the voltage drop across the epi-layer and the substrate results in approximately linear I-V characteristics.

The dominant components in the on-state voltage drop (V_F) in a *PiN* diode are given by,

$$V_F = V_{P+Cont} + V_{bi} + V_m + V_{Subs} + V_{N+Cont} \tag{5.21}$$

where V_{P+Cont} and V_{N+Cont} are the anode and cathode contact resistance voltage drop, respectively, V_{bi} is the p^+n junction drop, V_m is the n^- layer drop, and V_{Subs} is the resistive voltage drop in the substrate.

Figure 5.32 shows an schematic draw of these resistive contributions in a *PiN* rectifier under low- and high-injection conditions.

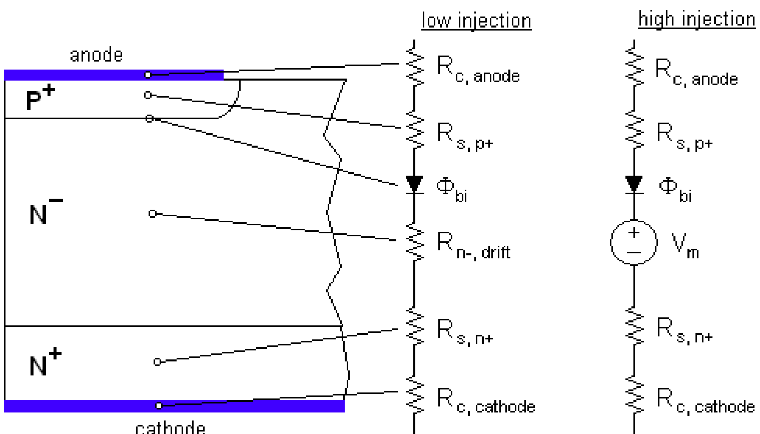


Figure 5.32 Schematic over the parasitic resistances in a PiN rectifier under low- and high-injection conditions.

Contact resistances $R_C < 10^{-3}$ Ω have been obtained to both n^- and p^+ silicon carbide, giving a voltage drop of less than 100 mV each. Assuming a resistivity in the implanted p^+ anode of 0.4 Ωcm (as extracted from TLM structures) at a thickness of 0.25 μm would only add another 7 mV of voltage drop at 100 A/cm^2. The contribution of the silicon carbide substrate material is determined by its resistivity and thickness (Table 3.1) and causes an additional voltage drop of only 60 mV. The forward voltage drop over the drift region is determined by the resistance of this layer in the case of unipolar or low-injection operation, or else by a constant voltage drop V_m at high level injection. Thus, the largest single contributions to the forward voltage drop are caused by the *pn* junction itself, with a built-in potential of 2.9V (using Eq. 5.19) and the drift region of the rectifier.

The mid-region drop, V_m, depends strongly on carrier recombination lifetimes and can be expressed by the following relationship [98]

$$V_m = \frac{3k_BT}{q}\left(\frac{t_{epi}}{2L_a}\right)^2 \qquad for \qquad t_{epi} \leq 2L_a \tag{5.22a}$$

$$V_m = \frac{3pk_BT}{8q} exp\left(\frac{t_{epi}}{L_a}\right) \qquad for \qquad t_{epi} \geq 2L_a \tag{5.22b}$$

where t_{epi} is the middle drift layer width (epilayer thickness) and L_a is the ambipolar diffusion length, which is given by,

$$L_a = \sqrt{D_a \cdot t_{HL}} \tag{5.23}$$

where D_a is the ambipolar diffusion constant given by $D_a = D_p + (m_p/m_n)D_n$, and t_{HL} is the high level injection carrier lifetime. D_p and D_n are the hole and electron diffusion coefficients given

by the Einstein relations, $D_p = m_p \cdot k_B T/q$ and $D_n = m_n \cdot k_B T/q$. Here m_n and m_p are the electron and hole mobility in the voltage blocking drift layer.

The on-state voltage drop of a *PiN* rectifier at a current density level of $100 A/cm^2$ is plotted in Fig. 5.33 as a function of carrier lifetime and epilayer thickness. This figure shows that a higher carrier lifetime results in better conductivity modulation, with on-state voltage drop approaching the built-in voltage drop of a p^+n junction.

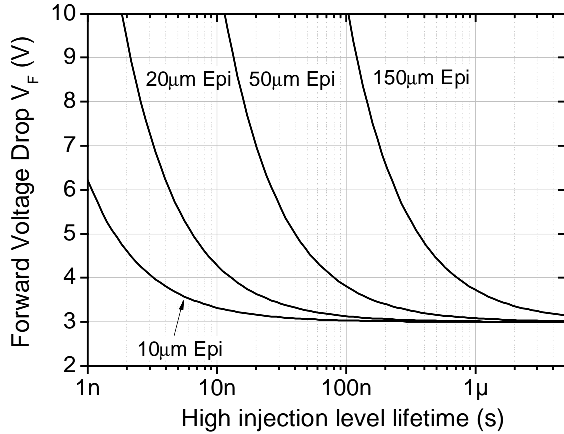


Figure 5.33 Forward voltage drop on 4H-SiC *PiN* diodes as a function of the high level lifetime and epitaxial thickness.

As expected, a thicker epitaxial layer (i.e. higher blocking voltage) requires a higher carrier lifetime in order to achieve a lower on-state voltage drop PiN diode. However, it is encouraging to note that beyond a carrier lifetime of 3 µs, even a 150 µm epitaxial layer is well modulated. Hence, SiC is expected to offer extremely high switching speeds even for devices using such large thicknesses.

The minority carrier lifetime is strongly related to the crystal quality and defects, which reduces the lifetime considerably. The lifetime of SiC has been investigated in several experiments over the past few years [180-185]. The highest reported values are up to 2 µs at room temperature, which is achieved in thick (40-60 µm) CVD grown epitaxial layers [182,183]. The lifetime decreases with decreasing epitaxial layer thickness and for a 10 µm thick epitaxial layer the lifetime is 0.2 µs because of both higher surface and junction recombination rates. An increased surface recombination rate is commonly seen in semiconductor device technology due to dangling bonds caused by imperfections at the surface termination. In SiC an increased recombination rate is also observed in the metallurgic junction between the epilayer and the substrate. By introducing a lifetime shorter than 1 ns in the volume closer than 0.1 µm to the metallurgic junction, contradictions between steady-state and transient current can be explained [185] using simulations. A highly reduced lifetime is also observed in the junction region in the measurements presented in refs [180] and [182]. A reduced lifetime in the junction region can be an advantage for switching diodes and is

sometimes created deliberately in silicon diodes by irradiation. The reverse recovery time is reduced, which increases the switching speed. This is preferable to a reduced lifetime within the whole base region of the diode, which increases the series resistance and consequently increases the forward losses.

Table 5.6 shows the forward voltage drop at 100 A/cm^2 from samples CQ2 (10 μm epi thickness) and S1 (15 μm epi thickness) after the different RTA processes carried out. The ideality factor (*n*) and contact resistivity (ρ_c) are also shown for reference.

Table 5.6 Forward voltage drop (V_F) at 100A/cm^2, ideality factor (*n*), and contact resistivity (ρ_c) of samples CQ2 (10μm epi) and S1 (15μm epi) after the different RTA processes.

RTA Temp.	Sample CQ2			Sample S1		
	V_F (V)	*n*	r_c (Wcm^2)	V_F (V)	*n*	r_c (Wcm^2)
As-deposited	4.50	3.21	$9 \cdot 10^{-4}$	4.65	3.25	$8 \cdot 10^{-4}$
350ºC	4.05	2.95	$3 \cdot 10^{-4}$	4.30	3.05	$2 \cdot 10^{-4}$
500ºC	3.25	1.97	$4 \cdot 10^{-5}$	3.70	2.85	$9 \cdot 10^{-5}$
700ºC	3.00	1.85	$1 \cdot 10^{-5}$	3.20	1.89	$2 \cdot 10^{-5}$
900ºC	3.20	1.78	$3 \cdot 10^{-5}$	3.35	1.81	$3 \cdot 10^{-5}$

As it was explained in chapter 3 section 3.4.2, the contact becomes ohmic after annealing at 500ºC and it improves its ohmic characteristic significantly after RTA at 700ºC. This ohmic contact formation is also reflected in the forward voltage drop decrease. The on-state voltage drop was found to be very uniform (i.e. ± 0.05V) across all the examined samples and was not a yield-limiting factor.

Figure 5.34 shows the J-V characteristics of a *PiN* diode of the two samples (CQ2 and S1) after the RTA at 700ºC.

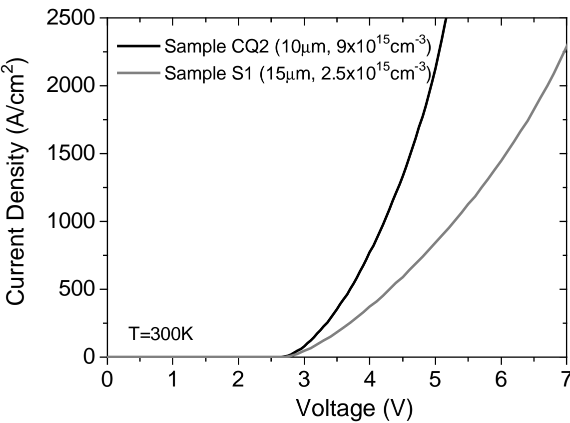


Figure 5.34 Forward J-V characteristics at room temperature of the PiN diodes fabricated on samples CQ2 and S1.

As it can be seen from the above figure, *PiN* diodes fabricated on sample CQ2 exhibit lower specific on-resistance and higher conductivity modulation than those fabricated on sample S1. This is probably due to two main causes, i) a higher on-resistance of the drift base

in sample S1 at low injection levels and, ii) a lower lifetime of the minority carriers in the drift layer of sample S1 due to the presence of a higher amount of material defects than in sample CQ2. However, both samples show good conductivity modulation and the diode specific on- resistance decreased with the increase of the forward bias reaching the values 4×10^{-4} Ωcm^2 and 1×10^{-3} Ωcm^2 for samples CQ2 and S1, respectively, at current density ~2kA/cm^2.

Measurements on larger area (ϕ=400 μm) diodes indicated similar forward characteristics. The forward current density of the large area devices was found to be lower than that observed in small diodes, as it can be observed in Fig 5.35. This effect is attributed to the lateral current spread in the base and the anisotropic carrier mobility. An anode contact resistance due to the thin metal layer is also a cause of this phenomenon, and larger diodes are influenced by the metal resistance while current spreading in metal.

As an illustration of the high injection level on the two different sized diodes Figure 5.36 shows an optical photo of both diodes forward biased at 5V. The blue light emission is supposed to originate from the radiative recombination (via several deep centers in the bandgap) of injected holes in the n^- drift layer. In that case, the light intensity must be proportional to the injection current as it is qualitatively observed in our diodes.

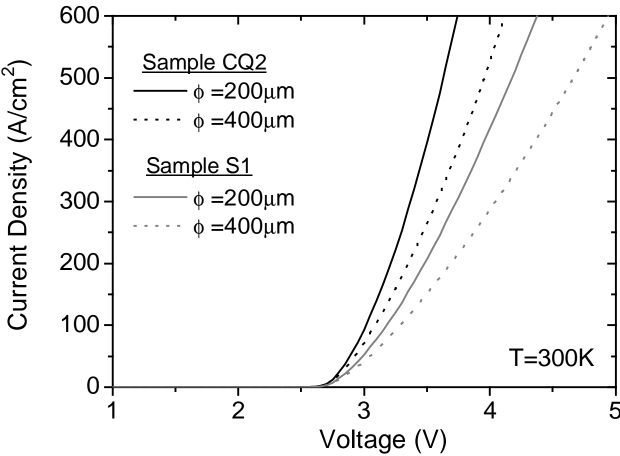


Figure 5.35 J-V forward characteristics of 200 μm and 400 μm diameter diodes on samples CQ2 and S1.

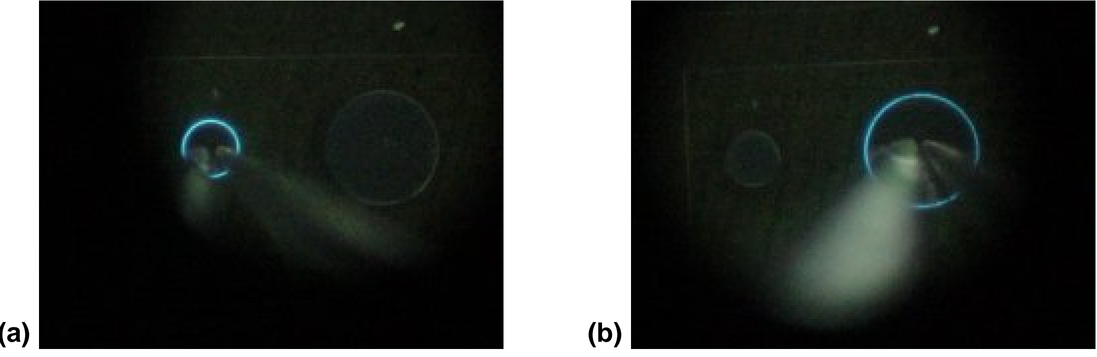


Figure 5.36 Optical microscopy photos of (a) 200 μm and (b) 400 μm diameter SiC PiN diodes at high forward injection level.

5.4.2 High temperature forward characteristics

After the highest contact RTA process at 900ºC, forward current-voltage (*I-V)* characteristics of the diodes were measured at a temperature range from room temperature (RT) to T=300ºC. The typical measured curves at low and medium current densities using an HP4155B semiconductor parameter analyser are shown on Fig.5.37 in semilog scale.

As it can be observed in Fig. 5.37, an excess current bump was observed between 0V and 2.5V, this effect being more pronounced at room temperature. This anomalous *I-V* curves have been previously reported in other works, which are attributed to the presence of defects in the junction depletion region [186,187]. However, it is not known whether this irregular conduction is due to defects formed by ion implantation or to native defects in the epitaxial layer. Ohyanagi et al. [188] have associated this irregular conduction to the presence of an epitaxial "linear defect" but they could not verify whether this "linear defect" was related to the screw dislocations or other defects.

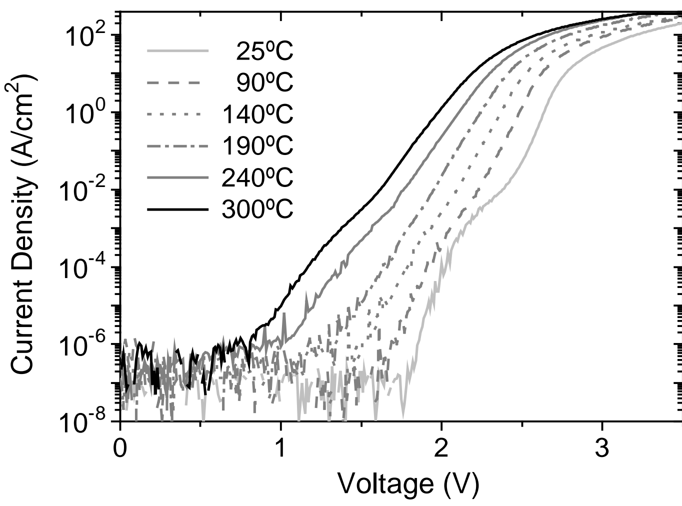


Figure 5.37 Forward J-V characteristics at different temperatures up to 300ºC of PiN diodes in logarithmic current density scale.

In order to model this excess current, these defects are considered to produce parallel diodes to the "ideal" ones with areas correspondingly reduced, similar to the model used in section 5.2.3.2 to explain similar *I-V* characteristics of silicon carbide Schottky diodes. The initial high current region is then due to the turn-on of one of the "defect" diodes having a smaller effective turn-on voltage. The current rises through this "defect" diode with increasing applied voltage until becoming limited by the high series resistance corresponding to its very small area. As the applied voltage further increases the current of the parallel "ideal" diode with higher turn on voltage becomes significant and once it exceeds the "defect" diode, the second current rise is observed. On the other hand, when the temperature is increased the "ideal" portion of the I-V curve shifts left and up at a higher rate than the "defect" portion due

to its larger area. This effect begins to smooth out the bump of the high temperature *I-V* curves with respect to the RT ones. This trend can be clearly observed in Fig. 5.37.

At current densities 10^{-2} A/cm^2 < J < 10 A/cm^2, the diodes follow the typical behaviour described by

$$J = J_o \, exp\left(\frac{qV}{nk_B T}\right) \tag{5.24}$$

where J_o is the saturation current; n, the ideality factor; q, the elemental charge; k_B the Boltzmann constant, and V the applied bias voltage. Fitting the measured data by using Eq. (5.24) the values of n and J_o were extracted and are summarized in Table 5.7 together with the forward voltage drop (V_F) at 100 A/cm^2 and the on-resistance (R_{on}) values.

Table 5.7 Extracted parameters from J-V characterisation at different temperatures.

Temperature	V_F @100A/cm^2 [V]	R_{on} @100A/cm^2 [mΩcm^2]	n	J_o [A/cm^2]
25ºC	3.23	1.62	1.78	5.43×10^{-28}
90ºC	3.06	1.59	1.72	1.73×10^{-22}
140ºC	2.94	1.56	1.69	2.06×10^{-19}
190ºC	2.87	1.52	1.65	3.11×10^{-15}
240ºC	2.71	1.51	1.63	1.30×10^{-13}
300ºC	2.57	1.49	1.59	5.43×10^{-28}

The ideality factor close to 2 at room temperature suggests that the space charge recombination is the dominant mechanism. However, the decrease of the ideality factor with temperature indicates that the current transport mechanism is dominated by the diffusion of minority carriers as the temperature rises. The diffusion current increases with the temperature faster than the recombination current since the diffusion and recombination currents are roughly estimated to be proportional to n_i^2 and n_i, respectively, n_i being the intrinsic carrier concentration that increases exponentially with temperature.

Furthermore, assuming that the recombination centers reside energetically near the middle of the bandgap, the temperature dependence of the recombination current is thermally dominated by the ratio n_i/t_o, (t_o being the effective carrier lifetime in the depletion region) whose exponential temperature dependence yields the thermal activation energy (E_a). The pre-exponential factor J_o reflects this thermal activation, i.e. $J_o \sim exp(-E_a/kT)$ with an activation energy E_a=1.79eV derived from the slope of the plot shown in Fig 5.38.

Therefore, it can be concluded that the recombination via multiple recombination levels controls the recombination current at room temperature yielding an ideality factor $n=(s+2d)/(s+d)$ where s accounts for the number of shallow levels and d for the number of deep levels according to the generalized Shockley-Noyce-Sah model [189]. In our case, the ideality factor n=1.78 indicates that s=1 and d=4. The activation energy (E_a=1.79eV) is in

good agreement with the predicted multiple-level model value E_a»E_g/n, where E_g is the bandgap energy (E_g=3.25eV for 4H-SiC).

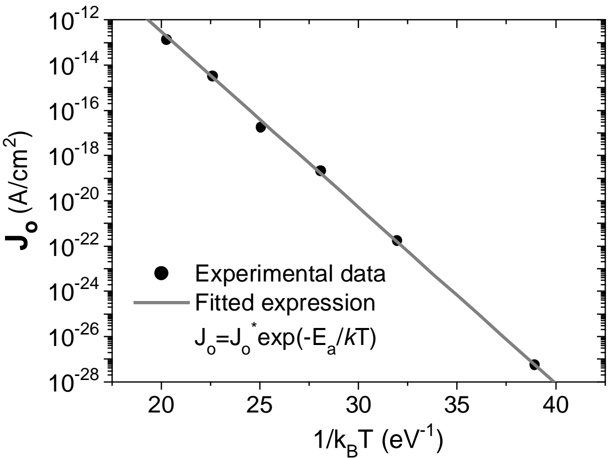


Figure 5.38 Saturation current density (J_o) versus 1/k_BT. The slope gives an activation energy of E_a=1.79eV.

Forward current-voltage measurements at high current densities (up to 5 kA/cm^2) were made on a Tektronix 370A curve tracer and are shown in Fig. 5.39. The on-state voltage drop of a typical device (ϕ=200 μm) at 100 A/cm^2 was 3.23eV at room temperature and decreases to 2.57eV at 300ºC mainly due to the decreased built-in voltage at elevated temperatures. The specific resistance decreases when increasing the forward bias reaching the value R_{on}= 6.5×10^{-4} Ωcm^2 at a current densities J> 3kA/cm^2 at room temperature. Besides, the on-resistance becomes smaller at higher temperatures. These results may be attributed to the increased minority carrier lifetime and thereby the longer diffusion length at high temperatures which produce a more effective conductivity modulation. The reduced contact resistance at high temperatures (as it was shown in chapter 3, section 3.4.2) might also contribute to this phenomenon. This performance demonstrates the existence of low resistivity value contacts on *p*-doped 4H-SiC, as confirmed from TLM measurements.

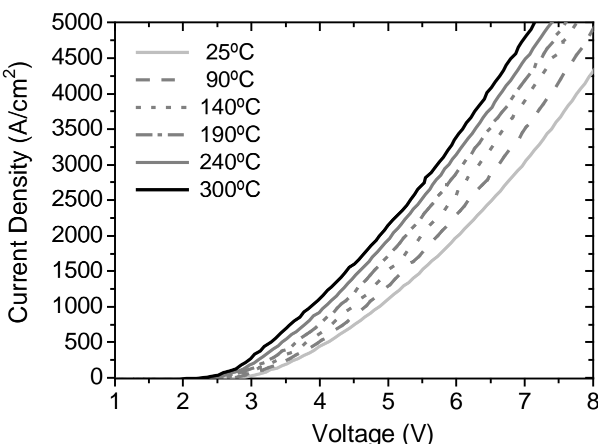


Figure 5.39 Linear forward J-V characteristics of fabricated PiN diodes at different temperatures and high current density levels.

In the entire 25ºC to 300ºC range, the on-state voltage drop at 1 kA/cm^2 remains in a low 1V range, as seen from Fig. 5.38. This shows that SiC PiN rectifiers are stable with temperature even at high forward current densities. In case of Si diodes, over 40% reduction in on-state voltage drop was measured in the 25ºC to 125ºC range [190].

5.4.3 Forward bias degradation

For blocking voltages above 3kV PiN diodes using bipolar conductivity modulation in the base layer have a lower forward voltage drop than unipolar Schottky diodes. Recently, however, it was discovered that bipolar SiC power diodes gradually degrade in the sense that the voltage drop across the diode, for a constant current, gradually increases with the time of operation [48,191]. The stochastic voltage increase is typically in the range 0.1-10% of the ideal voltage drop across the diode, and is, in fact a serious obstacle in the development and application of bipolar SiC technology.

This degradation phenomenon is associated with the growth of defects during the process of forward-bias reliability testing. The defects responsible for the increase of forward voltage drop have been identified as stacking faults. Such defects were only observed in the biased diodes and were restricted to the diode area, indicating that the nucleation and growth of these defects are induced by electron-hole pair recombination. It is also generally believed that the edges of the stacking faults act as recombination centers that reduce the carrier lifetime in the material and lead to the observed on-state voltage degradation [192]. However, only the high current forward characteristics is affected. The sub-threshold forward, the reverse leakage and the blocking voltage characteristics do not change at all [48].

The forward voltage (V_F) degradation and the stacking faults (SF) are correlated, and the value of ΔV_F (which represents the V_F difference between before and after the forward bias stress) increases with an increase in the area of the SFs. Since the extension of the triangular SFs occurs within 8 degrees (in 4H-SiC) inclined basal plane up to the surface, the area of the SFs on the basal plane increases with an increase in the drift layer thickness. Therefore, the value of ΔV_F increases with increasing drift layer thickness [193].

We have performed an electrical testing of current-voltage characteristics to evaluate the forward bias degradation on our fabricated PiN diodes on CREE´s wafer AD-0602-02 (10µm of epilayer thickness). A brief statistical analysis has been performed based on test measurements over 50 diodes on the same sample (CQ3) at room temperature. We have stressed each diode at a forward current density of 500 A/cm^2, and stressing proceeded in a series of steps. During each step, the stressing current was applied for 10 seconds and the I-V curve was acquired 1 minute after stopping the stress current, to avoid the effect of self-heating of the device. The stressing steps were performed until stabilization of the forward voltage drop at 500 A/cm^2 was observed and an additional stressing did not significantly

increase the voltage. However, a minimum number of 20 stressing steps was set for all measured diodes. Figure 5.40 reports the statistical results on forward voltage degradation of the 50 tested diodes.

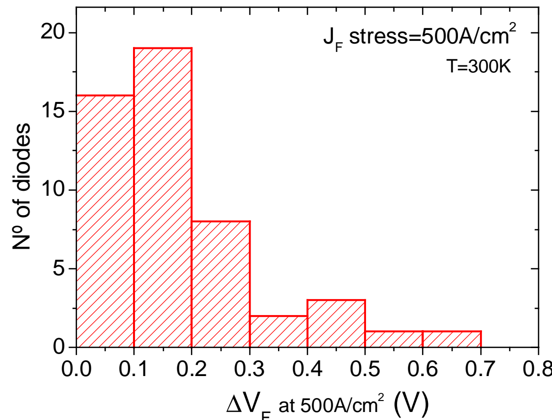


Figure 5.40 Statistical report on forward voltage drift at 500A/cm^2 after forward current stressing.

As it can be observed from Fig. 5.40, the forward voltage increased in a rather low 0.7V range, showing an average value of 0.18V. It must be pointed out that 10 diodes showed almost no degradation on their forward voltage drop, with ΔV_F<0.05V. Moreover, some of the diodes with no degradation observed were submitted to a constant current stress at 500 A/cm^2 for 1 hour and they showed a small decrease (0.05V) in their forward voltage drop due to the self-heating effect, thus demonstrating good reliability at high current densities.

As already stated in a previous paragraph, only the high current forward characteristics is affected by the voltage drop degradation, and as it can be observed in Figure 5.41b the sub-threshold forward characteristic does not change at all. Figure 5.41 shows the successive current-voltage (J-V) characteristics after the several sequential stressing steps, where it can be clearly observed the forward bias degradation and the saturation on V_F drift after 10 stressing steps.

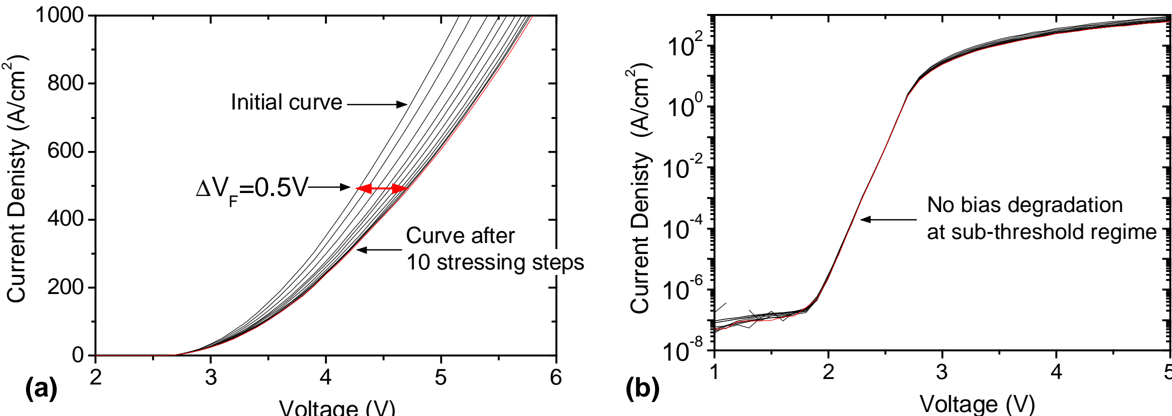


Figure 5.41 Forward J-V characteristics of a stressed PiN diode. (a) Linear J-V characteristics showing the forward bias degradation. (b) Semilog J-V plot showing no bias degradation at forward bias lower than the built-in voltage.

As our diodes had no anode metallisation windows, it was difficult to correlate the bias degradation with the propagation of stacking faults during forward current stressing. However, on some diodes showing the greater ΔV_F values (higher than 0.5V) it was able to observe some possible stacking faults at the anode edge, as it can be seen in Figure 5.42. We speculate the possibility that stacking faults indicated as SF1 and SF1? could be the same SF crossing the entire diode area.

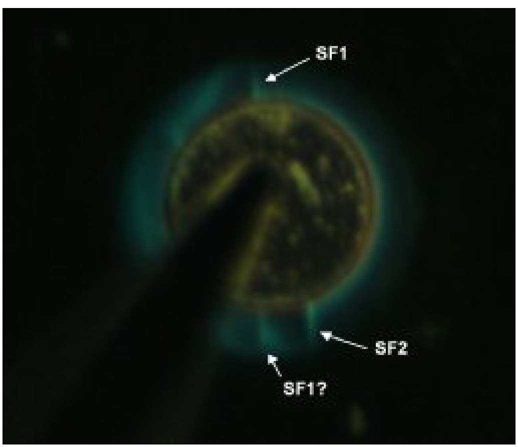


Figure 5.42 Electroluminiscence graph of a diode after forward current stressing. White arrows indicate the stacking faults present on the diode area.

Thus, it has been shown that SiC PiN diodes may suffer from significant forward voltage instability due to stacking faults spawned from basal plane dislocations (BPD). Clearly, the reduction of BPD is vital in developing a stable PiN diode. It must be considered here that the employed wafer to fabricate our previously reported diodes was purchased from CREE in winter 2000. Since the summer of 2001, when the first reports on bipolar degradation were published [48,191], the SiC device community at large has confronted the issue of unstable forward voltage drop in bipolar SiC devices.

Recently, CREE researchers have reported a process modification to 3-inch substrates that reduces the BPD density in epilayers by approximately 2 orders of magnitude and dramatically reduces the average V_F drift of resultant diodes [194]. This has allowed to demonstrate a 50 A, 10 kV 4H-SiC PiN diode technology where good crystalline quality and high carrier lifetime of the material has enabled a high yielding process with V_F as low as 3.9V@100A/cm^2. Furthermore, they have produced a large number of devices that exhibit a high degree of forward voltage stability with encouraging reverse blocking capability. This is a significant step in the evolution of a commercially viable SiC PiN diode technology expected to meet the demands of high voltage, high frequency power conversion applications.

5.5 Summary

In this chapter we have demonstrated performant characteristics of 1.2kV Schottky, Junction Barrier Schottky (JBS) and implanted PiN diodes processed on the same 4H-SiC wafer. A bi-layer Ni/Ti scheme for the contact metallisation submitted to high temperature rapid thermal anneals is proved to form good ohmic contact on p^+ implanted areas while maintaining good Schottky characteristics on lightly doped *n*-type regions. I-V characteristics of the three types of rectifiers have been evaluated from room temperature up to 300ºC.

Schottky and JBS diodes show a current density inflexion point where the temperature coefficient changes from positive to negative and where the forward voltage drop remains almost constant in this temperature range. We have shown that this inflexion point occurs at lower current density levels for higher blocking layers. For moderate forward current densities and temperatures up to 150ºC the Schottky diode has a slightly better performance due to a lower specific on-resistance. However, for high current densities and high temperatures the JBS diode with the highest hole concentration shows better characteristics due to the bipolar current injection from the p^+ grid. JBS diodes with lower implantation dose in the *p*-type grid were proved to behave like a Schottky diode with higher on-resistance.

Concerning the reverse characteristics, we have proved the high efficiency of the optimised single JTE termination on both Schottky and JBS diodes, achieving blocking voltages of nearly 85% of the ideal plane-parallel value. We have performed a detailed investigation of the origin of the relatively large leakage current commonly observed in SiC Schottky diodes. Forward and reverse I-V characteristics measured on Schottky diodes agree well with the proposed model of localized regions at the metal/SiC interface where Schottky barrier height is lowered. The origin of this barrier inhomogeneities is still not clear, although a correlation with surface epitaxial defects is discarded and interface disorder due to the multiple metallic phases present after the RTA process is suggested to be a possible source for the presence of low-barrier regions.

The leakage current of JBS diodes is proved to be lower than that of Schottky barrier diodes both at room and high temperature. This is due to the p-type regions that reduce the field strength at the Schottky contact region thus preventing it from the Schottky barrier lowering effect at high temperature. Similar values of leakage currents and breakdown voltages at room and high temperature are obtained on the JBS diodes with lower p-type grid doping. This shows that the p-type doping concentration decrease does not affect the pinch-off effect, in the range of doping we considered. This results clearly demonstrate that SiC JBS diodes can be optimised to be a good candidate for high power and high temperature applications.

Finally a detailed description of the forward characteristics of fabricated PiN diodes has been performed. High bipolar conductivity modulation has been proved and low on-resistance values have been achieved due mainly to the proper good ohmic contact formed. Measurements at temperatures up to 300ºC have shown a good thermal stability of the current-voltage characteristics of the PiN diodes. It has been shown that the recombination via multiple recombination levels controls the recombination current at room temperature. However, the decrease of the ideality factor with temperature indicates that the current transport mechanism is dominated by the diffusion of minority carriers as the temperature rises.

General Conclusions

The aim of this thesis research has been to make tangible contributions towards the development of 4H-SiC high power rectifiers. The area of edge termination research with emphasize laid on design and optimisation of junction termination extension structures has been identified as the field where most contributions could be made and consequently, much efforts have been directed along those lines. Moreover, several contributions to the process technology field have been made, with some excellent results.

With the device fabrication processes as a guideline, we will briefly report the most relevant conclusions.

- Concerning the ion implantation process and high temperature activation anneal, it has been proved that high activation rates (approaching 100%) can be achieved on Al implanted at moderately high temperatures (300ºC-400ºC) after an activation anneal performed at 1650ºC for 30min. Moreover, we have shown that annealing in N_2 ambient improves the surface morphology after the activation annealing. It has been also checked the difficulties in the suppression of implanted boron diffusion after the high temperature activation anneal, even when a promising two step annealing was performed.

- Good Schottky and ohmic contacts have been formed on diodes in the same wafer and with the same metallisation scheme. A Ni/Ti bilayer metal system has been demonstrated to form both a rectifying Schottky contact with low leakage current level and a performant ohmic contact with a low contact resistivity ($1\times10^{-5}\ \Omega cm^2$) and good thermal stability after a high temperature RTA (700ºC). Some non ideal behaviour of the Schottky contacts have been associated with the presence of inhomogeneities at the metal-SiC interface.

- Ø High efficiency on edge termination can be achieved with both single and double zone JTE structures with moderate constraints on their design. Floating guard rings structures have been proved to provide lower blocking capabilities, and it appears to be a less reliable termination structure due to a higher complexity on its optimisation.

- Ø During this thesis a novel edge termination technique namely “Floating guard rings assisted JTE” has been developed. It has demonstrated great blocking performances, reaching breakdown voltages close to 95% of the theoretical 1D breakdown. Its higher reliability is based on the inner floating guard rings effect that “assist” the JTE zone when it moves away from the ideal performance.

- Ø We have demonstrated that the implementation of a metal field plate over the passivation layer can reduce the leakage current and improve the blocking capabilities on diodes with low termination efficiency. Moreover, it has been proved that a primary passivation layer is needed in order to obtain low leakage currents and to allow the achievement of the best blocking performances.

- Ø Positive temperature behaviour of the avalanche breakdown has been observed in our 4H-SiC PiN diodes, which is one the most crucial characteristics required for reliable power devices.

- Ø JBS diodes have been designed and fabricated, showing lower leakage current levels and higher blocking voltages than Schottky diodes fabricated in the same sample. Besides, the increase of the p-type grid resistance with increasing p-type doping profile depth has been confirmed together with the need of high p-type grid doping concentration to reach the bipolar injection regime and achieve good surge current capabilities of the JBS diodes.

- Ø Good thermal behaviour of the three different rectifiers developed during this thesis (Schottky, JBS, and PiN diodes) has been demonstrated for temperatures up to 300ºC.

Thus, during this thesis research some of the more important issues linked to the development of a silicon carbide technology have been investigated and some contributions towards the development of 4H-SiC power rectifiers have been made. After the references section, the author´s published papers derived from this PhD work are listed.

The development in the silicon carbide research community is today faster than ever. After years of moderate interest additional silicon carbide material suppliers have entered

the scene during the past recent years. National and international research cooperation have identified and solved problems and developed models for the understanding of silicon carbide as the probably best understood wide band gap semiconductor. During the last years several silicon carbide based devices have been introduced to the market, most prominently radio frequency MESFETs and high power Schottky diodes. It is now up to circuit and systems engineers to make use of these first components in order to establish silicon carbide among conventional technologies.

Appendix A. Experimental Results on SiC Power Rectifiers

Table A1 List of SiC power rectifiers that have been experimentally demonstrated during the recent years.

Device type	Polytype	Power Ratings	Epilayer (thickness, doping)	Features	Developer/year
PiN	6H-SiC	2 kV 1mA	24µm, $4\times10^{15}cm^{-3}$	V_{F100} > 6V Mesa-terminated	NASA 1993
PiN	6H-SiC	4.5 kV 20mA	45µm, $1\times10^{15}cm^{-3}$	V_{F100} = 6V Mesa-terminated	Linköping U./ABB 1995
PiN	4H-SiC	6.2 kV	50µm, $1\times10^{15}cm^{-3}$	V_{F100} = 4.7V Mesa-JTE	Kansai/CREE 1999
PiN	4H-SiC	1.1 kV	10µm, $1\times10^{16}cm^{-3}$	V_{F100} = 3.5V Single JTE	Rensselaer P.I. 1999
PiN	4H-SiC	5.5 kV	85µm, $8\times10^{14}cm^{-3}$	V_{F100} = 5.0V Single JTE	Ioffe I./CREE 1999
PiN	4H-SiC	4.5 kV 5A	39µm, $2\times10^{15}cm^{-3}$	V_{F100} = 4.0V 2 zone JTE	*Si*CED 2000
PiN	4H-SiC	4.5 kV 1A	40µm, $1\times10^{15}cm^{-3}$	V_{F100} = 4.2V 3 zone JTE	Rensselaer P.I. 2001
PiN	4H-SiC	12 kV	120µm, $2\times10^{14}cm^{-3}$	V_{F100} = 4.4V Mesa-JTE	Kansai/CREE 2001
PiN	4H-SiC	19 kV	200µm, $8\times10^{13}cm^{-3}$	V_{F100} = 6.5V Mesa-JTE	Kansai/CREE 2001
PiN	4H-SiC	5 kV 5A	30µm, $1\times10^{15}cm^{-3}$	V_{F100} = 4.2V Mesa-multistep-JTE	Rutgers U. 2001
PiN	4H-SiC	10 kV 200A	150µm, $2\times10^{14}cm^{-3}$	V_{F100} = 4.9V Mesa-JTE	CREE 2001
PiN	6H-SiC	4.2 kV	31µm, $1\times10^{15}cm^{-3}$	V_{F100} = 3.75V Single JTE	Kyoto U. 2002
PiN	6H-SiC	1.4kV	10µm, $2\times10^{16}cm^{-3}$	V_{F100} = 2.92V Mesa terminated	AIST Tsukuba. 2003
PiN	6H-SiC	1.3kV	10µm, $2\times10^{16}cm^{-3}$	V_{F100} = 4.0V Single JTE	INSA Lyon 2004
PiN	4H-SiC	8.0kV	110µm, $6\times10^{14}cm^{-3}$	V_{F100} = 5.0V 4 zone mutistep JTE	Rensselaer P.I. 2004
PiN	4H-SiC	10kV 50A	100µm, $2\times10^{14}cm^{-3}$	V_{F100} = 3.9V Mesa-JTE	CREE 2004
PiN	4H-SiC	4.6kV	40µm, $4\times10^{14}cm^{-3}$	V_{F100} = 4.1V Mesa-JTE	Kansai Inc. 2004
PiN	4H-SiC	4.5kV 6A	35µm, $2\times10^{15}cm^{-3}$	V_{F100} = 3.7V Single JTE	*Si*CED 2004

Device type	Polytype	Power Ratings	Epilayer (thickness, doping)	Features	Developer/year
Schottky	4H-SiC	1.1 kV	10µm, 9×10^{15}cm^{-3}	V_{F100} = 1.3V Ti ,Φ_B = 1.17eV B^+ guard ring	Kyoto U. 1996
Schottky	4H-SiC	1.7 kV	13µm, 3×10^{15}cm^{-3}	R_{on}= 5.6mΩcm^2 Ni ,Φ_B = 1.50eV B^+ guard ring	Purdue U. 1998
Schottky	4H-SiC	3.85kV	43µm, 7×10^{14}cm^{-3}	V_{F100} = 4.4V Ni ,Φ_B = 1.30eV Field Plate	Linköping U. 1999
Schottky	4H-SiC	600V	8µm, 7×10^{15}cm^{-3}	R_{on}= 1.0mΩcm^2 Ti ,Φ_B = 1.27eV Single JTE	Infineon/Siemens 1999
Schottky	4H-SiC	4.9kV	50µm, 7×10^{14}cm^{-3}	R_{on}= 17 mΩcm^2 Ni ,Φ_B = 1.41eV B^+ guard ring	CREE 2002
Schottky	4H-SiC	10kV	115µm, 5.6×10^{14}cm^{-3}	R_{on}= 97 mΩcm^2 Ni ,Φ_B = 1.44eV Multistep-JTE	Rutgers U. 2003
Schottky	4H-SiC	4.15kV	33µm, 3×10^{15}cm^{-3}	R_{on}= 9.1 mΩcm^2 Mo ,Φ_B = 1.27eV 3 zone JTE	CRIEPI 2004
JBS	6H-SiC	1.1kV	10µm, 7×10^{15}cm^{-3}	R_{on}= 20 mΩcm^2 Ti ,Φ_B = 0.98eV 50% Schottky	KTH/ABB 1998
JBS	4H-SiC	2.8kV	27µm, 3×10^{15}cm^{-3}	R_{on}= 7.5 mΩcm^2 Ti ,Φ_B = 1.4eV 2 zone JTE	Linköping U. 1999
JBS	4H-SiC	3.6kV	50µm, 1.5×10^{15}cm^{-3}	R_{on}= 43 mΩcm^2 Ni , 50% Schottky B^+ guard ring	Kansai Inc. 1999
JBS	4H-SiC	1.5kV 4A	20µm, 2×10^{15}cm^{-3}	R_{on}= 10 mΩcm^2 Ni , 50% Schottky Single JTE	CREE 2000
JBS	4H-SiC	4.3kV	30µm, 2×10^{15}cm^{-3}	R_{on}= 21 mΩcm^2 Ti, 70% Schottky Multistep-JTE	Rutgers U. 2003
JBS	4H-SiC	1.8kV 6A	12µm, 6×10^{15}cm^{-3}	R_{on}= 6.7 mΩcm^2 Ti , 50% Schottky Multistep-JTE	Rutgers U. 2004

Appendix B. Parameters for 4H-SiC MEDICI Simulation

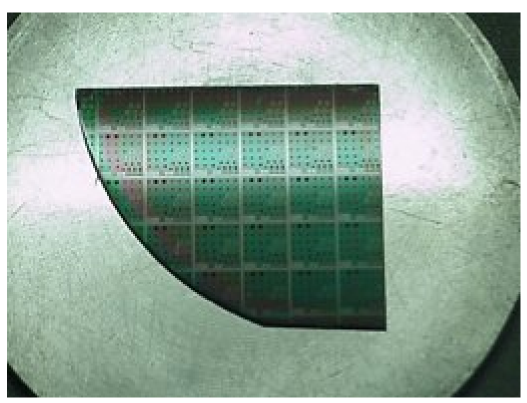
Table B.1 Parameters for 4H SiC used in device simulation.

Parameter	4H-SiC	Units	Ref.
Dielectric constant	9.76	--	[68]
Band structure			[68]
EG300	3.26	eV	
EGALPH	3.3×10^{-4}		
EG.MODEL	1	--	
NC300	1.67×10^{19}	cm^{-3}	
NV300	3.19×10^{19}	cm^{-3}	
Bandgap narrowing			[70]
ANC.BGN	-1.5×10^{-2}	--	
CNC.BGN	-2.9×10^{-3}	--	
BNV.BGN	1.9×10^{-2}	--	
CNV.BGN	8.7×10^{-3}	--	
BPC.BGN	-1.6×10^{-2}	--	
CPC.BGN	-3.9×10^{-4}	--	
APV.BGN	1.3×10^{-2}	--	
CPV.BGN	1.15×10^{-3}	--	
Incomplete ionisation			[71]
EDB	0.08	eV	
EAB	0.19	eV	
Recombination			
Shockley-Read-Hall			[73]
TAUN0	5×10^{-7}	s	
NSRHN	1×10^{-30}	cm^{-3}	
TAUP0	1×10^{-7}	s	
NSRHP	1×10^{-30}	cm^{-3}	
Auger			[73]
AUGN	5×10^{-31}	$cm^{-6}s^{-1}$	
AGP	2×10^{-31}	$cm^{-6}s^{-1}$	
Low-field mobility			[76]
MUN.MIN	40	cm^2/Vs	
MUN.MAX	950	cm/Vs	
NUN	-2.6	--	
ALPHAN	0.76	--	
NREFN	1.94×10^{17}	cm^{-3}	
MUP.MIN	16	cm^2/Vs	
MUP.MAX	117	cm^2/Vs	
NUP	-2.6	--	
ALPHAP	0.34	--	
NREFP	1.76×10^{19}	cm^{-3}	
High-field mobility			[77]
VSATN	2.2×10^{7}	cm/s	
BETAN	1.2	--	
VSATP	2.2×10^{7}	cm/s	
BETAP	1.2	--	
Impact ionisation			[85]
N.IONIZA	1.76×10^{8}		
ECN.II	3.30×10^{7}		
P.IONIZA	3.41×10^{8}		
ECP.II	2.50×10^{7}		

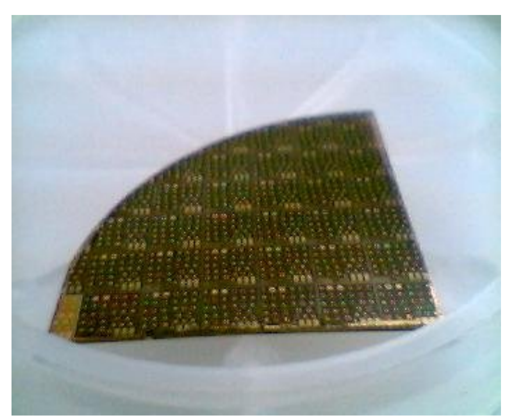
Appendix C. Samples and Processes Resume

Sample	Wafer ID	Implantations			Activation Anneal	Anode Metal	RTA processes (3min)					2nd Metal
		P^+ ($2\times10^{19}cm^{-3}$)	P ($2\times10^{18}cm^{-3}$)	P^- ($2\times10^{17}cm^{-3}$)			350ºC	500ºC	700ºC	900ºC	1025ºC	
CQ1	AD-0602-02	Al^+ (IBS)	Al^+ (IBS)	(Al^+ Bologna)	1700ºC 30min Ar	Ni/Ti	✓	✓	✓	bad	✗	Au
CQ2	AD-0602-02	Al^+ (IBS)	Al^+ (IBS)	(Al^+ Bologna)	1650ºC 45min N_2	Ni/Ti	✓	✓	✓	✓	✗	Au
CQ3	AD-0602-02	Al^+ (IBS)	Al^+ (IBS)	Al^+ (IBS)	1650ºC 45min N_2	Ni/Ti	✓	✗	✓	✓	✗	Au
CQ4	AD-0602-02	Al^+ (IBS)	Al^+ (IBS)	(Al^+ Bologna)	1650ºC 45min N_2	W/Ti	✓	✓	✓	✓	✓	---
S1	B-8141-13	Al^+ (IBS)	Al^+ (IBS)	(Al^+ Bologna)	1700ºC 30min Ar	Ni/Ti	✓	✓	✓	✓	✗	Al
S2	B-8141-13	Al^+ (IBS)	Al^+ (IBS)	(Al^+ Bologna)	1650ºC 30min N_2	W/Al/Ti	✓	✓	✓	✓	✓	---
CB1	XU-0884-01	B^+ (CNM)	r	B^+ (CNM)	1650ºC 45min Ar	Ni/Ti	✗	✗	✗	✗	✗	---
CB2	XU-0884-01	B^+ (CNM)	r	B^+ (CNM)	1650ºC 45min N_2	Ni/Ti	✗	✗	✗	✓	✗	---
CB3	XU-0884-01	B^+ (CNM)	r	B^+ (CNM)	1650ºC 45min N_2	Ni/Ti	✓	✓	✓	✓	✗	Au
CB4	XU-0884-01	B^+ (CNM)	r	B^+ (CNM)	1650ºC 45min N_2	Ni/Ti	✗	✗	✗	✓	✗	Au

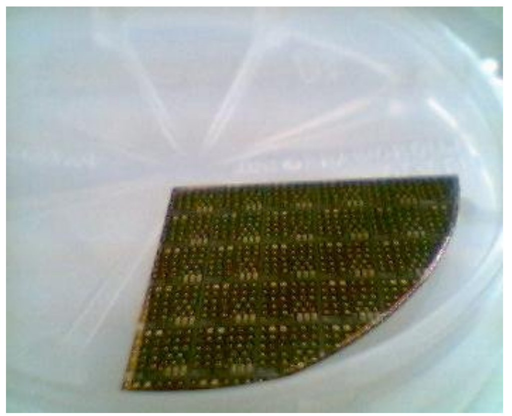
Sample CQ1



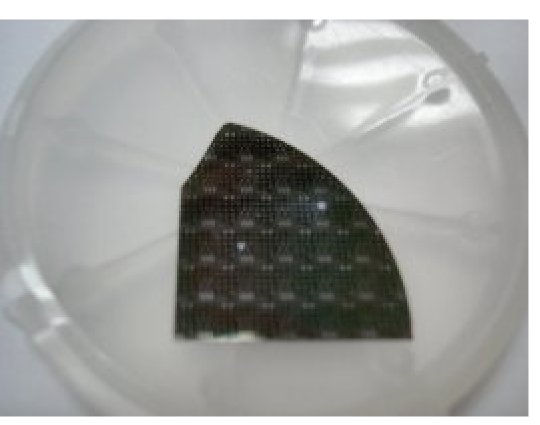
Sample CQ2



Sample CQ3

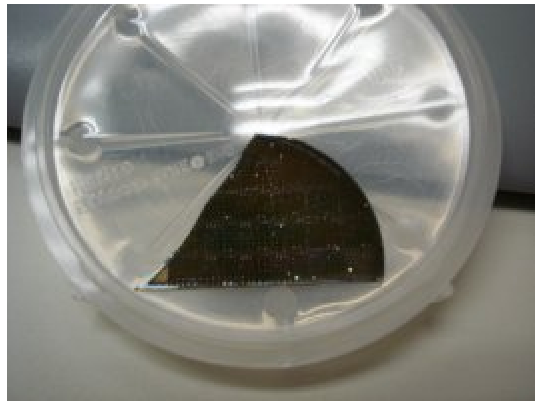


Sample CQ4



Sample S1

Sample S2



Appendix D. Metal-semiconductor Junctions

D.1 Schottky barrier formation

When a metal and a semiconductor are brought in contact, the respective Fermi-levels must coincide in thermal equilibrium as shown in Figure C.1 (b). There are two limiting cases such as the ideal case (referred to as Schottky-Mott limit [195]) and a practical case (known as the Bardeen limit [196]) to describe the relationship between a metal and a semiconductor. Figure C.1 shows the energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states.

In this case the barrier height for n-type semiconductor can simply be determined to be the difference between the metal work function (ϕ_m) and electron affinity (χ_s) of the semiconductor;

$$q\phi_{Bn} = q(\phi_m - \chi_s) \tag{C.1}$$

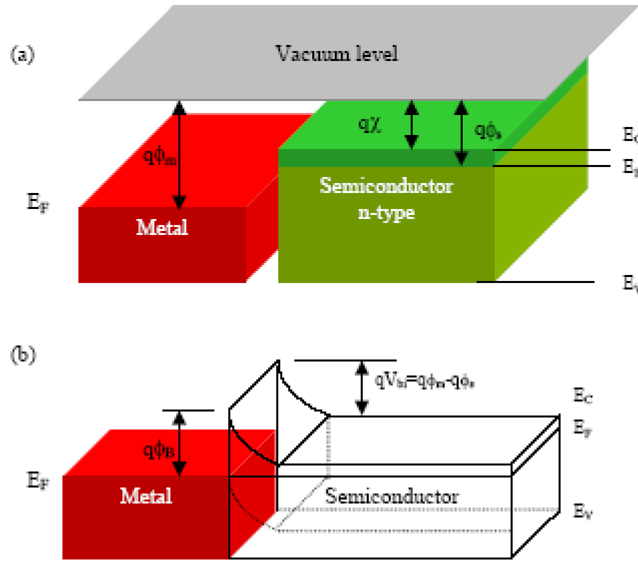


Figure C.1 The formation of a barrier between the metal and the semiconductor when (a) neutral and isolated and (b) in perfect contact without any oxide between them (Schottky-Mott limit).

For a given semiconductor and a metal, the sum of the barrier height on n- and p-type semiconductor is expected to be equal to the energy bandgap

$$q(\phi_{Bn} + \phi_{Bp}) = E_g \tag{C.2}$$

This relationship for Schottky-Mott limit implies that the control of the barrier height is achieved by the choice of the metal. The second limiting case is the Bardeen limit where a

large density of states is present at the semiconductor to metal interface. In the Bardeen limit the barrier height ϕ_B is completely independent of the metal work function ϕ_m in contrast to the Schottky-Mott limit and the Fermi level is said to be pinned by the high density of interface states.

Recent results on Schottky contact formation on SiC [197,198] indicate that the Schottky barrier height strongly depends on the metal work function even though there is partial Fermi level pinning. Figure C.2 summarizes the barrier height from C-V and I-V for n- and p-type 4H-SiC as a function of the metal work function. From the Schottky-Mott limit, the sum of the Schottky barrier height for n- and p-type semiconductor should be given by ($\phi_{Bn}+\phi_{Bp} \approx E_g$-4H-SiC). From Figure C.2, the sum of the SBH is very close to the energy band gap of 4H-SiC, satisfying the Schottky-Mott model without strong Fermi-level pinning. It also indicates that n-type Schottky barrier diodes have weaker Fermi-level pinning compared to p-type Schottky diodes. In addition, the plot of various metals as a function of the metal work function is shown in Figure C.3. It shows there is a great deal of scatter in the experimental data for a given metal on 4H-SiC. As pointed out above the surface contribution caused by different sample preparation and surface quality are important factors to have good Schottky barrier diodes without strong Fermi level pinning.

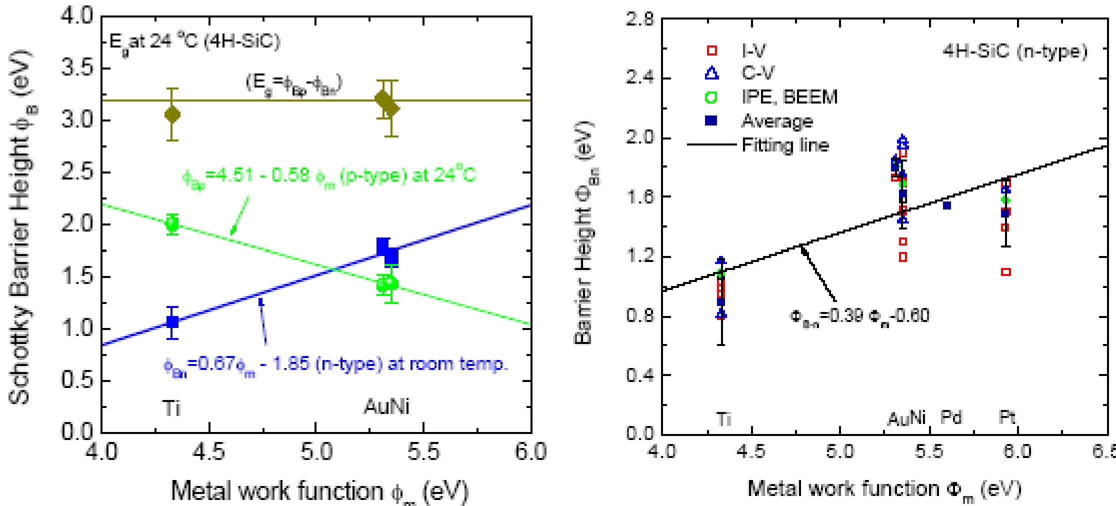


Figure C.2 Schottky barrier heights o Ni, Ti, and Au to both n- and p-type type 4H-SiC as a function of the metal work function [197].

Figure C.3 Schottky barrier heights of various metals on n-type 4H-SiC as a function of the metal work function.

D.2 Current transport mechanism

Figure C.4 shows four basic transport processes for n-type semiconductors under forward bias [143]. The four processes are a) emission of electrons from the semiconductor over the top of the barrier into the metal, b) quantum mechanical tunnelling through the barrier, c) recombination in the space-charge region, and d) recombination in the neutral region (called hole injection).

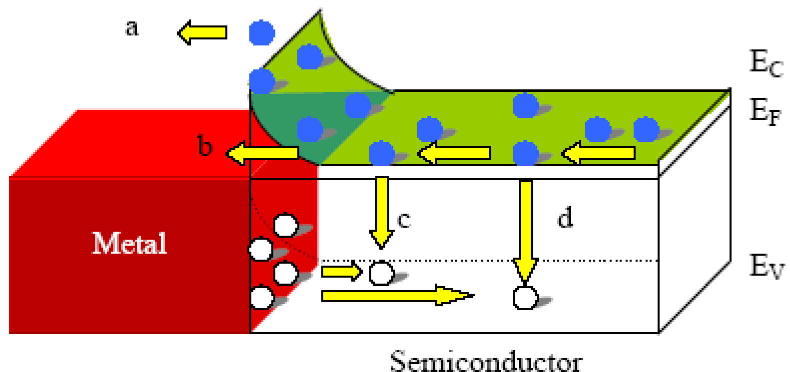


Figure C.4 Current transport processes in a forward-biased Schottky barrier.

For the lowly doped semiconductor the current flows as a result of thermionic emission (TE) as shown in Figure C.5 (a) with electrons thermally excited over the barrier. In the intermediate doping range, thermionic field emission (TFE) dominates as shown in Figure C.5 (b).

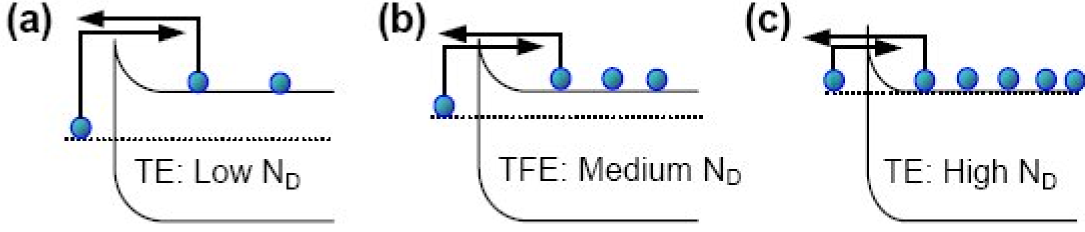


Figure C.5 Energy band diagram for (a) low doped, (b) intermediate doped, and (c) high doped n-type semiconductor. The arrow indicates the electron flow.

For high doping, the barrier is sufficiently narrow at or near the bottom of the conduction band for the electrons to tunnel directly, known as field emission (FE). The three regimes can be distinguished by considering the characteristic energy E_{00} defined by [198]

$$E_{00} = \frac{q\mathbf{h}}{2}\sqrt{\frac{N_D}{m^*_{tun}\boldsymbol{e}_S}} = 8.82\times10^{-12}\sqrt{N_D} \qquad \text{[eV]} \qquad \text{(C.3)}$$

where N_D is the doping concentration, m^*_{tun} (≈0.45m$_0$ for 4H-SiC) is the effective tunnelling mass, and e_s (≈ 9.76ε$_0$) is the dielectric constant for SiC. Using Equation B.3 a plot of the characteristic energy E_{00} as a function of doping density is shown in Figure B.6. The relationship between temperature and doping which determines which conduction mechanism is dominant is given by

field emission for $kT << qE_{00}$,

thermionic field emission for $kT » qE_{00}$,

thermionic emission for $kT >> qE_{00}$,

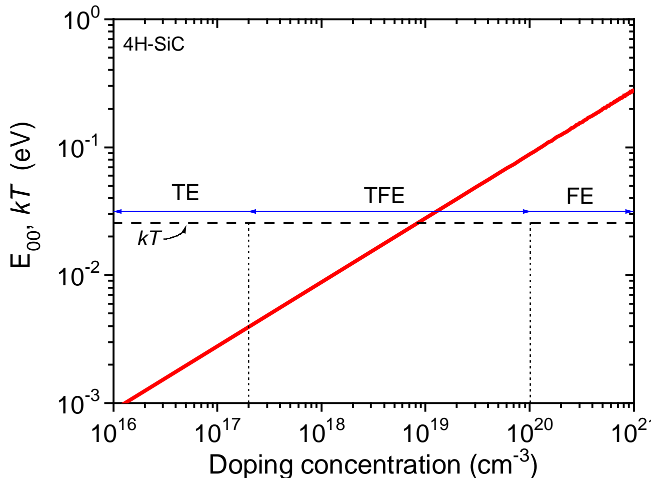


Figure C.6 E_{00} and thermal energy kT as a function of the doping density for 4H-SiC with m^{*}_{tun}/m_0=0.45, T=300K.

D.3 Ohmic contact formation

Ohmic contacts may be considered a limiting case of the more general class of Schottky contacts. A metal-semiconductor combination that upon preparation has Schottky characteristics can be converted into an ohmic contact with certain processing steps that modify the Schottky barrier. Although there are metal-semiconductor combinations which are ohmic as prepared, these too have a Schottky barrier at the metal-semiconductor interface which is either too low or too thin to produce an asymmetric *I-V* characteristic.

Contact resistance is a term that describes the electrical resistance present at the interface between the metal and semiconductor in an ohmic contact. The contact resistance associated with an ohmic metal-semiconductor interface is the total electrical resistance of the interface and depends on the area or geometry of the contact. The interface itself, however, has certain properties which influence the contact resistance, R_c, independent of the contact geometry. This interfacial property is known as the specific contact resistance, ρ_c , and should in principal be independent of the area of the metal-semiconductor interface. The difference in contact resistance and specific contact resistance is analogous to the difference in the resistance R of a standard carbon resistor and

the resistivity ρ of the carbon from which the resistor is made; the resistance is equal to the resistivity times a geometric factor, specifically the length l divided by the cross sectional area A or $R=\rho \cdot l/A$. Similarly the contact resistance of a metal-semiconductor interface is equal to the specific contact resistance divided by the cross-sectional area of the metal-semiconductor interface or $R_c=\rho_c/A$; this of course assumes the entire contact area takes part in the conduction process which is not always true. The units of contact resistance are Ω while

specific contact resistance has units of Ω times length squared. Generally the unit of length used is cm thus specific contact resistance is given in $\Omega{\cdot}cm^2$. The specific contact resistance is related to the current density *J* (units of A/cm^2) by

$$r_C = \left[\frac{\partial V}{\partial J}\right]_{V\to 0} \tag{C.4}$$

and, can be calculated by using the following equations for each current transport process [197].

$$\rho_C = \frac{k}{qA^*T}\exp\left(\frac{\varphi_B}{kT}\right) \quad \text{for TE} \tag{C.5}$$

$$\rho_C = \frac{k\sqrt{E_{00}}}{qA^*\sqrt{p(\varphi_B + U_f)}}\cosh\left(\frac{E_{00}}{kT}\right)\coth\left(\frac{E_{00}}{kT}\right)\exp\left(\frac{\varphi_B + U_f}{E_0} - \frac{U_f}{kT}\right) \quad \text{for TFE} \tag{C.6}$$

$$\rho_C = \left[\frac{A^*\pi qT^2}{kT\sin(\pi ckT)}\exp\left(\frac{-\varphi_B}{E_{00}}\right) - \frac{A^*cq^2T^2}{c^2k^2q}\exp\left(\frac{-\varphi_B}{E_{00}} - cU_f\right)\right]^{-1} \quad \text{for FE} \tag{C.7}$$

where A* is the modified Richardson´s constant, U_f is the Fermi level with respect to the band edge, and E_0 and *c* are given by

$$E_0 = E_{00}\,coth\left(\frac{E_{00}}{kT}\right) \qquad c = \frac{1}{2E_{00}}ln\left(\frac{4j_B}{U_f}\right) \tag{C.8}$$

The theoretical specific contact resistance for different doping concentration can be calculated using equation C.5 to C.7. For example, Schottky barrier height for a 0.3eV and surface concentration of $1\times10^{19}cm^{-3}$, the specific contact resistance is $1.0\times10^{-6}\ \Omega cm^2$ using equations C.3, C.4 and C.7.

For ohmic contacts with high doping concentrations, the predominant mode of conduction is field emission. Taking the expression for the forward field emission current one can show that the specific contact resistance ρ_c is proportional to the exponential of the barrier height divided by the square root of the doping or

$$r_C \propto exp\left(\frac{j_B}{\sqrt{N}}\right) \tag{C.9}$$

This relationship is very useful for predicting trends in contact resistance as a function of barrier height and the semiconductor doping.

Lower specific contact resistances are usually obtained to *n*-type 4H- and 6H-SiC (~10^{-4}–10^{-6} Ωcm^2) than to *p*-type 4H- and 6H-SiC (~10^{-3}–10^{-5} Ωcm^2). Consistent with narrow-bandgap ohmic contact technology, it is easier to make low resistance ohmic contacts to heavily doped SiC. Regardless of doping, it is common practice with SiC to thermally anneal ohmic contacts to obtain the minimum possible contact resistance. Most SiC ohmic contact anneals are performed at temperatures around 900-1000°C in non-oxidizing environments. Depending on the contact metallisation employed, this anneal generally causes limited interfacial reactions (usually metal carbide or metal silicide formation) that broaden and}or roughen the metal-semiconductor interface.

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