

# Work Function Tuning in Sub-20nm Titanium Nitride (TiN) Metal Gate: Mechanism and Engineering

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# ABSTRACT

## Work Function Tuning in Sub-20nm TiN Metal Gate- Mechanism and Engineering

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Scaling of transistors (the building blocks of modern information age) provides faster computation at the expense of excessive power dissipation. Thus to address these challenges, high-k/metal gate stack has been introduced in commercially available microprocessors from 2007. Since then titanium nitride (TiN) metal gate's work function ( $W_f$ ) tunability with its thickness (thickness increases, work function increases) is a well known phenomenon. Many hypotheses have been made over the years which include but not limited to: trap charge and metal gate nucleation, nitrogen concentration, microstructure agglomeration and global stress, metal oxide formation, and interfacial oxide thickness. However, clear contradictions exist in these assumptions. Also, nearly all these reports skipped a comprehensive approach to explain this complex paradigm. Therefore, in this work we first show a comprehensive physical investigation using transmission electron microcopy/electron energy loss spectroscopy (TEM/EELS), x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) to show replacement of oxygen by nitrogen in the metal/dielectric interface, formation of  $TiON_x$ , reduction of Ti/N concentration and grain size increment happen with TiN thickness increment and thus may increase the work function. Then, using these finding, we experimentally show 100meV of work function modulation in

10nm TiN Metal-oxide-semiconductor capacitor by using low temperature oxygen annealing. A low thermal budget flow (replicating gate-last) shows similar work function boost up. Also, a work function modulation of 250meV has been possible using oxygen annealing and applying no thermal budget. On the other hand, etch-back of TiN layer can decrease the work function. Thus this study quantifies role of various factors in TiN work function tuning; it also reproduces the thickness varied TiN work function modulation in single thickness TiN thus reducing the burden of complex integration and gate stack etch; and finally it shows that in a low thermal budget flow, it is more effective to achieve higher work function.

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# LIST OF ABBREVIATIONS

MOSCAP	Metal Oxide Semiconductor Capacitor
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
PMOS	p-channel Metal Oxide Semiconductor
NMOS	n-channel Metal Oxide Semiconductor
MTCMOS	Multi-threshold CMOS
TiN	Titanium Nitride
ALD	Atomic layer deposition
XPS	X-ray photoelectron spectroscopy
EELS	Electron energy loss spectroscopy
TEM	Transmission electron microscope
SIMS	Secondary ion mass spectroscopy
XRD	X-ray diffraction
PDA	Post Deposition Annealing
TEOS	Tetraethyl orthosilicate
STI	Shallow trench isolation

# LIST OF SYMBOLS

$V_t$	Threshold voltage
$V_b$	Bias voltage
$V_G$	Gate voltage
$V_{FB}$	Flatband voltage
$EOT$	Effective oxide thickness
$E_C$	Conduction band energy
$E_V$	Valence band energy
$E_F$	Fermi Energy
$E$	Energy
$E_g$	Energy gap
$E_{vacuum}$	Vacuum level energy
$\Phi_M$	Metal work function
$\Phi_S$	Silicon work function
$\Psi_S$	Surface potential
$\Psi_F$	Fermi potential
$\psi_i$	Intrinsic potential

$\chi$	Electron affinity
$q$	Electronic charge
$N_b$	Donor or acceptor concentration
$n_i$	Intrinsic carrier concentration
$C_g$	Gate capacitance
$C_{ox}$	Oxide capacitance
$C_{Si}$	Silicon capacitance
$Q_S$	Total charge per unit area induced in the silicon
$\epsilon_{ox}$	Permittivity of silicon dioxide
$\epsilon_S$	Permittivity of silicon
$t_{ox}$	Thickness of silicon dioxide
$W_D$	Depletion width

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# CHAPTER I: INTRODUCTION

## 1.1 GENERAL INTRODUCTION

The metal–oxide–semiconductor field-effect transistor (MOSFET) which is the basic unit in a microprocessor integrated circuit is a 4-terminal electronic device used for switching electronic signals in the microprocessor. The multitude of functionality of a microprocessor depends of the number of transistor that can be inexpensively incorporated in the whole chip without increasing power dissipation a lot. Dr. Jack Kilby demonstrated first integrated circuit (IC) in 1958 [1] where all the components of the circuit were fully integrated [2]. Based on that pioneering work, present advancement permits the integration of billions [3] of transistors on a piece of silicon substrate.

Transistors in integrated circuit technology have constantly migrated to smaller feature sizes over the years and the integration of more transistors and circuit elements have been possible on the same small piece of silicon substrate. This increased capacity per unit area at a decreasing cost increases the functionality per cost. This trend closely follows Moore's law [4, 5] which states that the number of transistors that can be integrated on a chip doubles approximately every two years. Because the number of transistors increases in the same given area, thus the transistor size gets smaller. Significant technological advancements have been exercised to keep the cost lower but the overall power dissipation increases. But the integrated circuits with nanoscale transistor are having several problems; one of the major problems is the sub-threshold leakage [6]. These problems are likely to be solved or at least amended by introducing of high-k gate

dielectrics instead of conventional silicon dioxide ( $\text{SiO}_2$ ) dielectric. At the same time, metal gates are also introduced instead of poly-silicon gates to solve the issues such as poor bonding between poly-silicon gate and high-k dielectric, phonon scattering in channel region and uneven dielectric trap charges. For these reasons, since 2007, semiconductor industry has introduced high-k/metal gate stacks instead of classical  $\text{SiO}_2$ /poly-silicon gate [7]. Among the few materials which are well established in present technology, titanium nitride is proved as remarkably stable [8].

TiN is a mid-gap work-function material and well-known for work function tunability i.e. the work function of TiN metal gate can be varied with the thickness of the TiN layer. As the work function is related to the threshold voltage of the transistor, the threshold voltage of the transistors can be varied by varying the thickness of TiN layer. This paves a way to have multi-threshold voltage device on the chip.

The potential of the multiple threshold CMOS (MTCMOS) is that it employs transistor devices with multiple threshold voltages ( $V_t$ ) to for power or delay optimization. Lower threshold voltage transistors offer faster operation than that of higher threshold transistors. These transistors can be used on the circuit path where delay is higher so that the whole circuit does not become slow. But the consequence of using low threshold devices is larger power dissipation. Power dissipation is lower in higher threshold voltage transistors though they operate in slower speed. So higher threshold devices can be used in the circuit path where delay is not critical; using these devices can decrease static leakage power dissipation. Generally a higher threshold voltage device decrease static leakage by 10 times compared to a lower voltage threshold device. However, one way to have transistors with different threshold voltages in a same circuit

is to apply different bulk bias voltages in different transistors; the other way is the gate work function engineering. In a NMOS transistor, lower bias voltage will enhance voltage, decrease the performance, and decrease static leakage. A common method to decrease power dissipation in multiple threshold CMOS circuit is to use higher threshold transistor as sleep transistor. This sleep transistor is connected to a virtual power rail which supply power to the set of lower threshold transistors in which the logic operation is faster but power dissipation is higher. By turning off the virtual power rail through sleep transistor, the transistor set can be turned off and power can be saved when there is no logic operation in that specific circuit block [9].

## 1.2 MOTIVATION

As we discussed in previous section, the ability of TiN gate metal to tune its work function can pave a way to have mutli-threshold ( $V_t$ ) device in a chip and multi-threshold CMOS is one of the approaches to have the optimization of power consumption and speed of the operation of the whole chip. Normally it is well-observed that the work function of TiN metal gate can be varied by changing the thickness of the TiN layer. So the threshold voltage of MOSFET with TiN metal gate can be tuned by varying the thickness of TiN metal. To get the multi-threshold devices in a same chip, we have to have TiN layers of different thicknesses in different devices.

But the integration of TiN layers of different thickness in different transistors on the same substrate is quite complex. The etching of deposited the subsequent layers (such as contact layers) on different TiN thicknesses is a process technology nightmare and a uniform gate stack profile may not achieved because of this problem [Figure 1]. Here

three MOS gate stacks with three different TiN thicknesses are etched to have MOS structure. As they are on the same substrate, the left MOS is over-etched while the right one is under-etched. As any of them are not expectable in any integration, the work function tuning using different metal gate thicknesses is not a good idea. So our mission is to investigate an alternative way to tune the work function of TiN metal gate with easier process without changing the metal gate thickness.

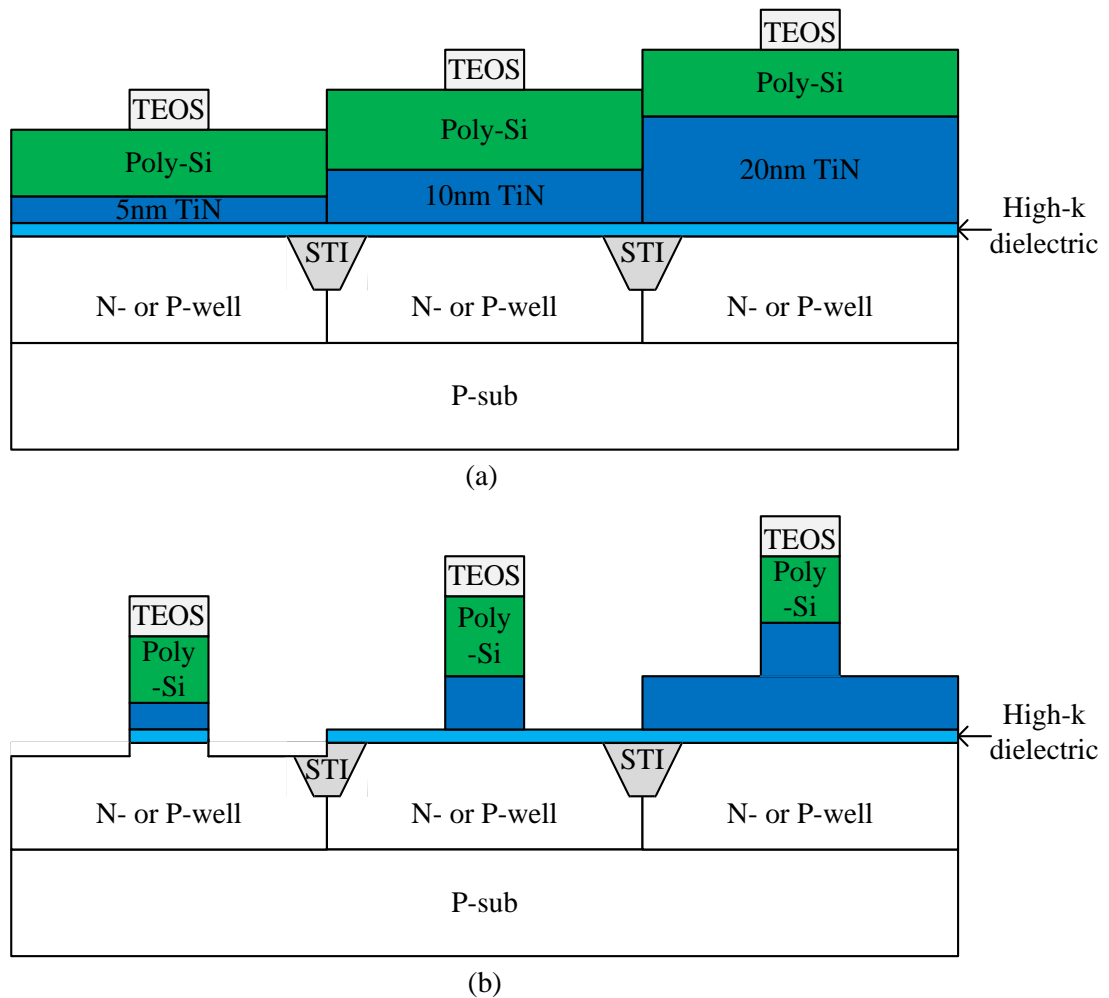


Figure 1: Process technology nightmare of etching the gate stacks with different metal gate thickness. (a) gate stacks before etching and (b) after etching.

### **1.3 OBJECTIVES**

To investigate a better solution to tune TiN work function without changing the thickness, we first need to understand why the work function modulates with thickness change. So we have done comprehensive physical investigation using transmission electron microscope/electron energy loss spectroscopy (TEM/EELS), secondary ion mass spectroscopy (SIMS), x-ray photoelectron spectroscopy (XPS) and x-ray diffraction (XRD). Based on the developed understanding from the physical investigation, we applied some appropriate processes to replicate the same work function tuning mechanism without changing the thickness. Then, the measurement of capacitance versus voltage (*CV*) characteristics of the Metal Oxide Semiconductor Capacitor (MOSCAP) and analysis of that data to plot the flat band voltages ( $V_{FB}$ ) versus effective oxide thickness (EOT) verifies the change of the flat band voltage i.e. the change of the work function to TiN metal gate.

### **1.4 THESIS ORGANIZATION**

A comprehensive physical investigation of work function tuning with thickness and investigation of alternative to tune the work function of TiN gate metal is the scope of this study. For this purpose, we investigated the fabricated metal-oxide-semiconductor structure. So the physics of metal-oxide-semiconductor is related to this study. Also, the review of the previous attempt for the related investigation is in the scope of this study.

So chapter II describes the physics behind the fabricated structure as well as the review of the related literature. Chapter III describes the fabrication process steps. The first part of chapter IV analyzes the mechanism of changing work function with thickness change

based on the experimental result and analysis. The second part of chapter IV investigates the work function engineering based on study described in the first part of the chapter IV and studies the work function modulation due to the engineering adopted. The last chapter provides the general conclusion and discusses the limitation and future directions.

# CHAPTER II: REVIEW OF LITERATURE

## 2.1 MOS CAPACITOR

As the metal-oxide-semiconductor (MOS) structure is basis for the MOS field effect transistor (MOSFET), we will concentrate on the MOS capacitor structure to study the work function of metal gate. After reviewing the brief physics of MOS structure which has been studied extensively by Nicollian and Brews[10], we will discuss the related literature.

Figure 2 shows a MOS capacitor which consists of a silicon substrate, a thin dielectric layer (silicon dioxide) and a conducting gate electrode (metal or heavily doped polysilicon). There is another metal layer to form the contact on the backside of the substrate. Here, the substrate has a p-type and silicon dioxide is used as the dielectric layer.

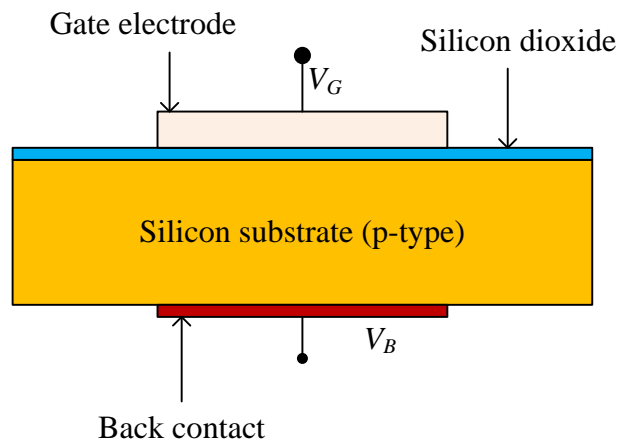


Figure 2: MOS capacitor structure [11].

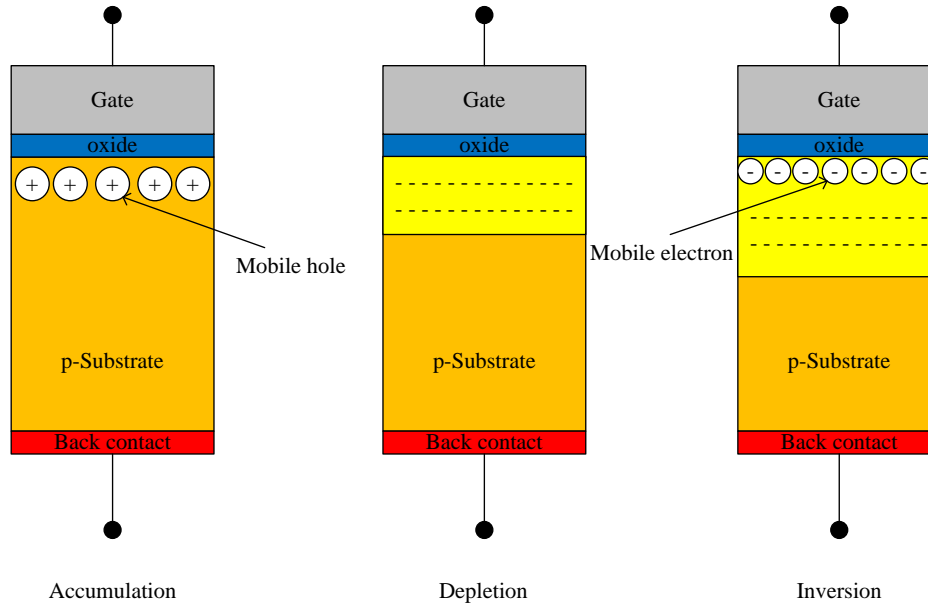


Figure 3: Different modes in an n-channel MOS structure [11].

To understand the operation, let us explain the voltages in the three modes of operation such as accumulation, depletion and inversion respectively (Figure 3).

Accumulation mode normally takes place when a negative voltage is applied between the metal or polysilicon gate and back contact. Here the gate negative charges attract holes from the p-substrate to the interface of substrate and oxide. Depletion mode occurs normally when positive voltages are applied. The gate positive charges push the holes into the p-type substrate. So at the interface, the substrate is depleted of carriers and acceptor ions negative charges are left in the depletion region. When a voltage greater than the threshold voltage is applied, inversion occurs. At that time, not only holes are depleted but also free electrons gather at the surface i.e. the surface behaves like n-type material. This n-type surface is not formed by doping; it is formed by inverting the p-type substrate with an electric field [11, 12].



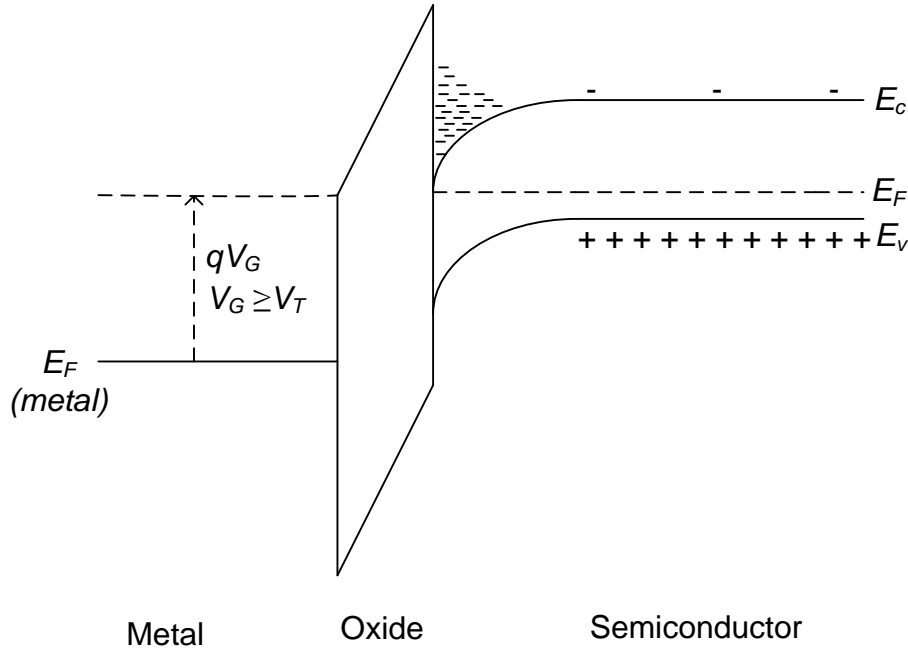


Figure 4: Inversion Mode Energy diagram for a MOS structure[11].

Figure 4 shows the band diagram of an n-channel MOS capacitor operating in inversion mode. After entering into the depletion mode, when the positive gate voltage increases, depletion region increases resulting in more band bending in semiconductor. When the band bending increases in such extent that the conduction band edge becomes almost same as the Fermi level, the device enters into the inversion mode[10, 12].

Before discussing the flatband condition which is our point of interest, let us discuss about the work function. Work function is the difference between the energy of the free electron level and that of the Fermi level. The work function for p-type silicon can be define as

$$\phi_s = \chi + \frac{E_g}{2q} + \psi_B \dots \dots \dots (1)$$

Here  $E_g$  is the energy gap,  $q$  is the electronic charge,  $\chi$  is the electron affinity and  $\psi_B$  is

the difference between the Fermi potential  $\psi_f$  and the intrinsic potential  $\psi_i$  and define by following equation

$$\psi_B = |\psi_f - \psi_i| = \frac{kT}{q} \ln\left(\frac{N_b}{n_i}\right) \dots \dots \dots (2)$$

where  $N_b$  is the donor or acceptor concentration,  $n_i$  is the intrinsic carrier concentration,  $k$  is the Boltzmann constant[12].

Figure 5 shows the band diagram of an MOS structure under the flatband condition when the energy bands in semiconductor become flat. As the silicon work function is greater than that of metal, we achieve this flatband condition by applying a negative gate voltage which is equal to  $\Phi_{MS} = -(\Phi_M - \Phi_S)$ . This voltage is called the flatband voltage. Flat band condition occurs when no charge exists in the semiconductor and the semiconductor energy bands become flat[12].

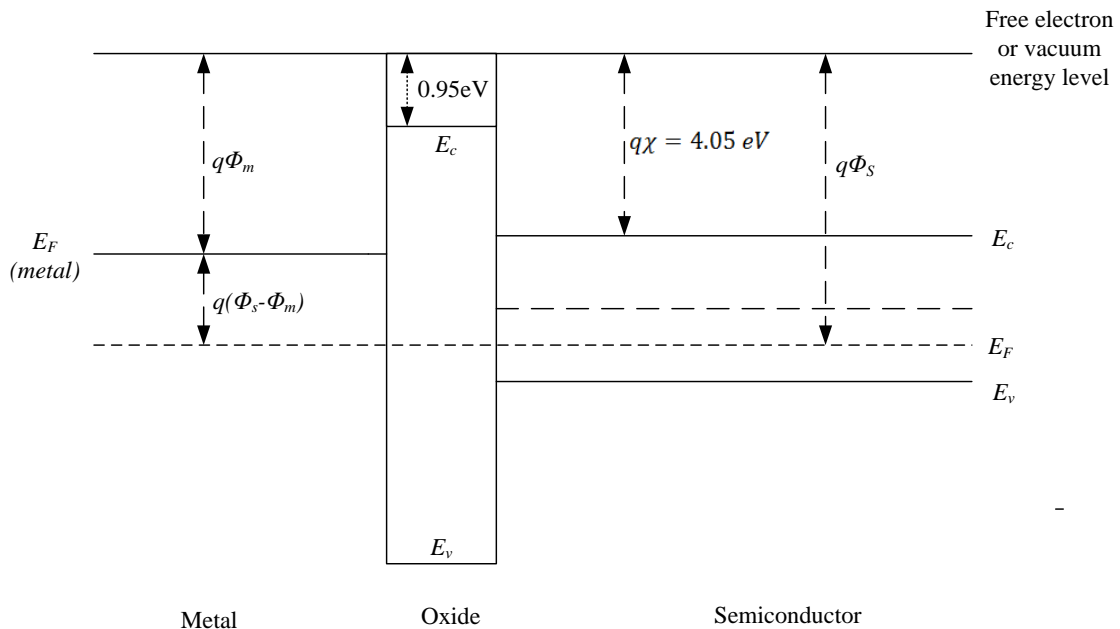


Figure 5: Energy band diagram under the flat band condition[11].

The flatband voltage of an MOS device is given by

$$V_{fb} = \phi_m - \phi_s - \frac{Q_{ox}}{C_{ox}} \dots \dots \dots (3)$$

where  $\phi_m$  is the work function of the gate metal,  $\phi_s$  is the work function of semiconductor,  $Q_{ox}$  is the equivalent oxide charge per unit area at the oxide-silicon interface and  $C_{ox}$  is the oxide capacitance per unit area [12]. If  $Q_{ox}=0$ , then from (3), we get

$$V_{fb} = \phi_m - \phi_s \dots \dots \dots (4)$$

where  $\phi_m - \phi_s = \phi_m - \chi - \frac{E_g}{2q} - \frac{kT}{q} \ln \left( \frac{N_b}{n_i} \right)$  [using equation (1) and (2)]

If the interface charge and the charge density distribution are considered, the flatband voltage is given by:

$$V_{fb} = \phi_m - \phi_s - \frac{Q_{ox}}{C_{ox}} - \frac{1}{\epsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx \dots \dots \dots (5)$$

Here,  $Q_i$  is the charge located at the interface between the semiconductor and semiconductor substrate,  $\rho_{ox}$  is the charge density distributed within the oxide. [12].

The threshold voltage is given the following relation.

$$V_T = V_{fb} + 2\phi_F + \frac{\sqrt{4\epsilon_s q N_a \phi_F}}{C_{ox}} \dots \dots \dots (6)$$

Here,  $N_a$  is the substrate doping concentration,  $\phi_F$  is the Fermi level work function and  $C_{ox}$  is the oxide capacitance.

## 2.2 CAPACITANCE-VOLTAGE CHARACTERISTICS

Figure 6 shows the equivalent circuits of an MOS capacitor. Let us assume that all the silicon capacitances are lumped into  $C_{Si}$ . Then the gate capacitance can be given by the following relation[12]:

$$\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} = \frac{1}{C_{ox}} - \frac{d\psi_S}{dQ_S} \dots \dots \dots (7)$$

$$\text{where } C_{Si} = \frac{d(-Q_S)}{d\psi_S} \dots \dots \dots (8)$$

Here,  $Q_S$  is the total charge per unit area induced in the silicon and  $\psi_S$  is the surface potential.

When the  $C_{Si}$  is divided into a depletion charge capacitance,  $C_d$  and an inversion-layer capacitance,  $C_i$ . The depletion charge capacitance comes from the majority carriers and has response for both high and low frequency signals. The inversion layer capacitance

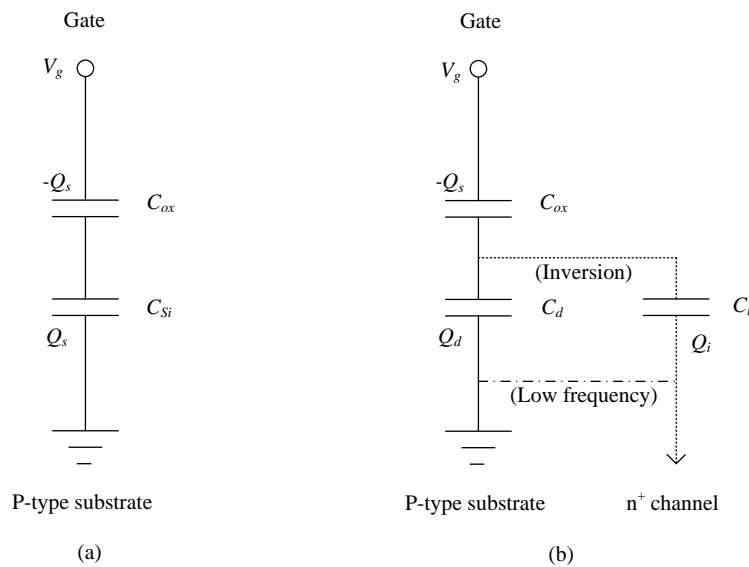


Figure 6: Equivalent circuit of an MOS capacitor. (a) All the silicon capacitance is expressed as  $C_{Si}$ ; (b)  $C_{Si}$  is divided into a depletion charge capacitance,  $C_d$  and an inversion layer capacitance,  $C_i$  [12].

arises from the minority carriers and has response for only low frequency signals unless the surface inversion channel is connected to a reservoir of minority carrier. The depletion charge capacitance is given by

$$C_d = \frac{\epsilon_{Si}}{W_D} \dots \dots \dots (9)$$

Here  $W_D$  is the depletion layer width.

Figure 7 shows the capacitance-voltage characteristics of a p-type MOS capacitor. When the voltage applied to the gate is negative and less than the flatband voltage by a value which is more than a few  $kT/q$ , the p-type MOS capacitor, the p-type MOS capacitor is in accumulation and the capacitance becomes maximum which is given by [13]

$$C_g \approx C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \dots \dots \dots (10)$$

In depletion region,

$$C_g = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_S} W_D} \dots \dots \dots (11)$$

As the depletion width  $W_D$  increases with the increase of voltage in the depletion region, capacitance decreases with the increase of the voltage according to equation (11).

For low frequency signals, as the gate voltage increases, the capacitance stops decreasing when  $\psi_S = 2\psi_B$  [12]. Here, the inversion of the channel happens and the capacitance begins to increase. Here the value of  $C_{Si}$ , the variation of the inversion charge with respect to  $\psi_S$  is much larger than  $C_d$ . The silicon charge is mainly the inversion charge and the capacitance values can be assumed same as in accumulation region expressed by equation (10).

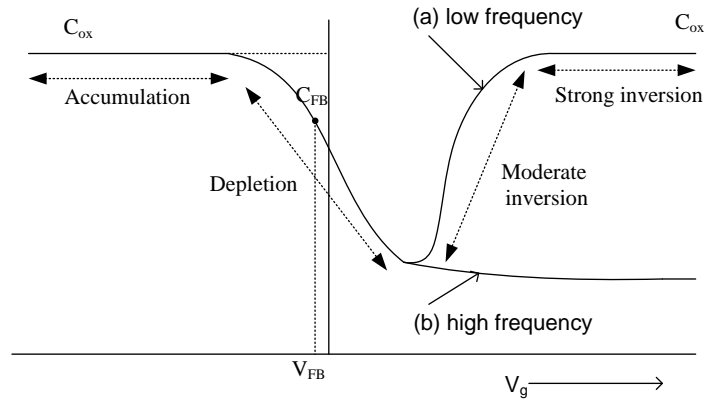


Figure 7: MOS capacitor-voltage(CV) characteristics: (a) low frequency and (b) high frequency[12].

For high frequency signals, as we have discussed earlier,  $C_i$  cannot respond i.e. the inversion charges cannot respond to ac signal; only depletion charge can respond. So the capacitance is mainly given by the depletion capacitance.

### 2.3 TiN AS A METAL GATE WITH HIGH-K DIELECTRIC

As the gate leakage through the silicon dioxide gate increases with the decrease of gate dielectric thickness due to scaling down of CMOS transistor, high-k gate dielectric came as the better alternative to reduce the gate leakage. Because of higher capacitance values, high-k dielectric is able to maintain the performance with decreasing leakage. But using the same poly-silicon as the gate electrode creates some problems i.e. poor bonding between gate and dielectric increased the threshold voltages and phonon-scattering in channel and uneven dielectric surface trap charges became problematic. However, the incorporation of metal gate instead of the poly-silicon gate solves the problems because the metal gate bond well with high-k dielectric. So the high-k/metal gate stack becomes

an unavoidable choice [13-16] and since 2007, semiconductor industry has migrated to high-k/metal gate stacks. Now the metal gate selection with correct work function is important for getting a specific threshold voltage. As titanium nitride (TiN) is a metal with a mid-gap work-function (the term 'mid-gap' denotes the average of the work functions of p+ poly-Si/SiO<sub>2</sub> and n+ poly-Si/SiO<sub>2</sub>), it is one of the metals which is selected as metal gate electrode. An additional property of TiN is that its work-function is tunable with the metal film thickness. So getting a specific threshold voltage is possible by using specific thickness of TiN.

# CHAPTER III: EXPERIMENTAL METHODOLOGY

## 3.1 INTRODUCTION

Our experimental samples are prepared on heavily doped p-type Si (100) substrates. A gate dielectric consisting of chemical SiO<sub>2</sub> as a host interface and post-deposition NH<sub>3</sub> annealed 2nm thick hafnium dioxide (HfO<sub>2</sub>) was then deposited by atomic layer deposition (ALD). Then a series of 5, 10 and 20nm thick TiN (metal gate film) were deposited using ALD on top of the gate dielectric. Multiple samples are prepared in each split to ensure statistical accuracy. Next a 100nm poly-Si was deposited using chemical vapor deposition. Then a spike anneal was carried out at 1000°C for 1 sec to imitate the actual device [17-19]. The characterization was done by using transmission electron microscope/electron energy loss spectroscopy (TEM/EELS), x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) to analyze the samples. By these analyses, we understand the possible reasons for increasing the work function with increasing the TiN metal thickness.

Based on the developed understanding by analyzing the samples, another batch of experimental samples was prepared. First, following the same steps as in the previous samples, just after TiN metal deposition, the nitrogen implantation was done in several samples and the oxygen anneal was carried out in some samples. Then, after poly-silicon deposition and subsequent P-implantation, short activation anneal is carried out in several samples, long anneal is done in some samples and no anneal is done in a sample.



After having the second batch of devices, we measured the capacitance-voltage (CV) characteristics of the fabricated MOS capacitors. The total number of CV characteristics measured is 540. In order to confirm enough accuracy, at least five devices of same size of the same sample are measured. For each CV characteristic, 152 data points are collected with small step of 0.05V.

### 3.2 FABRICATION STEPS

Here are the details of fabrication steps. The layers are not drawn to scale.

1. **Oxidation:** A set of P-type,  $\langle 100(\pm 0.5) \rangle$  orientated, 180nm lithograde general purpose test wafers is used as the substrates. Oxidation is done to have 550nm of  $\text{SiO}_2$  layer on the substrate [Figure 9].
2. **Lithography:** Photoresist is deposited, baked and UV exposed through the mask. Then the photoresist are developed to have the opening on photoresist where the device will be fabricated.
3. **Reactive ion etching:** It is done to etch the 550nm oxide layer through the opening of photoresist [Figure 10].

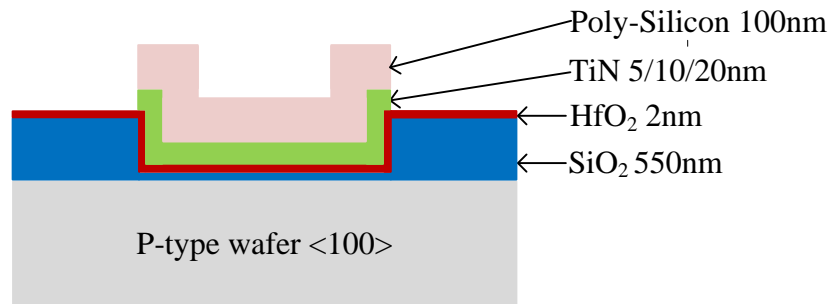


Figure 8: Fabricated MOSCAP structure.

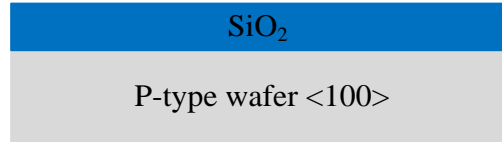


Figure 9: Oxidized wafer.

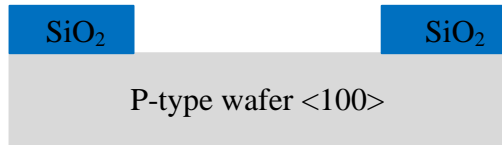


Figure 10: Oxide layer is patterned on the wafer.

4. **Wafer pre-clean:** Before starting the other process, the substrates are pre-cleaned with HF.
5. **High-k deposition:** 2nm Hafnium dioxide is deposited by atomic layer deposition.
6. **Post Deposition Annealing(PDA):** PDA is one of the fundamental technique to improve the material properties in the deposited film[20]. N post-deposition annealing is done by at 700°C for 60 sec.
7. **Metal deposition:** TiN of 5nm, 10nm and 15nm are deposited in several wafers using atomic layer deposition (ALD) [Figure 11].

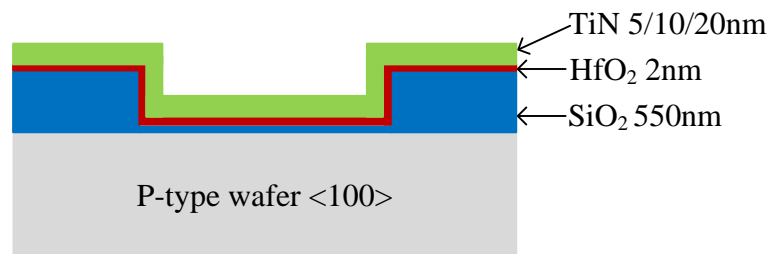


Figure 11: The structure on substrate after high-k dielectric, PDA and metal deposition.

8. **Poly-silicon deposition with P-implantation:** 100nm poly-silicon is deposited by chemical vapor deposition [Figure 12]. Then P is implanted with the implantation dose of  $2.5 \times 10^{15} / \text{cm}^2$ .
9. **Activation anneal:** A spike anneal of one sec is carried out at  $1000^\circ\text{C}$ .
10. **Gate lithography:** Photoresist is coated, baked and UV exposed through the mask. Then the wafers are developed. This lithography is done to cover the expected device part on the wafer and etch all other parts to the oxide layer.
11. **Reactive ion etching:** RIE is done to etch the poly-Silicon and metal layer.
12. **Photoresist strip:** Photoresist is stripped from the whole wafer by using acetone and oxygen plasma.

After having the first batches of fabricated devices [Figure 13], the TEM/EELS, XRD, XPS and SIMS analysis are carried out to understand why the work function is changing with the change of the TiN metal thickness.

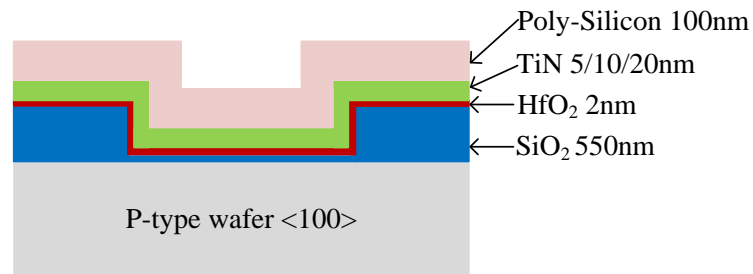


Figure 12: The structure on substrate after poly-silicon deposition.

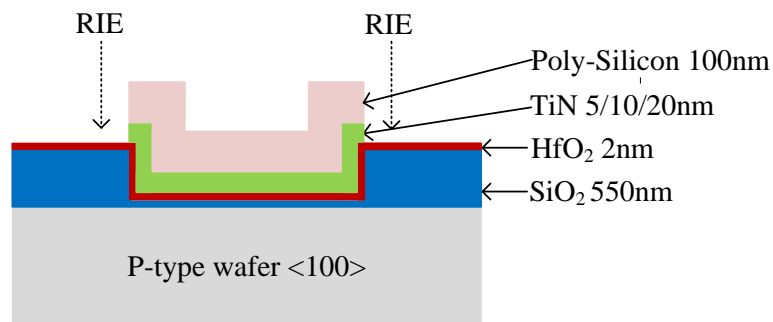


Figure 13: Final structure after RIE and photoresist strip.

### 3.3 CHARACTERIZATION

The first set of devices is characterized using the transmission electron microscope/electron energy loss spectroscopy (TEM/EELS), secondary ion mass spectroscopy (SIMS), X-ray photoelectron spectroscopy (XPS) and x-ray diffraction (XRD).

1. **Transmission electron microscope (TEM)/ Electron energy loss spectroscopy**

**(EELS):** TEM samples were prepared by using focused ion beam (Helios 400s, FEI) with lift-out method. First-beam and Ion beam assist Pt deposition is occurred in FIB to make protection layer on the surface of sample for minimizing Ga ion damage during ion beam milling. Second, Ga ion beam milling with the beam condition (30 kV, 21 nA) was used to cut the sample from the bulk. After attaching the sample to the Cu TEM grid with lift-out method, the sample was thinned down(30kV, 0.98nA). The final cleaning was done with low energy Ga ion beam (2 kV, 28 pA) to get rid of amorphied and damaged areas, which occurred during the ion beam thinning process.

EELS measurements were performed using a probe CS corrected FEI TITAN CUBED system, under high-tension voltage of 300 kV. The probe size was set to 0.9 Å in diameter to obtain sub-angstrom level resolution.

2. **Secondary ion mass spectroscopy (SIMS):** The SIMS analyses were performed

on the Physical Electronics ADEPT-1010. Cs, CsN, CsO, Cs<sub>2</sub>F, Cs<sup>28</sup>Si, Cs<sub>2</sub><sup>35</sup>Cl, Cs<sup>48</sup>Ti, and <sup>178</sup>Hf were monitored as positive secondary ions under 500eV Cs<sup>+</sup> bombardment at 60°. Secondary ions were collected from the center 20% of a 400 mm x 400 mm rastered area. 1-cm<sup>2</sup> pieces were taken from the center of each

wafer. Stylus profilometry was used to determine the depth of the craters and calibrate the depth scale. However, the presence of multiple layers of different materials different sputter rates means the depth scale is likely off.

3. **X-ray diffraction (XRD):** A Rigaku Ultima III x-ray diffraction system was used to detect crystallization as a function of thermal annealing process.
4. **X-ray photoelectron spectroscopy (XPS):** A PHI Model 5700 X-Ray Photoelectron Spectrometer was used for XPS analysis. The operation of the analyzer is done using constant analyzer energy mode with the scanning steps of 0.2 eV and 0.5 eV and with the pass energies of 25 eV and 50 eV for the narrow and wide scans respectively. The un-monochromated MgK $\alpha$  (1253.6 eV) is used as the source of the radiation (incident); it was running respectively at 15 kV and 20 mA. A standard ionization gun is used for Ar<sup>+</sup> ion beam etching where the incident energy was 1500 eV and 6-10 mA was the sample current. For physical characterization, poly silicon was removed from all the processed samples.

### **3.4 FABRICATION OF SECOND BATCH OF DEVICES**

The fabrication of second batch of devices is almost the same except some additional steps. After metal deposition, the following steps are followed for the second batches of devices.

1. N-implantation is done with  $1 \times 10^{15}$  /cm<sup>2</sup> dose on several wafers.
2. Furnace annealing in O<sub>2</sub> is carried out at 400°C for 30min on several wafers.
3. Etch back: For one wafer, standard clean 1 (SC1) is used 20 minutes.

The activation anneal step is modified by the following way:

Activation anneal: On several substrates, a low thermal budget of 5 sec is carried out at 1000°C. A long anneal of 3 minutes is also carried out on some other substrates. For a substrate, no annealing is carried out.

### **3.5 CAPACITANCE-VOLTAGE MEASUREMENT AND ANALYSIS**

After having the second batches of fabricated devices, in order to verify the work function tuning, capacitances versus voltage (CV) characteristics are measured using Keithley Semiconductor Characterization System (SCS) 4200 with a CV module setup. For three frequencies such as 10 KHz, 100 KHz and 1 MHz, a large number of devices of different sizes are measured from each wafer so that we can ensure maximum statistical accuracy. These data are analyzed using Hauser CVC-software [21] and the equivalent oxide thickness (EOT) and flat-band voltage ( $V_{FB}$ ) were extracted for each device. The variation of  $V_{FB}$  from wafer to wafer equals the variation of work function.

# CHAPTER IV: WORK FUNCTION TUNING

## 4.1 INTRODUCTION

Recent advancement of high-k/metal gate Complementary Metal Oxide Semiconductor (CMOS) technology shows many evidences that effective work function ( $W_f$ ) of Titanium Nitride (TiN) metal gate increases with its thickness [17-19, 22, 23]. This can pave the way for multiple threshold voltage ( $V_t$ ) Systems-on-Chip (SoC). Many hypotheses are made over the years which include but not limited to: trap charge and metal gate nucleation [18], nitrogen concentration [17], microstructure agglomeration and global stress [19], metal oxide formation [22], and interfacial oxide thickness [23]. However, clear contradictions exist in these assumptions. Also, nearly all the papers skipped a comprehensive approach to explain this complex paradigm. Concentration of oxygen and nitrogen is a prominent one where some studies showed its richness leads to higher work function whereas findings are available to support the reverse fact [24-26]. Therefore, we first comprehensively examined the mechanism how the physical properties of TiN changes with its various thickness and impacts its work function. Then we replicated those physical properties by process engineering to get the work function tuning without changing the TiN thickness.

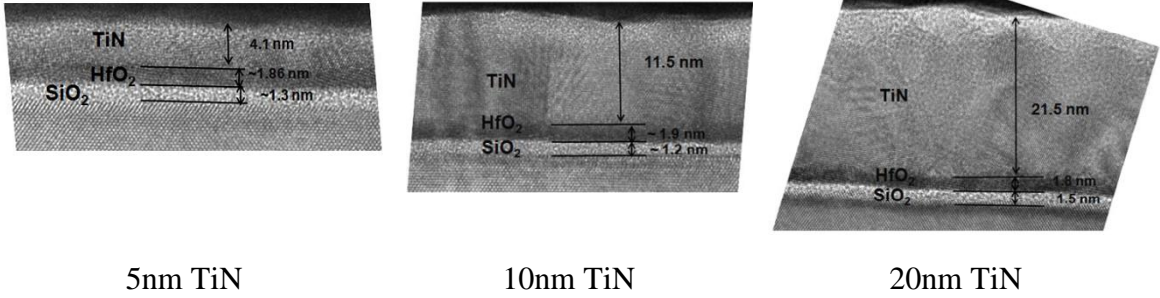
## 4.2 STUDY OF MECHANISM

### 4.2.1 TEM/EELS ANALYSIS

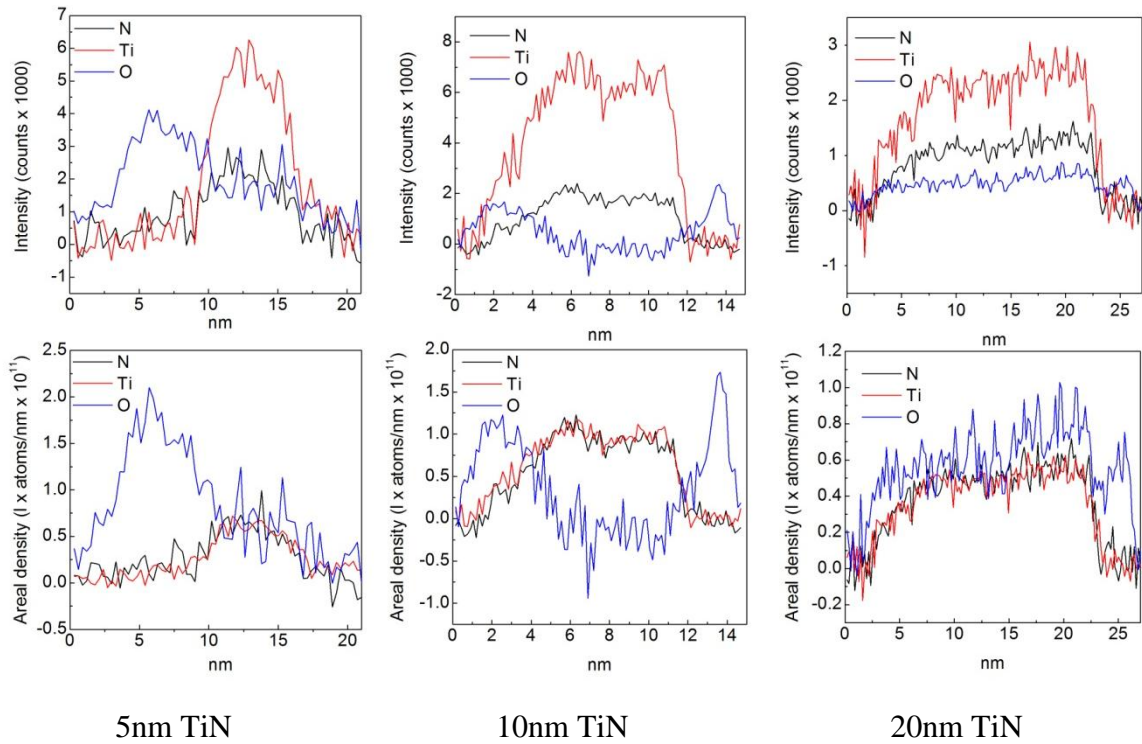
At first, we studied our samples with TEM and it showed uniform deposition of gate stacks (high-k/metal) and the thicknesses of each intended split were nearly right on target [Figure 14(a)]. Although in the past discontinuous TiN island formation and thus direct mix-up of poly-silicon and high-k for thin film (<5nm) was speculated to be the reason for lower work function [18], in the TEM analysis we did not observe the same [Figure 14(a)]. We observed continuous TiN films without any penetration of poly-silicon to the underlying dielectric. Therefore, possible interaction between high-k/poly-Si cannot be a reason for work function variation. It was also speculated that there is the incursion of the electron wave function tail of n+ poly-silicon through extremely thin TiN layer. Probable consequences from extrinsic reasons such as interfacial reaction or stoichiometry change with film thickness due to diffusion was not closed out [27]. Another possible reason for the work function change is the increased value of interfacial fixed charge ( $Q_f$ ), an effect that can shift  $V_{FB}$  and change the effective work function. However, the value of  $Q_f$  increased by only a factor of two over the entire TiN thickness range, suggesting that fixed charge alone cannot explain the entire increase in TiN work function ( $1 \times 10^{10} \text{ cm}^{-2}$  vs.  $2 \times 10^{10} \text{ cm}^{-2}$ )[17].

In our EELS analysis, we observed that the density of nitrogen is increasing in TiN/HfO<sub>2</sub> interface while increasing TiN thickness from 5 to 10nm. [Figure 14(b)]. Though the increment in 20nm TiN is not clear, we assume that nitrogen increases with TiN thickness based on the elemental analysis of XPS results [Figure 15] and the





(a)



(b)

Figure 14: (a) TEM and (b) EELS analysis of TiN (5, 10 and 20 nm)/SiO<sub>2</sub> (Interface oxide)/HfO<sub>2</sub>. The TEM image shows uniform and continuous deposition of high-k/metal gate stacks.

previous reports [17, 24-26] about the work function tuning and nitrogen concentration. It is possible that oxygen replacement by nitrogen in the interface can increase the work function. This effect is due to a balance of two opposing dipoles associated with the Ti and Hf atoms at the interface (the sequence O–Hf–O–Ti–N is being replaced by O–Hf–

N–Ti–N). Due to the larger polarizability of the Hf atom compared with that of Ti, the dipole associated with the Hf atom is more pronounced creating a net increase of the work function [28]. Previously three reports claimed nitrogen concentration may tune the work function characteristics [17, 24-26]. Our XPS analysis [Figure 15] also resonate the same. Increased nitrogen will reduce influence of low vacuum work function material Ti and thus results in TiN higher work function[18].

Previously, Wakabayashi [24] and Westlinder [25] reported that by using ion implantation or higher nitrogen gas flow during sputtering, respectively, the work function increases in n-MOSFET. However, Wakabayashi's claim was convoluted with channel doping. Also, it is not clear what perturbation was caused by ion implantation process. On the other hand, Liu [26] contradicted this observation by using a sputtering system (same as Westlinder [25] ) where with higher nitrogen gas flow the NMOS work function in non-planar FinFET device was reduced. Thus, based on our physical analysis and careful review of contradictory reports, we believe that the nitrogen can play some role to alter the work function depends on nitrogen inclusion process as well as the device architecture.

Previously M.M. Hussain *et al.* reported that typically ALD processed TiN contains some oxygen and the thicker the TiN, the probability of oxygen intrusion is higher too and thus resulting in thicker interfacial oxide [29]. Current TEM images also show thicker interfacial oxide associate with thicker TiN [Figure 14(a)]. Our EELS analysis also shows oxygen is fairly distributed throughout the high-k/TiN gate stack [Figure 14(b)]. However, the relative composition of oxygen reduces with higher thickness of TiN.

### 4.2.2 XPS ANALYSIS

Besides stoichiometric analysis, in our XPS analysis for Ti 2*p* and N 1*s*, we did not observe any shifting in the peak position [Figure 15]. This suggests that there was not any significant bonding trend shift for N 1*s*. Therefore, chemical analysis does not indicate any significant correlation related to surface chemistry or bonding. However, the elemental analysis shows that the amount of nitrogen is increasing with the increase of TiN thickness.

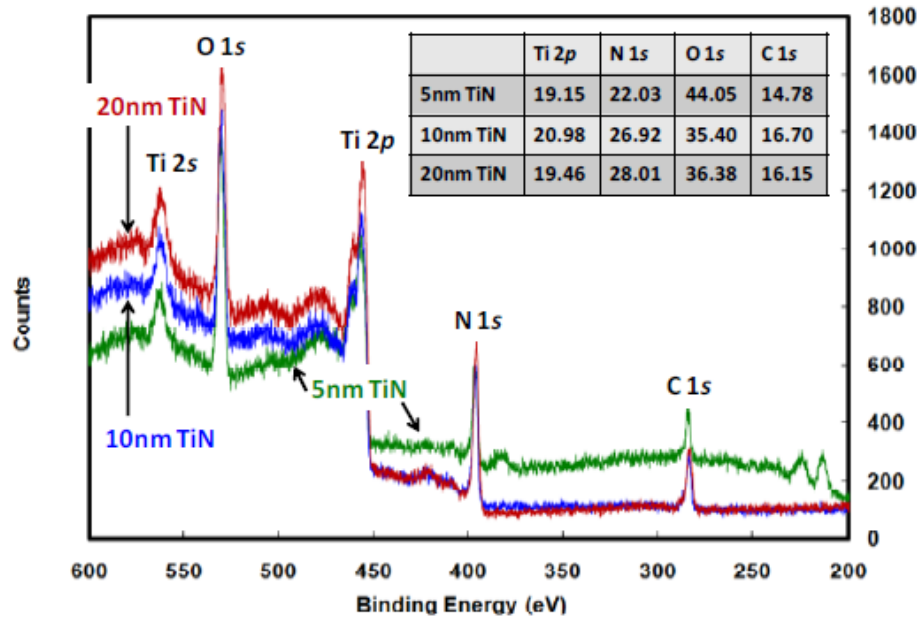


Figure 15: XPS analysis of TiN experimental samples. Inset shows the elemental composition. We did not observe any significant peak shifting for Ti 2*p* and N 1*s*. Elemental analysis shows increased amount of nitrogen in thicker TiN.

### 4.2.3 SIMS ANALYSIS

Our SIMS study [Figure 16] shows a correlation between TiON<sub>x</sub> formation in metal/dielectric interface and TiN thickness. When the metal and the dielectric surfaces

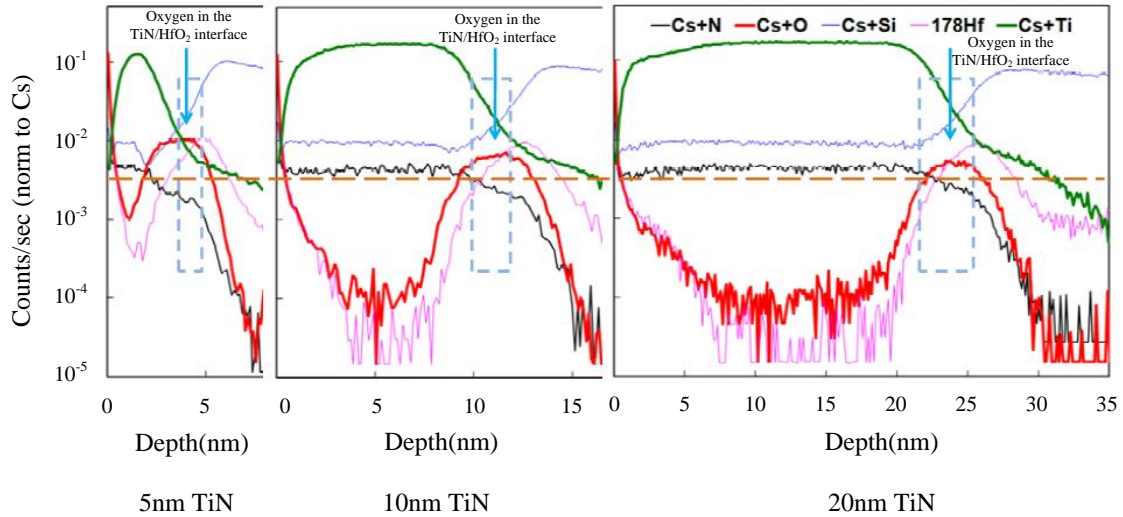


Figure 16: SIMS analysis of TiN experimental samples shows a direct correlation between  $TiON_x$  formation in metal/dielectric interface and TiN thickness.

comes into contact, exchanged charge between the two surface states results in the formation of an interfacial dipole. The changes in work function suggest that an increase in the oxygen excess regions at the interface can also change the amount of charges exchanged at the interface [30].

#### 4.2.4 STRESS ANALYSIS

In the past, Bae [19] inconclusively indicated some interference by global stress in TiN. C.Y. Kang *et al.* observed that the stress of TiN increases with its thickness [31]. For 5nm TiN the tensile stress is 1.12 GPa and it goes up to 1.7GPa for 20nm TiN. At the same time, the same set of samples show increased work function, with increased thickness of TiN. This is indicative that stress may play some fringe role to tune the work function like previously reported for some other material systems [32]. We took a set of 10nm

ALD TiN/2nm HfO<sub>2</sub> MOSCAP devices and when uniaxial stress was applied, no significant change (work function change was less than 5%) was observed.

#### 4.2.5 XRD ANALYSIS

During our XRD analysis [Figure 17], we observed no significant changes in crystal phase or orientation. Also, in the past amorphous TiN has shown work function rise with its thickness increment without any preferred crystal orientation [17]. There was no peak shifting in the rocking curves. Then general observation on the grain size (volume-weighted size) using Scherrer method (which ignores the role of the microstrain and gives lower limit values of the titanium nitride grain size) that thicker films seem to have larger grains [33, 34]. It might be explained by the fact that work function decreases with small grain size due to the increasing fractional defect area near the crystallite edges [35].

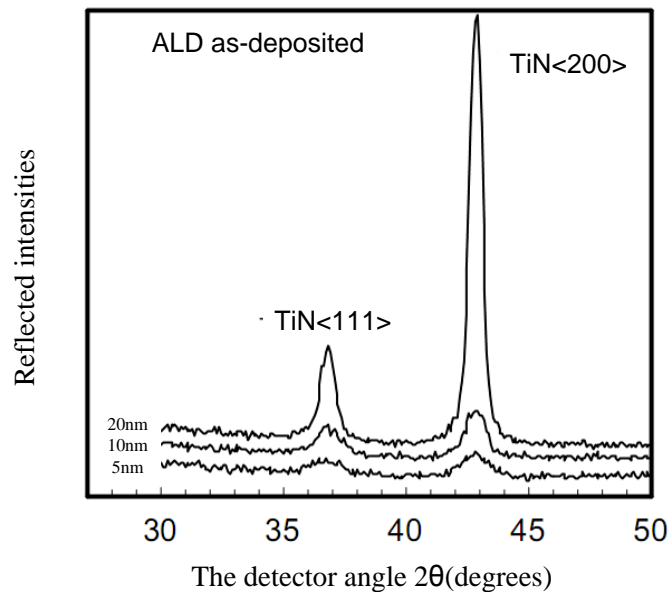


Figure 17: XRD analysis of TiN experimental samples shows no significant changes in crystal phase or orientation. The general observation on the grain size (volume-weighted size) using Scherrer method, (which ignores the role of the microstrain and gives lower limit values of the TiN grain size) that thicker films seem to have larger grains.

Also, the film with small grain size indicates that it is of poor crystalline quality [36]. Furthermore, the amorphous layer has lesser work function than its crystalline form [37, 38]. Thus the poor crystalline quality with small grain size may reduce the work function.

#### **4.2.6 COMMENTS ON MECHANISM**

We attribute that with increased thickness of TiN, formation of  $\text{TiO}_x$  or  $\text{TiON}_x$ , replacement of oxygen by nitrogen in the metal/dielectric interface, reduction of Ti/N concentration and grain size increment also increase and thus may affect the work function. Also, apparently a weak correlation exists between stress and work function of TiN metal gate. Advancement in process technology based on our study, which is discussed in the next section, can create a larger window of work function tunability in single thickness based TiN to reproduce its multi-thickness induced work function. This is a simple and practical solution for multi-threshold voltage devices in Systems-on-Chip.

### **4.3 WORK FUNCTION ENGINEERING**

#### **4.3.1 BASICS**

The work function of TiN metal gate can be modulated by changing the thickness of the layer[17]. Study of the mechanism of this work function modulation shows the increasing the thickness of TiN results in the formation of  $\text{TiO}_x/\text{TiON}_x$  in the TiN/ $\text{HfO}_2$  interface layer, increase of N/Ti ratio, replacement of oxygen by nitrogen in the TiN/high-k interface and hence increase of the work function. But without changing the thickness of

TiN layers, some additional process engineering also can recreate such changes in physical properties. Oxygen annealing can incorporate oxygen and form  $\text{TiO}_x$  or  $\text{TiON}_x$  in the TiN/high-k interface layer and boost the work function up. Additional Nitrogen implantation/annealing may replace some oxygen by nitrogen in the interface layer. Activation anneal associated thermal budget also may have some effect on the oxygen concentration in the TiN/High-k interface; some oxygen can go the high-k/Si layer and thus decreasing the work-function. This section will describe these processes engineering basic first and then present our results.

Oxygen has the property to boost the work function of the metals such as titanium nitride, molybdenum and tantalum carbide [39-43]. During high temperature process, it is also able to diffuse into the gate stack and react with the substrate which leads to the increase in effective oxide thickness(EOT) [39, 44]. However, oxygen can be incorporated in TiN and  $\text{HfO}_2$  film by oxygen annealing; this oxygen incorporation decreases the oxygen vacancies and increases the work-function. Oxygen annealing may also reverse the shift of the Fermi level pinning due to the formation of Hf-metal bonds and tune the work function [45, 46].

Nitrogen ion implantation may increase the nitrogen/titanium ratio in the film as discussed in previous chapter. Nitrogen annealing also increases the nitrogen concentration. Nitrogen/titanium ratio can also be controlled by controlling the nitrogen gas flow during sputtering.

Increasing activation anneal time decreases the work function as we observe in our experimental results. Increasing the anneal time may enable more oxygen to move from TiN/ $\text{HfO}_2$  interface to  $\text{HfO}_2/\text{SiO}_x$  interface as the oxygen atoms are more likely to bond

with silicon than TiN; when they get enough activation energy, they move towards their more appropriate position- the silicon interstitial sites. So increasing the thermal budget by increasing the activation anneal time decreases the work function.

#### **4.3.2 DESCRIPTION OF PREPARED SAMPLES**

In this work, a set of nine MOSCAP wafers are prepared to tune work function by process engineering. The fabrication steps are discussed in the chapter III and the key processing steps which are different from wafer to wafer are shown in the Table 1. The first five wafers consist of MOS capacitors with 10 nm ALD TiN. After TiN deposition, for the first sample, nitrogen is implanted but no oxygen anneal is carried out. After 100nm amorphous silicon deposition and P-deposition, it was annealed for 5 sec at 1000 °C. For the second sample, no nitrogen implantation is carried out, but oxygen annealing is done and annealing for 5 sec at 1000 °C is also done. For the third sample, both the nitrogen implantation and oxygen annealing as well as low thermal budget is carried out. For the fourth sample, only long anneal is done with no nitrogen implantation and oxygen annealing. For the fifth sample, both nitrogen implantation and oxygen anneal are done, but no activation anneal is carried out.

Four more samples are prepared among which only one is of 5 nm TiN and three samples are of 20 nm. For 5 nm sample, no ion implantation and oxygen annealing are carried out, but a short activation anneal of 5 sec at 1000 °C is done. For first 20 nm sample, both nitrogen ion implantation and oxygen anneal as well as low thermal budget are carried out. For the second sample, none of nitrogen ion implantation and oxygen annealing is done but long anneal is carried out. For the last sample with 20 nm TiN film,



Table 1: Summary of key processing steps in fabrication.

Wafer Sample	ALD TiN (nm)	N Implantation	O <sub>2</sub> Anneal	Etch	Anneal at 1000°C time (sec)
1	10	Done (☑)	Not done (☒)	☒	5
2	10	☒	☑	☒	5
3	10	☑	☑	☒	5
4	10	☒	☒	☒	180
5	10	☑	☑	☒	☒
6	5	☒	☒	☒	180
7	20	☑	☑	☒	5
8	20	☒	☒	☒	180
9	20	☒	☒	Etch-back to 5nm	5

none of nitrogen ion implantation and oxygen annealing is done, but etch-back to 5 nm is carried out with standard clean 1 (SC-1) for 20 minutes; short activation anneal is also done for 5 sec.

### 4.3.3 CAPACITANCE-VOLTAGE (CV) CHARACTERISTICS

In order to compare the work function among different samples, we need to determine the flat band voltage of the MOSCAP by measuring the capacitance-voltage characteristics. Also, from the maximum capacitance values, we can determine the effective oxide thickness (EOT).

Figure 18 shows the capacitance versus voltage (CV) characteristics for the devices from samples with 10nm metal thickness. The measurements are done at 1MHz frequency. The shown CV data are for  $2 \times 10^{-5} \text{ cm}^2$  device area.

If we compare the CV characteristic curves of sample 1 and 3, we can observe that the flat band point is at higher voltage in sample 3 compared to sample 1 due to additional oxygen annealing. Due to the oxygen annealing, the oxygen vacancies in Hf-based dielectric near the metal-dielectric interface are filled and  $\text{TiO}_x/\text{TiON}_x$  is formed; hence the work function increases. So the work function of sample 3 will be higher than that of sample 1. We also can observe the effect of lowering the thermal budget; the flat band voltage of the devices in sample 5 becomes higher than that of sample 3 because of lowering the thermal budget. Sample 4 exhibits the lowest flat band voltage as no

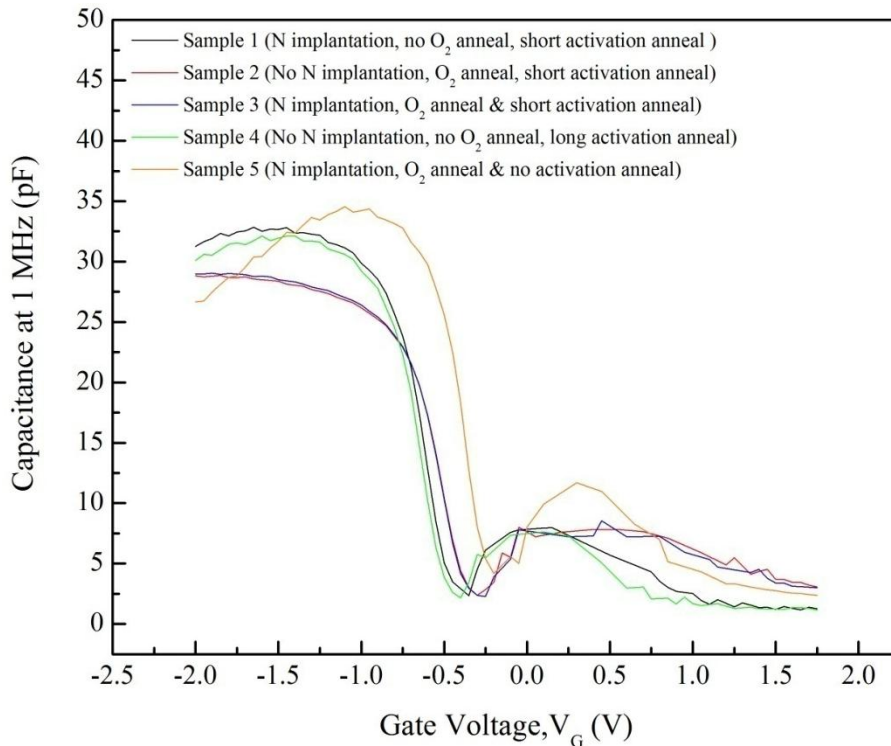


Figure 18: Capacitance versus gate voltage at 1MHz for the device with same TiN metal thickness of 10nm and area  $2 \times 10^{-5} \text{ cm}^2$ .

oxygen anneal and no nitrogen implantation are carried out while a long activation anneal is done. However, there is an anomaly in the CV characteristic curve that at some points in the depletion region, capacitance gets some higher value; this might be due to the trapped charges which become active or come out when a positive voltage is applied and make the part of the channel conductive which increases the capacitances of MOSCAP. When a higher positive voltage is applied, we assume that the trap charges are swept away and the semiconductor becomes clearly depleted.

Figure 19 shows capacitance versus voltage (CV) characteristics for the rest samples with different TiN thicknesses. Here, the area of all devices is  $2 \times 10^{-5} \text{ cm}^2$  and the measurements are done at 1MHz frequency. Here, we can see that the flat band voltage increases with the increase of TiN thickness and decreases with longer activation anneal.

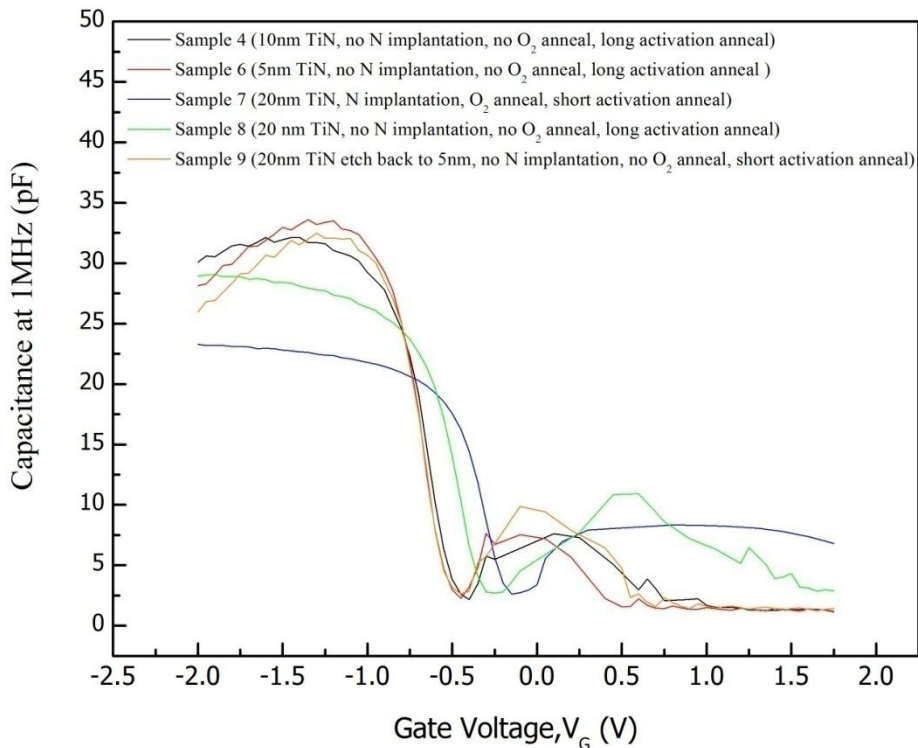


Figure 19: Capacitance versus gate voltage at 1MHz for the device with same area  $2 \times 10^{-5} \text{ cm}^2$  but different TiN thicknesses.

From each CV characteristic, it is possible to calculate the flat band voltage of a MOSCAP device. By comparing the flat band voltage of two different devices, the work function difference between these two devices can be calculated. As we are changing the flat band point of MOSCAP devices by some mechanisms, we are also modulating the work function of the metal in MOSCAP.

#### 4.3.4 FLATBAND VOLTAGE AND WORK FUNCTION TUNING

Figure 20 shows the work-function modulation for 10nm TiN film at 1 MHz frequency. If we compare sample 1 and 3 where both nitrogen ion implantation and low thermal budget are carried out in both samples, but no oxygen anneal is carried out in sample 1

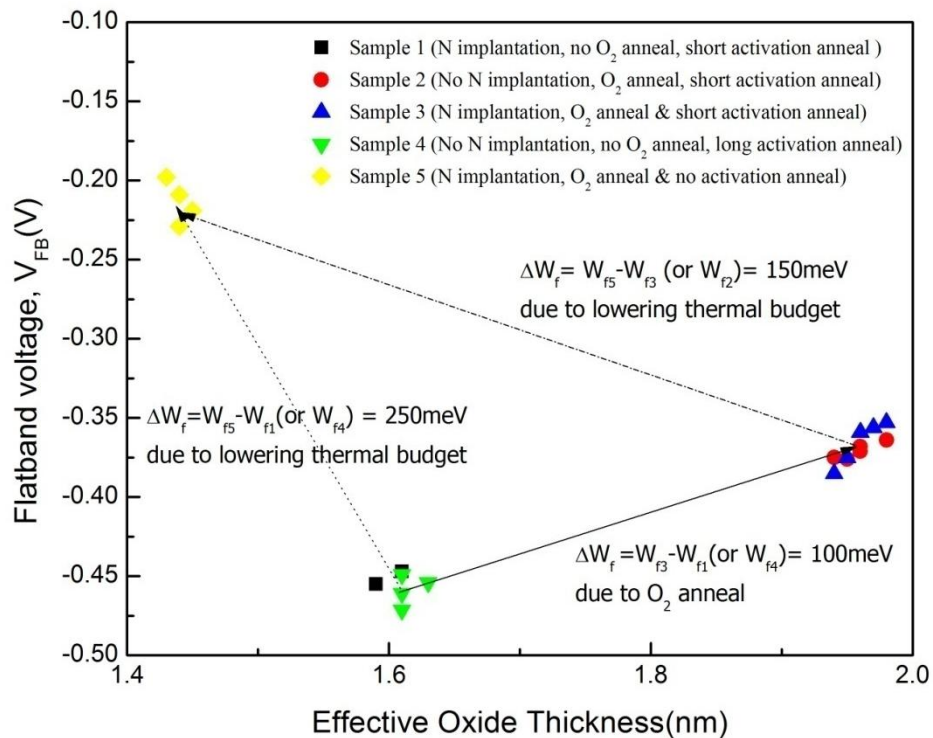


Figure 20: Flatband voltage ( $V_{FB}$ ) versus effective oxide thickness (EOT) at 1 MHz frequency for a single thickness (10 nm) of TiN metal gate.

though a low thermal budget is carried out in sample 3. Here, we get a work function increment of 100meV in sample 3 compared to sample 1. So, due to oxygen annealing, the work function is modulated by 100meV with the increase of effective oxide thickness. So, the work function can be increased in single thickness of TiN by doing oxygen annealing.

If we compare sample 3 and 5, both the nitrogen ion implantation and oxygen anneal are done in both samples and sample 3 is annealed for short time, but sample 5 is not annealed at all. Here, the increase of the work function in sample 5 is 150 meV and the effective oxide thickness is decreased. So, using less time in activation annealing, we can increase the work function.

Now if we compare sample 1 and 5, the nitrogen ion implantation is done in both samples, but in sample 5, oxygen anneal is done with no activation anneal where in sample 1, no oxygen anneal is done but a short activation anneal is carried out. Here, the work function is increased by 250mV in sample 5 compared to sample 1. Here the oxygen anneal and less activation anneal time works to increase the work function.

In this experiment, we did not find any work-function modulation due to nitrogen ion implantation alone as expected in our analysis in last chapter. Perhaps higher nitrogen gas follow during sputtering, nitrogen annealing or nitrogen ion implantation with higher dose will be able to increase N/Ti concentration ratio and increase the work function as expected.

Figure 21 shows the flat band voltage versus effective oxide thickness for the rest samples with different thicknesses and processes. The plot shows the change in work function with the variation of TiN thicknesses as depicted by sample 6 (5 nm), sample 4

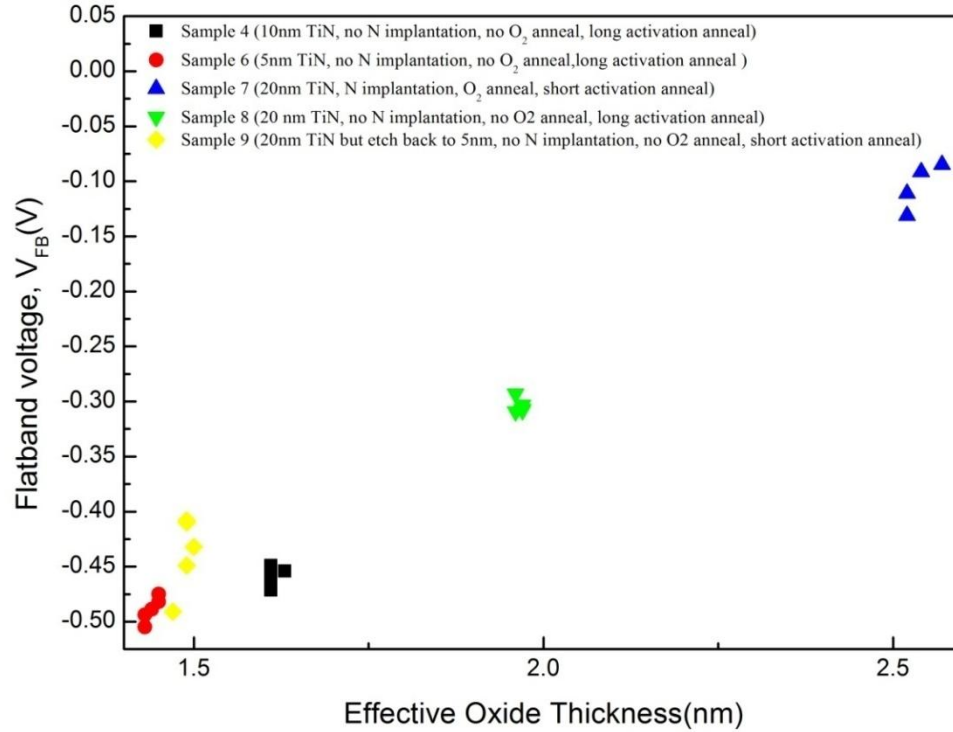


Figure 21: Flatband voltage ( $V_{FB}$ ) versus effective oxide thickness (EOT) at 1 MHz frequency for different thicknesses and processes.

(10 nm) and sample 8 (20nm).

If we compare the results of 20 nm TiN samples, we can observe the flat band increase of 200 meV in sample 7 compared to sample 8 due to the effect of nitrogen ion implantation, oxygen anneal and short activation anneal instead of long anneal.

Another important point is that the etch-back of 20nm TiN layer to 5nm in sample 9 (with 20nm TiN and low thermal budget) decrease the work function a lot compared to sample 8 (with 20 nm TiN and long anneal). Even though short activation anneal is generally found to increase the work function compared to the long anneal, etch-back in sample 9 decrease the work function a lot- even near the work function of sample 5 (with 5nm TiN) where long anneal is done. So, the etch-back can decrease the work-function to a value near the normal work function of its final thickness.

Figure 22 shows the same result as in Figure 20, but with different frequency (100 KHz) where we get the same type of results we get for 1MHz frequency. These results verify the work function tuning irrespective of frequencies.

The other samples with different TiN thicknesses (non-10nm single thickness) are also investigated in 100 KHz frequency. The results shown in Figure 23 for 100 KHz show the same type of work function tuning shown in Figure 21 for 1 MHz. This verifies the work function tuning irrespective of frequencies.

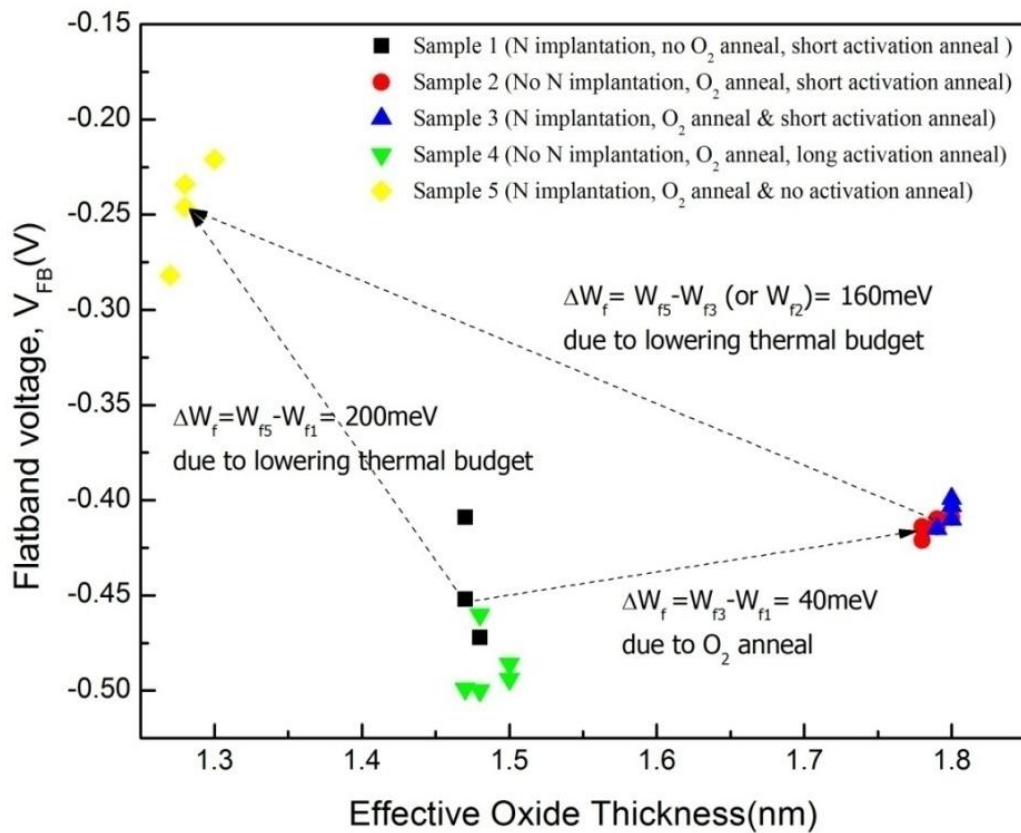


Figure 22: Flatband voltage ( $V_{FB}$ ) versus effective oxide thickness (EOT) at 100 KHz frequency for a single thickness (10 nm) of TiN metal gate.

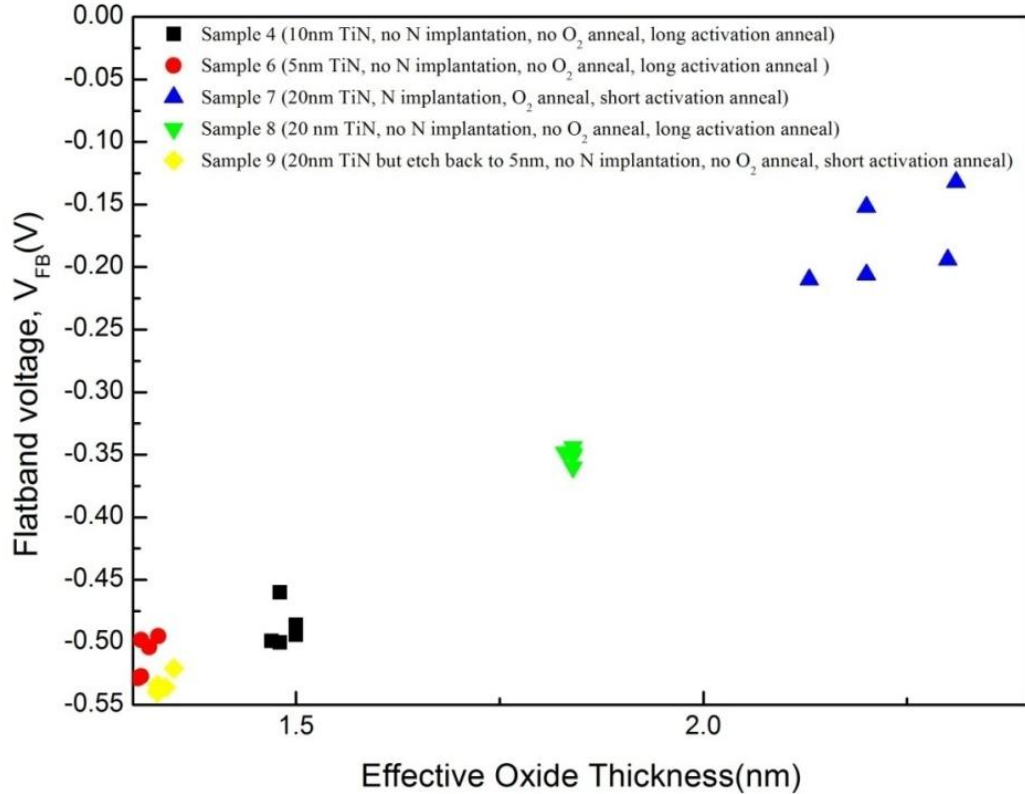


Figure 23: Flatband voltage ( $V_{FB}$ ) versus effective oxide thickness (EOT) at 100 KHz frequency for different thicknesses and processes.

#### 4.3.5 RELATION WITH GATE LEAKAGE CURRENT

The gate leakage current density ( $J_g$ ) also supports the concept of work function tuning. Generally higher metal work function reduces the gate leakage [47] and it is resonated in the most of our samples as shown in Figure 24 and Figure 25. Oxygen annealing always increases the resistivity of the gate-to-channel path; hence reduces the gate leakage. Activation anneal for long time is assumed to remove the oxygen from the HfO<sub>2</sub>/TiN interface and increases the leakage. Here, in most cases, oxygen annealing and shorter activation anneal or lower thermal budget increases the work function.



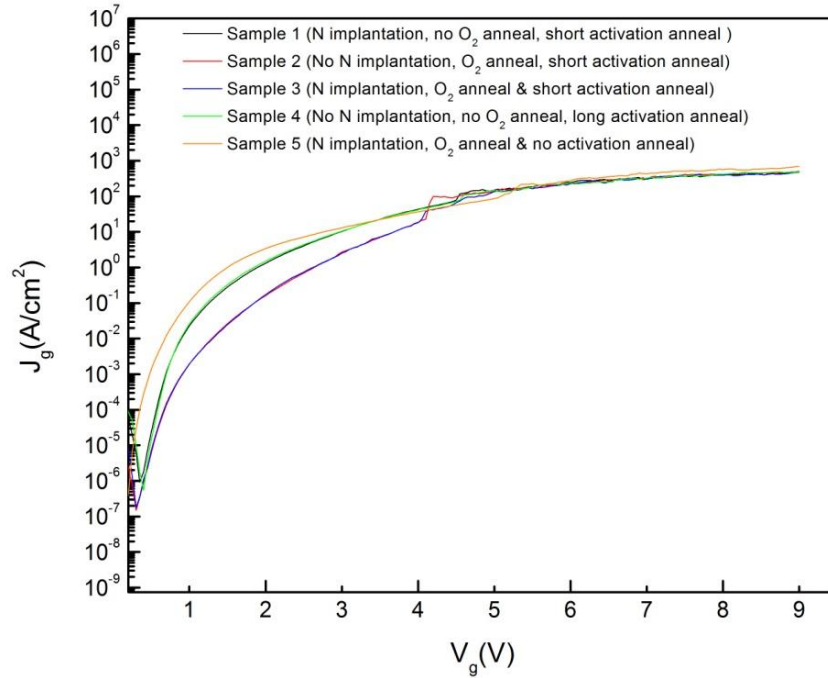


Figure 24: Gate leakage current density( $J_g$ ) versus the gate voltage( $V_g$ ) for the samples with 20nm TiN.

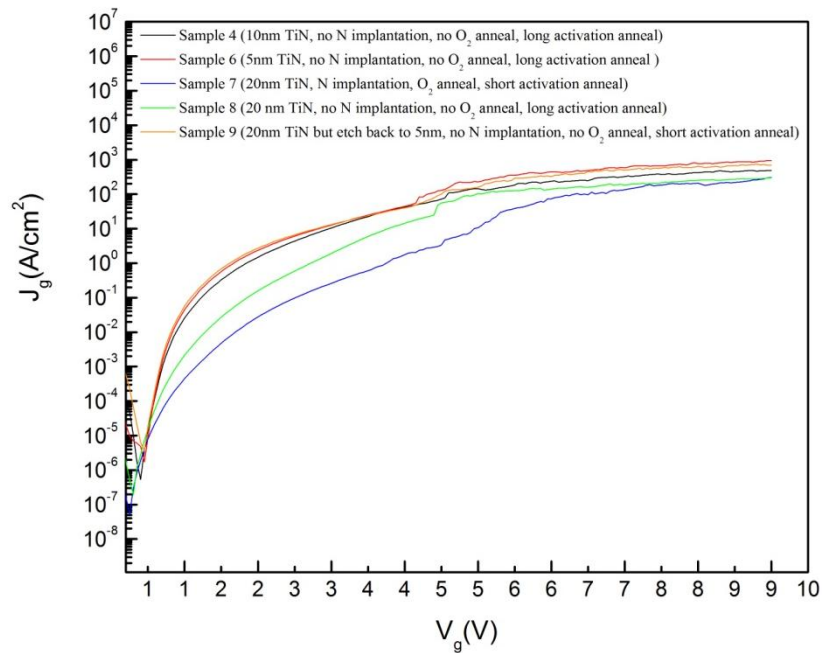


Figure 25: Gate leakage current density ( $J_g$ ) versus the gate voltage( $V_g$ ) for the samples with different TiN thicknesses.

#### **4.3.6 SUMMARY**

In summary, this section describes how the work function modulation can be engineered without changing the TiN metal thickness. The results obtained to verify the expectation for work function modulation are presented and explained. O<sub>2</sub> annealing and lowering the thermal budget are found as the effective ways to tune the work functions. N implantation is also expected to have some effect but our results did not show that due to some probable limitation which has been explained. However, we demonstrated the work function tuning without changing the thickness which is a simple solution for having multiple threshold voltages devices on a same substrate.

# CHAPTER V: CONCLUSION

## 5.1 GENERAL CONCLUSION

Since 2007, semiconductor industry is shifted to high-k/metal gate stack based field effect transistor instead of classical  $\text{SiO}_2$ /poly-Si gate. Titanium nitride is one of the materials used as a metal gate electrode. It is a mid-gap work function material in which the work-function can be tuned with the TiN film thickness which is promising solution for multi-threshold voltage devices. But due to the integration complexity arises from the metal gates with different thicknesses, an alternative way to tune the work function of metal gate electrode with simple integration is preferable. So for that purpose, we first do the physical investigation of the prepared samples and understand why the work function changes with thickness with the thickness. The physical investigation reveals that with the increased thickness of TiN metal gate, formation of  $\text{TiO}_x$  or  $\text{TiON}_x$  and replacement of oxygen by nitrogen in the metal/dielectric interface increases. Oxygen annealing, nitrogen implantation and thermal budget control can replicate same physical phenomena without changing the TiN thickness. Oxygen annealing incorporates the oxygen in TiN and  $\text{HfO}_2$  film, decreases the oxygen vacancies and increases the work function. Nitrogen ion implantation may increase the nitrogen/titanium ratio in the film and increase the work function. The activation anneal also has effect on work function; decreasing the anneal time at same temperature can increase the work function. Based on this developed understanding, we replicate the same physical changes happened with the thickness change by the process engineering in single thickness devices. The collected data shows

that the oxygen annealing and activation anneal controlling tune the work function without any need of varying the thickness of the layer. So the engineering of TiN work function has been demonstrated in this thesis research. In brief, in this thesis, we demonstrated two things: physical investigation of MOSCAPs with different TiN thicknesses to understand the mechanism of work function tuning and demonstration of work function tuning by engineering same physical phenomena without changing the TiN thickness.

So, this thesis explains the mechanism of work function modulation as well as offers some process engineering to tune the work function without changing the thickness of metal gate electrode. Among the offered processing engineering, to best of our knowledge, controlling the activation anneal time is a completely new way discovered through this thesis research. So, this research ultimately paves a way for integrating devices of multiple work function i.e. multiple threshold voltage CMOS process which is a solution for optimizing power and speed in any process node.

## **5.2 LIMITATION**

We expected that N implantation will be able to tune the work function based on our understanding we have had through the physical analysis. However, it is not reflected in our experimental results. It might be because of lower dose in implantation. Perhaps higher nitrogen gas follow during sputtering, nitrogen annealing or nitrogen ion implantation with higher dose could be able to increase N/Ti concentration ratio and increase the work function as expected. Further investigation can provide accurate

information regarding the effect of nitrogen annealing, implantation or nitrogen gas follow.

### **5.3 FUTURE DIRECTIONS**

There are some significant scopes to contribute in the research topic. Some of them are as follows:

1. Investigation on the effect of N implantation on the effective work function of TiN metal gate. There is significant contradiction between the different research groups about effect of N implantation.
2. Making an empirical relationship between the work function and different process parameters. This relationship will be a valuable asset to any research group (academic or industrial) to tune the work function of the device to get a particular threshold voltage easily.
3. Investigation on the work function tunability of other metals like molybdenum and tantalum carbide.
4. Extensive physical analysis to investigate how the thermal budget tunes the work function of the metal.
5. Making a complete multi-threshold system-on-chip by engineering the work function.
6. More investigation on the work function tuning with activation anneal time which is a new phenomena found through this thesis research.

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