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On-Chip Patch Antenna on InP Substrate for Short-Range Wireless Communication at 140 GHz

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Abstract—**This paper presents the design of an on-chip patch antenna on indium phosphide (InP) substrate for short-range wireless communication at 140 GHz. The antenna shows a simulated gain of 5.3 dBi with 23% bandwidth at 140 GHz and it can be used for either direct chip-to-chip communication or chip-level integration and packaging. In the transmission frequency band from 130 GHz to 150 GHz the estimated in-band gain variation is 0.5 dBi which guarantees gain uniformity. The antenna with optimized dimension is implemented for a transition between elevated coplanar waveguide (ECPW) and rectangular waveguide. The chip-to-waveguide transition in back-to-back configuration exhibits a simulated return loss of 10 dB and insertion loss of 3 dB from 128 GHz to 153 GHz. For higher directivity, a horn antenna is used together with the chip-to-waveguide transition forming an extended packaging structure that is suitable for the transceiver (Tx and Rx) chips. The simulated gain of the extended packaging structure is 11.9 dBi with 21.4% bandwidth at 140 GHz and the in-band gain variation is 2 dBi.**

I. INTRODUCTION

With the ever increasing demand worldwide for wireless data transmission and multimedia services, the future wireless communication systems will require higher data rate in order to provide wider bandwidth for signal transmission. With higher carrier frequency, wider bandwidth can be achieved which makes THz an ideal candidate for the future wireless communication systems. However, the THz wireless communication faces difficulties, such as low-cost compact transceiver and system packaging methodology. According to [1], 10 Gbit/s data rate can be realized by an outdoor wireless communication link at 120 GHz over a distance of 1 km. Besides, a fully integrated amplitude-shift keying (ASK) receiver MMIC at 300 GHz is reported in [2].

Fig. 1 shows the potential system diagram for fully integrated ASK transceiver MMICs based on InP double hetero-junction bipolar transistor (DHBT) technology for short-range wireless communication. The carrier frequency of the system is 140 GHz with an expected data rate of 10 Gbit/s. By using ASK modulation scheme, at least 20 GHz analog bandwidth is required by the wireless communication system for signal transmission. The antenna used for transmitting and receiving data is integrated on the transceiver chips. The challenge of designing the on-chip antenna is to achieve a high gain and at the same time provide a wideband matching from 130 GHz to 150 GHz. By using on-chip antennas, the chip-level assembly can be avoided which simplifies the integration and packaging
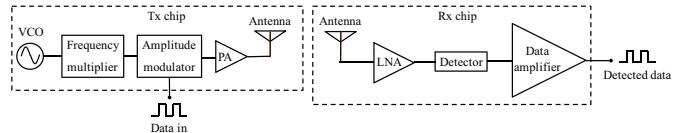

Fig. 1. System diagram for fully integrated ASK transceiver MMICs based on InP DHBT technology for short-range wireless communication.

of the transceiver chips. As a result, it provides lower loss, higher reliability, and easier fabrication especially for MMICs at THz frequencies.

By aligning the transceiver chips towards each other, the direct chip-to-chip communication can be realized and the assembly is not needed. When the transceiver chips are packaged, the on-chip antenna can be implemented for a chip-to-waveguide transition which makes it versatile and suitable for connecting to other components and systems at THz frequencies. Since the transceiver chips are based on InP DHBT technology, the on-chip antenna have to be designed using the same substrate. Fig. 2 shows the substrate structure and the 50 Ω ECPW. The ECPW is used for designing the transceiver chips as well as feeding the on-chip antenna. The substrate consists of a 160 μm InP layer on the bottom and a 3.8 μm polyimide layer on the top. The dielectric constant (ϵ_r) and dissipation factor (tanδ) of polyimide are 2.9 and 0.005, respectively. TiAuPt is used as the conductor material which is a compound of titanium, gold, and platinum. Its conductivity is 3.3e7 S/m and the metal thickness is 1.2 μm. The signal conductor layer is located on the top of polyimide while the ground conductor layer is located inside polyimide and 1.22 μm away from the top surface.

In this work, contributed to the system design, on-chip patch antenna on InP substrate is designed and analyzed by using High Frequency Structural Simulator (HFSS). The packaging structures of the designed on-chip patch antenna and the transceiver chips are addressed. In Section II, the design of on-chip patch antenna on InP substrate is described. Besides, the simulated far-field radiation pattern and gain are shown. In Section III, the rectangular waveguide packaging and assembly structure of the optimized on-chip patch antenna in back-to-back configuration are demonstrated. In Section IV, the extended packaging structure used for the potential transceiver chips is presented. The far-field radiation pattern, gain, and assembly structure of the proposed system packaging structure are explained.
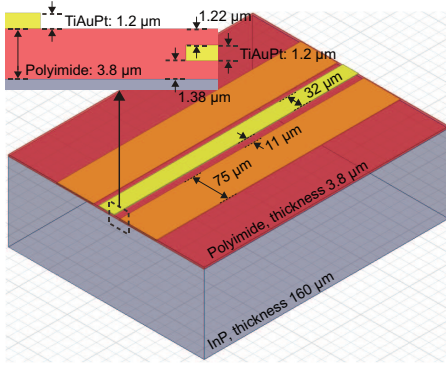
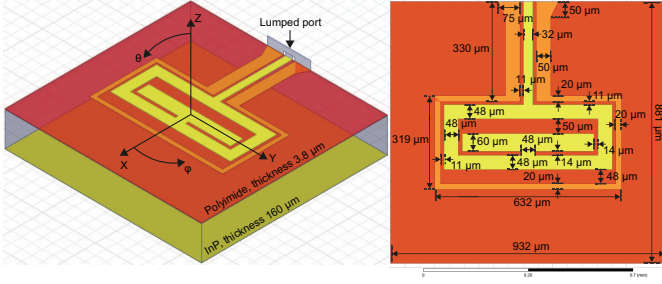Fig. 2. Substrate structure and the ECPW used for transceiver MMIC designs.

Fig. 3. Simulation structure and dimensions of the on-chip patch antenna.

Fig. 4. Far-field radiation pattern of the on-chip patch antenna at 140 GHz.

II. DESIGN OF ON-CHIP PATCH ANTENNA

In the wireless communication system shown in Fig. 1, the antenna is used for transmitting and receiving data through free-space communication link. Patch antenna is selected to be used due to its simple planar structure and reasonable occupation area which make it suitable for on-chip integration. Besides, it can be easily fed by different types of planar transmission lines. For a conventional patch antenna design, the antenna is normally fed by microstrip line and the ground plane is on the bottom of the substrate. When a patch antenna is fed by ECPW, the patch is connected to the signal trace while the ground traces are designed either to be faded out or as a part of the patch antenna. As is shown in Fig. 2, for the 50 Ω ECPW feed, the width of the signal trace is 32 μm and the width of the ground trace is 75 μm with a gap width of 11 μm.

Fig. 3 shows the simulation structure and dimensions of the on-chip patch antenna. Lumped port with vertical perfect electric conductor (PEC) bridge is used as the excitation scheme in the simulation. The PEC bridge touches the ground traces and the port is assigned to a sheet between the signal trace and the PEC bridge. The inductance of the port sheet is calibrated out from the simulation results. Another conductor layer is added on the backside of the InP substrate which works as a bottom ground plane. For simulating far-field radiation, an air box is added around the patch antenna which must be large enough reaching the far-field region of the designed on-chip patch antenna. The coordinate system for calculating far-field radiation, as is shown in Fig. 3, is located at the center of the patch geometry.

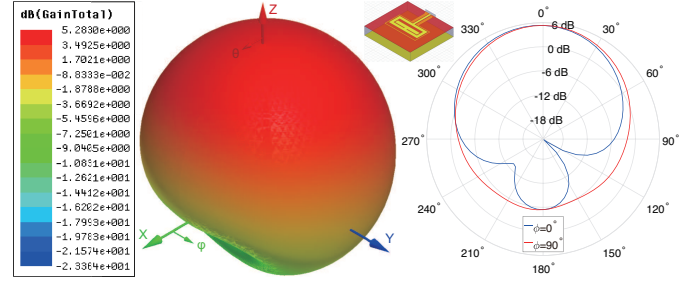The designed on-chip patch antenna is fed by ECPW and the ground traces are tapered in from 75 μm to 50 μm at the beginning. The signal trace, on the top conductor layer, is connected to a rectangular patch. The ground traces are tapered in from 50 μm to 20 μm around the patch forming a rectangular ring. In order to achieve wider bandwidth and at the same time keep the gain, the conventional rectangular patch is cut into a rectangular ring connecting to a smaller rectangular patch at the center of the patch geometry. The dimensions shown in Fig. 3 are optimized for maximum bandwidth and gain. Besides, the antenna gain in the transmission frequency band is required to be uniform in order to transmit and receive data around the same power level at different frequencies. In Fig. 4, the simulated far-field radiation pattern at 140 GHz is shown. The maximum gain at 140 GHz of the designed on-chip patch antenna is 5.3 dBi and it is achieved in the direction when θ and ϕ are 0°.

The designed on-chip patch antenna is simulated in terms of frequency and the results are shown in Fig. 5. The simulated return loss is better than 10 dB from 123.5 GHz to 156 GHz which represents 23% bandwidth at 140 GHz. As the transmission frequency band ranges from 130 GHz to 150 GHz, the designed on-chip patch antenna fulfills the requirement of 20 GHz bandwidth. In the transmission frequency band, the simulated maximum antenna gain is 5.3 dBi while the minimum value is 4.8 dBi. A good gain uniformity is achieved since there is only 0.5 dBi difference between the maximum and the minimum values. In comparison with the conventional rectangular patch antenna, the designed patch antenna with cutting ring structure exhibits wider bandwidth and similar gain. With integrated on-chip patch antenna, the direct chip–to-chip wireless communication can be realized between transceiver chips. The chips need to be aligned towards each other in the direction of maximum radiation and the communication system does not require any extra chip-level assembly. Antennas with high directivity are preferred for THz wireless communications while it is normally limited for on-chip antennas due to their planar structures. According to [3], the directivity of the on-chip antenna can be increased by adding a hemisphere silicon lens on the top of the antenna which concentrates the antenna beams in the direction of wireless communication link.

III. PACKAGING STRUCTURE OF ON-CHIP PATCH ANTENNA

The on-chip patch antenna shown in Fig. 3 is designed for direct chip-to-chip wireless communication without any packaging or measurement structures. For THz applications, the designed MMICs normally need to be packaged carefully in order to restrict parasitic modes, keep the bandwidth, provide good isolation from the environment, dissipate the heat generated by the circuits, and connect to other components or
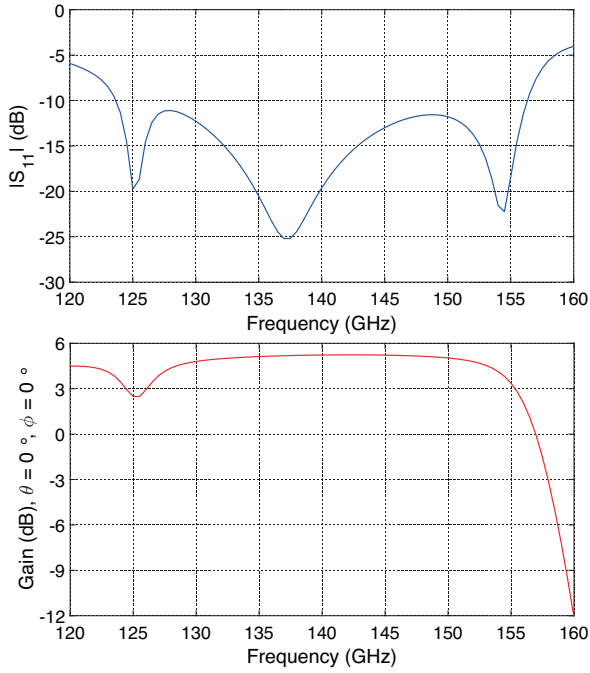
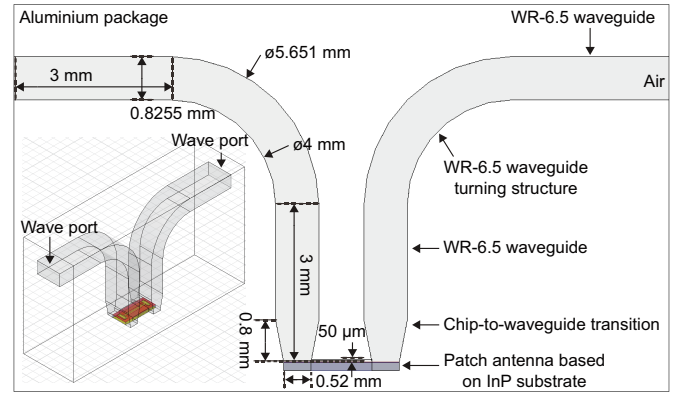Fig. 5. Simulated return loss and gain of the on-chip patch antenna.

Fig. 6. Rectangular waveguide packaging structure of the optimized on-chip patch antenna.

Fig. 7. Dimensions of the optimized on-chip patch antenna.

systems. At such high frequencies, rectangular waveguide is used as the standardized interface for connecting or cascading different circuits and components. It is also the primary type of transmission line used for guiding electromagnetic waves into and out of the circuits due to its simple structure and low loss property. Under this circumstance, the designed on-chip patch antenna can also be implemented for a chip-to-waveguide transition, in which the on-chip patch antenna is optimized and packaged by using D-band rectangular waveguide (WR-6.5, 110–170 GHz). Fig. 6 shows the rectangular waveguide packaging structure of the optimized on-chip patch antenna in back-to-back configuration. WR-6.5 rectangular waveguide is used as the input and output of the packaging structure. The width and height of WR-6.5 rectangular waveguide are 1.651 mm and 0.8255 mm, respectively. Electromagnetic waves are guided inside the rectangular waveguide and turn 90° towards the direction of the maximum antenna gain. Before electromagnetic waves reaching the on-chip patch antenna, the height of the rectangular waveguide is reduced from 0.8255 mm to 0.52 mm forming a chip-to-waveguide transition which smoothly guides the electromagnetic waves from the rectangular waveguide to the on-chip patch antenna. The width of the tapered structure are kept constant and the length is 0.8 mm. The on-chip patch antenna is located at the center of the packaging structure with an air cavity above the substrate. The height of the air cavity is 50 μm with the purpose of suppressing parasitic modes.

Since the on-chip patch antenna in back-to-back configuration is packaged using rectangular waveguide inside an aluminium box, the dimensions of the on-chip patch antenna are optimized based on the new boundary conditions. As is shown in Fig. 7, two optimized on-chip patch antennas are connected by a 50 Ω ECPW in the middle with a length of 860 μm. The length and width of the whole InP substrate are 2.214 mm and 0.947 mm, respectively. It is also the typical
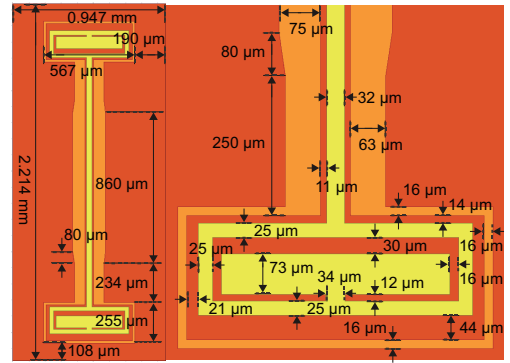
size of InP transceiver chips at 140 GHz. The length of the cavity is the same as the length of the InP substrate which means there is no gap between the end of the substrate and the wall of the cavity. It helps to suppress parasitic modes and align the InP substrate at the correct position.

Fig. 8 shows the simulation results of the chip-to-waveguide transition in back-to-back configuration. Wave ports are used as the excitation scheme and they are assigned to the input and output surfaces of the packaging structure. The chip-to-waveguide transition in back-to-back configuration exhibits a simulated return loss of 10 dB and insertion loss of 3 dB from 128 GHz to 153 GHz which covers the transmission frequency band and proves the wideband matching behavior of the optimized on-chip patch antenna. Besides on-chip antenna, E-plane probe and wire bonding can also be used for chip-to-waveguide transitions [4].

In Fig. 9, the assembly structure of the chip-to-waveguide transition in back-to-back configuration is shown. The packaging structure shown in Fig. 6 is divided into 3 parts and each part can be manufactured from an aluminium box by milling. By using a spinner with a diameter of 400 μm, the milled cavity for InP substrate has rounded corners.

IV. Extended Packaging Structure of the System

For higher directivity, a horn antenna is used together with the chip-to-waveguide transition forming an extended packaging structure that is suitable for the wireless communication system. Instead of direct chip-to-chip communication,
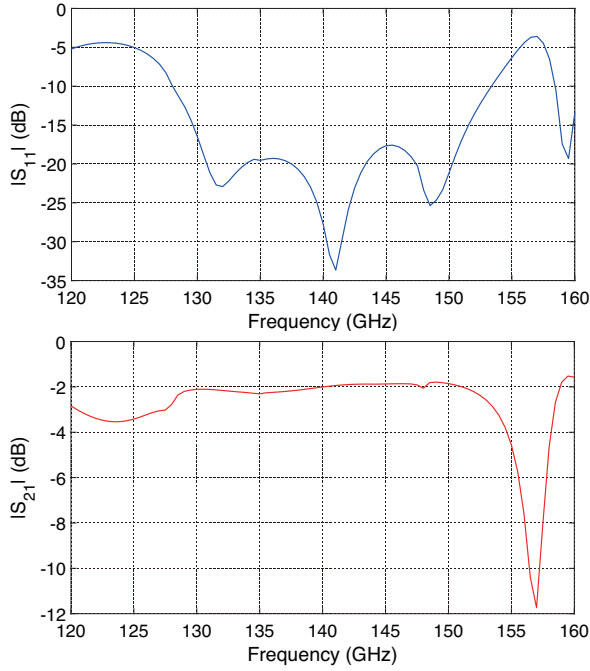
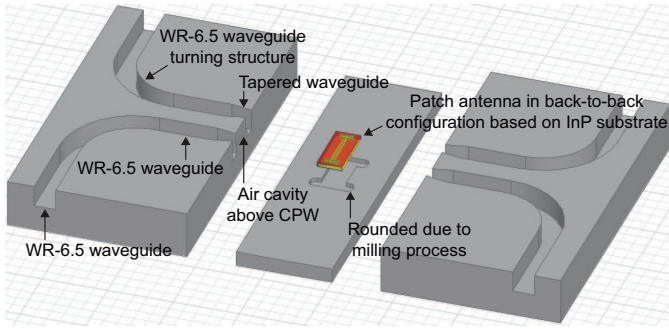Fig. 8.   Simulation results of the chip-to-waveguide transition.

Fig. 9.   Assembly structure of the chip-to-waveguide transition.

Fig. 10.   Extended packaging structure of the system.

Fig. 11.   Far-field radiation pattern of the extended packaging structure at 140 GHz.

the transceiver chips are packaged which makes the system more stable and increases the directivity. Fig. 10 shows the extended packaging structure of the transceiver chips. The chip-to-waveguide transition demonstrated in Fig. 6 can be used for packaging of the transceiver chips and the on-chip patch antenna has the same dimension as it is shown in Fig. 7. The on-chip patch antenna is fed by a ECPW with a length of 370 μm. Besides, E-plane horn antenna is used for free-space data transmission which can be connected to rectangular waveguides and provide high antenna gain in a wide frequency range. The E-plane horn antenna is a sectoral horn flared in the direction of the E-field in the waveguide. The width and height of the antenna aperture are 1.651 mm and 3 mm, respectively. The length of the E-plane horn antenna is 4 mm.

In order to generate the correct mode at the feed point, wave port is used as the excitation scheme in the simulation and the edges of the wave port touch the ground traces of the ECPW feed. For simulating far-field radiation, an air box is added around the extended packaging structure and it is large enough reaching the far-field region. The coordinate system for calculating far-field radiation pattern, as is shown in Fig. 10,
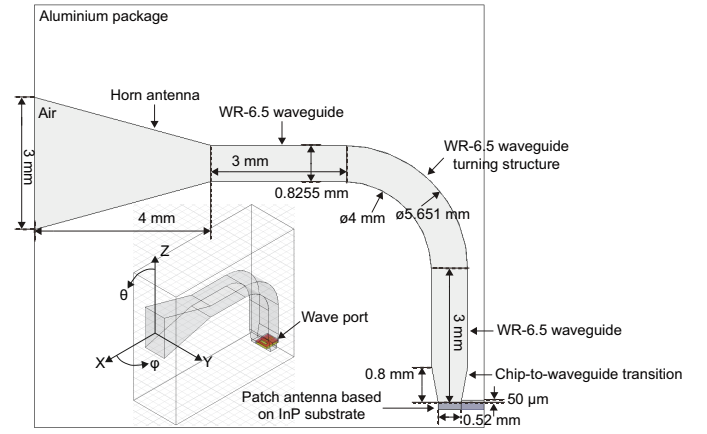
is located at the center of the antenna aperture. The simulated far-field radiation pattern of the E-plane horn antenna together with the system packaging structure at 140 GHz is shown in Fig. 11. A maximum gain of 11.9 dBi is achieved at the direction when θ and ϕ are 90° and 0°, respectively.

Fig. 12 shows the simulation results of the extended system packaging structure. The simulated return loss is better than 10 dB from 123 GHz to 153 GHz which covers the transmission frequency band and represents 21.4% bandwidth at 140 GHz. In the transmission frequency band, the simulated maximum gain is 12.3 dBi while the minimum gain is 10.3 dBi. The difference between the maximum and minimum values is 2 dBi which guarantees a good uniformity of the data power level through a free-space communication link.

Fig. 13 shows the assembly structure of the packaged transceiver chips. The extended packaging structure shown in Fig. 10 is divided into 3 parts and each part can be manufactured from an aluminium box by milling. The on-chip patch antenna, in the assembly structure, represents the transceiver chips and the cavity size needs to be adjusted when the full transceiver chips are packaged. The milled cavity has rounded corners due to the spinner whose diameter is 400 μm.

V.   CONCLUSION

The design of on-chip patch antenna on InP substrate for short-range wireless communication at 140 GHz has been presented. A chip-to-waveguide transition has been implemented by using the on-chip patch antenna with optimized dimension. Besides, an extended packaging structure is proposed for
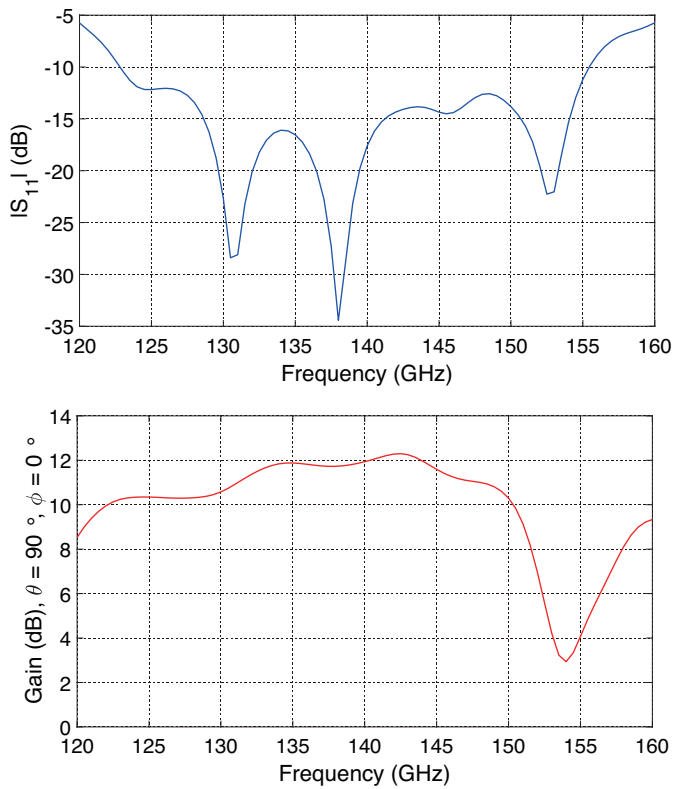
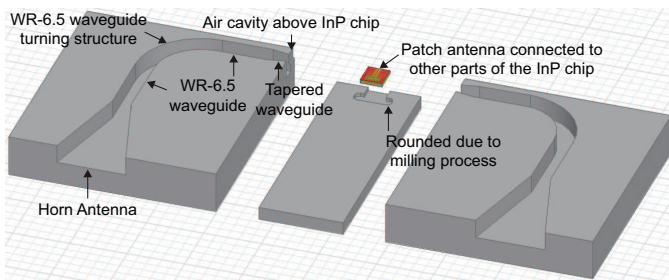Fig. 12. Simulation results of the extended packaging structure.

Fig. 13. Assembly structure of the extended packaging structure.

the system consisting of chip-to-waveguide transition and E-plane horn antenna. For direct chip-to-chip communication, the designed on-chip patch antenna shows a simulated gain of 5.3 dBi with 23% bandwidth at 140 GHz. In the transmission frequency band, a good gain uniformity has been achieved. The maximum simulated gain of the designed on-chip patch antenna is 5.3 dBi while the minimum value is 4.8 dBi. The chip-to-waveguide transition in back-to-back configuration has been demonstrated. The dimensions of the on-chip patch antenna have been optimized due to the packaging boundary conditions. The proposed packaging structure consists of WR-6.5 rectangular waveguides, chip-to-waveguide transitions, and optimized on-chip patch antennas. The chip-to-waveguide transition in back-to-back configuration exhibits a simulated return loss of 10 dB and insertion loss of 3 dB from 128 GHz to 153 GHz. The assembly structure has been shown to prove the possibility of manufacturing the proposed packaging structure by aluminium milling. As for the system packaging of the

transceiver chips, the extended packaging structure consists of on-chip patch antenna, chip-to-waveguide transition, WR-6.5 rectangular waveguide, and E-plane horn antenna. A simulated return loss of 10 dB has been achieved from 123 GHz to 153 GHz which covers the transmission frequency band and represents 21.4% bandwidth at 140 GHz. In the transmission frequency band, the maximum simulated gain is 12.3 dBi while the minimum value is 10.3 dBi.

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