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Davidsen, Jeppe Gaardsted; Yosef-Hay, Yoni; Larsen, Dennis Øland; Jørgensen, Ivan Harald Holger

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Synthesis and Design of a Fully Integrated Multi-Topology Switched Capacitor DC-DC Converter with Gearbox Control

Jeppe Gaardsted Davidsen* Yoni Yosef-Hay* Dennis Øland Larsen*†, Ivan H. H. Jørgensen*
*Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, Denmark
†R&D Hardware Platforms IC, GN Hearing A/S, Ballerup, Denmark
s134087@student.dtu.dk, s154607@student.dtu.dk, deno@elektro.dtu.dk, ihhj@elektro.dtu.dk

***Abstract*—This paper discusses a methodology of minimizing the amount of switches in a multi-topology fully integrated switched capacitor dc-dc converter powered by a super capacitor for energy harvesting purposes. The design of a simple controlling circuit for the multi-topology power stage using a gearbox approach is presented with all the required circuits. The converter is able to generate a output voltage of 1.2 V from a 470 mF capacitor charged to 3 V down to 1.4 V. The output voltage is regulated with a ripple voltage below 7 mV. The controlling circuit including buffers with ideal comparators has a power consumption of 129 μW, the average efficiency is 67% and the peak efficiency of the converter is 81%.**

I. Introduction

With the current trend of combining digital and analogue circuitry on to a combined Systems-on-Chip (SoC), power management is more vital than ever. Due to this trend the dc-dc converters are starting to get integrated into the same chip and switched mode converters are the main integrated solutions [1].

In portable devices there are strict requirements on area and power consumption. Inductive dc-dc converters are very popular for external supplies, they however have their limitations when being integrated due to the magnetic devices and need for external components. Even though inductors are getting smaller due to high frequency switching their size is still not applicable to portable devices [2]. Fully integrated switched-capacitor (SC) dc-dc converters are more feasible to integrate in CMOS technologies due to their higher power-density and high efficiency [1].

The efficiency of SC converters is very dependent on the choice of topologies as a certain topology can only achieve a theoretical 100% efficiency at one specific voltage-conversion-ratio (VCR $= V_{out}/V_{in}$). Thus the choice of the topologies is very important to achieve a high average efficiency for the entire input voltage range.

The SC converter for this project will have to generate a 1.2 V output voltage for minimum of 8 minutes when the input capacitor is fully charged. The energy is supplied from a 470 mF super capacitor which have been charged by energy harvesting. The voltage of the input capacitor will range between 1.4 V and 3 V. Furthermore, the output voltage should not be more than 3 mV below the 1.2 V output voltage when the SC converter is operating and in general the peak-peak ripple voltage should be below 7 mV. The specifications for the SC converter are summed up in Table I including the current steps which can be expected at the output.

TABLE I. Converter specification

$\mathbf{V_{in}}$	1.4 V - 3 V	$\mathbf{R_{out,min}}$	30 Ω
$\mathbf{V_{out}}$	1.2 V	$\mathbf{V_{ripple}}$	7 $\mathrm{mV_{pp}}$
$\mathbf{I_{load}}$	50 μA - 2 mA	$\mathbf{I_{step,1\mu}}$	0.5 mA → 1.1 mA
$\mathbf{f_s}$	10 MHz	$\mathbf{I_{step,5\mu}}$	1 mA → 2 mA
$\mathbf{C_{out}}$	350 nF	$\mathbf{V_{out,min}}$	1.197 V
$\mathbf{C_{in}}$	470 mF	**Min reg. time**	8 min

This paper will go through the process of designing a SC converter with the minimum amount of switches for application in energy harvesting systems. It will be presented how to find the maximum amount of common phases for different conversion ratios. Furthermore the circuits for controlling the SC power stage using a gearbox approach will be presented and a simulation in schematic level will be presented.

II. Switched Capacitor Losses

SC converters are often modeled as an ideal transformer with a varying non zero output impedance, R_{out} where only certain conversion ratios of VCR is available [3].

The losses for SC converters are separated into intrinsic and extrinsic losses. The losses due to the non-zero output impedance are called the intrinsic losses and can be described by (1), the intrinsic losses are due to the operation of the SC converter.

$$P_{Rout} = R_{out} I_{load}^2 \tag{1}$$

where the output impedance for SC converters can be described using equations (2)-(3), [4]:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2}$$

$$R_{SSL} = \frac{K_C}{C_{tot} f_s} \qquad R_{FSL} = \frac{2K_S}{G_{tot}} \tag{3}$$

where R_{SSL} and R_{FSL} is the effective resistance in the slow switching limit (SSL) and fast switching limit (FSL), K_C and K_S are proportionality constant associated with the structure of the capacitors and switches respectively, f_s is the switching frequency, C_{tot} is the total amount of flying capacitance and G_{tot} is the total conductance due to the switches. The intrinsic loss and output impedance for each topology is changed

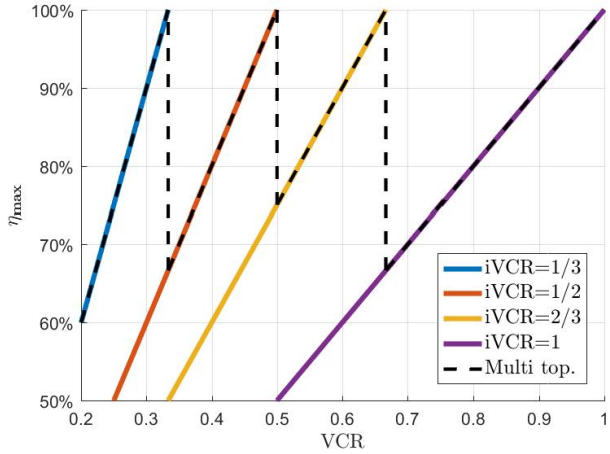

Fig. 1. Different conversion ratios maximum efficiency as a function of the VCR

with the switching frequency effectively regulating the output voltage.

The extrinsic losses are caused by the switching operation of the SC converter. The two main switching losses are the loss due the parasitics at the gate of the switches, see (4), and the bottom-plate losses of the flying capacitors, see (5).

$$P_{gate} = \sum_i V_{gate,i}^2 f_s C_{gate,i} \tag{4}$$

$$P_{bp} = \sum_j V_{node,j}^2 f_s C_{bp,j} = \sum_j V_{node,j}^2 f_s \alpha C_{fly,j} \tag{5}$$

where $V_{gate,i}$ and $C_{gate,i}$ is voltage change and the capacitance at the gate of switch i, $V_{node,j}$ and $C_{bp,j}$ is the voltage change and the capacitance at the bottom plate of the flying capacitors and α is the proportion of the flying capacitance which is considered to be the bottom plate capacitance. Further extrinsic losses in the SC converter are due to the switches which are not being used for a certain topology and due to the extra circuitry which are needed to operate the SC converter. It is important to note that the efficiency of the SC converter is mainly voltage dependent, and thus the choice and implementation of the conversion ratios have a great impact on the efficiency.

III. Synthesis of Multi-Topology Output Stage

When implementing a SC converter only a limited number of different VCRs can be obtained as proved in [5]. To get a good average efficiency the power stage of the SC converter need to be implemented using multiple conversion ratios. The maximum efficiency characteristics, $\eta_{max} = \mathrm{iVCR}/\mathrm{VCR}$ for a certain conversion ratio is only very efficient at a certain VCR. This can be seen in Fig. 1 where all possible step-down converters using 2 flying capacitors and 1 output capacitor have been plotted, the dotted line shows how the multi-topology is needed to increase the average efficiency.

Using the voltage distribution in time depending on the chosen conversion ratios, it was found that the average efficiency would not increase much if choosing more than

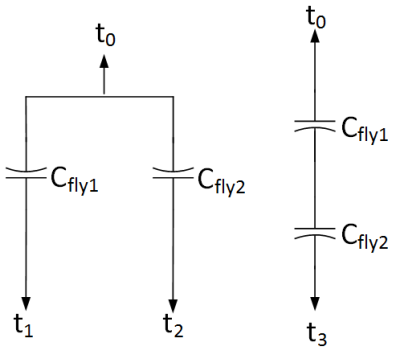

Fig. 2. A schematic representation of the two phases for the series-parallel SC converter with 2 flying capacitors and 4 terminals

TABLE II. Combined realization table for the 1/2, 2/3 and 1/1 conversion ratios

Terminal	t_0	t_1	t_2	t_3
1/2	V_{out}	V_{in}	V_{out}	V_{SS}
2/3	V_{out}	V_{in}	V_{in}	V_{SS}
1/1	V_{out}	V_{in}	V_{in}	V_{in}

three VCRs. The three optimal conversion ratios could all be implemented with 2 flying capacitors, thus the power stage of the SC converter should be able to realize the VCRs of 1/2, 2/3 and 1/1. The method used to design the SC converter took into account the operational losses in the converter.

If each conversion ratio had to be implemented with different switches optimized for each VCR there would be between 15-21 switches. However, by finding common phases between the different conversion ratios a lot of switches can be saved. An easy approach to find common phases, is to set up realization tables like done in [6] and look at the phases for the SC topology.

Using two flying capacitors the two phases for the series-parallel topology can be seen in Fig. 2. Here it can be seen that a common phase between two conversion ratios exist if terminals t_0, t_1 and t_2 are connected to the same nodes (input, output or ground). The same can be done if terminals t_0 and t_3 are connected to the same nodes. By setting up realization tables for all conversion ratios the common phases can easily be identified by finding two conversion ratios which utilizes the same nodes. In Table II it can be seen that the 2/3 and 1/1 conversion ratios have terminal t_0, t_1 and t_2 in common thus leading to a common phase. Conversion ratios 1/2 and 2/3 have terminals t_0 and t_3 in common, leading to one more common phase.

Realizing the power stage for the SC converter with this approach leads to the SC schematic seen in Fig. 3 where the switches should be operated as seen in Fig. III to realize the different conversion ratios.

IV. Implementation of circuits for SC converter

This section will go through the different circuits which has been implemented in order to control the multi topology power stage for the SC converter. The block diagram for this implementation can be seen in Fig. 6

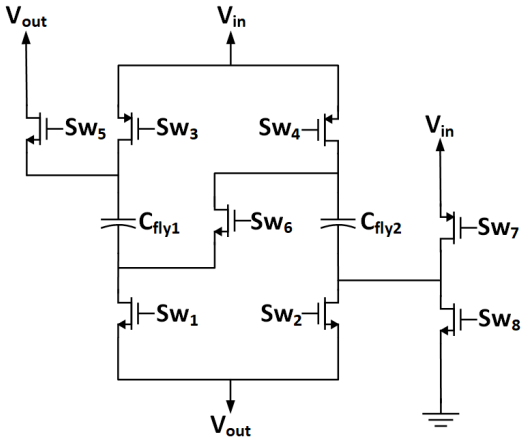

Fig. 3. A schematic representation of the SC circuit which can realize the 1/1, 2/3 and 1/2 topologies

TABLE III. SWITCH TABLE WHICH REALIZES THE DIFFERENT TOPOLOGIES ACCORDING TO FIG. 3

	Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	Sw8
1/2	ϕ_1	ϕ_1	OFF	ϕ_{1n}	ON	ϕ_2	OFF	ϕ_2
2/3	ϕ_1	ϕ_1	ϕ_{1n}	ϕ_{1n}	ϕ_2	ϕ_2	OFF	ϕ_2
1/1	ϕ_1	ϕ_1	ϕ_{1n}	ϕ_{1n}	ϕ_2	ϕ_2	ϕ_{2n}	OFF

A. Switching Regulation Stage

The switching regulating stage consist of pulse skipping and non over-lapping clock stages. The implementation of the proposed pulse skip design can be seen in Fig. 4 .

The pulse skippers purpose is to skip clock pulses depending on V_{out}. The two inputs to the comparator are V_{out} and V_{ref}, the output voltage is compared with the reference voltage. In case $V_{out} > V_{ref}$ the comparator output is grounded and the output of the AND gate is therefore also set to logic '0'. If $V_{ref} > V_{out}$ the output of the AND gate is the clock. The D-flipflop has a negative edge reset that is connected to the clock. This will result in Q equal to V_{ref} when $V_{ref} > V_{out}$ and clock at rising edge, on the other hand when the clock is low the reset is enabled and Q will be equal to zero regardless of the input D.

The non-overlapping clock stage is critical to the operation of the SC converter. Non-overlapping clock signals are generally required to operate corresponding switches which charge and discharge the flying capacitors. Non-overlapping clock signals means signals running at the same frequency and there is a time between the pulses that both pulses are logic 0 (for the positive phases), this time is called dead-time. Dead-time takes place when the pulses are switching from logic 1 to logic 0 or from logic 0 to logic 1. The dead-time for the design was set to 3 ns and can be easily adjusted by changing the W/L ratio of the internal buffer stage. The non-overlapping clock stage has 4 output signals, a negation signals for ϕ_1 and ϕ_2

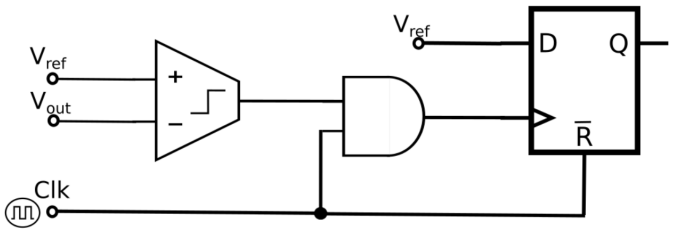

Fig. 4. Schematic of the pulse skip stage

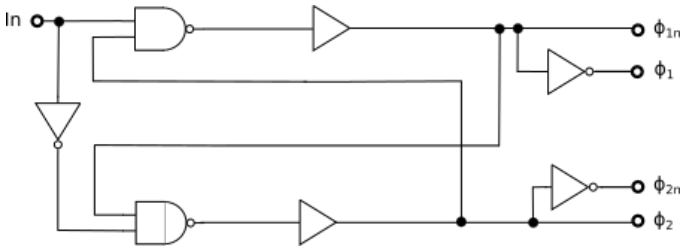

Fig. 5. Schematic of the non-overlapping clock stage

called ϕ_{1n} and ϕ_{2n}. This is due to the gear shift circuit which will be discussed in the following section and needs to switch both PMOS and NMOS transistors. The implementation of the non-overlapping clock stage is shown in Figure 5.

B. Gearshift stage

The gear shift stage was implemented to efficiently switch between the multiple conversion ratios of the power stage. This design supports the battery voltage (V_{in}) range 1.4 V - 3 V, with the three different step down topologies to maintain an output of 1.2 V. It has a low power density and maximal efficiency over the battery voltage ranges. The gear shift stage proposed is to utilize the different topologies and operate the required topology in the input range intended.

In order to drive the SC stage, the gear shift stage outputs eight switch signals (Sw_1 - Sw_8) in Fig. 3. The conversion ratio of the SC stage is depended on the switch state. Table III describes the switches phases for every conversion ratio. The implantation of the multi-topology power stage utilizes the same four switches in all conversion ratios ($Sw_1, Sw_2, Sw_4.Sw_6$) and therefore these switches do not require to be altered when operating in different conversion ratios. The other switches (Sw_3, Sw_5, Sw_7, Sw_8) are set to the same phase or supply in two conversion ratios out of three. Sw_3 and Sw_5 are common for conversion ratio 2/3 and 1/1, while Sw_7 and Sw_8 are common for topologies 1/2 and 2/3. This SC implementation made it possible to create an efficient and effective way to shift between the topologies by controlling only 4 of the 8 switches.

The challenge in the gear shift stage is to set the correct phase or supply according to the battery voltage. The controller

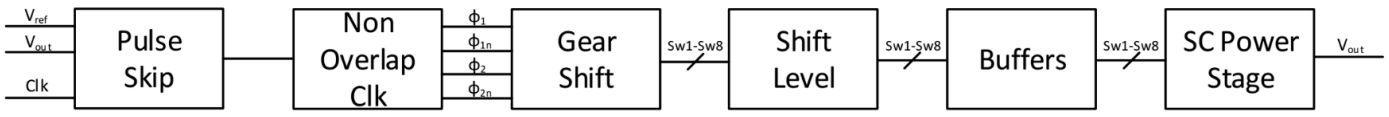

Fig. 6. Block diagram of the control gearbox with the switched-capacitor stage

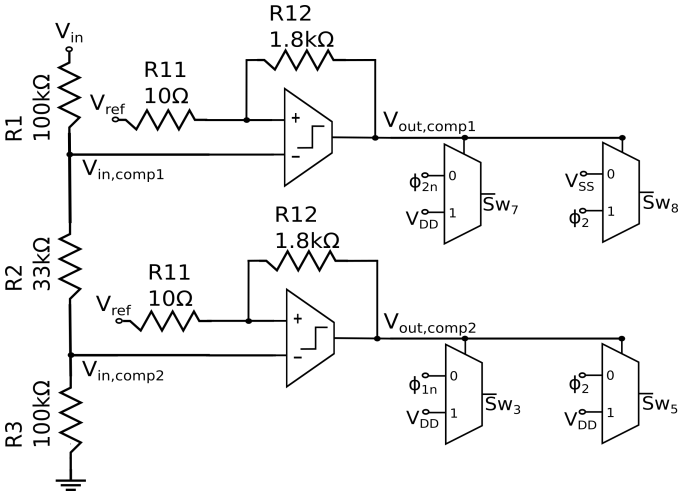

Fig. 7. Schematic of the Gear Shift Stage

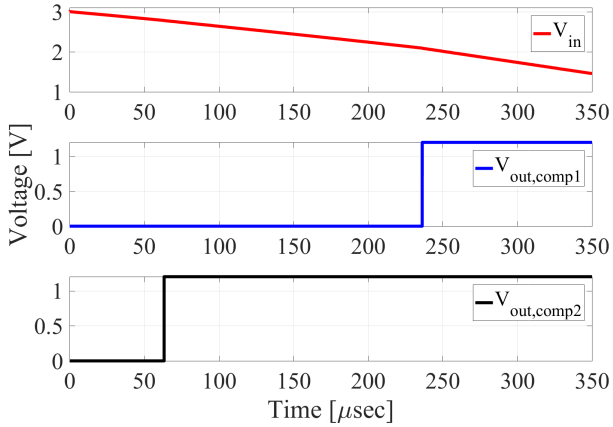

Fig. 8. Wave Forms of the comparators outputs

is designed to implement the switching described in Table III. It consists of resistors, comparators and multiplexers (MUXs). The resistor chain is used to scale down the battery voltage, there are two different scaled down voltages with a value depended in the battery voltage ($V_{in,comp1}$ and $V_{in,comp2}$). The resistor ratio will lead to an input to the first comparator $V_{in,comp1}$ of V_{in}/1.75, the second input $V_{in,comp2}$ will be scaled down to V_{in}/2.5. The value of the resistors in the resistor ladder is set so that the current limit is 6 µA. The scaled down voltage is then compared with a reference voltage of 1.2 V. By comparing the scaled voltage with the reference voltage the intended conversion ratio is applied for a the intended input voltage range. An the range of 2.8 V - 3 V both outputs will be lower than the reference voltage and thereby setting $V_{out,comp1}$ and $V_{out,comp2}$ to V_{SS}. For input voltages between 2 V - 2.8 V will result in $V_{out,comp1}$ equal to V_{SS} and $V_{out,comp2}$ set to V_{DD}. For the input voltage range 1.4 V - 2 V, $V_{out,comp1}$ and $V_{out,comp2}$ will be V_{DD}. One can understand the idea behind the voltage divider as having two different bits ($V_{out,comp1}$ and $V_{out,comp1}$) that will be set to V_{SS} or V_{DD} and will represent 3 states of input voltage range. The different outputs for every topology can be seen in Table IV, Fig. 8 is the waveform showing the correct functionality of the voltage ladder with the comparator.

TABLE IV. SUMMARY OF COMPARATOR OUTPUTS DEPENDED ON THE BATTERY VOLTAGE

Battery Voltage [V]	Intended topology	$V_{out,comp1}$	$V_{out,comp2}$
1.4 - 2.0	1/1	V_{DD}	V_{DD}
2.0 - 2.8	2/3	V_{SS}	V_{DD}
2.8 - 3.0	1/2	V_{SS}	V_{SS}

The outputs of both comparators are connected to select signal of the multiplexers. For Sw_7 and Sw_8 the common conversion ratios are 2/3 and 1/2, in this case $V_{out,comp1}$ is controlling both switch signals. When $V_{out,comp1} = V_{SS}$ the multiplexers selects the common phases for those topologies (V_{DD} and ϕ_2). When $V_{out,comp1} = V_{DD}$ the two switches should present the state for the 1/1 topology, $Sw_7 = \phi_{2n}$ and $Sw_8 = V_{SS}$.

Sw_3 and Sw_5 are common for topologies 1/1 and 2/3, these conversion ratios require the same phases and therefore are connected to $V_{out,comp2}$ which control these switches. When $V_{out,comp1} = V_{DD}$, the multiplexers outputs will be connected to ϕ_{1n} and ϕ_2. When $V_{out,comp2} = V_{SS}$, this means the input voltage is between 2.8 V - 3 V, Sw_3 and Sw_5 will be connected to V_{DD} as required in the 1/2 topology.

The resistors R_{11} and R_{12} are placed in the feedback path of the comparator in order to ensure a 10 mV hysteresis. These are necessary to avoid high frequency toggling between the conversion ratios. To solve the inverted output logic of the comparator, which is connected to the select signal in the MUX, the inputs of the MUX where switched. The switched inputs can be seen in Fig. 7.

C. Comparator

For this paper ideal comparators have been used in the pulse skipper and the gearshift stage. If the comparators were to be designed they would be designed as clocked comparators. Even though ideal comparators have been used it would not have a huge impact on the power consumption as the speed requirements of the system is relatively slow. As seen in [7] and [8] a faster comparator can be designed using only between 1.33 nW and 6 nW, thus the power consumption for the SC converter would not increase much as only 3 comparators are used in total. Furthermore, the noise generated by the comparators is not critical as we are dealing with a converter and not something more sensitive, which could lead to a very low power design.

D. Level shifter

To be able to pull the signal at the gates of the transistors up to the desired level of $V_H = 3$ V, a level shifter is implemented. The reason for this being a necessity is the fact the control circuit should be able to run at only 1.2 V to minimize losses here while still having high signals available for the gates. The chosen level shifter topology for this project can be seen in Fig. 9.

When the input voltage, V_{in}, for the level shifter goes high the N_1 and P_2 turns on, while the other transistors are off, and thus V_H is applied at the output node V_{out}. Whenever V_{in} goes low the N_2 and P_1 transistors turn on and V_{out} is discharged.

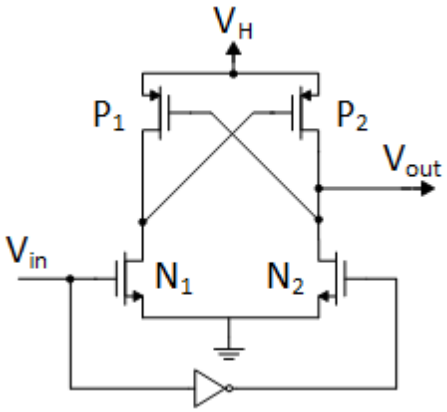

Fig. 9. Schematic for the level shifter topology

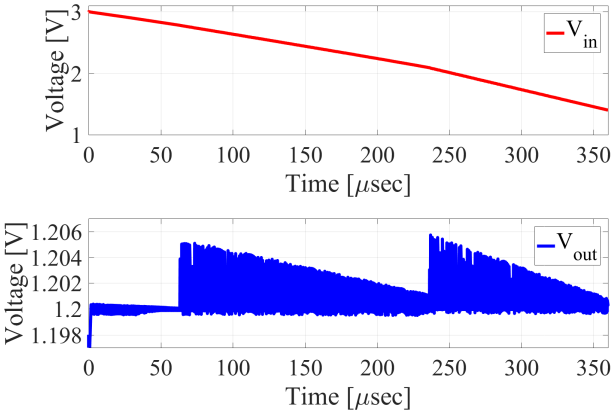

Fig. 10. Transient response simulation with 2 mA constant load current

E. Buffers

The buffers are needed to drive the large gate capacitance of the switches in the power stage. The buffers were optimized to save power rather than speed as described in [9]. The buffer was designed to drive the largest switch in the power stage and was reused for the other switches for simplicity. More power could naturally be saved by optimizing the buffers for each switch. Furthermore the buffers were designed after the specification for dead time given by the non overlapping clock of 3 ns. Thus the buffers should be able to turn on and off in less than 3 ns to avoid shoot-through-currents.

F. Power stage

As all the conversion ratios are implemented with common phases the optimization approach presented in [4] can only be used on one of the topologies. It was chosen to do this for the 2/3 conversion ratio as this is where the converter is operated for the majority of the time. The corner frequency between the SSL and the FSL is set to the switching frequency at 10 MHz and the output impedance is set to 30 Ω as this frequency, as specified in Table I. Using the opimization approach and (2)-(3), the individual flying capacitance and switch conductance can be found to be $C_i = 1.05$ nF and $G_i = 73$ mS.

It was chosen to implement the flying capacitors, C_i, as MOS capacitors as these provide the highest density. However, due to the bigger bottom plate parasitics for MOScaps the efficiency will decrease but area for the capacitors will be saved. The switches were implemented as NMOS and PMOS transistors which were sized so that the conductance would be $G_i = 73$ mS.

V. Simulation Results

The proposed SC converter has been implemented in a 180 nm CMOS process. The results that are presented in this section include the complete design behavior in transient simulation on schematic level. Due to simulation time the system has not been tested with the 470 mF but with a 350 nF capacitor as this will of cause result in a lower regulation time but there should be a linear relationship with the regulation time and capacitor size difference.

The worst case for the regulation time would be if a constant output load current of 2 mA was applied to the converter. This case can be seen in Fig. 10 where the final regulation time is 360 µs. Using the worst case regulation time corresponds to a regulation time of 8.1 minutes if the input capacitor was changed to the 470 mF super capacitor. The low voltage seen in the beginning of Fig. 10 is a start-up phenomenon and does not influence the performance of the SC converter.

TABLE V. Average power consumption for the controlling circuits with a constant 2 mA load

Circuit	Pulse skipper	Non-overlap	Gearshift	Level shifter	Buffers
Power consumed	239 nW	3.5 µW	11.7 µW	7.2 µW	106 µW

The average power consumed by the different parts of the system running, see Fig 6, with a constant 2 mA current load can be seen in Table V, this leads to a average efficiency at $\eta_{avg} = 0.67$.

The efficiency of the power stage can be seen in Fig. 11. The peak efficiency of the converter is $\eta = 0.81$ for the 1/1 conversion ratio around 1.4 V. The low peak efficiency is due to a combination of the high switching frequency, and the capacitors available in the 180 nm process. A higher efficiency can be obtained if the MIM capacitors in the process were used, however this would lead to a bigger area consumption. It has been estimated through simulations and (2)-(5) that the losses in the power stage is due to 14% intrinsic losses, 22% from switching losses at gate and 64% switching losses at the bottom plate.

In Fig. 12 the transient response while constantly changing the load step between 1 mA to 2 mA is plotted. The current have a 20 µs period, a duty cycle of 50% and a 5 µs rise and fall time. The simulation was preformed with C_{out} = 350 nF. It should be noted that a smaller current reduces the amount of current drawn from the supply and therefore the input voltage drains slower, as seen when comparing Fig. 10 and 12. Furthermore, it can be seen that the ripple voltage is below the specified 7 mV and it can be seen that the output voltage never goes below the minimum specified 1.197 V. The reason the output voltage is not dropping below 1.197 V when switching between conversion ratios is the converter is able to compare input and output voltages multiple times when the

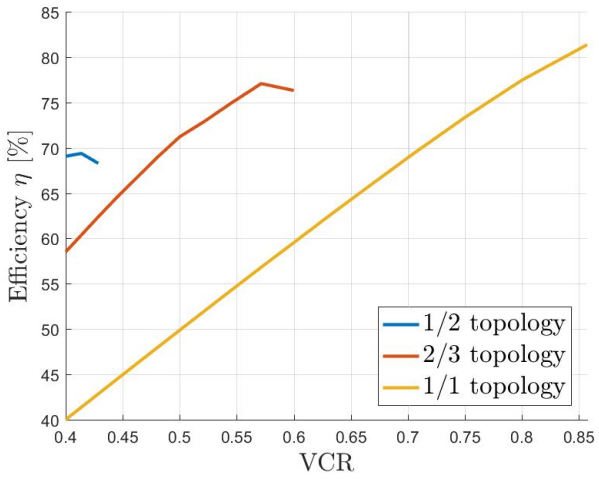

Fig. 11. Efficiency for the SC converter

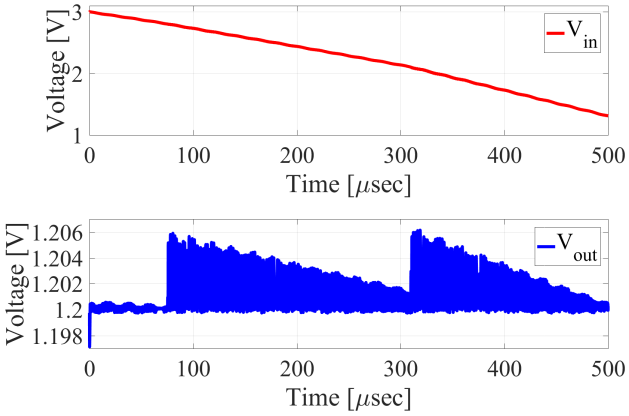

Fig. 12. Transient response simulation with current step 1 mA to 2 mA

load current is stepped.

VI. Discussion

The realization approach used to realize the different conversion ratios with minimal switches leads to the 1/2 topology being implemented very poorly as the minimum output resistance never gets below 68 Ω relative to the allowed 30 Ω as seen in Fig. 13. This makes the intrinsic losses very large and thus the efficiency for this topology is much lower compared to the other topologies implemented.

To improve this one additional switch should be used so that the two flying capacitors is placed in parallel for this application. This would however increase the complexity of the control circuits as less switches are common for the different conversion ratios. However, it is worth noticing that the 1/2 conversion ratio did not require any additional switches in the power stage and thus the efficiency gained from this can be considered free.

VII. Conclusion

This paper describes an easy methodology to minimizing the number of switches required to implement a multi-topology

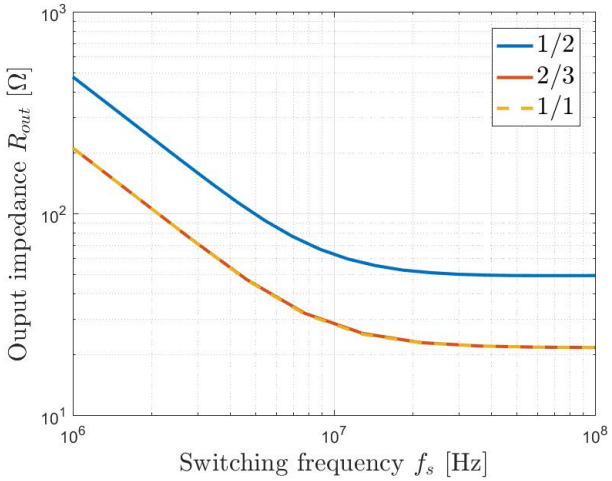

Fig. 13. Effective output impedance of the SC power stage

SC power stage by using common phases. By reducing the many switches in the power stage made it possible to implement a simpler gearbox control circuit. The realization method however also leads to one of the conversion ratios having a reduced performance.

The designed SC converter is able to regulate a 1.2 V output supply voltage with an input voltage in the range of 1.4 V to 3 V supplied from a super capacitor of 470 mF for 8.1 minutes. This regulations is done with ripple voltage below 7 mV and a peak efficieny of 81%.

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