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# High-Voltage Integrated Linear Regulator with Current Sinking Capabilities for Portable Ultrasound Scanners

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**Abstract**—This paper presents a high-voltage integrated regulator capable of sinking current for driving pulse-triggered level shifters in drivers for ultrasound applications. The regulator utilizes a new topology with a feedback loop and a current sinking circuit to satisfy the requirements of the portable ultrasound scanner: a great driving strength in the scanner’s transducer and a low undershoot voltage in the output node. The design regulates an output voltage of 45 V from an input voltage of 50 V, and it can sink currents up to 100 mA using no external components with only 340 mV of undershoot voltage. The proposed design has been implemented in high-voltage 0.18  $\mu\text{m}$  process within an area of 0.11  $\text{mm}^2$  and it is suitable for system-on-chip integration due to its low component count and the fully integrated design.

## I. INTRODUCTION

Medical scanning using ultrasound devices is a technique widely used due to its operating simplicity, non-invasive nature, live imaging capabilities and extended diagnosis range. However, the static ultrasound scanners that are currently used are large and plugged in the grid, because of their high power consumption and over-designed devices.

The trend of ultrasound scanners has been in the direction of portable scanners as they are cheaper and more power efficient. The main challenges in the design of portable scanners are the power dissipation, the power consumption and the size.

A medical ultrasound scanner consists of several channels, each one with a transducer, transmitting circuit (Tx) and a receiving circuit (Rx). The Tx part produces a high-voltage signal to excite the transducer that generates the ultrasound wave. The reflection of the ultrasound wave is induced in the transducer is amplified and digitalized in the Rx part.

In order to reduce power consumption, the Tx part is designed for driving a given transducer. For this study, the Tx part designed in [1] has been considered with the pulse-triggered level shifter configuration with  $V_{HI} = 50$  V and  $V_{LO} = 45$  V, referred to Fig.1.

The purpose of the design presented in this paper is supplying the  $V_{LO} = 45$  V node from the  $V_{HI} = 50$  V. Regulators can be switch mode (SM) or linear. SM regulators are bidirectional converters that have a very good efficiency [2]. However, they

need an inductor, so they cannot be fully integrated in silicon. On the other side, linear regulators can be highly integrated and save a lot of volume, which is a major issue when making a portable scanner. The possibility of integration shows that is the best option for the requirements of the project. Typical linear regulators are designed to source current to the load [3], but this regulator needs current sinking capabilities, hence, a new topology is required. An application specific integrated circuit (ASIC) solution is needed to custom design the electronics and minimize the size and power consumption needed for the device.

This paper presents a high voltage integrated linear regulator with current sinking capabilities for driving the lower supply rail,  $V_{LO}$  of the pulse-triggered level shifters in portable ultrasound scanners designed in [1]. The circuit is designed and implemented in high-voltage 0.18  $\mu\text{m}$  process.

## II. CIRCUIT SPECIFICATION

The designed circuit is capable of supplying 8 Tx channels of the ultrasound scanner. As explained in [1] the circuitry is designed for a given ultrasound transducer; in this case the transducer needs a driving strength corresponding to a slew-rate (SR) of 2 V/ns.

Additionally, due to the pulse-triggered level shifter structure, there are some limitations in the voltages for the  $V_{LO}$  node, as referred in the Fig.1. The breakdown gate-source voltage for the MOS devices, whose source voltage is determined the output voltage of the regulator, is 5.5 V. Hence, the maximum undershoot in the output voltage is  $V_{LOmin} = 50 - 5.5 = 44.5$  V

The schematic of the level shifter, as shown in Fig.1, determines that the  $V_{LO}$  node is sinking current. A simulation with ideal power supplies that produces the desired driving signal in the transducer has been done. The driving signal is a 5 MHz square waveform with 50 V amplitude, that can be seen in the Fig.2 in blue. During the rising edge in the transducer voltage, the current waveform to be sunk by the regulator has a peak of 324 mA during 3 ns, followed by a flat zone at

55 mA that lasts for 30 ns. At the falling edge, a peak of 90 mA is occurred.

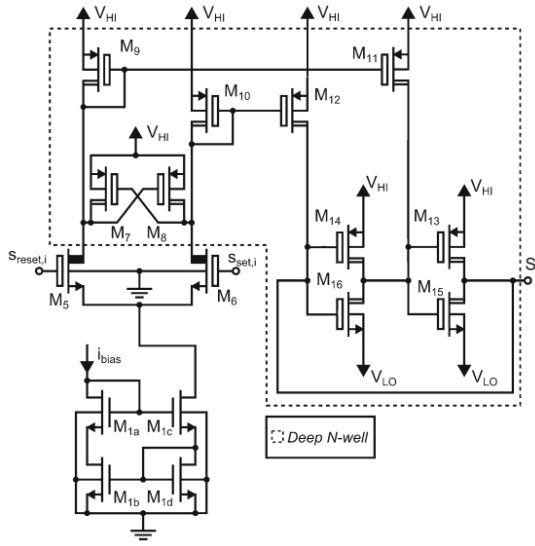


Fig. 1. Pulse-triggered level shifter extracted from [1].

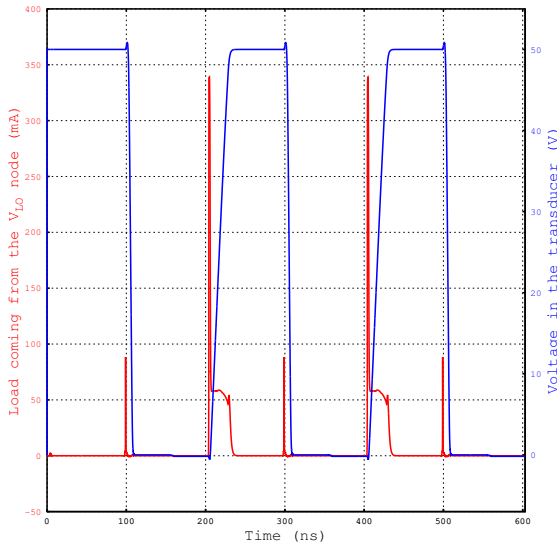


Fig. 2. Ideal voltage waveform in the transducer (red) and current profile to be sunk by the regulator (blue).

### III. CIRCUIT DESCRIPTION

In this section, the design of the different blocks of the regulator is described. In each part, the specifications and design choices are discussed. The main focus for the design of the system is satisfying the specifications for the  $V_{LOmin} = 44.5$  V and the driving strength in the transducer corresponding to a  $SR = 2$  V/ns in the driving signal waveform, and lowering the power consumption.

As it is possible to see in the Fig.3, the system is composed of an operational amplifier, an output stage and a current sinking circuit. The PMOS transistors have the bulk connected to  $V_{HI} = 50$  V and the NMOS transistors have the bulk connected to  $V_{SS}$ . The operational amplifier compares the  $V_{LO}$  node with 45 V and it amplifies the error. The operational amplifier controls the output stage formed by M1, M2, M3 and M4 and sets the  $V_{LO}$  node voltage. The current sinking circuit, formed by M5, Q1 and R4, is triggered by a high level of current flowing in M2 and M4 and it is activated by the current mirror M4, M5.

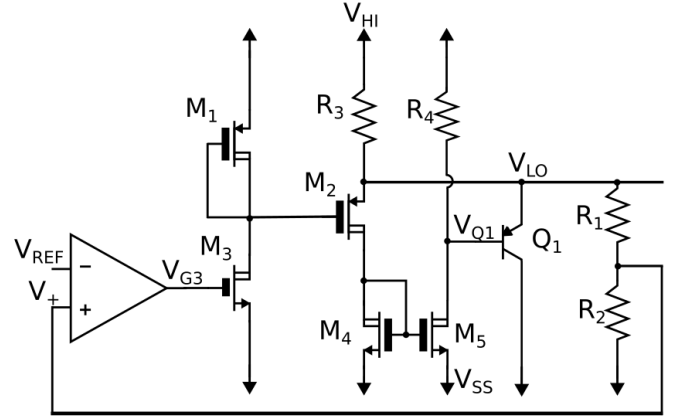


Fig. 3. Functional diagram for the proposed system.

As stated in [1], ultrasound scanners transmit for a short period, in this case 400 ns, and receive for a longer period, in this case 106.4  $\mu$ s. The sizes of the resistors R1, R2 and R3 set the desired voltage  $V_{LO} = 45$  V. This means that the operational amplifier, the output stage and the current sinking circuit can be switched off in the receiving mode, that represents more than the 99% of the time, which will lead to lower the power consumption.

The circuit designed is used for portable ultrasound scanners but it could potentially be used in other applications with a similar behaviour.

#### A. Operational Amplifier

The operational amplifier is supplied by 1.8 V to reduce the area and the power consumption of the block. It amplifies the error in the  $V_{LO}$  node to 45 V, thanks to a feedback from that node to the  $V_+$  input to the amplifier. The voltage in  $V_{LO}$  node is reduced to the 1.8 V domain thanks to the resistor divider R1, R2. For the performance of the regulator, the amplifier needs a gainbandwidth (GBW) of 60 MHz.

The selected topology is a symmetrical current mirror operational transconductance amplifier (OTA) because it has a low power consumption and a big output swing [4] that will be useful for controlling the gate of M3.

Considering that the gate capacitance of M3,  $C_{g3}$  referred to Fig.3, is 1 pF (based on simulations), the characterization of the transistors of the OTA is done with the equation 1.

$$GBW = B \cdot \frac{g_{m6}}{2 \cdot \pi \cdot C_{g3}} \quad (1)$$

$$\text{where } B = \frac{W_{11}}{W_9} \quad (2)$$

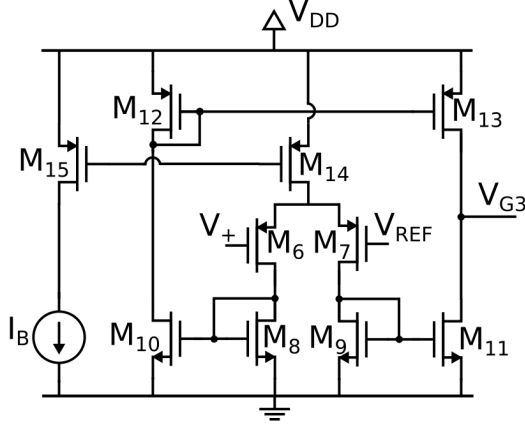


Fig. 4. Symmetrical OTA structure.

The final GBW of the OTA is 96 MHz, with a phase margin (PM) of  $60^\circ$  and a DC gain of 35 dB. The OTA is consuming a total of 208  $\mu\text{A}$ , 66  $\mu\text{A}$  in the differential pair and 71  $\mu\text{A}$  in each of the other branches (M10 and M12; M11 and M13).

TABLE I  
DEVICE DIMENSIONS OF THE OPERATIONAL AMPLIFIER

Device	Width	Length
M6, M7	20 $\mu\text{m}$	1 $\mu\text{m}$
M8, M9	6 $\mu\text{m}$	1 $\mu\text{m}$
M10, M11	12 $\mu\text{m}$	1 $\mu\text{m}$
M12, M13	10 $\mu\text{m}$	1 $\mu\text{m}$
M14, M15	40 $\mu\text{m}$	1 $\mu\text{m}$

### B. Output Stage

The output stage is composed of the transistors M1, M2, M3, M4 and the resistor R3. The main purpose of the output stage is maintaining the  $V_{LO}$  node at 45 V, thanks to the  $V_{G3}$  controlled by the operational amplifier. All of them are high voltage (HV) components due to the voltages present in this part of the system. The transistor M3 has a different maximum gate-source voltage ( $V_{gs-\max}$ ) from all the other transistors, due to voltage levels of the operational amplifier. The  $V_{gs3-\max}$  is 2 V, while all the other transistors have a  $V_{gs-\max}$  of 5.5 V.

The transistors M1 and M3 convert the 1.8 V level output from the operational amplifier to an HV voltage level, needed in the M2 gate. The M2 transistor's main purpose is controlling the voltage in the  $V_{LO}$  node. The transistor adjusts its current ( $I_{d2}$ ) due to voltage variations in the  $V_{LO}$  node: more  $I_{d2}$  if  $V_{LO}$  is higher than 45 V and vice versa.

Other approaches have been made to the level shifter composed by the transistors M1, M3; like having a resistor instead

of M1. The final solution using two transistors uses more power than the resistor variant, but has a better performance, in terms of undershoot and settling time of the voltage in  $V_{LO}$  node. However, this part of the system is only on 1/266 of the total period of the operation [1]. Consequently, the performance of the system is more important than the higher power used by this approach.

TABLE II  
DEVICE DIMENSIONS OF THE OUTPUT STAGE

Device	Width	Length
M1	60 $\mu\text{m}$	600 nm
M2	2000 $\mu\text{m}$	600 nm
M3	50 $\mu\text{m}$	200 nm
M4	250 $\mu\text{m}$	400 nm

### C. Current sinking circuit

The current sinking circuit is composed of the transistors M5 and Q1, and the resistor R4. This block sinks the major part of the current coming from the load. The capability of this block to sink the current affects directly the SR of the ultrasound transducer in its rising edge of the driving signal waveform.

The working principle is the activation of the bipolar transistor Q1, which is only needed to conduct in the rising edge of the exciting waveform for the transducer. During this rising edge, the  $V_{LO}$  node receives the most charge. M2 starts sinking current to keep the  $V_{LO}$  node at 45 V and the current in that branch is mirrored by the current mirror M4, M5 (M5 is 8 times bigger than M4). The sinking of current, in the branch composed by M5 and R4, activates Q1 in conduction mode when the base terminal voltage of Q1 is lower than  $V_{LO}$ .

R4 can be adjusted for a bigger current sinking capability, but it can make the system unstable. Trimming is needed for the resistors, as each corner needs a different value of resistance. However, for the test chip it has been decided to put off chip resistors. Nevertheless, in the final circuit the resistors will be trimmed on-chip.

TABLE III  
DEVICE DIMENSIONS OF THE CURRENT SINKING CIRCUIT

Device	Width	Length
M4	250 $\mu\text{m}$	400 nm
M5	1000 $\mu\text{m}$	400 nm
Q1	15 $\mu\text{m}$	60 $\mu\text{m}$

### D. Resistors

The resistors in this design are HV components with an important responsibility. The resistors R1, R2 and R3 set the voltage of the  $V_{LO}$  node. The resistor R4 controls the current sinking starting point.

TABLE IV  
RESISTORS IN THE DESIGN

Device	Width
R1	182.5 k $\Omega$
R2	3.7 k $\Omega$
R3	20.7 k $\Omega$
R4	300 $\Omega$

### E. Complete system

The layout of the presented design occupies a space of 470  $\mu\text{m}$  x 220  $\mu\text{m}$ , excluding the pads. The major part of the area is occupied by the resistors and the HV transistors including the guard rings. The design has been sent to fabrication to perform measurements in the integrated circuit.

In the Fig.5 the different components can be seen with the naming used in the Fig.3. Number 1 refers to the OTA, number 2 refers to R2, number 3 refers to M3 and number 4 refers to M1.

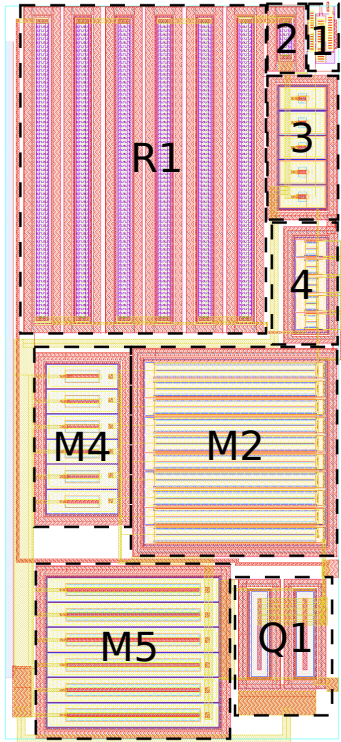


Fig. 5. Layout of the design in high-voltage 0.18  $\mu\text{m}$  technology.

## IV. SIMULATION RESULTS

It is possible to see in the Fig.7 that the performance is within the specifications, when the transducer is producing the desired driving signal waveform with a 5 MHz frequency and a 50 V amplitude. The SR in the ultrasound transducer with the pulse-triggered level shifter imported from [1], is 2.01 V/ns. The minimum voltage in the  $V_{LO}$  node is 44.66 V, thus

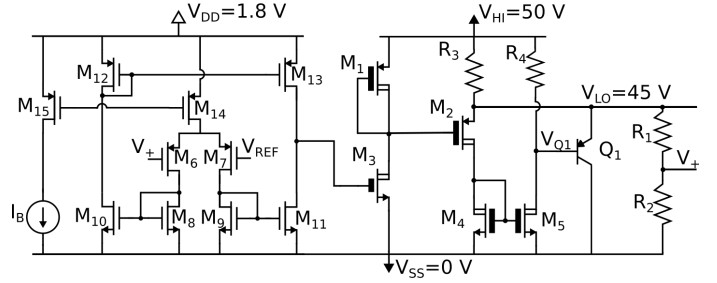


Fig. 6. Complete schematic of the linear regulator.

the system is compatible with the pulse-triggered level shifter regarding voltage level.

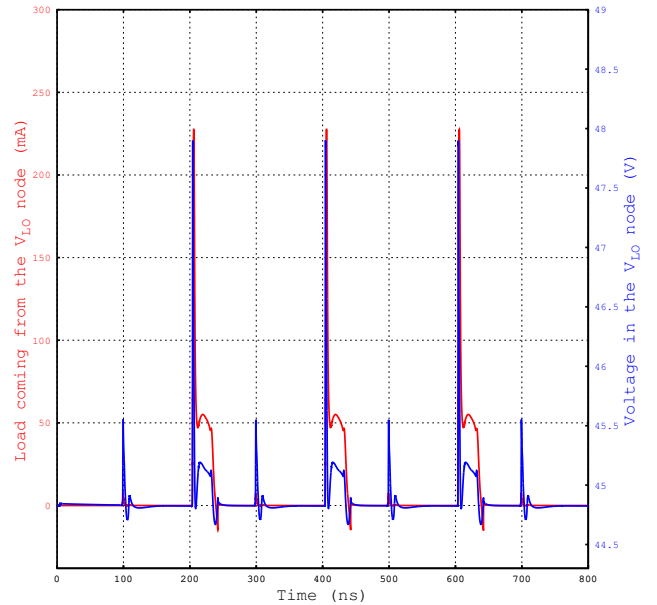


Fig. 7. Voltage and current in the  $V_{LO}$  node, when the ultrasound transducer is supplied with an driving signal waveform of 5 MHz of frequency, 50 V of amplitude and 2 V/ns of SR.

The system is totally configurable thanks to the off-chip components (R3, R4) and the control of the voltage in the  $V_{REF}$  pin. The R3 value and the  $V_{REF}$  voltage change the mean of the voltage in the  $V_{LO}$  node, and the R4 helps to provide more current sinking capabilities to the system. With the variation of these parameters it is possible to fulfil the specifications in all the corners.

In the cycle of Tx process and Rx process, the average current used in the whole period in the HV part is 287.74  $\mu\text{A}$ ; whereas in the LV part the average current is 199.56  $\mu\text{A}$  only in the Tx process.

## V. DISCUSSION

In order to assess the quality of the design, a comparison with state of the art regulators is needed. The comparison is not including a SM regulator because it is using an external inductor, not meeting the integration requirement of the regulator. A circuit based in TL431 [6] is a similar regulator to the device proposed, because linear regulators are normally designed to source current. However the TL431 can only regulate up to 36 V, and a maximum 100 mA of current sinking, so it would not resist the current peak during the rising edge of the voltage in the ultrasound transducer. The system designed uses only 1 bipolar transistor, far from the 13 of the TL431.

Additionally, the TL431 is capable of regulating with minimum current of 400  $\mu\text{A}$ , while the design presented has an average current consumption of 287  $\mu\text{A}$  during a period of normal operation.

TABLE V  
COMPARISON OF THE SPECIFICATIONS BETWEEN THIS WORK AND A  
TL431 BASED CIRCUIT

Specification	This work	TL431 based circuit
Vout [V]	45	36
Iout avg [ $\mu\text{A}$ ]	287	407
Vout undershoot [mV]	340	120
Bipolar transistors	1	13

The Table V has been filled with simulation results of this design and a TL431 based circuit. The only difference is the output voltage in the  $V_{LO}$  node, all the other parameters are the same.

Those parameters lead to the conclusion that the proposed design is the only suitable option for the application of driving the pulse-triggered level shifters.

## VI. CONCLUSION

The new topology for linear regulators with current sinking capabilities has been designed, simulated and integrated in 0.18  $\mu\text{m}$  technology. The linear regulator can sink currents up to 100 mA. The pulse-triggered level shifters for driving the transducers of ultrasound devices are able to perform perfectly when they are supplied in the low rail  $V_{LO}$  node with this regulator: producing a  $\text{SR} = 2 \text{ V/ns}$  in the driving signal waveform of the transducer. The undershoot voltage in the output is 340 mV using an average current of 287  $\mu\text{A}$ . The integration in high-voltage 0.18  $\mu\text{m}$  technology within an area of 0.11  $\text{mm}^2$  and the possibility to regulate without external components make this linear regulator a suitable option for supplying the low rail of the pulse-triggered level shifters.

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