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Comparison of Bipolar Sub-Modules for the Alternate Arm Converter

Harith R. Wickramasinghe[(1)], Georgios Konstantinou[(1)], Josep Pou[(1)(2)], Ricard Picas[(3)],
Salvador Ceballos[(4)], and Vassilios G. Agelidis[(1)(5)]

[(1)]UNSW Australia, Sydney, NSW 2052, Australia, [(2)]Nanyang Technological University, Singapore,
[(3)]Technical University of Catalonia, Spain, [(4)]Tecnalia Energy, Spain, [(5)]Technical University of Denmark, Denmark.
email: harith@student.unsw.edu.au.

Abstract—Research on dc-fault tolerant multilevel converters has gained noticeable attention over recent years. The alternate arm converter (AAC) is one of such emerging multilevel converter topologies, and a hybrid topology of the two-level converter and the modular multilevel converter (MMC). Bipolar submodules (SMs) that can produce both positive and negative voltages are the building blocks of the AAC. This paper analyses the operation of an AAC with the full-bridge SM (FB-SM) and the cross-connected SM (CC-SM). The conduction and switching losses of the two SM configurations are evaluated and compared, in order to identify the suitability of CC-SM for AACs and its performance compared to the FB-SM. The CC-SM with identical semiconductor devices has reduced losses compared to the CC-SM with higher rated devices in the cross-connected path. It is concluded that the CC-SM does not offer advantages in the losses, construction, and application to the AAC, compared to FB-SM.

Index Terms—Alternate arm converter, cross-connected sub-modules, losses, identical semiconductor devices.

Fig. 1. MMC vs AAC; (a) MMC phase-leg and (b) AAC phase-leg.

I. INTRODUCTION

The modular multilevel converter (MMC) has become one of the leading topologies in high-voltage direct current (HVDC) systems and medium voltage applications since its first introduction [1]–[3]. Modularity, scalability, simplicity of submodule (SM) capacitor voltage balancing, and redundant configuration [4] are the salient features of the MMC, which provide near sinusoidal output voltages and currents with low harmonic distortion owing to the large number of voltage levels.

The MMC topology in Fig. 1(a), consists of N series-connected SMs per arm, and two inductors (L) connecting the two arms to form one phase-leg. By inserting or bypassing the N SMs in each arm (upper and lower) depending on the modulation waveform, the arms behave as controllable voltage sources. Various types of modulation techniques are applicable [3], [5], [6] in order to determine the number of SMs to be inserted, while the staircase type modulation methods are more efficient over the alternative techniques as the number of output voltage levels increases [7]. Different capacitor voltage balancing strategies [8], [9] are used and the SM sorting algorithms are the most common. Circulating current control is important for the MMC in order to regulate the capacitor voltages, maintain upper and lower arm energy balance, and efficiently utilize semiconductor ratings. Two major categories
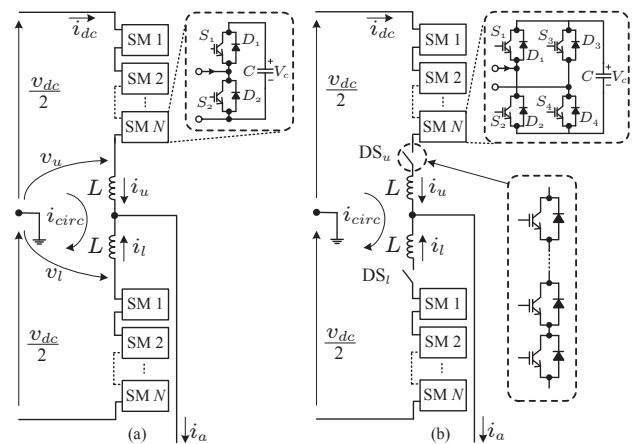
of circulating current control techniques based on double-frequency synchronous reference frame [10], and proportional-resonant controllers [11], [12] are reported in the existing literature.

One of the main drawbacks of MMCs with unipolar SMs is the lack of dc-fault handling capability. Bipolar SMs used in MMCs can offer voltage blocking during dc-faults. Availability of such diverse SM configurations [13], [14], provide additional functionalities and dc-fault tolerant MMCs can be developed at the cost of more semiconductor devices and increased losses.

The alternate arm converter (AAC) [15], shown in Fig. 1(b), offers dc-fault blocking capability with full-bridge SMs (FB-SMs) which are capable of providing the blocking voltage for dc-faults [16]. The AAC has a similar structure to the MMC except the director switches (DSs) located in the upper and lower arms as shown in Fig. 1(b). The AAC topology can push the ac voltages above the peak dc-link voltage up to a maximum ac peak voltage of $4/\pi$ times the dc-link voltage, which is called the "sweet-spot" [15]. At the "sweet-spot" operation, the net energy exchanged within an arm is zero while nonsweet-spot operation causes nonzero net power exchange leading to deviations of SM capacitor voltages. Overlap period based control techniques [17], [18], and zero-sequence voltage injection [19] can be utilized to

achieve SM capacitor voltage regulation and upper/lower arm energy balancing.

As the AACs share some traits with MMCs in terms of topology, and SM capacitor sorting and balancing [8], [16], different SM structures available for MMCs can be adopted to AACs. Reviews of MMC SM configurations analysing the component count, complexity, and the voltage balancing characteristics, can be found in [13], [14]. MMC SMs can be categorized based on the capability of generating negative voltage levels in the output. Unipolar SMs generate only positive voltage levels and bipolar configurations generate both positive/negative voltage levels [13]. Alternative to the FB-SM, only the cross-connected SM (CC-SM) is applicable to AACs, as it offers the bipolar operation with full controllability [13].

These two SMs offer their own advantages and drawbacks in terms of simplicity, modularity, device count, and effort of capacitor voltage balancing. A generalized SM structure based on the CC-SM has been proposed for AACs in [20] with nonidentical switching devices, while reducing the device count compared to FB-SM-based AAC. Losses in an AAC based on CC-SMs with identical switching devices are yet to be investigated contrary to the FB-SM-based AAC. Hence, the objective of this paper is to study the operational losses of the CC-SM-based AAC over the FB-SM-based AAC, and to identify the effect of nonidentical switching devices on the losses in CC-SM. The study includes the adaptation of a restricted voltage balancing algorithm in order to balance the capacitor voltages in FB-SM- and CC-SM-based AACs.

The paper is organized in the following manner. Section II provides a brief overview of the basic principals of AAC operation, and a summary of suitable SMs for the AAC topology is presented in Section III. Simulation results of FB-SM- and CC-SM-based AACs are demonstrated in Section IV. Section V evaluates the losses in CC-SM and FB-SM-based AACs at different power factors, where the impact of identical and nonidentical switching devices on the losses in CC-SM is deduced. Section VI summarizes the conclusions of the work.

II. AAC OPERATING PRINCIPLES

The single-phase AAC topology (Fig. 1(b)) consists of N series-connected SMs with one inductor (L) and a DS per arm, forming two arms per phase-leg of the converter and utilising a single dc-source for the three-phase topology. The SM, which is the basic building block of the AAC, is based on multilevel-bipolar configurations; the most commonly used configuration is the FB-SM.

The AAC topology has a similar structure to MMC (Fig. 1(a)) except the DSs in upper and lower arms (DS$_u$ and DS$_l$). DS$_u$ and DS$_l$ operate alternatively during the positive and negative half cycles of the output reference voltage $v_{am} = m_a \cos(\omega t)$, respectively. Hence, within a half cycle, only one arm carries the output current $i_a = \hat{I}_a \cos(\omega t + \phi)$.

An overlap period that is evenly distributed besides the zero-crossing points of v_{am}, can be defined in order to exchange energy between upper and lower arms as well as to balance the SM capacitor voltages. During the overlap period, a circulating

current i_{circ} flows within the phase-leg. Thus, the upper and lower arm currents (i_u and i_l) during the overlap period are given by:

$$i_u = \frac{i_a}{2} + i_{circ}, \qquad \text{and} \qquad i_l = \frac{i_a}{2} - i_{circ}, \qquad (1)$$

which are similar to MMC operation.

Unlike the MMC, the energy balancing of the AAC is limited due to the short overlap period at which, energy between the arms can be exchanged. This limitation can be addressed by utilizing a longer overlap period while the circulating current is controlled appropriately in order to regulate the energy exchange among SM capacitors [17]. However, longer overlap periods can lead to output voltage distortions. In order to operate with a longer overlap period avoiding such distortions, SM voltages in the upper and lower arms should be sufficient enough to synthesize the output voltage well-below and above zero, respectively. In MMCs, the average SM voltage V_C is chosen as: V_{dc}/N, where the each upper/lower arm is capable of synthesizing the full cycle of the output voltage. However, N of an AAC is chosen in order to provide the capability to block the ac-peak voltage, depending on the rated SM capacitor voltage V_C. Assuming the grid side peak ac voltage is $\hat{V}_a$, the number of SMs per arm of an AAC can be determined as:

$$N = \left\lceil \frac{\hat{V}_a}{V_C} \right\rceil. \qquad (2)$$

The maximum applicable overlap duration which avoids additional output voltage distortions is limited by the redundant voltage (V_r),

$$V_r = NV_C - \frac{V_{dc}}{2}. \qquad (3)$$

Redundant SMs can purposely be included in order to achieve higher flexibility to control energy within a phase-leg [4].

Due to the large number of SMs in the AAC arms, SM sorting algorithms are required in order to keep the voltage balance among the SMs. Even though such techniques are applied, the total energy within the arms should be maintained close to the rated value for satisfactory operation of the converter [15]. To achieve this, the net energy absorbed by the SMs of an arm during each half cycle needs to be kept at zero. Assuming that all SM capacitor voltages are balanced, and a lossless converter, the net energy of the arm capacitors within a half cycle can be determined as the difference between dc-link energy and the energy exchanged by the arm current.

Defining the ac voltage produced at the converter output as:

$$v_a = v_{am}\frac{V_{dc}}{2} = m_a\frac{V_{dc}}{2}\cos(\omega t), \qquad (4)$$

and considering that the arm current and phase current are similar during a half-cycle, the exchanged energy in the dc-link E_{dc} and the SMs E_{ac} can be given using i_a and (4) as:

$$E_{dc} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \frac{V_{dc}\hat{I}_a}{2}\cos(\omega t + \phi)\, dt, \qquad (5)$$

$$E_{ac} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \frac{m_a V_{dc} \hat{I}_a}{2} \cos(\omega t) \cos(\omega t + \phi) \, dt. \qquad (6)$$

Hence, from (5) and (6), the net energy in the arm capacitors can be determined as:

$$E_{dc} - E_{ac} = \frac{\pi V_{dc} \hat{I}_a \cos \phi}{4\omega} \left(\frac{4}{\pi} - m_a \right) \qquad (7)$$

Eq. (7) describes that, energy balance can only be achieved at one operating point ($m_a = 4/\pi$), without additional controllers. This operating point is called "sweet-spot" [15]. It should be noted that, the energy balancing control becomes relatively easy when the converter operates near the sweet-spot due to the low excessive energy at the SMs.

III. SUB-MODULE CONFIGURATIONS

The common traits of MMC and AAC topologies allow the use of MMC SMs in AACs, and capacitor voltage balancing of AACs can be achieved by accommodating similar methods as in MMCs [8], [16]. Unlike in MMCs, AACs require SMs which can generate both positive and negative voltage levels, in order to push the output voltage above the dc-link voltage during normal operation. These include the commonly used FB-SM as well as the CC-SM [13], [14]. The characteristics of each SM are briefly described here.

1) FB-SM: The FB-SM (Fig. 2(a)) has the simplest structure where one leg operates as a half-bridge SM (HB-SM) and the other leg operates in a single state depending on the required output voltage polarity. Due to the single capacitor configuration, capacitor voltage balancing can be accomplished by using 'sort and select' approaches similarly to the HB-SMs. Two semiconductor devices are always present in the conduction path which leads to higher losses.

2) CC-SM: The CC-SM (Fig. 2(b)) consists of two HB-SMs connected on the dc side using cross switches (S_3, S_4). Owing to the cross-connection, the CC-SM can generate a symmetrical bipolar multilevel voltage waveform at the output. The voltage ratings of the cross switches need to be at least twice the voltage rating of S_1, S_2, S_5, and S_6 (V_C), in order to withstand the total of two capacitor voltages ($2V_C$).

The component count depends on the ratings of semiconductor devices used to configure the cross-connections. Each cross-connection can be configured either with two series-connected devices which have the voltage rating V_C, or with one device rated at $2V_C$ [20]. The former ensures device-level modularity of the CC-SM but with higher device count. The latter leads to an asymmetric CC-SM structure with a relatively low device count but at the cost of a less-modular structure. Total losses of the modular-structure-based AAC can be comparatively lower with respect to the asymmetric-structure-based AAC, especially as the number of levels increases. In general, the high device count, and the semiconductor ratings of the cross switches add to the complexity of the SM. The losses depend on the semiconductor device count, and as well as the device ratings. These aspects of operation will be analyzed in the following section and compared against the FB-SM.
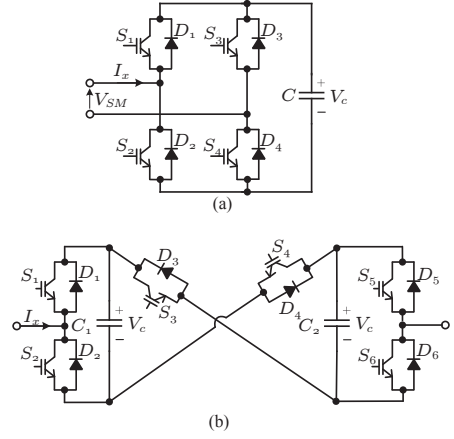

Fig. 2. SM configurations; (a) FB-SM and (b) CC-SM.

IV. STEADY-STATE SIMULATION RESULTS

In order to evaluate the operational losses in FB-SM-based and CC-SM-based AACs, three-phase grid-connected AAC models (17-level) are simulated in MATLAB-Simulink and PLECS. Since the CC-SM yields double levels, the FB-SM-based AAC and CC-SM-based AAC have $N = 8$ FB-SMs/arm and $N = 4$ CC-SMs/arm, respectively. The models are developed adopting the CIGRE benchmark MMC test system [21] for $N = 4$ and 8 SMs with 35 kV per SM capacitor. The stored energy of the AAC is limited to a third compared to the MMC with similar power ratings [22], which results in a SM capacitance of 150 μF. Fig. 1(b) shows the circuit configuration of one phase-leg of the simulated three phase system and modeling parameters are given in Table I. Phase-disposition PWM is adopted for the modulation of the AAC, and the restricted sorting algorithm of [8] is utilized for SM capacitor voltage balancing within the arms of both AACs, accordingly modifying the gate-pulse generation stage.

The rated power at the sweet-spot for unity power factor operation is 400 MW. In steady state, each AAC operates near the sweet-spot ($m_a = 1.26$) and the corresponding active

TABLE I
SIMULATION PARAMETERS OF THE GRID-CONNECTED AAC

Rated Power	400 MVA
Number of SMs/arm (N)	8 (FB-SM), 4 (CC-SM)
DC-Link Voltage (V_{dc})	400 ($\pm$200) kV
SM Capacitance (C)	150 μF
SM Capacitor Voltage (V_C)	35 kV
Arm Inductance (L)	0.019 pu
Transformer Leakage Inductance	0.045 pu
Transformer Resistance	0.0015 pu
Transformer Ratio	1.218
Grid Voltage (for $m_a = 4/\pi$)	380 kV
Carrier frequency (f_c)	7.2 kHz
System frequency (f)	50 Hz

Fig. 3. Simulation results of the FB-SM-based AAC for near sweet-spot operation; (a) output voltages and (b) output currents.

Fig. 4. Steady-state results of phase a of the FB-SM-based AAC for near sweet-spot operation; (a) upper arm capacitor voltages, (b) lower arm capacitor voltages, and (c) upper/lower arm currents.
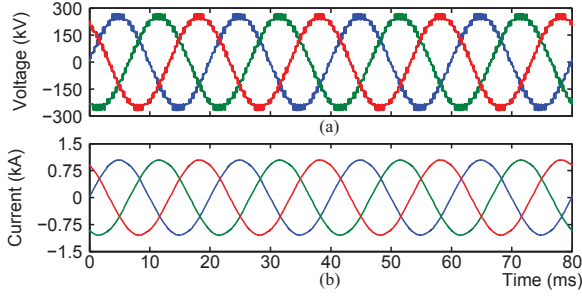

Fig. 5. Simulation results of the CC-SM-based AAC for near sweet-spot operation; (a) output voltages and (b) output currents.
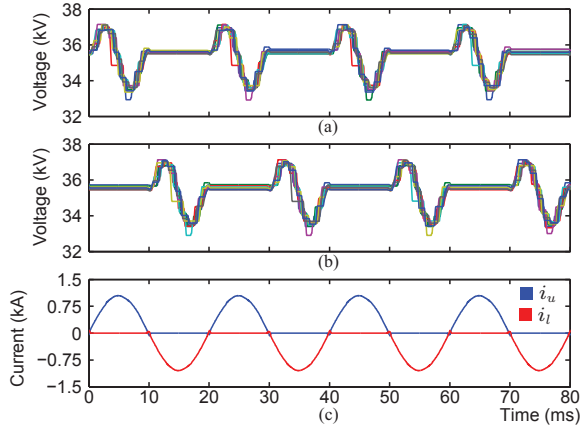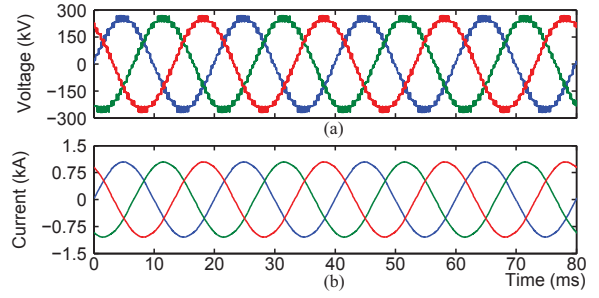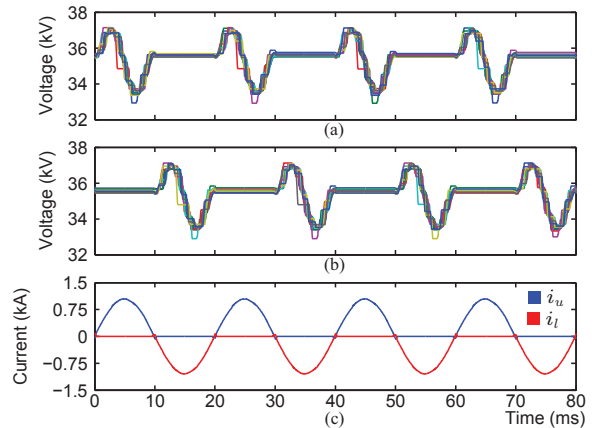

Fig. 6. Steady-state results of phase a of the CC-SM-based AAC for near sweet-spot operation; (a) upper arm capacitor voltages, (b) lower arm capacitor voltages, and (c) upper/lower arm currents.

power for near sweet-spot operation is 395.8 MW at unity power factor. The operating point is simulated by specifying the grid voltage depending on the desired modulation index. Neither the overlap period control nor circulating current control for capacitor voltage regulation are applied, in order to avoid the impact of additional controllers on the AAC operational losses. As the converter operates near the sweet-spot, no major influence due to the absence of these controllers is expected.

Fig. 3 shows the steady-state output voltage and current of the FB-SM-based AAC. The generated output voltages are 17-level waveforms. The steady-state upper/lower SM capacitor voltages and the arm currents of phase-leg a are shown in Figs. 4(a), (b), and (c), respectively. The balanced upper and lower arm capacitor voltages demonstrate the successful operation of the restricted sorting algorithm [8] for FB-SM in AAC topologies. It should be noted that the capacitors are slightly overcharged due to the absence of circulating current control. The capacitor voltages can be regulated to the rated value at the sweet-spot operation ($m_a = 4/\pi$), according to (7).

Fig. 5 shows the steady-state operation of CC-SM-based AAC. Fig. 5 represents the output voltage and the current similar to the output of FB-SM-based AAC shown in Fig. 3. Subsequently, Fig. 6 demonstrates the steady-state upper/lower SM capacitor voltages and the arm currents in phase-leg a

of the CC-SM-based AAC. The upper/lower SM capacitor voltages (Fig. 6 (a), (b)) convey that the adopted restricted-voltage balancing algorithm balances the capacitor voltages in the CC-SM-based AAC, similarly as in FB-SM-based AAC (Fig. 4(a), (b)).

The similarity between the steady-state simulation results of FB-SM-based and CC-SM-based AACs allow a valid comparison of the losses between the two AACs, under the same operating conditions. The loss evaluation of the two types of AACs are presented in Section V.

V. LOSS EVALUATION AND COMPARISON

Based on the description of Section III, CC-SM can be configured either with identical semiconductor devices or non-identical devices. In order to study the losses considering the identicalness of the devices, losses in FB-SM- and CC-SM-based AACs are compared while modeling the SMs using identical semiconductor devices, and the loss profiles of two distinct insulated-gate bipolar transistor (IGBT) and diode modules are analysed.

A. FB-SM-Based AAC Losses vs. CC-SM-Based AAC Losses

The FB-SM-based and CC-SM-based AAC models demonstrated in Section IV are simulated for loss analysis with PLECS thermal modeling. One SM in each upper and lower

#	Model No. (ABB)	V_{CE}	I_C	I_{Cmax}
1	5SNA 0750G650300	6.5 kV	750 A	1500 A
2	5SNA 0800N330100	3.3 kV	800 A	1600 A

arm of both AACs are modeled with loss characteristics of the IGBT Module-1 given in Table II. The voltage ratings of the switches at each position in FB-SM (Fig. 2(a)) and CC-SM (Fig. 2(c)) are defined by the nominal capacitor voltage (35 kV). Hence, the voltage rating of 35 kV is matched by connecting six IGBT modules (6.5 kV) in series.

Although ideal semiconductor devices are used for simulations, PLECS thermal model has the ability to calculate conduction losses and switching losses of the devices, based on the thermal descriptions provided by the manufacturers. Therefore, the device losses are not reflected in the voltage and current waveforms of the converter [23]. If the SM capacitor voltages are balanced within the arms, as shown in Section IV, losses in one SM represent the losses of all SMs within the arm. Hence, the average conduction and switching loss per SM in an AAC phase-leg can be calculated in terms of the instantaneous loss components of one upper-arm and one lower-arm SM.

Accordingly, the steady-state conduction and switching losses per FB-SM and per CC-SM are calculated while varying the power factor from 0.7-lagging to 0.7-leading. The required number of CC-SMs per arm is half the number of FB-SMs per arm, in order to generate similar multilevel output voltages. Hence, the calculated conduction and switching losses per two FB-SMs and per CC-SM at different power factors, are compared as shown in Figs. 7(a) and (b), respectively. The results show that the losses in the CC-SM-based AAC are almost similar to the FB-SM-based AAC, when the CC-SM is configured with identical semiconductor devices. However, if one device with twice the voltage rating as in half-bridge legs is used for each cross switch of the CC-SM, the losses in CC-SM-based AAC can be different from the results shown in Fig. 7. This is due to the loss characteristics not being proportional to the device ratings.

B. Impact of Nonidentical Devices on Losses in CC-SM

Two IGBT and diode modules manufactured by ABB (Table II) are considered in the following analysis. Module-1 has a voltage rating of 6.5 kV, and the Module-2 which is rated at 3.3 kV can be considered as a half-rated device compared to Module-1. The current ratings of both devices are also similar. Based on these two modules, CC-SM can be configured in three ways as; 1) CC-SM with identical 6.5 kV IGBT modules (8×6.5 kV devices), 2) CC-SM with identical 3.3 kV IGBT modules (8×3.3kV devices), and 3) CC-SM with mixed IGBT modules (4×3.3 kV devices and 2×6.5 kV devices).

The first configuration can have capacitor voltages up to 6.5 kV. The resultant CC-SM-based AAC generates a mul-
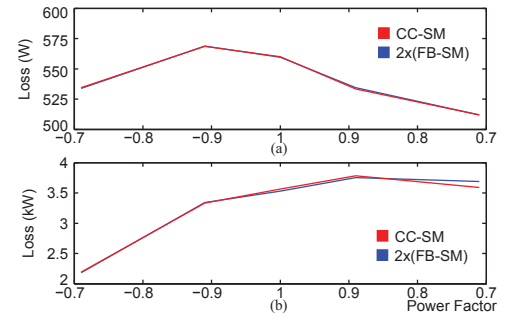

Fig. 7. Comparison of the losses per two FB-SMs with losses per one CC-SM of the AAC, operating at different power factors; (a) conduction loss, and (b) switching loss.
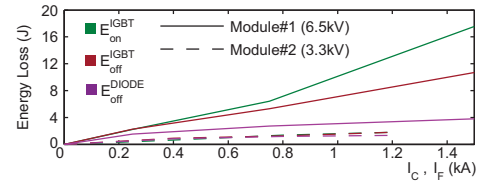

Fig. 8. Switching energy losses of IGBT and diode modules in Table II.

tilevel output voltage with less number of levels compared to other two configurations, for the same converter rating as less number of SMs are required. The second and third configurations have capacitor voltages up to 3.3 kV and the generated multilevel output voltages of both resultant CC-SM-based AACs are same in terms of the number of voltage levels. The conduction and switching losses in each configuration can be compared by analyzing the on-state/forward characteristics and switching energy loss profiles of the IGBT and the diode in each module.

Fig. 8 shows the switching energy losses of the IGBT and diode of each module given in Table II. The switching on/off losses of the IGBT with a higher voltage rating (6.5 kV) are several times (more than twice) the equivalent switching losses of the IGBT with lower voltage rating (3.3 kV). Moreover, the turn-off energy loss of the diode in Module-1 (6.5 kV) is slightly above twice the equivalent energy loss of the diode in Module-2 (3.3 kV). Although not shown here, the conduction losses of the IGBTs of two modules are approximately similar and the conduction loss of the diode in Module-1 is higher than individual but lower than twice the conduction loss of the diode in Module-2.

Based on the information of Fig. 8, CC-SM Configuration-1 has the highest switching loss and it is not comparable with other two configurations as the SM capacitor voltage ratings of the Configuration-1 are different from other two configurations. CC-SM Configuration-2 and 3 have the same capacitor voltage rating and the losses are comparable. The difference between the CC-SM Configuration-2 and 3 are the device count and the ratings of the cross switches. Although the device count is less in the CC-SM Configuration-3, switching losses are still higher than Configuration-2 due to the significantly high switching energy losses in the 6.5 kV
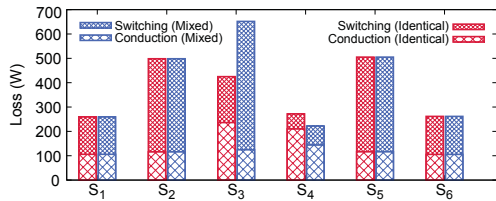
Fig. 9. Losses of CC-SM with identical and mixed IGBT modules by semiconductor device position.

IGBT and diode module as shown in Fig. 8. Additionally, the conduction losses of the CC-SM Configuration-3 can be lower than the Configuration-2 caused by the low device count.

Fig. 9 demonstrates the per SM losses at each switch position of the CC-SM Configuration-2 and 3 for unity power factor operation of AAC. The voltage rating at each switch position (Fig. 2(c)) of both Configuration-2 and 3 is matched by series-connecting the relevant IGBT modules. Switching losses are increased and the conduction losses are reduced at the cross-connections (S_3 and S_4) of CC-SM Configuration-3. Overall SM loss of Configuration-3 is higher than the Configuration-2, due to the significant increment of switching losses at S_3 regardless of the reduced total loss at S_4. The switching energy losses are dominantly increased compared to the conduction losses when the voltage rating of the semiconductor device becomes higher. Hence, the CC-SM with identical devices is a better choice over the mixed device configuration.

VI. Conclusion

The AAC is an alternative dc-fault tolerant topology. Multiple bipolar SMs available for MMCs can be used for AACs. In this paper a loss analysis of FB-SM-based AACs and CC-SM-based AACs are presented. Two AAC models are developed in MATLAB-Simulink and PLECS including thermal modeling of the two SM types. The steady-state results of the two AAC models demonstrate the successful operation of restricted voltage balancing algorithm for different SM configurations.

Analysis and loss comparison for the CC-SM does not signify any advantage over the FB-SM-based AAC. Further loss analysis of CC-SM with identical and nonidentical semiconductor devices shows that, the switching losses are dramatically increased regardless of the conduction losses (hence the total loss) when the higher rated devices are used for cross-connections, adding to the complexity. Conclusively, unlike for the MMC, the CC-SM is not a better alternative for the AAC as they do not offer advantages in terms of the losses, complexity, and application in contrast to the FB-SM-based AAC.

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