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## ARTICLE OPEN

Reversible hysteresis inversion in MoS<sub>2</sub> field effect transistorsNaveen Kaushik<sup>1</sup>, David M. A. Mackenzie<sup>2</sup>, Kartikey Thakar<sup>1</sup>, Natasha Goyal<sup>1</sup>, Bablu Mukherjee<sup>1</sup>, Peter Boggild<sup>2</sup>, Dirch Hjorth Petersen<sup>2</sup> and Saurabh Lodha<sup>1</sup>

The origin of threshold voltage instability with gate voltage in MoS<sub>2</sub> transistors is poorly understood but critical for device reliability and performance. Reversibility of the temperature dependence of hysteresis and its inversion with temperature in MoS<sub>2</sub> transistors has not been demonstrated. In this work, we delineate two independent mechanisms responsible for thermally assisted hysteresis inversion in gate transfer characteristics of contact resistance-independent multilayer MoS<sub>2</sub> transistors. Variable temperature hysteresis measurements were performed on gated four-terminal van der Pauw and two-terminal devices of MoS<sub>2</sub> on SiO<sub>2</sub>. Additional hysteresis measurements on suspended (~100 nm air gap between MoS<sub>2</sub> and SiO<sub>2</sub>) transistors and under different ambient conditions (vacuum/nitrogen) were used to further isolate the mechanisms. Clockwise hysteresis at room temperature (300 K) that decreases with increasing temperature is shown to result from intrinsic defects/traps in MoS<sub>2</sub>. At higher temperatures a second, independent mechanism of charge trapping and de-trapping between the oxide and p<sup>+</sup> Si gate leads to hysteresis collapse at ~350 K and anti-clockwise hysteresis (inversion) for temperatures >350 K. The intrinsic-oxide trap model has been corroborated through device simulations. Further, pulsed current–voltage (*I*–*V*) measurements were carried out to extract the trap time constants at different temperatures. Non-volatile memory and temperature sensor applications exploiting temperature dependent hysteresis inversion and its reversibility in MoS<sub>2</sub> transistors have also been demonstrated.

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## INTRODUCTION

Among two-dimensional materials, graphene<sup>1,2</sup> was the first to be isolated and studied with respect to electronic applications. Due to lack of an energy bandgap in graphene, other 2D materials such as layered transition metal dichalcogenides (TMDs) comprising a wide selection of materials with different bandstructures, and therefore different electrical and optical properties, have garnered significant attention.<sup>3–5</sup> Molybdenum disulfide (MoS<sub>2</sub>) has emerged as a prospective candidate for transistor applications. The presence of a direct bandgap (~1.8 eV) in monolayer form and an indirect bandgap (~1.2 eV) in multilayer MoS<sub>2</sub> makes it a promising channel material for field effect transistors (FETs).<sup>6</sup> High *I*<sub>ON</sub>/*I*<sub>OFF</sub> ratio (>10<sup>6</sup>), low sub-threshold swing, absence of dangling bonds, negligible OFF current and high effective mass (to reduce short channel effects) are some of the key advantages reported for MoS<sub>2</sub> transistors in various studies.<sup>7–9</sup> Other than logic applications, MoS<sub>2</sub> is also being actively researched for use in display technology, optoelectronics, memories and energy harvesting.<sup>10</sup>

Reliability and performance of MoS<sub>2</sub> transistor devices used in these various applications are highly dependent on the measure of threshold voltage instability with changing gate voltage (*V*<sub>GS</sub>) sweep directions.<sup>11–14</sup> The occurrence of hysteresis screens out intrinsic properties of MoS<sub>2</sub> and limits its potential in realizing expected device performance.<sup>15</sup> Comparison of previous reports on hysteresis in MoS<sub>2</sub> devices with this work is listed in Table 1. Hysteresis observed in previous studies<sup>16–18</sup> has been attributed to several possibilities such as adsorption of water molecules,<sup>18–21</sup> oxide traps close to MoS<sub>2</sub>,<sup>22</sup> oxide–MoS<sub>2</sub> interface traps<sup>23,24</sup> and

gate voltage stress effects.<sup>25</sup> A lack of uniformity in the hysteresis data and consensus on its origin among the reports listed in Table 1 results, at least partly, from differences in measurement conditions as well as device architecture. Impact of temperature, temperature-dependent contact resistance, ambient conditions, sweep rate, ON pulse width (drain/gate) and presence of interface and oxide traps through dielectric proximity to MoS<sub>2</sub> (suspended vs. supported devices) are critical to the understanding of hysteresis in MoS<sub>2</sub> devices. As can be seen in Table 1, some of these aspects have not been looked at in detail in previous reports. Further, reversibility of hysteresis inversion (clockwise to anti-clockwise) with temperature in MoS<sub>2</sub> transistors has not yet been demonstrated.

This work reports a comprehensive study that isolates and identifies the contributions of two different and independent mechanisms to hysteresis in multilayer MoS<sub>2</sub> FETs. We demonstrate, for the first time, temperature dependent reversible hysteresis inversion (from clockwise (CW) at 300 K to anti-clockwise (ACW) for >350 K) in four-terminal contact resistance-independent, MoS<sub>2</sub> van der Pauw (vdP) devices. VdP correction allows to compensate for the errors that might occur in hysteresis analysis due to arbitrarily shaped MoS<sub>2</sub> flakes.<sup>26,27</sup> Effect of contact resistance on hysteresis was also studied by comparing two-terminal and four-terminal gated devices (Fig. S6 in Supplementary Information). Almost similar magnitude of hysteresis, in both two and four-terminal MoS<sub>2</sub> devices indicates that the contact resistance has negligible impact on hysteresis. Further, similar evolution of hysteresis with temperature in two and four-terminal MoS<sub>2</sub> devices indicates that the contact resistance does not change significantly with temperature. Thermally assisted

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**Table 1.** Hysteresis properties and mechanisms in MoS<sub>2</sub> transistors reported previously and in this work

Ref. no.	Device type		Hysteresis properties		Hysteresis mechanism		
	Layer	Device type	Type	Inversion and reversibility	Temperature dependence	R <sub>C</sub>	
18, 19	Mono	Supported	CW	No	NA	With	Adsorbates
34, 35	Mono	Supported	ACW	No	NA	With	Mobile ions
25	Multi	Supported + Suspended	CW	No	NA	With	V <sub>GS</sub> stress/intrinsic
23, 24, 42	Multi	Supported	CW	No	NA	With	Interface traps
22	Multi	Supported	CW	No	NA	With	Oxide traps close to MoS <sub>2</sub>
29	Mono	Supported	ACW	No	Yes	With	Oxide traps close to p+ Si
This work	Multi	Supported	CW + ACW	Yes	Yes	Without	Intrinsic + oxide traps
		Suspended	CW	NA	Yes	With	Intrinsic traps

CW and ACW are acronyms for clockwise and anti-clockwise hysteresis, respectively

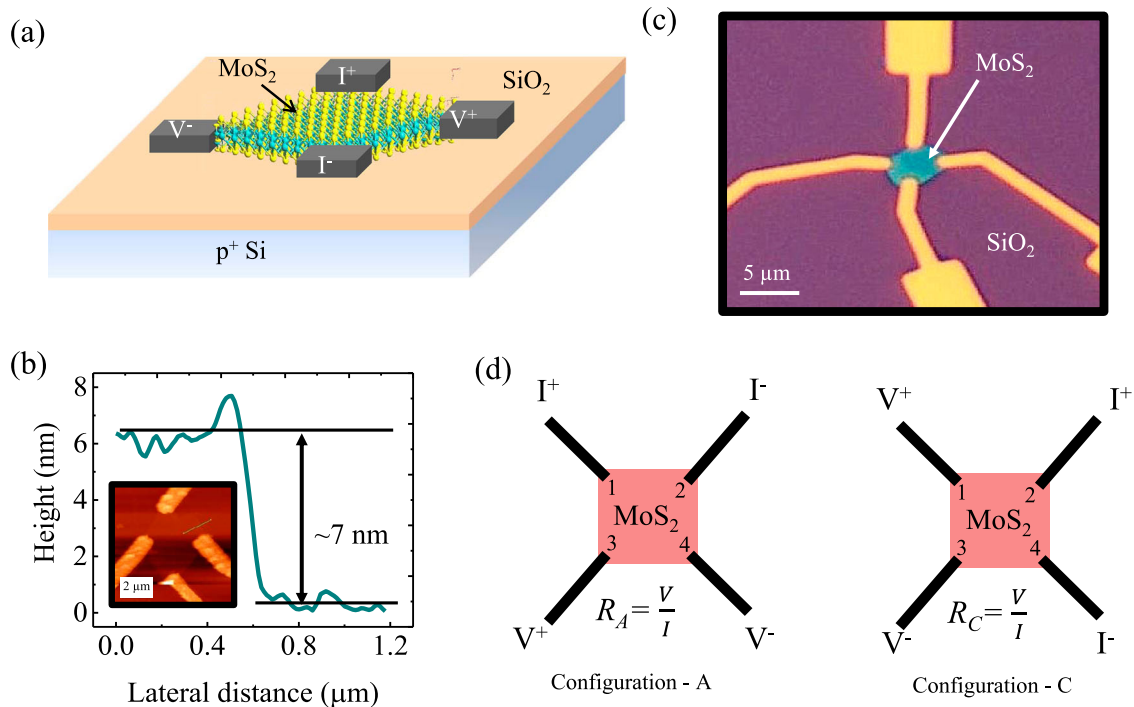
hysteresis inversion requires hysteresis crossover at a critical temperature that is shown to vary with the maximum applied gate voltage. Measurements were carried out at different temperatures, ambient conditions as well as in both supported and suspended transistor configurations to examine the effect of traps and adsorbates on hysteresis in the MoS<sub>2</sub> FETs. Analysis of the hysteresis data reveals that two different mechanisms are at play, one involving intrinsic defects/traps native to MoS<sub>2</sub> (i.e. atomic interlayer and intralayer point defects—for e.g. molybdenum and/or sulfur vacancies<sup>28</sup>) at room temperature, and the second due to extrinsic charge exchange between SiO<sub>2</sub> and p<sup>+</sup> Si gate at higher temperatures (>350 K).<sup>29</sup> Trap time constants at different temperatures were extracted using pulsed *I*-*V* measurements. Moreover, trap densities in MoS<sub>2</sub> and the gate oxide were extracted from the experimental data and used in simulations to reproduce the experimental inversion of hysteresis, thereby validating the intrinsic-oxide trap model.

Although hysteresis is usually seen as an obstacle for device applications, a recent work has shown that hysteresis can be exploited for thermally assisted non-volatile memory applications.<sup>29</sup> The requirement of high temperature (495 K)<sup>29</sup> to perform read and write operations is still a roadblock for the realization of fully functional heat-assisted memories. By exploiting hysteresis and its inversion, we have demonstrated thermally assisted programmable non-volatile memory at a much lower temperature (375 K) than previously reported.<sup>29</sup> Further, the variation in difference of forward (FS) and reverse sweep (RS) conductances over a wide temperature range of 100 K, as well as the reversibility of the hysteresis, can be harnessed for temperature sensing applications.

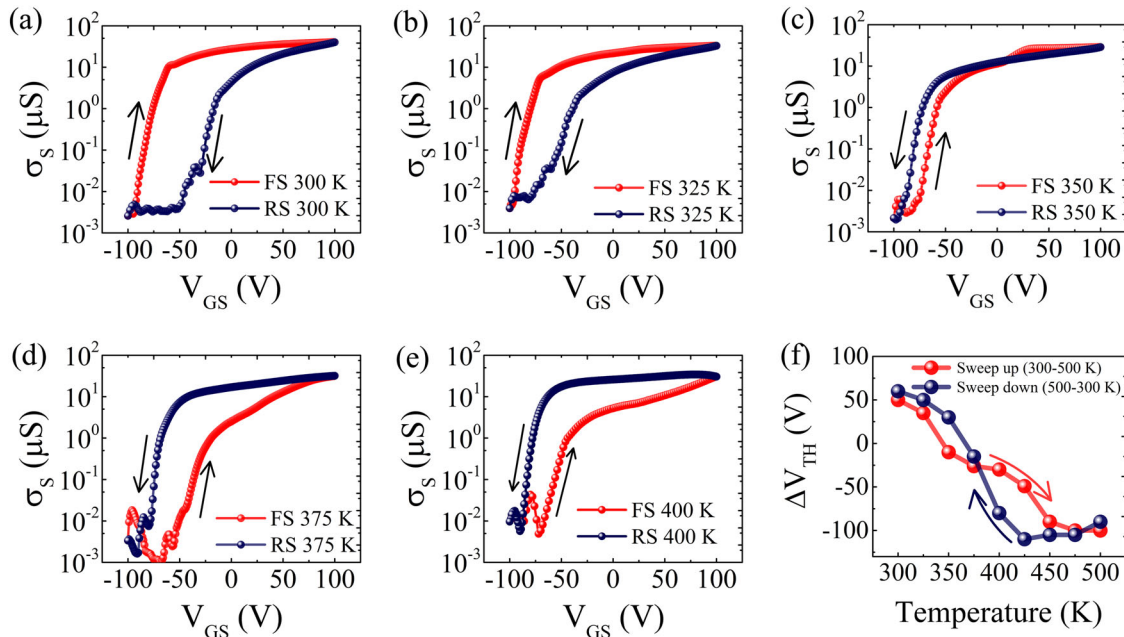
## RESULTS AND DISCUSSION

A schematic of back-gated MoS<sub>2</sub> vdP devices used in this work is shown in Fig. 1a. MoS<sub>2</sub> sheets were mechanically exfoliated<sup>1,5,6</sup> from MoS<sub>2</sub> crystal using adhesive tape on a heavily doped p-type silicon substrate with a 280 nm SiO<sub>2</sub> layer. MoS<sub>2</sub> flakes were then identified using an optical microscope. Further, the thickness and the number of layers were confirmed using Atomic Force Microscopy (AFM) and Raman spectroscopy. Figure 1b shows an AFM line scan across the MoS<sub>2</sub> flake, with the AFM image as inset. This was followed by patterning of source/drain contacts using electron beam lithography and metal deposition. Optical micrograph of a typical MoS<sub>2</sub> vdP device is shown in Fig. 1c. Contact resistance and its temperature dependence<sup>30</sup> can affect the magnitude of the hysteresis data as well as its evolution with temperature. At the same time it can screen out contributions to hysteresis from other mechanisms. Therefore, devices were fabricated in vdP configuration to eliminate the contact resistance using four-terminal measurements.<sup>31–33</sup> Fig. 1d shows the measurement schematics of the vdP MoS<sub>2</sub> device in A and C configurations. In A (C) configuration, current (*I*<sup>+</sup> = *I*<sup>−</sup>) is passed between terminals 1 and 2 (2 and 4) by applying a fixed set voltage of 1 V. The resulting potential drop (*V*<sup>+</sup> − *V*<sup>−</sup>) is measured between terminals 3 and 4 (1 and 3). More details on van der Pauw measurements are given in Supplementary Information S1. Sheet conductance ( $\sigma_s = \rho_s^{-1}$ ) was calculated using vdP equation,  $e^{-\frac{R_A}{\rho_s}} + e^{-\frac{R_C}{\rho_s}} = 1$ , where *R*<sub>A</sub> and *R*<sub>C</sub> are the resistances measured in configurations A and C, respectively<sup>26</sup> (shown in Fig. 1d).

Figure 2 shows transfer characteristics ( $\sigma_s$ -*V*<sub>GS</sub>) of a supported (on SiO<sub>2</sub>) multilayer MoS<sub>2</sub> vdP device at different temperatures. These measurements were done in nitrogen ambient. From the transfer characteristics, we estimate a field effect mobility ( $\mu_{FE}$ ) of ~16–80 cm<sup>2</sup>/Vs using  $\mu_{FE} = \frac{\partial \sigma_s}{\partial V_{GS}} \times \frac{1}{(C_{ox})}$ , where gate oxide capacitance per unit area  $C_{ox} = \epsilon_0 \epsilon_r / d$ ,  $\epsilon_r = 3.9$  and the oxide thickness, *d* = 280 nm.  $\Delta V_{TH}$  is the difference between RS (*V*<sub>GS</sub> = +100 to −100 V) and FS (*V*<sub>GS</sub> = −100 to +100 V) threshold voltages. Clockwise



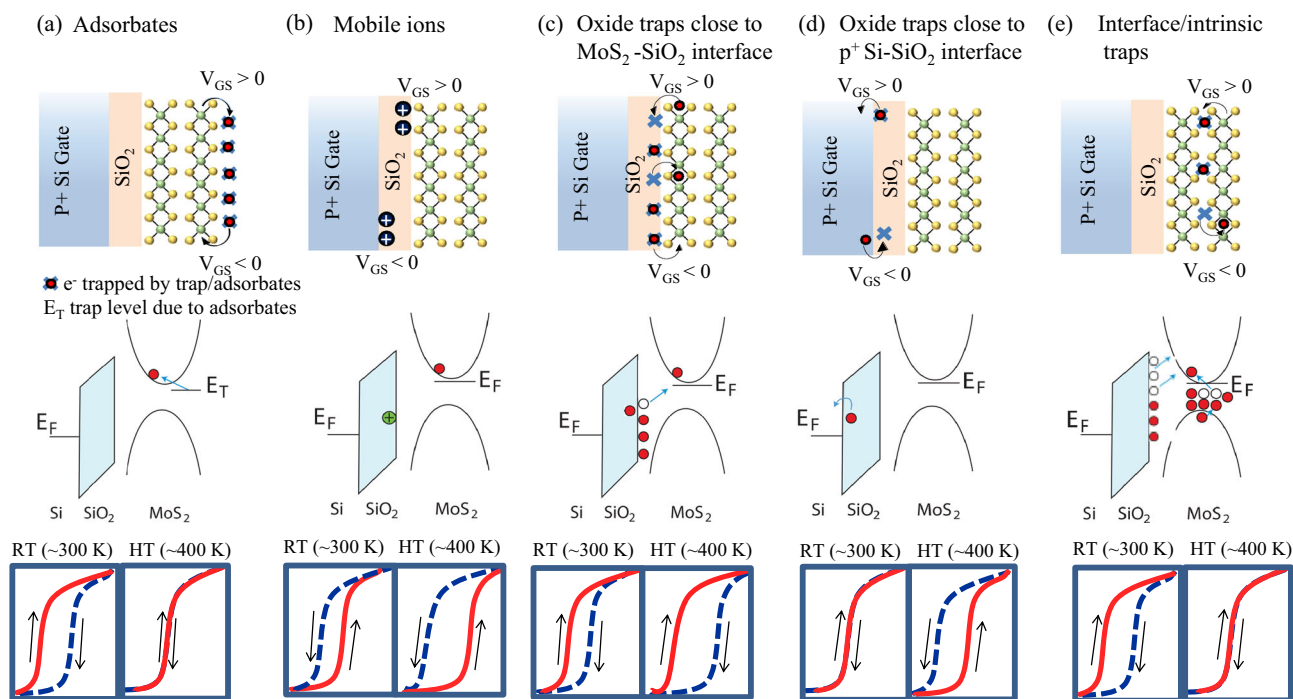
**Fig. 1** **a** 3D schematic of an MoS<sub>2</sub> FET in van der Pauw configuration. **b** AFM line scan (green line) across the edge of the MoS<sub>2</sub> flake shown in the inset. **c** Optical micrograph of a multilayer MoS<sub>2</sub> van der Pauw device. **d** Different van der Pauw configurations used to measure the sheet resistance ( $\rho_s$ ) for varying  $V_{GS}$



**Fig. 2** Transfer characteristics of a four-terminal MoS<sub>2</sub> vdP device for varying temperature (300–400 K), show **a** clockwise hysteresis at 300 K, **b** hysteresis reduction with increase in temperature, **c** nearly zero hysteresis at 350 K, and anti-clockwise hysteresis at **d** 375 K and **e** 400 K. **f** Experimentally extracted  $\Delta V_{TH}$  variation with increasing and decreasing temperature sweeps from 300–500 K shows reversible hysteresis inversion

hysteresis at 300 K (positive  $\Delta V_{TH}$ ) shown in Fig. 2a, reduces as the temperature increases to 325 K (Fig. 2b), and crosses zero at  $\sim 350$  K (shown in Fig. 2c). Further increase in temperature results in anti-clockwise hysteresis (negative  $\Delta V_{TH}$ ) as shown in Fig. 2d, indicating hysteresis inversion. The hysteresis direction (clockwise at room temperature<sup>18,22,23</sup> and anti-clockwise at high temperature<sup>29</sup>) is

the same as stated in earlier reports. However, the reasons given for hysteresis in these reports such as adsorbates, oxide and interface traps do not explain hysteresis inversion and its reversibility. The critical crossover temperature at which  $\Delta V_{TH} = 0$  is found to vary with the maximum gate voltage ( $V_{GS}^{max}$ ). For example, hysteresis crossover occurred at a higher temperature



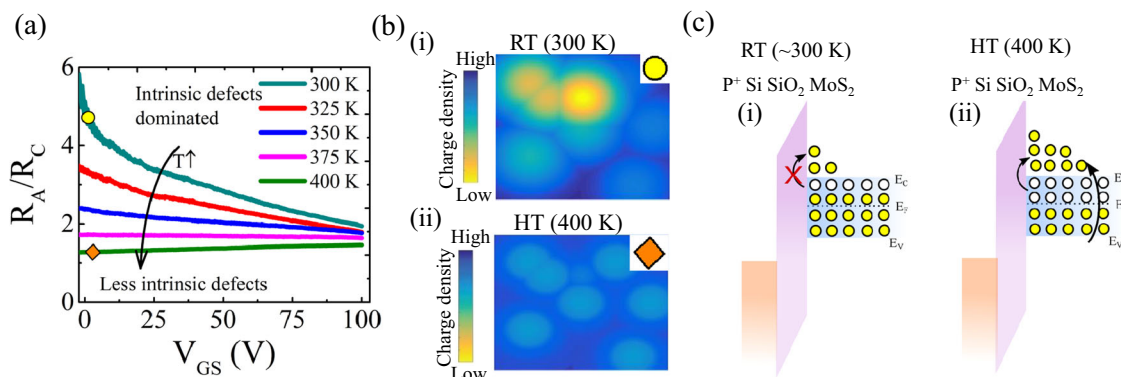
**Fig. 3** Schematic representation of different models used to explain hysteresis with band diagrams and their corresponding effect on transfer curves at room temperature (RT) and high temperature (HT). **a** Electron capture/release by adsorbates, where a large positive gate voltage attracts adsorbates on MoS<sub>2</sub> surface that act as dopants. This effect should diminish at higher temperatures due to desorption. **b** Gate voltage dependent spatial distribution of mobile ions in the oxide gives anti-clockwise hysteresis at RT. **c** Thermally activated oxide traps (close to MoS<sub>2</sub>) that can capture and release electrons from MoS<sub>2</sub>. A negative gate bias releases electrons trapped at the SiO<sub>2</sub>-MoS<sub>2</sub> interface into the MoS<sub>2</sub> channel, leading to positively charged traps, whereas a large positively biased gate results in electron capture, resulting in electrically neutral traps. **d** charge exchange between the gate and the oxide results in anti-clockwise hysteresis mainly at HT. **e** Intrinsic/interface defects/traps in MoS<sub>2</sub> cause hysteresis primarily at RT and collapses at HT

(425 K) for small  $V_{GS}^{max}$  (-40 to +80 V) compared to 350 K for  $V_{GS}^{max}$  of  $\pm 100$  V, as shown in Supplementary Information S2. Figure 2f shows  $\Delta V_{TH}$  for increasing (300–500 K) and decreasing (500–300 K) temperature sweeps. Hysteresis changes from clockwise at 300 K to anti-clockwise at 500 K for increasing temperature sweep (300–500 K). The transition of hysteresis from anti-clockwise at 500 K back to clockwise at room temperature for decreasing temperature sweep implies that the hysteresis inversion is reversible.

To understand the origin of the hysteresis phenomena described above, we examine different hysteresis mechanisms (shown in Fig. 3 and Table 1) considered in previous studies.<sup>16–19,22,23,25</sup> Adsorbate mediated hysteresis mechanism<sup>18,19</sup> is shown in Fig. 3a. For large positive gate bias, water and oxygen molecules get attracted towards the MoS<sub>2</sub> surface. These adsorbed molecules capture electrons from MoS<sub>2</sub>, which leads to electron depletion and an increase in the threshold voltage. For large negative gate bias these trapped electrons are released from adsorbed molecules into the MoS<sub>2</sub> channel which reduces  $V_{TH}$ .<sup>19</sup> This leads to a positive  $\Delta V_{TH}$  and therefore, clockwise hysteresis. However, our results do not support adsorbate mediated hysteresis because, (1) for measurements done in a dry vacuum/nitrogen ambiance increasing the temperature should reduce the amount of adsorbates on MoS<sub>2</sub>, and hence decrease the hysteresis until it collapses (shown in Fig. 3a). However, further increase in temperature would not result in anti-clockwise hysteresis (negative  $\Delta V_{TH}$ ), and, (2) loss of adsorbates implies that hysteresis cannot be recovered by decreasing temperature to room temperature (shown in Fig. 2f). Hysteresis due to mobile ions<sup>34,35</sup> (Na<sup>+</sup> and K<sup>+</sup>) in the oxide is shown in Fig. 3b. Depending on the gate voltage, mobile ions come close to MoS<sub>2</sub> (onset of RS,  $V_{GS} = 100$  V) or close to gate (onset of FS,  $V_{GS} = -100$  V). This results in

anti-clockwise hysteresis at 300 K that increases at higher temperature which is inconsistent with hysteresis collapse and inversion observed in our devices. Another possible hysteresis mechanism due to oxide traps close to MoS<sub>2</sub> is shown in Fig. 3c.  $V_{TH}$  increases for large positive gate bias due to electron trapping in SiO<sub>2</sub>, whereas electron release from the oxide traps into MoS<sub>2</sub> at large negative gate bias decreases the  $V_{TH}$ . This mechanism leads to a positive  $\Delta V_{TH}$  (i.e. clockwise hysteresis) at room temperature and  $\Delta V_{TH}$  increases with temperature due to enhanced thermally assisted trapping and de-trapping<sup>22</sup> which does not explain the hysteresis inversion seen in our devices. To further understand the exchange of electrons between SiO<sub>2</sub> and MoS<sub>2</sub> (shown in Fig. 3c), we compared the hysteresis behavior of two-terminal supported and suspended transistors. Comparable magnitude of hysteresis in suspended (~44 V) and supported devices (~65 V) at 300 K (Supplementary Information S3) indicates that the contribution to hysteresis from exchange of electrons between oxide and MoS<sub>2</sub>, and from the reduced effective gate voltage due to the additional ~100 nm air-gap between SiO<sub>2</sub> and the MoS<sub>2</sub> flake is small. Clockwise nature of the hysteresis at 300 K and its reduction with increase in temperature due to intrinsic traps is consistent with similar results for suspended devices. However, variable temperature measurements on suspended devices do not show hysteresis crossover for the same applied voltage and temperature values as in the case of supported ones, likely due to reduced effect of trapped oxide charges, gate field, and temperature (as air has low thermal conductivity than SiO<sub>2</sub>) with the additional ~100 nm air-gap. Hysteresis mechanisms due to oxide traps close to p<sup>+</sup> Si gate is shown in Fig. 3d. In a recent study, He et al. have shown zero hysteresis at room temperature and negative hysteresis (anti-clockwise) at high temperatures (>350 K) in monolayer MoS<sub>2</sub> FET due to charge tunneling between the oxide and the p<sup>+</sup> Si gate.<sup>29</sup>





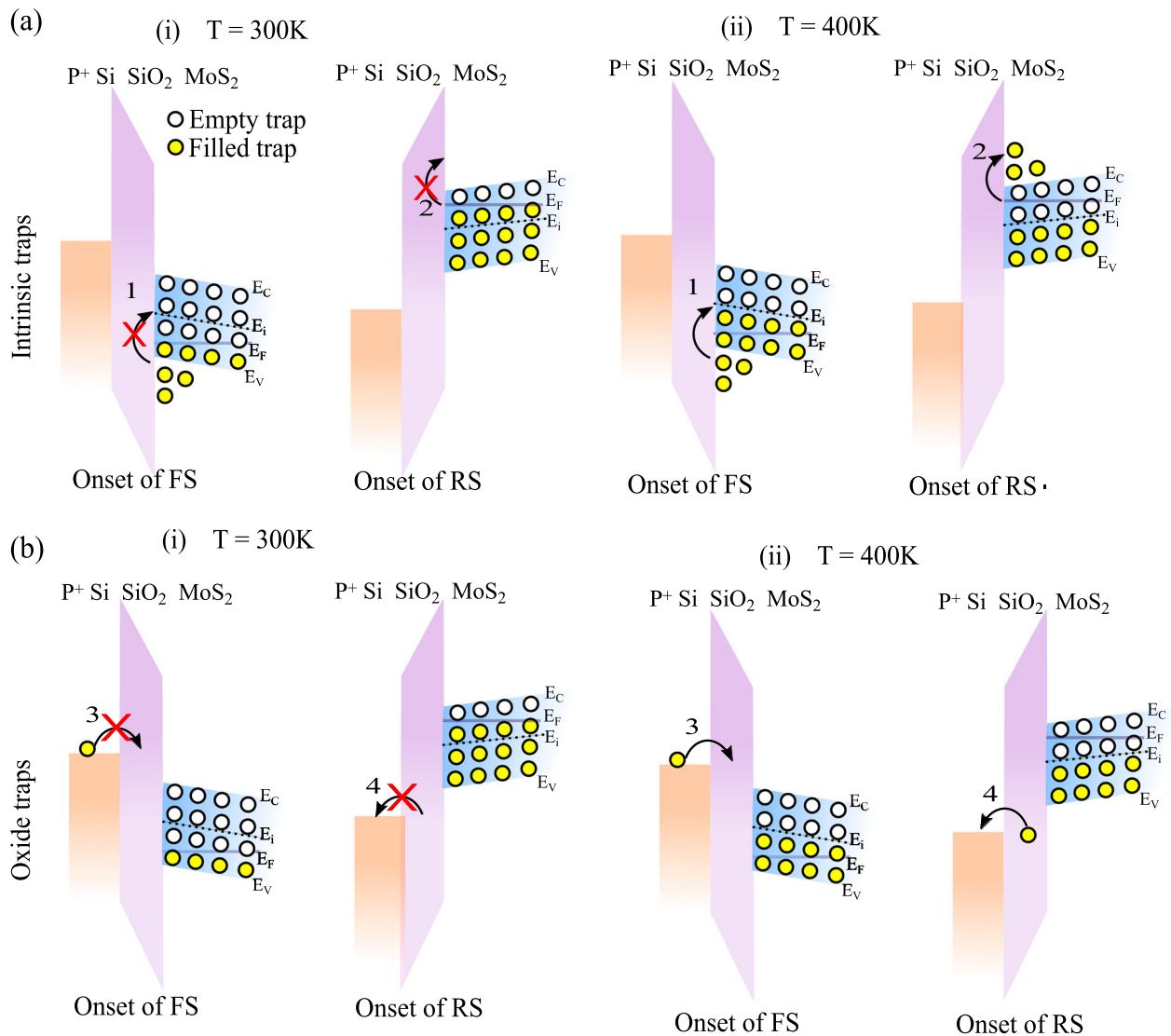
**Fig. 4** **a** Change in  $R_A/R_C$  with gate voltage indicates defect-induced variation in local sheet conductance. For defect-free MoS<sub>2</sub>,  $R_A/R_C$  ratio will be constant. **b** Schematic charge density plots at RT and HT where yellow regions represent low charge density (high defect density) areas. **c** Energy band diagram at ~400 K shows increase in charge density through de-trapping and increased intrinsic carrier concentration which reduces the effect of defects as shown in (b) ii

The possibility of the existence of oxide traps nearer to the  $p^+$  Si gate is more than their existence close to MoS<sub>2</sub>, due to the thermal oxidation process on  $p^+$  Si for gate oxide formation.<sup>36</sup> We will refer to oxide traps near  $p^+$  Si as ‘oxide traps’ in further discussion. Hysteresis due to intrinsic/interface defects is illustrated in Fig. 3e. It reduces with increasing temperature and eventually becomes zero for high temperature as shown in Fig. 3e. First consider the case of low temperatures for intrinsic/interface defects/traps. At the onset of FS ( $V_{GS} = -100$  V), the channel is fully depleted and there is insufficient thermal energy for bound electrons to get trapped. Conversely, at the onset of RS ( $V_{GS} = 100$  V), the channel has significant free carriers which quickly fill traps causing a decrease in conduction, and clockwise hysteresis is observed. However, at higher temperatures, the traps become thermally available at all values of  $V_{GS}$  and therefore any hysteresis is no longer observed above a threshold temperature. Though, both interface (MoS<sub>2</sub>/SiO<sub>2</sub>) and intrinsic (MoS<sub>2</sub>) traps distributed in energy bandgap show clockwise hysteresis at RT and collapse at HT, significant hysteresis in suspended transistors (Supplementary Information S3) suggests that intrinsic traps are the primary cause of hysteresis in MoS<sub>2</sub> at RT. A more detailed explanation of hysteresis due to intrinsic and oxide traps is given in Fig. 5.

Van der Pauw measurements in different configurations (Fig. 1d) reinforce the presence of intrinsic traps/defects in the multilayer MoS<sub>2</sub> channel, which could be both, interlayer and intralayer defects (i.e. atomic point defects such as molybdenum and/or sulfur vacancies), unlike monolayer MoS<sub>2</sub> which does not show any clockwise hysteresis at room temperature<sup>29</sup> likely due to the absence of interlayer traps and smaller number of intralayer defects. The advantage of using  $R_A/R_C$  measurements is that they allow the gate-dependent homogeneity of charges to be determined.<sup>27</sup> This information can let us know at what temperatures doping inhomogeneities exist (Fig. 4a), and therefore at what temperatures they may contribute to hysteresis behaviour. Resistance calculated in configurations A and C must be equal for defect/trap free MoS<sub>2</sub>.<sup>27</sup> However, non-uniform sheet conductance due to defects in MoS<sub>2</sub> makes the current path different in A and C configurations resulting in different  $R_A$  and  $R_C$  values.<sup>27</sup> Large changes in  $R_A/R_C$  ratio at 300 K (shown in Fig. 4a) for varying gate voltage confirms non-uniformity in local sheet conductance as shown in Fig. 4b i, which is most likely due to non-uniform intrinsic defects in the MoS<sub>2</sub> flake.<sup>27,37</sup> Constant  $R_A/R_C$  ratio with varying gate voltage at high temperatures results from increase in charge density due to both de-trapping and increase in intrinsic concentration (shown in Fig. 4c ii). This increase in free carriers significantly reduces the effect of defects resulting in uniform charge density (sheet conductance) as shown in Fig. 4b ii.

A detailed analysis of the transfer characteristics at 300 K (Fig. 2a) and 400 K (Fig. 2e) is shown through corresponding band diagrams for FS and RS in Fig. 5a, b (i) and (ii), respectively. To explain clockwise hysteresis at RT that collapses at higher temperatures, we propose a model based on temperature dependent trapping/de-trapping of electrons associated with intrinsic traps in the MoS<sub>2</sub> channel that can only be observed in devices with a fully depleted channel.<sup>38</sup> Schematic energy band diagrams perpendicular to the channel are shown in Fig. 5 for  $V_{GS} = 100$  and  $-100$  V. Onset of RS (100 V) and FS ( $-100$  V) will affect the entire RS and FS range, respectively, considering deep level traps that require times longer than the sweep times to trap/de-trap electrons. The different amount of trapped charges at the onset of FS and RS result in clockwise hysteresis at 300 K as shown in Fig. 5a i. When the temperature is increased, filled-traps close to the conduction band (onset of RS) get empty, while empty-traps close to the valence band (onset of FS) get filled (Fig. 5a ii). Hence, reduction in the difference of trapped charges in FS and RS reduces hysteresis. As the temperature is increased further, a situation arises when all the traps above the intrinsic energy-level ( $E_i$ ) are empty and completely filled below  $E_i$  in both FS and RS (same probability of trapping and de-trapping at  $E_i$  ensures no further change in trapped charges with temperature). Equal number of filled and empty traps in FS and RS implies similar  $V_{TH}$  values leading to a collapse of the hysteresis ( $\Delta V_{TH} = 0$  V).

However, Fig. 2f shows  $\Delta V_{TH}$  going from positive to negative values at a crossover temperature and becoming zero at a temperature lower than what is expected solely from intrinsic traps. This suggests another hysteresis mechanism arising from charge exchange between the gate and gate oxide<sup>29</sup> at play, which starts at a temperature lower than the crossover temperature but with an opposite sign of  $\Delta V_{TH}$ . Anti-clockwise hysteresis emerges when the temperature is increased beyond 350 K. At room temperature, carriers in the gate do not have sufficient energy to access traps within the oxide and hence they do not contribute to the hysteresis at 300 K (shown in Figs. 3e and 5b i). However, increased thermal energy at higher temperatures (>350 K) allows these sites to participate in carrier trapping/de-trapping (shown in Figs. 3d and 5b ii). The activation energy associated with filling of deep traps in SiO<sub>2</sub> has been estimated to be ~130 meV.<sup>29</sup> This is gained in the form of thermal energy at higher temperatures leading to electron injection from the gate into the oxide for large negative  $V_{GS}$ . These trapped charges in the oxide cause a shift towards more positive  $V_{TH}$  for FS. On the contrary, a large positive  $V_{GS}$  transfers the trapped charge carriers back into the gate resulting in a shift towards more negative  $V_{TH}$  for RS. Higher  $V_{TH}$  for FS as compared to RS implies a negative  $\Delta V_{TH}$  or anti-clockwise hysteresis. Variation of the FS and RS

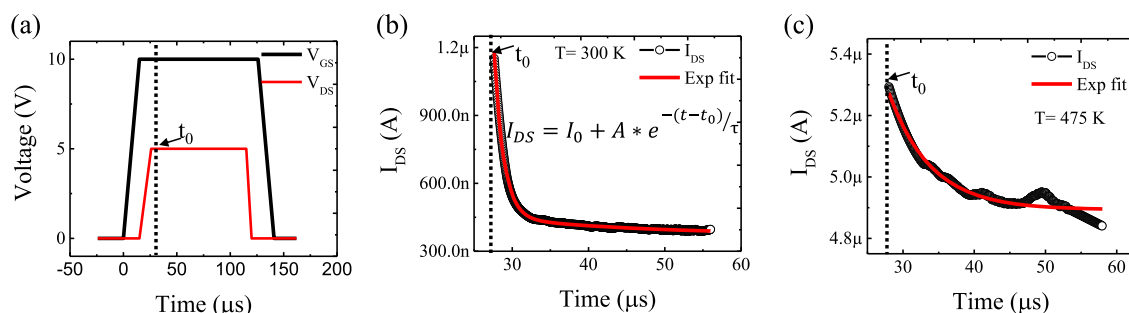


**Fig. 5** Energy band diagram schematics at the onset of FS ( $V_{GS} = -100$  V) and RS ( $V_{GS} = +100$  V) for 300 and 400 K showing key mechanisms responsible for hysteresis. **a** Temperature dependent trapping (1) in FS and de-trapping (2) in RS of intrinsic traps in MoS<sub>2</sub> channel. (i) Trapped (de-trapped) charges for reverse (forward) sweep at 300 K result in increase (decrease) in  $V_{TH}$  and hence, clockwise hysteresis. (ii) Increase in temperature enhances the de-trapping in RS and trapping in FS. Further, increase in temperature ( $\sim 400$  K) results in equal number of trapped charges in both FS and RS resulting in hysteresis collapse ( $\Delta V_{TH} = 0$  V). **b** Temperature dependent tunneling into oxide from p<sup>+</sup> Si gate (3) and tunneling from oxide into p<sup>+</sup> Si gate (4). (i) Lack of tunneling at 300 K indicates mechanisms 3–4 are insignificant and there is no hysteresis due to oxide traps. (ii) At high temperatures ( $\sim 400$  K) electrons will tunnel into (out of) gate oxide for large negative (positive) bias which results in increase (decrease) in  $V_{TH}$  for forward (reverse) sweep and hence, anti-clockwise hysteresis

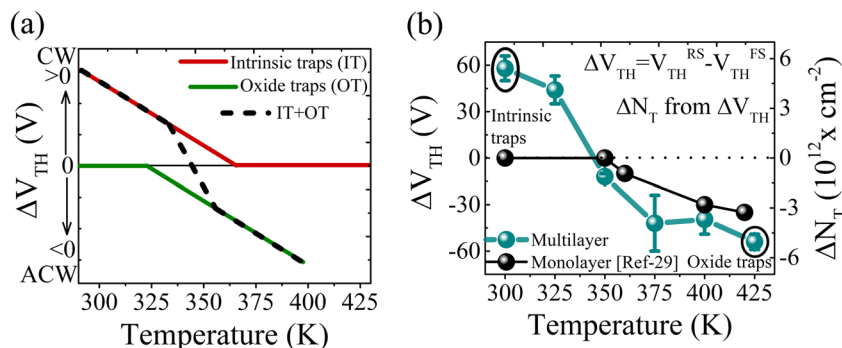
transconductance peaks with  $V_{GS}$  and temperature as shown and analyzed in Supplementary Information S5 further validates the intrinsic-oxide trap model.

Hysteresis primarily occurs due to charge trapping and de-trapping at interface/intrinsic or oxide traps. Pulsed  $I-V$  measurements were performed on two-terminal devices to extract the time response of traps at different temperatures, where one of the contacts is defined as source and the other as drain. Since traps have a certain time constant, they will not respond when the ON pulse width is smaller than this value, resulting in reduced hysteresis.<sup>39</sup> Therefore, we extracted the trap time constants at different temperatures, to determine the minimum ON pulse (drain/gate) width for traps to respond. Figure 6a shows the gate and drain pulses and biases applied to MoS<sub>2</sub> FETs. Change in drain current during the first 40  $\mu$ s of the 100  $\mu$ s drain pulse is shown in Fig. 6b, c for 300 and 475 K, respectively. The drain current ( $I_{DS}$ ) is

best fitted (red line) with  $I_{DS} = I_0 + A \cdot \exp(-(t - t_0)/\tau)$ , where  $I_0$  is the steady state drain current,  $A$  is a fitting parameter,  $t$  is the time,  $t_0$  is the beginning time of the drain pulse and  $\tau$  is the trap time constant. This equation yields trap time constant values of  $\sim 1.5$   $\mu$ s for intrinsic traps at 300 K and  $\sim 6.5$   $\mu$ s for oxide traps close to p<sup>+</sup> Si at 475 K. The extracted oxide trap time constant is similar to values reported in previous reports on oxide traps close to the p<sup>+</sup> Si-SiO<sub>2</sub> interface<sup>40</sup> but smaller than the oxide trap time constant close to the MoS<sub>2</sub>-SiO<sub>2</sub> interface.<sup>41</sup> The pulse width should be larger than these trap time constants to ensure participation of all traps in hysteresis. Another important factor which affects the hysteresis is the sweep rate ( $S$ ) of transfer characteristics,  $S = \frac{\Delta V}{t_s}$ , which was varied from 0.3 to 30 V/s by changing the voltage step size ( $\Delta V$ ) for a given sampling time  $t_s$ . Low sweep rate ensures that nearly all the traps are taking part in the hysteresis phenomenon.<sup>42</sup> We also varied the measurement frequency,  $f = \frac{1}{N \times t_s}$  from 0.002 to 0.27 Hz,



**Fig. 6** **a** Schematic diagram of gate and drain pulse applied to MoS<sub>2</sub> transistor. **b, c** Change in drain current in response to drain pulse time shown in Fig. 6a at 300 and 475 K, respectively



**Fig. 7** **a** Schematic showing expected evolution of  $\Delta V_{TH}$  for two different hysteresis mechanisms with temperature. The solid red line shows clockwise hysteresis due to intrinsic traps and the solid green line shows anti-clockwise hysteresis at high temperature which results from charge exchange between the gate and the oxide. The dotted black line shows the combined effect due to both intrinsic (MoS<sub>2</sub> and MoS<sub>2</sub>-SiO<sub>2</sub>) and oxide traps. **b** Experimentally extracted  $\Delta V_{TH}$  for monolayer<sup>29</sup> and various vdP multilayer (this work) MoS<sub>2</sub> devices and extracted trap density variation with temperature. Error bars indicate variation in the  $\Delta V_{TH}$  values

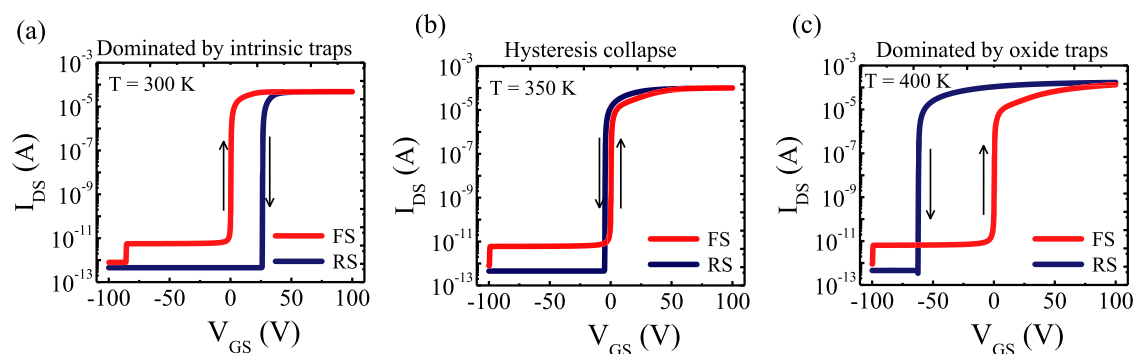
where  $N$  is the number of voltage step points.<sup>42</sup> However, we did not see any significant change in  $\Delta V_{TH}$ .

Inversion of hysteresis with temperature mediated by the two independent mechanisms of intrinsic and oxide traps is illustrated in the schematic shown in Fig. 7a. The solid red line shows the effect of hysteresis due to intrinsic traps in MoS<sub>2</sub>. Here,  $\Delta V_{TH}$  reduces with increasing temperature and eventually becomes zero for high temperature. The solid green line shows  $\Delta V_{TH}$  to be zero at room temperature and negative at high temperature resulting from charge tunneling between the oxide and the gate. The algebraic sum of these two hysteresis curves (black dotted line) is qualitatively similar to the data shown in Figs. 2f and 7b. The difference between RS and FS  $V_{TH}$ ,  $\Delta V_{TH} = q \frac{\Delta N_T}{C_{ox}}$  was used to extract the trap density  $\Delta N_T$  in  $\text{cm}^{-2}$  (shown in Fig. 7b).<sup>22</sup> Trap density extracted at room temperature was normalized with MoS<sub>2</sub> flake thickness to give the total intrinsic trap density considering that hysteresis at low temperature stems from intrinsic MoS<sub>2</sub> traps. On the contrary, anti-clockwise hysteresis at 400 K has been attributed to the charge stored in the gate oxide depending on the gate voltage. Therefore, trap density calculated at 400 K was normalized to oxide thickness to give the total oxide trap density. To further validate the proposed intrinsic-oxide trap model for hysteresis, technology computer-aided design (TCAD) device simulations were performed using the experimental intrinsic and oxide trap densities as described in more detail in Supplementary Information S7 and S8. Consistent with the experimental data, Fig. 8a shows clockwise hysteresis at room temperature that collapses at a crossover temperature of  $\sim 350$  K as shown in Fig. 8b. Figure 8c shows anti-clockwise hysteresis due to exchange of charge between the gate and the oxide traps, thereby reproducing the experimentally observed thermally assisted hysteresis inversion.

We demonstrate two possible applications using thermally assisted hysteresis inversion in MoS<sub>2</sub>. The hysteresis transfer curve can be exploited for non-volatile memory applications. At 375 K, the dominating mechanism is tunneling of electrons into the gate oxide from the gate which gives fairly uniform transfer characteristics throughout the operating window. We would like to emphasize that the working temperature of 375 K is lower compared to MoS<sub>2</sub> devices demonstrated in previous studies.<sup>29</sup> More details are available in Supplementary Information S9. Hysteresis inversion can be exploited for power reduction in heavy-'0' and heavy-'1' digital applications where the occurrence of one state (state '0'/'1') is more frequent than the other. Depending on the case, one can assign an operating temperature for the device which has lower read conductance for the more frequent state, '0' or '1'. For the devices in this work, heavy-'0' and heavy-'1' conditions can be operated at 375 and 300 K respectively. More details are available in Supplementary Information S10. This device can also be used as a temperature sensor by mapping the differential conductance ( $\Delta\sigma_s = \sigma_{FS} - \sigma_{RS}$ ) at a given  $V_{GS}$  to different operating temperatures. More details are available in Supplementary Information S9. This data can be used as a look-up table to calibrate the sensor as well as read out the existing temperature using appropriate intra/extra-polation techniques.

In conclusion, this work demonstrates thermally assisted reversible hysteresis inversion in contact resistance-independent, gated few layer MoS<sub>2</sub> vdP devices. By analyzing measurements in varying ambient (vacuum vs. nitrogen) conditions and configurations (supported vs. suspended), as well as accounting for the nature of hysteresis (CW vs. ACW) and its reversibility using temperature, we exclude the role of adsorbates, interface traps and oxide traps close to MoS<sub>2</sub> in giving rise to hysteresis. Instead, we show that intrinsic MoS<sub>2</sub> traps give rise to CW hysteresis at RT that decreases with temperature and charge exchange between





**Fig. 8** Device simulations using experimental intrinsic and oxide trap densities show, **a** clockwise hysteresis due to intrinsic traps at RT (300 K), **b** hysteresis collapse at a crossover temperature of 350 K, and, **c** anti-clockwise hysteresis due to charge exchange between oxide traps and the p<sup>+</sup> Si gate, thereby validating the intrinsic-oxide trap model for hysteresis

the gate and gate oxide traps at higher temperatures results in ACW hysteresis. Device simulations incorporating experimental intrinsic and oxide trap densities are shown to reproduce temperature dependent hysteresis inversion reinforcing the intrinsic-oxide trap model, which is also consistent with vdP measurements ( $R_A/R_C$  variation with  $V_{GS}$ ).

The hysteresis in few layer MoS<sub>2</sub> can be used to develop a non-volatile memory where its temperature dependence can be used to control the read window and power dissipation, and its inversion can be used to minimize power dissipation for specific digital logic requirements. Similarly, temperature dependent differential conductance arising from the hysteresis can be used to develop temperature sensors where the inversion of hysteresis enables a large working temperature range (100 K). It is important to note that the reversibility of hysteresis with temperature is a must for temperature sensing applications, hitherto undemonstrated in few layer MoS<sub>2</sub> devices.

## METHODS

Gated MoS<sub>2</sub> devices were fabricated in vdP configuration (shown in Fig. 1a, c) to eliminate the effects of contact resistance on hysteresis. Device fabrication started with 280 nm thermally grown SiO<sub>2</sub> on a degenerately doped p-type Si substrate. Reactive ion etching of the SiO<sub>2</sub> surface was carried out to improve MoS<sub>2</sub> adhesion on the SiO<sub>2</sub> surface. MoS<sub>2</sub> was mechanically exfoliated from a molybdenite crystal (from SPI supplies) using scotch tape method similar to graphene. The flakes were then identified using an optical microscope, and their thickness was measured by AFM. Multilayer flakes with ~5–10 nm thickness were selected for ease of device fabrication as well as better electrical conduction as compared with monolayer flakes. Nearly square large area flakes were chosen to make four contacts at the corners. After flake identification, alignment markers were made by standard electron beam lithography (Raith 150-Two) followed by electron beam source/drain patterning using PMMA. Finally, 60 nm of Au was deposited using an electron beam evaporator under high vacuum conditions followed by lift-off. Electrical transport studies were conducted at room temperature using a probe station connected to an Agilent BX-1500 parameter analyzer. Temperature dependent electrical transport measurements were conducted using a Lakeshore low-temperature measurement system (CRX-4K) and Linkam probe station under vacuum and nitrogen ambient conditions.<sup>43</sup> The sample was heated by heating the chuck (on which it was placed) and not the entire chamber. Further, the nitrogen gas was flowing continuously between inlet and outlet line of the chamber which assures that nitrogen gas is not at the same temperature as that of the sample, rather it is closer to room temperature.

## Data availability

The authors declare that [the/all other] data supporting the findings of this study are available within the paper [and its [Supplementary Information](#) files]. Any additional data that supports the findings of this study are available from the corresponding author upon reasonable request.

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## AUTHOR CONTRIBUTIONS

N.K., D.H.P. and S.L. designed and discussed the project. N.K., K.T. and N.G. carried out the fabrication. N.K. and D.M. performed the variable temperature measurements. P. B. and D.H.P. provided assistance with vdP measurements. B.M. carried out the suspended transistor fabrication. N.K. and K.T. performed the TCAD simulations. All authors discussed the results and N.K. wrote the paper.

## ADDITIONAL INFORMATION

**Supplementary information** accompanies the paper on the *npj 2D Materials and Applications* website (<https://doi.org/10.1038/s41699-017-0038-y>).

**Competing interests:** The authors declare that they have no competing financial interests.

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