Optimum phase shift in the self-oscillating loop for piezoelectric transformer-based power converters

Ekhtiari, Marzieh; Zsurzsan, Tiberiu-Gabriel; Andersen, Michael A. E.; Zhang, Zhe

Published in:
I E E E Transactions on Power Electronics

Link to article, DOI:
10.1109/TPEL.2017.2771297

Publication date:
2017

Document Version
Peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

Optimum phase shift in the self-oscillating loop for piezoelectric transformer-based power converters

Marzieh Ekhtiari, Tiberiu-Gabriel Zsurzsan, *Member, IEEE,* Michael A. E. Andersen, *Senior Member, IEEE,* and Zhe Zhang, *Senior Member, IEEE*

***Abstract*—A new method is implemented in designing of self-oscillating loop for driving piezoelectric transformers. The implemented method is based on combining both analog and digital control systems. Digitally controlled time delay through the self-oscillating loop results in very precise frequency control and ensures optimum operation of the piezoelectric transformer in terms of gain and efficiency. Time delay is implemented digitally for the first time through a 16 bit digital-to-analog converter in the self-oscillating loop. The new design of the delay circuit provides 45 ps time resolution, enabliong fine-grained control of phase in the self-oscillating loop. This allows the control loop to dynamically follow frequency changes of the transformer in each resonant cycle. Ultimately, by selecting the optimum phase shift, maximum efficiency under the load and temperature condition is achievable.**

***Index Terms*—Optimum delay line; self-oscillating loop; phase shift; switch mode power supply; zero-voltage switching; piezoelectric transformer.**

NOMENCLATURE

ADL-CEZC	Adjustable delay line circuit added to the CEZC block.
C	Resonant capacitance of the piezoelectric transformer.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
CEZC	Current estimation zero crossing.
DDL	Dynamic delay line.
DDL_{in}	Input signal of the DDL block.
DDL_{out}	Output signal of the DDl block.
EDDL_{in}	Input signal of the digitized delay line block passed through the edge detector.
FF	Flip-flop.
FPGA	Field-programmable gate array.
FTD	Fixed time delay.
HS	High-side gate voltage.
i_{res}	The resonant current of the piezoelectric transformer.
L	Internal inductance of the piezoelectric transformer.
LS	Low-side gate voltage.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
ODL	Optimum delay line circuit block.
ODL_{out}	Output signal of the optimum delay line circuit block.
R	Dielectric losses inside the transformer.
R_m	Matched load for the piezoelectric transformer.
v_F	Switching voltage.
$\text{ZC}i_{res}$	Zero crossed signal of the estimated resonant current.
ZVS	Zero-voltage switching.
ω	Switching angular frequency.
ϕ_I	Phase shift of the resonant current with reference to the turn-off time of the low-side switch.

All authors are with the Electronics Group, Department of Electrical Engineering, Technical University of Denmark, Elektrovej, bld. 325, Kgs. Lyngby,DK-2800, Denmark.

E-mail: [maekh, tgzsur, ma, zz]@elektro.dtu.dk

Part of the work described in this paper has been published in the IEEE Applied Power Electronics Conference and Exposition 2016 (APEC 2016) [1]

Manuscript received March 31, 2017; revised July 7, 2017 and August 30, 2017; accepted October 23, 2017. Date of publication November XX, 2017; date of current version XX, 2017. This work was supported by the Danish National Advanced Technology Foundation. Recommended for publication by Associate Editor XX.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.XXXXXXX

I. INTRODUCTION

516.0ptPiezoelectric transformer-based switch-mode power supplies have never seen wide-spread commercial success, but still see development and use in niche applications where their replacement is difficult [2]–[4]. Specifically, inductorless PT-based switch-mode power supplies (SMPS) are being used because of their magnetic neutrality and immunity to high magnetic fields, where no substitute technology exists [5]–[8]. While these transformers exhibit some advantages over conventional transformer-based converters, such as smaller size, lighter weight and lower electromagnetic interference [9]–[12], their research interest has been hampered by their long prototype iteration times. The PT is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with a matched load coupled to the output of the transformer. The optimum operating frequency shows strong dependency on parameters such as temperature, load, fixation and age [9], [13]–[15]. In order to optimally operate a PT at a frequency slightly above resonance [16], where it exhibits inductive behavior, it is necessary to follow the parametrically dependent resonant peak [13], [17]–[19].

When an inductorless topology is employed for PT-based converters, the operating frequency of the transformer is reduced to a narrow band in which it exhibits an inductive behavior. Due to a very high Q factor, small variations in the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

resonant frequency can easily cause instability in the converter. However, keeping operating frequency at a proper point slightly above resonant frequency is difficult through open-loop control. As a consequence, closed loop control is indispensable for compensating influence of parameters such as load and temperature, in order to have stable transformer operation and thereby accurate converter performance [12], [20]–[22]. Nonetheless, despite their difficulty in implementation and higher cost, inductorless topologies are the only solution in applications where magnetic neutrality of the converter is of paramount importance. The converter presented herein is designed to be used inside of a magnetic resonance imaging (MRI) scanner, in the presence of magnetic fields in excess of 3 T. In such a high field, magnetic cores would fully saturate, while the uncontained magnetic fields of coreless inductors would negatively impact the scanner image quality.

Moreover, the intended final application of the converter is to drive a highly capacitive load at low frequencies, ranging from dc to 100 Hz in the form of a quasi-static piezoelectric motor. The motor is called Piezoelectric Actuator Drive (PAD) and is intended to be used inside an MRI chamber for precise positioning of the patient table within the bore of the scanner itself [23]. Therefore, the load range is narrow and quasi-static from the converter perspective as it essentially meant to operate in tracking dc mode.

The options for closed-loop control are phased locked loop (PLL) and self-oscillating loop control methods. The PLL approach, which is also a controlled oscillator, is not a good option for the inductorless PT-based converters, as their multi-period lock-in delays do not allow for fast tracking of changes in converter operating point [16]. Thus, self-oscillating loop is used for the closed-loop control of the transformer's operating point, which enables cycle-by-cycle adjustments.

The self-oscillating loop is able to adjust its phase shift to follow the PT's resonant frequency. An implemented adjustable time delay compensates for the rest of the phase shift in the loop for frequency variations. This is more important when a PT-based converter is operating in bi-directional mode for energy recovery [21]. As an example, when the energy transfered by the converter needs to be controlled to maintain DC output voltage at different voltage levels, the PT's load changes [19], [21]. Any change in the PT's load causes a change in its operating point [19]. In order to keep the PT operating efficiently, its driving frequency should follow resonance peak changes. This is performed by changing the converter's switching frequency. The switching frequency is controlled through a self-oscillating loop [20], [24]. Therefore, by changing the pre-designed phase shift, the switching frequency follows variations in the PT's resonant current.

Phase shift compensation with high resolution becomes necessary, especially when the load of the converter is variable. Notably, the PT's transfer function also varies with temperature [13], [25]. These variations directly translate to the PT's load variations. If the total phase shift of the loop is not properly adjusted to an integer factor of 360°, it causes a damping of the resonant current. Therefore, closed-loop operation cannot be achieved and basically the converter will not start working. Therefore, very fine resolution for phase shift adjustment is required. A more thorough explanation of the self-oscillating loop is provided in the Section II.

Several attempts have been made for closing the feedback loop in the PT-based SMPS [12], [20], [26]. In previous research, an adjustable time delay block that controls the total loop phase has been implemented for a bi-directional converter through an analog circuit. This was done by detecting peaks in the PT's resonant current [21], [27]. In closed-loop operation, 360° phase difference cannot be ensured for the load or temperature variations of the PT, particularly in bi-directional operation [21]. The principle behind self-oscillation obtained in the prior art is explained in the sub-section II-A and experimental results are provided in the sub-section II-C.

The analog implementation becomes unstable when the phase error approaches 0 [21]. To solve this problem, a mixed-signal phase shift compensation is applied in this paper. Changes in the PT's resonant frequency are compensated for by detecting and adding required phase shift in order to obtain a full loop phase shift of 360°. Furthermore, digital implementation allows for fine changes in time delay inside the loop for frequency tracking. Compensation is performed by adding a finely-controlled time delay to the feedback chain. Resolution of the applied time delay is 45 ps. This ensures that the added time delay is finely controllable in order to precisely adapt the frequency of the self-oscillating loop and match changes in the PT's operating point [28]. More explanation about the proposed method is provided in the sub-section III-A and experimental results are provided in the sub-sections II-C and IV. This further ensures soft switching operation of the PT and therefore, the highest attainable efficiency.

II. Self-oscillating loop for PT-based converters

A. Principle and design considerations

Any piezoelectric transformer presents three distinct circuit behaviors with frequency, from its impedance perspective. It is capacitive at low frequencies, behaves like a resistor at resonance and antiresonance and presents inductive properties in between. This is illustrated in a simplified, qualitative fashion in Fig. 1a. In order for a PT-based inductorless resonant converter to be able to both soft switch and oscillate, the PT needs to be operated in its inductive region. This is achieved by ensuring a phase lag between the transformer current and its corresponding voltage of up to $\pi/2$ radians. In a simplified fashion, this can be achieved in a switch-mode converter by using the PT resonant current to generate the corresponding switching waveforms while ensuring the right amount of time delay to maintain transformer inductive operation. Fig. 1b illustrates this process. Thereby, delays induced by circuitry in these types of converters are actually beneficial, as long as the total amount of circuit delay does not exceed the resonant period length of the transformer.

Essentially, two requirements need to be satisfied in order to be able to produce sustained oscillation in closed-loop. One is that phase angle of the entire loop should be an integer multiple of 360°; the other requirement is that the loop gain should be greater than unity to start-up oscillation. This criterion is the Barkhausen oscillation criterion for feedback systems and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

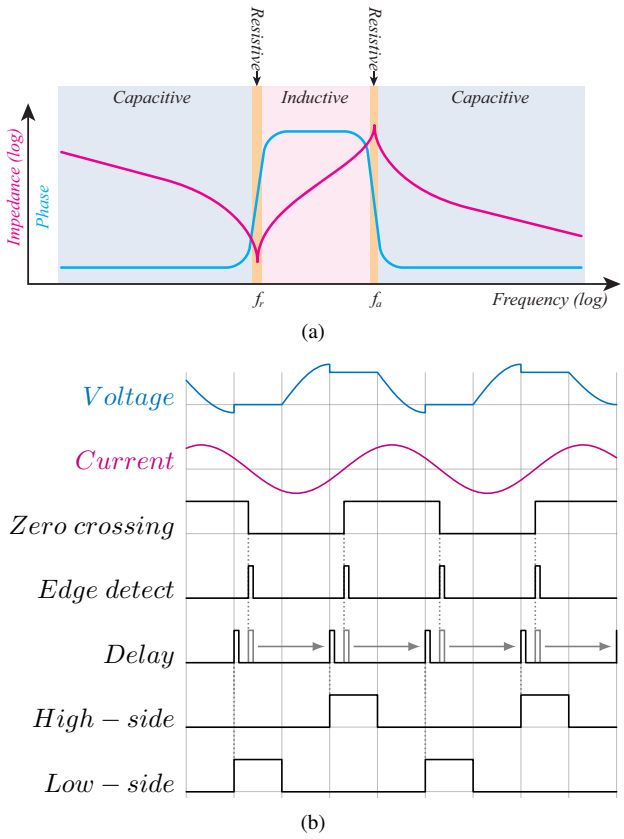


Fig. 1. Illustrative impedance and phase behavior of piezoelectric transformers versus frequency (a) and simplified method of maintaining inductive operation (b).

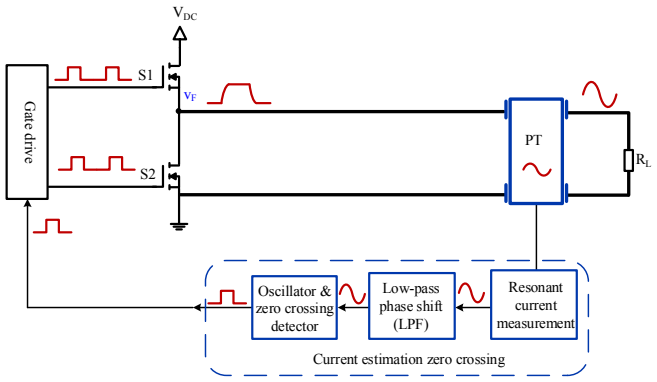


Fig. 2. Block diagram of prior art self-oscillating loop.

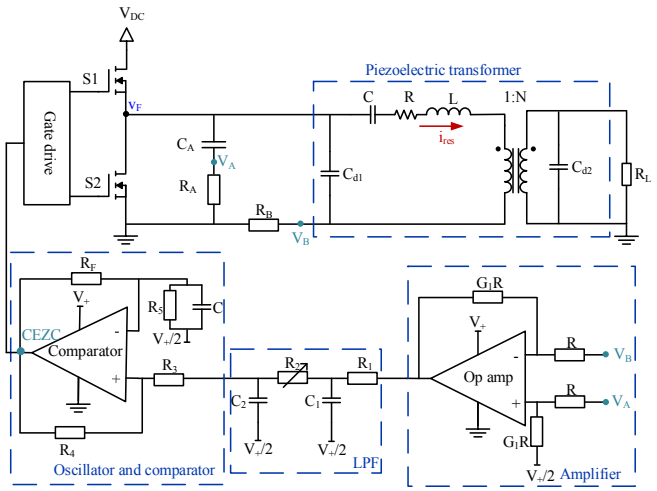


Fig. 3. Circuit design demonstrates principle of self-oscillating loop in PT-based SMPS.

is essentially a simplified and less mathematically rigorous loop-gain method for attaining self-oscillation, compared to the harmonic balance approach [29], [30]. Its attractiveness lies within its simplicity, even though its conditions are not sufficient to ensure self-oscillation in all possible operating conditions. The former condition is fulfilled by adjusting phase shift through the loop. The latter condition is fulfilled by a comparator-based design since the comparator's gain can be considered infinite and therefore its output becomes saturated to the rail voltages, generating square waves in the output. In the designed circuit there is a hysteresis controller which operates as an oscillator during start-up with a frequency close to or lower than the PT's resonance frequency. The start-up frequency can be designed to be slightly lower than the resonance frequency. In this case, it is ensured that oscillation does not lock into the second or higher resonance of the PT. Fig. 2 shows the block diagram for the self-oscillating loop [20], and Fig. 3 shows the circuit for the self-oscillating loop together with the PT-based power stage with matched load. Equation (1) represents the time period of this self-induced oscillation.

$$T = R'_F\, C_3\, ln(1 + \frac{2R_4}{R_5}) \tag{1}$$

where R'_F is equivalent resistance of two parallel resistors, R_F and R_3. The resistor R_5 is used in order to provide an initial condition for the capacitor and helps with oscillation start-up. The ratio of R_4/R_5 forms the hysteresis window to specify a voltage range and to build the appropriate level of noise immunity.

Thereby, small perturbations in the loop start the self-induced oscillation. This results in self-excitation of the resonant current inside the PT during the start-up. Self-excited square waves with a frequency lower than or close to the resonant frequency of the PT will excite resonant modes inside the transformer. This is achieved by the fundamental frequency of the square waves and its higher order harmonics. Since the PT is operating as a high Q band-pass filter (BPF), it filters higher order harmonics out and transfers the fundamental component to its output. The electrical quality factor of the PT is derived as:

$$Q = \frac{1}{\omega\, C_{d2}\, R_L} \tag{2}$$

where $\omega = 1/\sqrt{LC}$ is the series-resonance angular frequency of the PT [31], [32]. Therefore, resonant current is considered as sinusoidal waveform described in (3).

$$i_{res}(t) = I_{pk}(t)\ sin(\omega t\ -\ \phi_I) \tag{3}$$

where $\phi_I\ \in\ [0,\ \pi]$ is the current phase angle and ω is the same angular frequency defined above.

The amplitude of the fundamental resonant current grows

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

with time, until its level is large enough compared to the self-induced oscillation. Since the amplitude of the sinusoidal waveform at the output of low-pass filter (LPF), shown in Fig. 2, is greater than the amplitude of the self-induced oscillation waveform, the oscillator operates as a comparator. This allows the comparator's behavior to change from that of an oscillator to that of a true comparator. Therefore, it compares resonant current with a DC level in order to mark the zero crossing of the current. The loop is designed for the case where the PT is connected to the resistive matched load [20] by considering Mason's equivalent parameters [33], [34]. The load resistance is obtained from

$$R_{matched} = \frac{1}{\omega\, C_{d2}} \tag{4}$$

The reasoning behind this design choice is that a matched load is considered to be the worst-case scenario for a PT, in terms of achieving soft switching [35]. Attaining zero-voltage switching (ZVS) is crucial for efficient converter operation. Fig. 4a shows the trend of load resistance versus ZVS factor [35]. The ZVS factor, denoted V_P', is a dimensionless, qualitative metric that provides a simplified measure of the soft-switching capability of a piezoelectric transformer used as a resonant tank in an inductorless converter configuration. At the matched load, the energy transfer through the PT is maximum and therefore its efficiency is maximized as well. This results in a point of minimum on the ZVS factor axis [19], [34]. The role of the ZVS factor is to provide the worst-case scenario for analyzing PTs in terms of soft switching capability. Therefore, if ZVS is achieved for the matched load, it will be obtained for other loads as well [35]. The expression for the soft-switching factor is based on an analytic analysis of ZVS in the following equation [36]:

$$V_P' = \frac{1}{n^2}\frac{C_{d2}}{C_{d1}}\frac{36\sqrt{6}}{9\pi^2}\eta \tag{5}$$

where η is the efficiency of the transformer and n is the transformation ratio. If the ZVS factor V_P' is above unity, then the PT is capable of achieving soft-switching. The full mathematical derivation and proof of general validity for this factor are elaborated in [35], [36]. For sake of clarity, the proof will not be presented here. Therefore, the ZVS region is a narrow frequency range above resonance, where the PT behaves as an inductor and $V_P' > 1$. Furthermore, the ZVS bandwidth of the PT is a ratio of L/C for a constant resonance frequency [35]. Equation (5) and Fig. 4b are based on a primary analysis of ZVS in order to justify the necessity to design a driver and self-oscillating loop for the matched load, where Fig. 4b shows the soft switching factor for a PT as an example [35].

B. Current estimation zero crossing (CEZC)

The resonance current in the PT is not directly measurable and is therefore reconstructed two measurement points, which successively capture the individual dynamics within either conduction or dead-time. Voltage $v_B(t)$ across R_B, denoted as V_B in Fig. 3 measures the dynamics of the resonance current while the switches are on. Voltage $v_A(t)$ across R_A, denoted V_A in the same figure measures the dynamics of the resonant

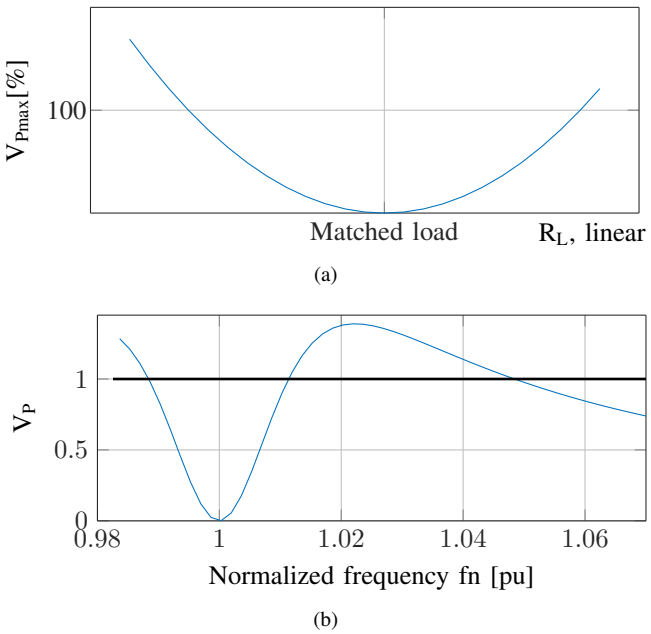


Fig. 4. Soft-switching factor for PT as a function of load resistance (a) and normalized frequency vs. normalized soft switching factor for PT; $R = 98\ m\Omega$, $C = 11.27\ nF$, $L = 733$ µH, $C_{d1} = 112\ nF$, $C_{d2} = 14.6\ pF$, $N = 112$ (b).

current during dead time, while both switches are off. The current in this period is supplied by the Mason-equivalent inductor to the PT's input capacitor C_{d1}. This current can be measured by differentiating the voltage across C_{d1}. This is performed by using C_A and R_A as a differentiator. C_A should be at least 10 times lower than C_{d1} in order not to affect the input capacitance of the PT and, subsequently, dead time and ZVS factor of the transformer. R_A and R_B are also chosen to have low values and in order to set a ratio between $v_A(t)$ and $v_B(t)$ for the input of the op-amp. Subtraction of these two voltage waveforms through the op-amp results in elimination of the steady-state current through both measurement points and therefore an approximate sine waveform representing the resonant current will be reconstructed in the output [16], [20], [37]. The voltage in the output of the op-amp is thus

$$\begin{aligned} v_{out|opamp}(t) &= G_1(v_A(t) - v_B(t)) \\ &= G_1(R_A C_A \frac{d}{dt} v_{C_{d1}}(t) - R_B i_{res}(t)) \end{aligned} \tag{6}$$

where G_1 represents the gain of the op-amp. The estimated current has a 180° phase shift compared to the resonance current which results in the same zero-crossing points. Thereafter, the estimated resonance current is transmitted to a second order low-pass filter (LPF) which provides an additional phase shift through the feedback loop. In order to have adequate phase shift through the LPF, its cut-off frequency is adjusted to be around the resonance frequency. The sole purpose of this additional phase shift is to adjust the control variable zero point to an initial, arbitrary phase shift. This is purely for ease of experimentation and the same effect can be achieved by initializing the control variable to a value different from 0. Additionally, some harmonics are eliminated by the LPF, resulting in a smoother waveform which contains the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

TABLE I
PT EQUIVALENT PARAMETERS

Parameter	Value	Parameter	Value
C_{d1}	3.83 nF	C_{d2}	626 pF
C	565 nF	R	5.63 Ω
L	3.5 mH	N	3.57

TABLE II
MAIN CIRCUIT COMPONENTS

Component	Model	Manufacturer
MOSFET	IPD600N25N3 G	Infineon
Gate Driver	MAX15019	Maxim
DAC	AD5689	Analog Devices

TABLE III
PHASE SHIFT DURING ONE SWITCHING CYCLE IN THE SELF-OSCILLATING LOOP; SWITCHING FREQUENCY IS 118.3 KHZ WITH TIME PERIOD OF 8.45 µS.

Delay	Time[µs]	Phase[°]	Duty cycle[%]
HS→HSGD	1.59	67.8	18.85
HSGD→I_{est}	0.27	11.5	3.19
I_{est}→LPF	6.09	259.4	72.04
LPF→CEZC	0.5	21.3	5.92
Total	8.45	360	100

fundamental harmonic of the resonance current. The filtered signal is transmitted to the comparator and generates a square wave indicating the zero crossing of the input signal. The square wave signal is fed into the adjustable time delay in order to compensate for the rest of the phase shift to have a total of 360° in the whole loop from the input of the gate driver to the output of feedback loop. In case the switching frequency needs to be decreased, the total phase shift should be increased.

C. Experimental results

Fig. 5 shows experimental waveforms. The designed board is shown in Fig. 6. A radial-mode PT with Mason's equivalent circuit, shown in Fig. 3, is used, driven by square wave signals with a switching frequency of 118.3 kHz, while driving a resistive load of 225 Ω. Moreover, the reconstructed resonant current from voltages V_A and V_B is shown in Fig. 5. Furthermore, the equivalent parameter values of the PT are measured and shown in Table I. The most important circuit components are identified in Table II. Phase shifts and corresponding time delays between stages are measured and shown in Table III.

III. PHASE-SHIFT SELF-OSCILLATING LOOP WITH DIGITAL DELAY LINE

A. Digitized delay line

An initial investigation, performed by mapping relative changes in the frequency to the output voltage variations, confirms the necessity of very fine time adjustment capabilities. The result of this investigation shows that there is an measurable change in the amplitude of the PT's output voltage for every 10 Hz change in switching frequency. For example,

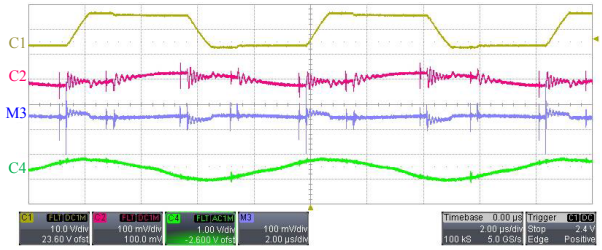


Fig. 5. Reconstruction of the resonant current. C1: switching voltage v_F, C2: V_A, M3: V_B, C4: G1 (V_A-V_B).

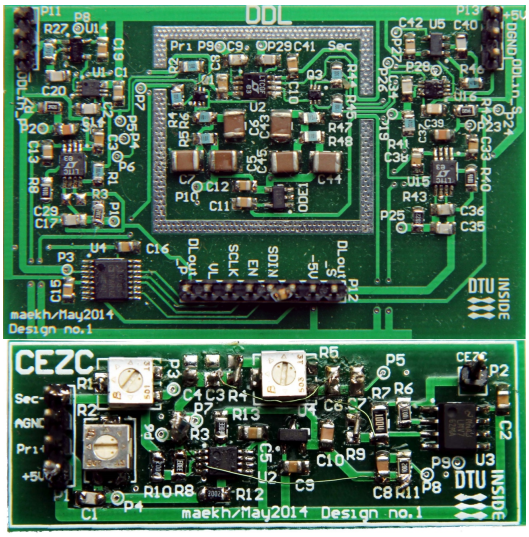


Fig. 6. DDL and CEZC-A boards.

if the operating frequency of 100 kHz increases by 10 Hz, the output voltage shows a considerable change in the amplitude, with empirical experiments showing up to 25 % deviation. This output voltage variation depends on the transformer, the range of operating frequency and the output load. Therefore, a precision of minimum 10 Hz is set as a design target, which results in a minimum 1 ns time delay resolution, as

$$\Delta t_{res} = \left| \frac{1}{f_2} - \frac{1}{f_1} \right| \quad \Rightarrow \quad \left| \frac{1}{100000} - \frac{1}{100010} \right| \approx 1\,\text{ns}.$$

where Δt_{res} is the desired time step and f_1 and f_2 represent an arbitrary change in operating frequency. Thereby, a phase shift self-oscillating closed loop is designed together with the contribution of the digital-to-analog converter (DAC) and field-programmable gate array (FPGA). These are used to implement a high-resolution time delay inside the dynamic time delay block.

Fig. 7a shows the circuit designed for the dynamic delay line (DDL) together with the drawing of the input and output waveforms of the DDL circuit block. In this block, the input signal is first transformed into edge-detected one-shot pulses which are then used as a clock source for the flip-flop. The output of this flip-flop is then used to reset the hardware integrator present in the circuit. Namely, when the input signal edge-triggers the flip-flop, the feedback capacitor in the op-amp feedback starts charging, thereby creating a linear voltage

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

slope. This is then compared to the variable reference voltage provided by the DAC. Thereafter, the complementary output of the comparator resets the flip-flop which consequently turns the MOSFET D1 on and discharges the feedback capacitor, thereby resetting the integrator. Since the input pulse triggers the start of the integration, the variable reference provided to the comparator by the DAC coupled with the voltage slope work together to create a time-delayed version of the input pulse which is proportional to the DAC output value. The output of the comparator is then latched for a short time by its own output through a high-passed signal to its latch pin, resulting in one-shot pulses at the output of the DDL. The performance achieved by the delay block is illustrated in Fig. 7c. A total delay of 3 µs is adjustable in $2^{16} - 1$ steps, with an average exhibited jitter of 90 ps, although the last 3000 samples show a drastic increase in jitter, making the uppermost range of the control variable unusable in practice. This drastic increase in jitter is due to the reference voltage in the comparator in Fig. 7a hitting its supply rail. These timing and jitter measurements were performed with a 40 Gb/s oscilloscope.

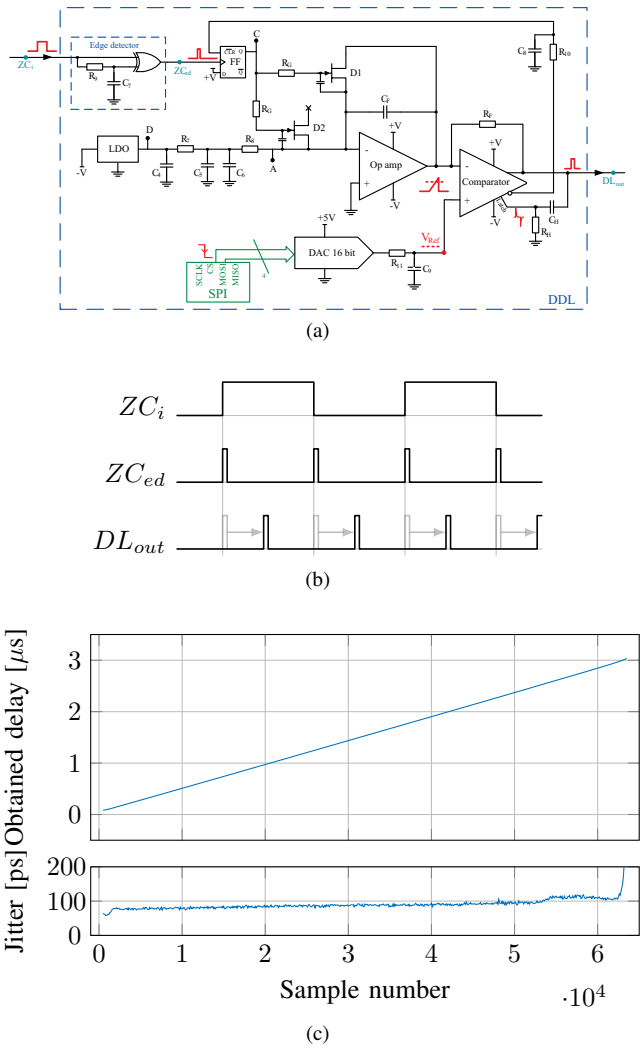


Fig. 7. DDL circuit (a), input and output signals (b) and circuit performance in terms of linearity and jitter (c). The delay sweep shows a linear response with a 45 ps step resolution and an average jitter of 90 ps.

B. Self-oscillating loop based on the optimum time delay

A new phase shift self-oscillating loop for the PT-based converter is designed and proposed consisting of mixed-signal control. Fig. 8a shows the simplified block diagram of the proposed closed-loop with its main blocks. The output signal of the current estimation zero-crossing (CEZC) block is a 50% duty cycle square wave signal ZC_i, having the same frequency as the PT. For the closed-loop operation the reference signal is considered to be the high-side gate voltage (HS). The resonant current zero crossings will then be used to determine the MOSFET gate signals. In this design, the rising edge of ZC_i is used for turning on the high-side switch. By working on the different operating frequency ranges, there is a need for adjusting the phase shift of the LPF inside the CEZC analog block to synchronize the ZC_i and high-side signals. In order to avoid adjusting phase shift in hardware, a digital time delay circuit is added to the CEZC block, named adjustable delay line (ADL-CEZC). The delayed estimated resonant current is then tied to the optimum delay line block (ODL). The output of the ODL is then capable of prolonging the switching period by changing the on time of the switches (Ton). The output of the ODL is fed into the control block in order to generate the high-side and low-side signals as input to the gate driver. In addition to the hardware control gates, the FPGA is also capable to break the control loop and force open-loop operation through the control block.

Fig. 8b shows a more detailed view of the feedback path from Fig. 8a, while also expanding on the main input and output signals inside the block diagram. The voltage v_F is the transformer's primary-side voltage while exhibiting soft switching. i_{res} shows the resonance current of the PT. However, in the PT-based SMPS the resonant current is dependent on the characteristic parameters of the PT and it changes its polarity when either the switches are turned on or their body diodes conduct. Therefore, depending on the operating frequency and temperature of the PT, there is a phase shift between the resonant current and the switching voltage, that is defined as ϕ_I in (3), [34]. The signal ZCi_{res} shows the zero crossing resonant current. The output of the adjustable delay line (ADL-CEZC) turns on the half-bridge switches. This block is composed of a digital delay line (DL_{on}) and a FF with 50% square waves in its input and output. The 50% square wave signal fed into to the ODL and it can be time delayed through a reference signal. In the end the one-shot pulse signal (DL_{off}) generated in the output of the ODL turns off the MOSFETs. The high-side and low-side switches are turned on by rising edges of ZC_{dly} and $\overline{ZC_{dly}}$ signals, respectively, which are used as clock inputs to the control block FFs. The output of the ODL block is then used to reset the FFs, thereby turning the switches off.

The dead-time is first adjusted for a specific design regarding a certain PT and switching frequency. By adjusting the time-delay for turning the switches off, the frequency of self-oscillation changes. The propagation delay in the control block is assumed negligible in the waveforms shown in Fig. 8c.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

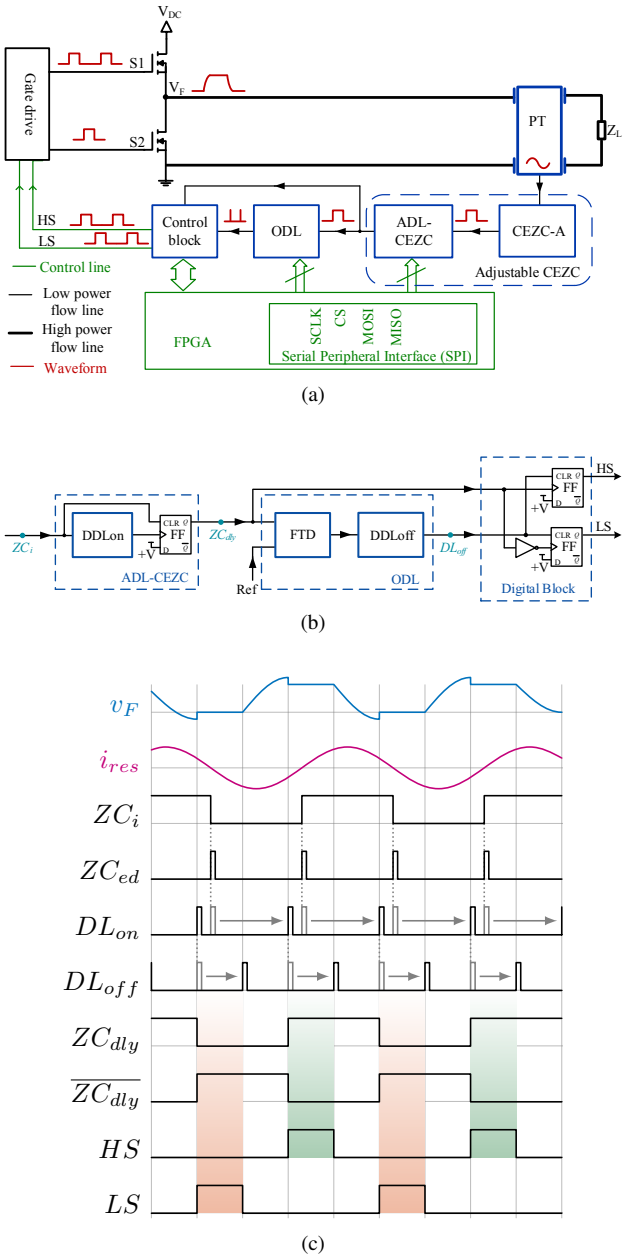


Fig. 8. Block digram of self-oscillating loop with optimum phase (a), a more detailed view of the main circuit blocks(b) and signals with proportional delay for demonstrating the functionality of the optimum phase control method (c).

IV. Results

A prototype has been built and analyzed. Great focus has been placed on full circuit modularity. Fig. 6 shows designed modular boards for DDL and CEZC blocks. The circuit implemented for CEZC is very similar to one explained in section II-B. Fig. 9 shows signals in the input and output of the DDL module in the setup.

Fig. 10 shows the full converter efficiency as a function of both the delay and per-unit voltage gain. The input voltage is 24 V and the load is a 225 Ω resistor in parallel with a 470 µF capacitance. For each specific output voltage the delay has been swept from a minimum value to the maximum value in the range that ZVS is obtained. The starting point for the delay sweep is set to 115.6 kHz for each voltage gain step. Efficiency

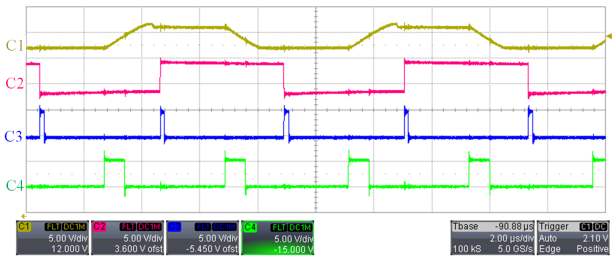


Fig. 9. Signal waveforms where dynamic delay is applied; C1: switching waveform ($v_F(t)$); C2: CEZC as input of DDL block; C3: one-shot pulse as input of DDL block ($EDDL_{in}$); C4: output of DDL (DDL_{out}).

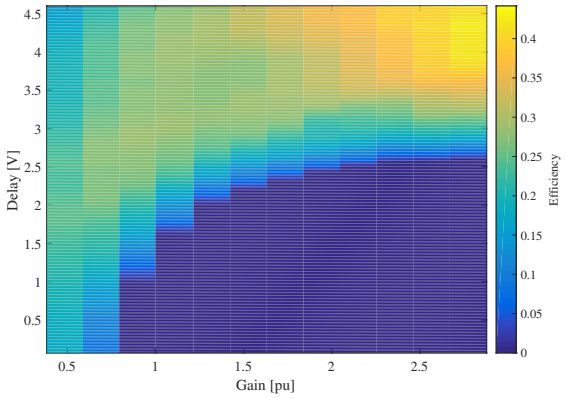


Fig. 10. Experimental results: Efficinecy as a function of delay and per-unit voltage gain.

is increasing with both delay and gain, but the delay is seen to have a more important impact on the final result. As the output power increases, the overall soft-switching region narrows down drastically, with the converter actually being unstable in the dark blue region. Moreover, while switching losses are eliminated through soft-switching, due to the relatively low switching frequencies, conduction losses are still present and have a significant impact on the overall efficiency, especially in the low power region. That being said, the overall efficiency may seem unattractive but this is attributed mainly to a sub-optimal piezoelectric transformer design process. Finally, the overall performance of the proposed mixed-signal controller is independent of the obtained efficiency, as its dual capability of following changes in operation point and ensuring soft-switching is achieved.

V. Conclusion

General operation of a self-oscillating loop for piezoelectric transformer-based power converters was explained. The designed circuit for operating the transformer together with experimental results were provided. The circuit is based on a new idea for compensating and controlling the total loop phase shift for the self-oscillating PT loop through digital means, in order to achieve and maintain soft switching. This is combined with a resonance current estimation that is able to start and maintain the circuit oscillation. The operation of and cooperation between the analog resonance current estimator and digital phase shift adjustment were presented

in detail, together with some insight into the performance of the designed circuit. The concept was proven through experimental results. 45 ps time step resolution is deemed more than sufficient for adjusting the phase shift of the loop. The designed circuit is able to follow fine changes in the resonance frequency of the PT in every cycle. Experimental results show the proof of concept. Although this application is focused on PT-based power converters, the method has a general application and can potentially be used for other types of resonant converters. The main advantage is that the method implemented has flexibility for phase shift compensation, but the disadvantage is a complex control method.

ACKNOWLEDGMENT

The authors would like to thank Noliac A/S for supplying the prototype piezoelectric transformer.

REFERENCES

[1] M. Ekhtiari, T. Andersen, Z. Zhang, and M. A. E. Andersen, "Digitized self-oscillating loop for piezoelectric transformer-based power converters," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 1430–1436.

[2] Y. P. Liu, D. Vasic, F. Costa, and D. Schwander, "Piezoelectric 10w dc/dc converter for space applications," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Aug 2011, pp. 1–7.

[3] I. Kim, M. Kim, S. Jeong, J. Song, and V. V. Thang, "Piezotransformer with ring-dot-shape for easy heat radiation and high efficiency power," in *2011 International Symposium on Applications of Ferroelectrics (ISAF/PFM) and 2011 International Symposium on Piezoresponse Force Microscopy and Nanoscale Phenomena in Polar Materials*, July 2011, pp. 1–6.

[4] S. Lele, R. Sobot, and T. Sidhu, "Piezoelectric transformer based disturbance monitoring methodology for high-voltage power supply lines," *IEEE Sensors Journal*, vol. 14, no. 5, pp. 1425–1434, May 2014.

[5] R. L. Lin, F. C. Lee, E. M. Baker, and D. Y. Chen, "Inductor-less piezoelectric transformer electronic ballast for linear fluorescent lamp," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, vol. 2, 2001, pp. 664–669 vol.2.

[6] S. Bronstein and S. Ben-Yaakov, "Design considerations for achieving zvs in a half bridge inverter that drives a piezoelectric transformer with no series inductor," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, vol. 2, 2002, pp. 585–590 vol.2.

[7] M. Sanz, P. Alou, A. Soto, R. Prieto, J. A. Cobos, and J. Uceda, "Magnetic-less converter based on piezoelectric transformers for step-down dc/dc and low power application," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 2, Feb 2003, pp. 615–621 vol.2.

[8] E. L. Horsley, N. Nguyen-Quang, M. P. Foster, and D. A. Stone, "Achieving zvs in inductor-less half-bridge piezoelectric transformer based resonant converters," in *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Nov 2009, pp. 446–451.

[9] A. V. Carazo, "50 years of piezoelectric transformers. Trends in the technology," in *Symposium D Materials and Devices for Smart Systems*, ser. MRS Proceedings, vol. 785, 2003.

[10] E. M. Baker, W. Huang, D. Y. Chen, and F. C. Lee, "Radial mode piezoelectric transformer design for fluorescent lamp ballast applications," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1213–1220, Sept 2005.

[11] S. Ben-Yaakov and S. Lineykin, "Maximum power tracking of piezoelectric transformer hv converters under load variations," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 73–78, Jan 2006.

[12] J. Diaz, F. Nuno, M. J. Prieto, J. A. Martin-Ramos, and P. J. V. Saiz, "Closing a second feedback loop in a dc-dc converter based on a piezoelectric transformer," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2195–2201, Nov 2007.

[13] M. Ekhtiari, Z. Zhang, and M. A. E. Andersen, "State-of-the-art piezoelectric transformer-based switch mode power supplies," *40th Annual Conference of the IEEE Industrial Electronics Society, IECON2014*, pp. 5072–5078, in press, 2014.

[14] E. Horsley, M. Foster, and D. Stone, "State-of-the-art piezoelectric transformer technology," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–10.

[15] A. M. Flynn and S. R. Sanders, "Fundamental limits on energy transfer and circuit considerations for piezoelectric transformers," *Power Electronics, IEEE Transactions on*, vol. 17, no. 1, pp. 8–14, 2002.

[16] M. S. Rodgaard, "Piezoelectric transformer based power converters; design and control," *Ph.D. Thesis, Department of Electrical Engineering, Technical University of Denmark*, 2012.

[17] S. Bronstein, "Piezoelectric transformers in power electronics," Ph.D. dissertation, Ben-Gurion University of the Negev, 2005.

[18] A. M. Sánchez, M. Sanz, R. Prieto, J. A. Oliver, P. Alou, and J. A. Cobos, "Design of piezoelectric transformers for power converters by means of analytical and numerical methods," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 1, pp. 79–88, 2008.

[19] C. y. Lin, "Design and analysis of piezoelectric transformer converters," *PhD Dissertation, Virginia Tech*, 1997.

[20] M. Rodgaard, M. A. E. Andersen, T. Andersen, and K. Meyer, "Self-oscillating loop based piezoelectric power converter," *US patent 61/638,883 and WIPO, WO2013083678-A2*, 2011.

[21] M. S. Rodgaard, "Bi-directional piezoelectric transformer based converter for high-voltage capacitive applications," *30th Applied Power Electronics Conference and Exposition, 2015,Charlotte, NC*, 2015.

[22] J. Díaz, F. Nuño, J. M. Lopera, and J. A. Martín-Ramos, "A new control strategy for an ac/dc converter based on a piezoelectric transformer," *IEEE Transactions on Industrial Electronics*, pp. 850–856, 2004.

[23] T.-G. Zsurzsan, M. A. E. Andersen, Z. Zhang, and N. A. Andersen, "Investigating the electromechanical coupling in piezoelectric actuator drive motor under heavy load," *Proceedings of Ieee International Power Electronics and Application Conference and Exposition*, pp. 538–542, 2014.

[24] B. Putzeys, "Simple self-oscillating class D amplifier with full output filter control," *Audio Engineering Society - 118th Convention Spring Preprints 2005*, pp. 1908–1915, 2005.

[25] T. Andersen, M. A. Andersen, O. C. Thomsen, M. Foster, and D. Stone, "Nonlinear effects in piezoelectric transformers explained by thermal-electric model based on a hypothesis of self-heating," in *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2012, pp. 596–601.

[26] J. Alonso, C. Ordiz, and M. Dalla Costa, "A novel control method for piezoelectric-transformer based power supplies assuring zero-voltage-switching operation," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 3, pp. 1085–1089, March 2008.

[27] M. A. E. Andersen, K. Meyer, M. S. Rodgaard, and T. Andersen, "Piezoelectric power converter with bi-directional power transfer," *US patent 61/567,924 and 2013, WIPO, WO2013083679-A1*, 2011.

[28] T. Andersen, ThomasAnd Zsurzsan and M. Ekhtiari, "Resonant power converter comprising adaptive dead-time control," *WIPO, WO2017001184-A1*, 2015.

[29] H. Pinheiro, P. K. Jain, and G. Joos, "Self-sustained oscillating resonant converters operating above the resonant frequency," *IEEE Transactions on Power Electronics*, vol. 14, no. 5, pp. 803–815, Sep 1999.

[30] M. Ekhtiari, T. Andersen, M. A. E. Andersen, and Z. Zhang, "Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 783–793, Jan 2017.

[31] G. Ivensky, I. Zafrany, and S. Ben-Yaakov, "Generic operational characteristics of piezoelectric transformers," *Power Electronics, IEEE Transactions on*, vol. 17, no. 6, pp. 1049–1057, Nov 2002.

[32] A. V. Mezheritsky, "Quality factor concept in piezoceramic transformer performance description," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 53, no. 2, pp. 429–442, 2006.

[33] E. M. Syed, "Analysis and modeling of piezoelectric transformer," *M.Sc. Thesis, Department of Electrical and Computer Engineering, University of Toronto*, 2001.

[34] R. L. Lin, "Piezoelectric transformer characterization and application of electronic ballast," *Ph.D. Dissertation, Virginia Polytechnic Institute and State University*, 2001.

[35] K. Meyer, M. Andersen, and F. Jensen, "Parameterized analysis of zero voltage switching in resonant converters for optimal electrode layout of piezoelectric transformers," *Power Electronics Specialists Conference. PESC 2008. IEEE*, pp. 2543–2548, June 2008.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2771297, IEEE Transactions on Power Electronics

[36] M. Rodgaard, T. Andersen, and M. Andersen, "Empiric analysis of zero voltage switching in piezoelectric transformer based resonant converters," *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on*, p. 63, March 2012.

[37] T. Andersen, "Piezoelectric transformer based power supply for dielectric electro active polymers," *Ph.D. Thesis, Department of Electrical Engineering, Technical University of Denmark*, 2012.

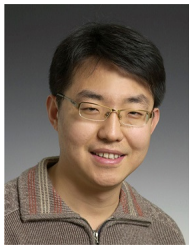
Marzieh Ekhtiari received the B.Sc. and M.Sc. degrees in electrical communication engineering from Shiraz University, Shiraz, Iran, in 2002 and 2005, respectively, and the Ph.D. degree in power electronics from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2015.

She is currently a Sr. Engineer in IC design verification. Her research interests include piezoelectric transformers, mixed-signal control, switch-mode power supplies, communication systems, integrated circuit design, and mixed-signal verification.

Gabriel Zsurzsan received the B.Sc. degree in applied electronics from the Polytechincal University of Timisoara, Timisoara, Romania, in 2010, the M.Sc. degree in automation and robotics and Ph.D. degree in power electronics from the Technical University of Denmark, Kgs. Lyngby, Denmark in 2013 and 2016, respectively.

He is currently a Postdoctoral Researcher at the Technical University of Denmark. From October 2014 to March 2015 he was with Tokyo University, Tokyo, Japan, as a visiting scholar. His research interests include resonant converters, mixed-signal control, switch-mode power supplies, piezoelectric actuators, sensors and transformers and permanent magnet motors.

Michael A.E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark, where since 2009, he has been the Deputy Head of the Department of Electrical Engineering. He is the author or coauthor of more than 300 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.



Zhe Zhang (M'11-SM'16) received the B.Sc. and M.Sc. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 2002 and 2005, respectively, and the PhD degree from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2010.

He is currently an Associate Professor in the Department of Electrical Engineering, at the Technical University of Denmark. From 2005 to 2007, he was an Assistant Professor at Yanshan University. From June 2010 to August 2010, he was with the University of California, Irvine, CA, USA, as a visiting scholar. He was a Postdoctoral Researcher in 2011 and Assistant Professor at the Technical University of Denmark during 2011 and 2014. He has authored or co-authored more than 100 transactions and international conference papers.

His current research interests include dc-dc converters, multiple-input dc-dc converters, soft-switching power converters and multi-level dc-ac inverters for renewable energy systems (RES), hybrid electric vehicles (HEV) and uninterruptable power supplies (UPS); piezoelectric-actuator and piezoelectric-transformer based power conversion systems.