A Low-cost Vector Network Analyzer: Design and Realization

J Verhaevert, P Van Torre

IDLab, Department of Information Technology, Ghent University-imec,
Technologiepark-Zwijnaarde 15, Ghent B-9052, Belgium, jo.verhaevert@ugent.be

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Abstract

In this paper, a low-cost Vector Network Analyzer (VNA) design is presented: from an initial study of network analysis fundamentals to a working design. In a first part of this paper, the architecture and functionality of a VNA are handled. The hardware components and their specifications are described. The design in this paper uses a Direct Digital Synthesizer (DDS) to generate signals. To measure phase and magnitude differences, integrated detectors are used. The design needs to be able to run embedded software in order to work. The programs, written in C code on an ARM processor, give the user the opportunity to set up the measurements using an LCD display, showing the results in a magnitude and phase plot or a Smith chart with a marker indication for reading out characteristics.

1 Introduction

Network analyzers can be split up in two main groups, Scalar Network Analyzers (SNA) and Vector Network Analyzers (VNA) [1]. The SNA is limited to measurements of the magnitude, where the VNA also measures phase shifts. This makes the VNA a more complex and hence more expensive device. The most expensive types also cover a large frequency range (from nearly DC to hundreds of GHz). In contrast, this paper is focused on a low-cost VNA by limiting the measured frequencies and by using low-cost components for its design and realization.

Network analysis requires 4 main parts: a signal generator, a Device Under Test (DUT), a way to measure signals and a form of signal processing and display. Signals are generated to excite the DUT, measuring the DUT's response. The output signals are interpreted and processed by a microcontroller and visualized on the LCD display in different graphs [1].

The rest of the paper is structured as follows. In section 2, the different main hardware components are explained, whereas section 3 handles the software. Results can be found in section 4. Section 5 presents the conclusions.

2 Hardware

The block diagram of the hardware is displayed in Fig. 1, showing both the functionality and the complete architecture of the design. The key components and their most important specifications will be explained further in this section. A Printed Circuit Board (PCB) was designed as an add-on module for the STM32F4 discovery board [2]. This PCB was finally realized (as illustrated in Fig. 2) and extensively tested. An overview of the system, with a Smith chart of the LCD screen, the ARM Discovery Board, and the plug in network analyzer PCB is displayed in Fig. 3.

2.1 Microcontroller interface

The add-on module relies on the STM32F4 Discovery Board to perform the processing and visualization of data and settings. This unit plugs onto the Discovery Board, connecting to the STM32F4 processors General Purpose Input-Output (GPIO) lines. By using a dual 25x2 pin header, the unit is plugged onto the discovery board in a mechanically robust way. An LCD display with touch screen is also connected to the STM32F4.

2.2 Generating signals

For generating the signals a Direct Digitale Synthesizer (DDS) [3] with an in-phase (I) and quadrature (Q) output signals is employed. Both output signals are low pass filtered and then used as reference signals for the RF detectors, as explained further. The Q output is also passed through a buffer amp and can be output through an SMA connector.

The AD9854 [4] is a DDS designed by Analog Devices. It supports I and Q outputs, having 90° phase difference. The internal clock frequency can be generated by multiplying the external 24 MHz clock signal. Since the chip only supports clock frequencies up to 200 MHz, a multiplication of 8 was used. Respecting the Nyquist theorem, output signals with frequencies of up to 40 % of this clock frequency, thus 80 MHz, are considered usable. Both outputs have their own 85 MHz low pass filter, suppressing the effects of aliasing and smoothening the square wave into a sine wave.

The buffer amp (AD8079 [5]) prevents the DUT from intensively loading the system. Since the buffer has a high input impedance, only a small current is taken from the input signal. The low output impedance insures that the DUT can easily excited by the system.

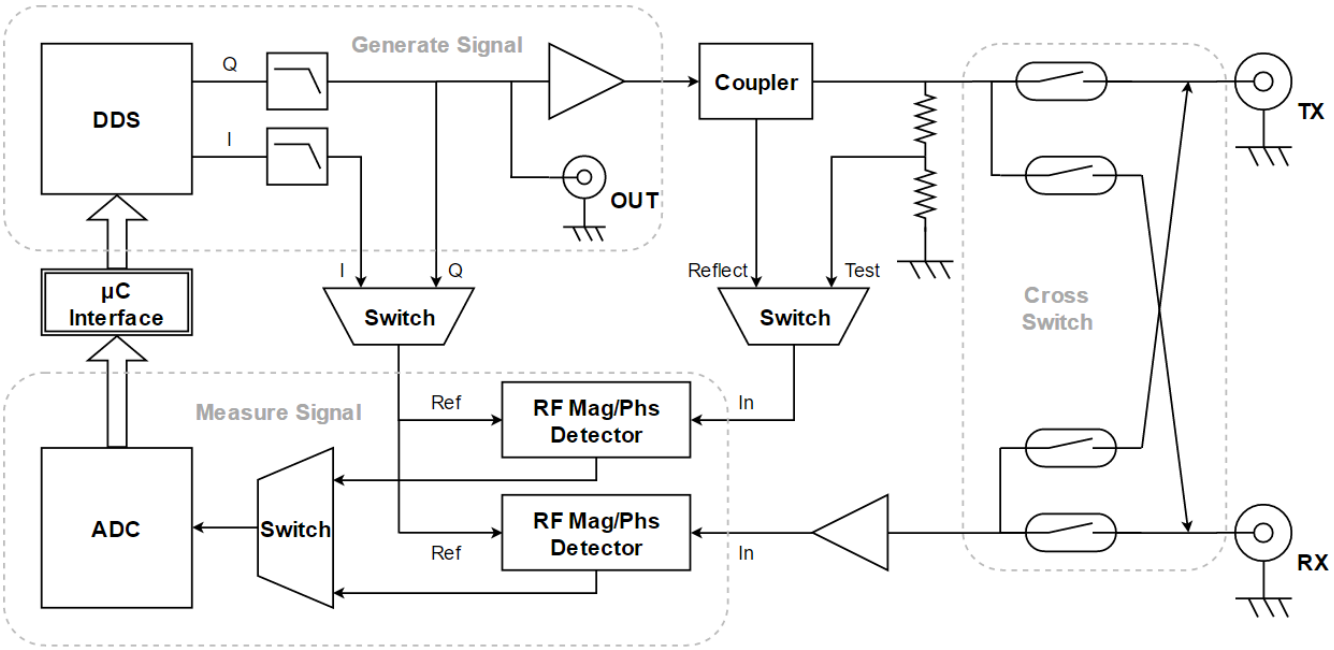

Fig. 1: Block diagram of the low-cost vector network analyzer.

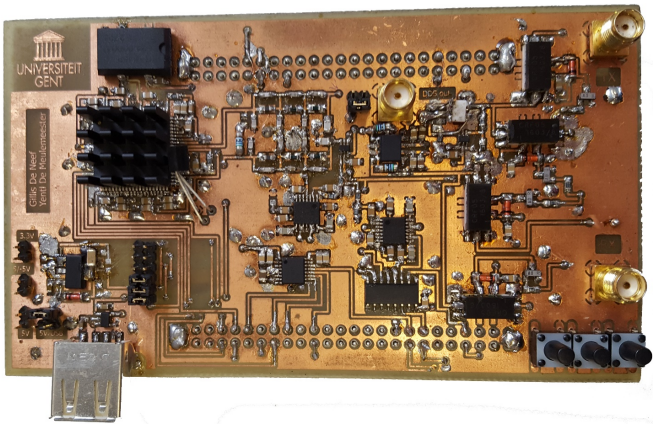

Fig. 2: PCB of the low-cost vector network analyzer.

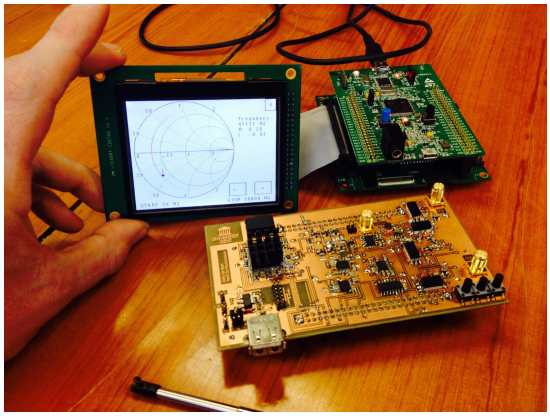

Fig. 3: Overview of a measurement on the LCD screen, the Discovery Board and the network analyzer PCB.

2.3 Directional coupler

A vector network analyzer measures both the transmission and reflection of a DUT. The transmitted signal can be measured at the RX port, whereas the reflected signal is measured at the TX port by using a directional coupler. The MACP-010507-CH0160 [6] allows the output signal to travel with minimal losses from the DDS to the TX port. Signals reflecting back into this port propagate to the coupled port of this passive component. Connecting the coupled port of the coupler to a second RF detector allows the system to measure reflected signals.

The voltage divider placed next to the directional coupler allows the user to connect a test signal to the detector for calibration purposes. This test signal has the same frequency as the output signal of the DDS, but the amplitude is scaled by a fixed factor. The measurement selection between voltage divider and reflection is implemented by an analog switch (FSA4157 [7]).

2.4 Measuring signals

Two AD8302 [8] detectors by Analog Devices are used to measure transmitted and reflected signals. The detectors measure the difference in phase and magnitude of an input signal compared to a reference signal. By using the DDS signals as reference, the output voltages of the detectors relate directly to the response of the DUT. The first output of the AD8302 is the phase output, a DC voltage in the range of 1.8 V (0°) to 0 V (180°) phase difference, scaled at 10 mV/°. The magnitude output is centered around 900 mV (0 dB) and supports a dynamic range of ±30 dB at 30 mV/dB.

Since the difference between positive and negative angles cannot be detected by the phase output, both the I and Q outputs

of the DDS are used as reference. The known $90°$ phase difference between I and Q can be used to determine the quadrant of the phase vector. Switching the reference signals is done by another FSA4157 switch, the same switch type as mentioned earlier.

Since every detector has 2 outputs and 2 detectors are used, 4 analog signals need to be converted to digital signals. These signals can then be read by the microcontroller and processed. Multi-channel ADCs are expensive, therefore a 4:1 analog switch (TS3A5017 [9]) was used to connect each output to the ADC. The ADS7229 [10] supports a 12-bit resolution and 1 Msps, which is more than fast enough to sample the DC values output by the detectors.

2.5 Cross switch

By measuring the transmitted and reflected waves, only 2 of the 4 S-parameters can be obtained: transmission is represented as S_{21} and reflection as S_{11}, the forward S-parameters. The reverse parameters, S_{12} and S_{22}, can be calculated by connecting the DUT the other way around, using the cross switch. This switch uses 4 Reed relays [11] (see also Fig. 1). When the outer relays are conducting and the inner are open, the forward S-parameters are measured. By opening the outer and closing the inner relays, the reverse S-parameters are measured.

3 Software

In order to develop the embedded software for the network analyzer, the CoIDE toolchain of CooCox was used [12]. The code was written to program the STM32F4 discovery board. The main tasks of the software are controlling the hardware components (such as the relays, switches, DDS and ADC) as well as interpreting instructions and visualizing the measurement results via the touchscreen. In the current version of the software an export of the measurement results is not included.

3.1 Menu structure

The menu contains buttons and input fields, to interact with the software. In the main menu, 5 buttons are used. With the first 2 buttons, a frequency range for transmission and reflection measurements can be set, resulting in a plot of attenuation and phase. The third button controls the function generator, generating sine waves with a frequency between 0 and 80 MHz. The fourth button results in the Smith chart, plotting the reflection coefficient as a function of the frequency, within the predefined frequency range. The fifth and last button is for calibration, explained further in this paper.

3.2 Coordinate system

For plotting, a coordinate system is used, where the grid divides the Y-axis in 10 divisions an the X-axis in 7 decades. This grid is also used to give a first visual interpretation of the phase and attenuation behavior. If more accurate information

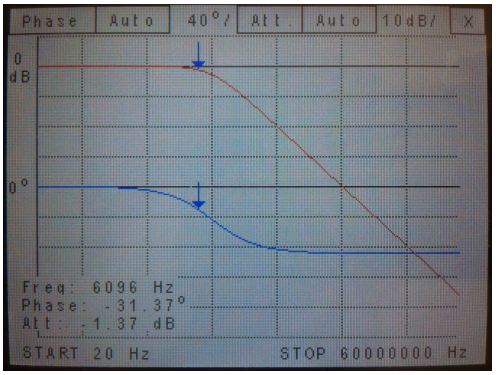

Fig. 4: Coordinate system with amplitude and phase plot.

is necessary, the marker function can be used, by touching the amplitude or phase graph at the region of interest. Then two marker arrows pop up as shown Fig. 4. One arrow denotes a point on the attenuation graph, while the other denotes the point on the phase graph at the same frequency. The phase and amplitude can be displayed or hidden independently of each other. Finally, an auto scale function was added to allow using the full size of the screen. An example of a amplitude and phase plot of a low pass filter is given in Fig. 4.

3.3 Smith chart

When the option Smith is chosen in the main menu, a frequency range can be set, visualizing the reflection coefficient S_{11} as a function of the frequency. The corresponding complex impedance and the exact on screen position is calculated. Because of the computationally intensive calculations for an embedded system, the complex impedance, the reflection coefficient and the on screen position are calculated once and stored in the memory of the microcontroller for future reference.

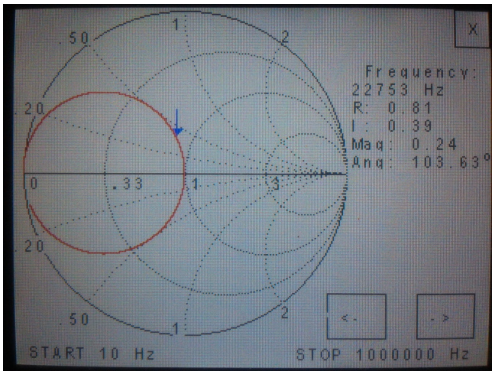

Fig. 5: The Smith chart.

The Smith Chart is also extended with a marker function. One of the 2 buttons next to the Smith chart is used to adjust the marker arrow to the place of interest. The frequency, complex impedance and reflection coefficient are retrieved from

the memory and shown next to the Smith Chart, as shown in Fig. 5.

3.4 Calibration

Three calibration methods are possible: Through, SOLT and detector calibration [13]. The Through calibration is implemented for transmission measurements and measures the values of attenuation and phase when a Through connection is connected between the connections of the reference plane. These values are subtracted from the amplitude and phase measurements in case of DUT connection. However, this calibration method requires a lot of memory use.

This problem can be solved by implementing SOLT calibration. It models the errors caused by the system and affecting the S-parameters [14]. The error model only takes 12 error terms into account, so only 12 variables should be stored.

The detector calibration is used to calibrate the detector for phase measurements. Therefore, an SMA cable with a fixed length is used [15], leading to linear phase changes as a function of frequency. This behavior is used to make an array with increasing voltages by linearly increasing the frequency. When the detector calibration is finished, the array of voltages can be used as a lookup table for the phase.

4 Results

In this section, measurement results for the low-cost vector network analyzer are discussed. A comparison was made between the results of the proposed network analyzer and a reference Rohde & Schwarz ZVRE [16].

4.1 Notch filters

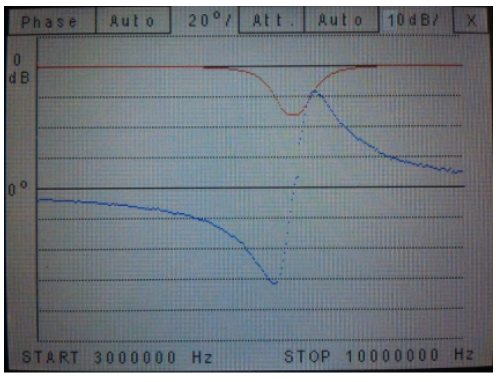

Fig. 6: 6 MHz notch filter with proposed design.

For transmission tests, 2 notch filters are designed and realized: one with a dip at 6.2 MHz, the other at 22 MHz. These filters are used as an accuracy test. Fig. 6 shows a picture of the phase and magnitude characteristics of the 6 MHz notch filter. Fig. 7 shows the response measured with the ZVRE. An attenuation of -16 dB occurs at 6.2 MHz. The phase drops to $-64°$, passes $0°$ at 6.2 MHz and then rises to $58°$. Similar results were obtained when measuring the filter with the low-cost vector network analyzer. The magnitude response closely matches that of the ZVRE. The phase has a slight offset of a couple degree. The 22 MHz filter showed similar results.

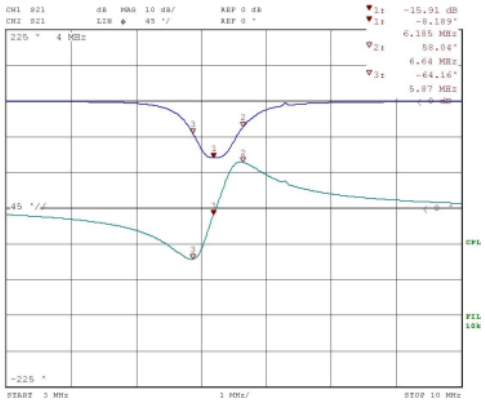

Fig. 7: 6 MHz notch filter with R & S ZVRE.

4.2 Coaxial cable

Fig. 8: 7.5 m coaxial cable with proposed design.

Coaxial cables have a constant group delay. Since this group delay is calculated by derivation of the phase to the frequency, it can be concluded that a linear phase shift occurs. By measuring a 7.5 m coaxial cable, a $360°$ phase shift can be measured. Fig. 8 uses $40°$/division scaling. The phase shifts from $+180°$ to $-180°$, resulting in full $360°$ phase measurement. Note that on first sight it does not appear to be linear. This is due to the fact that the frequency uses a logarithmic scale. The results can be compared with the measurements with R & S ZVRE of Fig. 9.

4.3 Attenuator

An external attenuator by Marconi Instruments was used to assess the magnitude range of the device. The dynamic range was theoretically predicted to be from 0 dBm to -50 dBm. Practical measurements showed that 0 dBm to -40 dBm is

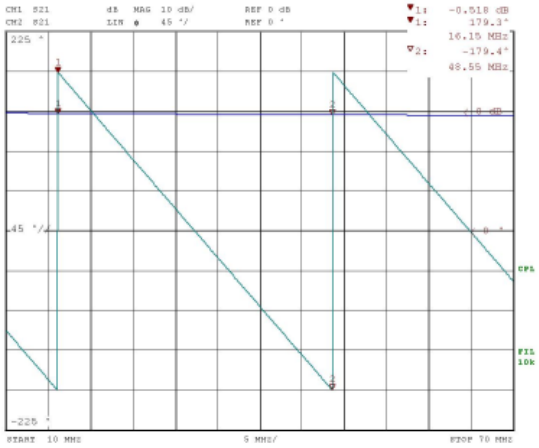

Fig. 9: 7.5 m coaxial cable with R & S ZVRE.

more realistic. The AD8302 detector also appears not to measure signals lower than -23 dB compared to the reference signal, possible because of limited signal coupling on the PCB.

5 Conclusions

In a first part of this paper, the design of a low-cost vector network analyzer was analyzed by explaining its functions and structure. The network analyzer employs an ARM Discovery Board with LCD tochscreen, with the designed and implemented network analyzer board pluggen onto it. After specifying all characteristics, the development of the PCB and the embedded software was documented. The results of the low-cost network analyzer were compared to the Rohde & Schwarz ZVRE, by means of a number of standard tests, employing a notch filters, a length of coaxial cable as well as a switchable attenuator. Although limited in amplitude and frequency range, the proposed design is fully functional, allowing with similar measurement results in the frequency range from 5 MHz to 80 MHz.

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References

[1] A. Estrada. "The vector network analyzer - an essential tool in modern ate measurements", *IEEE AUTOTESTCON*, Baltimore, MD, USA, pp. 16-21, (2011).

[2] ST Microelectronics. "STM32F4 Discovery Board", `www.st.com/resource/en/user_manual/dm00039084.pdf`.

[3] Y. Hang, K. Sun, Y. Liu, S. Zhu, X. Cheng. "A design and implementation of simple spectrum analyzer based on DDS", *3rd International Conference on Machinery, Materials and Information Technology Applications (ICMMITA2015)*,pp. 1257-1261 (2015).

[4] Analog Devices. AD9854, `http://www.analog.com/media/en/technical-documentation/data-sheets/AD9854.pdf`.

[5] Analog Devices. AD8079, `http://www.analog.com/media/en/technical-documentation/data-sheets/AD8079.pdf`.

[6] Macom. MACP-010507-CH0160, `http://cdn.macom.com/datasheets/MACP-010507-CH0160.pdf`.

[7] Fairchild. FSA4157, `http://www.farnell.com/datasheets/1811321.pdf`.

[8] Analog Devices. AD8302, `http://www.analog.com/media/cn/technical-documentation/evaluation-documentation/AD8302.pdf`.

[9] Texas Instruments. TS3A5017, `http://www.ti.com.cn/cn/lit/ds/symlink/ts3a5017.pdf`.

[10] Texas Instruments. ADS7229. `http://www.ti.com.cn/cn/lit/ds/symlink/ads7229.pdf`.

[11] Meder Electronics. CRF05-1A, `http://datasheet.octopart.com/CRF05-1A-MEDER-datasheet-5376852.pdf`.

[12] CooCox CoIDE, `http://www.coocox.org/software.html`.

[13] K. J. Silvonen. "A general approach to network analyzer calibration", *IEEE Transactions on Microwave Theory and Techniques*, **vol. 40, no. 4**, pp. 754-759, (1992).

[14] A. Henze, N. Tempone, G. Monasterios, H. Silva. "Incomplete 2-port vector network analyzer calibration methods", *IEEE Biennial Congress of Argentina (ARGENCON), Bariloche, Argentina*, pp. 810-815 (2014).

[15] B. De Mulder, K. Van Renterghem, E. De Backer, P. Suanet and J. Vandewege. "Java-enabled low cost RF vector network analyzer", *3rd International IEEE-NEWCAS Conference, Quebec, Canada*, pp. 377-380, (2005).

[16] Rohde & Schwarz ZVRE, `http://www.testequipmenthq.com/datasheets/Rohde-Schwarz-ZVRE-Datasheet.pdf`