

Passive loop filter assistance for CTSDMs

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Abstract

This paper presents a power reduction technique for continuous time sigma delta modulators (CTSDM). The approach consists of two elements. First, a passive low pass filter is added in front of the modulator's loop filter to reduce the high frequency components in the loop. As a result, the slew rate requirements of the opamps can be greatly reduced which allows a significant power saving. Unfortunately, the insertion of this low pass filter also changes the modulator's loop gain, and hence affects the NTF and STF (Noise- and Signal Transfer Functions), in an undesired way. Therefore, the second proposed element consists of inserting a compensation branch which is such that the original loop gain, NTF and STF are restored. Thanks to this, our power saving technique is completely transparent on the system level such that all established techniques and toolboxes for CTSDM design can still be used. The technique is especially suited for one-bit CTSDMs where the amount of high-frequency components in the loop is excessive. To showcase the technique, an SOSDM (which is a dedicated type of one-bit CTSDM) was implemented in a 65nm CMOS process. It achieves a peak SNDR of 63dB over a 20MHz bandwidth at a power consumption of 1.7mW while occupying a very small chip area of only 0.009 mm².

Index Terms

Analog-to-digital conversion, self-oscillating sigma delta modulator, pulse-width modulation, small area ADC, CTSDM, low power.

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